# BQ25853-Q1 Automotive Bidirectional Charge Controller for Backup Power

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 0: −40°C ≤ $T_A$ ≤ 150°C
- Wide input voltage operating range: 4.4V to 70V
- Wide output voltage operating range: up-to 70V supercapacitor charging
- Synchronous buck-boost controller with NFET drivers
  - Buck only mode configurable with MODE pin
  - Adjustable $f_{SW}$ from 200kHz to 600kHz
  - Switching frequency dithering for EMI noise reduction (DRSS)
  - Optional synchronization to external clock
  - Integrated loop compensation with soft start
  - Optional gate driver supply input for optimized efficiency
- Bidirectional converter operation to support autonomous backup mode with no $I^2C$ interactions
  - VREV_FB pin to program system voltage in reverse mode with resistor divider
  - ACUV pin to program reverse mode automatic entry/exit threshold
  - Adjustable output current regulation ($R_{BAT_SNS}$) up to 35A using 2.5mΩ resistor
- High accuracy
  - ±0.5% charge voltage regulation
  - ±3% charge/input current regulation
  - ±0.5% reverse mode voltage regulation
  - ±2% input voltage regulation
- $I^2C$ controlled for optimal system performance with resistor-programmable option
  - Hardware adjustable input and output current limits
- Integrated 16-bit ADC for voltage, current, and temperature monitoring
- High safety integration
  - Adjustable input over- and under-voltage protection
  - Overvoltage and overcurrent protection
  - Thermal shutdown
- Package
  - 36-pin 5mm × 6mm QFN with wettable flanks
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

## 2 Applications

- Low voltage battery system
- Battery management unit
- Domain Gateway
- ADAS Domain Controller
- Front Door Module

## 3 Description

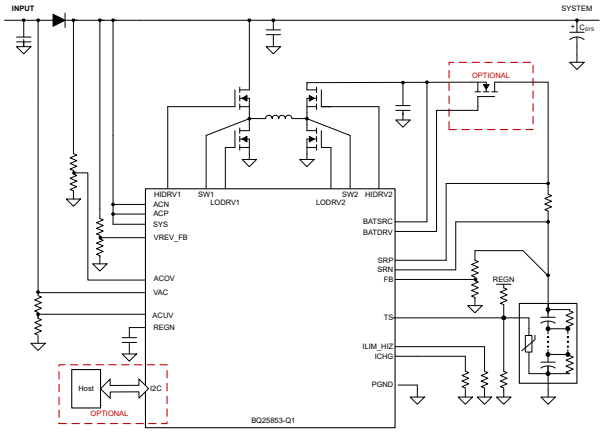
The BQ25853-Q1 is an automotive grade, wide input voltage, switched-mode buck-boost battery charge controller with bidirectional power flow support. The device offers high-efficiency supercapacitor charging over a wide voltage range with accurate charge current and charge voltage regulation. The device integrates all the loop compensation for the buck-boost converter, thereby providing a high density design with ease of use. In reverse mode, the device draws power from the supercapacitor and regulates the input terminal voltage with an added constant current loop for protection.

Besides the $I^2C$ host-controlled charging mode, the device also supports standalone charging mode via resistor programmable limits. Input current, charge current, charge voltage regulation, and reverse mode voltage regulation targets can be set via the ILIM_HIZ, ICHG, and FB pins, respectively.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM) |
|---|---|---|---|
| BQ25853-Q1 | VQFN (36) | 6.0mm × 5.0mm | 6.0mm × 5.0mm |

(1) For all available packages, see *Section 11*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**BQ25853-Q1 Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Device Comparison**....3
**5 Pin Configuration and Functions**....4
**6 Specifications**....7
6.1 Absolute Maximum Ratings....7
6.2 ESD Ratings....7
6.3 Recommended Operating Conditions....7
6.4 Thermal Information....8
6.5 Electrical Characteristics....9
6.6 Timing Requirements....15
6.7 Typical Characteristics....16
**7 Detailed Description**....17
7.1 Overview....17
7.2 Functional Block Diagram....18
7.3 Feature Description....19
7.4 Device Functional Modes....36
7.5 BQ25853Q1 Registers....38
**8 Application and Implementation**....63
8.1 Application Information....63
8.2 Typical Applications....63
8.3 Power Supply Recommendations....71
8.4 Layout....71
**9 Device and Documentation Support**....74
9.1 Device Support....74
9.2 Receiving Notification of Documentation Updates....74
9.3 Support Resources....74
9.4 Trademarks....74
9.5 Electrostatic Discharge Caution....74
9.6 Glossary....74
**10 Revision History**....75
**11 Mechanical, Packaging, and Orderable Information**....75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# 4 Device Comparison

| PART NUMBER | BQ25853Q1 | BQ25856Q1 | BQ25858Q1 |
|---|---|---|---|
| Key Feature | Supercap, automatic reverse mode, DRSS, TSHUT → 165C, automotive qualified | Li-Ion, LFP, DRSS, TSHUT → 165C, automotive qualified | Li-Ion, DRSS, TSHUT → 165C, automotive qualified |
| Topology | Buck-Boost charger | Buck-Boost charger | Buck-Boost controller |
| Power Topology | Non Power-Path | Non Power-Path | Non Power-Path |
| $I^2C$ Address | 0X6B | 0X6B | 0X6B |
| Default Charge Profile | CC/CV | Li-Ion (trickle, precharge, CC, CV) | CC/CV |
| Configuration | $I^2C$ + Standalone | $I^2C$ + Standalone | $I^2C$ + Standalone |
| Operating VIN | 4.4V → 70V | 4.4V → 70V | 4.4V → 70V |
| Reverse mode VAC program method | Resistor divider | $I^2C$ | $I^2C$ |
| Forward mode VOUT/ VREG program method | Resistor divider | Resistor divider | $I^2C$ |
| Pin Count | 36 | 36 | 36 |
| Package | 5×6 QFN | 5×6 QFN | 5×6 QFN |
| TS Pin Function | JEITA profile | JEITA profile | Disabled |

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# 5 Pin Configuration and Functions

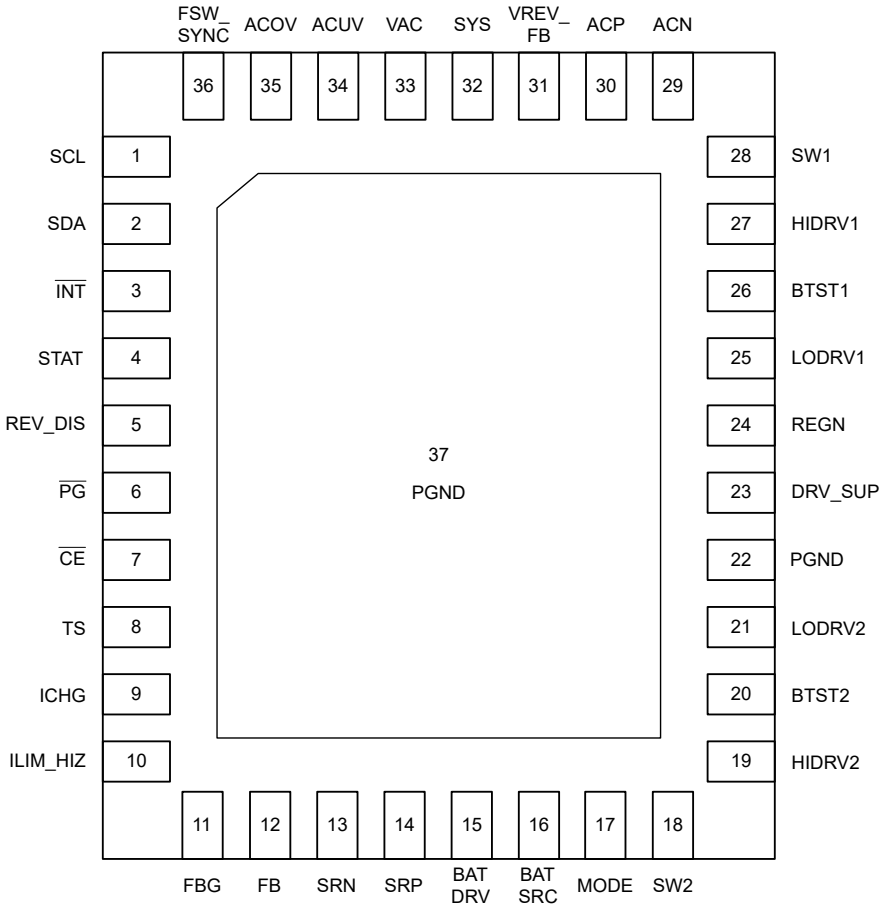


**Figure 5-1. BQ25853-Q1, RRV Package 36-Pin VQFN Top View**


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**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SCL | 1 | I | **I²C Interface Clock –** Connect SCL to the logic rail through a 10kΩ resistor. |
| SDA | 2 | IO | **I²C Interface Data –** Connect SDA to the logic rail through a 10kΩ resistor. |
| $\overline{INT}$ | 3 | O | **Open Drain Interrupt Output –** Connect the $\overline{INT}$ pin to a logic rail via 10kΩ resistor. The $\overline{INT}$ pin sends an active low, 256µs pulse to host to report the charger device status and faults. |
| STAT | 4 | O | **Open Drain Charge Status Output –** Connect to the pull up rail via 10kΩ resistor. The STAT pin function can be disabled when DIS_STAT_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT_ON bit. |
| REV_DIS | 5 | IO | **Reverse Disable -** External pin used to control entry and exit to reverse mode when valid input is not present. When pulled up, reverse mode is disabled which means that when the input voltage is not valid, the device does not automatically go into reverse mode. Pull down means reverse mode enabled. |
| $\overline{PG}$ | 6 | O | **Open Drain Active Low Power Good Indicator –** Connect to the pull up rail via 10kΩ resistor. LOW indicates a good input source if VAC is within the programmed ACUV / ACOV operating window. The $\overline{PG}$ pin function can be disabled when DIS_PG_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT3_ON bit. |
| $\overline{CE}$ | 7 | IO | **Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating. The $\overline{CE}$ pin function can be disabled when DIS_CE_PIN bit is set to 1. When disabled, this pin can be used as a general purpose indicator via the FORCE_STAT4_ON bit. |
| TS | 8 | I | **Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to PGND. Charge suspends when TS pin voltage is out of range. Recommend 103AT-2 10kΩ thermistor. |
| ICHG | 9 | I | **Charge Current Limit Setting –** ICHG pin sets the maximum charge current, and can be used to monitor the charge current. A programming resistor to PGND is used to set the charge current limit as $I_{CHG} = K_{ICHG} / R_{ICHG}$. When the device is under charge current regulation, the voltage at ICHG pin is $V_{REF_ICHG}$. When ICHG pin voltage is less than $V_{REF_ICHG}$, the actual charge current can be calculated as: $IBAT = K_{ICHG} \times V_{ICHG} / ( R_{ICHG} \times V_{REF_ICHG})$. The actual charge current limit is the lower of the limits set by ICHG pin or the ICHG_REG register bits. This pin function can be disabled when EN_ICHG_PIN bit is 0. If ICHG pin is not used, this pin must be pulled to PGND, do not leave floating. |
| ILIM_HIZ | 10 | I | **Input Current Limit Setting and HIZ Mode Control Pin –** ILIM_HIZ pin sets the maximum input current limit, can be used to monitor the input current and can be pulled HIGH to force device into HIZ mode. A programming resistor to PGND is used to set the input current limit as $I_{LIM} = K_{ILIM} / R_{ILIM}$. When the device is under input current regulation, the voltage at ILIM_HIZ pin is $V_{REF_ILIM}$. When ILIM_HIZ pin voltage is less than $V_{REF_ILIM}$, the actual input current can be calculated as: $IAC = K_{ILIM} \times V_{ILIM} / ( R_{ILIM} \times V_{REF_ILIM})$. The actual input current limit is the lower of the limits set by ILIM_HIZ pin or the IAC_DPM register bits. This pin function can be disabled when EN_ILIM_HIZ_PIN bit is 0. If ILIM_HIZ pin is not used, this pin must be pulled to PGND, do not leave floating. |
| FBG | 11 | I | **Voltage Feedback Divider Return –** Connect to the bottom of battery feedback resistor. When charging, this pin is driven to PGND internally. When input voltage is outside of the ACUV / ACOV operating window, this pin is high-impedance, minimizing battery leakage current. |
| FB | 12 | I | **Charge Voltage Analog Feedback Adjustment –** Connect the output of a resistive voltage divider from the battery terminals to this node to adjust the output battery regulation voltage. |
| SRN | 13 | I | **Charge Current-Sense Resistor, Negative Input –** A 0.47µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1µF ceramic capacitor is placed from the SRN pin to PGND for common-mode filtering. |
| SRP | 14 | I | **Charge Current-Sense Resistor, Positive Input –** A 0.47µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1µF ceramic capacitor is placed from the SRP pin to PGND for common-mode filtering. |
| BATDRV | 15 | O | **N-Channel Battery FET Gate Drive –** Connect directly to the BATFET gate. Pin drives the gate with 10V relative to BATSRC to turn on BATFET. |
| BATSRC | 16 | I | **N-Channel Battery FET Source -** Connect directly to the BATFET common source. |
| MODE | 17 | I | Connect a resistor from this pin to PGND to select between buck-boost or buck-only operation. Refer to Section 7.3.3.2 section for more details. |
| SW2 | 18 | P | **Boost Side Half Bridge Switching Node –** Connect to the source of boost HS FET and the drain of boost LS FET. Connect the inductor between SW1 and SW2. |
| HIDRV2 | 19 | O | **Boost Side High-Side Gate Driver –** Connect to the boost high-side N-channel MOSFET gate. |

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**Table 5-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BTST2 | 20 | P | **Boost Side High-Side Power MOSFET Gate Driver Power Supply –** Connect a 100nF capacitor between BTST2 and SW2 to provide bias to the high-side MOSFET gate driver. |
| LODRV2 | 21 | O | **Boost Side Low-Side Gate Driver –** Connect to the boost low-side N-channel MOSFET gate. |
| PGND | 22 | P | **Power Ground Return –** The high current ground connection for the low-side gate drivers. |
| DRV_SUP | 23 | P | **Charger Gate Drive Supply Input –** Voltage on this pin is used to drive the gates of buck-boost converter switching FET. Connect a 4.7µF ceramic capacitor from DRV_SUP to power ground. REGN LDO voltage can be used as the gate driver supply for all switching FETs by connecting REGN to DRV_SUP pin. In high-voltage applications, directly providing the DRV_SUP voltage with an external supply up to 12V is also possible to achieve higher switching efficiency. See Section 7.3.3.3 for more details. |
| REGN | 24 | P | **Charger Internal Linear Regulator Output –** Connect a 4.7µF ceramic capacitor from REGN to power ground. REGN LDO voltage can be used as the gate driver supply for all switching FETs by connecting REGN to DRV_SUP pin. In high-voltage applications, directly providing the DRV_SUP voltage with an external supply up to 12V is also possible to achieve higher switching efficiency. See Section 7.3.3.3 for more details. |
| LODRV1 | 25 | O | **Buck Side Low-Side Gate Driver –** Connect to the buck low-side N-channel MOSFET gate. |
| BTST1 | 26 | P | **Buck Side High-Side Power MOSFET Gate Driver Power Supply –** Connect a 100nF capacitor between BTST1 and SW1 to provide bias to the high-side MOSFET gate driver. |
| HIDRV1 | 27 | O | **Buck Side High-Side Gate Driver –** Connect to the buck high-side N-channel MOSFET gate. |
| SW1 | 28 | P | **Buck Side Half Bridge Switching Node –** Connect to the source of buck HS FET and the drain of buck LS FET. Connect the inductor between SW1 and SW2. |
| ACN | 29 | I | **Adapter Current-Sense Resistor, Negative Input –** A 0.47µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1µF ceramic capacitor is placed from the ACN pin to PGND for common-mode filtering. |
| ACP | 30 | I | **Adapter Current-Sense Resistor, Positive Input –** A 0.47µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1µF ceramic capacitor is placed from the ACP pin to PGND for common-mode filtering |
| VREV_FB | 31 | I | **Reverse Voltage Analog Feedback Adjustment –** Connect the output of a resistive voltage divider from system to this node to GND to adjust the reverse regulation voltage. |
| SYS | 32 | I | **System voltage sense point –** Sense point for system voltage. |
| VAC | 33 | P | **Input Voltage Detection and Power –** Connect a 1µF capacitor from pin to PGND. VAC pin is the input bias to power the IC. |
| ACUV | 34 | I | **AC Undervoltage Comparator Input –** Connect a resistor divider from VAC to PGND to program the undervoltage protection. When this pin falls below $V_{REF_ACUV}$, the device stops charging. The hardware limit for input voltage regulation reference is $V_{ACUV_DPM}$. The actual input voltage regulation is the higher of the pin-programmed value and the VAC_DPM register value. If ACUV programming is not used, pull this pin to VAC, do not leave floating. |
| ACOV | 35 | I | **AC Overvoltage Comparator Input –** Connect a resistor divider from VAC to PGND to program the overvoltage protection. When this pin rises above $V_{REF_ACOV}$, the device stops charging. If ACOV programming is not used, pull this pin to PGND, do not leave floating. |
| FSW_SYNC | 36 | I | **Switching Frequency and Synchronization Input –** An external resistor is connected to the FSW_SYNC pin and PGND to set the nominal switching frequency. This pin can also be used to synchronize the PWM controller to an external clock with 200kHz to 600kHz frequency. |
| Thermal Pad | 37 | P | **Exposed pad beneath the IC –** Always solder the thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter. This also serves as a thermal pad to dissipate the heat. |

(1) I = Input; O = Output; I/O = Input or Output; P = Power, AI = Analog Input; AO = Analog Output; DAI = Digital or Analog Input; DI = Digital Output; DO = Digital Output; DIO = Digital Input or Output


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | VAC, ACUV, ACOV, ACP, ACN, SYS, SRP, SRN, FB, FBG, VREV_FB, BATDRV, BATSRC | –0.3 | 85 | V |
| Voltage | SW1, SW2 | –2 | 85 | V |
| Voltage | SW1, SW2 (40ns transient) | –4 | 85 | V |
| Voltage | $\overline{PG}$ | –0.3 | 40 | V |
| Voltage | BATDRV with respect to BATSRC | -0.3 | 12 | V |
| Voltage | BTST1, HIDRV1 with respect to SW1 | –0.3 | 14 | V |
| Voltage | BTST2, HIDRV2 with respect to SW2 | –0.3 | 14 | V |
| Voltage | DRV_SUP, LODRV1, LODRV2 | –0.3 | 14 | V |
| Voltage | ACP with respect to ACN, SRP with respect to SRN | –0.3 | 0.3 | V |
| Voltage | $\overline{CE}$, FSW_SYNC, ICHG, ILIM_HIZ, $\overline{INT}$, REGN, SCL, SDA, MODE, STAT, REV_DIS, TS | –0.3 | 6 | V |
| Output Sink Current | $\overline{CE}$, $\overline{PG}$, STAT, REV_DIS | | 5 | mA |
| $T_J$ | Junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins | ±750 | |
| | | | All pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{AC}$ | Input voltage | 4.4 | | 70 | V |
| $V_{BAT}$ | Battery voltage | 0 | | 70 | V |
| $V_{DRV_SUP}$ | DRV_SUP pin direct drive voltage range | 4.0 | | 12 | V |
| $F_{SW}$ | Switching Frequency | 200 | | 600 | kHz |
| $C_{VAC}$ | VAC capacitor | 1 | | | µF |
| $C_{IN}$ | Buck-boost input capacitance (minimum value after derating) | 80 | | | µF |
| $C_{REGN}$ | REGN capacitor (nominal value before derating) | 4.7 | | | µF |
| $C_{DRV_SUP}$ | DRV_SUP capacitor (nominal value before derating) | 4.7 | | | µF |
| L | Switched Inductor | 2.2 | | 15 | µH |
| $R_{DCR}$ | Inductor DC resistance | 1.75 | | 60 | mΩ |
| $R_{AC_SNS}$ | Input current sense resistor | 0(1) | 5 | 10 | mΩ |
| $R_{BAT_SNS}$ | Battery current sense resistor | | 2.5 | | mΩ |
| $R_{ICHG}$ | ICHG programming pulldown resistor | 0.0(2) | | 100 | kΩ |

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over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{ILIM_HIZ}$ | ILIM_HIZ programming pulldown resistor | 0.0(3) | | 50 | kΩ |
| $T_J$ | Operating junction temperature(4) | –40 | | 150 | °C |

(1) When $R_{AC_SNS}$ is 0mΩ, input current limit function is disabled
(2) When $R_{ICHG}$ is pulled to GND, the hardware charge current limit is disabled, actual charge current is controlled by the ICHG_REG register setting
(3) When $R_{ILIM_HIZ}$ is pulled to GND, the hardware input current limit is disabled, actual input current is controlled by the IAC_DPM register setting
(4) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperature greater than 125°C

## 6.4 Thermal Information

| THERMAL METRIC(1) | | BQ25853-Q1 RRV 36 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (JEDEC(1)) | 29.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 19.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 10.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 10.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.


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## 6.5 Electrical Characteristics

VAC = ACP = ACN = SYS = SRP = SRN = 28V, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **QUIESCENT CURRENTS** | | | | | | |
| $I_{SD_BAT}$ | Shutdown battery current with BATFET off ($I_{SRN}$ + $I_{SRP}$) | $V_{BAT}$ = 12V, VAC = 0V, ADC_EN = 0, FORCE_BATFET_OFF = 1, $T_J$ < 105 °C | | 10 | | µA |
| $I_{Q_BAT}$ | Quiescent battery current with BATFET on ($I_{SRN}$ + $I_{SRP}$) | $V_{BAT}$ = 12V, VAC = 0V, ADC_EN = 0, $T_J$ < 105 °C | | 17 | | µA |
| | | $V_{BAT}$ = 12V, VAC = 0V, ADC_EN = 1, $T_J$ < 105 °C | | 500 | 700 | µA |
| $I_{Q_VAC}$ | Quiescent input current ($I_{VAC}$) | Not switching | | 0.75 | 1 | mA |
| $I_{Q_REV}$ | Quiescent battery current in Reverse mode ($I_{SRN}$ + $I_{SRP}$) | Not switching | | 0.75 | 1 | mA |
| **VAC / BAT POWER UP** | | | | | | |
| $V_{VAC_OP}$ | VAC operating range | | 4.4 | | 70 | V |
| $V_{VAC_OK}$ | VAC converter enable threshold | VAC rising, no battery | 4.4 | | | V |
| $V_{VAC_OKZ}$ | VAC converter disable threshold | VAC falling, no battery | | | 3.5 | V |
| $V_{REF_ACUV}$ | ACUV comparator threshold to enter VAC_UVP | $V_{ACUV}$ falling | 1.089 | 1.1 | 1.108 | V |
| $V_{REF_ACUV_HYS}$ | ACUV comparator threshold hysteresis | $V_{ACUV}$ rising | | 50 | | mV |
| $V_{VAC_INT_OV}$ | VAC internal threshold to enter VAC_OVP | IN rising | 72 | 74 | 76 | V |
| $V_{VAC_INT_OVZ}$ | VAC internal thresholds to exit VAC_OVP | IN falling | 69 | 71 | 73 | V |
| $V_{REF_ACOV}$ | ACOV comparator threshold to enter VAC_OVP | $V_{ACOV}$ rising | 1.184 | 1.2 | 1.206 | V |
| $V_{REF_ACOV_HYS}$ | ACOV comparator threshold hysteresis | $V_{ACOV}$ falling | | 50 | | mV |
| $V_{SRN_OK}$ | Battery voltage to enable BATFET | $V_{SRN}$ rising, no input | | | 3.1 | V |
| $V_{SRN_OKZ}$ | Battery voltage to disable BATFET | $V_{SRN}$ falling, no input | 2.15 | | 2.65 | V |
| **CHARGE VOLTAGE REGULATION** | | | | | | |
| $V_{VFB_RANGE}$ | Feedback voltage range | | 1.504 | | 1.566 | V |
| $V_{VFB_STEP}$ | Typical feedback voltage step | | | 2 | | mV |
| $V_{VFB_NOM}$ | Nominal feedback voltage | VFB_REG = 0x10 | | 1.536 | | V |
| $V_{VFB_ACC}$ | Feedback voltage regulation accuracy | $T_J$ = 0°C to 85°C | –0.5 | | 0.5 | % |
| | | $T_J$ = -40°C to 125°C | –0.7 | | 0.7 | % |
| $I_{FB}$ | Leakage current into FB pin | | | | 100 | nA |
| $R_{FBG}$ | FBG resistance to PGND | $I_{FBG}$ = 1mA | | 33 | 55 | Ω |
| **FAST CHARGECURRENT REGULATION** | | | | | | |
| $I_{CHG_REG_RANGE}$ | Charge current regulation range | $R_{BAT_SNS}$ = 2.5mΩ | 0.8 | | 35 | A |
| $I_{CHG_REG_STEP}$ | Charge current regulation step | | | 100 | | mA |
| $I_{CHG_REG_ACC}$ | $I^2C$ setting charge current regulation accuracy | $R_{BAT_SNS}$ = 2.5mΩ, VBAT = 12V, 36V, 55V. ICHG_REG = 0x012C | | 30 | | A |
| | | | –3 | | 3 | % |
| | | $R_{BAT_SNS}$ = 2.5mΩ, VBAT = 12V, 36V, 55V. ICHG_REG = 0x0064 | | 10 | | A |
| | | | –3 | | 3 | % |
| | | $R_{BAT_SNS}$ = 2.5mΩ, VBAT = 12V, 36V, 55V. ICHG_REG = 0x0028 | | 4 | | A |
| | | | –5 | | 5 | % |

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VAC = ACP = ACN = SYS = SRP = SRN = 28V, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $K_{ICHG}$ | Hardware charge current limit set factor (Amperes of charge current per kΩ on ICHG pin) | $R_{BAT_SNS}$ = 2.5mΩ, $R_{ICHG}$ = 10kΩ, 5kΩ, and 3.33kΩ | 96 | 100 | 104 | A × kΩ |
| $V_{REF_ICHG}$ | ICHG pin voltage when ICHG pin is in regulation | | | 2.0 | | V |
| **INPUT CURRENT REGULATION** | | | | | | |
| $I_{IREG_DPM_ACC}$ | I²C setting input current regulation accuracy in forward mode | $R_{AC_SNS}$ = 2mΩ, IAC_DPM = 0x00A0 | | 20 | | A |
| | | | –3 | | 3 | % |
| | | $R_{AC_SNS}$ = 2mΩ, IAC_DPM = 0x0050 | | 10 | | A |
| | | | –4 | | 4 | % |
| | | $R_{AC_SNS}$ = 2mΩ, IAC_DPM = 0x0028 | | 5.0 | | A |
| | | | –7 | | 7 | % |
| $K_{ILIM}$ | Hardware input current limit set factor (Amperes of input current per kΩ on ILIM_HIZ pin) | $R_{AC_SNS}$ = 2mΩ, $R_{ILIM}$ = 5kΩ, 2.5kΩ, and 1.67kΩ | 48 | 50 | 52 | A × kΩ |
| $V_{REF_ILIM_HIZ}$ | ILIM_HIZ pin voltage when ILIM_HIZ pin is in regulation | | | 2.0 | | V |
| $V_{IH_ILIM_HIZ}$ | ILIM_HIZ input high threshold to enter HIZ mode | $V_{ILIM_HIZ}$ rising | 3.7 | | | V |
| **INPUT VOLTAGE REGULATION** | | | | | | |
| $V_{VREG_DPM_RANGE}$ | Input voltage DPM regulation range | | 4.4 | | 70 | V |
| $V_{VREG_DPM_ACC}$ | I²C setting input voltage regulation accuracy | VAC_DPM = 0x076C | | 38 | | V |
| | | | –2 | | 2 | % |
| $V_{VREG_DPM_ACC}$ | I²C setting input voltage regulation accuracy in forward mode | VAC_DPM = 0x04E2 | | 25 | | V |
| | | | –2 | | 2 | % |
| | | VAC_DPM = 0x03B6 | | 19 | | V |
| | | | –2 | | 2 | % |
| $V_{ACUV_DPM}$ | ACUV pin voltage when in VDPM regulation | | 1.188 | 1.2 | 1.212 | V |
| **REVERSE MODE VOLTAGE REGULATION** | | | | | | |
| $V_{REVFB_RANGE}$ | Reverse Mode feedback voltage range | | 1.504 | | 1.566 | V |
| $V_{REVFB_STEP}$ | Reverse mode typical feedback voltage step | | | 20 | | mV |
| $V_{REVFB_NOM}$ | Reverse mode nominal feedback voltage | VFB_REG = 0x10 | | 1.536 | | V |
| $V_{REVFB_ACC}$ | Reverse mode feedback voltage accuracy | TJ = 0℃ to 85℃ | –0.5 | | 0.5 | % |
| | | TJ = –40℃ to 125℃ | –0.7 | | 0.7 | % |
| **REVERSE MODE CURRENT REGULATION** | | | | | | |
| $I_{IREV_ACC}$ | Input current regulation accuracy in Reverse mode | $R_{AC_SNS}$ = 2mΩ, IAC_REV = 0x00A0 | | 20 | | A |
| | | | –3.5 | | 3.5 | % |
| | | $R_{AC_SNS}$ = 2mΩ, IAC_REV = 0x0028 | | 5.0 | | A |
| | | | –5.5 | | 5.5 | % |
| **CHARGE MODE BATTERY-PACK NTC MONITOR** | | | | | | |
| $V_{T1_RISE}$ | TS pin voltage rising T1 threshold, charge suspended above this voltage. | As Percentage to REGN, TS_T1=0°C with 103AT | 72.75 | 73.25 | 73.85 | % |
| $V_{T1_RISE}$ | TS pin voltage rising T1 threshold, charge suspended above this voltage. (SPEC only) | As Percentage to REGN, TS_T1=-10°C with 103AT | 76.65 | 77.15 | 77.65 | % |


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VAC = ACP = ACN = SYS = SRP = SRN = 28V, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T1_FALL}$ | TS pin voltage falling T1 threshold, charge re-enabled below this voltage. | As Percentage to REGN, TS_T1=0°C with 103AT | 71.5 | 72 | 72.5 | % |
| $V_{T1_FALL}$ | TS pin voltage falling T1 threshold, charge re-enabled below this voltage. (SPEC only) | As Percentage to REGN, TS_T1=-10°C with 103AT | 75.5 | 76.1 | 76.6 | % |
| $V_{T2_RISE}$ | TS pin voltage rising T2 threshold, charge back to reduced ICHG above this voltage | As Percentage to REGN, TS_T2=5°C with 103AT | 70.38 | 70.88 | 71.38 | % |
| $V_{T2_RISE}$ | TS pin voltage rising T2 threshold, charge back to reduced ICHG above this voltage | As Percentage to REGN, TS_T2=10°C with 103AT | 67.75 | 68.25 | 68.75 | % |
| $V_{T2_RISE}$ | TS pin voltage rising T2 threshold, charge back to reduced ICHG above this voltage (SPEC only) | As Percentage to REGN, TS_T2=15°C with 103AT | 64.85 | 65.35 | 65.85 | % |
| $V_{T2_RISE}$ | TS pin voltage rising T2 threshold, charge back to reduced ICHG above this voltage (SPEC only) | As Percentage to REGN, TS_T2=20°C with 103AT | 61.75 | 62.25 | 62.75 | % |
| $V_{T2_FALL}$ | TS pin voltage falling T2 threshold. Charge back to normal below this voltage | As Percentage to REGN, TS_T2=5°C with 103AT | 69.1 | 69.8 | 70.5 | % |
| $V_{T2_FALL}$ | TS pin voltage falling T2 threshold. Charge back to normal below this voltage | As Percentage to REGN, TS_T2=10°C with 103AT | 66.45 | 66.95 | 67.45 | % |
| $V_{T2_FALL}$ | TS pin voltage falling T2 threshold. Charge back to normal below this voltage (SPEC only) | As Percentage to REGN, TS_T2=15°C with 103AT | 63.6 | 64.2 | 64.6 | % |
| $V_{T2_FALL}$ | TS pin voltage falling T2 threshold. Charge back to normal below this voltage (SPEC only) | As Percentage to REGN, TS_T2=20°C with 103AT | 60.5 | 61.1 | 61.6 | % |
| $V_{T3_FALL}$ | TS pin voltage falling T3 threshold, charge to ICHG and reduced $V_{FB_REG}$ below this voltage. | As Percentage to REGN, TS_T3=40°C with 103AT | 47.9 | 48.4 | 48.9 | % |
| $V_{T3_FALL}$ | TS pin voltage falling T3 threshold, charge to ICHG and reduced $V_{FB_REG}$ below this voltage. | As Percentage to REGN, TS_T3=45°C with 103AT | 44.25 | 44.75 | 45.25 | % |
| $V_{T3_FALL}$ | TS pin voltage falling T3 threshold, charge to ICHG and reduced $V_{FB_REG}$ below this voltage. (SPEC only) | As Percentage to REGN, TS_T3=50°C with 103AT | 40.7 | 41.2 | 41.7 | % |
| $V_{T3_FALL}$ | TS pin voltage falling T3 threshold, charge to ICHG and reduced $V_{FB_REG}$ below this voltage. (SPEC only) | As Percentage to REGN, TS_T3=55°C with 103AT | 37.2 | 37.7 | 38.2 | % |
| $V_{T3_RISE}$ | TS pin voltage rising T3 threshold. Charge back to normal above this voltage. | As Percentage to REGN, TS_T3=40°C with 103AT | 49.2 | 49.7 | 50.2 | % |
| $V_{T3_RISE}$ | TS pin voltage rising T3 threshold. Charge back to normal above this voltage. | As Percentage to REGN, TS_T3=45°C with 103AT | 45.55 | 46.05 | 46.55 | % |
| $V_{T3_RISE}$ | TS pin voltage rising T3 threshold. Charge back to normal above this voltage. (SPEC only) | As Percentage to REGN, TS_T3=50°C with 103AT | 42.0 | 42.5 | 43.0 | % |
| $V_{T3_RISE}$ | TS pin voltage rising T3 threshold. Charge back to normal above this voltage. (SPEC only) | As Percentage to REGN, TS_T3=55°C with 103AT | 38.5 | 39 | 39.95 | % |
| $V_{T5_FALL}$ | TS pin voltage falling T5 threshold, charge suspended below this voltage | As Percentage to REGN, TS_T5=60°C with 103AT | 33.875 | 34.375 | 34.875 | % |

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| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T5_FALL}$ | TS pin voltage falling T5 threshold, charge suspended below this voltage (SPEC only) | As Percentage to REGN, TS_T5=65°C with 103AT | 30.75 | 31.25 | 31.75 | % |
| $V_{T5_RISE}$ | TS pin voltage rising T5 threshold. Charge back to ICHG and reduced $V_{FB_REG}$ above this voltage. | As Percentage to REGN, TS_T5=60°C with 103AT | 35 | 35.5 | 36 | % |
| $V_{T5_RISE}$ | TS pin voltage rising T5 threshold. Charge back to ICHG and reduced $V_{FB_REG}$ above this voltage. (SPEC only) | As Percentage to REGN, TS_T5=65°C with 103AT | 32.0 | 32.5 | 33.0 | % |
| **REVERSE MODE BATTERY-PACK NTC MONITOR** | | | | | | |
| $V_{BCOLD_RISE}$ | TS pin voltage rising TCOLD threshold. Reverse mode suspended above this voltage | As Percentage to REGN (BCOLD = –20°C with 103AT) | 79.45 | 80.0 | 80.55 | % |
| $V_{BCOLD_RISE}$ | TS pin voltage rising TCOLD threshold. Reverse mode suspended above this voltage | As Percentage to REGN (BCOLD = –10°C with 103AT) | 76.65 | 77.15 | 77.65 | % |
| $V_{BCOLD_FALL}$ | TCOLD comparator falling threshold. | As Percentage to REGN (–20°C with 103AT) | 78.2 | 78.7 | 79.2 | % |
| $V_{BCOLD_FALL}$ | TCOLD comparator falling threshold. | As Percentage to REGN (–10°C with 103AT) | 75.5 | 75.6 | 76.5 | % |
| $V_{BHOT_FALL}$ | TS pin voltage falling THOT threshold. Reverse mode suspends below this voltage | As Percentage to REGN, (BHOT = 55°C with 103AT) | 37.2 | 37.7 | 38.2 | % |
| $V_{BHOT_FALL}$ | TS pin voltage falling THOT threshold. Reverse mode suspends below this voltage | As Percentage to REGN, (BHOT = 60°C with 103AT) | 33.875 | 34.375 | 34.875 | % |
| $V_{BHOT_FALL}$ | TS pin voltage falling THOT threshold. Reverse mode suspends below this voltage | As Percentage to REGN, (BHOT 65°C with 103AT) | 30.75 | 31.25 | 31.75 | % |
| $V_{BHOT_RISE}$ | TS pin voltage rising THOT threshold. Reverse mode allowed above this voltage | As Percentage to REGN, (BHOT = 55°C with 103AT) | 38.5 | 39.0 | 39.95 | % |
| $V_{BHOT_RISE}$ | TS pin voltage rising THOT threshold. Reverse mode allowed above this voltage | As Percentage to REGN, (BHOT = 60°C with 103AT) | 35 | 35.5 | 36 | % |
| $V_{BHOT_RISE}$ | TS pin voltage rising THOT threshold. Reverse mode allowed above this voltage | As Percentage to REGN, (BHOT 65°C with 103AT) | 32.0 | 32.5 | 33.0 | % |
| **BATTERY CHARGER PROTECTION** | | | | | | |
| $V_{ICHG_OC}$ | Battery over-current threshold to latch off BATFET and converter (toggle FWD_DIS pin to restart operation) | $\lvert V_{SRP} - V_{SRN} \rvert$ rising (monitors current in both forward and reverse directions) | 120 | | 170 | mV |
| **REVERSE MODE PROTECTION** | | | | | | |
| $V_{REV_OV}$ | Reverse mode overvoltage threshold to suspend converter | $V_{VREV_FB}$ rising, as percentage of VREVFB_NOM | | 120 | | % |
| $V_{REV_OVZ}$ | Reverse mode overvoltage falling threshold to resume converter | $V_{VREV_FB}$ falling, as percentage of VREVFB_NOM | | 107 | | % |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SHUT}$ | Thermal shutdown rising threshold | Temperature increasing | | 165 | | °C |
| | Thermal shutdown falling threshold | Temperature decreasing | | 150 | | °C |
| **REGN REGULATOR AND GATE DRIVE SUPPLY (DRV_SUP)** | | | | | | |


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VAC = ACP = ACN = SYS = SRP = SRN = 28V, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REGN}$ | REGN LDO output voltage | IREGN = 20mA | 4.8 | 5 | 5.2 | V |
| | | VAC = 5V, IREGN = 20mA | 4.35 | 4.6 | | V |
| $I_{REGN}$ | REGN LDO current limit | VREGN = 4.5V | 70 | | | mA |
| $V_{REGN_OK}$ | REGN OK threshold to allow switching | REGN rising | | 3.55 | | V |
| $V_{DRV_UVPZ}$ | DRV_SUP under-voltage threshold to allow switching | DRV_SUP rising | | | 3.7 | V |
| $V_{DRV_OVP}$ | DRV_SUP over-voltage threshold to disable switching | DRV_SUP rising | 12.8 | 13.2 | 13.6 | V |
| **POWER-PATH MANAGER** | | | | | | |
| $V_{BATDRV_REG}$ | BATFET drive voltage | $V_{BATDRV}$ - $V_{BATSRC}$, VAC = 0V, $I_{BATDRV}$ = 10µA | | 10 | | V |
| $V_{BATDRV_REG}$ | BATFET reduced drive voltage | $V_{BATDRV}$ - $V_{BATSRC}$, VAC = 0V, $I_{BATDRV}$ = 10µA, PWRPATH_REDUCE_VDRV = 1 | | 7 | | V |
| $I_{BATDRV_REG}$ | BATFET charge pump current limit | $V_{BATDRV}$ - $V_{BATSRC}$ = 5V, VAC = 0V | | 40 | | µA |
| $I_{BATDRV_OFF}$ | BATFET turnoff current | | | 400 | | µA |
| $I_{AC_LOAD}$ | VAC discharge load current | | 16 | | | mA |
| $I_{BAT_LOAD}$ | Battery (SRP) discharge load current | | 16 | | | mA |
| **SWITCHING FREQUENCY AND SYNC** | | | | | | |
| $f_{SW}$ | Switching Frequency | $R_{FSW_SYNC}$ = 133kΩ | 212 | 250 | 288 | kHz |
| | | $R_{FSW_SYNC}$ = 50kΩ | 425 | 500 | 575 | kHz |
| $V_{IH_SYNC}$ | FSW_SYNC input high threshold | | 1.3 | | | V |
| $V_{IL_SYNC}$ | FSW_SYNC input low threshold | | | | 0.4 | V |
| $PW_{SYNC}$ | FSW_SYNC input pulse width | | 80 | | | ns |
| **PWM DRIVERS** | | | | | | |
| $R_{HIDRV1_ON}$ | Buck side high-side turnon resistance | $V_{BTST1}$ - $V_{SW1}$ = 5V | | 3.4 | | Ω |
| $R_{HIDRV1_OFF}$ | Buck side high-side turnoff resistance | $V_{BTST1}$ - $V_{SW1}$ = 5V | | 1.0 | | Ω |
| $V_{BTST1_REFRESH}$ | Bootstrap refresh comparator threshold voltage | BTST1 falling, $V_{BTST1}$ - $V_{SW1}$ when low-side refresh pulse is requested | 2.7 | 3.1 | 3.9 | V |
| $R_{LODRV1_ON}$ | Buck side low-side turnon resistance | VREGN = 5V | | 3.4 | | Ω |
| $R_{LODRV1_OFF}$ | Buck side low-side turnoff resistance | VREGN = 5V | | 1.0 | | Ω |
| $t_{DT1}$ | Buck side dead time, both edges | | | 45 | | ns |
| $R_{HIDRV2_ON}$ | Boost side high-side turnon resistance | $V_{BTST2}$ - $V_{SW2}$ = 5V | | 3.4 | | Ω |
| $R_{HIDRV2_OFF}$ | Boost side high-side turnoff resistance | $V_{BTST2}$ - $V_{SW2}$ = 5V | | 1.0 | | Ω |
| $V_{BTST2_REFRESH}$ | Bootstrap refresh comparator threshold voltage | BTST2 falling, $V_{BTST2}$ - $V_{SW2}$ when low-side refresh pulse is requested | 2.7 | 3.1 | 3.9 | V |
| $R_{LODRV2_ON}$ | Boost side low-side turnon resistance | VREGN = 5V | | 3.4 | | Ω |
| $R_{LODRV2_OFF}$ | Boost side low-side turnoff resistance | VREGN = 5V | | 1.0 | | Ω |
| $t_{DT2}$ | Boost side dead time, both edges | | | 45 | | ns |
| **ANALOG-TO-DIGITAL CONVERTER (ADC)** | | | | | | |
| $t_{ADC_CONV}$ | Conversion-time, each measurement | ADC_SAMPLE[1:0] = 00 | | 24 | | ms |
| | | ADC_SAMPLE[1:0] = 01 | | 12 | | ms |
| | | ADC_SAMPLE[1:0] = 10 | | 6 | | ms |

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VAC = ACP = ACN = SYS = SRP = SRN = 28V, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $ADC_{RES}$ | Effective resolution | ADC_SAMPLE[1:0] = 00 | 14 | 15 | | bits |
| | | ADC_SAMPLE[1:0] = 01 | 13 | 14 | | bits |
| | | ADC_SAMPLE[1:0] = 10 | 12 | 13 | | bits |
| **ADC MEASUREMENT RANGE AND LSB** | | | | | | |
| $I_{AC_ADC}$ | Input current ADC reading (positive or negative) | Range with 2mΩ $R_{AC_SNS}$ | –50000 | | 50000 | mA |
| | | LSB with 2mΩ $R_{AC_SNS}$ | | 2 | | mA |
| $I_{BAT_ADC}$ | Battery current ADC reading (positive or negative) | Range with 2.5mΩ $R_{BAT_SNS}$ | –40000 | | 40000 | mA |
| | | LSB with 2.5mΩ $R_{BAT_SNS}$ | | 4 | | mA |
| $V_{AC_ADC}$ | Input voltage ADC reading | Range | 0 | | 65534 | mV |
| | | LSB | | 2 | | mV |
| $V_{BAT_ADC}$ | Battery voltage ADC reading | Range | 0 | | 65534 | mV |
| | | LSB | | 2 | | mV |
| $V_{SYS_ADC}$ | System voltage ADC reading | Range | 0 | | 65534 | mV |
| | | LSB | | 2 | | mV |
| $TS_{ADC}$ | TS voltage ADC reading, as percentage of REGN | Range | 0 | | 99.9 | % |
| | | LSB | | 0.098 | | % |
| $V_{FB_ADC}$ | FB voltage ADC reading | Range | 0 | | 2047 | mV |
| | | LSB | | 1 | | mV |
| **$I^2C$ INTERFACE (SCL, SDA)** | | | | | | |
| $V_{IH}$ | Input high threshold level | | 1.3 | | | V |
| $V_{IL}$ | Input low threshold level | | | | 0.4 | V |
| $V_{OL}$ | Output low threshold level | Sink current = 5mA | | | 0.4 | V |
| $I_{IN_BIAS}$ | High-level leakage current | Pull up rail 3.3V | | | 1 | µA |
| **LOGIC I/O PIN ($\overline{CE}$, $\overline{PG}$, REV_DIS, STAT)** | | | | | | |
| $V_{IH}$ | Input high threshold level ($\overline{CE}$, REV_DIS) | | 1.3 | | | V |
| $V_{OL}$ | Output low threshold level ($\overline{PG}$, STAT) | Sink current = 5mA | | | 0.4 | V |
| $V_{IL}$ | Input low threshold level ($\overline{CE}$, REV_DIS) | | | | 0.4 | V |
| $I_{OUT_BIAS}$ | High-level leakage current ($\overline{CE}$, REV_DIS, $\overline{PG}$, STAT) | Pull up rail 3.3V | | | 1 | µA |


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## 6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **VAC / BAT POWER UP** | | | | | |
| $t_{ACOV_DGL}$ | Enter ACOV deglitch time, ACOV rising | | 100 | | µs |
| $t_{ACOVZ_DGL}$ | Exit ACOV deglitch time, ACOV falling | | 12 | | ms |
| $t_{ACUV_DGL}$ | Enter ACUV deglitch time, ACUV falling | | 100 | | µs |
| $t_{ACUVZ_DGL}$ | Exit ACUV deglitch time, ACUV rising | | 12 | | ms |
| **BATTERY-PACK NTC MONITOR** | | | | | |
| $t_{TS_DGL}$ | Deglitch time for TS threshold crossing | | 25 | | ms |
| **I²C INTERFACE** | | | | | |
| $f_{SCL}$ | SCL clock frequency | | | 1000 | kHZ |
| **DIGITAL CLOCK AND WATCHDOG** | | | | | |
| $t_{LP_WDT}$ | I²C Watchdog reset time (EN_HIZ = 1, WATCHDOG[1:0] = 160s) | 100 | 160 | | s |
| $t_{WDT}$ | I²C Watchdog reset time (EN_HIZ = 0, WATCHDOG[1:0] = 160s) | 130 | 160 | | s |

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## 6.7 Typical Characteristics

$C_{VAC}$ = 160µF, $C_{OUT}$= 160µF, $f_{SW}$ = 250kHz, L = 4.7µH, $T_A$ = 25°C (unless otherwise specified)

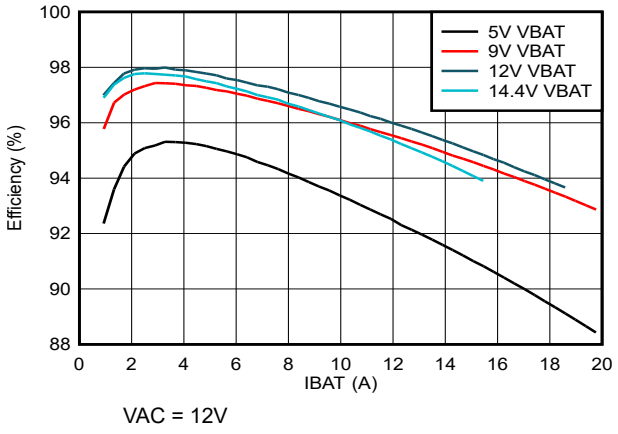


**Figure 6-1. Charge Efficiency vs Charge Current**

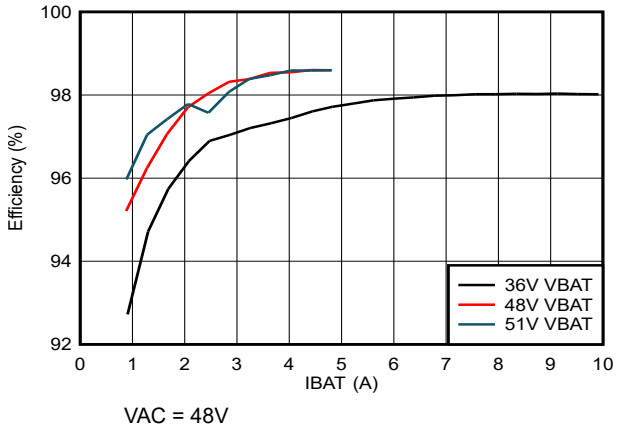


**Figure 6-2. Charge Efficiency vs Charge Current**

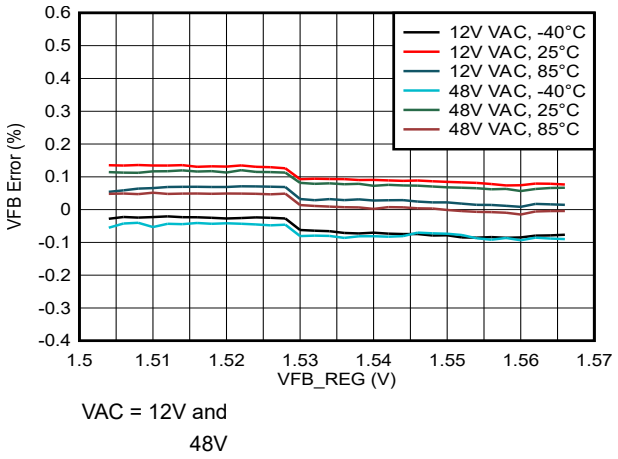


**Figure 6-3. Forward Feedback Voltage Accuracy (at different temperatures)**

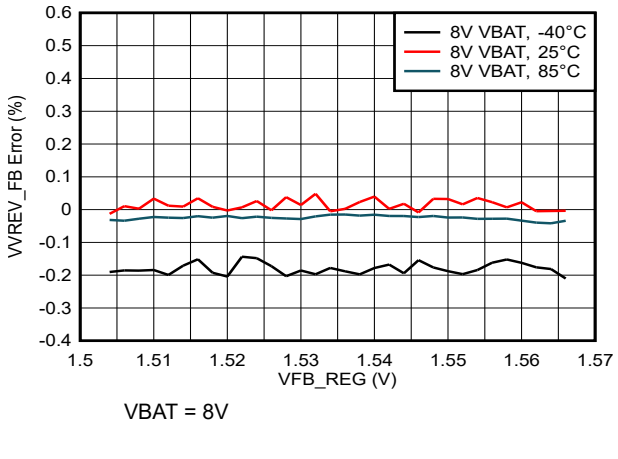


**Figure 6-4. Reverse Feedback Voltage Accuracy (at different temperatures)**

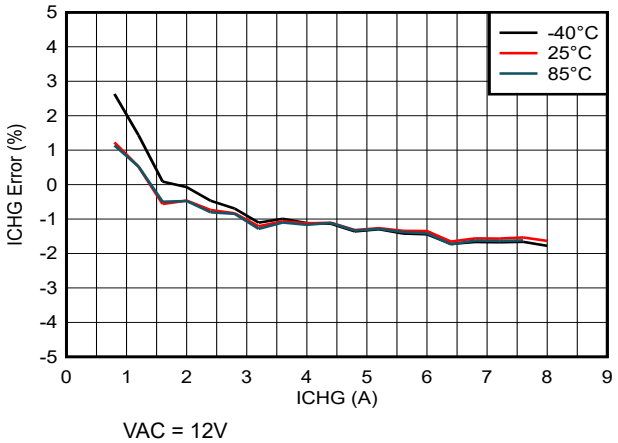


**Figure 6-5. Charge Current Accuracy (at different temperatures)**

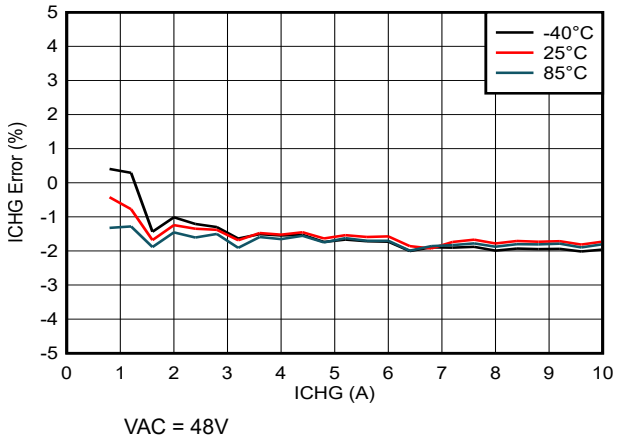


**Figure 6-6. Charge Current Accuracy (at different temperatures)**


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# 7 Detailed Description

## 7.1 Overview

The BQ25853-Q1 is a wide input voltage, supercapacitor switched-mode buck-boost battery charge controller with direct power path control. The device offers high-efficiency battery charging over a wide voltage range with accurate and programmable charge current and charge voltage regulation. The device integrates all the loop compensation and 5V gate drivers for the buck-boost converter, thereby providing a high density design with ease of use. The switching frequency of the device can be programmed or forced to follow an external clock frequency via the FSW_SYNC pin. While switching under light-load the device offers an optional Pulse Frequency Modulation (PFM) mode to increase efficiency. The charger has a digital state machine that advances the states of the charger as the converter analog feedback loops hand off control to each other. The digital state machine also manages the fault protection comparators. The loops regulate and comparators compare against reference values in the $I^2C$ registers, unless clamped by external resistors.

Besides the $I^2C$ host-controlled charging mode, the device also supports autonomous charging mode via resistor programmable limits. Input current, charge current and charge voltage regulation targets can be changed via the ILIM_HIZ, ICHG, and FB pins, respectively. The device can complete a charging cycle without any software intervention. Charging function is controlled via the $\overline{CE}$ pin.

The device charges a supercapacitor in two phases: constant current (CC) charging and constant voltage (CV) charging. By default, at the end of the charging cycle, the charger automatically terminates when the charge current is below the termination current limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger automatically starts a new charge cycle. The termination can be disabled by $I^2C$.

The input operating window is programmed via the ACUV and ACOV pins. When the input voltage is outside the programmed window, the device automatically stops the charger, and the $\overline{PG}$ pin pulls HIGH. In the absence of an input source, the device can power the system load from supercapacitor through BATFET or via reverse power flow, discharging the supercapacitor through the buck-boost converter to generate a programmable, regulated voltage on system which is above or below the supercapacitor voltage.

The charger provides various safety features for supercapacitor charging and system operation, including battery temperature negative thermistor (NTC) monitoring, charge timers and over-voltage/over-current protections on supercapacitor and input. The thermal shutdown prevents charging when the junction temperature exceeds the $T_{SHUT}$ limit.

The device has two status pins (STAT and $\overline{PG}$) to indicate the charging status and input voltage status. These pins can be used to drive LEDs or communicate with a host processor. If needed, these pins can also be used as general purpose indicators and the status controlled directly by the $I^2C$ interface. In addition, the $\overline{CE}$ pin can also be used as a general purpose indicator. The $\overline{INT}$ pin immediately notifies host when the device status changes, including faults.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring input current, charge current and input/battery/system/thermistor voltages (IAC, IBAT, VAC, VBAT, VSYS, TS).

The device comes with a 36-pin 5mm × 6mm QFN package with 0.5mm pin pitch.

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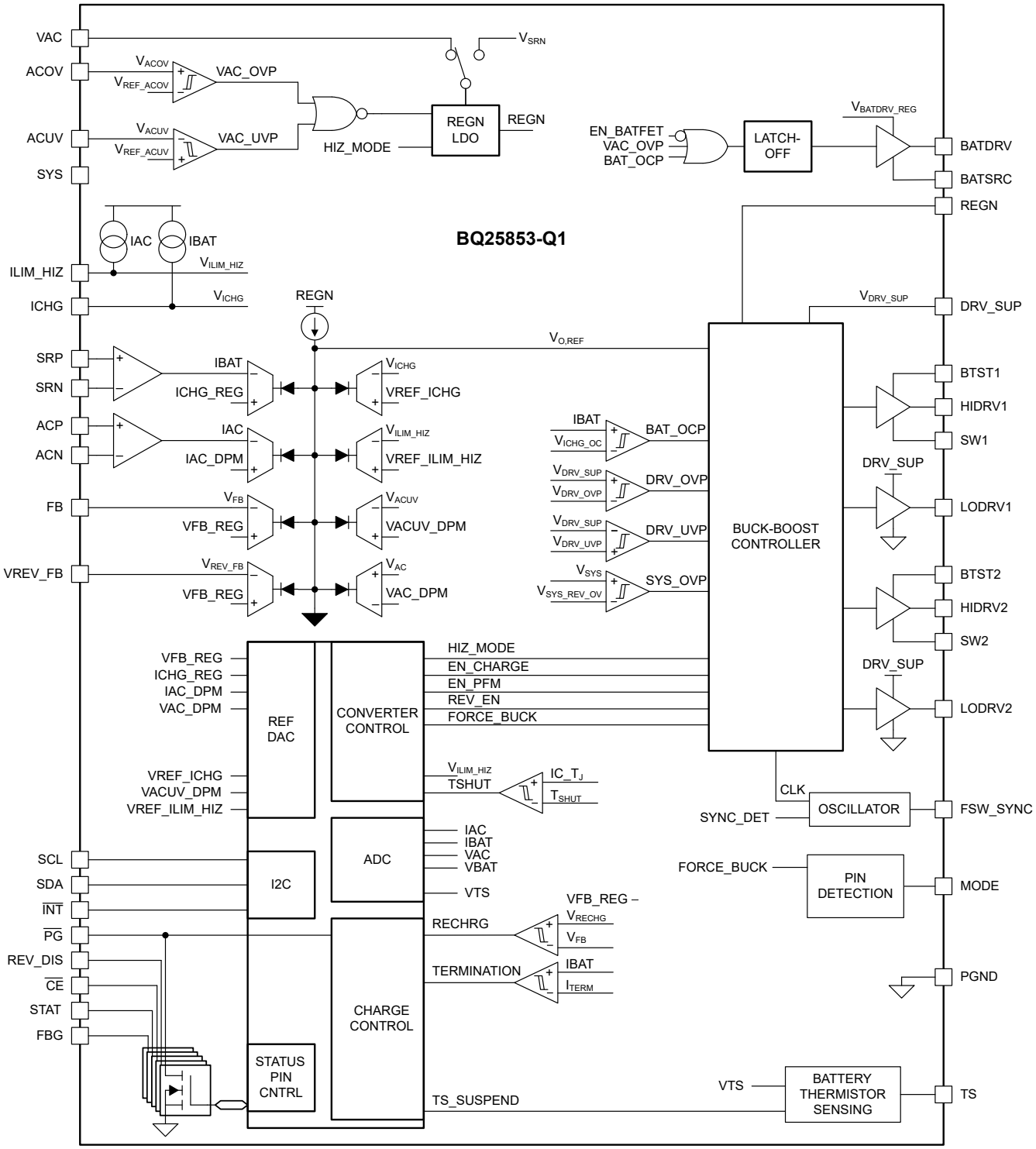
## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Device Power-On-Reset

The internal bias circuits are powered from either VAC or SRN. When VAC rises above $V_{VAC_OK}$, charging is allowed. When BAT rises above 3V, the BATFET driver is active, and reverse mode operation is allowed.

A POR occurs when one of these supplies rises above the corresponding $V_{OK}$ level, while the other supply is below the corresponding $V_{OK}$ level. After the POR, $I^2C$ is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

### 7.3.2 Device Power-Up From Battery Without Input Source

If only battery is present and the voltage is above $V_{SRN_OK}$ threshold, the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The N-type driver allows for use of low $R_{DS,ON}$ external BATFET, minimizing the conduction loss. The low quiescent current on BAT maximizes the battery run time. The ADC can be used to monitor discharge current through SRP and SRN pins. The BATFET can be forced to turn off using the FORCE_BATFET_OFF register bit.

If only battery is present and the voltage is above 3V threshold, the device is ready for $I^2C$ communication , and the converter is ready to start operation in reverse mode. The REGN LDO stays off to minimize the quiescent current. The ADC can be used to monitor all system parameters.

### 7.3.3 Device Power Up from Input Source

#### 7.3.3.1 VAC Operating Window Programming (ACUV and ACOV)

The VAC operating window can be programmed using the ACUV and ACOV pins using a three-resistor divider from VAC to PGND as shown in Figure 7-1.

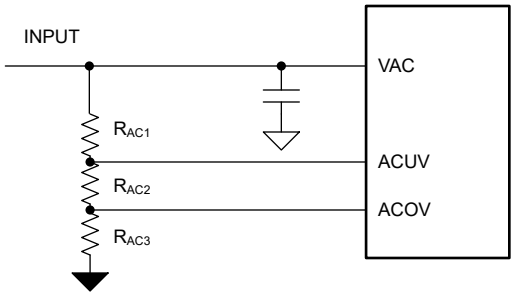


**Figure 7-1. ACUV and ACOV Programming**

When $V_{ACUV}$ falls and reaches $V_{ACUV_DPM}$, the device enters input voltage regulation, thereby reducing the charge current. $V_{ACUV}$ continues falling below $V_{REF_ACUV}$, the device automatically stops the converter and the $\overline{PG}$ pin pulls high.

**System Note:** if VAC_DPM register is programmed to a value higher than POR, the device regulates the VAC voltage to the higher of VAC_DPM register or $V_{ACUV_DPM}$ pin voltage. Refer to Section 7.3.5.1.2 for more information.

When $V_{ACOV}$ rises above $V_{REF_ACOV}$, the device automatically stops the converter and the $\overline{PG}$ pin pulls high.

The following equations govern the relationship between the resistor divider and the target operating voltage window programmed by ACOV and ACUV pins:

$$V_{ACOV_TARGET} = V_{REF_ACOV} \times \frac{R_{AC1} + R_{AC2} + R_{AC3}}{R_{AC3}} \quad (1)$$

$$V_{ACUV_TARGET} = V_{REF_ACUV} \times \frac{R_{AC1} + R_{AC2} + R_{AC3}}{R_{AC2} + R_{AC3}} \quad (2)$$

If unused, tie ACUV to VAC and ACOV to PGND to apply the internal VAC operating window ($V_{VAC_OP}$).

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#### 7.3.3.2 MODE Pin Configuration

The MODE pin can be used to configure the device as either a buck-boost or buck-only configuration. When configured as buck-only typical inductor value used must be provided to appropriately compensate the converter. The closest inductor to the values presented below must be programmed via the MODE pin.

At POR, the device detects the MODE pin pull down resistance, then sets the device operating mode as shown below. The MODE pin resistance detection is only done one time at the device POR, after that, the charger does not sense the MODE pin voltage any more. Follow the resistance listed in the table below to set the desired operating mode. The surface mount resistor with ±1% or ±2% tolerance is recommended.

**Table 7-1. MODE Pin Resistance Configuration Options**

| OPERATION | L (nom) | $R_{DCR}$ (min) | $R_{DCR}$ (max) | TYPICAL RESISTANCE AT MODE PIN |
|---|---|---|---|---|
| Buck-Boost, device detects inductance automatically | 2.2µH - 15µH | L/DCR = 1260µs(1) | 60mΩ | ≤3.0kΩ |
| Buck-Only | 3.3µH | 2.6mΩ | 60mΩ | 4.7kΩ |
| Buck-Only | 4.7µH | 3.7mΩ | 60mΩ | 6.04kΩ |
| Buck-Only | 5.6µH | 4.4mΩ | 60mΩ | 8.2kΩ |
| Buck-Only | 6.8µH | 5.4mΩ | 60mΩ | 10.5kΩ |
| Buck-Only | 8.2µH | 6.5mΩ | 60mΩ | 13.7kΩ |
| Buck-Only | 10µH | 7.9mΩ | 60mΩ | 17.4kΩ |
| Buck-Only | 15µH | 11.9mΩ | 60mΩ | ≥27.0kΩ |

(1) The minimum DCR varies as a function of selected inductor: for example, a 10µH inductor supports 7.9mΩ as the minimum DCR.

#### 7.3.3.3 REGN Regulator (REGN LDO)

The REGN LDO regulator provides a regulated bias supply for the IC and the TS external resistors. Additionally, REGN voltage can be used to drive the buck-boost switching FETs directly by tying the DRV_SUP pin to REGN. The pull-up rail of $\overline{PG}$, STAT can be connected to REGN as well. The REGN LDO is enabled when below conditions are valid:

1. VAC voltage above $V_{VAC_OK}$ and charge is enabled in forward mode.
2. BAT voltage above 3V in Reverse mode and Reverse Mode is enabled (EN_REV = 1)

At high input voltages and/or large gate drive requirements, the power loss from gate driving via the REGN LDO can be excessive. This power for the gate drivers can be provided externally by directly driving the DRV_SUP pin with a high efficiency supply ranging from 4.5V to 12V. This supply must be able to provide at least 50mA or more as required to drive the switching FET gate charge. When the converter is disabled, the DRV_SUP supply needs to be disabled such that BTST1/BTST2 and DRV_SUP pins are not biased.

The power dissipation for driving the gates via the REGN LDO is: $P_{REGN} = \left(VAC - V_{REGN}\right) \times Q_{G(TOT)1,2,3,4} \times f_{SW}$, where $Q_{G(TOT)1,2,3,4}$ is the sum of the total gate charge for all switching FETs and $f_{SW}$ is the programmed switching frequency. The Safe Operating Area (SOA) below is based on a 1W power loss limit.


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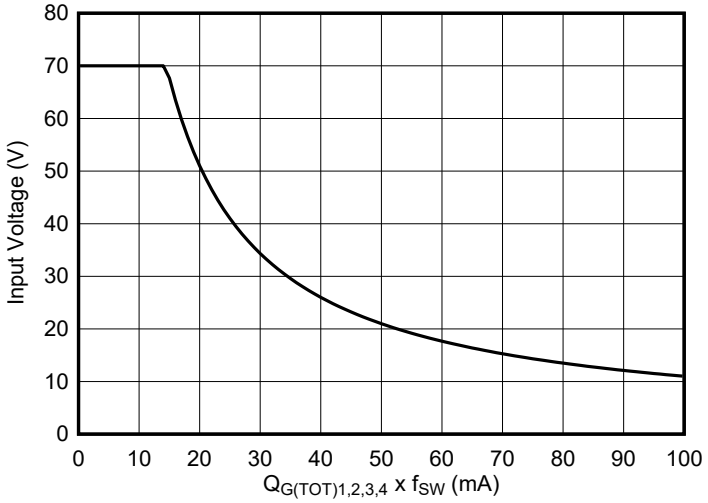


**Figure 7-2. REGN LDO Safe Operating Area (SOA)**

#### 7.3.3.4 Compensation-Free Buck-Boost Converter Operation

The device integrates all the loop compensation, thereby providing a high density design with ease of use. At startup, the device toggles the SW node for about 40ms to determine the correct compensation values for a given set of passives. If the battery is above VBAT_LOWV, then SW2 is toggled. SW1 is toggled otherwise.

The charger employs a synchronous buck-boost converter that allows charging from a wide range of input voltage sources. The charger operates in buck, buck-boost or boost mode. The converter can operate uninterruptedly and continuously across the three operation modes. During buck-boost mode, the converter alternates a SW1 pulse with a SW2 pulse, with effective switching frequency interleaved among these pulses for highest efficiency operation.

During boost mode operation, the HS FET is forced to turn on for 225ns in each switching cycle to verify that inductor energy is delivered to the output, effectively limiting the maximum boosting ratio. For example, when device is configured to switch at 500kHz, the switching period is 2µs, yielding a duty cycle limit of (1 - 0.225µs/2µs) = 88.75%. Given a 5V input, this translates to a maximum 44V output assuming 100% efficiency. The true output is lower than this ideal limit. At lower switching frequencies, the maximum duty cycle increases, making the limitation less significant.

**Table 7-2. Switching MOSFET Operation**

| MODE | BUCK | BUCK-BOOST | BOOST |
|---|---|---|---|
| HS BUCK FET | Switching at $f_{SW}$ | Switching ($f_{SW}$ interleaved between SW1 and SW2) | ON |
| LS BUCK FET | Switching at $f_{SW}$ | Switching ($f_{SW}$ interleaved between SW1 and SW2) | OFF |
| LS BOOST FET | OFF | Switching ($f_{SW}$ interleaved between SW1 and SW2) | Switching at $f_{SW}$ |
| HS BOOST FET | ON | Switching ($f_{SW}$ interleaved between SW1 and SW2) | Switching at $f_{SW}$ |

##### *7.3.3.4.1 Light-Load Operation*

To improve converter light-load efficiency, the device switches to Pulse Frequency Modulation (PFM) control at light load when the EN_PFM bit is set to 1. The effective switching frequency decreases accordingly when output load decreases.

EN_PFM bit is automatically cleared to 0 every time the converter starts and a valid SYNC clock input is detected on the FSW_SYNC pin, ensuring fixed frequency operation regardless of output current. The bit can be overwritten to 1 to allow PFM after startup even when SYNC signal is present.

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Light-load PFM mode can be disabled by clearing the EN_PFM bit. In this case, the device switches in PWM mode at a fixed switching frequency. It is recommended to disable PFM mode (EN_PFM = 0) when termination is enabled and set lower than 2A.

#### 7.3.3.5 Switching Frequency and Synchronization (FSW_SYNC)

The device switching frequency can be programmed between 200kHz to 600kHz using a resistor from the FSW_SYNC pin to PGND. The $R_{FSW}$ resistor is related to the nominal switching frequency ($f_{SW}$) by the equation:

$$R_{FSW} = \frac{1}{10 \times \left(f_{SW} \times 5 \times 10^{-12} - 500 \times 10^{-9}\right)} \quad (3)$$

This pin must be pulled to PGND using a $R_{FSW}$, do not leave floating. In addition to programming the nominal switching frequency, the FSW_SYNC pin can also be used to synchronize the internal oscillator to an external clock signal. The synchronization feature works over the same range as the switching frequency: 200kHz to 600kHz range.

**Table 7-3. Common $R_{FSW}$ and Switching Frequency Values**

| $R_{FSW}$ (kΩ) | SWITCHING FREQUENCY (kHz) |
|---|---|
| 200 | 200 |
| 133 | 250 |
| 100 | 300 |
| 80 | 350 |
| 66.67 | 400 |
| 57.1 | 450 |
| 50 | 500 |
| 44.4 | 550 |
| 40 | 600 |

#### 7.3.3.6 Device HIZ Mode

When a valid input supply is present, forcing the device into HIZ Mode is possible, which disables switching, disables REGN LDO. The charger enters HIZ Mode when EN_HIZ bit is set to 1 or the ILIM_HIZ pin is pulled above $V_{IH_ILIM_HIZ}$ (refer to Section 7.3.5.1.1.1).

If the device is operating in reverse mode with the converter turned on, and the device enters HIZ mode (EN_HIZ bit is set to 1 or ILIM_HIZ pin is pulled above $V_{IH_ILIM_HIZ}$), switching stops. Once HIZ mode condition is cleared by the host, the device resumes reverse mode operation.

The device exits HIZ Mode when the EN_HIZ bit is cleared to 0 or the ILIM_HIZ pin is pulled below 0.4V.

### *7.3.4 Battery Charging Management*

The device charges 1cell up-to 14cell Li-Ion batteries and 1cell up-to 16cell $LiFePO_4$ batteries, or 1 cell up-to 28cell super cap. The charge cycle is autonomous and requires no host interaction.

#### 7.3.4.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit =1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device charging parameters can be set by hardware through the FB pin to set regulation voltage and the ICHG pin to set charging current. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through $I^2C$.

A new charge cycle starts when the following conditions are valid:

- VAC is within the ACUV and ACOV operating window
- Device is not in HIZ mode (EN_HIZ = 0 and ILIM_HIZ pin voltage is below $V_{IH_ILIM_HIZ}$)


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- REGN is above $V_{REGN_OK}$
- Battery charging is enabled (EN_CHG = 1 and $\overline{CE}$ pin is LOW )
- No thermistor fault on TS
- No safety timer fault

For lithium-ion battery charging, the charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode. When a full battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits), the device automatically starts a new charging cycle. After the charge is done, toggle either $\overline{CE}$ pin or EN_CHG bit can initiate a new charging cycle.

The status register (CHARGE_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (VFB < $V_{BAT_SHORT}$)
- 010 – Pre-charge ($V_{BAT_SHORT}$ < VFB < $V_{BAT_LOWV}$)
- 011 – Fast-charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when charge cycle is completed, an INT pulse is asserted to notify the host.

Supercapacitors do not require Trickle Charge or Pre-charge regions when the voltage is low. For supercapacitor charging, setting the EN_PRECHG bit to 0 can disable both of these charging regions. In this case, the charger outputs ICHG current as long as the feedback voltage ($V_{FB}$) is below VFB_REG. The following settings are recommended for supercapacitor charging:

- EN_PRECHG = 0
- EN_TERM = 0
- EN_CHG_TMR = 0

#### *7.3.4.1.1 Charge Current Programming (ICHG pin and ICHG_REG)*

There are two distinct thresholds to limit the charge current (if both are enabled, the lowest limit of these apply):

1. ICHG pin pulldown resistor (hardware control)
2. ICHG_REG register bits (host software control)

To set the maximum charge current using the ICHG pin, a pulldown resistor to PGND is used. Using a 5mΩ $R_{BAT_SNS}$ sense resistor is required. The charge current limit is controlled by:

$$I_{CHG_MAX} = \frac{K_{ICHG}}{R_{ICHG}} \quad (4)$$

The precharge current limit is defined as $I_{PRECHG_MAX}$ = 20% × $I_{CHG_MAX}$, and the termination current is $I_{TERM}$ = 10% × $I_{CHG_MAX}$.

The actual charge current limit is the lower value between ICHG pin setting and $I^2C$ register setting (ICHG_REG). The device regulates ICHG pin at $V_{REF_ICHG}$. If ICHG pin voltage exceeds $V_{REF_ICHG}$, the device enters charge current regulation.

The ICHG pin can also be used to monitor charge current when device is not in charge current regulation. When not in charge current regulation, the voltage on ICHG pin ($V_{ICHG}$) is proportional to the actual charging current. ICHG pin can be used to monitor battery current with the following relationship:

$$I_{BAT} = \frac{K_{ICHG} \times V_{ICHG}}{R_{ICHG} \times V_{REF_ICHG}} \quad (5)$$

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If ICHG pin is shorted to PGND, the charge current limit is set by the ICHG_REG register. If hardware charge current limit function is not needed, short this pin to PGND. The ICHG pin function can be disabled by setting the EN_ICHG_PIN bit to 0 (recommended when pin is shorted to PGND). When the pin is disabled, charge current limit and monitoring functions via ICHG pin are not available.

To set the maximum charge current using the ICHG_REG register bits, write to the ICHG_REG register bits. The default ICHG_REG is set to maximum code, allowing ICHG pin to limit the current in hardware.

#### 7.3.4.2 Li-Ion Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

**Table 7-4. Recommended Li-Ion Charge Settings**

| PARAMETER | I²C REGISTER BITS | VALUE | EQUIVALENT PER 4.2V CHARGE (V) |
|---|---|---|---|
| Battery Low Voltage | VBAT_LOWV | 0x3 = 71.4% × VFB_REG | 3.0V |
| Recharge Voltage | VRECHG | 0x3 = 97.6% × VFB_REG | 4.1V |

If the charger device is in DPM regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Charging Safety Timer.

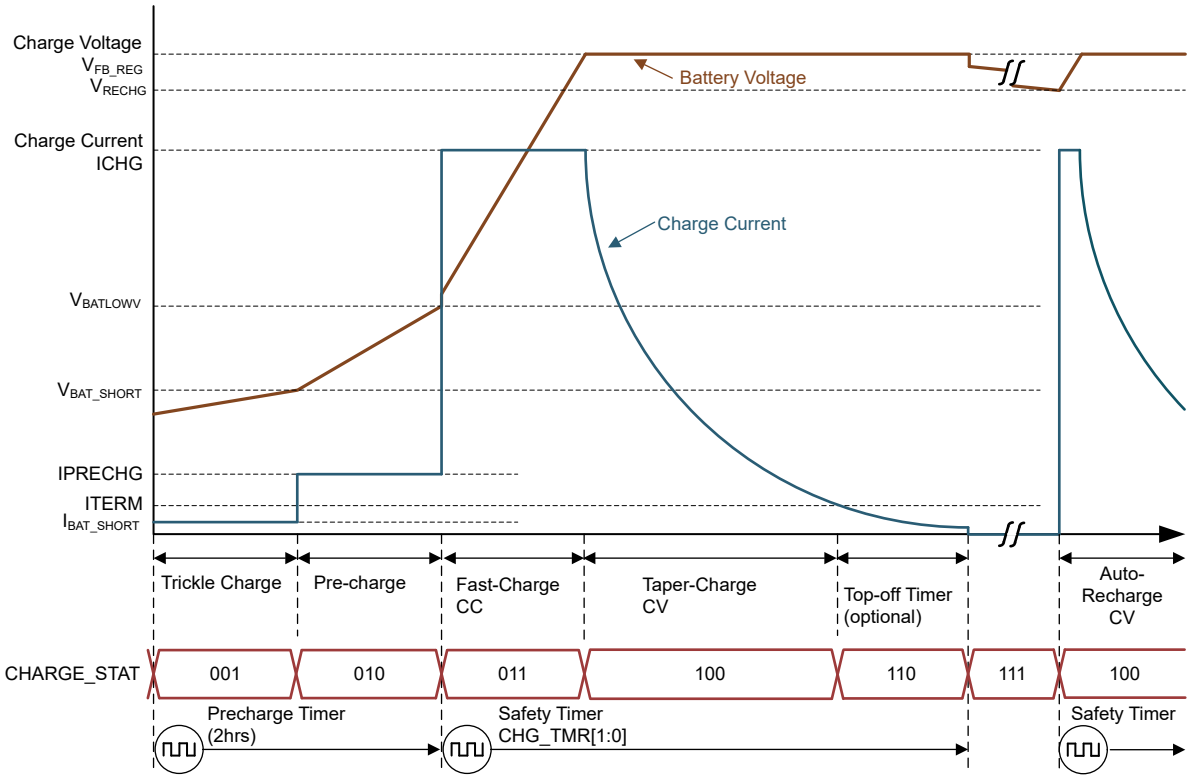


**Figure 7-3. Typical Li-Ion Battery Charging Profile**

#### 7.3.4.3 $LiFePO_4$ Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.


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**Table 7-5. Recommended $LiFePO_4$ Charge Settings**

| PARAMETER | $I^2C$ REGISTER BITS | VALUE | EQUIVALENT PER 3.6V CHARGE (V) |
|---|---|---|---|
| Battery Low Voltage | VBAT_LOWV | 0x1 = 55% × VFB_REG | 1.98V |
| Recharge Voltage | VRECHG | 0x0 = 93% × VFB_REG | 3.35V |

If the charger device is in DPM regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Charging Safety Timer. The typical charging cycle for $LiFePO_4$ follows the same profile as Typical Li-Ion Battery Charging Profile.

#### 7.3.4.4 Charging Termination for Li-ion and $LiFePO_4$

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. The termination current threshold is controlled by the lower option between 10% x ICHG pin setting or the ITERM register setting.

In standalone applications using the ICHG pin to program the current, the termination threshold is set at 10% of the ICHG pin value (10A ICHG pin programming results in 1A termination).

In host-controlled applications, the termination current can be programmed using the ITERM register bits. The ICHG pin can still be used to set a hardware limit for the charge current.

After the charging cycle is completed, the buck-boost converter turns off. When termination occurs, the status register CHARGE_STAT is set to 111, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, or input voltage regulation. Termination can be permanently disabled by writing 0 to EN_TERM.

At low termination currents, due to the comparator offset, the actual termination current can be up to 20% higher than the termination target. To compensate for comparator offset, a programmable top-off timer (default disabled) can be applied after termination is detected. The top-off timer follows safety timer constraints, such that if safety timer is suspended, so is the top-off timer. Similarly, if safety timer is doubled, so is the top-off timer. CHARGE_STAT reports whether the top off timer is active via the 110 code. Once the Top-Off timer expires, the CHARGE_STAT register is set to 111 and an INT pulse is asserted to the host.

#### 7.3.4.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The user can program fast charge safety timer through $I^2C$ (CHG_TMR bits). When safety timer expires, the fault register CHG_TMR_STAT bit is set to 1, and an INT pulse is asserted to the host. The safety timer feature can be disabled by clearing EN_CHG_TMR bit.

During input voltage or input current regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the programmed setting. For example, if the charger is in input current regulation (IAC_DPM_STAT=1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer expires in 10 hours. This half clock rate feature can be disabled by setting EN_TMR2X = 0.

During faults which disable charging, timer is suspended. Once the fault goes away, safety timer resumes. If the charging cycle is stopped and started again, the timer gets reset (toggle $\overline{CE}$ pin or EN_CHG bit restarts the timer).

The pre-charge safety timer is a fixed 2 hour counter that runs when VBAT < $V_{BAT_LOWV}$. The pre-charge safety timer is disabled when EN_PRECHG bit is 0.

#### 7.3.4.6 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

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#### 7.3.4.6.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1 to T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature, T1 to T2, JEITA recommends the charge current to be reduced to half of the charge current or lower. The device allows charge current in the cool temperature region to be programmed to 20%, 40% or 100% of the charge current at T2 to T3 or charge suspend, which is controlled by the register bits JEITA_ISETC. If charge current is reduced in the cool temperature region, the safety timer counts at half clock rate when EN_TMR2X = 1.

At warm temperature, T3 to T5, JEITA recommends charge voltage less than 4.1V / cell. The device provides the programmability of the charge voltage at T3T5, to be with a voltage offset less than charge voltage at T2 to T3 or charge suspend, which is controlled by the register bits JEITA_VSET.

The charger also provides flexible voltage/current settings beyond the JEITA requirements. The charge current setting at warm temperature T3 to T5 can be configured to be 40%, or 100% of the programmed charge current or charge suspend, which is programmed by the register bit JEITA_ISETH. If charge current is reduced in the JEITA warm region, the safety timer counts at half clock rate when EN_TMR2X = 1.

The default charging profile for JEITA is shown in the figure below, in which the blue line is the default setting and the red dash line is the programmable options.

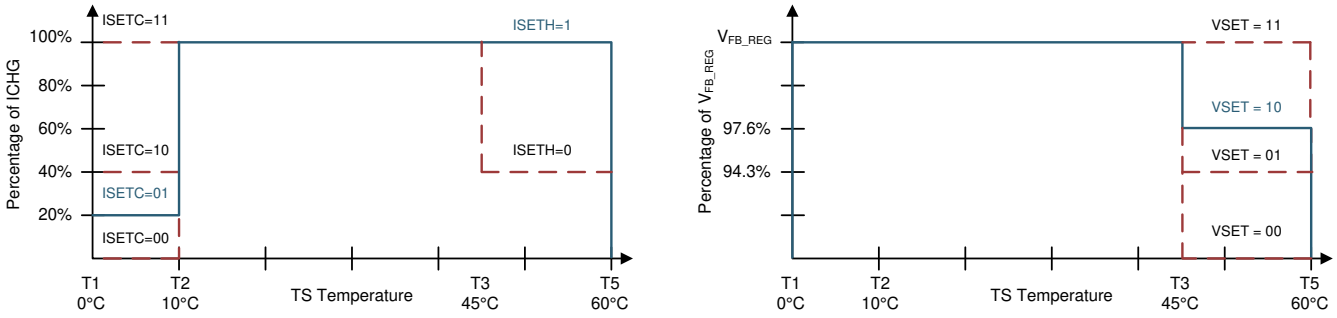
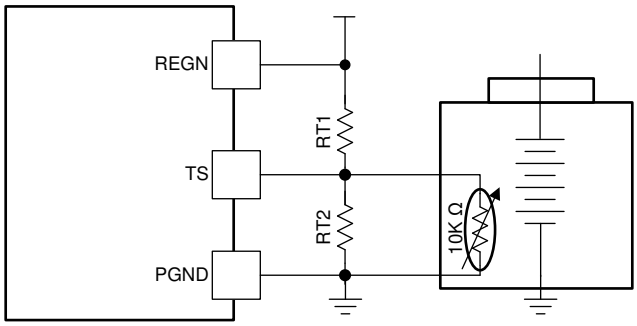



**Figure 7-4. TS Charging Values**




Assuming a 103AT NTC thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (6)$$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$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (7)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

$RTH_{T1}$ = 27.28kΩ

$RTH_{T5}$ = 3.02kΩ

RT1 = 5.24kΩ

RT2 = 30.31kΩ

The device also offers programmability for all the thresholds via the TS Charging Threshold Control register (REG0x1B). This flexibility can help to change the charger's operating window in software.

The JEITA profile can be disabled by clearing the EN_JEITA register bit. In this case, the device still limits the charging window from T1 to T5, but no special charge profile is employed within the Cool (T1 to T2) or Warm (T3 to T5) regions.

The NTC monitoring window can be disabled by clearing the EN_TS register bit. In this case, the TS pin voltage is ignored, and the device always reports normal TS status. If EN_TS is set to 0, TS pin can be floated or connected to PGND.

#### *7.3.4.6.2 Cold/Hot Temperature Window in Reverse Mode*

For battery protection during reverse or auto-reverse mode operation, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When temperature is outside of the thresholds, the reverse mode is shut off. In addition, EN_REV, EN_AUTO_REV and REVERSE_STAT bits are cleared to 0 and corresponding TS_STAT is reported (TS Cold or TS Hot). The temperature protection in reverse mode can be completely disabled by clearing the EN_TS bit to 0.

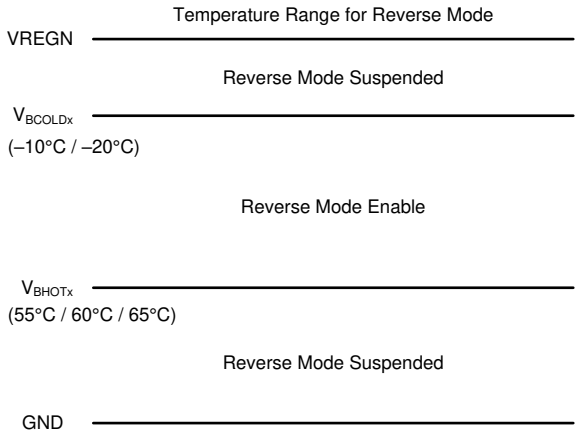


**Figure 7-5. TS Pin Thermistor Sense Threshold in Reverse Mode**

### *7.3.5 Power Management*

The device accommodates a wide range of input sources from 4.2V up to 70V.

#### 7.3.5.1 Dynamic Power Management: Input Voltage and Input Current Regulation

The device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (lower of IAC_DPM or ILIM_HIZ pin setting), or the voltage falls below the input voltage limit (higher of VAC_DPM or ACUV pin setting, $V_{ACUV_DPM}$). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

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When the charge current is reduced to zero, but the input source is still overloaded, the input voltage continues to drop. Once the input voltage drops below the ACUV limit ($V_{ACUV}$ < $V_{REF_ACUV}$), the charger stops switching.

#### 7.3.5.1.1 Input Current Regulation

The total input current is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without DPM, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the battery charger reduces the charging current when the input current exceeds the input current limit set by the lower of IAC_DPM register bits, or ILIM_HIZ pin. This allows the current capability of the input source to be lowered, reducing system cost.

There are two thresholds to limit the input current (if both are enabled, the lower limit of these two apply):

1. IAC_DPM register bits (host software control)
2. ILIM_HIZ pull down resistor (hardware control)

To set the maximum current using the IAC_DPM register bits, write to the IAC_DPM register bits. When using a 2mΩ resistor, the input current limit range is from 1A to 50A with 125mA/step. The default IAC_DPM is set to maximum code, allowing ILIM_HIZ pin to limit the current in hardware.

To set the maximum current using the ILIM_HIZ pin, refer to Section 7.3.5.1.1.1.

Although both limits are referenced to a 2-mΩ sense resistor, other values can also be used. A larger sense resistor provides a larger sense voltage and higher regulation accuracy, but at the expense of higher conduction loss. For example, using a 5mΩ resistor yields programmability from 400mA to 20A with 50mA/step.

##### 7.3.5.1.1.1 ILIM_HIZ Pin

To set the maximum input current using the ILIM_HIZ pin, a pull-down resistor to PGND is used. When using a 2mΩ $R_{AC_SNS}$ resistor, the input current limit is controlled by: $I_{AC_MAX}$ = $K_{ILIM}$ / $R_{ILIM_HIZ}$.

The actual input current limit is the lower value between ILIM_HIZ pin setting and register setting (IAC_DPM). For example, if the register setting is 20A, and ILIM_HIZ pin has a 5kΩ resistor ($K_{ILIM}$ = 50A-kΩ) to ground for 10A, the actual input current limit is 10A. ILIM_HIZ pin can be used to set the input current limit when EN_ILIM_HIZ_PIN bit is set to 1. The device regulates the pin at $V_{REF_ILIM_HIZ}$. If pin voltage exceeds $V_{REF_ILIM_HIZ}$, the device enters input current regulation. Entering input current regulation through the pin sets the IAC_DPM_STAT and FLAG bits, and produces an interrupt to host. The interrupt can be masked via the IAC_DPM_MASK bit.

The ILIM_HIZ pin can also be used to monitor input current. When not in input current regulation, the voltage on ILIM_HIZ pin ($V_{ILIM_HIZ}$) is proportional to the input current. Pin voltage can be used to monitor input current with the following relationship: IAC = $K_{ILIM}$ x $V_{ILIM_HIZ}$ / ($R_{ILIM_HIZ}$ x $V_{REF_ILIM_HIZ}$).

For example, if the pin is set with 5kΩ resistor, and the pin voltage is 1.0V, the actual input current is between 4.8A to 5.2A (based on $K_{ILIM}$ specified).

If ILIM_HIZ pin is shorted, the input current limit is set by the IAC_DPM register. If hardware input current limit function is not needed, short this pin to GND. If pin is pulled above $V_{IH_ILIM_HIZ}$, the device enters HIZ mode (refer to Section 7.3.3.6). The ILIM_HIZ pin function can be disabled by setting the EN_ILIM_HIZ_PIN bit to 0. When the pin is disabled, input current limit and monitoring functions as well as HIZ mode control using the pin are not available.

#### 7.3.5.1.2 Input Voltage Regulation

In addition to input current regulation, the device also offers input voltage regulation to limit the input power. This is especially useful when dealing with input sources such as solar panels, where the operating voltage must be controlled to extract the maximum power. Alternatively, if the input source current limitation is not known, input voltage regulation can be used to limit the power draw from the input source. By using input voltage regulation, the battery charger reduces the charging current when the input voltage falls below the input voltage limit set by the higher of VAC_DPM register bits, or ACUV pin.


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There are two thresholds to limit the input voltage (the higher limit of these apply)

1. VAC_DPM register bits (host software control)
2. ACUV pin falling threshold (hardware control)

To set the minimum input voltage using the VAC_DPM register bits, write the desired value directly to the VAC_DPM register bits. The default VAC_DPM is set to minimum code, allowing ACUV pin to limit the input voltage in hardware.

To set the minimum input voltage using the ACUV pin, refer to Section 7.3.3.1.

### *7.3.6 Switching Frequency Dithering Feature*

Normally, the IC switches in fixed frequency which can be adjusted through FSW_SYNC pin. The charger also supports frequency dithering to improve EMI performance and help pass the IEC-CISPR 32 specification. Dithering is disabled by default as EN_DITHER=00b at startup. Dithering can be enabled by setting EN_DITHER=01/10/11b. The switching frequency is not fixed when dithering is enabled and varies within determined range by setting EN_DITHER to 01/10/11b, which corresponds to ±2%/4%/6% switching frequency variation. A larger dithering range results in a smaller EMI noise peak, but a larger dithering range also causes slightly more output voltage ripple. Therefore, the dithering frequency range selection is a trade-off between EMI noise peak and output voltage ripple and we recommend you to select the lowest dithering range which can pass IEC-CISPR 32 specification. The patented dithering pattern can improve EMI performance in the switching frequency up to 30MHz range which covers the entire conductive EMI noise range.

Note that the Dithering feature does not work if an external clock is provided.

### *7.3.7 Reverse Mode Power Direction*

The device supports buck-boost reverse power direction with CC/CV profile to deliver power from the battery to the input when the adapter is not present. The reverse mode output voltage regulation is set by the VREV_FB pin resistor divider. The reverse mode also offers output current regulation via the $R_{AC_SNS}$ resistor. This parameter is controlled by the IAC_REV register bits. The reverse mode operation can be enabled if the following conditions are valid:

1. SRN above 3.8V.
2. DRV_SUP voltage within valid operating window ($V_{DRV_UVP} < V_{DRV} < V_{DRV_OVP}$).
3. Reverse mode operation is enabled (EN_REV = 1)
4. Voltage at TS (thermistor) pin is within range configured by Reverse Temperature Monitor as configured by BHOT and BCOLD register bits

While the reverse mode is active, the device sets the REVERSE_STAT bit to 1. Host can disable the reverse operation at any time by setting EN_REV bit to 0.

The charger also monitors and regulates the battery discharging current in reverse mode. When the battery discharge current rises above the IBAT_REV register setting, the charger reduces the reverse mode power flow to limit the discharge current.

Once a valid VAC voltage is detected for forward operation, the device automatically disables reverse mode (EN_REV = 0).

#### 7.3.7.1 Auto Reverse Mode

In some applications, a regulated system voltage is required when the adapter power is removed. The BQ25853-Q1 integrates an auto-reverse function which provides a regulated system voltage using the buck-boost converter in reverse direction once the input power is removed.

When enabled by setting the AUTO_REV register bit to 1, Auto Reverse mode can be used to provide a regulated system voltage immediately after the input power is removed. The device transitions to reverse mode when the input falls below the ACUV threshold.

The Auto Reverse mode operation is automatically enabled if the following conditions are valid:

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1. SRN voltage above $V_{SRN_OK}$
2. VAC is below ACUV threshold or VAC < $V_{VAC_OK}$.
3. Auto Reverse mode operation is enabled (EN_AUTO_REV = 1)
4. Voltage at TS (thermistor) pin is within range configured by Reverse Temperature Monitor as configured by BHOT and BCOLD register bits

While the Auto reverse mode is active, the device sets the REVERSE_STAT bit to 1. Host can disable the Auto reverse operation at any time by setting EN_AUTO_REV = 0 and EN_REV = 0 with $I^2C$ command. Pulling REV_DIS high also disables reverse mode and resets EN_AUTO_REV and EN_REV to 0.

### *7.3.8 Integrated 16-Bit ADC for Monitoring*

The device includes a 16-bit ADC to monitor critical system information based on the device's modes of operation. The ADC is allowed to operate if either the $V_{VAC}$>$V_{VAC_OK}$ or VBAT>$V_{REGN_OK}$ is valid. The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a one-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion.

The ADC_SAMPLE bits control the resolution and sample speed of the ADC. By default, ADC channels is converted in one-shot or continuous conversion mode unless disabled in the ADC Function Disable register. If an ADC parameter is disabled by setting the corresponding bit, then the read-back value in the corresponding register is from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device finishes the conversion of that parameter, but does not convert the parameter starting the next conversion cycle. If all channels are disabled in one-shot conversion mode, the ADC_EN bit is cleared.

The ADC_DONE_STAT and ADC_DONE_FLAG bits signal when a conversion is complete in one-shot mode only. This event produces an INT pulse, which can be masked with ADC_DONE_MASK. During continuous conversion mode, the ADC_DONE_STAT bit has no meaning and is '0'. The ADC_DONE_FLAG bit remains unchanged in continuous conversion mode.

ADC conversion operates independently of the faults present in the device. ADC conversion continues even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = '0' to disable the ADC. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN = 0, the ADC stops immediately, and ADC measurement values correspond to last valid ADC reading.

If the host wants to exit ADC more gracefully, do either of the following actions:

1. Write ADC_RATE to one-shot, and the ADC stops at the end of a complete cycle of conversions, or
2. Disable all ADC conversion channels, and the ADC stops at the end of the current measurement.

When system load is powered from the battery (the input source is removed, or the device is in HIZ mode), enabling the ADC automatically powers up REGN and increases the quiescent current. To keep the battery leakage low, it is recommended to duty cycle or completely disable the ADC.

### *7.3.9 Status Outputs ($\overline{PG}$, STAT and $\overline{INT}$)*

#### 7.3.9.1 Power Good Indicator ($\overline{PG}$)

The PG_STAT bit goes HIGH and the $\overline{PG}$ pin pulls LOW to indicate a good input source when a valid VAC voltage is detected. The $\overline{PG}$ pin can drive an LED. All conditions must be met to indicate power good:

1. $V_{VAC_OK}$ < $V_{VAC}$ < $V_{VAC_INT_OV}$
2. $V_{ACUV}$ > $V_{REF_ACUV}$
3. $V_{ACOV}$ < $V_{REF_ACOV}$
4. Device not in HIZ mode

The $\overline{PG}$ pin can be disabled via the DIS_PG_PIN bit. When disabled, this pin can be controlled to pull LOW using the FORCE_STAT3_ON bit.


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#### 7.3.9.2 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT_PIN bit. When disabled, the STAT pin can be controlled to independently pull LOW using the FORCE_STAT_ON bit. The STAT pin is not affected by the Reverse mode and remains OFF during this mode.

**Table 7-6. STAT Pin State**

| CHARGING STATE | STAT INDICATOR |
|---|---|
| Output powered (CC or CV modes) | LOW |
| HIZ mode, /CE pin high or EN_CE = 0 | HIGH |
| Input removed or Reverse mode active | HIGH |
| Fault condition which disables switching | Blinking at 1Hz |

#### 7.3.9.3 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the charger operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events generates an active-low, 256µs INT pulse.

1. Valid input source conditions detected (see conditions for $\overline{PG}$ pin)
2. Valid input source conditions removed (see conditions for $\overline{PG}$ pin)
3. Entering IAC_DPM regulation through register or ILIM_HIZ pin
4. Entering VAC_DPM regulation through register or ACUV pin
5. $I^2C$ Watchdog timer expired
6. Charger status changes state (CHARGE_STAT value change), including Charge Complete
7. TS_STAT changes state (TS_STAT value change)
8. Junction temperature shutdown (TSHUT)
9. Battery overvoltage detected (BATOVP)
10. A rising edge on any of the *_STAT bits

Each one of these INT sources can be masked off to prevent INT pulses from being sent out when the pulses occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each INT source
- The FLAG bit holds information on which source produced an INT, regardless of the current status
- The MASK bit is used to prevent the device from sending out INT for each particular event

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an INT pulse and keeps track of which source generated the INT via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

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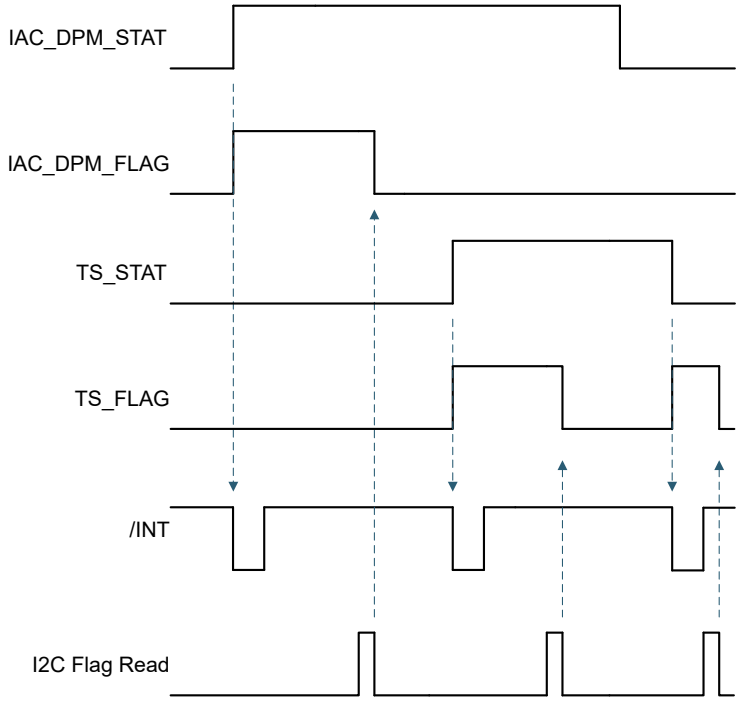


**Figure 7-6. INT Generation Behavior Example**

### *7.3.10 Protections*

The device closely monitors the input and battery voltage, as well as switching FET currents for safe switch-mode operation.

#### 7.3.10.1 Voltage and Current Monitoring

##### *7.3.10.1.1 VAC Over-voltage Protection (VAC_OVP)*

To protect downstream devices on the system rail, the input over-voltage threshold can be programed with the ACOV pin as $V_{VACOV}$ = $V_{REF_ACOV}$ (refer to Section 7.3.3.1). The device also features an internal over-voltage protection preset at $V_{VAC_INT_OV}$. When the input voltage rises above the lower of these two thresholds, the device disables the charger. During input over-voltage, an INT pulse is asserted to signal the host, and the VAC_OV_STAT, and _FLAG bits are set. Additionally, the PG_STAT bit is cleared and the $\overline{PG}$ pin pulls HIGH. The BATDRV is disabled to disconnect battery from the Boost high-side FET. The device can attempt to re-enable the BATDRV and converter by toggling $\overline{CE}$ pin.

##### *7.3.10.1.2 VAC Under-voltage Protection (VAC_UVP)*

To maintain a minimum operating voltage on the system rail, the input under-voltage threshold can be programed with the ACUV pin as $V_{VACUV}$ = $V_{REF_ACUV}$ (refer to Section 7.3.3.1). The device also features an internal under-voltage protection preset at $V_{VAC_OK}$. When the input voltage falls below the higher of these two thresholds, the device disables the charger. During input under-voltage, an INT pulse is asserted to signal the host, and the VAC_UV_STAT, and _FLAG bits are set. Additionally, the PG_STAT bit is cleared and the $\overline{PG}$ pin pulls HIGH. The device automatically resumes charging operation when the under-voltage condition goes away.

##### *7.3.10.1.3 Battery Over-current Protection (BAT_OCP)*

The device protects the battery against over-current condition using the BAT_OCP comparator. The device monitors the charge current and prevents the current from exceeding $V_{ICHG_OC}$ over $R_{BAT_SNS}$. If $V_{ICHG_OC}$ threshold is reached, the BATDRV is disabled to disconnect battery from the Boost high-side FET. The device can attempt to re-enable the BATDRV and converter by toggling $\overline{CE}$ pin.


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#### 7.3.10.1.4 Reverse Mode Over-voltage Protection (REV_OVP)

While operating the converter in reverse mode, the device monitors the system voltage, $V_{SYS}$, through $V_{VREV_FB}$. When $V_{VREV_FB}$ rises above regulation target and exceeds $V_{REV_OV}$, the device stops switching, and waits for the voltage to fall below $V_{REV_OVZ}$ to resume switching. An INT pulse is asserted to the host.

#### 7.3.10.1.5 DRV_SUP Under-voltage and Over-voltage Protection (DRV_OKZ)

The DRV_SUP pin must maintain a valid voltage between DRV_UVP and DRV_OVP for proper operation of the switching power converter stage. This is true both in charging mode and in reverse mode.

When DRV_SUP pin voltage falls below DRV_UVP threshold, the switching converter stops operation, an INT pulse is asserted to signal the host, the DRV_OKZ_STAT, and DRV_OKZ_FLAG bits are set to signal the fault.

When DRV_SUP pin voltage rises above DRV_OVP threshold, the switching converter stops operation, an INT pulse is asserted to signal the host, the DRV_OKZ_STAT, and DRV_OKZ_FLAG bit are set to signal the fault.

When the DRV pin returns to normal operating range, the device automatically resumes switching in either charging or reverse mode as configured before the fault.

#### 7.3.10.1.6 REGN Under-voltage Protection (REGN_OKZ)

The REGN pin is driven by an internal regulator, and must maintain a voltage above REGN_OKZ for proper device operation. This is true both in charging mode and in reverse mode, and for the ADC to function in battery only mode.

If the internal regulator is overloaded externally, the pin voltage can drop. When REGN falls below REGN_OKZ threshold, the switching converter stops operation. When the fault is removed, the REGN voltage recovers automatically and switching resumes in either charging or reverse mode as configured before the fault.

### 7.3.10.2 Thermal Shutdown (TSHUT)

The device has thermal shutdown to turn off the converter when IC surface temperature exceeds TSHUT. The fault register bits TSHUT_STAT and TSHUT_FLAG are set and an INT pulse is asserted to the host. The converter turns back on when IC temperature is below TSHUT_HYS. Note that TSHUT protection is active both in charging and reverse mode of operation.

## 7.3.11 Serial Interface

The device uses $I^2C$ compatible interface for flexible charging parameter programming and instantaneous device status reporting. $I^2C$ is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as controllers or targets when performing data transfers. A controller is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with address 0x6, receiving control inputs from the controller device like a micro-controller or digital signal processor through the registers defined in the Register Map. Registers read outside those defined in the map, return 0xFF. The $I^2C$ interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s), and fast mode plus (up to 1 Mbit/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

All 16-bit registers are defined as Little Endian, with the most-significant byte allocated to the higher address. 16-bit register writes must be done sequentially and are recommended to be programmed using multi-write approach described in the Section 7.3.11.7.

### 7.3.11.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

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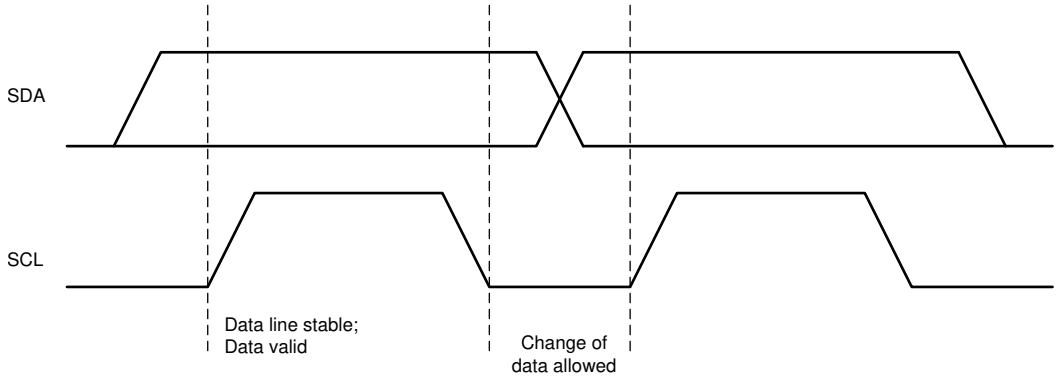


**Figure 7-7. Bit Transfers on the I²C Bus**

#### 7.3.11.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition. When timeout condition is met, for example START condition is active for more than 2 seconds and there is no STOP condition triggered, the charger I²C communication automatically resets and communication lines are free for another transmission.

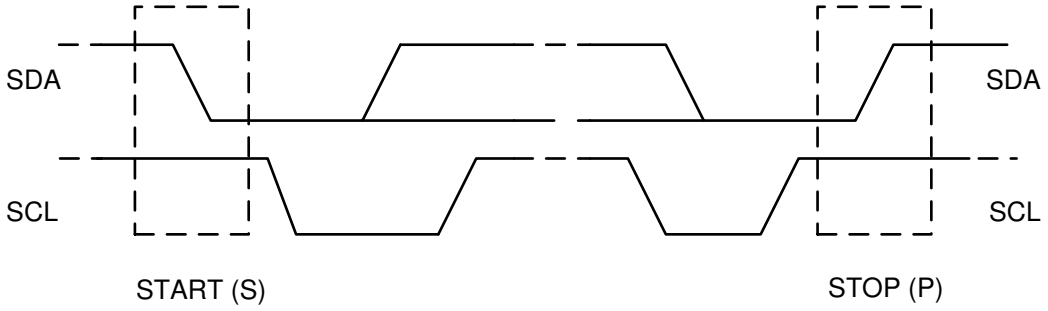


**Figure 7-8. START and STOP Conditions on the I²C Bus**

#### 7.3.11.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first.

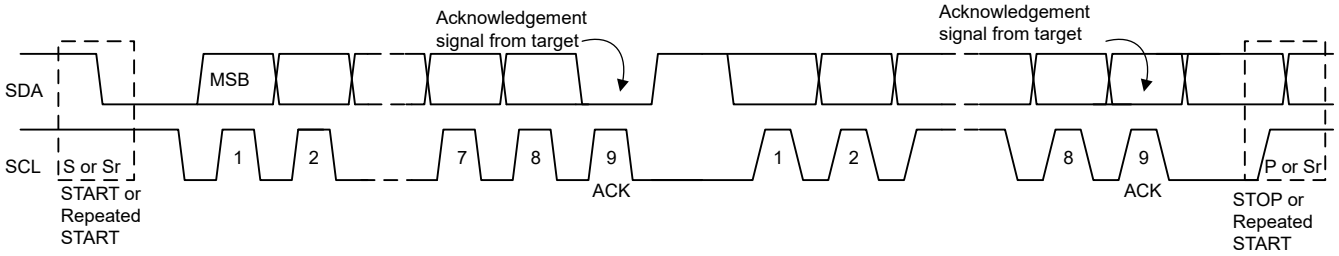


**Figure 7-9. Data Transfer on the I²C Bus**


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#### 7.3.11.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the target to signal the controller that the byte is successfully received and another byte can be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The controller releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

#### 7.3.11.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B) by default.

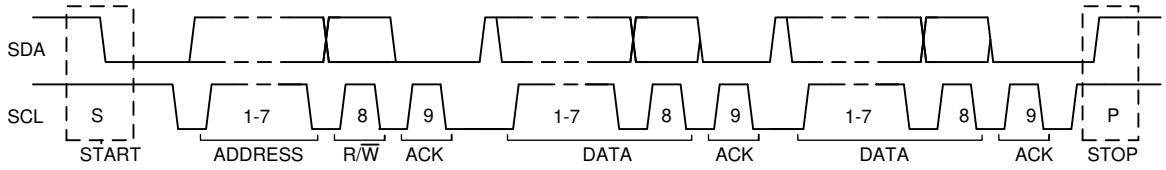


**Figure 7-10. Complete Data Transfer on the I²C Bus**

#### 7.3.11.6 Single Write and Read

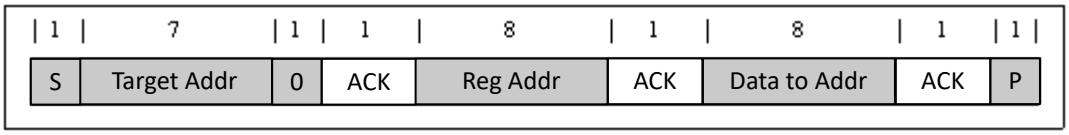


**Figure 7-11. Single Write**

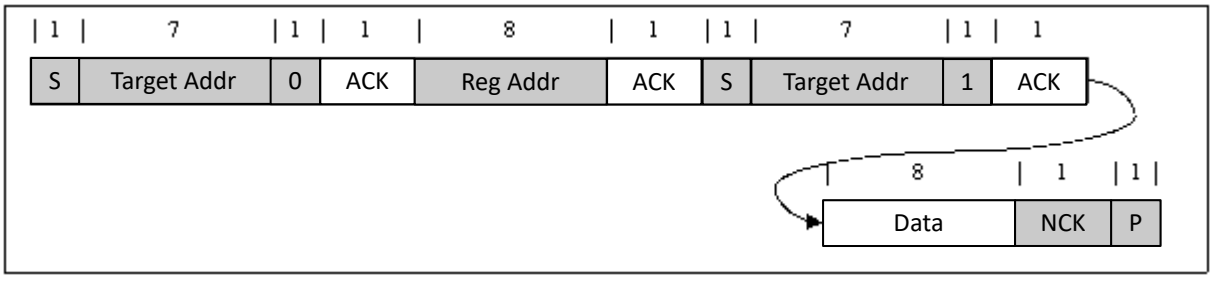


**Figure 7-12. Single Read**

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

#### 7.3.11.7 Multi-Write and Multi-Read

The charger device supports multi-read and multi-write of all registers.

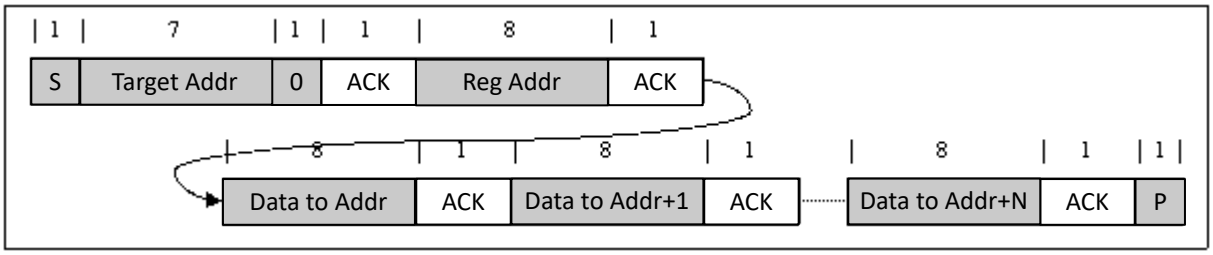


**Figure 7-13. Multi-Write**

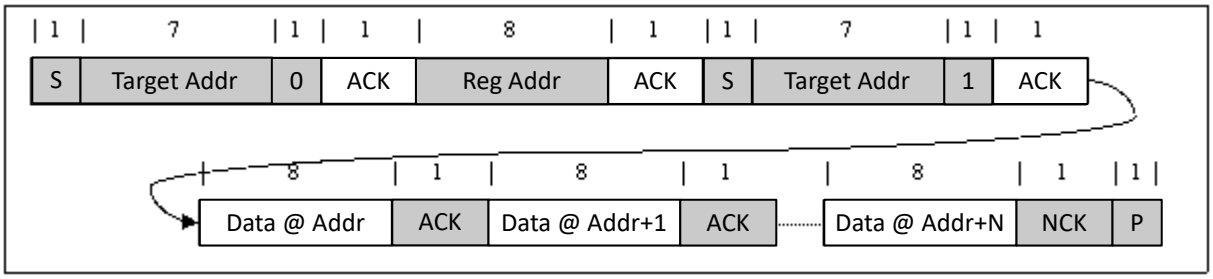


**Figure 7-14. Multi-Read**

## 7.4 Device Functional Modes

### *7.4.1 Host Mode and Default Mode*

The device is a host controlled charger, but the device can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and a $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit reads as a '1' upon the first read and then '0' upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

A write to any $I^2C$ register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and select registers are reset to default values as detailed in the Register Map section. The Watchdog timer is reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and /INT is asserted low to alert the host (unless masked by WD_MASK).


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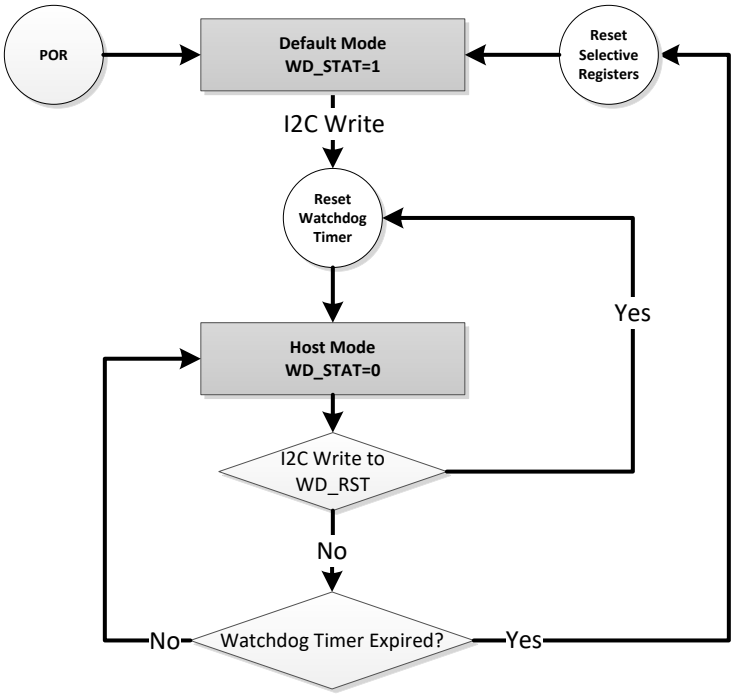


**Figure 7-15. Watchdog Timer Flow Chart**

### *7.4.2 Register Bit Reset*

Beside the register reset by the watchdog timer in the default mode, the register and the timer can be reset to the default value by writing the REG_RST bit to 1. The register bits which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

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## 7.5 BQ25853Q1 Registers

Table 7-7 lists the memory-mapped registers for the BQ25853Q1 registers. All register offset addresses not listed in Table 7-7 should be considered as reserved locations and the register contents should not be modified.

**Table 7-7. BQ25853Q1 Registers**

| Address | Acronym | Register Name | Section |
|---|---|---|---|
| 0x0 | REG0x00_Charge_Voltage_Limit | Charge Voltage Limit | Go |
| 0x2 | REG0x02_Charge_Current_Limit | Charge Current Limit | Go |
| 0x6 | REG0x06_Input_Current_DPM_Limit | Input Current DPM Limit | Go |
| 0x8 | REG0x08_Input_Voltage_DPM_Limit | Input Voltage DPM Limit | Go |
| 0xA | REG0x0A_Reverse_Mode_Input_Current_Limit | Reverse Mode Input Current Limit | Go |
| 0x10 | REG0x10_Precharge_Current_Limit | Precharge Current Limit | Go |
| 0x12 | REG0x12_Termination_Current_Limit | Termination Current Limit | Go |
| 0x14 | REG0x14_Precharge_and_Termination_Control | Precharge and Termination Control | Go |
| 0x15 | REG0x15_Timer_Control | Timer Control | Go |
| 0x17 | REG0x17_Charger_Control | Charger Control | Go |
| 0x18 | REG0x18_Pin_Control | Pin Control | Go |
| 0x19 | REG0x19_Power_Path_and_Reverse_Mode_Control | Power Path and Reverse Mode Control | Go |
| 0x1A | REG0x1A_Frequency_Dither_Control | Frequency Dither Control | Go |
| 0x1B | REG0x1B_TS_Charging_Threshold_Control | TS Charging Threshold Control | Go |
| 0x1C | REG0x1C_TS_Charging_Region_Behavior_Control | TS Charging Region Behavior Control | Go |
| 0x1D | REG0x1D_TS_Reverse_Mode_Threshold_Control | TS Reverse Mode Threshold Control | Go |
| 0x21 | REG0x21_Charger_Status_1 | Charger Status 1 | Go |
| 0x22 | REG0x22_Charger_Status_2 | Charger Status 2 | Go |
| 0x23 | REG0x23_Charger_Status_3 | Charger Status 3 | Go |
| 0x24 | REG0x24_Fault_Status | Fault Status | Go |
| 0x25 | REG0x25_Charger_Flag_1 | Charger Flag 1 | Go |
| 0x26 | REG0x26_Charger_Flag_2 | Charger Flag 2 | Go |
| 0x27 | REG0x27_Fault_Flag | Fault Flag | Go |
| 0x28 | REG0x28_Charger_Mask_1 | Charger Mask 1 | Go |
| 0x29 | REG0x29_Charger_Mask_2 | Charger Mask 2 | Go |
| 0x2A | REG0x2A_Fault_Mask | Fault Mask | Go |
| 0x2B | REG0x2B_ADC_Control | ADC Control | Go |
| 0x2C | REG0x2C_ADC_Channel_Control | ADC Channel Control | Go |
| 0x2D | REG0x2D_IAC_ADC | IAC ADC | Go |
| 0x2F | REG0x2F_IBAT_ADC | IBAT ADC | Go |
| 0x31 | REG0x31_VAC_ADC | VAC ADC | Go |
| 0x33 | REG0x33_VBAT_ADC | VBAT ADC | Go |
| 0x35 | REG0x35_VSYS_ADC | VSYS ADC | Go |
| 0x37 | REG0x37_TS_ADC | TS ADC | Go |
| 0x39 | REG0x39_VFB_ADC | VFB ADC | Go |
| 0x3B | REG0x3B_Gate_Driver_Strength_Control | Gate Driver Strength Control | Go |
| 0x3C | REG0x3C_Gate_Driver_Dead_Time_Control | Gate Driver Dead Time Control | Go |


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**Table 7-7. BQ25853Q1 Registers (continued)**

| Address | Acronym | Register Name | Section |
|---|---|---|---|
| 0x3D | REG0x3D_Part_Information | Part Information | Go |
| 0x62 | REG0x62_Reverse_Mode_Battery_Discharge_Current | Reverse Mode Battery Discharge Current | Go |

Complex bit access types are encoded to fit into small table cells. Table 7-8 shows the codes that are used for access types in this section.

**Table 7-8. BQ25853Q1 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 7.5.1 REG0x00_Charge_Voltage_Limit Register (Address = 0x0) [Reset = 0x0010]

REG0x00_Charge_Voltage_Limit is shown in Figure 7-16 and described in Table 7-9.

Return to the Summary Table.

I2C REG0x01=[15:8], I2C REG0x00=[7:0]

**Figure 7-16. REG0x00_Charge_Voltage_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | VFB_REG | | | | |
| R-0x0 | | | R/W-0x10 | | | | |

**Table 7-9. REG0x00_Charge_Voltage_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:5 | RESERVED | R | 0x0 | | Reserved |
| 4:0 | VFB_REG | R/W | 0x10 | Reset by:<br>REG_RESET | FB Voltage Regulation Limit:<br>POR: 1536mV (10h)<br>Range: 1504mV-1566mV (0h-1Fh)<br>Bit Step: 2mV<br>Offset: 1504mV |

### 7.5.2 REG0x02_Charge_Current_Limit Register (Address = 0x2) [Reset = 0x0640]

REG0x02_Charge_Current_Limit is shown in Figure 7-17 and described in Table 7-10.

Return to the Summary Table.

I2C REG0x03=[15:8], I2C REG0x02=[7:0]

**Figure 7-17. REG0x02_Charge_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | ICHG_REG | | |
| R-0x0 | | | | | R/W-0x190 | | |

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**Figure 7-17. REG0x02_Charge_Current_Limit Register (continued)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ICHG_REG | | | | | | RESERVED | |
| R/W-0x190 | | | | | | R-0x0 | |

**Table 7-10. REG0x02_Charge_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:11 | RESERVED | R | 0x0 | | Reserved |
| 10:2 | ICHG_REG | R/W | 0x190 | Reset by:<br>REG_RESET<br>WATCHDOG | Fast Charge Current Regulation Limit with 2.5mΩ RBAT_SNS:<br>Actual charge current is the lower of ICHG_REG and ICHG pin<br>POR: 40000mA (190h)<br>Range: 800mA-40000mA (8h-190h)<br>Clamped Low<br>Clamped High<br>Bit Step: 100mA |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.3 REG0x06_Input_Current_DPM_Limit Register (Address = 0x6) [Reset = 0x0640]

REG0x06_Input_Current_DPM_Limit is shown in Figure 7-18 and described in Table 7-11.

Return to the Summary Table.

I2C REG0x07=[15:8], I2C REG0x06=[7:0]

**Figure 7-18. REG0x06_Input_Current_DPM_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | IAC_DPM | |
| R-0x0 | | | | | | R/W-0x190 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IAC_DPM | | | | | | RESERVED | |
| R/W-0x190 | | | | | | R-0x0 | |

**Table 7-11. REG0x06_Input_Current_DPM_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:11 | RESERVED | R | 0x0 | | Reserved |
| 10:2 | IAC_DPM | R/W | 0x190 | Reset by:<br>REG_RESET | Input Current DPM Regulation Limit with 2mΩ RAC_SNS:<br>Actual input current limit is the lower of IAC_DPM and ILIM_HIZ pin<br>POR: 50000mA (190h)<br>Range: 1000mA-50000mA (8h-190h)<br>Clamped Low<br>Clamped High<br>Bit Step: 125mA |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.4 REG0x08_Input_Voltage_DPM_Limit Register (Address = 0x8) [Reset = 0x0348]

REG0x08_Input_Voltage_DPM_Limit is shown in Figure 7-19 and described in Table 7-12.

Return to the Summary Table.

I2C REG0x09=[15:8], I2C REG0x08=[7:0]


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**Figure 7-19. REG0x08_Input_Voltage_DPM_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | VAC_DPM | | | | | |
| R-0x0 | | R/W-0xD2 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VAC_DPM | | | | | | RESERVED | |
| R/W-0xD2 | | | | | | R-0x0 | |

**Table 7-12. REG0x08_Input_Voltage_DPM_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:14 | RESERVED | R | 0x0 | | Reserved |
| 13:2 | VAC_DPM | R/W | 0xD2 | Reset by:<br>REG_RESET | Input Voltage Regulation Limit:<br>POR: 4200mV (D2h)<br>Range: 4200mV-65000mV (D2h-CB2h)<br>Clamped Low<br>Clamped High<br>Bit Step: 20mV |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.5 REG0x0A_Reverse_Mode_Input_Current_Limit Register (Address = 0xA) [Reset = 0x0640]

REG0x0A_Reverse_Mode_Input_Current_Limit is shown in Figure 7-20 and described in Table 7-13.

Return to the Summary Table.

I2C REG0x0B=[15:8], I2C REG0x0A=[7:0]

**Figure 7-20. REG0x0A_Reverse_Mode_Input_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | IAC_REV | | |
| R-0x0 | | | | | R/W-0x190 | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IAC_REV | | | | | | RESERVED | |
| R/W-0x190 | | | | | | R-0x0 | |

**Table 7-13. REG0x0A_Reverse_Mode_Input_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:11 | RESERVED | R | 0x0 | | Reserved |
| 10:2 | IAC_REV | R/W | 0x190 | Reset by:<br>REG_RESET | Input Current Regulation in Reverse Mode with 2mΩ RAC_SNS:<br>POR: 50000mA (190h)<br>Range: 1000mA-50000mA (8h-190h)<br>Clamped Low<br>Clamped High<br>Bit Step: 125mA |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.6 REG0x10_Precharge_Current_Limit Register (Address = 0x10) [Reset = 0x0140]

REG0x10_Precharge_Current_Limit is shown in Figure 7-21 and described in Table 7-14.

Return to the Summary Table.

I2C REG0x11=[15:8], I2C REG0x10=[7:0]

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**Figure 7-21. REG0x10_Precharge_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | IPRECHG | |
| R-0x0 | | | | | | R/W-0x50 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IPRECHG | | | | | | RESERVED | |
| R/W-0x50 | | | | | | R-0x0 | |

**Table 7-14. REG0x10_Precharge_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:10 | RESERVED | R | 0x0 | | Reserved |
| 9:2 | IPRECHG | R/W | 0x50 | Actual pre-charge current is the lower of IPRECHG and ICHG pin<br>Reset by:<br>REG_RESET | Pre-charge current regulation limit with 2.5mΩ RBAT_SNS:<br>POR: 8000mA (50h)<br>Range: 500mA-20000mA (5h-C8h)<br>Clamped Low<br>Clamped High<br>Bit Step: 100mA |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.7 REG0x12_Termination_Current_Limit Register (Address = 0x12) [Reset = 0x00A0]

REG0x12_Termination_Current_Limit is shown in Figure 7-22 and described in Table 7-15.

Return to the Summary Table.

I2C REG0x13=[15:8], I2C REG0x12=[7:0]

**Figure 7-22. REG0x12_Termination_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | ITERM | |
| R-0x0 | | | | | | R/W-0x28 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ITERM | | | | | | RESERVED | |
| R/W-0x28 | | | | | | R-0x0 | |

**Table 7-15. REG0x12_Termination_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:10 | RESERVED | R | 0x0 | | Reserved |
| 9:2 | ITERM | R/W | 0x28 | Actual termination current is the lower of ITERM and ICHG pin if both functions enabled<br>Reset by:<br>REG_RESET | Termination Current Threshold with 2.5mΩ RBAT_SNS:<br>POR: 4000mA (28h)<br>Range: 500mA-20000mA (5h-C8h)<br>Clamped Low<br>Clamped High<br>Bit Step: 100mA |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.8 REG0x14_Precharge_and_Termination_Control Register (Address = 0x14) [Reset = 0x0E]

REG0x14_Precharge_and_Termination_Control is shown in Figure 7-23 and described in Table 7-16.

Return to the Summary Table.

**Figure 7-23. REG0x14_Precharge_and_Termination_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|


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**Figure 7-23. REG0x14_Precharge_and_Termination_Control Register (continued)**

| RESERVED | EN_TERM | VBAT_LOWV | EN_PRECHG |
|---|---|---|---|
| R-0x0 | R/W-0x1 | R/W-0x3 | R/W-0x0 |

**Table 7-16. REG0x14_Precharge_and_Termination_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:4 | RESERVED | R | 0x0 | | Reserved |
| 3 | EN_TERM | R/W | 0x1 | Reset by:<br>REG_RESET | Enable termination control<br>0b = Disable<br>1b = Enable |
| 2:1 | VBAT_LOWV | R/W | 0x3 | Reset by:<br>REG_RESET | Battery threshold for PRECHG to FASTCHG transition, as percentage of VFB_REG:<br>00b = 30% x VFB_REG<br>01b = 55% x VFB_REG<br>10b = 66.7% x VFB_REG<br>11b = 71.4% x VFB_REG |
| 0 | EN_PRECHG | R/W | 0x0 | Reset by:<br>REG_RESET | Enable pre-charge and BAT_SHORT functions:<br>0b = Disable<br>1b = Enable |

### 7.5.9 REG0x15_Timer_Control Register (Address = 0x15) [Reset = 0x15]

REG0x15_Timer_Control is shown in Figure 7-24 and described in Table 7-17.

Return to the Summary Table.

**Figure 7-24. REG0x15_Timer_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TOPOFF_TMR | | WATCHDOG | | EN_CHG_TMR | CHG_TMR | | EN_TMR2X |
| R/W-0x0 | | R/W-0x1 | | R/W-0x0 | R/W-0x2 | | R/W-0x1 |

**Table 7-17. REG0x15_Timer_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | TOPOFF_TMR | R/W | 0x0 | Reset by:<br>REG_RESET | Top-off timer control:<br>00b = Disable<br>01b = 15 mins<br>10b = 30 mins<br>11b = 45 mins |
| 5:4 | WATCHDOG | R/W | 0x1 | Reset by:<br>REG_RESET | Watchdog timer control:<br>00b = Disable<br>01b = 40s<br>10b = 80s<br>11b = 160s |
| 3 | EN_CHG_TMR | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Enable charge safety timer:<br>0b = Disable<br>1b = Enable |
| 2:1 | CHG_TMR | R/W | 0x2 | Reset by:<br>REG_RESET | Charge safety timer setting:<br>00b = 5hr<br>01b = 8hr<br>10b = 12hr<br>11b = 24hr |
| 0 | EN_TMR2X | R/W | 0x1 | Reset by:<br>REG_RESET | Charge safety timer speed in DPM:<br>0b = Timer always counts normally<br>1b = Timer slowed by 2x during input DPM |

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### 7.5.10 REG0x17_Charger_Control Register (Address = 0x17) [Reset = 0xC9]

REG0x17_Charger_Control is shown in Figure 7-25 and described in Table 7-18.

Return to the Summary Table.

**Figure 7-25. REG0x17_Charger_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VRECHG | | WD_RST | DIS_CE_PIN | EN_CHG_BIT_RESET_BEHAVIOR | EN_HIZ | EN_IBAT_LOAD | EN_CHG |
| R/W-0x3 | | R/W-0x0 | R/W-0x0 | R/W-0x1 | R/W-0x0 | R/W-0x0 | R/W-0x1 |

**Table 7-18. REG0x17_Charger_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | VRECHG | R/W | 0x3 | Reset by:<br>REG_RESET | Battery auto-recharge threshold, as percentage of VFB_REG:<br>00b = 93.0% x VFB_REG<br>01b = 94.3% x VFB_REG<br>10b = 95.2% x VFB_REG<br>11b = 97.6% x VFB_REG |
| 5 | WD_RST | R/W | 0x0 | Reset by:<br>REG_RESET | I2C Watchdog timer reset control:<br>0b = Normal<br>1b = Reset (bit goes back to 0 after timer reset) |
| 4 | DIS_CE_PIN | R/W | 0x0 | Reset by:<br>REG_RESET | /CE pin function disable:<br>0b = CE pin enabled<br>1b = CE pin disabled |
| 3 | EN_CHG_BIT_RESET_BEHAVIOR | R/W | 0x1 | Reset by:<br>REG_RESET | Controls the EN_CHG bit behavior when WATCHDOG expires:<br>0b = EN_CHG bit resets to 0<br>1b = EN_CHG bit resets to 1 |
| 2 | EN_HIZ | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG<br>Adapter Plug In | HIZ mode enable:<br>0b = Disable<br>1b = Enable |
| 1 | EN_IBAT_LOAD | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Battery Load (IBAT_LOAD) Enable:<br>Sinks current from SRN to GND. Recommend to disable IBAT ADC (IBAT_ADC_DIS = 1) while this bit is active.<br>0b = Disabled<br>1b = Enabled |
| 0 | EN_CHG | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Charge enable control:<br>0b = Disable<br>1b = Enable |

### 7.5.11 REG0x18_Pin_Control Register (Address = 0x18) [Reset = 0xC0]

REG0x18_Pin_Control is shown in Figure 7-26 and described in Table 7-19.

Return to the Summary Table.

**Figure 7-26. REG0x18_Pin_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN_ICHG_PIN | EN_ILIM_HIZ_PIN | DIS_PG_PIN | DIS_STAT_PINS | FORCE_STAT4_ON | FORCE_STAT3_ON | FORCE_STAT2_ON | FORCE_STAT1_ON |
| R/W-0x1 | R/W-0x1 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 |


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**Table 7-19. REG0x18_Pin_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | EN_ICHG_PIN | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | ICHG pin function enable:<br>0b = ICHG pin disabled<br>1b = ICHG pin enabled |
| 6 | EN_ILIM_HIZ_PIN | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | ILIM_HIZ pin function enable:<br>0b = ILIM_HIZ pin disabled<br>1b = ILIM_HIZ pin enabled |
| 5 | DIS_PG_PIN | R/W | 0x0 | Reset by:<br>REG_RESET | PG pin function disable:<br>0b = PG pin enabled<br>1b = PG pin disabled |
| 4 | DIS_STAT_PINS | R/W | 0x0 | Reset by:<br>REG_RESET | STAT1, STAT2 pin function disable:<br>0b = STAT pins enabled<br>1b = STAT pins disabled |
| 3 | FORCE_STAT4_ON | R/W | 0x0 | Reset by:<br>REG_RESET | CE_STAT4 pin override:<br>Can only be forced on if DIS_CE_PIN = 1<br>0b = CE_STAT4 open-drain off<br>1b = CE_STAT4 pulls LOW |
| 2 | FORCE_STAT3_ON | R/W | 0x0 | Reset by:<br>REG_RESET | PG_STAT3 pin override:<br>Can only be forced on if DIS_PG_PIN = 1<br>0b = PG_STAT3 open-drain off<br>1b = PG_STAT3 pulls LOW |
| 1 | FORCE_STAT2_ON | R/W | 0x0 | Reset by:<br>REG_RESET | STAT2 pin override:<br>Can only be forced on if DIS_STAT_PINS = 1<br>0b = STAT2 open-drain off<br>1b = STAT2 pulls LOW |
| 0 | FORCE_STAT1_ON | R/W | 0x0 | Reset by:<br>REG_RESET | STAT1 pin override:<br>Can only be forced on if DIS_STAT_PINS = 1<br>0b = STAT1 open-drain off<br>1b = STAT1 pulls LOW |

### 7.5.12 REG0x19_Power_Path_and_Reverse_Mode_Control Register (Address = 0x19) [Reset = 0x07]

REG0x19_Power_Path_and_Reverse_Mode_Control is shown in Figure 7-27 and described in Table 7-20.

Return to the Summary Table.

**Figure 7-27. REG0x19_Power_Path_and_Reverse_Mode_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG_RST | EN_IAC_LOAD | EN_PFM | FORCE_BATFET_OFF | BATFET_REDUCE_VDRV | TEST_BIT | EN_AUTO_REV | EN_REV |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x1 | R/W-0x1 | R/W-0x1 |

**Table 7-20. REG0x19_Power_Path_and_Reverse_Mode_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | REG_RST | R/W | 0x0 | Reset by:<br>REG_RESET | Register reset to default values:<br>0b = Not reset<br>1b = Reset (bit goes back to 0 after register reset) |
| 6 | EN_IAC_LOAD | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | VAC Load (IAC_LOAD) Enable:<br>0b = Disabled<br>1b = Enabled |

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**Table 7-20. REG0x19_Power_Path_and_Reverse_Mode_Control Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5 | EN_PFM | R/W | 0x0 | It is recommended to disable PFM when ITERM < 2A<br>Reset by:<br>REG_RESET | Enable PFM mode in light-load:<br>Note this bit is reset upon a valid SYNC signal detection on FSW_SYNC pin. Host can set this bit back to 1 to force PFM operation even with a valid SYNC input<br>0b = Disable (FPWM operation)<br>1b = Enable (PFM operation) |
| 4 | FORCE_BATFET_OFF | R/W | 0x0 | Reset by:<br>REG_RESET<br>Adapter Plug In | Force BATFET off control:<br>0b = Allow normal BATFET operation<br>1b = Force BATFET off |
| 3 | BATFET_REDUCE_VDRV | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | BATFET Drive Voltage Select:<br>0b = 10V<br>1b = 7V |
| 2 | TEST_BIT | R/W | 0x1 | Reset by:<br>REG_RESET | |
| 1 | EN_AUTO_REV | R/W | 0x1 | To exit reverse mode, it is recommended to clear both EN_AUTO_REV and EN_REV bits<br>Reset by:<br>REG_RESET<br>WATCHDOG | Auto Reverse Mode enable:<br>0b = Disable Auto Reverse<br>1b = Enable Auto Reverse |
| 0 | EN_REV | R/W | 0x1 | To exit reverse mode, it is recommended to clear both EN_AUTO_REV and EN_REV bits<br>Reset by:<br>REG_RESET<br>WATCHDOG<br>Adapter Plug In | Reverse Mode control:<br>0b = Disable<br>1b = Enable |

### 7.5.13 REG0x1A_Frequency_Dither_Control Register (Address = 0x1A) [Reset = 0x00]

REG0x1A_Frequency_Dither_Control is shown in Figure 7-28 and described in Table 7-21.

Return to the Summary Table.

**Figure 7-28. REG0x1A_Frequency_Dither_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | EN_DITHER | | RESERVED | | |
| R-0x0 | | | R/W-0x0 | | R-0x0 | | |

**Table 7-21. REG0x1A_Frequency_Dither_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:5 | RESERVED | R | 0x0 | | Reserved |
| 4:3 | EN_DITHER | R/W | 0x0 | Reset by:<br>REG_RESET | DRSS Enable<br>00b = Disable<br>01b = 1X<br>10b = 2X<br>11b = 3X |
| 2:0 | RESERVED | R | 0x0 | | Reserved |


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### 7.5.14 REG0x1B_TS_Charging_Threshold_Control Register (Address = 0x1B) [Reset = 0x96]

REG0x1B_TS_Charging_Threshold_Control is shown in Figure 7-29 and described in Table 7-22.

Return to the Summary Table.

**Figure 7-29. REG0x1B_TS_Charging_Threshold_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_T5 | | TS_T3 | | TS_T2 | | TS_T1 | |
| R/W-0x2 | | R/W-0x1 | | R/W-0x1 | | R/W-0x2 | |

**Table 7-22. REG0x1B_TS_Charging_Threshold_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | TS_T5 | R/W | 0x2 | Reset by: REG_RESET | TS T5 (HOT) threshold control:<br>00b = 41.2% (50C)<br>01b = 37.7% (55C)<br>10b = 34.375% (60C)<br>11b = 31.25%(65C) |
| 5:4 | TS_T3 | R/W | 0x1 | Reset by: REG_RESET | JEITA TS T3 (WARM) threshold control:<br>00b = 48.4% (40C)<br>01b = 44.8% (45C)<br>10b = 41.2% (50C)<br>11b = 37.7% (55C) |
| 3:2 | TS_T2 | R/W | 0x1 | Reset by: REG_RESET | JEITA TS T2 (COOL) threshold control:<br>00b = 71.1% (5C)<br>01b = 68.4% (10C)<br>10b = 65.5% (15C)<br>11b = 62.4% (20C) |
| 1:0 | TS_T1 | R/W | 0x2 | Reset by: REG_RESET | TS T1 (COLD) threshold control:<br>00b = 77.15% (-10C)<br>01b = 75.32% (-5C)<br>10b = 73.25% (0C)<br>11b = 71.1% (5C) |

### 7.5.15 REG0x1C_TS_Charging_Region_Behavior_Control Register (Address = 0x1C) [Reset = 0x57]

REG0x1C_TS_Charging_Region_Behavior_Control is shown in Figure 7-30 and described in Table 7-23.

Return to the Summary Table.

**Figure 7-30. REG0x1C_TS_Charging_Region_Behavior_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | JEITA_VSET | | JEITA_ISETH | JEITA_ISETC | | EN_JEITA | EN_TS |
| R-0x0 | R/W-0x2 | | R/W-0x1 | R/W-0x1 | | R/W-0x1 | R/W-0x1 |

**Table 7-23. REG0x1C_TS_Charging_Region_Behavior_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | | Reserved |
| 6:5 | JEITA_VSET | R/W | 0x2 | Reset by: REG_RESET | JEITA Warm (T3 < TS < T5) regulation voltage setting, as percentage of VFB_REG:<br>00b = Charge Suspend<br>01b = 94.3% x VFB_REG<br>10b = 97.6% x VFB_REG<br>11b = 100% x VFB_REG |
| 4 | JEITA_ISETH | R/W | 0x1 | Reset by: REG_RESET | JEITA Warm (T3 < TS < T5) regulation current setting, as percentage of ICHG_REG:<br>0b = 40% x ICHG_REG<br>1b = 100% x ICHG_REG |

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**Table 7-23. REG0x1C_TS_Charging_Region_Behavior_Control Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 3:2 | JEITA_ISETC | R/W | 0x1 | Reset by:<br>REG_RESET | JEITA Cool (T1 < TS < T2) regulation current setting, as percentage of ICHG_REG:<br>00b = Charge Suspend<br>01b = 20% x ICHG_REG<br>10b = 40% x ICHG_REG<br>11b = 100% x ICHG_REG |
| 1 | EN_JEITA | R/W | 0x1 | Reset by:<br>REG_RESET | JEITA profile control:<br>0b = Disabled (COLD/HOT control only)<br>1b = Enabled (COLD/COOL/WARM/HOT control) |
| 0 | EN_TS | R/W | 0x1 | Reset by:<br>REG_RESET | TS pin function control (applies to forward charging and reverse discharging modes):<br>0b = Disabled (ignore TS pin)<br>1b = Enabled |

### 7.5.16 REG0x1D_TS_Reverse_Mode_Threshold_Control Register (Address = 0x1D) [Reset = 0x40]

REG0x1D_TS_Reverse_Mode_Threshold_Control is shown in Figure 7-31 and described in Table 7-24.

Return to the Summary Table.

**Figure 7-31. REG0x1D_TS_Reverse_Mode_Threshold_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BHOT | | BCOLD | RESERVED | | | | |
| R/W-0x1 | | R/W-0x0 | R-0x0 | | | | |

**Table 7-24. REG0x1D_TS_Reverse_Mode_Threshold_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | BHOT | R/W | 0x1 | Reset by:<br>REG_RESET | Reverse Mode TS HOT temperature threshold control:<br>00b = 37.7% (55C)<br>01b = 34.2% (60C)<br>10b = 31.25%(65C)<br>11b = Disable |
| 5 | BCOLD | R/W | 0x0 | Reset by:<br>REG_RESET | Reverse Mode TS COLD temperature threshold control:<br>0b = 77.15% (-10C)<br>1b = 80% (-20C) |
| 4:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.17 REG0x21_Charger_Status_1 Register (Address = 0x21) [Reset = 0x00]

REG0x21_Charger_Status_1 is shown in Figure 7-32 and described in Table 7-25.

Return to the Summary Table.

**Figure 7-32. REG0x21_Charger_Status_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_DONE_STAT | IAC_DPM_STAT | VAC_DPM_STAT | RESERVED | WD_STAT | CHARGE_STAT | | |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | | |

**Table 7-25. REG0x21_Charger_Status_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | ADC_DONE_STAT | R | 0x0 | | ADC conversion status (in one-shot mode only):<br>0b = Conversion not complete<br>1b = Conversion complete |


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**Table 7-25. REG0x21_Charger_Status_1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | IAC_DPM_STAT | R | 0x0 | | Input Current regulation status:<br>0b = Normal<br>1b = In Input Current regulation (ILIM pin or IAC_DPM) |
| 5 | VAC_DPM_STAT | R | 0x0 | | Input Voltage regulation status:<br>0b = Normal<br>1b = In Input Voltage regulation |
| 4 | RESERVED | R | 0x0 | | Reserved |
| 3 | WD_STAT | R | 0x0 | | I2C Watchdog timer status:<br>0b = Normal<br>1b = WD timer expired |
| 2:0 | CHARGE_STAT | R | 0x0 | | Charge cycle status:<br>000b = Not charging<br>001b = Trickle Charge (VBAT < VBAT_SHORT)<br>010b = Pre-Charge (VBAT < VBAT_LOWV)<br>011b = Fast Charge (CC mode)<br>100b = Taper Charge (CV mode)<br>101b = Float Charge<br>110b = Top-off Timer Charge<br>111b = Charge Termination Done |

### 7.5.18 REG0x22_Charger_Status_2 Register (Address = 0x22) [Reset = 0x00]

REG0x22_Charger_Status_2 is shown in Figure 7-33 and described in Table 7-26.

Return to the Summary Table.

**Figure 7-33. REG0x22_Charger_Status_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PG_STAT | TS_STAT | | | RESERVED | | | |
| R-0x0 | R-0x0 | | | R-0x0 | | | |

**Table 7-26. REG0x22_Charger_Status_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | PG_STAT | R | 0x0 | | Input Power Good status:<br>0b = Not Power Good<br>1b = Power Good |
| 6:4 | TS_STAT | R | 0x0 | | TS (Battery NTC) status:<br>000b = Normal<br>001b = TS Warm<br>010b = TS Cool<br>011b = TS Cold<br>100b = TS Hot |
| 3:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.19 REG0x23_Charger_Status_3 Register (Address = 0x23) [Reset = 0x00]

REG0x23_Charger_Status_3 is shown in Figure 7-34 and described in Table 7-27.

Return to the Summary Table.

**Figure 7-34. REG0x23_Charger_Status_3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | FSW_SYNC_STAT | | RESERVED | REVERSE_STAT | RESERVED | BATFET_STAT |
| R-0x0 | | R-0x0 | | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

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**Figure 7-34. REG0x23_Charger_Status_3 Register (continued)**

**Table 7-27. REG0x23_Charger_Status_3 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | RESERVED | R | 0x0 | | Reserved |
| 5:4 | FSW_SYNC_STAT | R | 0x0 | | FSW_SYNC pin status:<br>00b = Normal, no external clock detected<br>01b = Valid ext. clock detected<br>10b = Pin fault (frequency out-of-range)<br>11b = Reserved |
| 3 | RESERVED | R | 0x0 | | Reserved |
| 2 | REVERSE_STAT | R | 0x0 | | Converter Reverse Mode status:<br>0b = Reverse Mode off<br>1b = Reverse Mode On |
| 1 | RESERVED | R | 0x0 | | Reserved |
| 0 | BATFET_STAT | R | 0x0 | | BATFET driver status:<br>0b = BATFET off<br>1b = BATFET on |

### 7.5.20 REG0x24_Fault_Status Register (Address = 0x24) [Reset = 0x00]

REG0x24_Fault_Status is shown in Figure 7-35 and described in Table 7-28.

Return to the Summary Table.

**Figure 7-35. REG0x24_Fault_Status Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VAC_UV_STAT | VAC_OV_STAT | IBAT_OCP_STAT | RESERVED | TSHUT_STAT | CHG_TMR_STAT | DRV_OKZ_STAT | RESERVED |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 7-28. REG0x24_Fault_Status Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VAC_UV_STAT | R | 0x0 | | Input under-voltage status:<br>0b = Input Normal<br>1b = Device in Input under-voltage protection |
| 6 | VAC_OV_STAT | R | 0x0 | | Input over-voltage status:<br>0b = Input Normal<br>1b = Device in Input over-voltage protection |
| 5 | IBAT_OCP_STAT | R | 0x0 | | Battery over-current status:<br>0b = Battery current normal<br>1b = Battery over-current detected |
| 4 | RESERVED | R | 0x0 | | Reserved |
| 3 | TSHUT_STAT | R | 0x0 | | Thermal shutdown status:<br>0b = Normal<br>1b = Device in thermal shutdown protection |
| 2 | CHG_TMR_STAT | R | 0x0 | | Charge safety timer status:<br>0b = Normal<br>1b = Charge safety timer expired |
| 1 | DRV_OKZ_STAT | R | 0x0 | In battery-only mode with ADC disabled, this bit always reads '1' | DRV_SUP pin voltage status:<br>0b = Normal<br>1b = DRV_SUP pin voltage is out of valid range |
| 0 | RESERVED | R | 0x0 | | Reserved |


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### 7.5.21 REG0x25_Charger_Flag_1 Register (Address = 0x25) [Reset = 0x00]

REG0x25_Charger_Flag_1 is shown in Figure 7-36 and described in Table 7-29.

Return to the Summary Table.

**Figure 7-36. REG0x25_Charger_Flag_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_DONE_FLAG | IAC_DPM_FLAG | VAC_DPM_FLAG | RESERVED | WD_FLAG | RESERVED | RESERVED | CHARGE_FLAG |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 7-29. REG0x25_Charger_Flag_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | ADC_DONE_FLAG | R | 0x0 | | ADC conversion INT flag (in one-shot mode only):<br>Note: always reads 0 in continuous mode<br>Access: R (ClearOnRead)<br>0b = Conversion not complete<br>1b = Conversion complete |
| 6 | IAC_DPM_FLAG | R | 0x0 | | Input Current regulation INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Device entered Input Current regulation |
| 5 | VAC_DPM_FLAG | R | 0x0 | | Input Voltage regulation INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Device entered Input Voltage regulation |
| 4 | RESERVED | R | 0x0 | | Reserved |
| 3 | WD_FLAG | R | 0x0 | | I2C Watchdog timer INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = WD_STAT rising edge detected |
| 2 | RESERVED | R | 0x0 | | Reserved |
| 1 | RESERVED | R | 0x0 | | Reserved |
| 0 | CHARGE_FLAG | R | 0x0 | | Charge cycle INT flag:<br>Access: R (ClearOnRead)<br>0b = Not charging<br>1b = CHARGE_STAT[2:0] bits changed (transition to any state) |

### 7.5.22 REG0x26_Charger_Flag_2 Register (Address = 0x26) [Reset = 0x00]

REG0x26_Charger_Flag_2 is shown in Figure 7-37 and described in Table 7-30.

Return to the Summary Table.

**Figure 7-37. REG0x26_Charger_Flag_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PG_FLAG | RESERVED | BATFET_FLAG | TS_FLAG | REVERSE_FLAG | RESERVED | FSW_SYNC_FLAG | RESERVED |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 7-30. REG0x26_Charger_Flag_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | PG_FLAG | R | 0x0 | | Input Power Good INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = PG signal toggle detected |

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**Table 7-30. REG0x26_Charger_Flag_2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | RESERVED | R | 0x0 | | Reserved |
| 5 | BATFET_FLAG | R | 0x0 | | BATFET driver INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = BATFET signal toggle detected |
| 4 | TS_FLAG | R | 0x0 | | TS (Battery NTC) INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = TS_STAT[2:0] bits changed (transitioned to any state) |
| 3 | REVERSE_FLAG | R | 0x0 | | Reverse Mode INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Reverse Mode toggle detected |
| 2 | RESERVED | R | 0x0 | | Reserved |
| 1 | FSW_SYNC_FLAG | R | 0x0 | | FSW_SYNC pin signal INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = FSW_SYNC status changed |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.23 REG0x27_Fault_Flag Register (Address = 0x27) [Reset = 0x00]

REG0x27_Fault_Flag is shown in Figure 7-38 and described in Table 7-31.

Return to the Summary Table.

**Figure 7-38. REG0x27_Fault_Flag Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VAC_UV_FLAG | VAC_OV_FLAG | IBAT_OCP_FLAG | RESERVED | TSHUT_FLAG | CHG_TMR_FLAG | DRV_OKZ_FLAG | RESERVED |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 7-31. REG0x27_Fault_Flag Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VAC_UV_FLAG | R | 0x0 | | Input under-voltage INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Entered input under-voltage fault |
| 6 | VAC_OV_FLAG | R | 0x0 | | Input over-voltage INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Entered Input over-voltage fault |
| 5 | IBAT_OCP_FLAG | R | 0x0 | | Battery over-current INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Entered Battery over-current fault |
| 4 | RESERVED | R | 0x0 | | Reserved |
| 3 | TSHUT_FLAG | R | 0x0 | | Thermal shutdown INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Entered TSHUT fault |


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**Table 7-31. REG0x27_Fault_Flag Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 2 | CHG_TMR_FLAG | R | 0x0 | | Charge safety timer INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = Charge Safety timer expired rising edge detected |
| 1 | DRV_OKZ_FLAG | R | 0x0 | | DRV_SUP pin voltage INT flag:<br>Access: R (ClearOnRead)<br>0b = Normal<br>1b = DRV_SUP pin fault detected |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.24 REG0x28_Charger_Mask_1 Register (Address = 0x28) [Reset = 0x00]

REG0x28_Charger_Mask_1 is shown in Figure 7-39 and described in Table 7-32.

Return to the Summary Table.

**Figure 7-39. REG0x28_Charger_Mask_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_DONE_MASK | IAC_DPM_MASK | VAC_DPM_MASK | RESERVED | WD_MASK | RESERVED | RESERVED | CHARGE_MASK |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 | R/W-0x0 | R-0x0 | R-0x0 | R/W-0x0 |

**Table 7-32. REG0x28_Charger_Mask_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | ADC_DONE_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | ADC conversion INT mask (in one-shot mode only):<br>0b = ADC_DONE produces INT pulse<br>1b = ADC_DONE does not produce INT pulse |
| 6 | IAC_DPM_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Input Current regulation INT mask:<br>0b = IAC_DPM_FLAG produces INT pulse<br>1b = IAC_DPM_FLAG does not produce INT pulse |
| 5 | VAC_DPM_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Input Voltage regulation INT mask:<br>0b = VAC_DPM_FLAG produces INT pulse<br>1b = VAC_DPM_FLAG does not produce INT pulse |
| 4 | RESERVED | R | 0x0 | | Reserved |
| 3 | WD_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | I2C Watchdog timer INT mask:<br>0b = WD expiration produces INT pulse<br>1b = WD expiration does not produce INT pulse |
| 2 | RESERVED | R | 0x0 | | Reserved |
| 1 | RESERVED | R | 0x0 | | Reserved |
| 0 | CHARGE_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Charge cycle INT mask:<br>0b = CHARGE_STAT change produces INT pulse<br>1b = CHARGE_STAT change does not produces INT pulse |

### 7.5.25 REG0x29_Charger_Mask_2 Register (Address = 0x29) [Reset = 0x00]

REG0x29_Charger_Mask_2 is shown in Figure 7-40 and described in Table 7-33.

Return to the Summary Table.

**Figure 7-40. REG0x29_Charger_Mask_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PG_MASK | RESERVED | BATFET_MASK | TS_MASK | REVERSE_MASK | RESERVED | FSW_SYNC_MASK | RESERVED |

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**Figure 7-40. REG0x29_Charger_Mask_2 Register (continued)**

| R/W-0x0 | R-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 | R/W-0x0 | R-0x0 |
|---|---|---|---|---|---|---|---|

**Table 7-33. REG0x29_Charger_Mask_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | PG_MASK | R/W | 0x0 | Reset by: REG_RESET | Input Power Good INT mask:<br>0b = PG toggle produces INT pulse<br>1b = PG toggle does not produce INT pulse |
| 6 | RESERVED | R | 0x0 | | Reserved |
| 5 | BATFET_MASK | R/W | 0x0 | Reset by: REG_RESET | BATFET driver INT mask:<br>0b = BATFET toggle produces INT pulse<br>1b = BATFET toggle does not produce INT pulse |
| 4 | TS_MASK | R/W | 0x0 | Reset by: REG_RESET | TS (Battery NTC) INT mask:<br>0b = TS_STAT change produces INT pulse<br>1b = TS_STAT change does not produce INT pulse |
| 3 | REVERSE_MASK | R/W | 0x0 | Reset by: REG_RESET | Reverse Mode INT mask:<br>0b = REVERSE_STAT toggle produces INT pulse<br>1b = REVERSE_STAT toggle does no produce INT pulse |
| 2 | RESERVED | R | 0x0 | | Reserved |
| 1 | FSW_SYNC_MASK | R/W | 0x0 | Reset by: REG_RESET | FSW_SYNC pin signal INT mask:<br>0b = FSW_SYNC status change produces INT pulse<br>1b = FSW_SYNC status change does not produce INT pulse |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.26 REG0x2A_Fault_Mask Register (Address = 0x2A) [Reset = 0x00]

REG0x2A_Fault_Mask is shown in Figure 7-41 and described in Table 7-34.

Return to the Summary Table.

**Figure 7-41. REG0x2A_Fault_Mask Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VAC_UV_MASK | VAC_OV_MASK | IBAT_OCP_MASK | RESERVED | TSHUT_MASK | CHG_TMR_MASK | DRV_OKZ_MASK | RESERVED |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 |

**Table 7-34. REG0x2A_Fault_Mask Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VAC_UV_MASK | R/W | 0x0 | Reset by: REG_RESET | Input under-voltage INT mask:<br>0b = Input under-voltage event produces INT pulse<br>1b = Input under-voltage event does not produce INT pulse |
| 6 | VAC_OV_MASK | R/W | 0x0 | Reset by: REG_RESET | Input over-voltage INT mask:<br>0b = Input over-voltage event produces INT pulse<br>1b = Input over-voltage event does not produce INT pulse |
| 5 | IBAT_OCP_MASK | R/W | 0x0 | Reset by: REG_RESET | Battery over-current INT mask:<br>0b = Battery over-current event produces INT pulse<br>1b = Battery over-current event does not produce INT pulse |
| 4 | RESERVED | R | 0x0 | | Reserved |


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**Table 7-34. REG0x2A_Fault_Mask Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 3 | TSHUT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Thermal shutdown INT mask:<br>0b = TSHUT event produces INT pulse<br>1b = TSHUT event does not produce INT pulse |
| 2 | CHG_TMR_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Charge safety timer INT mask:<br>0b = Timer expired rising edge produces INT pulse<br>1b = Timer expired rising edge does not produce INT pulse |
| 1 | DRV_OKZ_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | DRV_SUP pin voltage INT mask:<br>0b = DRV_SUP pin fault produces INT pulse<br>1b = DRV_SUP pin fault does not produce INT pulse |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.27 REG0x2B_ADC_Control Register (Address = 0x2B) [Reset = 0x60]

REG0x2B_ADC_Control is shown in Figure 7-42 and described in Table 7-35.

Return to the Summary Table.

**Figure 7-42. REG0x2B_ADC_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_EN | ADC_RATE | ADC_SAMPLE | | ADC_AVG | ADC_AVG_INIT | RESERVED | |
| R/W-0x0 | R/W-0x1 | R/W-0x2 | | R/W-0x0 | R/W-0x0 | R-0x0 | |

**Table 7-35. REG0x2B_ADC_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | ADC_EN | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | ADC control:<br>0b = Disable ADC<br>1b = Enable ADC |
| 6 | ADC_RATE | R/W | 0x1 | Reset by:<br>REG_RESET | ADC conversion rate control:<br>0b = Continuous conversion<br>1b = One-shot conversion |
| 5:4 | ADC_SAMPLE | R/W | 0x2 | Reset by:<br>REG_RESET | ADC sample speed:<br>00b = 15 bit effective resolution<br>01b = 14 bit effective resolution<br>10b = 13 bit effective resolution<br>11b = Reserved |
| 3 | ADC_AVG | R/W | 0x0 | Reset by:<br>REG_RESET | ADC average control:<br>0b = Single value<br>1b = Running average |
| 2 | ADC_AVG_INIT | R/W | 0x0 | Reset by:<br>REG_RESET | ADC average initial value control:<br>0b = Start average using existing register value<br>1b = Start average using new ADC conversion |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.28 REG0x2C_ADC_Channel_Control Register (Address = 0x2C) [Reset = 0x02]

REG0x2C_ADC_Channel_Control is shown in Figure 7-43 and described in Table 7-36.

Return to the Summary Table.

**Figure 7-43. REG0x2C_ADC_Channel_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

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**Figure 7-43. REG0x2C_ADC_Channel_Control Register (continued)**

| IAC_ADC_DIS | IBAT_ADC_DIS | VAC_ADC_DIS | VBAT_ADC_DIS | VSYS_ADC_DIS | TS_ADC_DIS | VFB_ADC_DIS | RESERVED |
|---|---|---|---|---|---|---|---|
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x1 | R-0x0 |

**Table 7-36. REG0x2C_ADC_Channel_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | IAC_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | IAC ADC control<br>0b = Enable<br>1b = Disable |
| 6 | IBAT_ADC_DIS | R/W | 0x0 | Recommend to disable IBAT ADC channel when EN_IBAT_LOAD bit is 1<br>Reset by:<br>REG_RESET | IBAT ADC control<br>0b = Enable<br>1b = Disable |
| 5 | VAC_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VAC ADC control<br>0b = Enable<br>1b = Disable |
| 4 | VBAT_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VBAT ADC control<br>0b = Enable<br>1b = Disable |
| 3 | VSYS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VSYS ADC control<br>0b = Enable<br>1b = Disable |
| 2 | TS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | TS ADC control<br>0b = Enable<br>1b = Disable |
| 1 | VFB_ADC_DIS | R/W | 0x1 | Reset by:<br>REG_RESET | VFB ADC control<br>Recommend to disable this channel when charging is enabled<br>0b = Enable<br>1b = Disable |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 7.5.29 REG0x2D_IAC_ADC Register (Address = 0x2D) [Reset = 0x0000]

REG0x2D_IAC_ADC is shown in Figure 7-44 and described in Table 7-37.

Return to the Summary Table.

I2C REG0x2E=[15:8], I2C REG0x2D=[7:0]

**Figure 7-44. REG0x2D_IAC_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IAC_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IAC_ADC | | | | | | | |
| R-0x0 | | | | | | | |


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**Table 7-37. REG0x2D_IAC_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | IAC_ADC | R | 0x0 | | IAC ADC reading with 2mΩ RAC_SNS:<br>Reported as 2s complement<br><br>POR: 0mA (0h)<br>Format: 2s Complement<br>Range: -50000mA-50000mA (9E58h-61A8h)<br>Clamped Low<br>Clamped High<br>Bit Step: 2mA |

### 7.5.30 REG0x2F_IBAT_ADC Register (Address = 0x2F) [Reset = 0x0000]

REG0x2F_IBAT_ADC is shown in Figure 7-45 and described in Table 7-38.

Return to the Summary Table.

I2C REG0x30=[15:8], I2C REG0x2F=[7:0]

**Figure 7-45. REG0x2F_IBAT_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IBAT_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBAT_ADC | | | | | | | |
| R-0x0 | | | | | | | |

**Table 7-38. REG0x2F_IBAT_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | IBAT_ADC | R | 0x0 | | IBAT ADC reading with 2.5mΩ RBAT_SNS:<br>Reported as 2s complement<br><br>POR: 0mA (0h)<br>Format: 2s Complement<br>Range: -40000mA-40000mA (D8F0h-2710h)<br>Clamped Low<br>Clamped High<br>Bit Step: 4mA |

### 7.5.31 REG0x31_VAC_ADC Register (Address = 0x31) [Reset = 0x0000]

REG0x31_VAC_ADC is shown in Figure 7-46 and described in Table 7-39.

Return to the Summary Table.

I2C REG0x32=[15:8], I2C REG0x31=[7:0]

**Figure 7-46. REG0x31_VAC_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VAC_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VAC_ADC | | | | | | | |
| R-0x0 | | | | | | | |

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**Table 7-39. REG0x31_VAC_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | VAC_ADC | R | 0x0 | | VAC ADC reading:<br>Reported as unsigned integer<br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-65534mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 2mV |

### 7.5.32 REG0x33_VBAT_ADC Register (Address = 0x33) [Reset = 0x0000]

REG0x33_VBAT_ADC is shown in Figure 7-47 and described in Table 7-40.

Return to the Summary Table.

I2C REG0x34=[15:8], I2C REG0x33=[7:0]

**Figure 7-47. REG0x33_VBAT_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VBAT_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBAT_ADC | | | | | | | |
| R-0x0 | | | | | | | |

**Table 7-40. REG0x33_VBAT_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | VBAT_ADC | R | 0x0 | | VBAT ADC reading:<br>Reported as unsigned integer<br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-65534mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 2mV |

### 7.5.33 REG0x35_VSYS_ADC Register (Address = 0x35) [Reset = 0x0000]

REG0x35_VSYS_ADC is shown in Figure 7-48 and described in Table 7-41.

Return to the Summary Table.

I2C REG0x36=[15:8], I2C REG0x35=[7:0]

**Figure 7-48. REG0x35_VSYS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VSYS_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYS_ADC | | | | | | | |
| R-0x0 | | | | | | | |


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**Table 7-41. REG0x35_VSYS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | VSYS_ADC | R | 0x0 | | VSYS ADC reading:<br>Reported as unsigned integer<br><br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-65534mV (0h-7FFFh)<br>Clamped Low<br>Bit Step: 2mV |

### 7.5.34 REG0x37_TS_ADC Register (Address = 0x37) [Reset = 0x0000]

REG0x37_TS_ADC is shown in Figure 7-49 and described in Table 7-42.

Return to the Summary Table.

I2C REG0x38=[15:8], I2C REG0x37=[7:0]

**Figure 7-49. REG0x37_TS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TS_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TS_ADC | | | | | | | |
| R-0x0 | | | | | | | |

**Table 7-42. REG0x37_TS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | TS_ADC | R | 0x0 | | TS ADC reading as percentage of REGN:<br>Reported as unsigned integer<br><br>POR: 0%(0h)<br>Format: 2s Complement<br>Range: 0% - 99.90234375% (0h-3FFh)<br>Clamped Low<br>Clamped High<br>Bit Step: 0.09765625% |

### 7.5.35 REG0x39_VFB_ADC Register (Address = 0x39) [Reset = 0x0000]

REG0x39_VFB_ADC is shown in Figure 7-50 and described in Table 7-43.

Return to the Summary Table.

I2C REG0x3A=[15:8], I2C REG0x39=[7:0]

**Figure 7-50. REG0x39_VFB_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VFB_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VFB_ADC | | | | | | | |
| R-0x0 | | | | | | | |

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**Table 7-43. REG0x39_VFB_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:0 | VFB_ADC | R | 0x0 | | VFB ADC reading:<br><br>POR: 0mV (0h)<br>Format: 2s Complement<br>Range: 0mV-2047mV (0h-7FFh)<br>Clamped Low<br>Clamped High<br>Bit Step: 1mV |

### 7.5.36 REG0x3B_Gate_Driver_Strength_Control Register (Address = 0x3B) [Reset = 0x00]

REG0x3B_Gate_Driver_Strength_Control is shown in Figure 7-51 and described in Table 7-44.

Return to the Summary Table.

**Figure 7-51. REG0x3B_Gate_Driver_Strength_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BOOST_HS_DRV | | BUCK_HS_DRV | | BOOST_LS_DRV | | BUCK_LS_DRV | |
| R/W-0x0 | | R/W-0x0 | | R/W-0x0 | | R/W-0x0 | |

**Table 7-44. REG0x3B_Gate_Driver_Strength_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | BOOST_HS_DRV | R/W | 0x0 | Reset by:<br>REG_RESET | Boost High Side FET Gate Driver Strength:<br><br>00b = Fastest<br>01b = Faster<br>10b = Slower<br>11b = Slowest |
| 5:4 | BUCK_HS_DRV | R/W | 0x0 | Reset by:<br>REG_RESET | Buck High Side FET Gate Driver Strength:<br><br>00b = Fastest<br>01b = Faster<br>10b = Slower<br>11b = Slowest |
| 3:2 | BOOST_LS_DRV | R/W | 0x0 | Reset by:<br>REG_RESET | Boost Low Side FET Gate Driver Strength:<br><br>00b = Fastest<br>01b = Faster<br>10b = Slower<br>11b = Slowest |
| 1:0 | BUCK_LS_DRV | R/W | 0x0 | Reset by:<br>REG_RESET | Buck Low Side FET Gate Driver Strength:<br><br>00b = Fastest<br>01b = Faster<br>10b = Slower<br>11b = Slowest |

### 7.5.37 REG0x3C_Gate_Driver_Dead_Time_Control Register (Address = 0x3C) [Reset = 0x00]

REG0x3C_Gate_Driver_Dead_Time_Control is shown in Figure 7-52 and described in Table 7-45.

Return to the Summary Table.

**Figure 7-52. REG0x3C_Gate_Driver_Dead_Time_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | BOOST_DEAD_TIME | | BUCK_DEAD_TIME | |
| R-0x0 | | | | R/W-0x0 | | R/W-0x0 | |


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**Table 7-45. REG0x3C_Gate_Driver_Dead_Time_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:4 | RESERVED | R | 0x0 | | Reserved |
| 3:2 | BOOST_DEAD_TIME | R/W | 0x0 | Reset by: REG_RESET | Boost Side FETs Dead Time Control:<br>00b = 45ns<br>01b = 75ns<br>10b = 105ns<br>11b = 135ns |
| 1:0 | BUCK_DEAD_TIME | R/W | 0x0 | Reset by: REG_RESET | Buck Side FETs Dead Time Control:<br>00b = 45ns<br>01b = 75ns<br>10b = 105ns<br>11b = 135ns |

### 7.5.38 REG0x3D_Part_Information Register (Address = 0x3D) [Reset = 0x32]

REG0x3D_Part_Information is shown in Figure 7-53 and described in Table 7-46.

Return to the Summary Table.

**Figure 7-53. REG0x3D_Part_Information Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | PART_NUM | | | | DEV_REV | |
| R-0x0 | | R-0x6 | | | | R-0x2 | |

**Table 7-46. REG0x3D_Part_Information Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | RESERVED | R | 0x0 | | Reserved |
| 5:3 | PART_NUM | R | 0x6 | | Part Number:<br>110 - BQ25853Q1 |
| 2:0 | DEV_REV | R | 0x2 | | |

### 7.5.39 REG0x62_Reverse_Mode_Battery_Discharge_Current Register (Address = 0x62) [Reset = 0x20]

REG0x62_Reverse_Mode_Battery_Discharge_Current is shown in Figure 7-54 and described in Table 7-47.

Return to the Summary Table.

**Figure 7-54. REG0x62_Reverse_Mode_Battery_Discharge_Current Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IBAT_REV | | RBAT_SNS | RESERVED | | | EN_CONV_FAST_TRANSIENT | RESERVED |
| R/W-0x0 | | R/W-0x1 | R-0x0 | | | R/W-0x0 | R-0x0 |

**Table 7-47. REG0x62_Reverse_Mode_Battery_Discharge_Current Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | IBAT_REV | R/W | 0x0 | Reset by: REG_RESET | Reverse mode battery discharge current limit:<br>00b = 20A<br>01b = 15A<br>10b = 10A<br>11b = 5A |
| 5 | RBAT_SNS | R/W | 0x1 | Reset by: REG_RESET | IBAT sense resistor value<br>0b = 5mOhm<br>1b = 2.5mOhm |
| 4:2 | RESERVED | R | 0x0 | | Reserved |

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**Table 7-47. REG0x62_Reverse_Mode_Battery_Discharge_Current Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1 | EN_CONV_FAST_TRANSIENT | R/W | 0x0 | Reset by:<br>REG_RESET | 0b = Disable<br>1b = Enable |
| 0 | RESERVED | R | 0x0 | | Reserved |


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The BQ25853Q1 battery charger is designed for high current charging and can charge multi-chemistry battery packs consisting of single cells or multiple cells in series up-to 70V. The BQ25853Q1EVM evaluation module is a complete module for evaluating the device performance. The application curves are taken using the BQ25853Q1EVM.

## 8.2 Typical Applications

### *8.2.1 Typical Application*

The device can be configured as a bidirectional buck-boost charge controller. The bi-directionality allows the battery to be charged as well as provide power to the input in reverse mode. Figure 8-1 shows a typical schematic when using the device as a bi-directional battery charger with an input voltage of 48V and an output voltage of 12V. The charging parameters and direction of power flow can be programmed using the $I^2C$ registers.

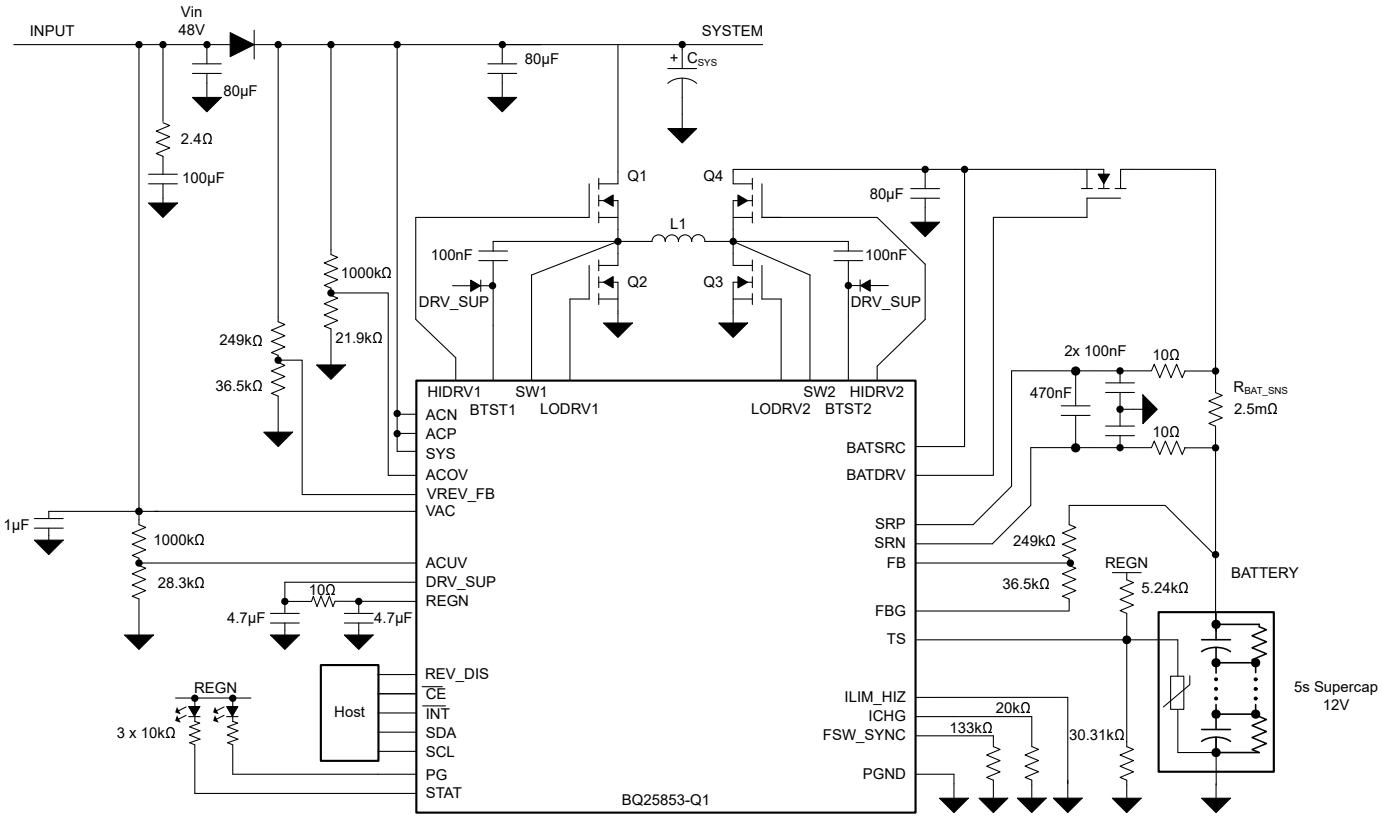


**Figure 8-1. BQ25853Q1: Bidirectional Charging From a 48V Input to Charge a 5s Supercapacitor**

**Table 8-1. Recommended Part Numbers**

| COMPONENT | VALUE | RECOMMENDED PART NUMBER |
|---|---|---|
| Q1, Q2, Q3, Q4 | 80V, 2.8mΩ | SiR680LDP |
| L1 | 10µH, 23mΩ | SRP1050WA-100M |

#### 8.2.1.1 Design Requirements

For this design example, use the parameters shown in the table below.

**Table 8-2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage operating range ($V_{AC}$) | 48V |
| Input current limit ($I_{AC}$) | 5A |
| Output current limit ($I_{OUT}$) | 5A |
| Battery charge voltage ($V_{BAT_REG}$) | 12V |
| Reverse mode voltage ($V_{SYS_REG}$) | 12V |
| Switching frequency | 250kHz |

#### 8.2.1.2 Detailed Design Procedure

##### *8.2.1.2.1 ACUV / ACOV Input Voltage Operating Window Programming*

The input voltage operating window is programmed by an ACUV / ACOV window with a resistor divider from VAC to GND. The top resistor, RAC1 and RAC3 is typically selected as 1,000kΩ to minimize the input voltage leakage current. Assuming the desired trip-points for under-voltage and over-voltage protection are labeled $V_{VACUVP}$ and $V_{VACOVP}$, the resistor divider required can be calculated as follows. The internal reference for the over-voltage threshold (VREF_ACOV) is 1.2V. The internal reference for the under-voltage threshold (VREF_ACUV) is 1.1V.

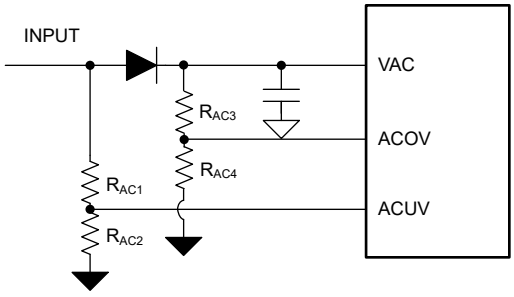


**Figure 8-2. ACUV and ACOV Resistor Divider**

$$V_{VACUVP} = \frac{1.1V(1{,}000k\Omega + R_{AC2})}{R_{AC2}} \quad (8)$$

$$V_{VACOVP} = \frac{1.2V(1{,}000k\Omega + R_{AC4})}{R_{AC4}} \quad (9)$$

For the default device operating window of 4.2V to 60V, the ACUV can be pulled up directly to VAC, while the ACOV can be pulled directly to GND.

##### *8.2.1.2.2 Charge Voltage Selection*

The battery regulation voltage is programmed using a resistor divider to the FB pin. The default internal voltage reference is 1.536V, and can be changed via the VFB_REG register bits. The top of the resistor divider is selected to be 249kΩ.

$R_{TOP}$ = 249kΩ


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The bottom resistor can be calculated as:

$$R_{BOT} = R_{TOP} \times \frac{V_{FB}}{V_{BATREG} - V_{FB}} - R_{FBG} \quad (10)$$

where

- $V_{FB}$ is the target feedback voltage programmed through I²C (default 1.536V),
- $V_{BATREG}$ is the desired battery regulation target (12V in this example)
- $R_{FBG}$ is the internal FBG pull-down resistor (33Ω)

$R_{FB_BOT}$ = 36.6kΩ.

Choosing the nearest 0.1% resistor value, gives $R_{FB_BOT}$ = 36.5 kΩ, for a nominal charge voltage of 12 V. Further fine-tuning of the regulation voltage can be achieved by changing the internal feedback reference.

Use 0.1% accurate resistors to maximize the charge voltage accuracy.

#### *8.2.1.2.3 Reverse Mode System Voltage Selection*

The reverse mode system regulation voltage is programmed using a resistor divider to the VREV_FB pin. The default internal voltage reference is 1.536V, and can be changed via the VFB_REG register bits. The top of the resistor divider is selected to be 249kΩ.

$R_{TOP}$ = 249kΩ

The bottom resistor can be calculated as:

$$R_{BOT} = R_{TOP} \times \frac{V_{VREV_FB}}{V_{SYSREG} - V_{VREV_FB}} \quad (11)$$

where

- $V_{FB}$ is the target feedback voltage programmed through I²C (default 1.536V),
- $V_{SYS}$ is the desired battery regulation target (12V in this example)

$R_{VREV_FB_BOT}$ = 36.55kΩ.

Choosing the nearest 0.1% resistor value, gives $R_{FB_BOT}$ = 36.5 kΩ, for a nominal charge voltage of 12 V. Further fine-tuning of the regulation voltage can be achieved by changing the internal feedback reference.

Use 0.1% accurate resistors to maximize the charge voltage accuracy.

#### *8.2.1.2.4 Switching Frequency Selection*

The switching frequency is set by a resistor connected from the FSW_SYNC pin to PGND. The RFSW resistor required to set the desired frequency is calculated using Equation 3 or Table 7-3. A 0.1% standard resistor of 133kΩ is selected to set $f_{SW}$ = 250kHz.

#### *8.2.1.2.5 Inductor Selection*

Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current must be higher than the inductor current ($I_L$) plus half the ripple current ($I_{RIPPLE}$):

$$I_{SAT} \geq I_L + \frac{1}{2} I_{RIPPLE} \quad (12)$$

The inductor ripple current in buck operation depends on input voltage ($V_{AC}$), duty cycle ($D_{BUCK}$ = $V_{BAT}/V_{AC}$), switching frequency ($f_{SW}$) and inductance (L):

$$I_{RIPPLE_BUCK} = \frac{V_{AC} \times D_{BUCK} \times (1 - D_{BUCK})}{f_{SW} \times L} \quad (13)$$

During boost operation, the duty cycle is: $D_{BOOST}$ = 1 – ($V_{AC}/V_{BAT}$). The inductor ripple current is:

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$$I_{RIPPLE_BOOST} = \frac{V_{AC} \times D_{BOOST}}{f_{SW} \times L} \quad (14)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Ripple calculations must be analyzed for both forward and reverse operating modes if applicable.

Typically inductor ripple is designed in the range of (20 – 40%) maximum inductor current (in either forward or reverse mode) as a trade-off between inductor size and efficiency for a practical design. For system stability, the inductor's time constant should be between 0.05µH/mΩ and 1.26µH/mΩ.

#### *8.2.1.2.6 Input (VAC / SYS) Capacitor*

Input capacitor must have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the output when duty cycle is 0.5 in forward buck mode, or reverse boost mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 15:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (15)$$

A combination of ceramic and bulk capacitors must be used to provide a short path for high di/dt current and to reduce the voltage ripple. Ceramic capacitors must be placed close to the switching half-bridge. Given total bulk input capacitance, distributing equally on either side of $R_{AC_SNS}$ is recommended. The complete schematic is a good starting point for input capacitor for typical applications.

#### *8.2.1.2.7 Output (VBAT) Capacitor*

In forward boost mode or reverse buck mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by where the minimum VAC corresponds to the maximum capacitor current.

$$I_{CBAT} = I_{BAT}\sqrt{\frac{V_{BAT}}{V_{AC}} - 1} \quad (16)$$

A 5mΩ output capacitor ESR causes an output voltage ripple of 74mV as given by:

$$\Delta V_{RIPPLE(ESR)} = I_{BAT} \times \frac{V_{BAT}}{V_{AC,min}} \times ESR \quad (17)$$

A 140µF output capacitor causes a capacitive ripple voltage of 66mV as given by:

$$\Delta V_{RIPPLE(CBAT)} = I_{BAT} \times \frac{\left(1 - \frac{V_{AC,min}}{V_{BAT}}\right)}{C_{BAT} \times f_{SW}} \quad (18)$$

A combination of ceramic and bulk capacitors must be used to provide low ESR and high ripple current capacity. Ceramic capacitors must be placed close to the switching half-bridge. Given total bulk output capacitance, distributing equally on either side of $R_{BAT_SNS}$ is recommended. The complete schematic is a good starting point for $C_{BAT}$ for typical applications.

#### *8.2.1.2.8 Sense Resistor ($R_{AC_SNS}$ and $R_{BAT_SNS}$) and Current Programming*

The battery current sense resistor between SRP and SRN is fixed at 2.5mΩ; using a different value is not recommended. The input current sense resistor between ACP and ACN is typically 2mΩ, but can be increased to achieve better accuracy at lower sensed currents. If input current limit function is not desired, ACP and ACN can be shorted together. For both of these sense resistors, a filter network is recommended as shown in the Typical Application.

For both the input current and the output current, the limits can be programmed using the $I^2C$ interface or an external programming resistor on ILIM_HIZ and ICHG pins, respectively.


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| PARAMETER | FORMULA | VALUE |
|---|---|---|
| Input Current Hardware Limit | Unused | Pull ILIM_HIZ pin to GND |
| Input Current Software Limit | Unused | REG06 = 0x0640 (50A with 2mΩ $R_{AC_SNS}$) |
| Charge Current Hardware Limit | $R_{ICHG} = K_{ICHG}$ / 5A | 20kΩ for 5A with 2.5mΩ $R_{BAT_SNS}$ |
| Output Current Software Limit | Unused | REG02 = 0x0640 (40A) |

The default input sense resistor ($R_{AC_SNS}$) is 2mΩ, and the register allows for a range of up to 50A input current limit. If lower currents are desired, use a higher resistor, such as 5mΩ. In this case, the IAC_DPM register value must be multiplied by a factor of 2/5 to program the correct current. For example, if a 5mΩ $R_{AC_SNS}$ is used, and the register is programmed to a value of 0x60, the true maximum current across the $R_{AC_SNS}$ is: 12A × 2/5 = 4.8A. Similarly, the $K_{ILIM}$ parameter used to set the ILIM_HIZ pulldown resistor must be scaled by 2/5. For example, with a 5mΩ $R_{AC_SNS}$ resistor, a 6A current limit is achieved as: $R_{ILIM} = K_{ILIM} \times (2/5) / 6A = 3.3k\Omega$.

#### *8.2.1.2.9 Power MOSFETs Selection*

Four external N-channel MOSFETs are used for a synchronous switching buck-boost battery charger. The gate drivers are integrated into the IC with 5V of gate drive voltage. An external gate drive voltage can be provided directly into the DRV_SUP pin for increased efficiency.

Figure-of-merit (FOM) is typically used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of the MOSFET on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, $Q_{GD}$. For the bottom side MOSFET, FOM is defined as the product of the on-resistance of the MOSFET, $R_{DS(ON)}$, and the total gate charge, $Q_G$.

$$FOM_{top} = R_{DS(on)} \cdot Q_{GD};\ FOM_{bottom} = R_{DS(on)} \cdot Q_G \quad (19)$$

The lower the FOM value, the lower the total power loss. Typically lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. Taking buck mode operation as an example the power loss is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current ($I_{CHG}$), on-resistance of the MOSFET ($R_{DS(ON)_top}$), input voltage ($V_{IN}$), switching frequency ($f_S$), turn-on time ($t_{on}$) and turn-off time ($t_{off}$):

$$P_{top} = P_{con_top} + P_{sw_top} \quad (20)$$

$$P_{con_top} = D \cdot I_{L_RMS}^2 \cdot R_{DS(on)_top}; \quad (21)$$

$$I_{L_RMS}^2 = I_{L_DC}^2 + I_{ripple}^2/12 \quad (22)$$

- $I_{L_DC}$ is the average inductor DC current;
- $I_{ripple}$ is the inductor current ripple peak-to-peak value;

$$P_{sw_top} = P_{IV_top} + P_{Qoss_top} + P_{Gate_top}; \quad (23)$$

The first item $P_{con_top}$ represents the conduction loss which is straight forward. The second term $P_{sw_top}$ represents the multiple switching loss items in top MOSFET including voltage and current overlap losses ($P_{IV_top}$), MOSFET parasitic output capacitance loss ($P_{Qoss_top}$) and gate drive loss ($P_{Gate_top}$). To calculate voltage and current overlap losses ($P_{IV_top}$):

$$P_{IV_top} = 0.5x\ V_{IN} \cdot I_{valley} \cdot t_{on} \cdot f_S + 0.5x\ V_{IN} \cdot I_{peak} \cdot t_{off} \cdot f_S \quad (24)$$

$$I_{valley} = I_{L_DC} - 0.5 \cdot I_{ripple} \text{ (inductor current valley value)}; \quad (25)$$

$$I_{peak} = I_{L_DC} + 0.5 \cdot I_{ripple} \text{ (inductor current peak value)}; \quad (26)$$

- $t_{on}$ is the MOSFET turn-on time that $V_{DS}$ falling time from $V_{IN}$ to almost zero (MOSFET turn on conduction voltage);
- $t_{off}$ is the MOSFET turn-off time that $I_{DS}$ falling time from $I_{peak}$ to zero;

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The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \tag{27}$$

where $Q_{sw}$ is the switching charge, $I_{on}$ is the turn-on gate driving current, and $I_{off}$ is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, the value can be estimated by gate-to-drain charge ($Q_{GD}$) and gate-to-source charge ($Q_{GS}$):

$$Q_{sw} = Q_{GD} + Q_{GS} \tag{28}$$

Gate driving current can be estimated by REGN voltage ($V_{REGN}$), MOSFET plateau voltage ($V_{plt}$), total turn-on gate resistance ($R_{on}$), and turn-off gate resistance ($R_{off}$) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \tag{29}$$

To calculate top MOSFET parasitic output capacitance loss ($P_{Qoss_top}$):

$$P_{Qoss_top} = 0.5 \cdot V_{IN} \cdot Q_{oss} \cdot f_S \tag{30}$$

- $Q_{oss}$ is the MOSFET parasitic output charge which can be found in MOSFET datasheet. Limit the total switch node capacitance $C_{SW}$ (nF) < 160/VIN; for example, for a application, keep the total $C_{SW}$ < 2.67nF

To calculate top MOSFET gate drive loss ($P_{Gate_top}$):

$$P_{Gate_top} = V_{IN} \cdot Q_{Gate_top} \cdot f_S \tag{31}$$

- $Q_{Gate_top}$ is the top MOSFET gate charge which can be found in MOSFET datasheet;
- Note here $V_{IN}$ is used instead of real gate drive voltage because the gate drive is generated based on LDO from $V_{IN}$, the total gate drive related loss are all considered when $V_{IN}$ is used for gate drive loss calculation.
- Alternatively, gate drive voltage can be supplied directly by external high efficiency supply into the DRV_SUP pin. In this case, the power loss to drive the gates becomes: $P_{Gate_top} = V_{DRV_SUP} \cdot Q_{Gate_top} \cdot f_S$

The bottom-side MOSFET loss also includes conduction loss and switching loss:

$$P_{bottom} = P_{con_bottom} + P_{sw_bottom} \tag{32}$$

$$P_{con_bottom} = (1 - D) \cdot I_{L_RMS}^2 \cdot R_{DS(on)_bottom}; \tag{33}$$

$$P_{sw_bottom} = P_{RR_bottom} + P_{Dead_bottom} + P_{Gate_bottom}; \tag{34}$$

The first item $P_{con_bottom}$ represents the conduction loss which is straight forward. The second term $P_{sw_bottom}$ represents the multiple switching loss items in bottom MOSFET including reverse recovery losses ($P_{RR_bottom}$), Dead time body diode conduction loss ($P_{Dead_bottom}$) and gate drive loss ($P_{Gate_bottom}$). The detail calculation can be found below:

$$P_{RR_bottom} = V_{IN} \cdot Q_{rr} \cdot f_S \tag{35}$$

- $Q_{rr}$ is the bottom MOSFET reverse recovery charge which can be found in MOSFET datasheet;

$$P_{Dead_bottom} = V_F \cdot I_{valley} \cdot f_S \cdot t_{dead_rise} + V_F \cdot I_{peak} \cdot f_S \cdot t_{dead_fall} \tag{36}$$

- $V_F$ is the body diode forward conduction voltage drop;
- $t_{dead_rise}$ is the SW rising edge deadtime between top and bottom MOSFETs which is around 40ns;
- $t_{dead_fall}$ is the SW falling edge deadtime between top and bottom MOSFETs which is around 30ns;


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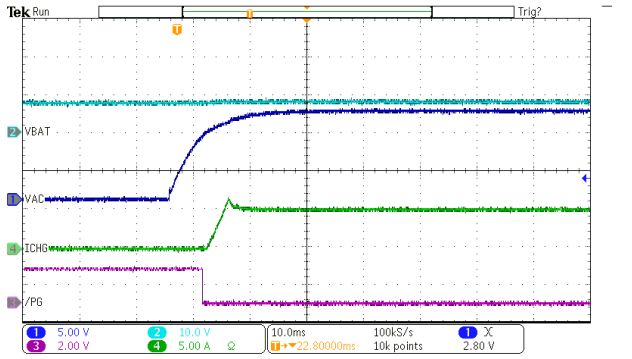
$P_{Gate_bottom}$ can follow the same method as top MOSFET gate drive loss calculation approach.

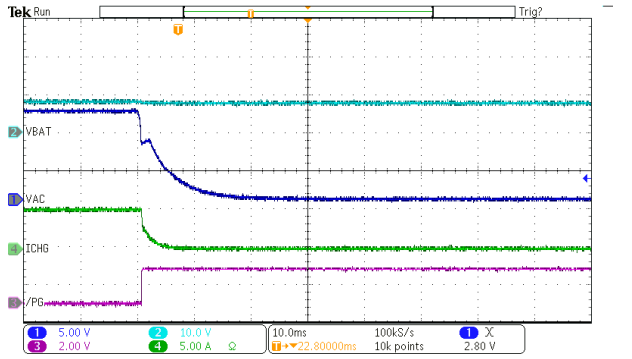
#### 8.2.1.3 Application Curves

$C_{VAC}$ = 160µF, $C_{OUT}$ = 160µF



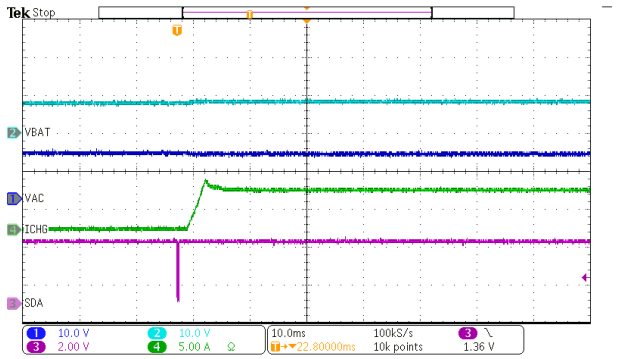

VAC = 0V → 12V VBAT = 8V ICHG = 5A

**Figure 8-3. VAC Plug-In Power Up With 5A ICHG**



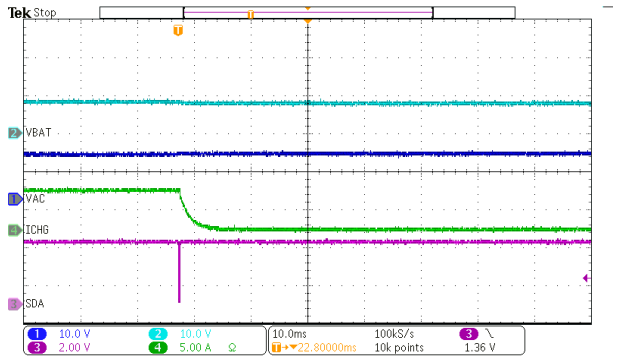

VAC = 12V → 0V VBAT = 8V ICHG = 5A

**Figure 8-4. VAC Unplug Power Down With 5A ICHG**



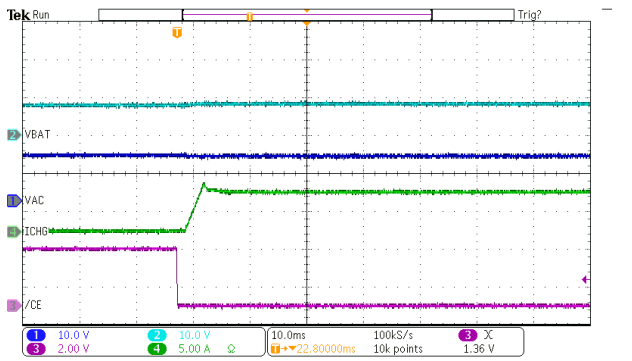

VAC = 12V VBAT = 8V ICHG = 5A

**Figure 8-5. Charge Enable Using I²C With 5A ICHG**



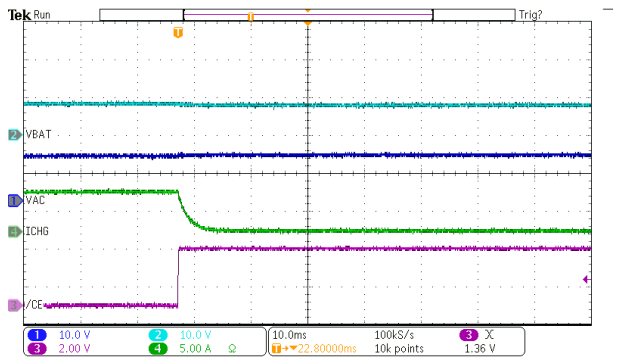

VAC = 12V VBAT = 8V ICHG = 5A

**Figure 8-6. Charge Disable Via I²C With 5A ICHG**




VAC = 12V VBAT = 8V ICHG = 5A

**Figure 8-7. Charge Enable Using $\overline{CE}$ Pin With 5A ICHG**




VAC = 12V VBAT = 8V ICHG = 5A

**Figure 8-8. Charge Disable Using $\overline{CE}$ Pin With 5A ICHG**

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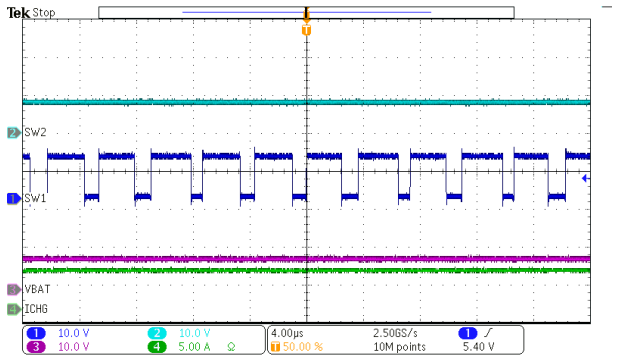
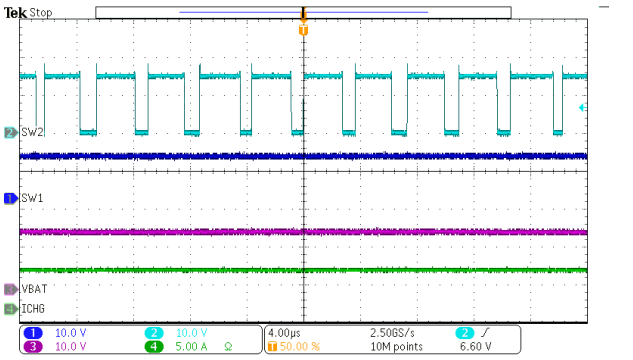


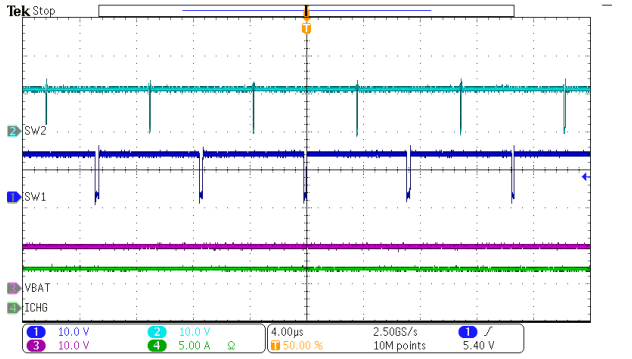

VAC = 12V VBAT = 8V ICHG = 5A

**Figure 8-9. Buck Switching Waveform**



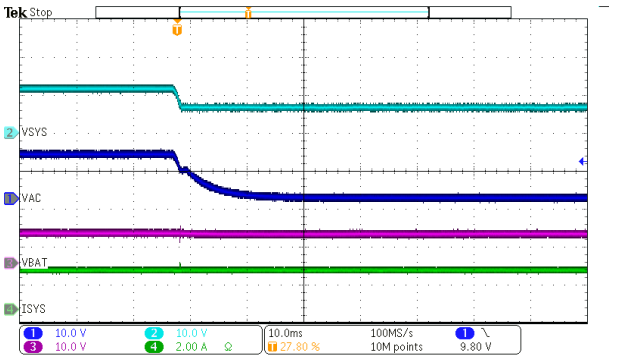

VAC = 12V VBAT = 15V ICHG = 5A

**Figure 8-10. Boost Switching Waveform**



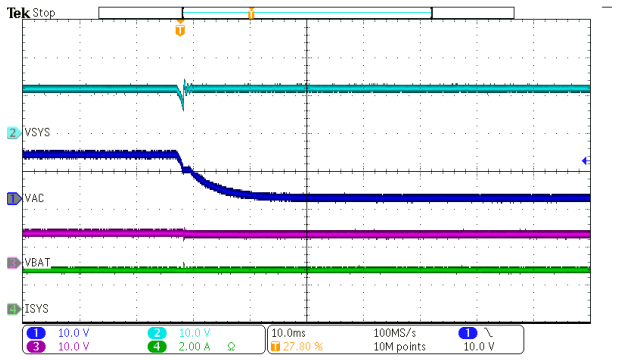

VAC = 12V VBAT = 11V ICHG = 5A

**Figure 8-11. Buck-Boost Switching Waveform**



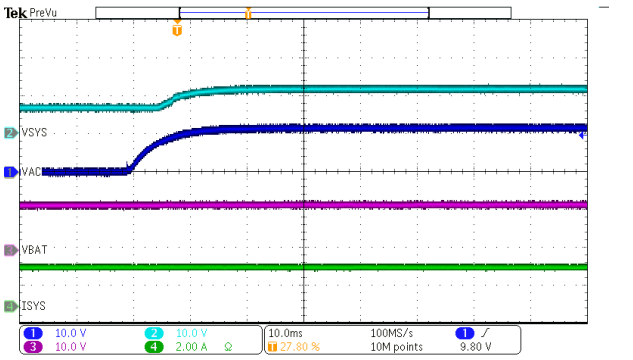

$V_{VACUVP}$ = 7.5V VBAT = 8V ISYS = 2A
VAC = 12V → 0V

**Figure 8-12. Autonomous Reverse Mode Entry With 7V VSYS_REG**




$V_{VACUVP}$ = 7.5V VBAT = 8V ISYS = 2A
VAC = 12V → 0V

**Figure 8-13. Autonomous Reverse Mode Entry With 12V VSYS_REG**




$V_{VACUVP}$ = 7.5V VBAT = 8V ISYS = 2A
VAC = 12V → 0V

**Figure 8-14. Autonomous Reverse Mode Exit With 7V VSYS_REG**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## 8.3 Power Supply Recommendations

The power supply for the device is any DC voltage source within the specified input range. The supply must also be capable of supplying sufficient current based on the programmed input current limit. The input supply must be bypassed with a combination of electrolytic and ceramic capacitors to avoid ringing due to the parasitic impedance of the connecting cables.

When device is operating in the reverse direction, the supply at the OUTPUT must follow the same recommendations as the input supply mentioned above.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

**Table 8-3. PCB Layout Guidelines**

| COMPONENTS | FUNCTION | IMPACT | GUIDELINES |
|---|---|---|---|
| Buck high side FET, Buck low side FET, input capacitors | Buck input loop | High frequency noise, ripple, efficiency | This path forms a high frequency switching loop due to the pulsating current at the input of the buck. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place input ceramic capacitors close to the switching FETs. |
| Boost low side FET, boost high side FET, output capacitors | Boost output loop | High frequency noise, ripple, efficiency | This path forms a high frequency switching loop due to the pulsating current at the output of the boost. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place output ceramic capacitors close to the switching FETs. |
| Sense resistors, switching FETs, inductor | Current path | Efficiency | The current path from input to output through the power stage and sense resistors need to have low impedance. Pay attention to via resistance if the vias are not on the same side. The number of vias can be estimated as 1A to 2A per via for a 10-mil via with 1oz. copper thickness. |
| Switching FETs, inductor | Power stage | Thermal, efficiency | The switching FETs and inductor are the components with highest power loss. Allow enough copper area for heat dissipation. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat. |
| DRV_SUP, BTST1, BTST2 capacitors | Switching FET gate drive | High frequency noise, parasitic ringing, gate drive integrity | The DRV_SUP capacitor is used to supply the power to drive the low side FETs. The BTST capacitors are used to drive the high side FETs. Place the capacitors as close as possible to the IC. |
| LODRV1, LODRV2 | Low side gate drive | High frequency noise, parasitic ringing, gate drive integrity | LODRV1 and LODRV2 supplies the gate drive current to turn on the low side FETs. The return of LODRV1 and LODRV2 is PGND. As current takes the path of least impedance, a ground plane close to the low side gate drive traces is recommended. Minimize gate drive length and aim for at least 20-mil gate drive trace width. |
| HIDRV1, HIDRV2, SW1 (pin trace), SW2 (pin trace) | High side gate drive | High frequency noise, parasitic ringing, gate drive integrity | HIDRV1 and HIDRV2 supplies the gate drive current to turn on the high side FETs. The return of HIDRV1 and HIDRV2 are SW1 and SW2, respectively. Route HIDRV1/SW1 and HIDRV2/SW2 pair next to each other to reduce gate drive parasitic inductance. Minimize gate drive length and aim for at least 20-mil gate drive trace width. |

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**Table 8-3. PCB Layout Guidelines (continued)**

| COMPONENTS | FUNCTION | IMPACT | GUIDELINES |
|---|---|---|---|
| Current limit resistors, FSW_SYNC resistor | IC programmable settings | Regulation accuracy, switching integrity | Pin voltage determines the settings for input current limit, output current limit and switching frequency. Ground noise on these can lead to inaccuracy. Minimize ground return from these resistors to the IC ground pin. |
| Input (ACP, ACN) and output (SRP, SRN) current sense | Current regulation | Regulation accuracy | Use Kelvin-sensing technique for input and output current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs, away from switching nodes. |
| Input (ACUV), and output (FB, VREV_FB) voltage sensing | Voltage sense and regulation | Regulation accuracy | ACUV divider sets internal input voltage regulation in forward mode ($V_{ACUV_DPM}$). FB divider sets battery voltage regulation in forward mode ($V_{FB_ACC}$). Route the top of the divider point to the target regulation location. VREV_FB sets the output voltage regulation in reverse mode ($V_{REVFB_ACC}$). Route directly to the target regulation location. Avoid routing close to high power switching nodes. |
| Bypass capacitors | Noise filter | Noise immunity | Place lowest value capacitors closest to the IC. |

### *8.4.2 Layout Example*

Based on the above layout guidelines, the buck-boost PCB layout example top view is shown below including all the key power components.

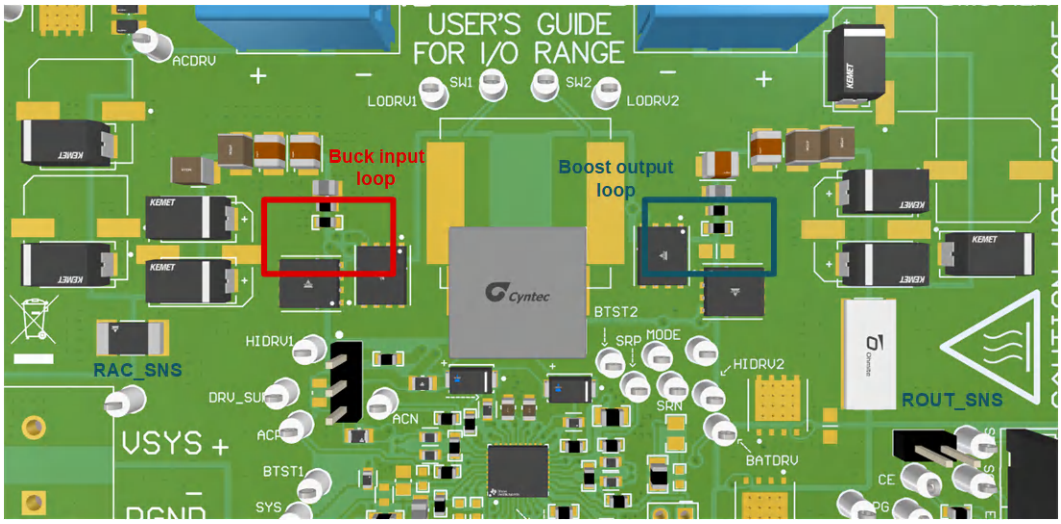


**Figure 8-15. PCB Layout Reference Example Top View**

For both input and output current sensing resistors, differential sensing and routing method are suggested and highlighted in figure below. Use wide trace for gate drive traces, minimum 20-mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad.


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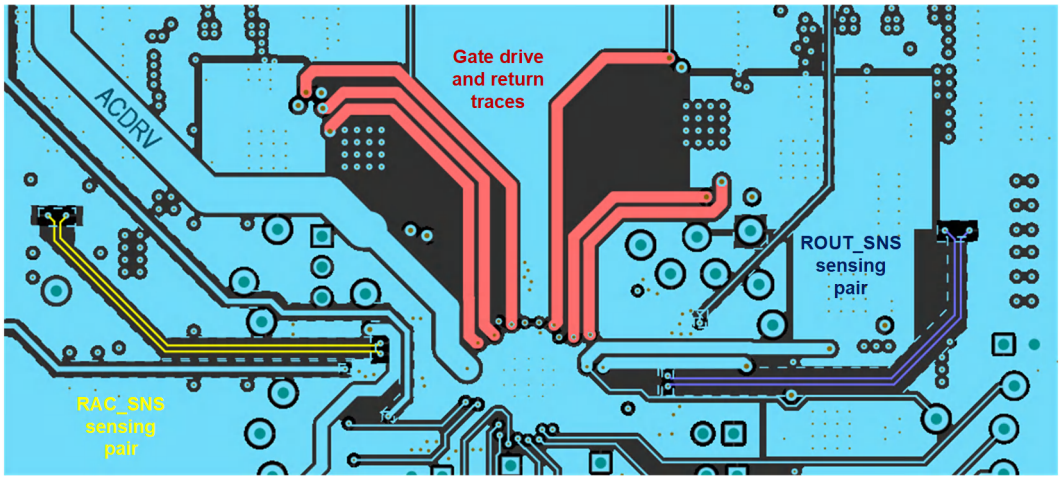


**Figure 8-16. PCB Layout Gate Drive and Current Sensing Signal Layer Routing**

# 9 Device and Documentation Support

## 9.1 Device Support

### *9.1.1 Third-Party Products Disclaimer*

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## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |


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## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (June 2026) to Revision B (November 2026)** **Page**

- Corrected the AEC-Q100 temperature grade to grade 0....1
- Updated BQ25853Q1 Registers section....1
- Corrected information in the Package Information table....1
- Corrected Pin Configuration Figure Title....4
- Added BATDRV, BATSRC, SYS pins' absolute maximum ratings....7
- Added BATDRV pin with respect to BATSRC pin's absolute maximum rating....7
- Added recommended VAC condition....7
- Added recommended VBAT condition....7
- Added recommended CVAC condition....7
- Added recommended RBAT_SNS condition....7
- Added recommended RICHG condition....7
- Added recommended RILIM_HIZ condition....7
- Added tTS_DGL....15
- Updated Device HIZ Mode section....22
- Corrected Reverse Mode Operation Conditions....29
- Update Integrated 16-Bit ADC for Monitoring section....30
- Updated Byte Format section....34
- Update Charge Voltage Selection section....64
- Updated Inductor Selection section....65
- Updated Layout Guidelines section....71

**Changes from Revision * (April 2026) to Revision A (June 2026)** **Page**

- Updated datasheet status from *Advanced Information* to *Production Data*. First public release of the datasheet....1
- Updated the *Features*, *Absolute Maximum Ratings* table, *Electrical Charateristics* table, *Typical Characteristics*, *Feature Description*, and *Application Curves* to the production data specifications....1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| BQ25853QWRRVRQ1 | Active | Production | VQFN (RRV) \| 36 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 853-Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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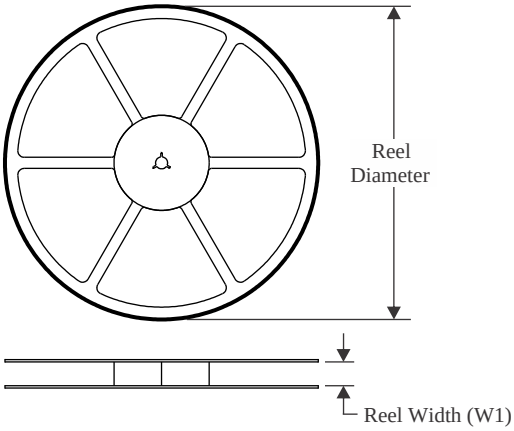
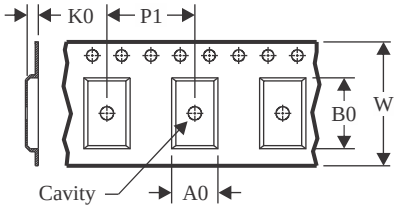
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

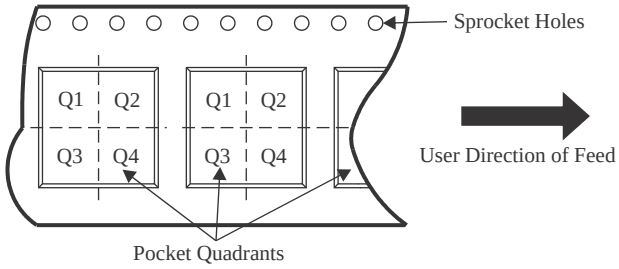



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

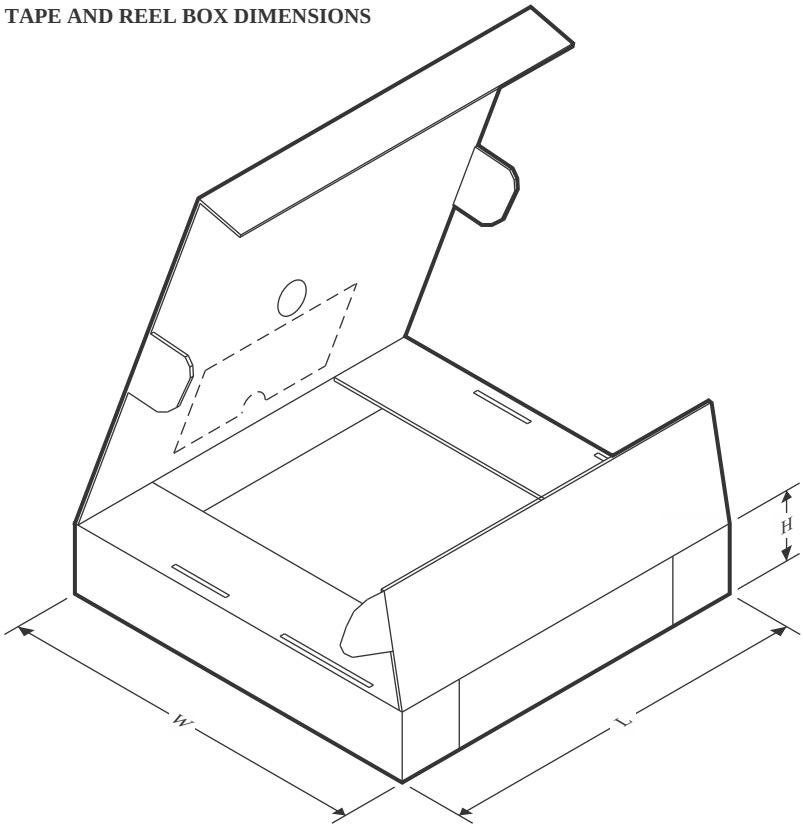
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25853QWRRVRQ1 | VQFN | RRV | 36 | 3000 | 330.0 | 12.4 | 5.3 | 6.3 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ25853QWRRVRQ1 | VQFN | RRV | 36 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

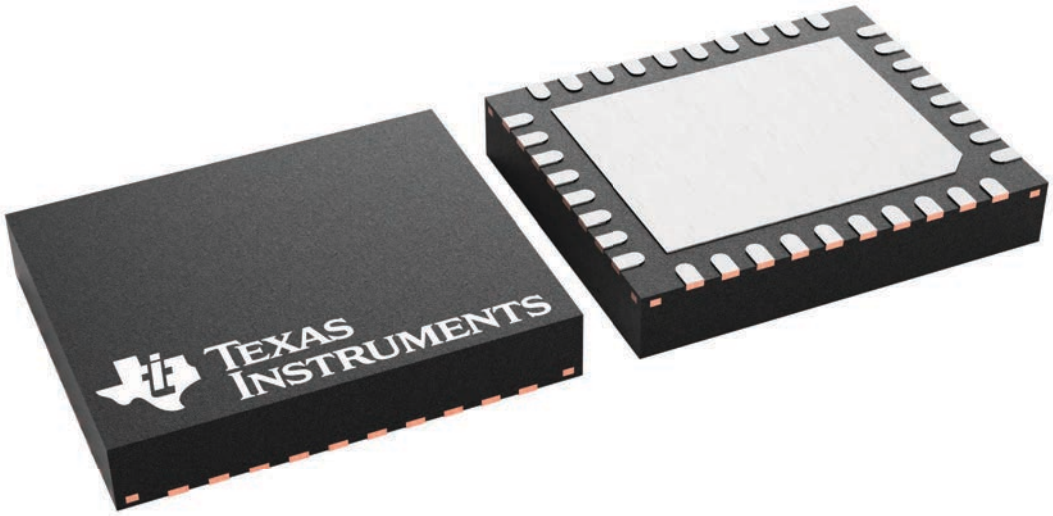
## RRV 36

## VQFN - 1 mm max height

**5 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4229484/A

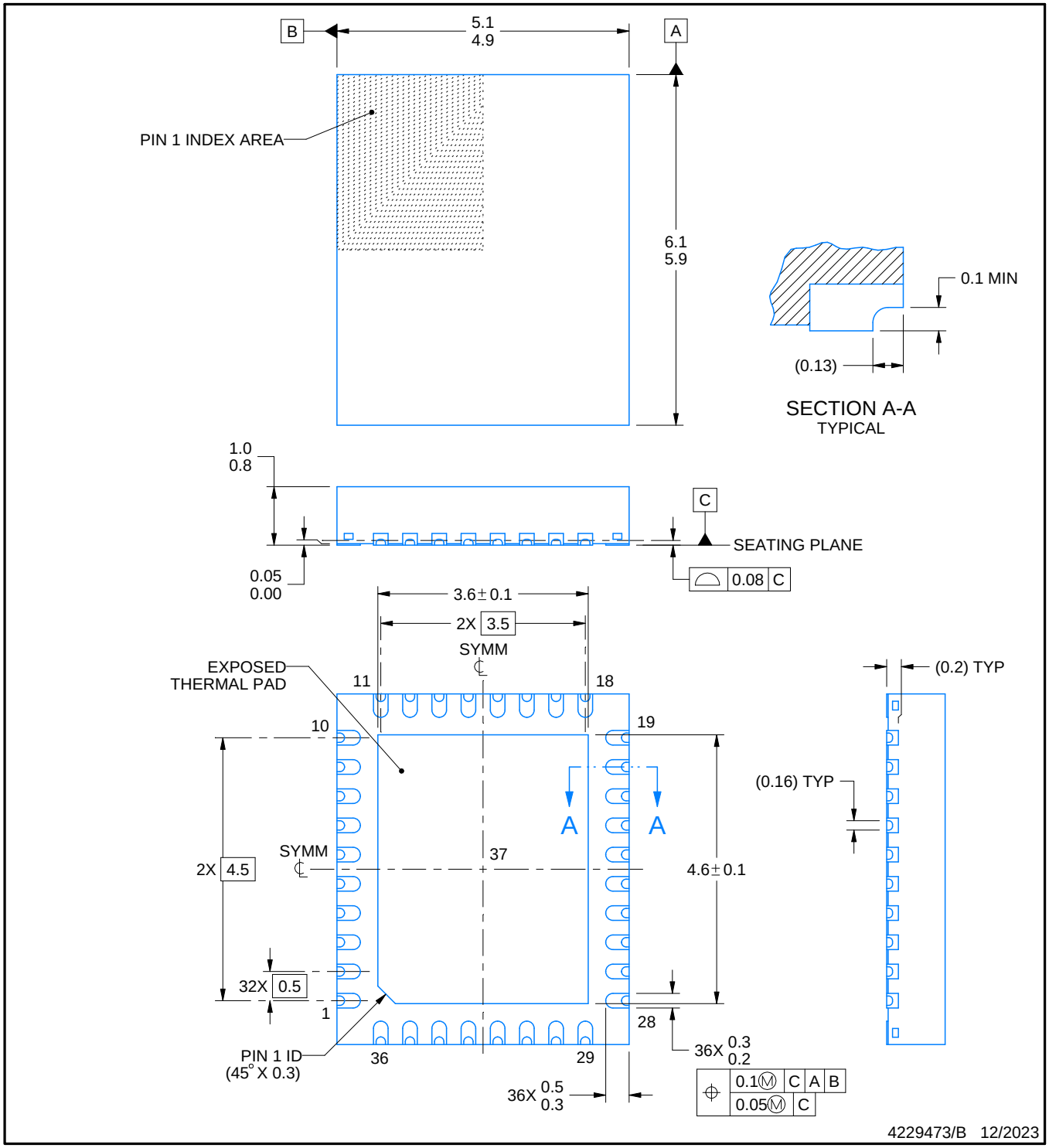
# RRV0036B



# PACKAGE OUTLINE

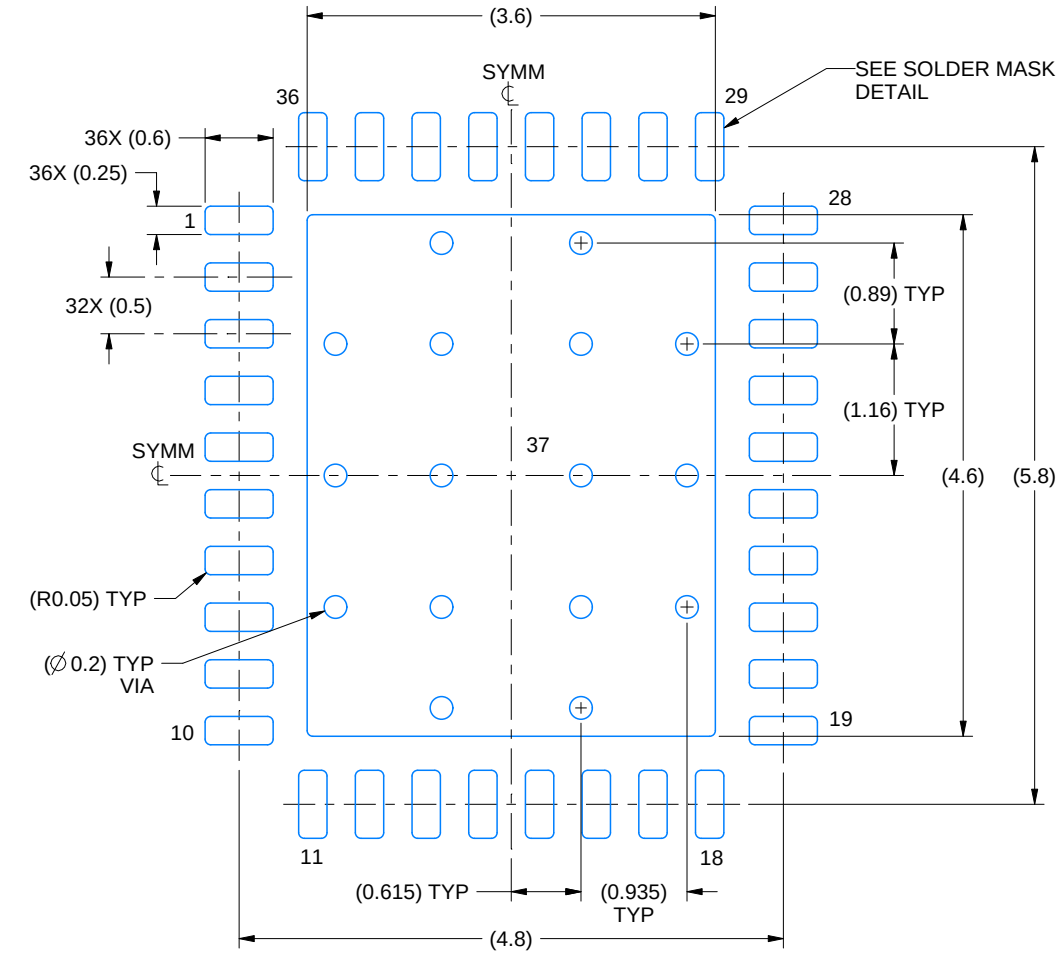
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

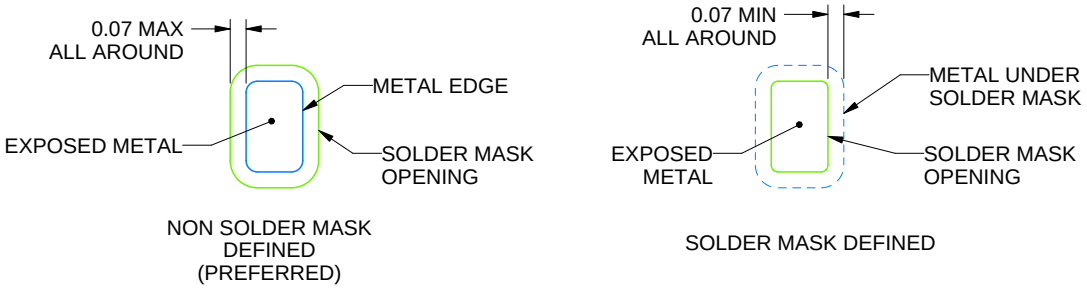



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

4229473/B 12/2023

NOTES: (continued)

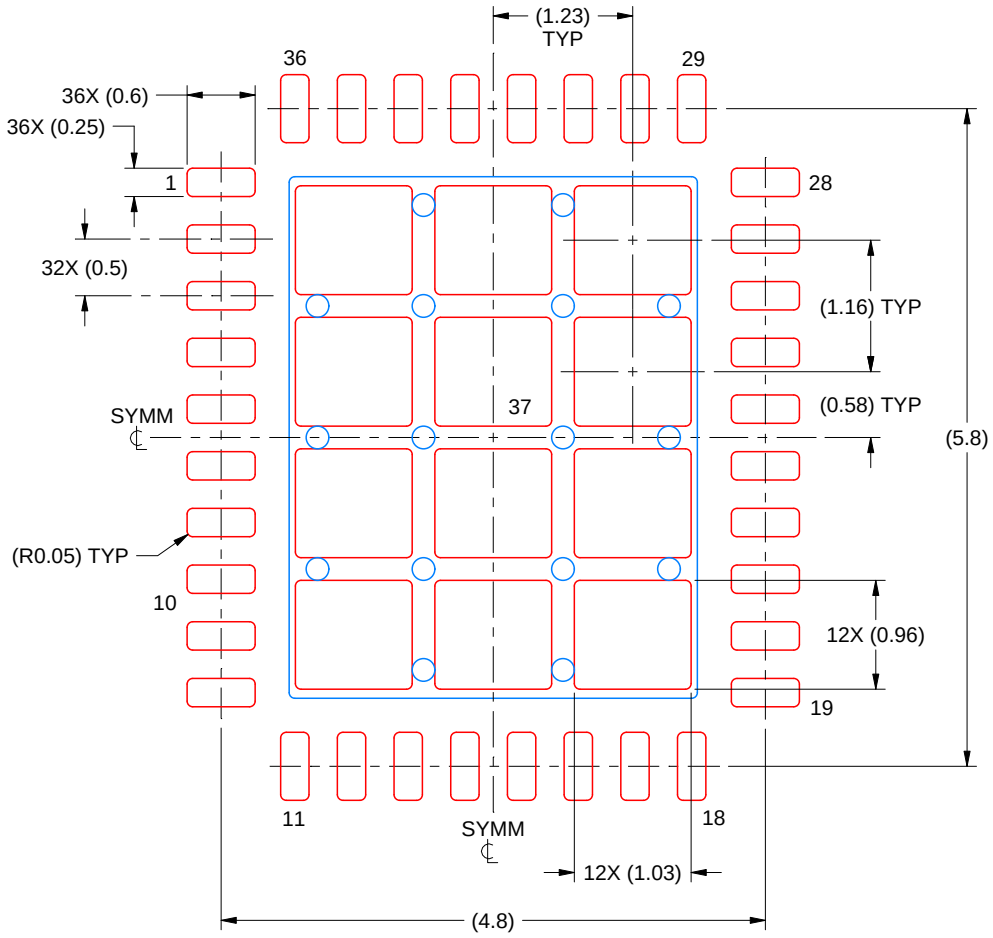
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## RRV0036B

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229473/B 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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