TCA9846 Ultra Low-Voltage 4-Channel 1MHz Capable I2C Switch

1 Features

- 1-to-4 bidirectional translating switches with ultra low voltage translation down to 0.65V
- I2C bus and SMBus compatible
- Active-low reset input
- 2 address pins, allowing up to 16 TCA9846 devices on the I2C bus
- Channel selection through an I2C Bus, in any combination
- Power up with all switch channels deselected
- Low R_{ON} switches
- Allows voltage-level translation between 0.65V, 0.8, 1.2V, 1.8V, 2.5V, and 3.3V
- No glitch on power up
- Supports hot insertion
- Low standby current
- Operating power-supply V_{DD2} voltage range of 1.65V to 3.6V
- Operating power-supply voltage V_{DD1} range of 0.65V to 3.6V
- 3.6V tolerant inputs
- 0 to 1MHz clock frequency
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - ±2000V human-body model (A114-A)
  - ±500V charged-device model (C101)

2 Applications

- Servers
- Routers (telecom switching equipment)
- Factory automation
- Products with I2C target address conflicts (such as multiple, identical temperature sensors)

3 Description

The TCA9846 is a quad bidirectional translating switch controlled via the I2C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

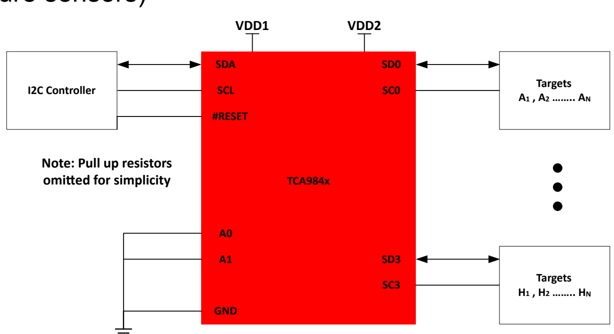
An active-low reset ($\overline{\text{RESET}}$) input allows the TCA9846 to recover from a situation in which one of the downstream I2C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I2C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed so that VDD1/VDD2 pins can be used to limit the maximum high voltage, which is passed by the TCA9846. Limiting the maximum high voltage allows the use of different bus voltages on each pair, so that 0.65V, 0.8V, 1.2V, or 1.8V parts can communicate with 3.3V parts, without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 3.6V tolerant.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TCA9846	PW (TSSOP, 16)	5mm × 6.4mm
	RUM (WQFN, 16)	4mm × 4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

Table of Contents

4 Pin Configuration and Functions

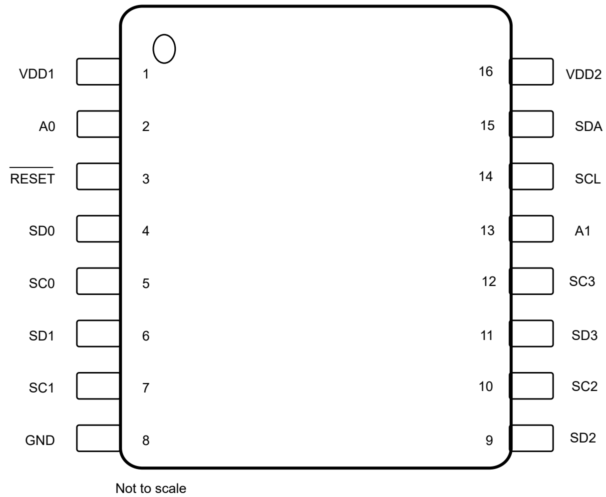


Figure 4-1. PW Package, 16-Pin TSSOP(Top View)

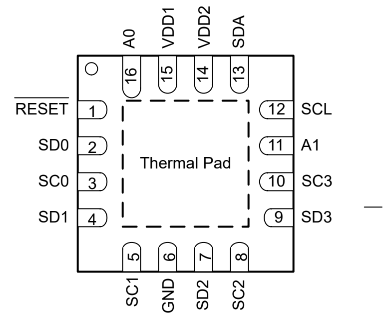


Figure 4-2. RUM Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TSSOP (PW)	WQFN (RUM)		
A0	2	16	I	Address input 0. Connect directly to V_{DD2} or ground
A1	13	11	I	Address input 1. Connect directly to V_{DD2} or ground
VDD1	1	15	Power	Logic Level Power Supply(VCC)
VDD2	16	14	Power	Core Logic Power Supply(VCC)
$\overline{RESET}$	3	1	I	Active-low reset input. Connect to V_{DD2} or V_{DPUM} (1) through a pull-up resistor, if not used
SD0	4	2	I/O	Serial data 0. Connect to V_{DPU0} (1) through a pull-up resistor
SC0	5	3	I/O	Serial clock 0. Connect to V_{DPU0} (1) through a pull-up resistor
SD1	6	4	I/O	Serial data 1. Connect to V_{DPU1} (1) through a pull-up resistor
SC1	7	5	I/O	Serial clock 1. Connect to V_{DPU1} (1) through a pull-up resistor
SD2	9	7	I/O	Serial data 2. Connect to V_{DPU2} (1) through a pull-up resistor
SC2	10	8	I/O	Serial clock 2. Connect to V_{DPU2} (1) through a pull-up resistor
SD3	11	9	I/O	Serial data 3. Connect to V_{DPU3} (1) through a pull-up resistor
SC3	12	10	I/O	Serial clock 3. Connect to V_{DPU3} (1) through a pull-up resistor
SCL	14	12	I/O	Serial clock bus. Connect to V_{DPUM} (1) through a pull-up resistor
SDA	15	13	I/O	Serial data bus. Connect to V_{DPUM} (1) through a pull-up resistor
GND	8	6	-	Supply Ground

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the controller I^2C reference voltage and V_{DPU0}-V_{DPU3} are the target channel reference voltages.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4	V
V_I	Input voltage(2)		–0.5	4	V
I_I	Input current		–20	20	mA
I_O	Output current		–25	25	mA
I_{CC}	Supply current		–100	100	mA
Tamb	Ambient Temperature	Ambient Temperature	-40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Tamb = –40°C to 125°C; unless otherwise specified

			MIN	TYP	MAX	UNIT
VDD1	Supply voltage 1		0.65		3.6	V
VDD2	Supply voltage 2		1.65		3.6	V
IDD (VDD2)	Supply Current on VDD2	VDD1 = 3.6; VDD2 = 3.6; SC0-7 and SD0-7 is not connected; RESET = VDD1; A0=A1=SCL; continuous register read/write				
		SCL = 0kHz		4	16	µA
		SCL = 100kHz		11	24	µA
		SCL = 1000kHz		56	150	µA
IDD (VDD1)	Supply Current on VDD1	VDD1 = 3.6; VDD2 = 3.6; SC0-7 and SD0-7 is not connected; RESET = VDD1; A0=A1=SCL; continuous register read/write				
		SCL = 0kHz	–5	0.11	+5	µA
		SCL = 100kHz		8	15	µA
		SCL = 1000kHz		58	100	µA
VPOR	Power-On Reset Voltage			1.2	1.5	V
T_A	Operating free-air temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TCA984x		UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.3	68.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.1	54.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.2	43.9	°C/W

THERMAL METRIC(1)		TCA984x PW (TSSOP) 16 PINS	TCA984x RUM (WQFN) 16 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	9.8	7.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	44	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	28.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics (Global)

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Recommended Supply Sequencing and Ramp Rates							
$(dV/dt)_f$	fall rate of change of voltage		–40°C to +125°C	0.1		2000	ms
$(dV/dt)_r$	rise rate of change of voltage		–40°C to +125°C	0.1		2000	ms
$t_{d(rst)}$	reset delay time		–40°C to +125°C	10			us
$\Delta V_{DD(gl)}$	glitch supply voltage difference		–40°C to +125°C			1	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width		–40°C to +125°C			10	us
$V_{POR(trip)}$	power-on reset trip voltage	Falling VDD2	–40°C to +125°C	0.7			V
		Rising VDD2	–40°C to +125°C			1.5	V
SCL/SDA							
V_{IH}	Logic voltage high		–40°C to +125°C	$0.7V_{DD1}$		3.6	V
V_{IL}	Logic voltage low		–40°C to +125°C	–0.5		$+0.3V_{DD1}$	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	–40°C to +125°C	20			mA
I_{IL}	Input leakage current	VI = VDD or 0	–40°C to +125°C	–1		1	uA
C_{IN}	Logic input capacitance	VI = VSS; all channels disabled	–40°C to +125°C		10	12	pF
SEL Inputs: A0A1, RESET							
V_{IH}	Logic voltage high		–40°C to +125°C	$0.7V_{DD1}$		3.6	V
V_{IL}	Logic voltage low		–40°C to +125°C	–0.5		$+0.3V_{DD1}$	V
I_{IL}	Input leakage current	VI = VDD or 0	–40°C to +125°C	–1		1	µA
C_{IN}	Logic input capacitance	VI = VSS; all channels disabled	–40°C to +125°C		2	4	pF
Pass Gate							
R_{ON}	ON-state resistance	VDD1 = 0.8V; VDD2 ≥ 1.65V; Vi(sw) = 0.16V; IO = 3mA	–40°C to +125°C		10	24	Ω
		VDD1 = 0.65V; VDD2 ≥ 1.65V; Vi(sw) = 0.16V; IO = 3mA	–40°C to +125°C		10	24	Ω
		VDD1 = 1.2V; VDD2 ≥ 1.8V; Vi(sw) = 0.24V; IO = 6mA	–40°C to +125°C		7	18	Ω
		VDD1 > 2V; VDD2 ≥ 2.5V; Vi(sw) = 0.4V; IO = 20mA	–40°C to +125°C		5	12	Ω
Io(sw)	Switch Output Current	VDD2 = 1.65V to 3.6V; Vi(sw) = VDD1 to 3.6V; Vo(sw) = VDD1 to 3.6V	–40°C to +125°C	0		100	µA
IL	Leakage current	VI = VDD or GND	–40°C to +125°C	–1		+1.5	µA
COFF	Input/Ouput Capacitance	VI = GND; all switches disables	–40°C to +125°C		3	5	pF

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
STANDARD MODE				
f_{scl}	I²C clock frequency	0	100	kHz
t_{sch}	I²C clock high time	4		µs
t_{scl}	I²C clock low time	4.7		µs
t_{sp}	I²C spike time	50		ns
t_{sds}	I²C serial-data setup time	250		ns
t_{sdh}	I²C serial-data hold time	0[1]		µs
t_{icr}	I²C input rise time		1000	ns

5.6 I^2C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_{icf}	I^2C input fall time			300	ns
t_{ocf}	I^2C output (SDn) fall time (10pF to 400pF bus)			300	ns
t_{buf}	I^2C bus free time between stop and start		4.7		µs
t_{sts}	I^2C start or repeated start condition setup		4.7		µs
t_{sth}	I^2C start or repeated start condition hold		4		µs
t_{sps}	I^2C stop condition setup		4		µs
$t_{vdL(Data)}$	Valid-data time (high to low)[(2)]	SCL low to SDA output low valid		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)[(2)]	SCL low to SDA output high valid		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	µs
C_b	I^2C bus capacitive load			400	pF
FAST MODE					
f_{scl}	I^2C clock frequency		0	400	kHz
t_{sch}	I^2C clock high time		0.6		µs
t_{scl}	I^2C clock low time		1.3		µs
t_{sp}	I^2C spike time		50		ns
t_{sds}	I^2C serial-data setup time		100		ns
t_{sdh}	I^2C serial-data hold time		0[(1)]		µs
t_{icr}	I^2C input rise time		$20 + 0.1C_b$ [(3)]	300	ns
t_{icf}	I^2C input fall time		$20 + 0.1C_b$ [(3)]	300	ns
t_{ocf}	I^2C output (SDn) fall time (10pF to 400pF bus)		$20 + 0.1C_b$ [(3)]	300	ns
t_{buf}	I^2C bus free time between stop and start		1.3		µs
t_{sts}	I^2C start or repeated start condition setup		0.6		µs
t_{sth}	I^2C start or repeated start condition hold		0.6		µs
t_{sps}	I^2C stop condition setup		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)[(2)]	SCL low to SDA output low valid		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)[(2)]	SCL low to SDA output high valid		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1	µs
C_b	I^2C bus capacitive load			400	pF
FAST MODE PLUS					
f_{scl}	I^2C clock frequency	I^2C clock frequency	0	1000	kHz
t_{sch}	I^2C clock high time	I^2C clock high time	0.26		µs
t_{scl}	I^2C clock low time	I^2C clock low time	0.5		µs
t_{sp}	I^2C spike time	I^2C spike time		50	ns
t_{sds}	I^2C serial-data setup time	I^2C serial-data setup time	100		ns
t_{sdh}	I^2C serial-data hold time	I^2C serial-data hold time	0[(1)]		µs
t_{icr}	I^2C input rise time	I^2C input rise time		120	ns
t_{icf}	I^2C input fall time	I^2C input fall time	20x (VDD / 5.5V) [(3)]	120	ns
t_{buf}	I^2C bus free time between stop and start	I^2C bus free time between stop and start	0.5		µs
t_{sts}	I^2C start or repeated start condition setup	I^2C start or repeated start condition setup	0.26		µs
t_{sth}	I^2C start or repeated start condition hold	I^2C start or repeated start condition hold	0.26		µs
t_{sps}	I^2C stop condition setup	I^2C stop condition setup	0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)[(2)]	SCL low to SDA output low valid		0.45	µs
$t_{vdH(Data)}$	Valid-data time (low to high)[(2)]	SCL low to SDA output high valid		0.45	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		0.45	µs

5.6 I2C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
C_b	I2C bus capacitive load	I2C bus capacitive load		550	pF

(1) A device internally must provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} min of the SCL signal), to bridge the undefined region of the falling edge of SCL.
(2) Data taken using a 1kΩ pullup resistor and 50pF load
(3) Cb = total bus capacitance of one bus line in pF

5.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{wrs(L)}$	Low-level reset time	100		ns
$t_{REC(STA)}$	Recovery time from $\overline{RESET}$ to start	0		ns

5.8 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤100pF (unless otherwise noted)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 50pF	SDA or SCL	SDn or SCn		1	ns
t_{rst} (2)	$\overline{RESET}$ time (SDA clear)		$\overline{RESET}$	SDA	500		ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by anideal voltage source (zero output impedance).
(2) t_{rst} is the propagation delay measured from the time the $\overline{RESET}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. t_{rst} must be a minimum of t_{WL}.

5.9 Typical Characteristics

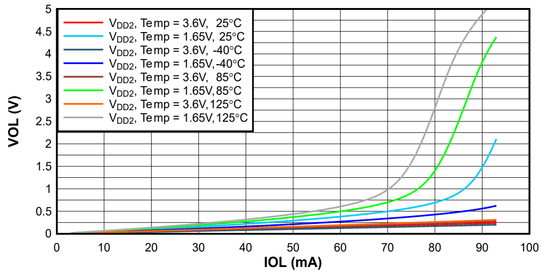


Figure 5-1. SDA Output Low Voltage (V_{OL}) vs Load Current (I_{OL}) at V_{DD2} Levels = 3.6V, 1.65V and T_A = -40 °C, 25 °C, 85 °C, 125 °C

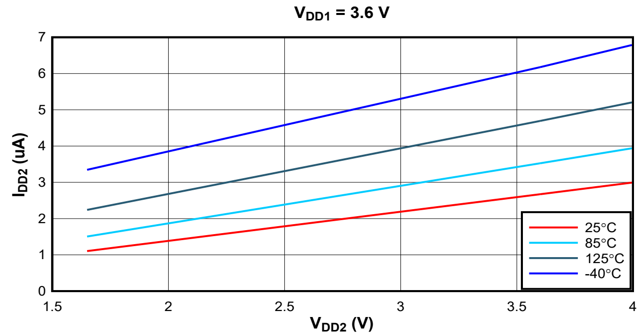


Figure 5-2. Standby Current (I_{DD}) vs Supply Voltage (V_{DD2}) at Four Temperature Points

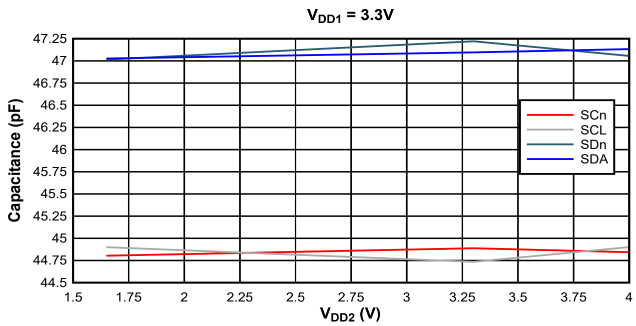


Figure 5-3. Target Channel (SCn/SDn) Capacitance ($C_{io(OFF)}$) vs Supply Voltage (V_{DD2}) at 25°C

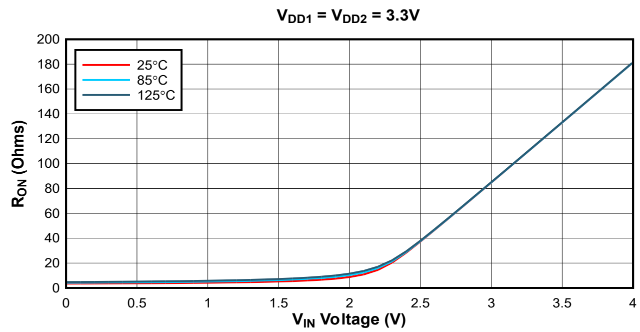
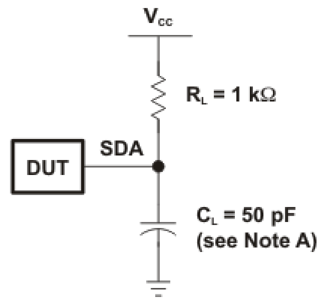
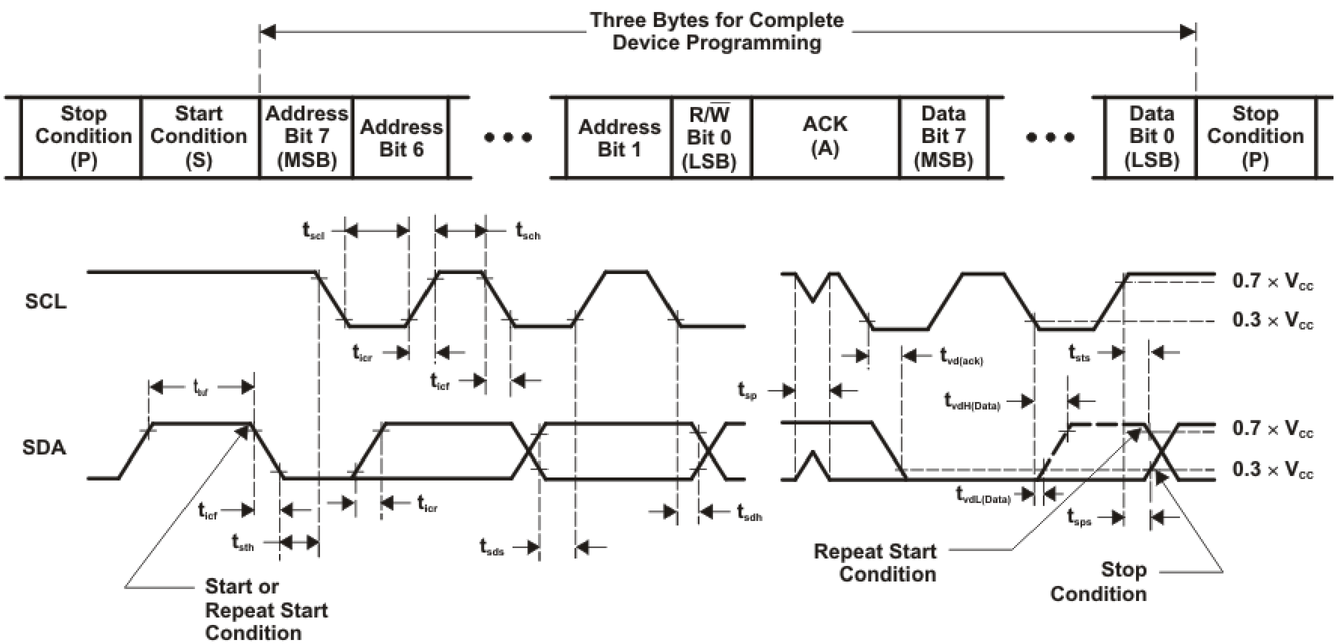


Figure 5-4. On-Resistance (R_{ON}) vs Input Voltage at Three Temperature Points

6 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

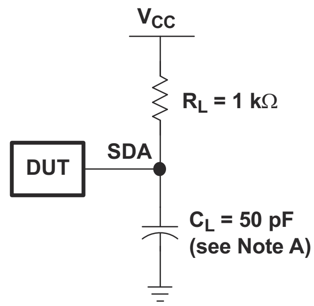
BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

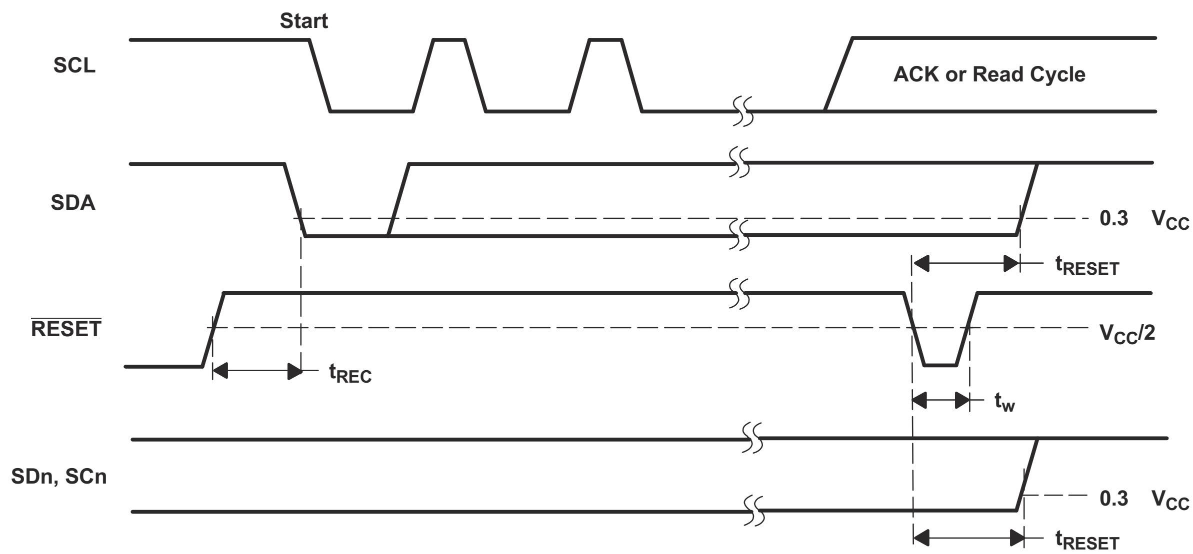
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.

C. Not all parameters and waveforms are applicable to all devices.

Figure 6-1. I²C Load Circuit and Voltage Waveforms



SDA LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. I/Os are configured as inputs.
D. Not all parameters and waveforms are applicable to all devices.

Figure 6-2. Reset Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

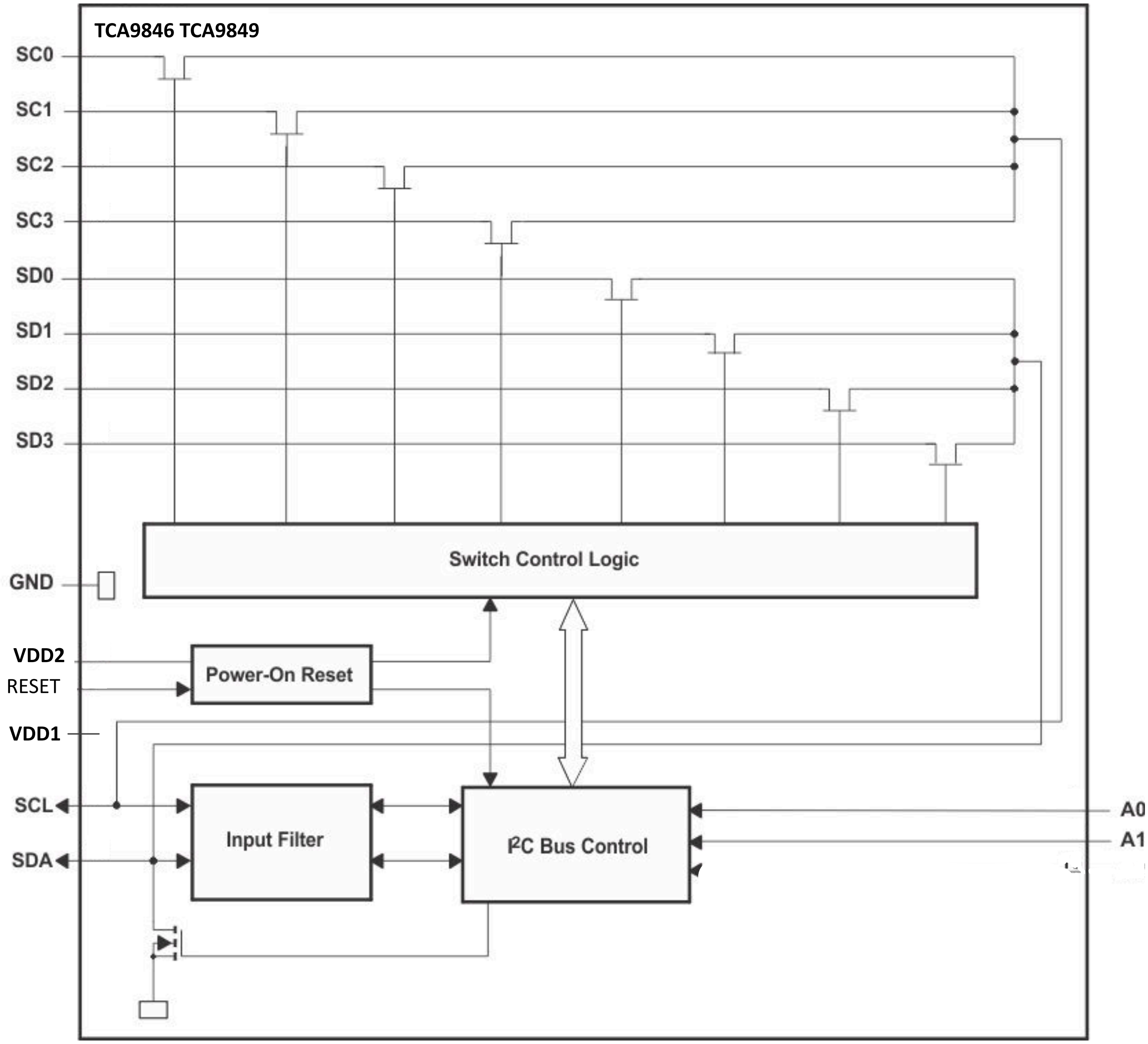
The TCA9846 is a 4-channel, bidirectional translating I2C switch. The controller SCL/SDA signal pair is directed to four channels of target devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels.

The device offers an active-low $\overline{\text{RESET}}$ input which resets the state machine and allows the TCA9846 to recover if one of the downstream I2C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, VCC(V_{DD2}), also known as a power-on reset (POR). Both the $\overline{\text{RESET}}$ function and a POR cause all channels to be deselected.

The connections of the I2C data path are controlled by the same I 2C controller device that is switched to communicate with multiple I2C targets. After the successful acknowledgment of the target address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The TCA9846 can also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 0.65V, 0.8V, 1.2V, or 1.8V parts can communicate with 3.3V parts. This action is achieved by using external pullup resistors to pull the bus up to the desired voltage for the controller and each target channel.

7.2 Functional Block Diagram



7.3 Feature Description

The TCA9846 is an 4-channel, bidirectional translating switch for I²C buses that supports Standard-Mode (100kHz), Fast-Mode (400kHz), and Fast-Mode-Plus (1Mhz) operation. The TCA9846 features I²C control using a single 8-bit control register in which each bit controls the enabling and disabling of one of the corresponding 4 switch channels for I²C data flow. Depending on the application, voltage translation of the I²C bus can also be achieved using the TCA9846 to allow 0.65V, 0.8V, 1.2V, or 1.8V parts to communicate with 3.3V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the TCA9846 can be reset to resume normal operation using the $\overline{RESET}$ pin feature or by a power-on reset which results from cycling power to the device.

7.4 Device Functional Modes

7.4.1 $\overline{RESET}$ Input

The $\overline{RESET}$ input is an active-low signal that can be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL}, the TCA9846 resets the registers and I²C state machine and deselects all channels. The $\overline{RESET}$ input must be connected to V_{CC} through a pullup resistor.

7.4.2 Power-On Reset

When power is applied to the VCC(V_{DD2}) pin, an internal power-on reset holds the TCA9846 in a reset condition until V_{CC} (V_{DD2}) has reached V_{PORR}. At this point, the reset condition is released, and the TCA9846 registers and I²C state machine are initialized to the default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below V_{PORF} to reset the device.

7.5 Programming

7.5.1 I²C Interface

The TCA9846 has a standard bidirectional I²C interface that is controlled by a controller device to be configured or read the status of this device. Each target on the I²C bus has a specific device address to differentiate between other target devices that are on the same I²C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical I²C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I²C lines. (For further details, see the *I²C Pull-up Resistor Calculation* application note. Data transfer can only be initiated when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition (See Figure 7-1 and Figure 7-2).

The following is the general procedure for a controller to access a target device:

1. If a controller wants to send data to a target:
   - Controller-transmitter sends a START condition and addresses the target-receiver.
   - Controller-transmitter sends data to target-receiver.
   - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
   - Controller-receiver sends a START condition and addresses the target-transmitter.
   - Controller-receiver sends the requested register to read to target-transmitter.
   - Controller-receiver receives data from the target-transmitter.
   - Controller-receiver terminates the transfer with a STOP condition.

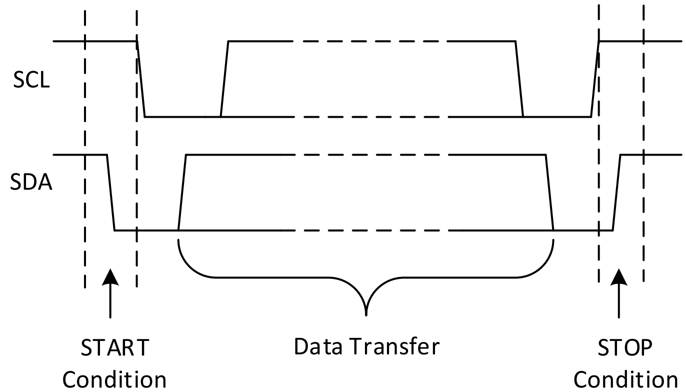


Figure 7-1. Definition of Start and Stop Conditions

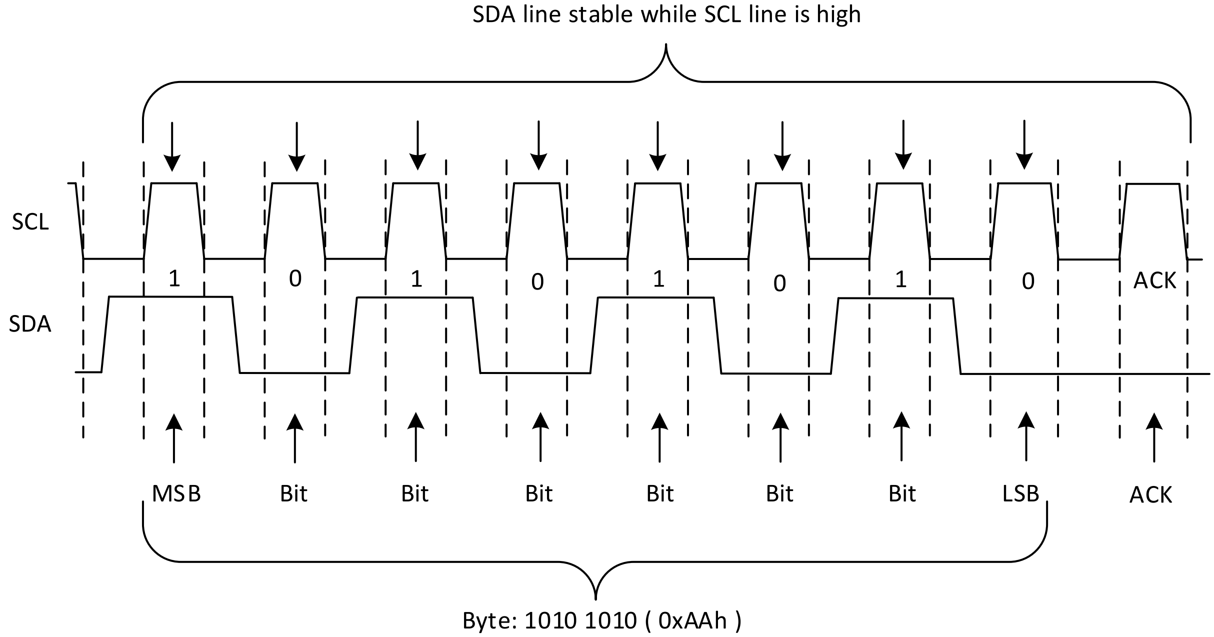


Figure 7-2. Bit Transfer

7.5.2 Device Address

The last bit of the target address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

For a read and write routine in software world for TCA984x, the actual address is 7 bit. For Example, 0xE2 = Write Operation on 0x71 I2C address (Address = 0x71 and then we shift left and add last bit for read/write, which has the I2C bus address write of 0xE2).

Table 7-1 shows the TCA9846 address reference.

Table 7-1. Address Reference

INPUTS		I^2C BUS TARGETADDRESS
A1	A0	
L	SCL	0xE0h (hexadecimal)
L	L	0xE2h (hexadecimal)
L	SDA	0xE4h (hexadecimal)
L:	H	0xE6h (hexadecimal)
H	SCL	0xE8h (hexadecimal)
H	L	0xEAh (hexadecimal)
H	SDA	0xECh (hexadecimal)
H	H	0xEEh (hexadecimal)
SCL	SCL	0xB0h (hexadecimal)
SCL	L	0xB2h (hexadecimal)
SCL	SDA	0xB4h (hexadecimal)
SCL	H	0xB6h (hexadecimal)
SDA	SCL	0xB8h (hexadecimal)
SDA	L	0xBAh (hexadecimal)
SDA	SDA	0xBCh (hexadecimal)
SDA	1	0xBEh (hexadecimal)

7.5.3 Bus Transactions

Data must be sent to and received from the target devices, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether configuration information or some sampled data to send back to the controller. The controller must write information to these registers to instruct the target device to perform a task.

While having registers in I^2C targets is common, note that not all target devices have registers. Some devices are simple and contain only 1 register, which can be written to directly by sending the register data immediately after the target address, instead of addressing a register. The TCA9846 is example of a single-register device, which is controlled through I^2C commands. Because it has 1 bit to enable or disable a channel, there is only 1 register needed, and the controller merely writes the register data after the target address, skipping the register number.

7.5.3.1 Writes

To write on the I^2C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. The target acknowledges, letting the controller know the target is ready. After this action, the controller starts sending the control register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

There is no limit to the number of bytes sent, but the last byte sent is what is in the register.

Figure 7-3 shows an example of writing a single byte to a target register.

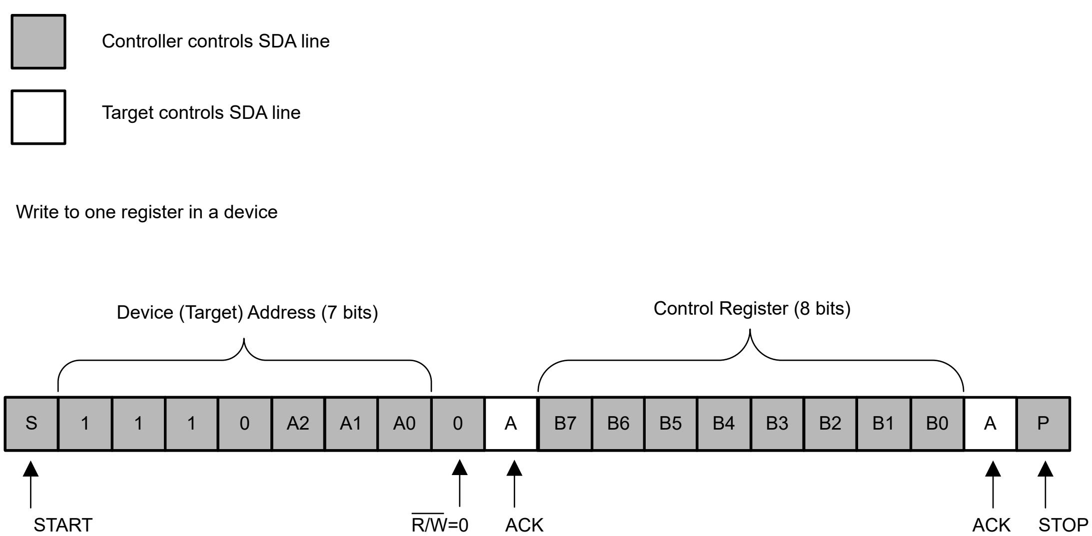


Figure 7-3. Write to Register

7.5.3.2 Reads

Reading from a target is very similar to writing, but the controller sends a START condition, followed by the target address with the R/$\overline{W}$ bit set to 1 (signifying a read). The target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that the controller is ready for more data. After the controller has received the number of bytes the controller is expecting, the controller sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

Figure 7-4 shows an example of reading a single byte from a target register.

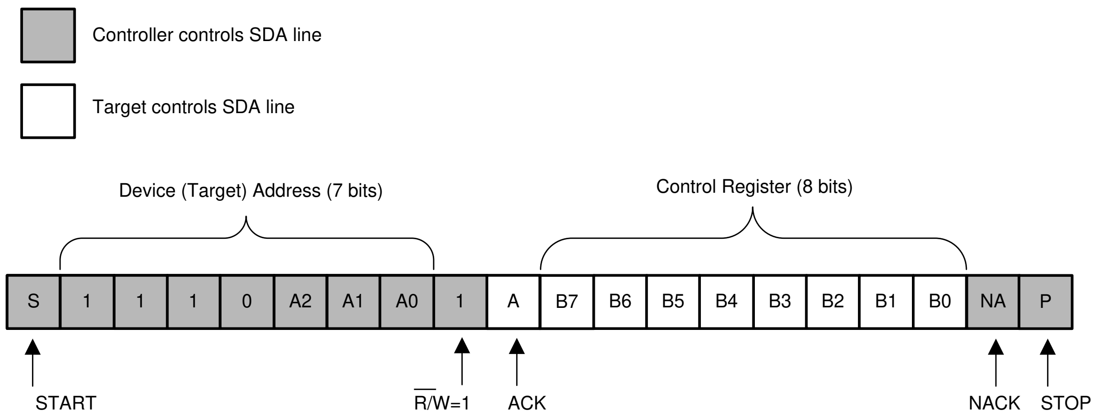


Figure 7-4. Read from Control Register

7.5.4 Control Register

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the TCA9846 (see Figure 7-5). This register can be written and read via the I^{2}C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels can be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^{2}C bus. This makes sure that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the TCA9848, the last byte received is saved.

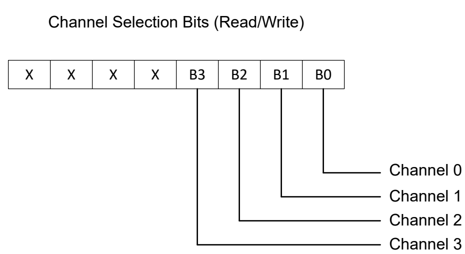


Figure 7-5. Control Register

Table 7-2 shows the TCA986 Command Byte Definition.

Table 7-2. Command Byte Definition

<table>
<tr><th colspan="8">CONTROL REGISTER BITS</th><th rowspan="2">COMMAND</th></tr>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>B3</th><th>B2</th><th>B1</th><th>B0</th></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td>Channel 0 disabled</td></tr>
<tr><td>1</td><td>Channel 0 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td>Channel 1 disabled</td></tr>
<tr><td>1</td><td>Channel 1 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 2 disabled</td></tr>
<tr><td>1</td><td>Channel 2 enabled</td></tr>
<tr><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>0</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">X</td><td>Channel 3 disabled</td></tr>
<tr><td>1</td><td>Channel 3 enabled</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>No channel selected, power-up/reset default state</td></tr>
</table>

7.5.5 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input is an active-low signal that can be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of t_{WL}, the TCA9846 resets its registers and I^2C state machine and deselects all channels. The $\overline{\text{RESET}}$ input must be connected to V_{CC} through a pull-up resistor.

7.5.6 Power-On Reset

When power (from 0V) is applied to V_{DD}, an internal power-on reset holds the TCA9846 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the TCA9846 registers and I^2C state machine initialize to the default states. After that, V_{CC} must be lowered to below V_{POR} and then back up to the operating voltage for a power-reset cycle.

7.5.7 Software Reset

The software reset call provides a mechanism to return all devices on the I²C bus to the power-up default state by issuing a specifically formatted I²C command. This operation assumes that the I²C bus is operating correctly and that no device is holding the bus in a latched or “hung” condition. The software reset sequence is defined as the following:

1. The I²C controller issues a START condition.
2. The controller transmits the reserved General Call address '0000 000' with the R/W bit set to 0 (write).
3. A device acknowledges only when the device detects the full General Call address 0000 0000 (00h). If the R/W bit is set to 1 (read), no acknowledge is generated.
4. After the General Call address is acknowledged, the controller transmits a single data byte with the value 06h.
    a. The device acknowledges only when this data byte is equal to 06h.
    b. If the data byte is not 06h, or if more than one data byte is transmitted, the device does not acknowledge further.
    c. When the correct byte has been received and acknowledged, the controller must issue a STOP condition to complete the Software Reset sequence. At this point, the device resets the registers to the power-up default values and becomes ready for subsequent bus transactions after the required bus-free time.
    d. If a Repeated START condition is issued instead of a STOP, the reset is not performed.
    e. Any missing acknowledge from the device at any point in this sequence is treated by the controller as a Software Reset Abort. In such a case, the device does not initiate any register reset.

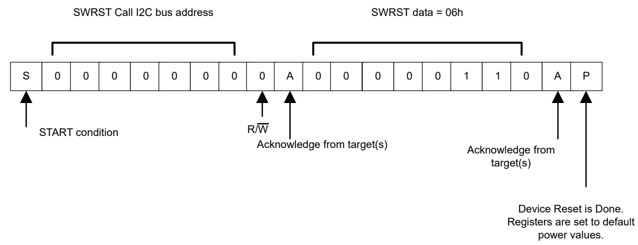


Figure 7-6. Software Reset Sequence

7.5.8 Device ID

The Device ID is a 24-bit (3-byte) read-only value containing the following fields:

- 12 bits: manufacturer identifier (unique per manufacturer, for example, TI)
- 9 bits: part number (assigned by the manufacturer)
- 3 bits: die revision (assigned by the manufacturer)

The Device ID is hardwired and accessible using the following procedure:

1. Send a START command.
2. The controller transmits the Reserved Device ID I²C address (1111 1000) with R/W = 0 (write).
3. The controller sends the target device address, with the LSB as "don't care." Only the matching device acknowledges.
4. Issue a Repeated START condition.
    a. A STOP command followed by a START command resets the target state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another target device resets the target state machine and the Device ID Read cannot be performed.
5. The controller sends the Reserved Device ID I²C address (1111 1001) with R/W = 1 (read).
6. The device transmits the Device ID in the following order:
    a. First byte + 4 MSBs of second byte: Manufacturer ID (12 bits)
    b. 4 LSBs of second byte + 5 MSBs of third byte: Part Identification (9 bits)
    c. 3 LSBs of third byte: Die Revision (3 bits)
7. The controller completes the read by sending a NACK after the last byte, resetting the device internal state machine and then issuing a STOP command.

If the controller sends additional acknowledgments after the third byte, the device restarts the data sequence from the first byte.

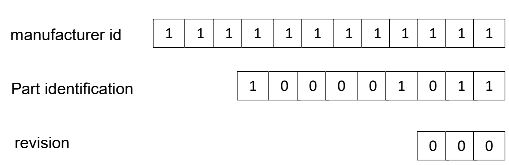


Figure 7-7. Device ID

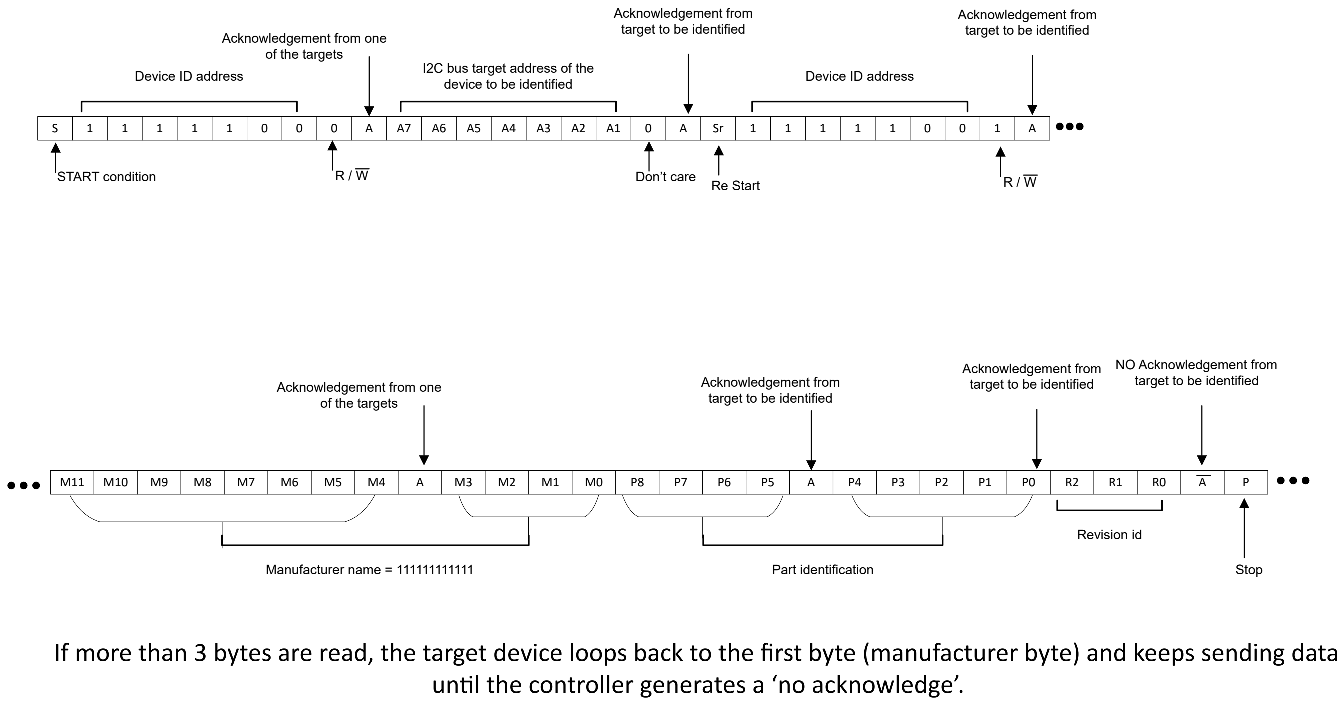


Figure 7-8. Device ID Sequence

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Applications of the TCA9846 contain an I^2C (or SMBus) controller device and up to eight I^2C target devices. The downstream channels are used to resolve I^2C target address conflicts. For example, if 4 identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0-3. When the temperature at a specific location is read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C controller can move on and read the next channel.

In an application where the I^2C bus contains many additional target devices that do not result in I^2C target address conflicts, these target devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (see the *Design Requirements* section and *Detailed Design Procedure* section).

8.2 Typical Application

Figure 8-1 shows an application in which the TCA9846 can be used.

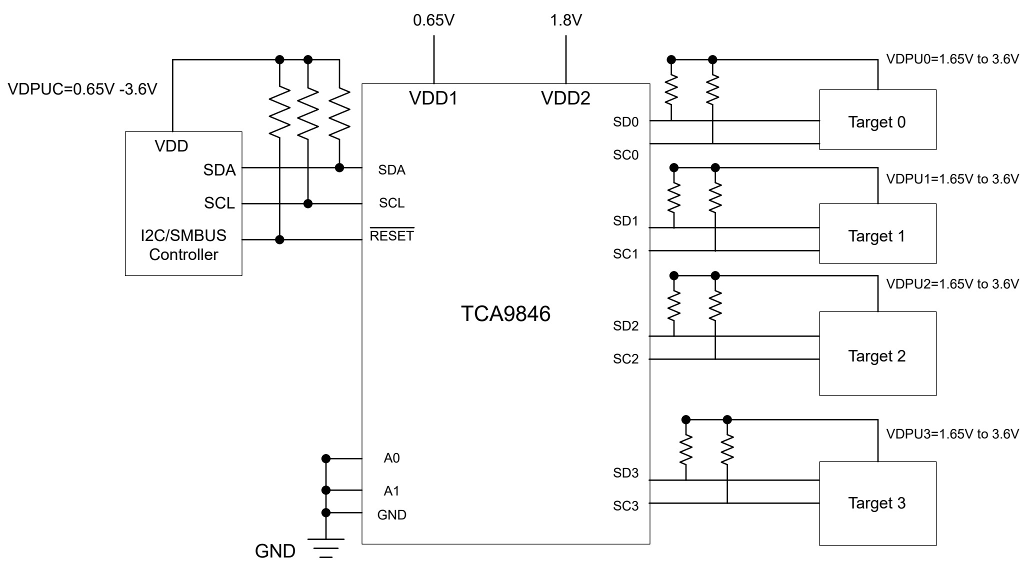


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

A typical application of the TCA9846 contains one or more data pull-up voltages, V_{DPUX}, one for the controller device (V_{DPUM}) and one for each of the selectable target channels (V_{DPU0} – V_{DPU7}). In the event where the controller device and all target devices operate at the same voltage, then V_{DPUM} = V_{DPUX} = VCC. In an application where voltage translation is necessary, additional design requirements must be considered to determine an appropriate V_{CC} voltage.

The A0, A1 pins are hardware selectable to control the target address of the TCA9846. These pins can be tied directly to GND or V_{CC} in the application.

If multiple target channels are activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the controller side is the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the TCA9846 are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

For the TCA9846 to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage.

8.2.1.1 Voltage Translation Requirements

UPSTREAM BUS VOLTAGE OR CONTROLLER PULLUP RESISTOR VOLTAGE VDPUC	TCA98xx VDD1 SUPPLY VOLTAGE	CHANNEL PASS TRANSISTOR CLAMP VOLTAGE	TCA98xx VDD2 SUPPLY VOLTAGE	LOWEST DOWNSTREAM BUS VOLTAGE VDPUx	COMMENTS
0.65	0.65	0.65	1.65-3.6	0.65-3.6	OK
1.8-3.6	0.65	0.65	1.65-3.6	0.65	OK
1.8	1.8	1.8	1.8-3.6	1.8-3.6	OK
2.5	2.5	1.8	1.8	1.8	OK
2.5	2.5	2.5	2.3-3.6	2.3-3.6	OK
3.6	3.6	1.8	1.8	1.8	OK
3.6	3.6	2.5	2.5	2.5	OK
3.6	3.6	3.6	3.6	3.6	OK
1.8	1.8	1.8	1.8	0.65	**NOT OK**
2.5	2.5	1.8	1.8	0.65	**NOT OK**
3.6	3.6	1.8	1.8	0.65	**NOT OK**

There is no buffering capability between the upstream and the downstream buses. This is simply a pass transistor, which acts like a multiplexer and a series resistor, between these bus segments.

8.2.2 Detailed Design Procedure

Once all the targets are assigned to the appropriate target channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pullup resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 1:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pullup resistance is a function of the maximum rise time, t_r (300ns for fast-mode operation, f_{SCL} = 400kHz) and bus capacitance, C_b as shown in Equation 2:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I^2C bus must not exceed 400pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9846, $C_{io(OFF)}$, the capacitance of wires, connections and traces, and the capacitance of each individual target on a given channel. If multiple channels are activated simultaneously, each of the targets on all channels contribute to total bus capacitance.

8.2.3 Application Curves

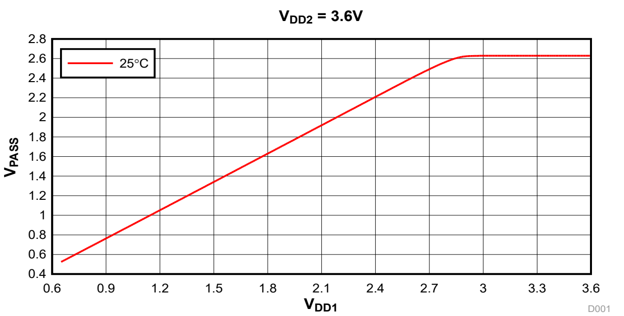
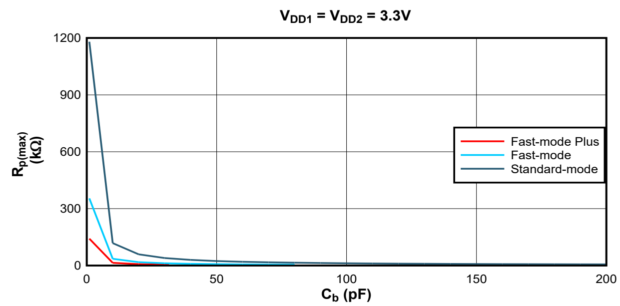


Figure 8-2. Pass-Gate Voltage (V_{pass}) vs V_{DD1} (V_{DD2} =3.6V at 25°C)



Standard-mode (f_{SCL} = 100kHz, t_r = 1µs)	Fast-mode (f_{SCL} = 400kHz, t_r = 300ns)	Fast-mode Plus (f_{SCL} = 1000kHz, t_r = 120ns)

Figure 8-3. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)

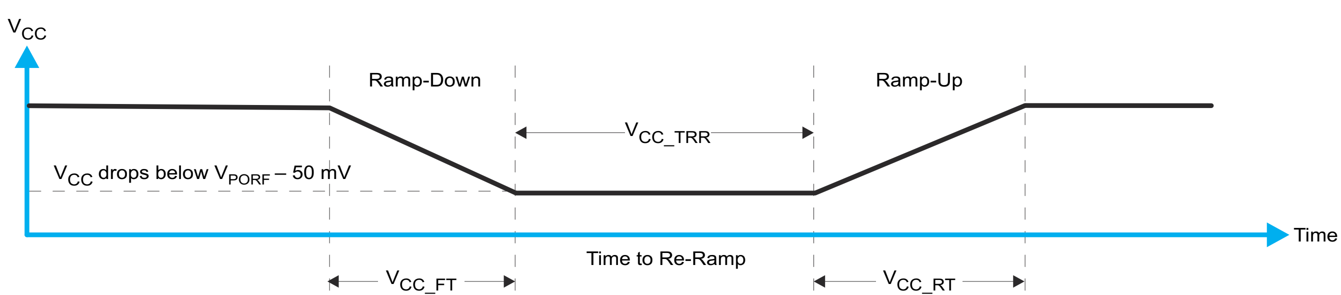
8.3 Power Supply Recommendations

The operating power-supply voltage range of the TCA9846 is 0.65V to 3.6V for VDD1 and 1.65-3.6V for VDD2. Whenever the TCA9846 is powered on, the device executes a power-on reset. Make sure the power supply sequencing follows the power-on reset requirements in the following section. The power-on reset requirements must be followed to make sure the I^2C bus logic is initialized properly.

8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9846 can be reset to the default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 8-4.



V_{CC} (V_{DD2}) is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC} (V_{DD2})

Figure 8-4. Power-On Reset Waveform

Table 8-1 specifies the performance of the power-on reset feature for TCA9846 for both types of power-on reset.

Table 8-1. Recommended Supply Sequencing and Ramp Rates VCC(V_{DD2})

PARAMETER[1]			MIN	MAX	UNIT
V_{CC_FT}	Fall time	See Figure 8-4	0.1	2000	ms
V_{CC_RT}	Rise time	See Figure 8-4	0.1	2000	ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops below $V_{PORF(min)}$ – 50mV or when V_{CC} drops to GND)	See Figure 8-4	10		µs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1µs	See Figure 8-5		1	V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC}	See Figure 8-5		10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 8-5 and Table 8-1 provide more information on how to measure these specifications.

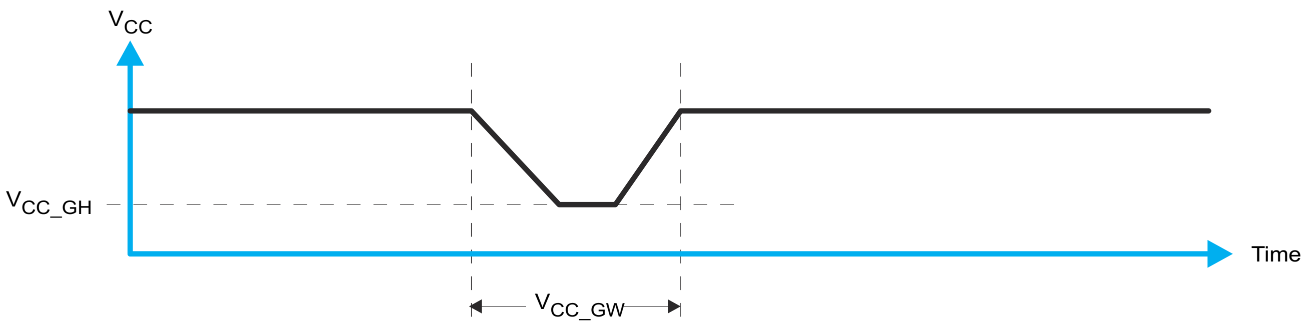


Figure 8-5. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to the default states. The value of V_{POR} differs based on the V_{CC} (V_{DD2}) being lowered to or from 0. Figure 8-6 and Table 8-1 provide more details on this specification.

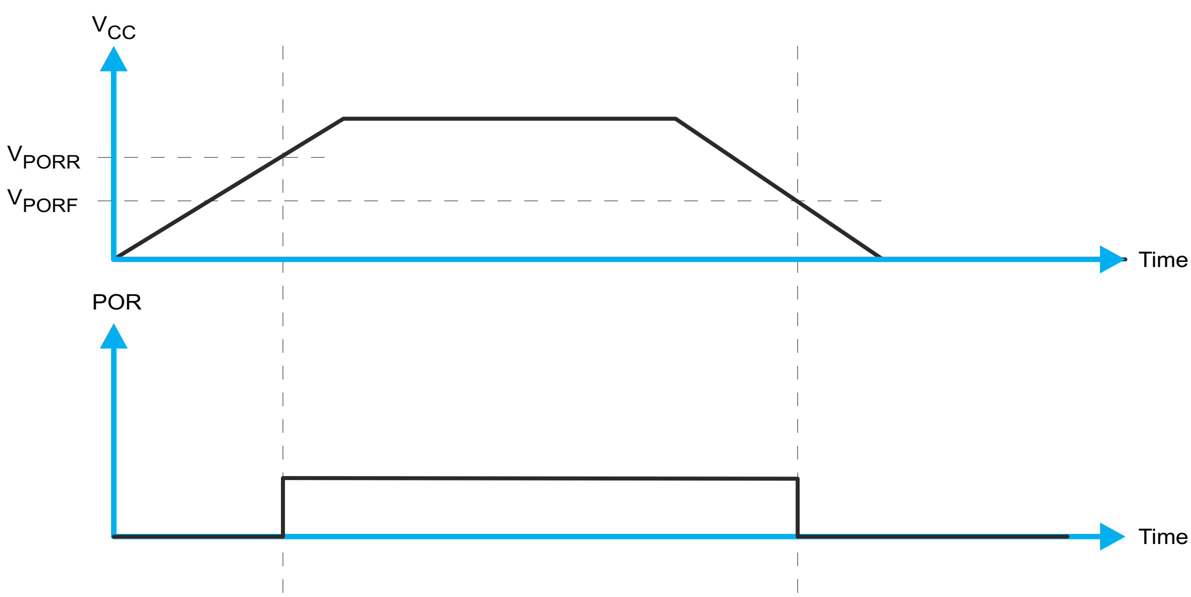


Figure 8-6. V_{POR}

8.4 Layout

8.4.1 Layout Guidelines

For PCB layout of the TCA9846, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. Having a dedicated ground plane on an inner layer of the board is common, and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. Bypass and decoupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} can be at the same potential and a single copper plane can connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM} and V_{DPU0} – V_{DPU7}, can all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn and SDn) must be a short as possible and the widths of the traces must also be minimized (for example, 5-10 mils depending on copper weight).

8.4.2 Layout Example

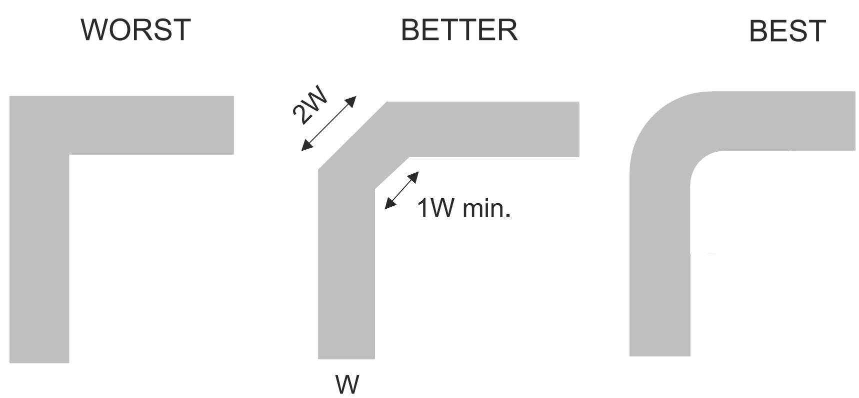


Figure 8-7. Layout Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *I2C Bus Pullup Resistor Calculation* application note
- Texas Instruments, *Maximum Clock Frequency of I2C Bus Using Repeaters* application note
- Texas Instruments, *Introduction to Logic* application note
- Texas Instruments, *Understanding the I2C Bus* application note
- Texas Instruments, *Choosing the Correct I2C Device for New Designs* application note
- Texas Instruments, *TCA9548AEVM* user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2026) to Revision B (September 2026)	Page
• Updated datasheet status from *Advanced Information* to *Production Data*	1
• Removed ordering information	1
• Added Thermal Information	4
• Added Typical Characteristics	9
• Added Application Curves	24

Changes from Revision * (March 2026) to Revision A (May 2026) **Page**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCA9846PWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TCA9846PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TC9846

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

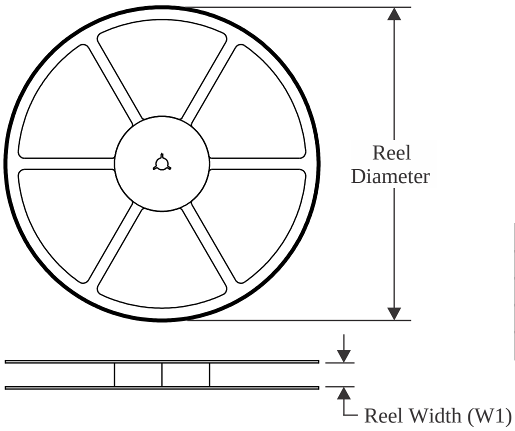
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

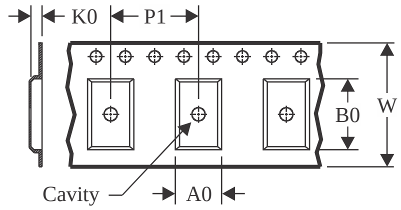
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

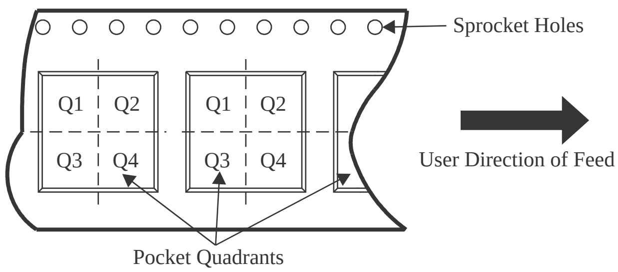


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

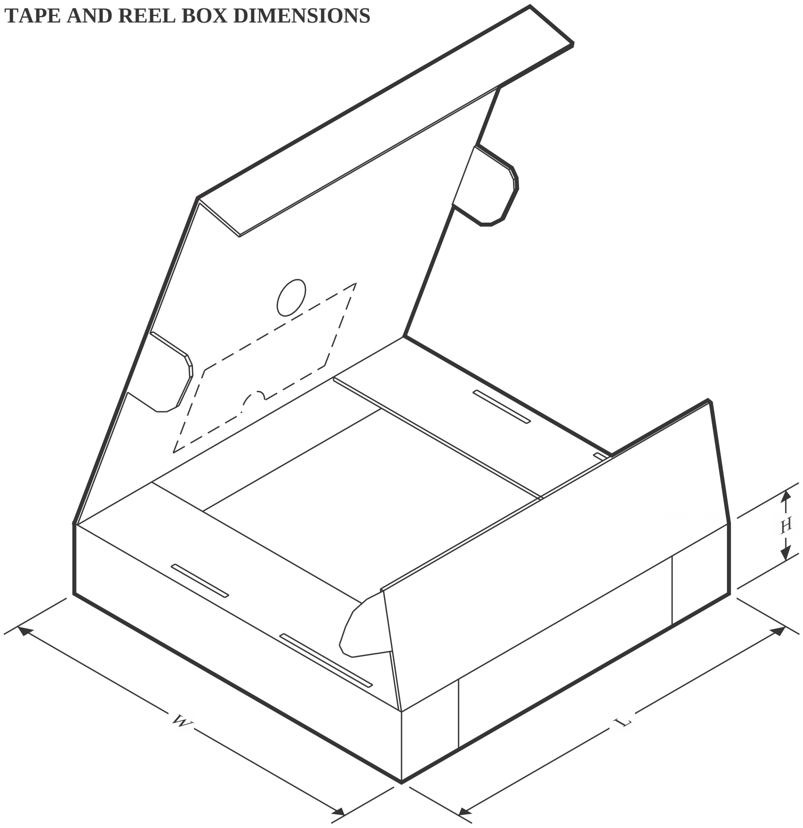
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

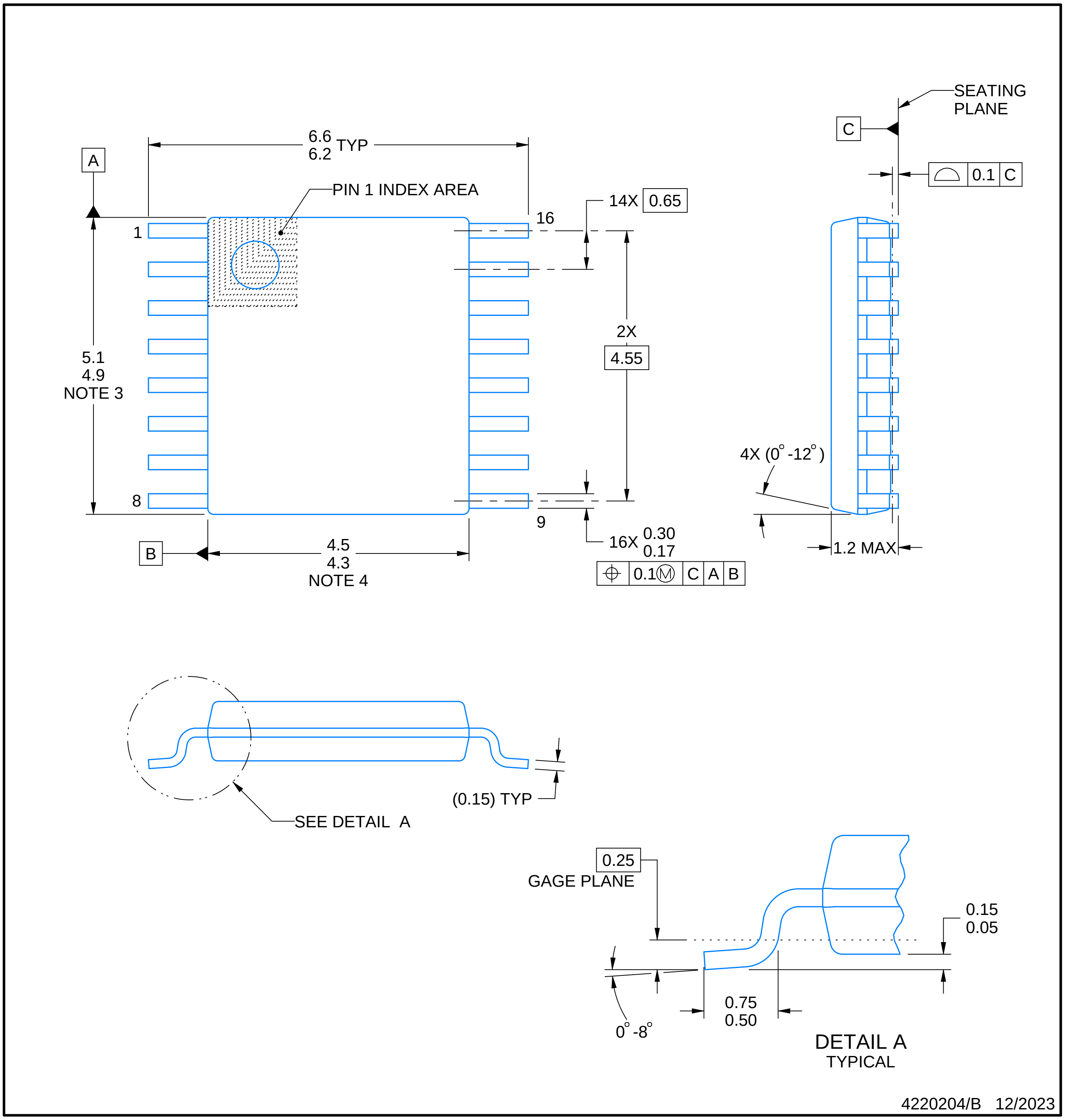
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9846PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

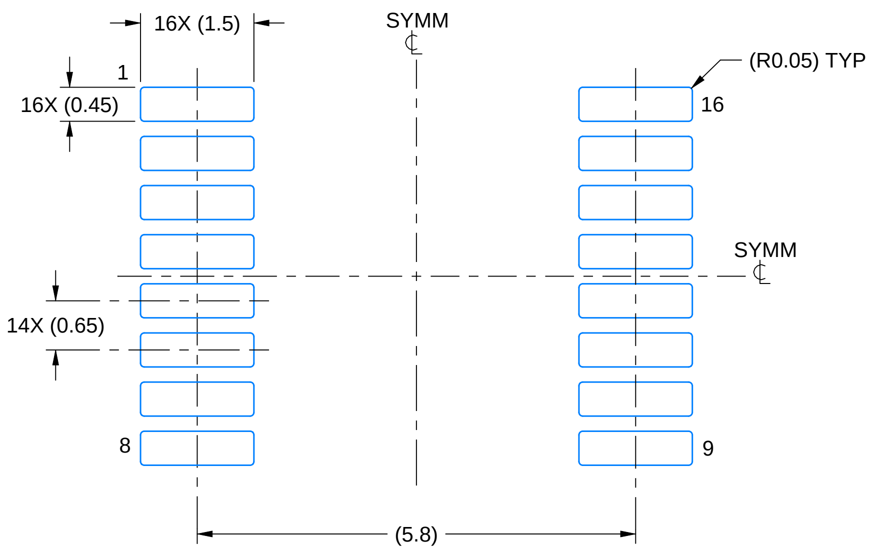
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9846PWR	TSSOP	PW	16	3000	353.0	353.0	32.0



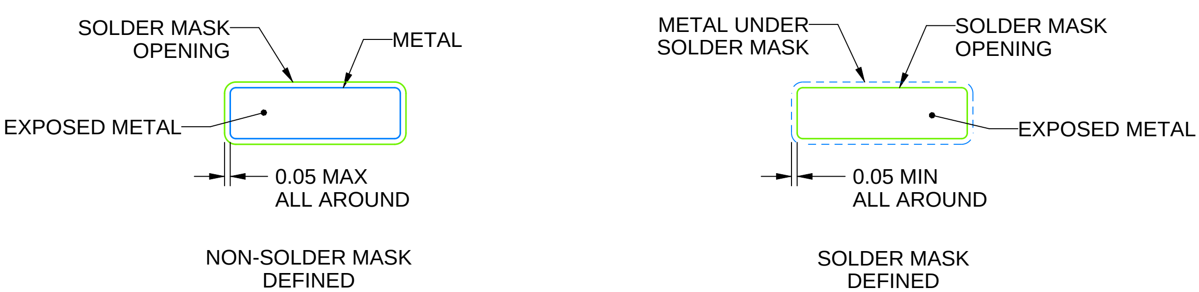
4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

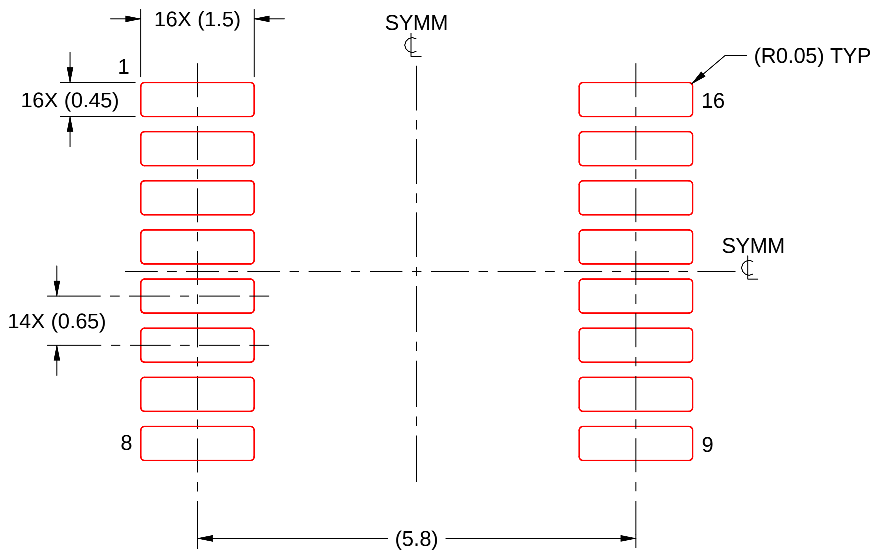


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.