LMX2624-SP 5MHz to 30GHz Wideband Synthesizer With Phase Synchronization and JESD204B/C Support

1 Features

- SMD 5962R2321001PXE
  - Total ionizing dose 100Krad (ELDRS-free)
  - Single event latch-up (SEL) immune up to 75MeV-cm^2/mg
  - Single event functional interrupt (SEFI) immune up to 75MeV-cm^2/mg
- Wide band frequency synthesizer : 5MHz to 30GHz output frequency
- –102dBc/Hz phase noise at 100kHz offset with 30GHz carrier
- 62fs RMS jitter at 30GHz (1kHz to 100MHz)
- Programmable output power
- PLL key specifications:
  - Figure of merit: –236dBc/Hz
  - Normalized 1/f noise: –129dBc/Hz
  - Up to 200MHz phase detector frequency in fractional mode.
- Synchronization of output phase across multiple devices
- Independent mute pins for RFoutA and RFoutB outputs
- Support for SYSREF with programmable delay
- 3.3V single power supply operation
- Pin-mode: Pin configurable N divider and output divider in Integer PLL mode
- 10 × 10mm² 64 lead QFP package
- Operating temperature range: –55°C to +125°C
- Supported by PLLatinum™ Simulator design tool

2 Applications

- Space communications payload up to Ku/Ka bands
- Space radar systems
- Command and Data handling system
- High-speed data converter clocking (supports JESD204B/C)
- Local Oscillator for Mixer up to 30GHz frequency

3 Description

The LMX2624-SP is a high performance wideband phase-locked loop (PLL) with integrated voltage controlled oscillator (VCO) that can output any frequency from 5MHz to 30GHz. The VCO on this device covers an entire octave so the frequency coverage is complete down to 5MHz. The high performance PLL with a figure of merit of –236dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter.

The LMX2624-SP allows users to synchronize the output of multiple instances of the device. This means that deterministic phase can be obtained from a device in use cases including the one with fractional engine or output divider enabled. The device also adds support for either generating or repeating SYSREF (compliant to JESD204B/C standard), making the device designed for low-noise clock source for high-speed data converters.

This device is fabricated in Texas Instruments' advanced BiCMOS process and is available in a 64-lead QFP plastic package.

Package Information

PART NUMBER	TYPE	PACKAGE(1)	PACKAGE SIZE(2)
5962R2321001PXE	Radiation Hardness Assured	QFP 64-pin	10mm × 10mm
LMX2624PAP/EM(3)	Engineering Samples		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) These units are intended for engineering evaluation only. They are not put through a compliant flow (so there is no burn-in, only 25ºC testing, and so forth.). Additionally, these units are not suitable for qualification, production, radiation testing, or flight use. The parts are not warranted for performance over temperature or operating life.

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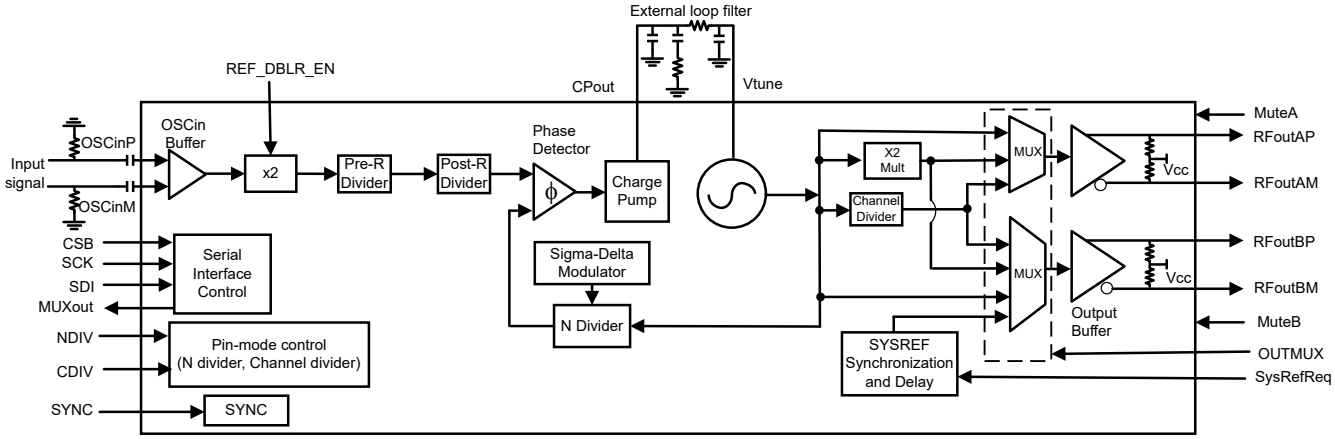

Functional Block Diagram

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4 Pin Configuration and Functions

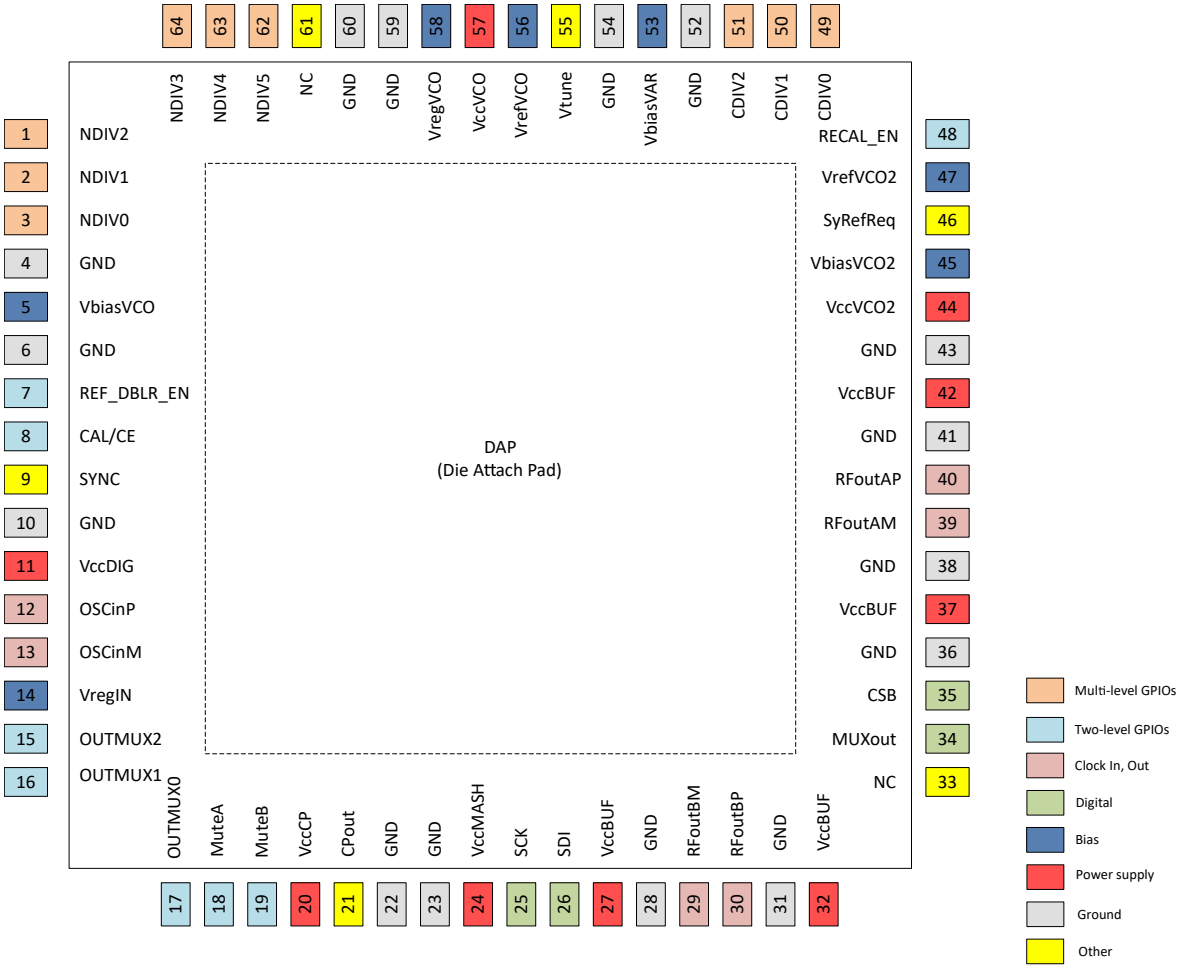

Figure 4-1. HBD Package 64-Pin CQFP Top View

Table 4-1. Pin Functions

PIN		TYPE[(1)]	TYPE	DESCRIPTION
NO.	NAME			
1	NDIV2	I	4-level pin	Integer N divider bit 2 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
2	NDIV1	I	4-level pin	Integer N divider bit 1 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
3	NDIV0	I	4-level pin	Integer N divider bit 0 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
4	GND	—	—	Ground
5	VbiasVCO	—	—	VCO bias. Requires connecting 10µF capacitor to ground. Place close to pin.
6	GND	—	—	Ground
7	REF_DBLR_EN	I	—	Input Reference Doubler enable in Pin-mode. A HIGH on this pin enables the reference doubler and LOW on this pin bypass the Input Reference Doubler. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	TYPE	DESCRIPTION
NO.	NAME			
8	CAL/CE	I	—	Chip enable. In Pin Mode (not SPI-mode), rising edges presented to this pin activate the VCO calibration. In SPI-mode, this pin acts like CE where a high on CE pin make device to enable and Low disables the device.
9	SYNC	I	—	Phase synchronization SYNC signal input pin. CMOS input. If not being used, connect to ground using a 1kΩ resistor.
10	GND	—	—	Ground
11	VccDIG	—	—	Digital supply. Connect to 3.3V with a 0.1µF capacitor to ground.
12	OSCinP	I	—	Reference Input clock pin (+). High input impedance. Requires connecting series capacitor (0.1µF recommended). For single-ended input, 50Ω resistor to GND needed before AC-coupling series capacitor. For Differential input, use 100Ω resistor between OSCinP and OSCinM.
13	OSCinM	I	—	Complimentary pin to OSCinP (-). If not being used, AC-coupled to GND through a 50Ω resistor.
14	VregIN	—	—	Input reference path regulator decoupling. Requires connecting 1µF capacitor to ground. Place close to pin.
15	OUTMUX2	I	—	Controls the Output Mux selection together with OUTMUX1 and OUTMUX0 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
16	OUTMUX1	I	—	Controls the Output Mux selection together with OUTMUX2 and OUTMUX0 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
17	OUTMUX0	I	—	Controls the Output Mux selection together with OUTMUX2 and OUTMUX1 for RFOUTA and RFOUTB. The eight options include selecting VCO output, Doubler output or Channel Divider output combinations for RFOUTA and RFOUTB. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
18	MuteA	I	—	Output Buffer mute control. High-impedance CMOS input. RFOUTA is muted or unmuted using a MuteA pin
19	MuteB	I	—	Output Buffer mute control. High-impedance CMOS input. RFOUTB is muted or unmuted using a MuteB pin
20	VccCP	I	—	Charge pump supply. Connect to 3.3V with a 0.1µF capacitor to ground.
21	CPout	O	—	Charge pump output. Recommend connecting C1 of loop filter close to charge pump pin.
22	GND	—	Ground	Ground
23	GND	—	Ground	Ground
24	VccMASH	—	—	Digital supply. Connect to 3.3V with a 0.1µF and a 10µF capacitor to ground.
25	SCK	I	—	SPI input clock. High impedance CMOS input. 1.6V – 3.3V logic.
26	SDI	I	—	SPI input data. High impedance CMOS input. 1.6V – 3.3V logic.
27	VccBUF	—	—	Output buffer supply. Connect to 3.3V with a 0.1µF capacitor to ground.
28	GND	—	Ground	Ground
29	RFoutBM	O	—	Differential output B Pair. 50Ω resistor pullup to V_{CC} is integrated. Can be used as a synthesizer output or SYSREF output.
30	RFoutBP	O	—	Differential output B Pair. 50Ω resistor pullup to V_{CC} is integrated. Can be used as a synthesizer output or SYSREF output.
31	GND	—	Ground	Ground
32	VccBUF	—	—	Output buffer supply. Connect to 3.3V with a 0.1µF capacitor to ground.
33	NC	—	—	Connect this pin to either V_{CC} or ground through 1KΩ resistor. This does not affect the performance.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[(1)]	TYPE	DESCRIPTION
NO.	NAME			
34	MUXout	—	—	Multiplexed output pin. Can output: lock detect, SPI readback and diagnostics.
35	CSB	—		SPI chip select bar. High impedance CMOS input. 1.6V – 3.3V logic.
36	GND	—	Ground	Ground
37	VccBUF	—	—	Output buffer supply. Connect to 3.3V with a 0.1µF capacitor to ground.
38	GND	—	Ground	Ground
39	RFoutAM	O	—	Differential output A Pair. 50Ω resistor pullup to V_{CC} is integrated.
40	RFoutAP	O	—	Differential output A Pair. 50Ω resistor pullup to V_{CC} is integrated.
41	GND	—	Ground	Ground
42	VccBUF	—	—	Output buffer supply. Connect to 3.3V with a 0.1µF capacitor to ground.
43	GND	—	Ground	Ground
44	VccVCO2	—	—	VCO supply. Connect to 3.3V with a 0.1µF and a 10µF capacitor to ground.
45	VbiasVCO2	—	—	VCO bias. Requires connecting 1µF capacitor to ground.
46	SysRefReq	I	—	SYSREF request input for JESD204B/C support.
47	VrefVCO2	—	—	VCO supply reference. Requires connecting 10µF capacitor to ground.
48	RECAL_EN	I	—	Enables the automatic recalibration feature. Low on this pin does not trigger calibration. High on this means the calibration is triggered whenever the device is unlocked after certain delay. This pin has internally 200kΩ pull-up.
49	CDIV0	I	4-level pin	Controls the Channel Divider along with CDIV2 and CDIV1 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
50	CDIV1	I	4-level pin	Controls the Channel Divider along with CDIV0 and CDIV2 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
51	CDIV2	I	4-level pin	Controls the Channel Divider along with CDIV1 and CDIV0 in Pin-mode option. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
52	GND	—	Ground	Ground
53	VbiasVARAC	—	—	VCO Varactor bias. Requires connecting 10µF capacitor to ground.
54	GND	—	Ground	Ground
55	Vtune	I	—	VCO tuning voltage input.
56	VrefVCO	—	—	VCO supply reference. Requires connecting 10µF capacitor to ground.
57	VccVCO	—	—	VCO supply. Connect to 3.3V with a 0.1µF and a 10µF capacitor to ground.
58	VregVCO	—	—	VCO regulator node. Requires connecting 1µF capacitor to ground.
59	GND	—	Ground	Ground
60	GND	—	Ground	Ground
61	NC	—	NC	Connect this pin to VCC through 1KΩ resistor.
62	NDIV5	I	4-level pin	Integer N divider bit 5 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
63	NDIV4	I	4-level pin	Integer N divider bit 4 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
64	NDIV3	I	4-level pin	Integer N divider bit 3 in Pin-mode. This is part of NDIV5-NDIV0, 6 bit value for N divider setting. Refer Pin-mode description details in Pin-Mode Integer Frequency Generation for more details.
—	DAP	—	Ground	Die Attach Pad. Connect DAP to PCB ground plane using multiple vias for good thermal performance.

(1) I=Input; O=Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Power supply voltage[1]	–0.3	3.6	V
V_{DIG}	Digital pin voltage (SYNC, SysRefReq, RECAL_EN, CAL, MUXout, REF_DBLR_EN, MuteX, OUTMUXx, CHDIVx, NDIVx)	−0.3	3.6	V
$\|V_{OSCin}\|$	Differential AC voltage between OSCinP and OSCinM		2.1	V_{PP}
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins[2]	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.2	3.3	3.45	V
T_C	Case temperature	–55	25	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		CQFP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	19.95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.84	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.91	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.11	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.87	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance [2]	0.45	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) DAP

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5.5 Electrical Characteristics

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{CC}	Supply current (VCO output selected on both channels; RFOUTA enabled, RFOUTB disabled)	OUTA_PD = 0, OUTB_PD = 1 OUTA_MUX = 1 OUTA_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = f_{OUT} = 14.5GHz			460		mA
	Supply current (VCO output both RFOUTA and RFOUTB enabled)	OUTA_PD = 0, OUTB_PD = 0 OUTA_MUX = 1, OUTB_MUX = 1 OUTA_PWR = 7, OUTB_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = f_{OUT} = 14.5GHz			660		mA
	Supply current (channel divider selected on both channels; RFOUTA enabled, RFOUTB disabled)	OUTA_PD = 0, OUTB_PD = 1, OUTA_MUX = 0 OUTA_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = 15GHz, f_{OUT} = 7.5GHz			510		
	Supply current (channel divider both RFOUTA and RFOUTB enabled)	OUTA_PD = 0, OUTB_PD = 0 OUTA_MUX = 0, OUTB_MUX = 0, OUTA_PWR = 7, OUTB_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = 15GHz, f_{OUT} = 7.5GHz			685		
	Supply current (Doubler output selected on both channels; RFOUTA enabled, RFOUTB disabled)	OUTA_PD = 0, OUTB_PD = 1, OUTA_MUX = 2, OUTA_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = 12GHz, f_{OUT} = 24GHz			650		
	Supply current (Doubler output on both RFOUTA and RFOUTB enabled)	OUTA_PD = 0, OUTB_PD = 0 OUTA_MUX = 2, OUTB_MUX = 2, OUTA_PWR = 7, OUTB_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = 12GHz, f_{OUT} = 24GHz			730		
	Supply current (Doubler output on RFOUTA and CHDIV on RFOUTB enabled)	OUTA_PD = 0, OUTB_PD = 0 OUTA_MUX = 2, OUTB_MUX = 0, OUTA_PWR = 7, OUTB_PWR = 7, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = 12GHz f_{OUTA} = 24GHz, f_{OUTB} = 6GHz			810		
	Power on reset current	RESET = 1 (Device wake-up)			250		
	Power down current	POWERDOWN = 1			17		
OUTPUT CHARACTERISTICS							
Fout	RF output frequency			5		30000	MHz
P_{OUT}	Single-ended output power(2) (4)	OUTx_PWR = 7; Doubler output	f_{OUT} = 30GHz		1.2		dBm
	Differential output power(5)				4.2		
	Single-ended output power(2) (4)		f_{OUT} = 27GHz		2		
	Differential output power(5)				5		
	Single-ended output power(2) (4)		f_{OUT} = 24GHz		3.5		
	Differential output power(5)				6.5		
	Single-ended output power(2) (4)		f_{OUT} = 18GHz		2		
	Differential output power(5)				5		
	Single-ended output power(2) (4)	OUTx_PWR = 7; VCO output	f_{OUT} = 15GHz		2.5		
	Differential output power(5)				5.5		
	Single-ended output power(2) (4)		f_{OUT} = 7.5GHz		6		
	Differential output power(5)				9		
	Single-ended output power(2) (4)	OUTx_PWR = 7; Divider output	f_{OUT} = 4GHz		6.5		
	Differential output power(5)				9.5		

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3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$H_{1/2}$	1/2 Harmonic, single ended measurement	Measured at 12GHz frequency	F_{out} = 2 × F_{vco} = 24GHz		–55		dBc
	1/2 Harmonic, differential ended				–60		
	1/2 Harmonic, single ended measurement	Measured at 8GHz frequency	F_{out} = 2 × F_{vco} = 16GHz		–42		
	1/2 Harmonic, differential ended				–45		
$H_{3/2}$	3/2 Harmonic, single ended measurement	Measured at 24GHz frequency	F_{out} = 2 × F_{vco} = 16GHz		–45		
	3/2 Harmonic, differential ended measurement				–45		
P_{mute}	Single-ended output power leakage when output is muted	Fout = 24GHz			–40		dBm
	Single-ended output power leakage when output is muted	Fout = 12GHz			–55		
	Single-ended output power leakage when output is muted	Fout = 6GHz; RFoutA & RFoutB configured for CHDIV and both muted			–85		
	Single-ended output power leakage when output is muted	Fout = 6GHz; RFoutA & RFoutB configured for CHDIV; RFoutA muted; measured at RFoutA			–60		
t_{MUTE}	Mute enable time	Fout = 12GHz			200		ns
t_{UNMUTE}	Mute disable time	Fout = 12GHz			200		
isoCH	Channel to channel isolation (Doubler to VCO)	RFOUTA = 24GHz; RFOUTB = 12GHz			−39		dBc
	Channel to channel isolation (VCO to CH divider)	RFOUTA = 12GHz; RFOUTB = 6GHz			−53		
	Channel to channel isolation (Doubler to CH divider)	RFOUTA = 24GHz; RFOUTB = 6GHz			−41		
Phase Noise	RF Output Frequency Phase Noise	Fout = 24GHz	1kHz		−92.5		dBc/Hz
			10kHz		−102		
			100kHz		−104		
			1MHz		−112.5		
			10MHz		−138		
			100MHz		−150.7		
		Fout = 15GHz	1kHz		−97		
			10kHz		−105.5		
			100kHz		−107.5		
			1MHz		−115		
			10MHz		−140		
			100MHz		−156		
Jitter	RMS Jitter	Fout = 24GHz, f_{OSCin} = 100MHz, f_{PD} = 200MHz; Integration range 1kHz to 100MHz			54		fs
Skew	Skew between RFOUTA and RFOUTB	RFOUTA = RFOUTB = 16GHz			32		ps
		RFOUTA = RFOUTB = 8GHz			6		
		RFOUTA = RFOUTB = 4GHz			5		
INPUT SIGNAL PATH							
f_{OSCin}	Reference input frequency	OSC_2X = 0		5		1200	MHz
		OSC_2X = 1		5		200	
v_{OSCin}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50Ω resistor	f_{OSCin} ≥ 20MHz	0.4		2	V_{PP}
			10MHz ≤ f_{OSCin} < 20MHz	0.8		2	
			5MHz ≤ f_{OSCin} < 10MHz	1.6		2	
PHASE DETECTOR AND CHARGE PUMP							

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PD}	Phase detector frequency[1]	MASH_ORDER = 0	0.125		250	MHz
		MASH_ORDER > 0	5		200	MHz
I_{CPout}	Charge-pump leakage current	CPG = 0		15		nA
	Effective charge pump current. This is the sum of the up and down currents	CPG = 4		3		mA
		CPG = 1		6		
		CPG = 5		9		
		CPG = 3		12		
		CPG = 7		15		
$PN_{PLL_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100MHz, f_{VCO} = 12GHz[3]		–129		dBc/Hz
PN_{PLL_FOM}	Normalized PLL noise floor	f_{PD} = 100MHz, f_{VCO} = 12GHz[3]		–236		

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3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS							
f_{VCO}	VCO frequency			7500		15000	MHz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1GHz	100kHz		–106		dBc/Hz
			1MHz		–129		
			10MHz		–148		
			100MHz		–158		
		VCO2 f_{VCO} = 9.3GHz	100kHz		–104		
			1MHz		–126		
			10MHz		–143		
			100MHz		–157		
		VCO3 f_{VCO} = 10.4GHz	100kHz		–102		
			1MHz		–126		
			10MHz		–142		
			100MHz		–157		
		VCO4 f_{VCO} = 11.4GHz	100kHz		–99		
			1MHz		–124		
			10MHz		–145		
			100MHz		–156		
		VCO5 f_{VCO} = 12.5GHz	100kHz		–99		
			1MHz		–123		
			10MHz		–143		
			100MHz		–156		
		VCO6 f_{VCO} = 13.6GHz	100kHz		–98		
			1MHz		–122		
			10MHz		–142		
			100MHz		–157		
		VCO7 f_{VCO} = 14.7GHz	100kHz		–97		
			1MHz		–121		
			10MHz		–141		
			100MHz		–156		
t_{VCOCAL}	VCO calibration time	Switch across the entire frequency band; f_{OSC} = f_{PD} = 100MHz; No assist calibration			650		µs
$t_{LockTime}$	Lock time	Full Assist mode, Loop Bandwidth = 300KHz, PFD Frequency = 100MHz; RFOUTA from 9.5GHz to 9.52GHz, 1PPM settling around RFOUT; Double buffering enabled			16		µs
K_{VCO}	VCO Gain	8.1GHz			94		MHz/V
		9.3GHz			106		
		10.4GHz			122		
		11.4GHz			148		
		12.5GHz			185		
		13.6GHz			202		
		14.7GHz			233		
$\lvert\Delta T_{CL}\rvert$	Allowable temperature drift when VCO is not re-calibrated	Device configured in SPI mode			125		°C
H2	VCO second harmonic	f_{VCO} = 8GHz, divider disabled; Single-ended output			–30		dBc
H3	VCO third harmonic	f_{VCO} = 8GHz, divider disabled; Single-ended output			−14		

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C., OSCIN = 100MHz, SM Clock = 12.5MHz, Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DIGITAL INTERFACE (Applies to SCK, SDI, CSB, CAL, RECAL_EN, MUXout, SYNC, SysRefReq, REF_DBLR_EN, MuteX, OUTMUXx)							
V_{IH}	High-level input voltage			1.6			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current					100	µA
I_{IL}	Low-level input current			–100			µA
V_{OH}	High-level output voltage	MUXout pin	Load current = –5mA	V_{CC} – 0.6			V
V_{OL}	Low-level output voltage	MUXout pin	Load current = 5mA			0.6	V
$V_{SysRefCM}$	SYSREF Output Common mode voltage	OUTB_PWR = 7; V_{CC} = 3.3V; Differential 100 Ω load			2.1		V
V_{SysRef}	SYSREF Output Swing	OUTB_PWR = 7; V_{CC} = 3.3V; Differential 100 Ω load			1.2		V
f_{SysRef}	SYSREF Frequency range					187.5	MHz
$f_{SysRefDly}$	SYSREF delay step size	$f_{Interpolator}$ = 800MHz			9		ps
VL	CDIV0, CDIV1, CDIV2 Voltage levels			0		0.4	V
VML	CDIV0, CDIV1, CDIV2 Voltage levels			0.8	V_{CC}/3	1.4	V
VMH	CDIV0, CDIV1, CDIV2 Voltage levels			1.9	2×V_{CC}/3	2.5	V
VH	CDIV0, CDIV1, CDIV2 Voltage levels			3	V_{CC}	3.45	V
VL	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels			0		0.4	V
VML	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels			0.8	V_{CC}/3	1.4	V
VMH	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels			1.9	2×V_{CC}/3	2.5	V
VH	NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5 Voltage levels			3	V_{CC}	3.45	V

(1) For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.
(2) Single-ended output power at device pin. Trace losses are de-embedded. Unused port terminated to 50Ω load.
(3) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20× log(Fvco/Fpd) + 10 × log(Fpd / 1Hz). PLL_flicker (offset) = PLL_1/f + 20 × log(Fvco / 1GHz) – 10× log(offset / 10kHz). After these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 × log($10^{PLL_Flat / 10} + 10^{PLL_flicker / 10}$)
(4) Output power, spurs, and harmonics can vary based on board layout and components.
(5) Differential output power measured with external Balun. Balun and Trace losses are de-embedded.

5.6 Timing Requirements

(3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C, except as specified. Nominal values are at V_{CC} = 3.3V, T_C = 25°C)

PARAMETERS			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE WRITE SPECIFICATIONS						
f_{SPI}Write	SPI write speed				40	MHz
t_{CE}	Clock to enable low time	See Timing Diagram	2.5			ns
t_{CS}	Data to clock setup time	See Timing Diagram	8.6			ns
t_{CH}	Data to clock hold time	See Timing Diagram	0.6			ns
t_{CWH}	Clock pulse width high	See Timing Diagram	10			ns
t_{CWL}	Clock pulse width low	See Timing Diagram	10			ns
t_{CES}	Enable to clock setup time	See Timing Diagram	6.5			ns
t_{EWH}	Enable pulse width high	See Timing Diagram	5			ns
DIGITAL INTERFACE READBACK SPECIFICATIONS						
f_{SPI}Readback	SPI readback speed				40	MHz

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(3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C, except as specified. Nominal values are at V_{CC} = 3.3V, T_C = 25°C)

PARAMETERS			MIN	NOM	MAX	UNIT
t_{CE}	Clock to enable low time	See Timing Diagram	2.5			ns
t_{CS}	Clock to data wait time		8.6			ns
t_{CWH}	Clock pulse width high		10			ns
t_{CWL}	Clock pulse width low		10			ns
t_{CES}	Enable to clock setup time		6.5			ns
t_{EWH}	Enable pulse width high		5			ns
t_{CD}	Falling clock edge to data wait time				10	ns
SYNC and SYSREFREQ						
t_{SETUP}	SYNC pin to OSCin setup time		2.5			ns
t_{HOLD}	SYNC pin to OSCin hold time		2.5			ns

5.7 Timing Diagrams

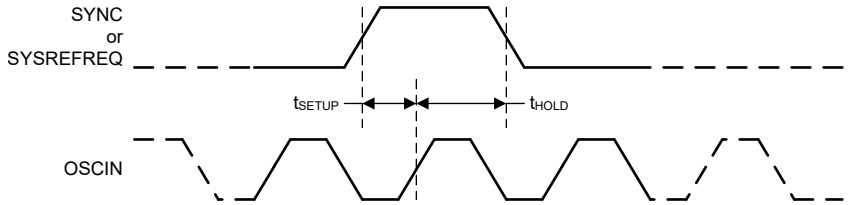

Figure 5-1. Trigger Signals Timing Diagram

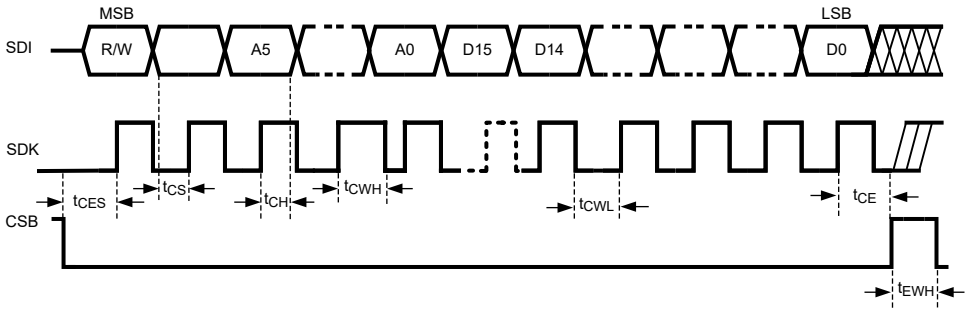

Figure 5-2. Serial Data Input Timing Diagram

LMX2624-SP supports SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=01 CPHA=1).

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin. On the rising edge of the 24th clock cycle, the data is transferred from the data field into the selected register bank.
- The CSB must be held low for data to be clocked. Device is ignore clock pulses if CSB is held high.
- If the MUXOUT pin is configured as SPI SDO, the MUXOUT pin is tristated during all write transactions and when CSB is high.
- When SCK and SDI lines are shared between devices, TI recommends hold the CSB line high on the device that is not to be clocked.

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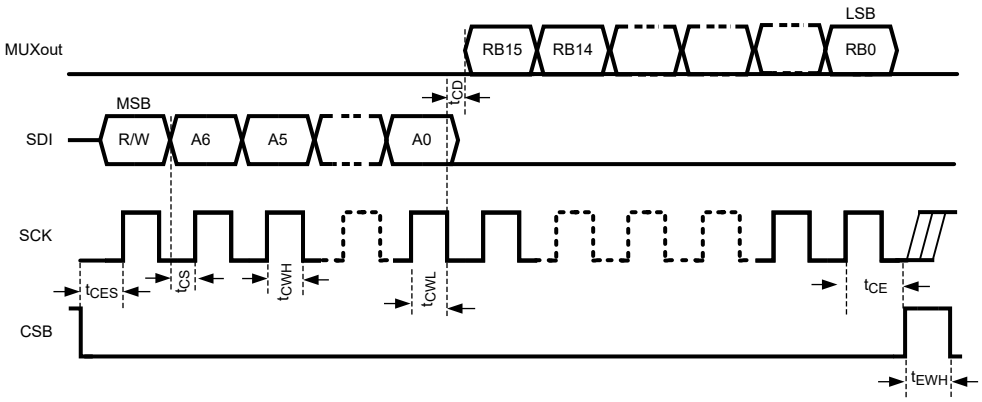

Figure 5-3. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXout pin is tristated for the address portion of the transaction, and when the CSB pin is high.
- The data on MUXout becomes available momentarily after the falling edge of SCK and therefore must be read back on the rising edge of SCK.
- The data portion of the transition on the SDI line is always ignored.

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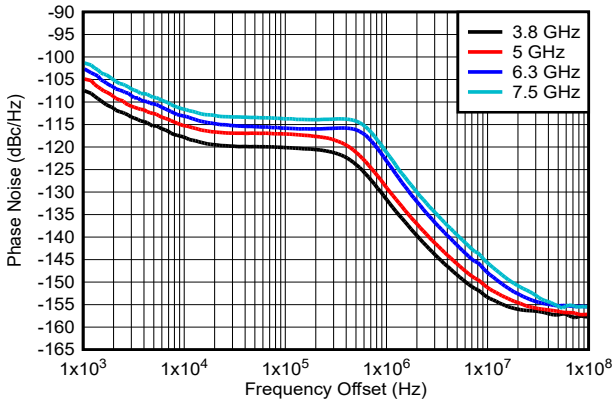
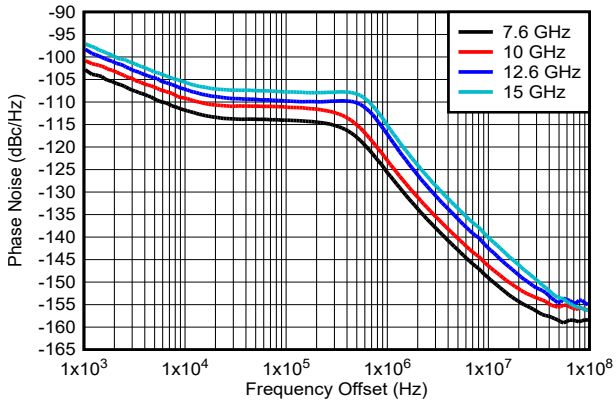
5.8 Typical Characteristics

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



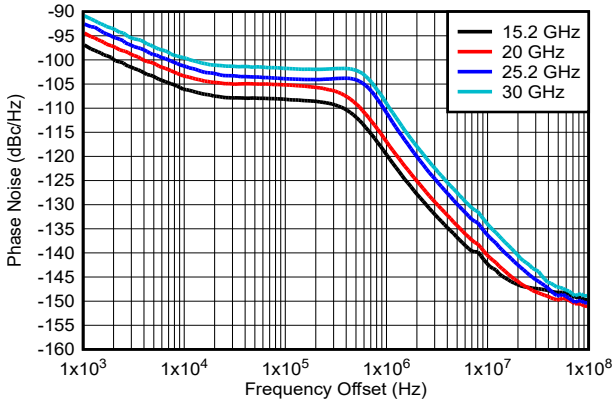
f_{OSC} = 100MHz, f_{PD} = 200MHz, Channel Divider Value: 2

Figure 5-4. Closed-Loop Phase Noise at Channel Divider Frequency Range



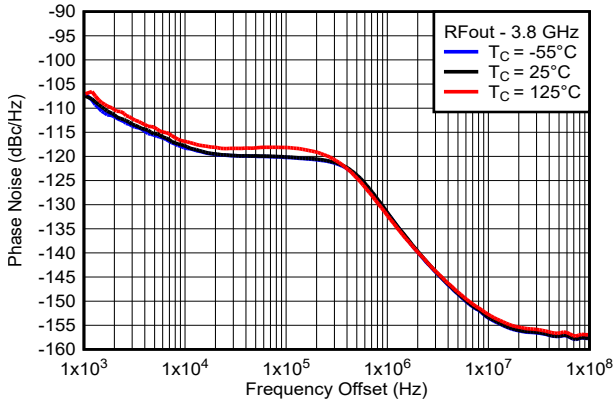
f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-5. Closed-Loop Phase Noise at VCO Frequency Range



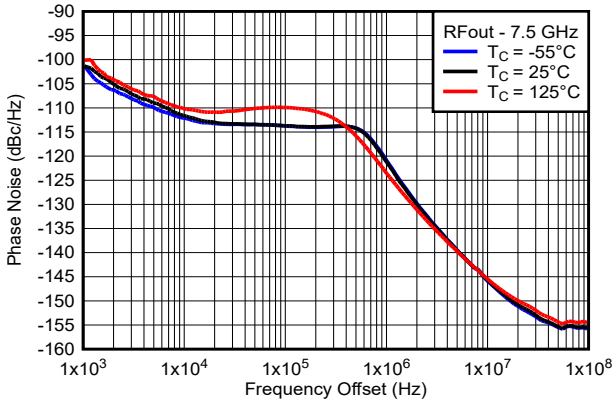
f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-6. Closed-Loop Phase Noise at Doubler Frequency Range



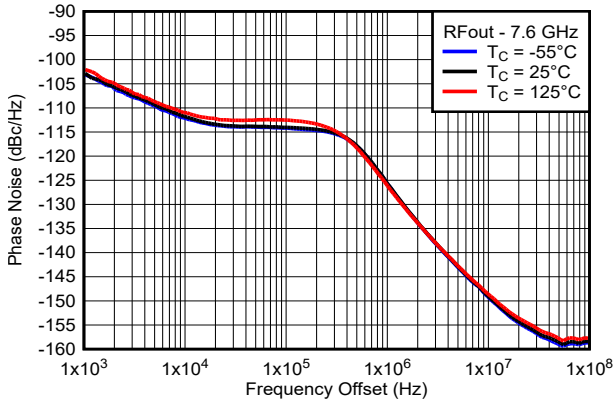
f_{OSC} = 100MHz, f_{PD} = 200MHz, Channel Divider Value: 2

Figure 5-7. Closed-Loop Phase Noise at 3.8GHz



f_{OSC} = 100MHz, f_{PD} = 200MHz, Channel Divider Value: 2

Figure 5-8. Closed-Loop Phase Noise at 7.5GHz

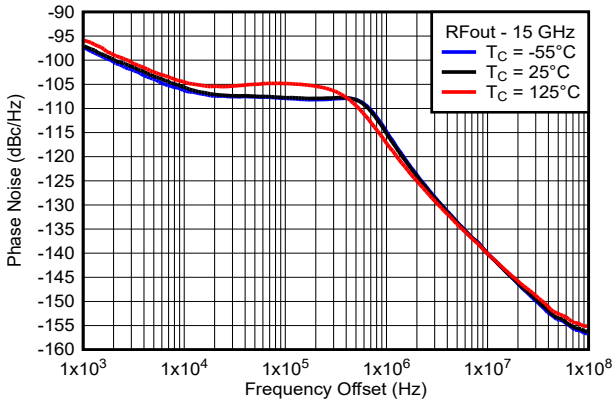


f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-9. Closed-Loop Phase Noise at 7.6GHz

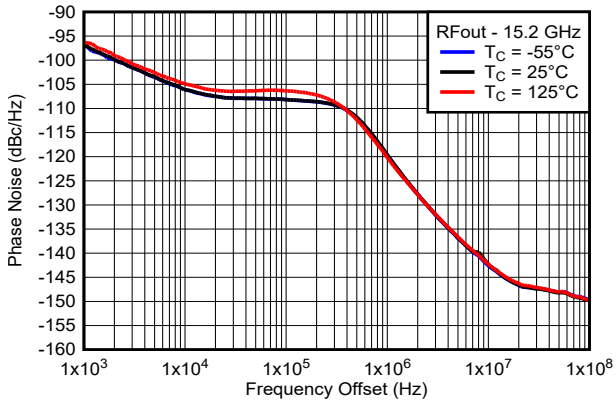
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



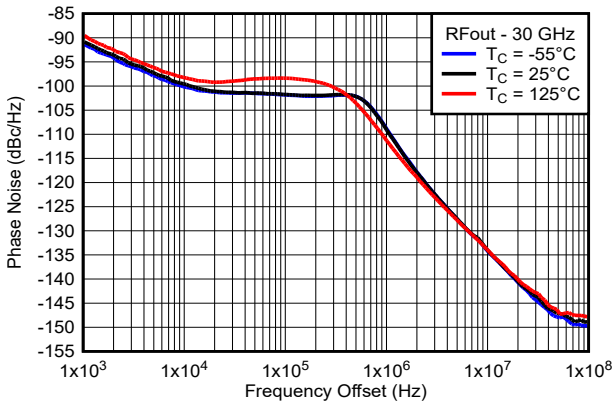
f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-10. Closed-Loop Phase Noise at 15GHz



f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-11. Closed-Loop Phase Noise at 15.2GHz (Doubler Range)



f_{OSC} = 100MHz, f_{PD} = 200MHz

Figure 5-12. Closed-Loop Phase Noise at 30GHz (Doubler Range)

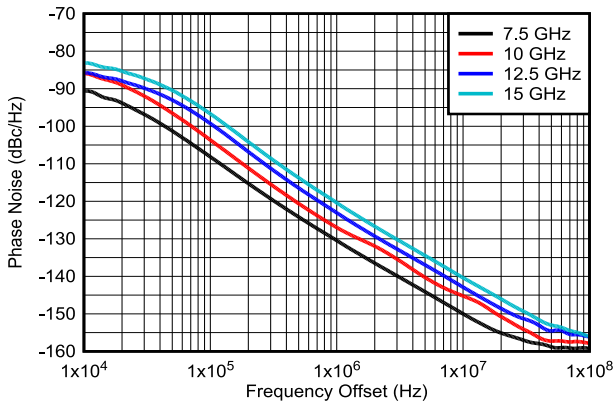


Figure 5-13. Open-Loop VCO Phase Noise

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5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.

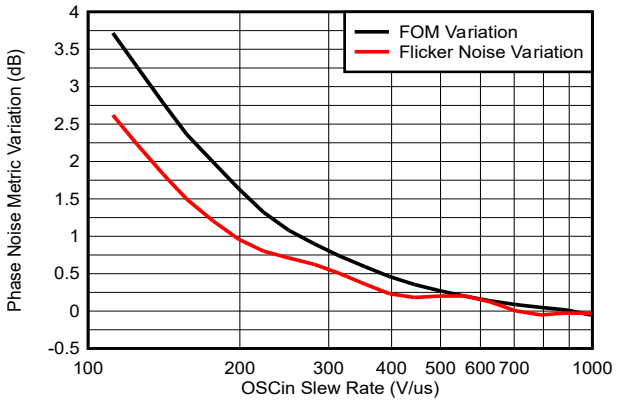
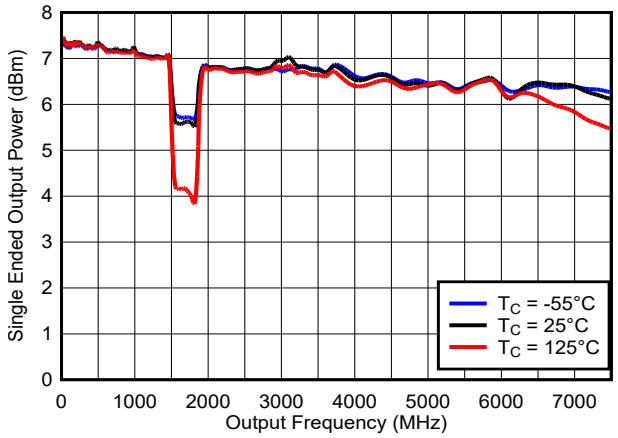


Figure 5-14. PLL Noise Metric Variation vs. OSCin Slew Rate



Power dip at divider value 6 due to not 50% duty cycle output.

Figure 5-15. Output Power vs. Temperature in Channel Divider Frequency Range

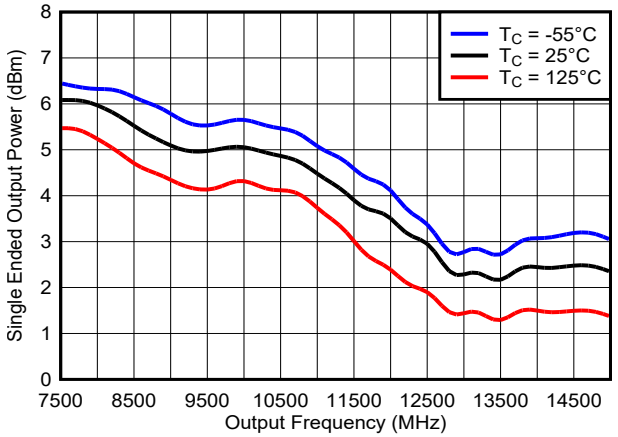


Figure 5-16. Output Power vs. Temperature in VCO Frequency Range

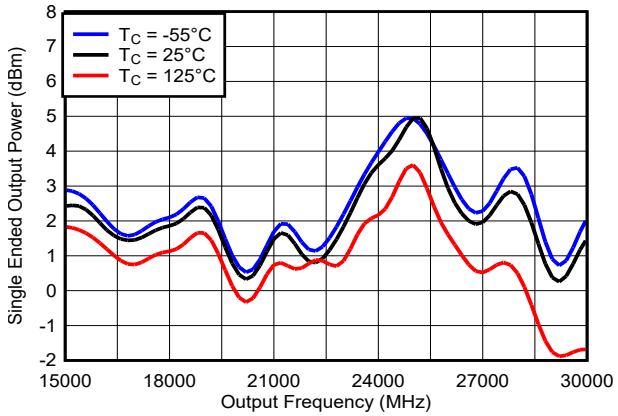


Figure 5-17. Output Power vs. Temperature in Doubler Frequency Range

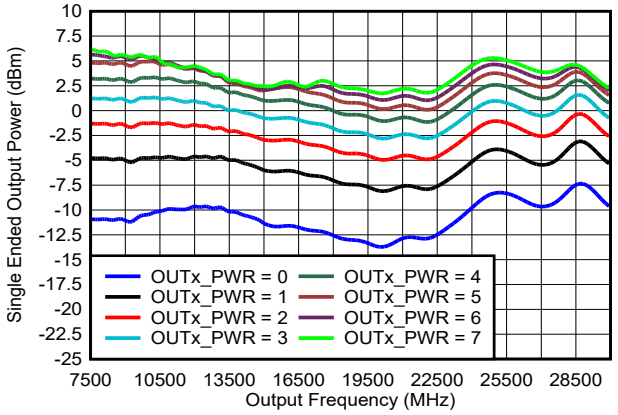


Figure 5-18. Output Power vs OUTx_PWR

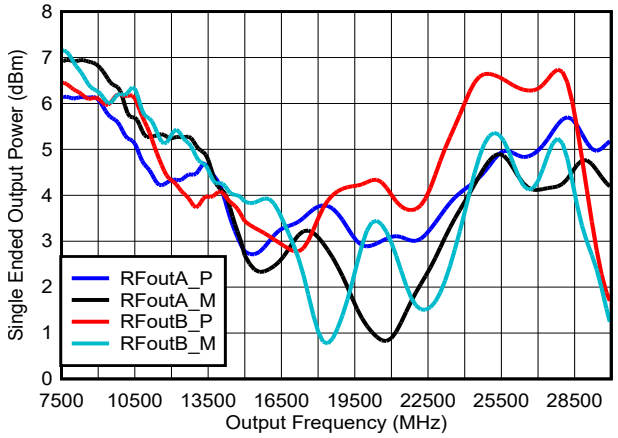
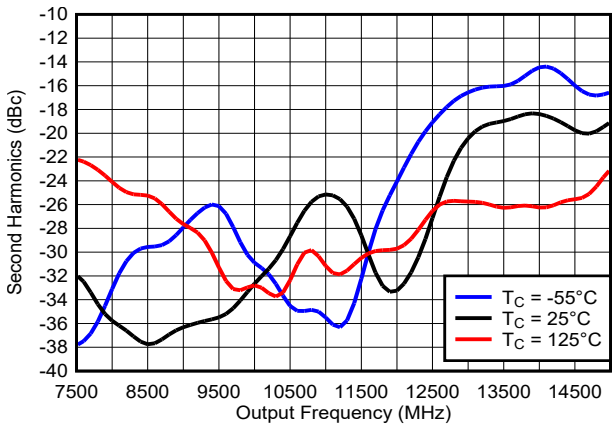


Figure 5-19. Each RFout Pin Output Power

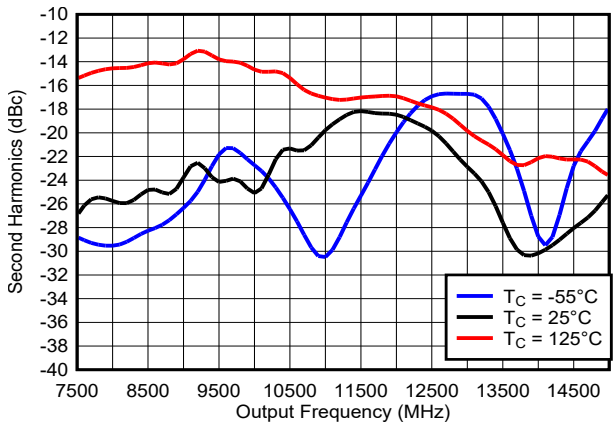
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



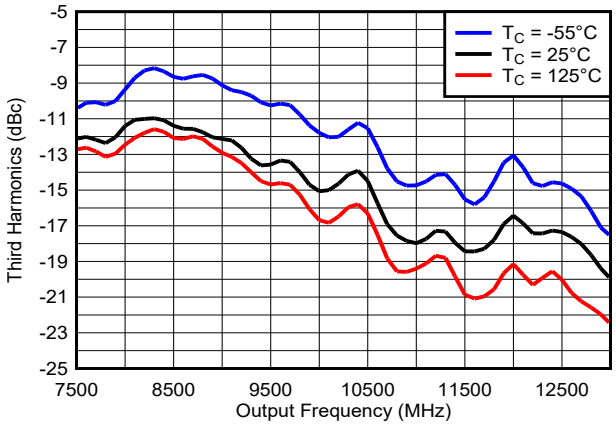
Single-Ended Output at RFoutx_P

Figure 5-20. Second Harmonics in VCO Frequency Range



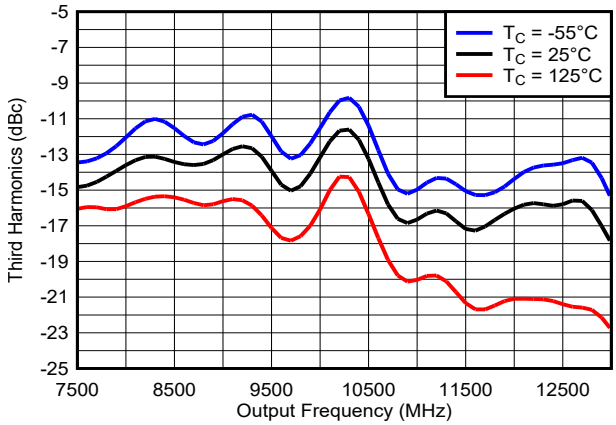
Single-Ended Output at RFoutx_M

Figure 5-21. Second Harmonics in VCO Frequency Range



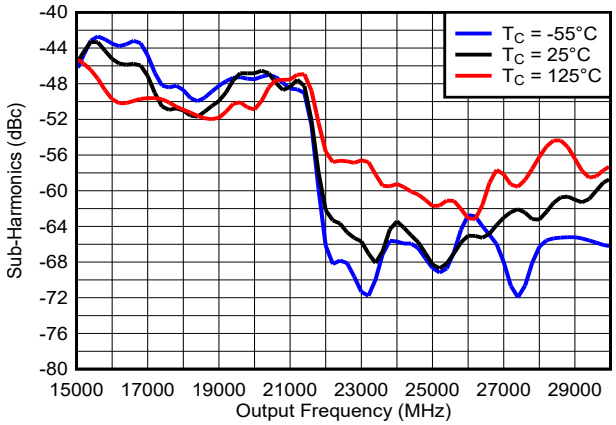
Differential Output

Figure 5-22. Third Harmonics in VCO Frequency Range



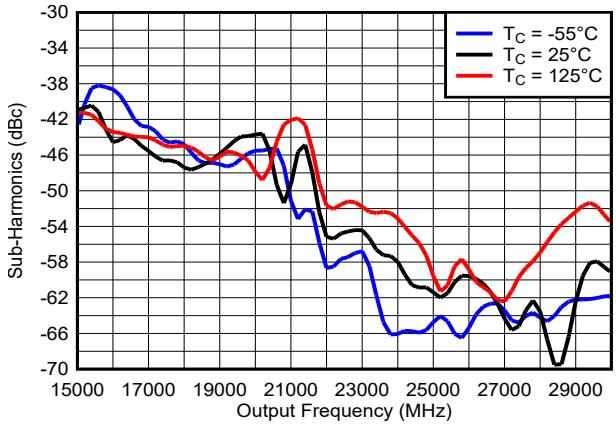
Single-Ended Output

Figure 5-23. Third Harmonics in VCO Frequency Range



Differential Output

Figure 5-24. Sub-Harmonics in Doubler Frequency Range



Single-Ended Output

Figure 5-25. Sub-Harmonics in Doubler Frequency Range

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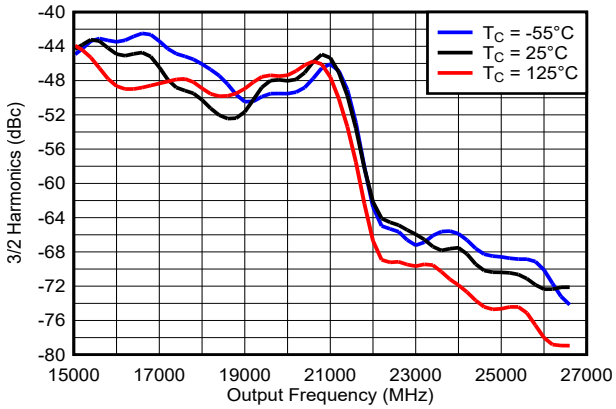
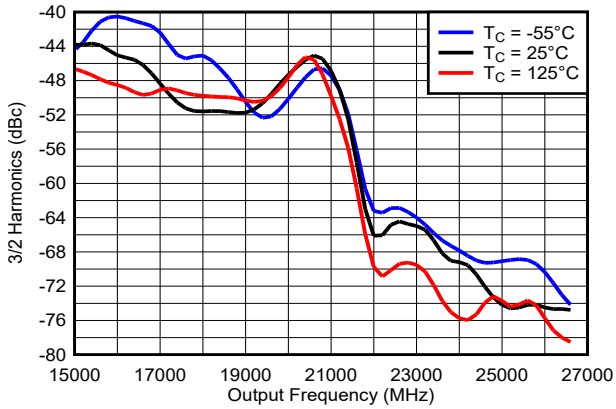
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



Differential Output

Figure 5-26. 3/2 Harmonics in Doubler Frequency Range



Single-Ended Output

Figure 5-27. 3/2 Harmonics in Doubler Frequency Range

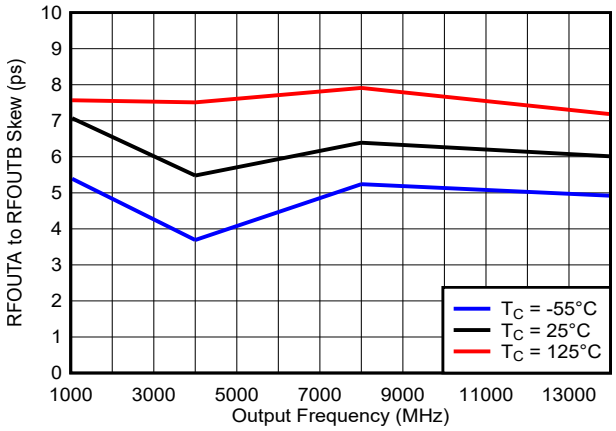
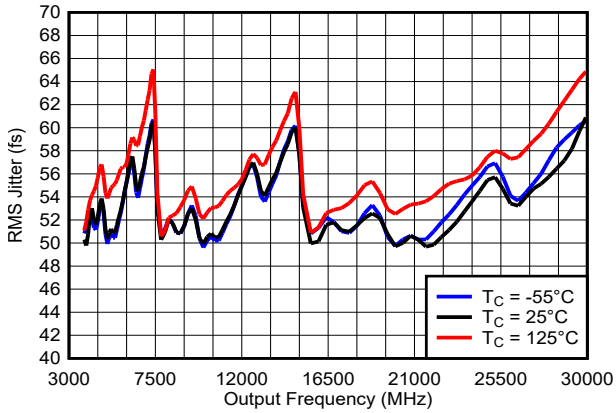
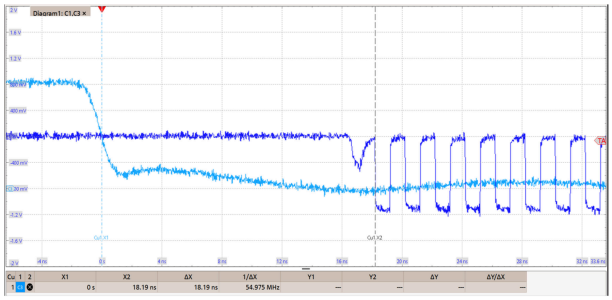


Figure 5-28. Channel to Channel Skew



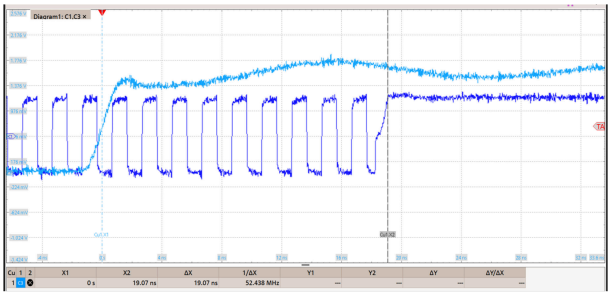
Integration Range is 1k-100MHz

Figure 5-29. Integrated Jitter (Jitter (fs) Vs Output Frequency (MHz)



SM Clock = 50MHz

Figure 5-30. Mute Pin Output Enable Time

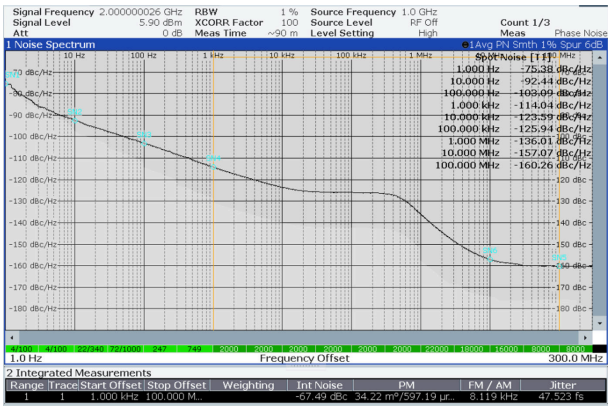


SM Clock = 50MHz

Figure 5-31. Mute Pin Output Disable Time

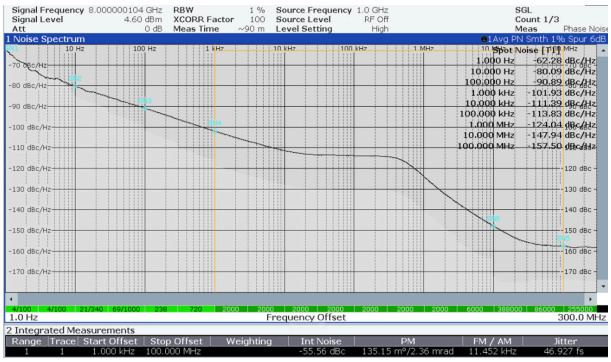
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



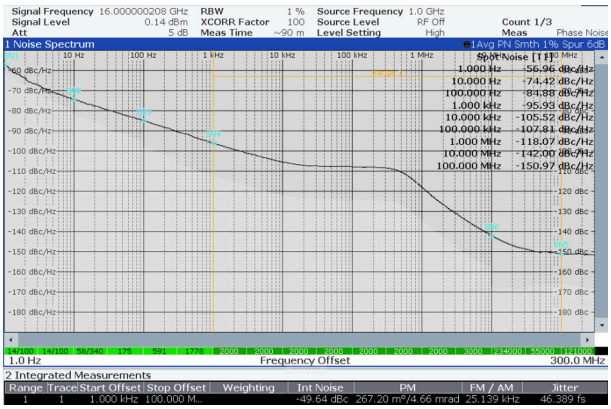
Single-Ended Output; f_{OSC} = 100MHz, f_{PD} = 200MHz, Loop Filter BW = 400kHz

Figure 5-32. Phase Noise Plot (2GHz)



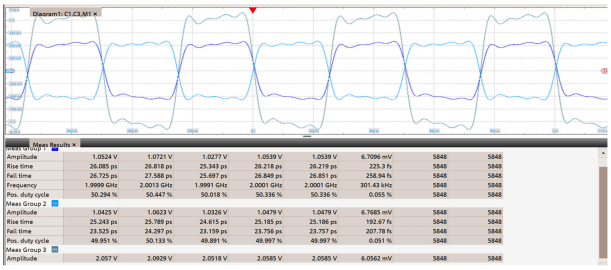
Single-Ended Output; f_{OSC} = 100MHz, f_{PD} = 200MHz, Loop Filter BW = 400kHz

Figure 5-33. Phase Noise Plot (8GHz)



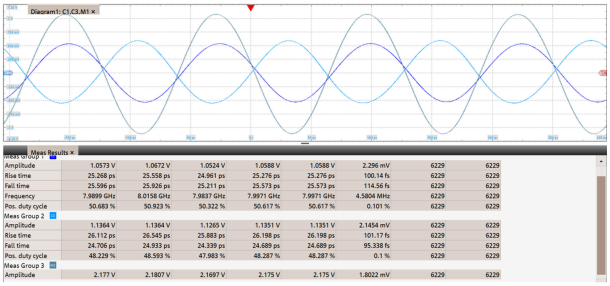
Single-Ended Output; f_{OSC} = 100MHz, f_{PD} = 200MHz, Loop Filter BW = 400kHz

Figure 5-34. Phase Noise Plot (16GHz)



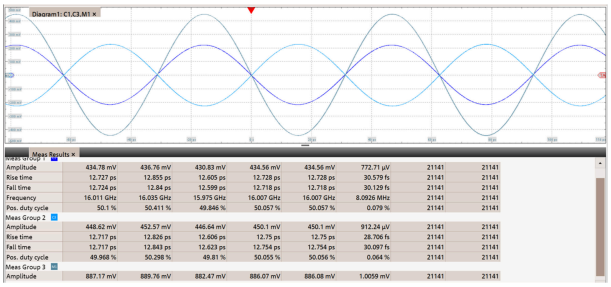
C1 : RFOUTAP; C3 : RFOUTAM; M1 : RFOUTAP - RFOUTAM (Differential)

Figure 5-35. Differential Output waveform in time domain (2GHz)



C1 : RFOUTAP; C3 : RFOUTAM; M1 : RFOUTAP - RFOUTAM (Differential)

Figure 5-36. Differential Output waveform in time domain (8GHz)



C1 : RFOUTAP; C3 : RFOUTAM; M1 : RFOUTAP - RFOUTAM (Differential)

Figure 5-37. Differential Output waveform in time domain (16GHz)

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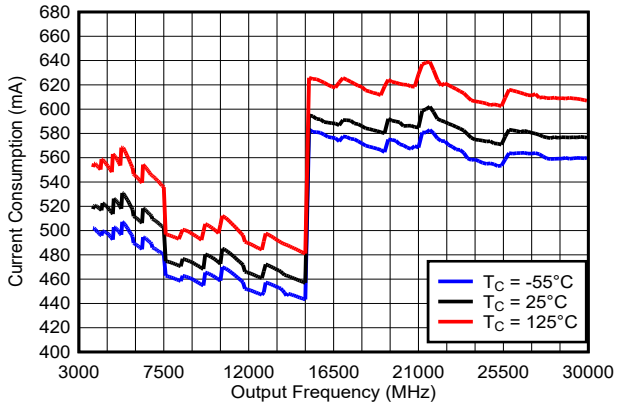
5.8 Typical Characteristics (continued)

Unless stated otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 3.3V, OUTx_PWR=7, OSCIN_P driven single ended with 10dBm at pin.



Single channel enabled

Figure 5-38. Current Consumption vs Output Frequency

6 Detailed Description

6.1 Overview

The LMX2624-SP is a high-performance, wideband frequency synthesizer with integrated VCO, output doubler and output divider. The VCO operates from 7500 to 15000MHz and this can be combined with the output divider and doubler to produce any frequency in the range of 5MHz to 30GHz.

The PLL is fractional-N PLL with programmable delta-sigma modulator up to 3rd order. The fractional denominator is a programmable 32-bit long, which can provide fine frequency steps easily below 1Hz resolution as well as be used to do exact fractions like 1/3, 7/1000, and many others.

The phase detector frequency goes up to 200MHz in fractional mode and 250MHz in integer mode, although minimum N-divider values must also be taken into account. For applications where deterministic phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic.

The ultra-fast VCO calibration is designed for applications where the frequency must be swept or abruptly changed. The device has both Pin-mode and SPI-mode options where the frequency can be configured manually using general purpose inputs or programmed using SPI.

The JESD204B/C support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

The LMX2624-SP device requires only a single 3.3V power supply. The internal power supplies are provided by high performance external LDOs.

Table 6-1 shows the range of several of the doubler, dividers, and fractional settings.

Table 6-1. Range of Doubler, Divider, and Fractional Settings

PARAMETER	FIELD	MIN	MAX	COMMENTS
OSCin doubler	OSC_2X	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	PLL_R_PRE	1 (bypass)	128	Only use the Pre-R divider if the input frequency is too high for the Post-R divider.
Post-R divider	PLL_R	1 (bypass)	255	The maximum input frequency for the post-R divider is 250MHz. Use the Pre-R divider if necessary.
N divider	PLL_N	≥ 29	$2^{19} – 1 = 524287$	The minimum divide depends on modulator order and VCO frequency. See *Section 6.3.5* for more details.
Fractional numerator	PLL_NUM	0 (Integer mode)	$2^{32} – 2 = 4294967294$	The fractional numerator is programmable. This numerator is ignored when fractional order = integer mode.
Fractional denominator	PLL_DEN	1	$2^{32} – 1 = 4294967295$	The fractional denominator is programmable and can assume any value between 1 and $2^{32} – 1$; the denominator is not a fixed value.
Fractional order	MASH_ORDER	0	3	Order 0 is integer mode and the order can be programmed
Channel divider	CHDIV	1 (bypass)	1536	This is the series of several dividers. Also, be aware that above 12GHz, the maximum allowable channel divider value is 4.
Output frequency		5MHz	30GHz	Below 7.5GHz, Channel Divider is used. 7.5GHz to 15GHz is from VCO. 15GHz to 30GHz is from VCO along with output doubler

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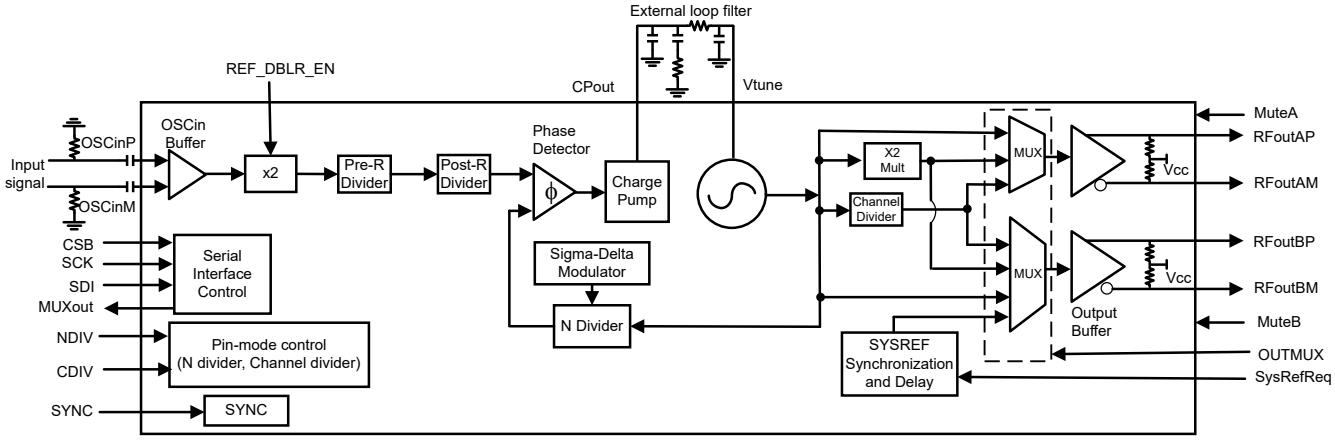
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling capacitors at the pin. The OSCin pins can be driven single-ended with a CMOS clock or XO. Differential clock input is also supported, making interfacing with high-performance system clock devices such as TI's LMK series clock devices simpler. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN = 1 or toggling CAL pin in pin mode.

6.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, and a Post-R divider.

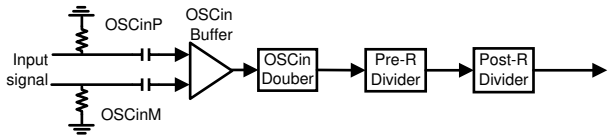


Figure 6-1. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. This doubler adds minimal noise and is useful for increasing the Phase Detector frequency and also to avoid spurs. When the phase detector frequency is increased, the flat portion of the PLL phase noise improves. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down. The phase detector frequency, f_{PD}, is calculated in Equation 1

$$f_{PD} = f_{OSC} \times OSC_2X / (PLL_R_PRE \times PLL_R) \quad (1)$$

6.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency while adding minimal noise. In some situations using the doubler can be advantageous to go to a higher frequency than the maximum phase detector frequency because the Pre-R divider is able to divide down this frequency to phase detector frequency that is advantageous for fractional spurs.

- If the OSCin doubler is used, the OSCin signal must have around 50% duty cycle as both the rising and falling edges are used. Otherwise the spurs are high.
- If the OSCin doubler is not used, only rising edges of the OSCin signal are used and duty cycle is not critical.

6.3.2.2 Pre-R Divider (PLL_R_PRE)

The pre-R divider is useful for reducing the input frequency to help meet the maximum 250MHz input frequency limitation to the PLL_R divider. Otherwise, the pre-divider does not have to be used.

6.3.2.3 Post-R Divider (PLL_R)

The post-R divider can be used to further divide down the frequency to the phase detector frequency. When the divider is used (PLL_R > 1), the input frequency to this divider is limited to 250MHz.

6.3.3 State Machine Clock

The state machine clock (SM clock) is a divided down version of the OSCin signal that is used internally in the device. This divide value 1, 2, 4, 8, or 16 and is determined by CAL_CLK_DIV programming word (described in the programming section). The device support max. state machine clock frequency up to 50MHz. This state machine clock impacts VCO calibration. The state machine clock is calculated as $f_{SM} = f_{OSC} / 2^{CAL_CLK_DIV}$.

6.3.4 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL.

6.3.5 N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The integer portion of N is the whole part of the N divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N divider value is determined by PLL_N + PLL_NUM / PLL_DEN. The PLL_N, PLL_NUM and PLL_DEN are software programmable in SPI mode. Pin-mode option has integer frequency generation and refer Pin-mode description details in Pin-mode section for more details.

The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200MHz, the output can increment in steps of 200MHz /(2^{32} – 1) = 0.047Hz. Equation 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an IncludedDivide divider that is shown in Equation 2.

$$f_{VCO} = f_{pd} \times \text{IncludedDivide} \times \left(N + \frac{NUM}{DEN}\right) \quad (2)$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to third order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY bit must be programmed in accordance to the Table 6-2. In SYNC mode, IncludedDivide can be larger than one, otherwise IncludedDivide is one.

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Table 6-2. Minimum N Divider Restrictions

MASH_ORDER	f_{VCO} / IncludedDivide (MHz)	MINIMUM N	PFD_DLY
0	≤ 12500	29	1
	> 12500	33	2
1	≤ 10000	30	1
	10000 – 12500	34	2
	>12500	38	3
2	≤ 4000	31	1
	7500 – 10000	33	2
	>10000	37	3
3	≤ 4000	33	1
	7500 – 10000	41	3
	>10000	45	4

6.3.6 MUXout Pin

The MUXout pin can be configured as lock detect indicator for the PLL, as serial data output (SDO) for the SPI to readback registers, and as copies of the R-port and N-port signals of the phase detector f_{PD}, and as a copy of the state machine clock f_{SM} at MUXout pin. MUXout Pin Configurations shows the MUXOUT pin configuration for Pin mode and SPI mode. Field MUXOUT can be configured as different functions.

Table 6-3. MUXout Pin Configurations

MODE of operation	MUXOUT	MUXOUT pin	FUNCTION
Pin-mode	X	Lock Detect	Lock detect indicator for PLL
SPI-mode	0	Lock Detect	Lock detect indicator for PLL
SPI-mode	1 (default)	Register read back	Outputs register read back data
SPI-mode	> 1	Diagnostics	Look at the R22 register

6.3.6.1 Serial Data Output for Readback

In SPI mode, MUXout pin has a couple of options. When MUXOUT is set to register read back output, MUXout pin is automatically tristate when there is no output data. Details of this pin operation are described with the Timing Diagrams. Readback is useful when a device is used is full assist mode and VCO calibration data are retrieve and saved for future use. Readback can also be used to read back the lock detect status using the field rb_LD_VTUNE(register R35[5:4]).

6.3.6.2 Lock Detect Indicator Set as Type “VCOcal” or "Vtune and VCOcal"

When lock detect indicator is selected, there are two types of indicator and the indicators can be selected with the field LD_TYPE (register R1[12]). The first indicator is called “VCOCal” (LD_TYPE=0) and the second indicator is called “Vtune and VCOCal” (LD_TYPE=1).

In “VCOcal” mode the MUXout pin is asserted HIGH after a VCO calibration is completed (no matter if the calibration is successful or not) and the lock detect delay timer is time out. During a VCO calibration and before the lock delay timer is time out, MUXout pin is LOW. The programmable lock detect timer (LD_DLY, register R23[15:0]) adds an additional delay after the VCO calibration finishes before the lock detect indicator is asserted high. LD_DLY is a 16 bit unsigned quantity that corresponds to 4 times the number of state machine clock cycles. For example, given f_{OSC} = 100MHz, CAL_CLK_DIV = 1, then state machine clock frequency = f_{OSC} / $2^{CAL_CLK_DIV}$ = 50MHz. If LD_DLY = 1000, the delay time is equal to 80µs. MUXout pin remains in the current state no matter if the PLL is actually locked or not. In other words, if the PLL goes out of lock or the input

reference goes away when the current state is high, then the current state remains high. This lock detect setting is useful for measuring VCO calibration time.

In "Vtune and VCOcal" mode the MUXout pin is high when the VCO calibration has finished, the lock detect delay timer is finished running, and the PLL is locked. This indicator can remain in the current state (high or low) if the OSCin signal is lost. The true status of the indicator is updated and resume operation only when a valid input reference to the OSCin pin is returned. An alternative method to monitor the OSCin of the PLL is recommended. This indicator is reliable as long as the reference to OSCin is present.

Since both types of lock detect indicator requires a completion of VCO calibration, at least one VCO calibration has to be performed in full assist mode, otherwise the lock detector does not work.

6.3.7 VCO (Voltage-Controlled Oscillator)

The LMX2624-SP includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies as shown in Equation 2.

6.3.7.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7500MHz to 15000MHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1 or toggle CAL pin from low-to-high in Pin-mode. A valid OSCin signal must be present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation can result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, temperature of 125°C means the device never loses lock if the device is operated within this range.

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The LMX2624-SP allows the user to assist the VCO calibration. In general, there are three kinds of assistance, as shown in Table 6-4. Refer to the application note for detailed implementation procedures and performance demonstrations of VCO calibration technique showcased for commercial devices. When performing the readback for VCO parameters including VCO doubler in full assist mode, confirm that bit R1[13] is set to 1.

Table 6-4. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	VCO_SEL	VCO_SEL_FORCE VCO_CAPCTRL_FORCE VCO_DACISET_FORCE	VCO_CAPCTRL VCO_DACISET
No assist	User does nothing to improve VCO calibration speed.	7	0	Don't Care
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting VCO_SEL	Select by table	0	Don't Care
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), frequency band (VCO_CAPCTRL), VCO doubler parameters and manually sets the value. If the two frequency points are no more than 5MHz apart and on the same VCO core, the user can set the VCO amplitude and capcode for any frequency between those two points using linear interpolation	Select by readback	1	Select by readback

For the no assist method, just set VCO_SEL=7 and this is done. For partial assist, the VCO calibration speed can be improved by changing the VCO_SEL bit according to the frequency. Note that the frequency is not the actual VCO core range, but favors selecting the VCO. This is not only optimal for VCO calibration speed, but required for reliable locking.

Table 6-5. Minimum VCO_SEL for Partial Assist

f_{VCO}	VCO CORE (MIN)
7500 - 8600MHz	VCO1
8600 - 9900MHz	VCO2
9900 - 10800MHz	VCO3
10800 -11900MHz	VCO4
11900 - 13000MHz	VCO5
13000 - 14000MHz	VCO6
14000 - 15000MHz	VCO7

For fastest calibration time, use the minimum VCO core as recommended in the previous table. Table 6-6 shows typical VCO calibration times with or without analog lock time for this choice in bold as well as showing how long the calibration time is increased if a higher than necessary VCO core is chosen. Realize that these calibration times are specific to these f_{OSC} and f_{PD} conditions specified and at the boundary of two cores, sometimes the calibration time can be increased.

Table 6-6. Typical Calibration Times (µs) Without Analog Lock Time for f_{OSC} = 100MHz, f_{PD} = 200MHz and f_{SM} = 50MHz

f_{VCO}	VCO_SEL						
	VCO7	VCO6	VCO5	VCO4	VCO3	VCO2	VCO1
8.1GHz	650	614	620	376	256	243	**191**
9.3GHz	606	589	587	335	196	**177**	Invalid
10.4GHz	598	579	570	338	**177**	Invalid	
11.4GHz	543	540	530	**284**	Invalid		
12.5GHz	396	346	**300**	Invalid			
13.6GHz	262	**218**	Invalid				
14.7GHz	**164**	Invalid					

Table 6-7. Typical Calibration Times (µs) With Analog Lock Time for f_{OSC} = 100MHz, f_{PD} = 200MHz and f_{SM} = 50MHz

f_{VCO}	VCO_SEL[(1)]						
	VCO7	VCO6	VCO5	VCO4	VCO3	VCO2	VCO1
8.1GHz	854	828	822	579	451	437	**393**
9.3GHz	819	800	794	551	401	**380**	Invalid
10.4GHz	808	786	781	551	**388**	Invalid	
11.4GHz	767	745	743	**494**	Invalid		
12.5GHz	603	560	**513**	Invalid			
13.6GHz	469	**426**	Invalid				
14.7GHz	**385**	Invalid					

(1) This include Analog lock time for typical loop bandwidth (300kHz).

6.3.7.2 Determining the VCO Gain

The VCO gain can vary based on core, and this can vary over temperature and process. Table 6-8 provides a rough guideline of expected VCO gain values based on the VCO core.

Based in this table, the VCO gain can be estimated for an arbitrary VCO frequency of f_{VCO} as Equation 3:

$$Kvco = Kvco1 + (Kvco2-Kvco1) \times (f_{VCO} – f1) / (f2 – f1) \quad (3)$$

Table 6-8. VCO Gain

f_1	f_2	$Kvco_1$	$Kvco_2$
7500	8600	73	112

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Table 6-8. VCO Gain (continued)

f_1	f_2	$Kvco_1$	$Kvco_2$
8600	9900	84	136
9900	10800	102	140
10800	11900	115	162
11900	13000	167	224
13000	14000	182	228
14000	15000	218	254

6.3.7.3 Double Buffering (Shadow Registers)

Double buffering—also known as "shadow registers"—allows the user to program multiple registers without having them actually take effect. When the R0 register is programmed, then these registers take effect. This is especially useful if one wants to change frequencies quickly and multiple register writes are required. When DBL_BUF_EN = 1, the double buffering is enabled for the registers related to VCO, Doubler, PLL, Output MUX and Channel Divider. More details on the registers are available in Register map section.

6.3.7.4 Watchdog Feature

The watchdog feature helps handle situations where radiation can interrupt or cause the VCO calibration to fail. When this feature is turned on, a timer runs in the background while VCO calibration is happening. If the calibration does not finish before the timer runs out, the calibration is automatically restarted. The WD_CNTRL word controls how many times the watchdog is allowed to restart the calibration.

6.3.7.5 RECAL Feature

The RECAL feature is used to mitigate the scenario when the VCO is in lock, but then radiation causes the VCO to go out of lock. When the RECAL_EN pin is high, if the PLL loses lock and stays out of lock for a time specified by the WD_DLY word, then RECAL triggers a VCO re-calibration. Lock detector must be set to "Vtune and VCOCal" (LD_TYPE = 1) and the lock detect timer (LD_DLY) must be non-zero. Suggested minimum lock detector timer delay time is 200µs for LD_DLY = 2500 (default) and 50MHz state machine clock frequency.

6.3.8 Channel Divider

To go below the VCO lower bound of 7500MHz, the channel divider can be used. The channel divider utilizes three stages with a total division ratio equal to the product of the three dividers. Therefore, not all values are valid.

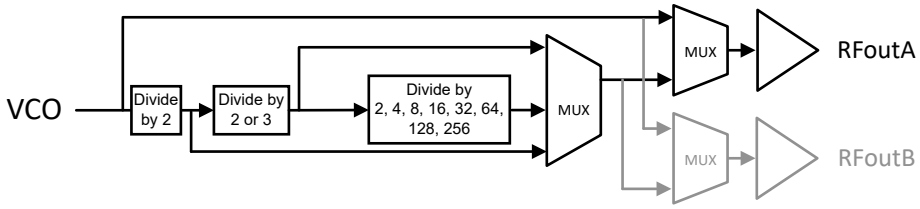

Figure 6-2. Channel Divider

Please note that, channel divider in by 6 (÷ 6) setting, the duty cycle is not 50%.

When the channel divider is used, there are limitations on the values. Table 6-9 shows how these values are implemented.

Table 6-9. Channel Divider Segments

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]
2	None	3750	7500	1
4		1875	3750	2
6	f_{VCO} ≤ 12GHz	1250	2000	3
8		937.5	1500	4
12		625	1000	5
16		468.75	750	6
24		312.5	500	7
32		234.375	375	8
48		156.25	250	9
64		117.1875	187.5	10
96		78.125	125	11
128		58.59375	93.75	12
192		39.0625	62.5	13
256		29.296875	46.875	14
384		19.53125	31.25	15
512		14.6484375	23.4375	16
768		9.765625	15.625	17
1024		7.32421875	11.71875	18
1536		4.8828125	7.8125	19

The channel divider is powered up whenever an output (OUTx_MUX) is selected to the channel divider or SysRef, regardless of whether the output is powered down or not. When an output is not used, TI recommends selecting the VCO output to verify that the channel divider is not unnecessarily powered up.

Table 6-10. Channel Divider

RFOUTA	RFOUTB	CHANNEL DIVIDER Status
Channel Divider	Channel Divider	Powered up
Channel Divider	VCO	Powered up
VCO	Channel Divider	Powered up
Doubler	Channel Divider	Powered up
VCO	VCO	Powered down
VCO	Doubler	Powered down
Doubler	VCO	Powered down
Doubler	Doubler	Powered down

6.3.9 Output Mute Pin and Ping Pong Approaches

The output buffer can be muted or unmuted using the MUTE pin. The polarity of this pin is programmable with the OUTx_MUTE_POL bit in SPI mode. When the output is muted, the PLL stays in lock, so this can be used to combine multiple synthesizers for faster lock time. The PLL with the muted output can be accepting programming commands or even locking to a new frequency. As the output is muted, the unwanted signal is greatly attenuated and can be further attenuated with an external RF switch.

MuteA and MuteB pins are provided to Mute RFOUTA and RFOUTB independently. While One output is Muted, other output can be operated normally. MuteA and MuteB support both dedicated pin control and SPI-based configuration. In SPI mode, MuteA and MuteB operation can be set to operate either through register settings or through MuteA and MuteB pins.

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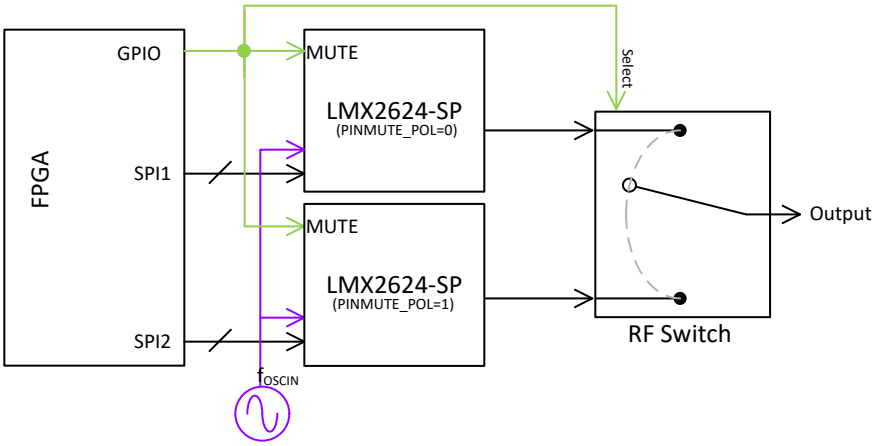

Figure 6-3. Output Mute implementation Using Two LMX2624-SP devices

6.3.10 Output Frequency Doubler

The frequency doubler is used to produce an output frequency that is twice the VCO frequency at RFOUTA and at RFOUTB based on OUTMUX2, OUTMUX1 and OUTMUX0 settings in Pin-mode or setting OUTx_MUX in SPI-mode. When the VCO frequency is doubled, the fundamental (non-doubled) VCO frequency does leak to the output and this is the sub-harmonic (0.5X). To minimize these sub-harmonics, there is tunable filter that tracks the output frequency and filters out this sub-harmonic as well as other undesired harmonics (1.5X, 2X, 3X, ...). The calibration for this tunable filter is automatically triggered whenever the VCO calibration is done.

6.3.11 Output Buffer

The RF output buffer utilizes a CML architecture with integrated 50Ω pull-up resistors and requires AC coupling to a 50Ω termination load. The output buffer can be programmed to various power levels or through OUTx_PD bit disabled while still keeping the PLL in lock.

OUTA_PWR and OUTB_PWR fields can be programed to increase or decrease the output buffer power level. There are 8 settings starting from 0 to 7 where 0 is for minimum power and 7 is for maximum power setting. During power on, default setting is 7.

6.3.12 Power-Down Modes

The LMX2624-SP can be powered up and down using the POWERDOWN bit or CAL pin. Setting the POWERDOWN bit to one or making the CAL pin to LOW moves the device to power down mode. To bring the device back to normal operation, either set the POWERDOWN bit to zero or pull back CAL Pin HIGH (if the device is powered down by CAL Pin). Register R0 must be programmed with FCAL_EN high again to re-calibrate the device. In Pin mode, a Low-to-High transition to the CAL pin activates a VCO calibration.

6.3.13 Phase Synchronization

6.3.13.1 General Concept

The SYNC pin allows one to synchronize the LMX2624-SP such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} is deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_COUNT if used in fractional mode.

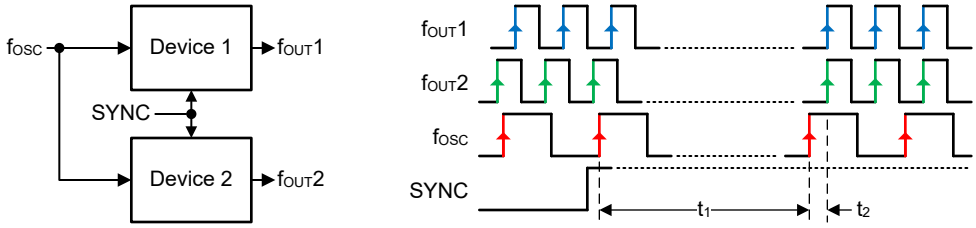

Figure 6-4. Multi-device Synchronization Using SYNC input

When the SYNC feature is enabled (VCO_PHASE_SYNC = 1), part of the channel divide (IncludedDivide) can be included in the feedback path. When IncludedDivide is not equal to 1:

- N divider is smaller. Care must be taken not to violate the minimum N divider restriction. Also make use of the FCAL_HPFD_ADJ register as per phase detector frequency range for valid VCO calibration.

Table 6-11. IncludedDivide With VCO_PHASE_SYNC = 1

OUTx_MUX	CHANNEL DIVIDER	IncludedDivide
OUTA_MUX = OUTB_MUX = 1 ("VCO") OUTA_MUX = OUTB_MUX = 2 ("Doubler")	Don't Care	1 (bypassed)
All Other Valid Conditions	Divisible by 3	6
	All other values	4

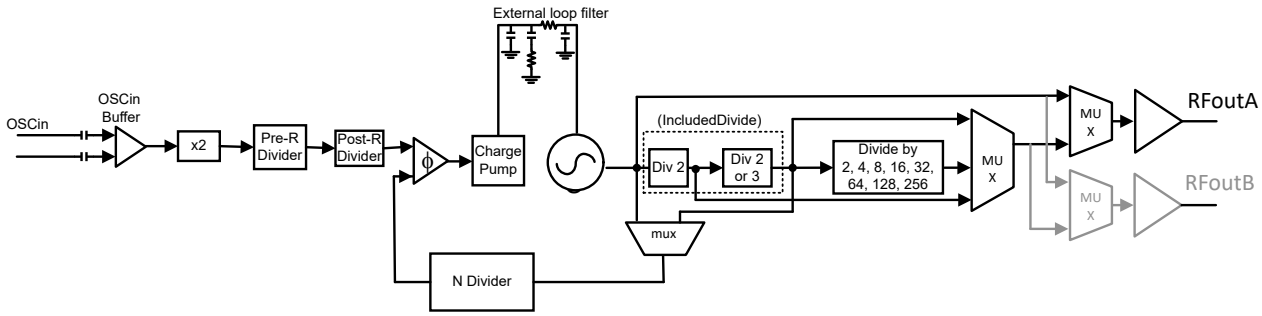

Figure 6-5. Phase SYNC Diagram

Phase SYNC refers to the process of getting the same phase relationship for every power up cycle and each time assuming that a given programming procedure is followed. However, there are some adjustments that can be made to get the most accurate results. As for the consistency of the phase SYNC, the only source of variation can be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10ps of variation. If this 10ps is not desirable, then the variation can be eliminated by reading back the VCO core, capcode, and DACISET values and forcing these values to provide the same calibration settings every time.

6.3.13.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. In cases that the SYNC is not timing critical, the SYNC can be done through software by toggling the VCO_PHASE_SYNC bit from 0 to 1. Figure 6-6 provides the different categories. When timing is critical, then SYNC must be done through the pin and the setup and hold times for the OSCin pin are critical. For timing critical sync (Category 3) ONLY, adhere to the following SYNC Pin Timing Characteristics for Category 3 SYNC.

Table 6-12. SYNC Pin Timing Characteristics for Category 3 SYNC

Parameter	Description	Min	Max	Unit
f_{OSC}	Input Reference Clock Frequency		50	MHz
t_{SETUP}	Setup time between SYNC and OSCin rising edges	2.5		ns
t_{HOLD}	Hold time between SYNC and OSCin rising edges	2.5		ns

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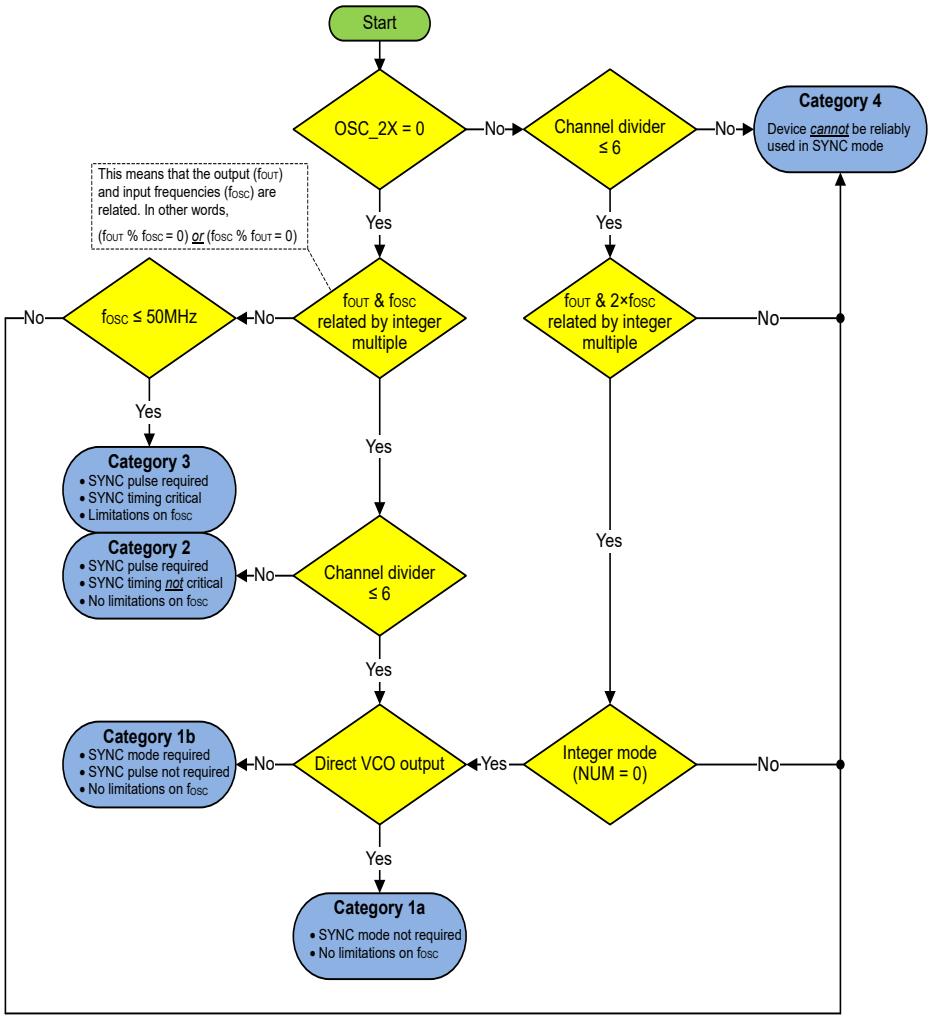

Figure 6-6. Determining the SYNC Category

6.3.13.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category
   a. If Category 4, SYNC cannot be performed in this setup.
   b. If Category 3, verify that the maximum f_{OSC} frequency for SYNC mode is not violated and there are hardware accommodations to use the SYNC pin.
3. If the channel divide is used, determine the IncludedDivide value from Table 6-11.
4. If not done already, divide the N divider and fractional values by IncludedDivide (Equation 2) to account for the included channel divide.
5. Program the device with the VCO_PHASE_SYNC = 1.
6. Apply the SYNC, if required
   a. If Category 2, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
   b. If Category 3, the timing of the SYNC signal with respect to OSCin clock as shown in Table 6-12 must obey.

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6.3.14 SYSREF

The LMX2624-SP can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with VCO_PHASE_SYNC = 1.

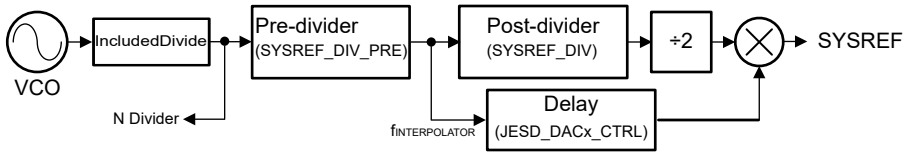

Figure 6-7. SYSREF Block Diagram

As Figure 6-7 shows, the SYSREF feature uses IncludedDivide and SYSREF_DIV_PRE divider to generate $f_{INTERPOLATOR}$. This frequency is used for re-clocking of the rising and falling edges at the SysRefReq pin. In SYSREF generation mode, the $f_{INTERPOLATOR}$ is further divided by 2×SYSREF_DIV to generate finite series or continuous stream of pulses.

Table 6-13. SYSREF Specification

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7500		15000	MHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
IncludedDivide		4 or 6		
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	÷ 4,6,8, ..., 4098			
$f_{INTERPOLATOR}$	$f_{INTERPOLATOR} = f_{VCO}$ /(IncludedDivide × SYSREF_DIV_PRE)			
f_{SYSREF}	$f_{SYSREF} = f_{INTERPOLATOR}$ / (2 × SYSREF_DIV)			
Pulses for pulsed mode (SYSREF_PULSE_CNT)	1		15	n/a

The delay can be programmed using the JESD_DAC1, JESD_DAC2, JESD_DAC3, and JESD_DAC4 fields. By concatenating these fields into a larger word called "SYSREFPHASESHIFT", the relative delay can be found. The sum of these words must always be 63. Altogether, there are 252 useful programmable steps. The delay time of each step is equal to:

SYSREF delay time = [(IncludedDivide × SYSREF_DIV_PRE) × 2] / 252 / f_{VCO}

Table 6-14. SysRef Delay

SYSREFPHASESHIFT	DELAY	JESD_DAC1	JESD_DAC2	JESD_DAC3	JESD_DAC4
0	Minimum	36	27	0	0
1		35	28	0	0
...		...	...	0	0
35		1	62	0	0
36		0	63	0	0
37		0	62	1	0
...		0	...	...	0
98		0	1	62	0
99		0	0	63	0
100		0	0	62	1
...		0	0	...	...
161		0	0	1	62
162		0	0	0	63
163		1	0	0	62
...		...	0	0	...
224		62	0	0	1
225		63	0	0	0
226		62	1	0	0
...		...	...	0	0
251	Maximum	37	26	0	0

6.3.14.1 Programmable Fields

Table 6-15 has the programmable fields for the SYSREF functionality.

Table 6-15. SYSREF Programming Fields

FIELD	PROGRAMMING	DEFAULT	DESCRIPTION
SYSREF_EN	0 = Disabled 1 = enabled	0	Enables the SYSREF mode. SYSREF_EN must be 1 if and only if OUTB_MUX=2 (SysRef)
SYSREF_DIV_PRE	1: DIV1 2: DIV2 4: DIV4 Other states: invalid	4	The output of this divider is the $f_{INTERPOLATOR}$.
SYSREF_REPEAT	0 = SYSREF generation mode 1 = SYSREF repeater mode	0	In SYSREF generation mode, the device creates a series of SYSREF pulses. In repeater mode, SYSREF pulses are generated with the SysRefReq pin.
SYSREF_PULSE	0 = Continuous mode 1 = Pulsed mode	0	Continuous mode continuously makes SYSREF pulses, where pulsed mode makes a series of SYSREF_PULSE_CNT pulses
SYSREF_PULSE_CNT	1 to 15	4	In the case of using pulsed mode, this is the number of pulses. Setting this to zero is an allowable, but not practical state.
SYSREF_DIV	0: Divide by 4 1: Divide by 6 2: Divide by 8 ... 2047: Divide by 4098	0	SYSREF_DIV divides down the interpolator clock to generate SYSREF frequency.

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6.3.14.2 Examples

In SYSREF generation mode, the SysRefReq pin is pulled HIGH and stay HIGH to allow continuous SYSREF clock output. To generate SYSREF pulses, a Low-to-High transition is required at the SysRefReq pin.

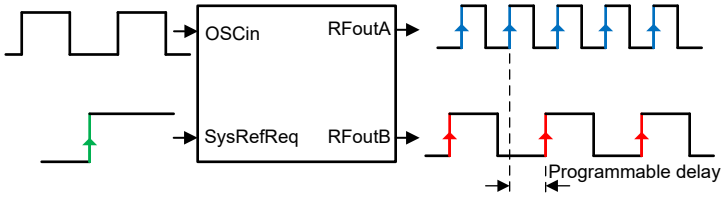

Figure 6-8. SYSREF Pulsed/Continuous Mode

Device support two types of repeater mode, asynchronous and reclocked. When RPTR_NONSYNC = 1, the SYSREF output passing through the signal without reclocking (asynchronous), whereas when RPTR_NONSYNC =0, the SYSREF output reclocked with VCO. In repeater mode, SYSREF output just echos the signal at SysRefReq pin, and then output to RFoutB. In repeater mode, the SysRefReq input signal can be single-shot, multiple pulses or continuous signal.

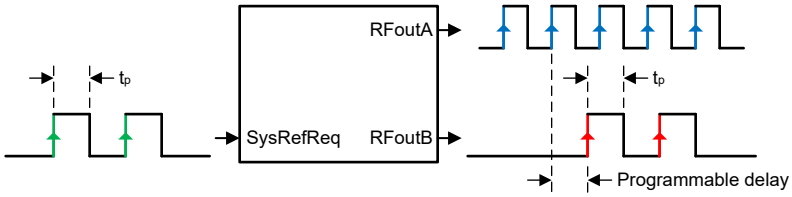

Figure 6-9. SYSREF Repeater Reclocked Mode

6.3.14.3 SYSREF Procedure

To configure and utilize the SYSREF signal, follow these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Find out IncludedDivide in the same way SYNC mode is done.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800MHz to 1500MHz.
4. If using SYSREF generation mode (SYSREF_REPEAT = 0), verify that SysRefReq pin is HIGH and stays HIGH for continuous SYSREF clock generation. To generate SYSREF pulses, set SYSREF_PULSE = 1, set up the pulse count as desired. Pulses are generated with a LOW-to-HIGH transition at SysRefReq pin.
5. If using SYSREF repeater mode (SYSREF_REPEAT = 1), apply the SYSREF signal to the SysRefReq pin.
   a. For asynchronous mode, RPTR_NONSYNC = 1.
   b. For VCO reclocked mode, RPTR_NONSYNC = 0.
6. Adjust the delay between the RFoutA and RFoutB (SYSREF output) signal using the JESD_DACx fields.

6.3.15 Pin-Mode Integer Frequency Generation

The LMX2624-SP has Pin-mode option to generate fixed frequency output without any serial programming. The output frequency is generated based on the Pin setting in the Pin-mode option. The Integer N divider, Output Channel Divider, OUTMUXs and Input Reference Doubler can be set using the Pin-mode options.

Conditions to use a device in Pin-mode.:

- Set the pin-mode using CDIVx pins. All pin combinations of CDIVx pins except when connected to GROUND is consider as Pin-mode. The SPI control cannot be used in Pin-mode. If CDIV2, CDIV1, and CDIV0 are tied to GROUND, the device is in SPI-mode.
- The rise time for the supply needs to be <50ms.
- Fractional Numerator and Denominator not available in Pin-mode, which means PLL can be used in Integer mode only.
- CAL pin tied to V_{CC}. CAL pin has to be toggled LOW to HIGH for frequency change from f_1 to f_2 in pin mode.

NDIVx and CDIVx pins are four level pins. Four level pins are used to get more number of division values with less number of pins which helps to reduce the overall package size. NDIVx has total of six pins and CDIVx has three pins. 6 pins of NDIVx (NDIV5, NDIV4, NDIV3, NDIV2, NDIV1, NDIV0) with four levels can create total of 4^6 combinations, which means 4096 values. Similarly CDIVx (CDIV2, CDIV1, CDIV0) with four level pins have total of 4^3 = 64 combinations. Due to the four level pins, 9 pins are sufficient instead of 18 pins for two level pins. The four levels of pin are VL, VML, VMH and VH as shows in Figure 6-10. Use three 10kΩ resistors across VCC and GROUND which have four levels including VCC, GROUND and two mid levels called VMH (Voltage Mid High) and VML (Voltage Mid Low).

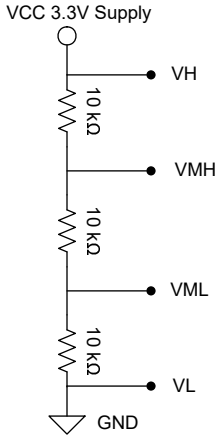

Figure 6-10. Four Level Pins Implementation

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NDIVx provides total of 4096 integer divider options in Pin-mode. Numerator (PLL_NUM) and Denominator (PLL_DEN) are not available in Pin-mode for fractional PLL and is only possible through SPI-mode. The minimum value for N divider restriction for Pin-mode NDIVx values are similar to the SPI-mode option. Refer to Table 6-2 for the N divider minimum value setting. Based on the N-divider decimal value, each NDIVx pin setting can be calculated with equivalent base 4.

Table 6-16. NDIVx Pin-Mode N-Divider Values

NDIV5	NDIV4	NDIV3	NDIV2	NDIV1	NDIV0	N-DIVIDER VALUE
VL	VL	VL	VL	VL	VL	0
VL	VL	VL	VL	VL	VML	1
VL	VL	VL	VL	VL	VMH	2
VL	VL	VL	VL	VL	VH	3
VL	VL	VL	VL	VML	VL	4
VL	VL	VL	VL	VML	VML	5
VL	VL	VL	VL	VML	VMH	6
VL	VL	VL	VL	VML	VH	7
VL	VL	VL	VL	VMH	VL	8
. . .	. . .				. . .	. . .
VL	VL	VL	VH	VMH	VH	59
VL	VL	VL	VH	VH	VL	60
VL	VL	VL	VH	VH	VML	61
VL	VL	VL	VH	VH	VMH	62
. . .	. . .				. . .	. . .
VH	VH	VH	VH	VH	VL	4092
VH	VH	VH	VH	VH	VML	4093
VH	VH	VH	VH	VH	VMH	4094
VH	VH	VH	VH	VH	VH	4095

All combinations of Channel Divider settings which are available in SPI-mode are also available in Pin-mode option using CDIVx pins. Refer to Table 6-17 for CDIVx settings in Pin-mode, CHDIV<4:0> settings in SPI-mode and the corresponding Channel Divider value. Based on the Channel Divider value needed, CDIV2, CDIV1, CDIV0 pins needed to be connected to one of the four levels.

Table 6-17. CDIVx Pin-Mode Divider Values

CDIV2	CDIV1	CDIV0	CHDIV<4:0> EQUIVALENT IN SPI MODE	CHANNEL DIVIDER VALUE
VL	VL	VL	0	SPI mode
VL	VML	VL	1	2
VL	VMH	VL	2	4
VL	VMH	VH	3	6
VML	VL	VL	4	8
VML	VL	VH	5	12
VML	VML	VL	6	16
VML	VML	VH	7	24
VML	VMH	VL	8	32
VML	VMH	VH	9	48
VML	VH	VL	10	64

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Table 6-17. CDIVx Pin-Mode Divider Values (continued)

CDIV2	CDIV1	CDIV0	CHDIV<4:0> EQUIVALENT IN SPI MODE	CHANNEL DIVIDER VALUE
VML	VH	VH	11	96
VMH	VL	VL	12	128
VMH	VL	VH	13	192
VMH	VML	VL	14	256
VMH	VML	VH	15	384
VMH	VMH	VL	16	512
VMH	VMH	VH	17	768
VMH	VH	VL	18	1024
VMH	VH	VH	19	1536

OUTMUX2, OUTMUX1 and OUTMUX0 pins are used to select the RFOUTx based on Table 6-18.

Table 6-18. OUTMUX Settings

OUTMUX2	OUTMUX1	OUTMUX0	RFOUTA OUTPUT	RFOUTB OUTPUT
0	0	0	Channel Divider	Channel Divider
0	0	1	Channel Divider	VCO
0	1	0	VCO	Channel Divider
0	1	1	VCO	VCO
1	0	0	Doubler	Channel Divider
1	0	1	VCO	Doubler
1	1	0	Doubler	VCO
1	1	1	Doubler	Doubler

6.3.15.1 4-level Pins Using GPIOs

Figure 6-10 described on creating VL, VML, VMH and VH levels using resistor network. This arrangement is sufficient if the RFOUTx frequency is fixed. For applications that require changes of frequency using pin-mode options, the NDIVx and CDIVx pins levels need to be changed as per the output frequency requirement. One option is to drive these 4-level pins using low speed precision DACs to create these four voltage levels which is complex.

Following arrangement can help in driving 4-level using GPIOs. See Driving 4-level Pins Using GPIOs in Pin-mode.

Table 6-19. Driving 4-level Pins Using GPIOs in Pin-mode

GPIO2	GPIO1	Nx	Voltage level at NDIVx Pin
VL	VL	VL	0
VL	VH	VML	VH/3
VH	VL	VMH	2×VH/3
VH	VH	VH	VH

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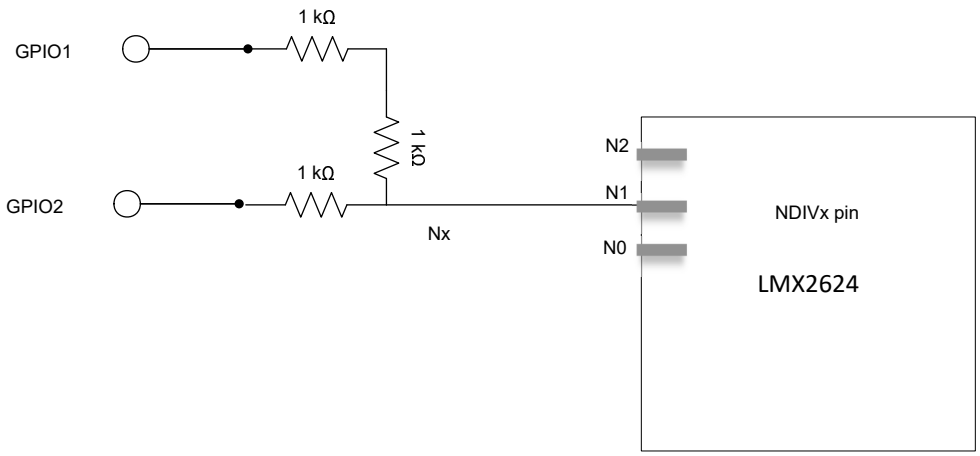

Figure 6-11. Driving 4 Level Pins Using GPIOs

The NDIVx and CDIVx pin configurations for pin-mode are dependent on the target output frequency; refer to Table 6-16 and Table 6-17 for lookup values.

6.3.15.2 Pin-Mode Example

LMX2624-SP need to be configure through pin-mode to generate clock frequency of 21GHz at RFoutA channel and RFoutB channel is disabled (no clock output / SYSREF).

Table 6-20. Pin-Mode Design Parameters

Parameter	Description	Value	Units
f_{OSC}	OSCin reference frequency	50	MHz
REF_DBLR_EN	Reference doubler enabled	x2	
f_{PD}	Phase detector frequency	100	MHz
f_{OUT}	RFoutA output frequency	21	GHz
f_{VCO}	VCO frequency	10.5	GHz

When frequency is known, the loop filter must be designed, through PLLatinum Sim tool. First look at the output frequency and confirm the frequency is operating in integer mode in Pin-mode configuration. Below table shows the pin mode settings for design requirements.

Table 6-21. GPIOs Pin-Mode Settings

Parameters	Description	Calculated/Required Value	GPIO settings
REF_DBLR_EN	OSCin doubler path	1	High (1)
N-divider	Feedback N-divider (f_{VCO}/f_{PD})	$(105)_{10}$ decimal	(NDIV5, NDIV4, NDIV3, NDIV2, NDIV1, NDIV0)$_4$ $(001221)_4$
CDIV	Channel Divider (f_{OUT}/f_{VCO})	≠ $(000)_{10}$ decimal	In RFout Doubler mode CDIV setting does not matter but must be ≠ 0 for pin-mode.
OUTMUXx	Output MUX settings	RFoutA Doubler, RFoutB OFF (set VCO path)	(OUTMUX2, OUTMUX1, OUTMUX0)$_2$ $(110)_2$
MuteA	Enable RFoutA output	0	Low (0)
MuteB	Disable RFoutB output	1	High (1)

Refer to Table 6-23 for configuring the connections for unused pins.

6.3.16 Device Functional Modes

Table 6-22. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in the reset state. This device does have a power on reset, but good practice is to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the datasheet that are reset as well.	RESET = 1 POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CAL Pin = Low
Pin-mode	Device settings are determined by pin states on CDIV.	Any one of the CDIV0, CDIV1, CDIV2 pins has value other than LOW
Normal operating mode	This is used with at least one output on as a frequency synthesizer and the device can be controlled through the SPI	All CDIV pins needs to be LOW
SYNC mode	This is used where part of the channel divider is in the feedback path to provide deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

6.4 Treatment of Unused Pins

This device has several pins for many features and there is a preferred way to treat these pins if not needed. For the input pins, a series resistor is recommend but can be directly shorted.

Table 6-23. Recommended Treatment of Pins

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
CDIV0, CDIV1, CDIV2	Always used	Always Used	SPI-mode: CDIV0, CDIV1, CDIV2 pins should be connect to GND with typical 1kΩ resistor. Pin-mode: CDIV0, CDIV1, CDIV2 pins must have value other than the GND for all pins at a time. Based on the value on these pins, output Divider is set.
NDIV0, NDIV1, NDIV2, NDIV3, NDIV4, NDIV5	Never used	Always Used	GND with 1kΩ
CAL	Sometimes Used	Always Used	VCC with 1kΩ
SYNC, SysRefReq	Sometimes Used	Never Used	GND with 1kΩ
OSCinP,OSCinM	Always Used	Always Used	GND with 50Ω to ground after the AC-coupling capacitor. If one side of complimentary side is used and other side is not, impedance looking out must be similar for both of these pins.
SCK, SDI	Always Used	Never Used	GND with 1kΩ
CSB	Always Used	Never Used	VCC with 1kΩ
RECAL_EN	Sometimes Used	Sometimes Used	Internally pulled to VCC with 200kΩ. When RECAL function is not used, GND with 1kΩ.
RFoutAP, RFoutAM, RFoutBP, RFoutBM	Sometimes Used	Sometimes Used	If both of the differential output pins are unused, the pins can be left floating and power down using SPI-mode or Mute the pins using Pin-mode options. If only one side of complimentary output is used, connect the unused pin to GND with 50Ω through AC coupling capacitor.
OUTMUX2, OUTMUX1, OUTMUX0	Never Used	Always used	GND with 1kΩ
REF_DBLR_EN	Never used	Some times used	GND with 1kΩ

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Table 6-23. Recommended Treatment of Pins (continued)

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
MuteA, MuteB	Sometimes used	Always used	GND with 1kΩ

6.5 Programming

When not in pin mode, the LMX2624-SP is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). See Figure 5-2 for timing details.

Only R/W type register fields as shown in Register Maps are required to program. programming to the read only register fields is not necessary, the fields cannot get written.

The reset or POR values of read only register fields are not necessary the same as shown in Register Maps because the initial state of these fields is not deterministic.

6.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure:

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program registers as shown in the Register Maps in REVERSE order from highest address to lowest address.
   - Programming of all registers down to R0 (with FCAL_EN = 1) is required. Even registers with no documented fields must also be programmed in accordance to the Register Maps. Do NOT assume that the power on reset state and the recommended value are the same.
4. Wait 10ms to verify that the internal LDOs has settled down
5. Program register R0 one additional time with FCAL_EN = 1 to verify that the VCO calibration runs from a stable state.

6.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change the N divider value.
2. Program the PLL numerator and denominator.
3. Program FCAL_EN (R0[2]) = 1.

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6.5.3 Register Maps

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	VCO_PHASE_SYNC	1	FCAL_DBLR_EN	0	0	OUT_MUTE		FCAL_HPFD_ADJ		FCAL_LPFD_ADJ		1	FCAL_EN	RESET	POWERDOWN
R1	0	MASH_SEED_EN	READBACK	LD_TYPE	OUTB_MUTE_POL	OUTA_MUTE_POL	OUTB_MUTE_PIN	OUTA_MUTE_PIN	OUTB_MUTE	OUTA_MUTE	OUTB_PD	OUTA_PD	1	CAL_CLK_DIV		
R2	0	0	0	0	1	CPG			0	0	OUTB_PWR			OUTA_PWR		
R3	OUTB_MUX		OUTA_MUX		OUTMUX	PFD_DLY						CHDIV				
R4	0	VCO_CAPCTRL_FORCE	VCO_DACISET_FORCE	VCO_SEL_FORCE	QUICK_RECAL_EN	1	1	0	0	1	0	0	0	1	0	0
R5	MASH_ORDER			VCO_FULL_ASSIST	VCO_SEL			VCO_DACISET								
R6	0	DBLR_AMP1_DACCTRL		DBLR_AMP_CAPCTRL				DBLR1_PD	VCO_CAPCTRL							
R7	0	VCO_FASTCHG_CNT								DBLR_PG_AMP_DACCTRL			DBLR_PG_AMP_CAPCTRL			
R8	PLL_N															
R9	PLL_N[18:16]			0	0	0	0	0	0	0	0	0	0	0	0	0
R10	PLL_DEN[15:0]															
R11	PLL_DEN[31:16]															
R12	MASH_SEED[15:0]															
R13	MASH_SEED[31:16]															
R14	PLL_NUM[15:0]															
R15	PLL_NUM[31:16]															
R16	0	0	0	0	0	0	0	DBL_BUF_EN	PLL_R							
R17	0	0	0	OSC_2X	PLL_R_PRE											
R18	SYSREF_DIV											SYSREF_DIV_PRE			SYSREF_EN	SYSREF_REPEAT
R19	0	JESD_DAC2						JESD_DAC1						RPTR_NONSYNC	0	SYSREF_PULSE
R20	SYSREF_PULSE_CNT				JESD_DAC4						JESD_DAC3					
R22	0	0	0	0	0	0	0	0	0	MUXOUT						
R23	LD_DLY															
R30	MASH_RST_COUNT[15:0]															
R31	MASH_RST_COUNT[31:16]															
R32	0	0	0	0	0	0	WD_DLY							WD_CNTRL		
R34	rb_VER_ID															
R35	0	0	0	0	0	0	0	0	0	0	rb_LD_VTUNE		rb_VCO_SEL			0

R84	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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6.5.3.1 Device Registers

Table 6-24 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 6-24 should be considered as reserved locations and the register contents should not be modified.

Table 6-24. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	R0		Section 6.5.3.1.1
1h	R1		Section 6.5.3.1.2
2h	R2		Section 6.5.3.1.3
3h	R3		Section 6.5.3.1.4
4h	R4		Section 6.5.3.1.5
5h	R5		Section 6.5.3.1.6
6h	R6		Section 6.5.3.1.7
7h	R7		Section 6.5.3.1.8
8h	R8		Section 6.5.3.1.9
9h	R9		Section 6.5.3.1.10
Ah	R10		Section 6.5.3.1.11
Bh	R11		Section 6.5.3.1.12
Ch	R12		Section 6.5.3.1.13
Dh	R13		Section 6.5.3.1.14
Eh	R14		Section 6.5.3.1.15
Fh	R15		Section 6.5.3.1.16
10h	R16		Section 6.5.3.1.17
11h	R17		Section 6.5.3.1.18
12h	R18		Section 6.5.3.1.19
13h	R19		Section 6.5.3.1.20
14h	R20		Section 6.5.3.1.21
16h	R22		Section 6.5.3.1.22
17h	R23		Section 6.5.3.1.23
1Eh	R30		Section 6.5.3.1.24
1Fh	R31		Section 6.5.3.1.25
20h	R32		Section 6.5.3.1.26
22h	R34		Section 6.5.3.1.27
23h	R35		Section 6.5.3.1.28
54h	R84		Section 6.5.3.1.29

Complex bit access types are encoded to fit into small table cells. Table 6-25 shows the codes that are used for access types in this section.

Table 6-25. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.5.3.1.1 R0 Register (Offset = 0h) [Reset = 33CCh]

R0 is shown in Table 6-26.

Return to the Summary Table.

Table 6-26. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	VCO_PHASE_SYNC	R/W	0h	Phase sync enable. If this bit is set as 1, a rising edge on SYNC pin triggers phase synchronization. SYSREF operation requires this bit set to 1. 0h = No phase synchronization 1h = Phase synchronization enabled
13	UNDISCLOSED	R/W	1h	Program this field to 0x1.
12	FCAL_DBLR_EN	R/W	1h	Enable bit for VCO doubler calibration. If this bit is set as 1, VCO doubler will be calibrated whenever VCO calibration is triggered. 0h = No VCO doubler calibration 1h = VCO doubler calibration enabled
11-10	UNDISCLOSED	R/W	0h	Program this field to 0x0.
9-8	OUT_MUTE	R/W	3h	Defines how to mute RF output during VCO calibration. If mute is selected, at least one VCO calibration has to be executed otherwise the selected mute channel will be muted. 0h = RFOUTA, RFOUTB not muted 1h = RFOUTA muted; RFOUTB not muted 2h = RFOUTA not muted; RFOUTB muted 3h = RFOUTA, RFOUTB muted
7-6	FCAL_HPFD_ADJ	R/W	3h	Adjustment to decrease the f_{PD} frequency for use in VCO calibration. Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0h = $f_{PD} \leq 50$MHz 1h = 50MHz < $f_{PD} \leq 100$MHz 2h = 100MHz < $f_{PD} \leq 200$MHz 3h = $f_{PD} > 200$MHz
5-4	FCAL_LPFD_ADJ	R/W	0h	Adjustment to increase the f_{PD} frequency for use in VCO calibration. Set this field in accordance to the phase detector frequency for optimal VCO calibration. 0h = $f_{PD} \geq 10$MHz 1h = 5MHz ≤ f_{PD} < 10MHz 2h = 2.5MHz ≤ f_{PD} < 5MHz 3h = f_{PD} < 2.5MHz
3	UNDISCLOSED	R/W	1h	Program this field to 0x1.
2	FCAL_EN	R/W	1h	Writing register R0 with this bit enabled as 1 triggers VCO calibration. 0h = No calibration 1h = Writing 1 triggers VCO calibration
1	RESET	R/W	0h	Resets all registers to silicon default values. Re-programming of all registers is required after a reset. 0h = Normal operation 1h = Writing 1 triggers reset
0	POWERDOWN	R/W	0h	Powers down the device. Register contents are retained when the device is powered down. 0h = Normal Operation 1h = Device power down

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6.5.3.1.2 R1 Register (Offset = 1h) [Reset = 10CBh]

R1 is shown in Table 6-27.

Return to the Summary Table.

Table 6-27. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	MASH_SEED_EN	R/W	0h	Enables MASH_SEED for spurious improvement. 0h = Disabled 1h = Enabled
13	READBACK	R/W	0h	Sets register read back control. 0h = Reads the written register values 1h = Reads the state machine values
12	LD_TYPE	R/W	1h	Defines Lock Detect type. VCOCal Lock Detect asserts a high output after the VCO has finished calibration and the LD_DLY timeout counter is finished. Vtune and VCOCal Lock Detect asserts a high output when VCOCal Lock Detect would assert a signal and the tuning voltage to the VCO is within acceptable limits (continuous monitoring of Vtune voltage). RECAL feature requires using Vtune and VCOCal Lock Detect. Both Lock Detect types require VCO calibration is executed at least one time, otherwise the output will stay low. 0h = VCOCal Lock Detect 1h = Vtune and VCOCal Lock Detect
11	OUTB_MUTE_POL	R/W	0h	Selects if MUTEB pin is active high or active low. 0h = Mutes when pin is high 1h = Mutes when pin is low
10	OUTA_MUTE_POL	R/W	0h	Selects if MUTEA pin is active high or active low. 0h = Mutes when pin is high 1h = Mutes when pin is low
9	OUTB_MUTE_PIN	R/W	0h	Selects if RFOUTB is muted through pin or register. 0h = Muted by pin 1h = Muted by register
8	OUTA_MUTE_PIN	R/W	0h	Selects if RFOUTA is muted through pin or register. 0h = Muted by pin 1h = Muted by register
7	OUTB_MUTE	R/W	1h	Mutes RFOUTB. 0h = RFOUTB is not muted 1h = RFOUTB is muted
6	OUTA_MUTE	R/W	1h	Mutes RFOUTA. 0h = RFOUTA is not muted 1h = RFOUTA is muted
5	OUTB_PD	R/W	0h	Powers down RFOUTB. 0h = RFOUTB is powered on 1h = RFOUTB is powered off
4	OUTA_PD	R/W	0h	Powers down RFOUTA. 0h = RFOUTA is powered on 1h = RFOUTA is powered off
3	UNDISCLOSED	R/W	1h	Program this field to 0x1.
2-0	CAL_CLK_DIV	R/W	3h	Sets state machine clock frequency equal to or less than 50MHz. $f_{SM} = f_{OSC} / 2^{CAL_CLK_DIV}$ 0h = $f_{OSC} \leq$ 50MHz 1h = $f_{OSC} \leq$ 100MHz 2h = $f_{OSC} \leq$ 200MHz 3h = $f_{OSC} \leq$ 400MHz 4h = $f_{OSC} \leq$ 800MHz 5h = $f_{OSC} >$ 800MHz

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6.5.3.1.3 R2 Register (Offset = 2h) [Reset = 0F3Fh]

R2 is shown in Table 6-28.

Return to the Summary Table.

Table 6-28. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	UNDISCLOSED	R/W	1h	Program this field to 0x1.
10-8	CPG	R/W	7h	Sets charge pump gain. 0h = Tri-state 1h = 6 mA 2h = Reserved 3h = 12 mA 4h = 3 mA 5h = 9 mA 6h = Reserved 7h = 15 mA
7-6	UNDISCLOSED	R/W	0h	Program this field to 0x0.
5-3	OUTB_PWR	R/W	7h	Controls RFOUTB output power. Higher values give more output power.
2-0	OUTA_PWR	R/W	7h	Controls RFOUTA output power. Higher values give more output power.

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6.5.3.1.4 R3 Register (Offset = 3h) [Reset = 5040h]

R3 is shown in Table 6-29.

Return to the Summary Table.

Table 6-29. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	OUTB_MUX	R/W	1h	Selects RFOUTB configuration. 0h = Divided down output 1h = Direct VCO output 2h = VCO doubler output 3h = SYSREF output
13-12	OUTA_MUX	R/W	1h	Selects RFOUTA configuration. 0h = Divided down output 1h = Direct VCO output 2h = VCO doubler output 3h = Reserved
11	OUTMUX	R/W	0h	Decides whether RF output selection (divided down, direct VCO or VCO doubler output) is controlled through OUTMUX pins or register. 0h = Controlled through pin 1h = Controlled through register
10-5	PFD_DLY	R/W	2h	Programmable phase detector delay. This should be programmed based on VCO frequency, fractional order, and N divider value. All other values must be set in accordance to the N divider value 0h = Reserved
4-0	CHDIV	R/W	0h	Sets VCO frequency divider value for RF output. Values not listed in the following are reserved. 1h = Divide by 2 2h = Divide by 4 3h = Divide by 6 4h = Divide by 8 5h = Divide by 12 6h = Divide by 16 7h = Divide by 24 8h = Divide by 32 9h = Divide by 48 Ah = Divide by 64 Bh = Divide by 96 Ch = Divide by 128 Dh = Divide by 192 Eh = Divide by 256 Fh = Divide by 384 10h = Divide by 512 11h = Divide by 768 12h = Divide by 1024 13h = Divide by 1536

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6.5.3.1.5 R4 Register (Offset = 4h) [Reset = 0644h]

R4 is shown in Table 6-30.

Return to the Summary Table.

Table 6-30. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14	VCO_CAPCTRL_FORCE	R/W	0h	Allows forcing the device to use the programmed VCO_CAPCTRL value for the VCO. 0h = Disabled 1h = Enabled
13	VCO_DACISET_FORCE	R/W	0h	Allows forcing the device to use the programmed VCO_DACISET value for the VCO. 0h = Disabled 1h = Enabled
12	VCO_SEL_FORCE	R/W	0h	Allows forcing the device to use the programmed VCO_SEL value to manually select the VCO core. 0h = Disabled 1h = Enabled
11	QUICK_RECAL_EN	R/W	0h	Selects VCO configuration (VCO_CAPCTRL, VCO_SEL and VCO_DACISET) values for VCO calibration to begin with. 0h = Use programmed VCO configuration 1h = Use current VCO configuration state machine values
10-0	UNDISCLOSED	R/W	644h	Program this field to 0x644.

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6.5.3.1.6 R5 Register (Offset = 5h) [Reset = 0F2Ch]

R5 is shown in Table 6-31.

Return to the Summary Table.

Table 6-31. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	MASH_ORDER	R/W	0h	Sets the MASH order. When MASH is disabled, the fractional numerator (PLL_NUM) is ignored. Values not listed in the following are reserved. 0h = MASH disabled 1h = First order modulator 2h = Second order modulator 3h = Third order modulator
12	VCO_FULL_ASSIST	R/W	0h	Enabling this bit forces the device to use the programmed value for the following fields: VCO_SEL, VCO_CAPCTRL, VCO_DACISET DBLR1_PD, DBLR_AMP_CAPCTRL, DBLR_AMP1_DACCTRL DBLR_PG_AMP_CAPCTRL, DBLR_PG_AMP_DACCTRL If enabled, DBL_BUF_EN = 1 is required. 0h = Disabled 1h = Enabled
11-9	VCO_SEL	R/W	7h	Sets the initial VCO core for VCO calibration. Unless QUICK_RECAL_EN = 1, VCO calibration always start with the value specified in this field. 0h = Reserved 1h = VCO1 2h = VCO2 3h = VCO3 4h = VCO4 5h = VCO5 6h = VCO6 7h = VCO7
8-0	VCO_DACISET	R/W	12Ch	Sets the initial value for VCO calibration, typical value is 300. Unless QUICK_RECAL_EN = 1, VCO calibration always start with the value specified in this field.

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6.5.3.1.7 R6 Register (Offset = 6h) [Reset = 41BFh]

R6 is shown in Table 6-32.

Return to the Summary Table.

Table 6-32. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14-13	DBLR_AMP1_DACCTRL	R/W	2h	VCO doubler configuration. Programming is required only with full assist mode. Field value is obtained by reading back the register after VCO doubler calibration.
12-9	DBLR_AMP_CAPCTRL	R/W	0h	VCO doubler configuration. Programming is required only with full assist mode. Field value is obtained by reading back the register after VCO doubler calibration.
8	DBLR1_PD	R/W	1h	Disables path 1 for VCO doubler. Programming is required only with full assist mode. Field value is obtained by reading back the register after VCO doubler calibration. 0h = Doubler path 1 is enabled 1h = Doubler path 1 is disabled
7-0	VCO_CAPCTRL	R/W	BFh	Sets the initial value for VCO calibration. Valid values are between 0 and 191. Higher value represents lower VCO frequency. Unless QUICK_RECAL_EN = 1, VCO calibration always start with the value specified in this field.

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6.5.3.1.8 R7 Register (Offset = 7h) [Reset = 7D40h]

R7 is shown in Table 6-33.

Return to the Summary Table.

Table 6-33. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14-7	VCO_FASTCHG_CNT	R/W	FAh	Sets the fast charge ON time for use in full assist mode or when double buffering is enabled. ON time = VCO_FASTCHG_CNT / f_{SM} Recommended ON time is 5µs.
6-4	DBLR_PG_AMP_DACCTRL	R/W	4h	VCO doubler configuration. Programming is required only with full assist mode. Field value is obtained by reading back the register after VCO doubler calibration.
3-0	DBLR_PG_AMP_CAPCTRL	R/W	0h	VCO doubler configuration. Programming is required only with full assist mode. Field value is obtained by reading back the register after VCO doubler calibration.

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6.5.3.1.9 R8 Register (Offset = 8h) [Reset = 0046h]

R8 is shown in Table 6-34.

Return to the Summary Table.

Table 6-34. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_N	R/W	46h	Lower 16 bits of N-divider, total 19 bits.

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6.5.3.1.10 R9 Register (Offset = 9h) [Reset = 0000h]

R9 is shown in Table 6-35.

Return to the Summary Table.

Table 6-35. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	PLL_N[18:16]	R/W	0h	Upper 3 bits of N-divider, total 19 bits.
12-0	UNDISCLOSED	R/W	0h	Program this field to 0x0.

6.5.3.1.11 R10 Register (Offset = Ah) [Reset = DA80h]

R10 is shown in Table 6-36.

Return to the Summary Table.

Table 6-36. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN[15:0]	R/W	DA80h	Lower 16 bits of fractional denominator, total 32 bits.

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6.5.3.1.12 R11 Register (Offset = Bh) [Reset = FD51h]

R11 is shown in Table 6-37.

Return to the Summary Table.

Table 6-37. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN[31:16]	R/W	FD51h	Upper 16 bits of fractional denominator, total 32 bits.

6.5.3.1.13 R12 Register (Offset = Ch) [Reset = 0000h]

R12 is shown in Table 6-38.

Return to the Summary Table.

Table 6-38. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[15:0]	R/W	0h	Lower 16 bits of MASH_SEED, total 32 bits.

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6.5.3.1.14 R13 Register (Offset = Dh) [Reset = 0000h]

R13 is shown in Table 6-39.

Return to the Summary Table.

Table 6-39. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED[31:16]	R/W	0h	Upper 16 bits of MASH_SEED, total 32 bits.

6.5.3.1.15 R14 Register (Offset = Eh) [Reset = 0000h]

R14 is shown in Table 6-40.

Return to the Summary Table.

Table 6-40. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM[15:0]	R/W	0h	Lower 16 bits of fractional numerator, total 32 bits.

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6.5.3.1.16 R15 Register (Offset = Fh) [Reset = 0000h]

R15 is shown in Table 6-41.

Return to the Summary Table.

Table 6-41. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM[31:16]	R/W	0h	Upper 16 bits of fractional numerator, total 32 bits.

6.5.3.1.17 R16 Register (Offset = 10h) [Reset = 0001h]

R16 is shown in Table 6-42.

Return to the Summary Table.

Table 6-42. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	UNDISCLOSED	R/W	0h	Program this field to 0x0.
8	DBL_BUF_EN	R/W	0h	Enables double buffering. Double buffering allows the user to program multiple registers without having them actually take effect until register R0 is written. When this bit is enabled, sufficient fast charge ON time needs to be set. Full Assist Mode requires this bit set to 1. 0h = Disables double buffering 1h = Enables double buffering
7-0	PLL_R	R/W	1h	Reference path Post-R divider. This is the divider after the Pre-R divider.

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6.5.3.1.18 R17 Register (Offset = 11h) [Reset = 1001h]

R17 is shown in Table 6-43.

Return to the Summary Table.

Table 6-43. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	UNDISCLOSED	R/W	0h	Program this field to 0x0.
12	OSC_2X	R/W	1h	Enables reference path input clock doubler. 0h = Disabled 1h = Enabled
11-0	PLL_R_PRE	R/W	1h	Reference path Pre-R divider. The upper 4 bits are not used.

6.5.3.1.19 R18 Register (Offset = 12h) [Reset = 0030h]

R18 is shown in Table 6-44.

Return to the Summary Table.

Table 6-44. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	SYSREF_DIV	R/W	1h	This divider further divides the clock frequency for SYSREF output.
4-2	SYSREF_DIV_PRE	R/W	4h	This divider is used to reduce the clock frequency to the SYSREF divider. Output frequency of this divider should be between 800MHz and 1.5GHz. Values not listed in the following are reserved. 1h = Bypassed 2h = Divide by 2 4h = Divide by 4
1	SYSREF_EN	R/W	0h	Enables SYSREF mode. 0h = Disables SYSREF module 1h = Enables SYSREF module
0	SYSREF_REPEAT	R/W	0h	Sets the device in SYSREF generation or repeater mode. In generation mode, SYSREF clocks are generated with internal circuitry. In repeater mode, incoming SYSREF signal passes through the device without reclocking. 0h = Generation mode 1h = Repeater mode

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6.5.3.1.20 R19 Register (Offset = 13h) [Reset = 01F8h]

R19 is shown in Table 6-45.

Return to the Summary Table.

Table 6-45. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	UNDISCLOSED	R/W	0h	Program this field to 0x0.
14-9	JESD_DAC2	R/W	0h	Programmable delay for SYSREF output.
8-3	JESD_DAC1	R/W	3Fh	Programmable delay for SYSREF output.
2	RPTR_NONSYNC	R/W	0h	Enables non-synchronous SYSREF repeater mode. In SYSREF repeater mode, if this bit is set to 1, the output SYSREF clock will not be re-clocked with the VCO, allowing the input SYSREF clock to pass through the device directly. 0h = Reclocking with VCO 1h = Passing through without reclocking
1	UNDISCLOSED	R/W	0h	Program this field to 0x0.
0	SYSREF_PULSE	R/W	0h	Sets the device for continuous SYSREF pulses or fixed number of pulses. In continuous mode, SYSREF pulses are generated continuously. Pulsed mode allows multiple pulses, as determined by SYSREF_PULSE_CNT, to be sent out whenever the SysRefReq pin goes HIGH. 0h = Continuous mode 1h = Pulsed mode

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6.5.3.1.21 R20 Register (Offset = 14h) [Reset = 0000h]

R20 is shown in Table 6-46.

Return to the Summary Table.

Table 6-46. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SYSREF_PULSE_CNT	R/W	0h	Defines how many pulses are sent in SYSREF pulsed mode. Valid values are between 1 and 15.
11-6	JESD_DAC4	R/W	0h	Programmable delay for SYSREF output.
5-0	JESD_DAC3	R/W	0h	Programmable delay for SYSREF output.

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6.5.3.1.22 R22 Register (Offset = 16h) [Reset = 0001h]

R22 is shown in Table 6-47.

Return to the Summary Table.

Table 6-47. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	UNDISCLOSED	R/W	0h	Program this field to 0x0.
6-0	MUXOUT	R/W	1h	Selects the functionality of the MUXOUT pin. 0h = Lock detect 1h = Register read back 2h = f_{PD} / 32 3h = f_{SM} / 32

6.5.3.1.23 R23 Register (Offset = 17h) [Reset = 09C4h]

R23 is shown in Table 6-48.

Return to the Summary Table.

Table 6-48. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LD_DLY	R/W	9C4h	For the VCOCal Lock Detect type, this is the delay in state machine clock cycles that is added after the calibration is finished before the lock detect is asserted high. Delay time = LD_DLY × 4 / f_{SM}

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6.5.3.1.24 R30 Register (Offset = 1Eh) [Reset = D6D8h]

R30 is shown in Table 6-49.

Return to the Summary Table.

Table 6-49. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[15:0]	R/W	D6D8h	Lower 16 bits of MASH_RST_COUNT, total 32 bits. This field defines the delay time that is necessary after the MASH engine is reset during phase synchronization. When PLL_NUM is not zero, the delay time should be set to at least four times the PLL lock time. This field can be set to 0 when PLL_NUM = 0. Delay time = MASH_RST_COUNT / f_{SM}

6.5.3.1.25 R31 Register (Offset = 1Fh) [Reset = 0000h]

R31 is shown in Table 6-50.

Return to the Summary Table.

Table 6-50. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT[31:16]	R/W	0h	Upper 16 bits of MASH_RST_COUNT, total 32 bits.

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6.5.3.1.26 R32 Register (Offset = 20h) [Reset = 026Fh]

R32 is shown in Table 6-51.

Return to the Summary Table.

Table 6-51. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	UNDISCLOSED	R/W	0h	Program this field to 0x0.
9-3	WD_DLY	R/W	4Dh	Delay for the internal watchdog timer. Delay time = WD_DLY × 2^{14} / f_{SM}
2-0	WD_CNTRL	R/W	7h	Watchdog control. 0h = Digital Watchdog disabled 1h = Watchdog triggers 1 time 2h = Watchdog triggers up to 2 times 3h = Watchdog triggers up to 3 times 4h = Watchdog triggers up to 4 times 5h = Watchdog triggers up to 5 times 6h = Watchdog triggers up to 6 times 7h = Watchdog retriggers as many times as necessary with no limit

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6.5.3.1.27 R34 Register (Offset = 22h) [Reset = 0000h]

R34 is shown in Table 6-52.

Return to the Summary Table.

Table 6-52. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_VER_ID	R	0h	Reads back device version ID.

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6.5.3.1.28 R35 Register (Offset = 23h) [Reset = 0000h]

R35 is shown in Table 6-53.

Return to the Summary Table.

Table 6-53. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	UNDISCLOSED	R/W	0h	Program this field to 0x0.
5-4	rb_LD_VTUNE	R	0h	Read back field for lock detect status. Applicable only when register R0 is programmed at least one time with LD_TYPE = 1, FCAL_EN bit is don't care. Values not listed in the following mean unlocked. 2h = Locked
3-1	rb_VCO_SEL	R	0h	Reads back the actual VCO core that the VCO calibration has selected. 0h = Reserved 1h = VCO1 2h = VCO2 3h = VCO3 4h = VCO4 5h = VCO5 6h = VCO6 7h = VCO7
0	UNDISCLOSED	R	0h	Program this field to 0x0.

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6.5.3.1.29 R84 Register (Offset = 54h) [Reset = 0000h]

R84 is shown in Table 6-54.

Return to the Summary Table.

Table 6-54. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UNDISCLOSED	R/W	0h	Program this field to 0x4000. Note that this is different than the reset value.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 OSCin Configuration

OSCin supports single-ended or differential clock. There must be a AC -coupling capacitor in series before the device pin. The OSCin inputs are high impedance CMOS with internal bias voltage. TI recommends putting termination shunt resistors to terminate the differential traces (if there are 50Ω characteristic traces, place 50Ω resistors). The OSCinP and OSCinM side must be matched in layout. A series AC-coupling capacitors must immediately follow OSCin pins in the board layout, then the shunt termination resistors to ground must be placed after.

Input clock definitions are shown in Figure 7-1:

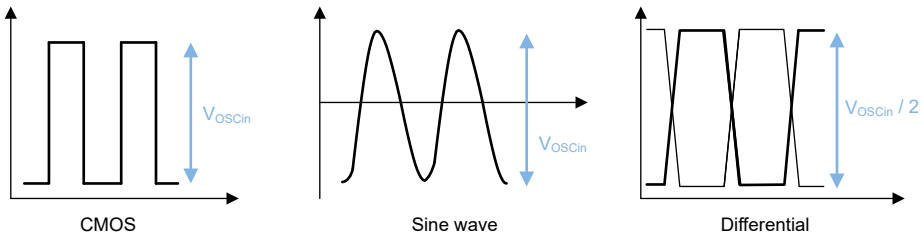

Figure 7-1. Input Clock Definitions

7.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the device if the slew rate is too low. In general, the best performance is for a high slew rate, but lower amplitude signal, such as LVDS.

7.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers control the amount of output power. OUTx_PWR setting "7" recommend to provide maximum output power with consume more current consumption and can be control the output power by reducing the setting till 1.

7.1.4 RF Output Buffer

The pull up resistors are integrated in this device. 50Ω resistors to VCC pull up is there internally for each pin on the differential outputs RFOUTA and RFOUTB.

7.1.5 RF Output Treatment for the Complimentary Side

Regardless of whether both sides of the differential outputs are used, both sides must see a similar load.

7.1.5.1 Single-ended Termination of Unused Output

The unused output must have approximately the same impedance as looking out of the pin to minimize harmonics and get the best output power. If the application requirement is to use only single-ended output, for example RFOUTAP, then the user must verify that the RFOUTAM also has same impedance. For a typical 50Ω systems with 50Ω PCB traces, the unused pin can be terminated with 50Ω with AC coupling capacitor.

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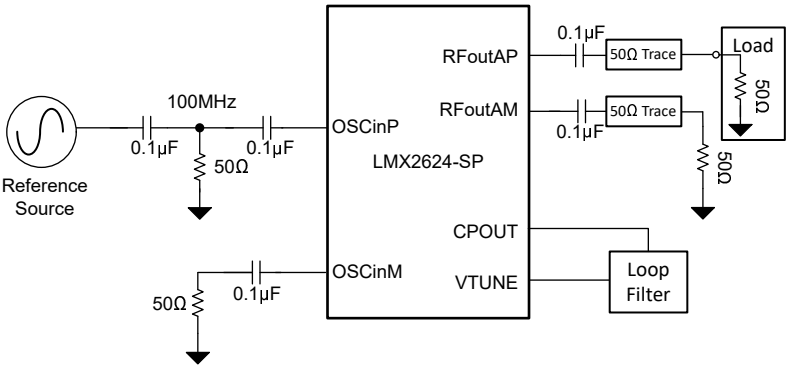

Figure 7-2. Termination of Unused Output

7.2 Typical Application

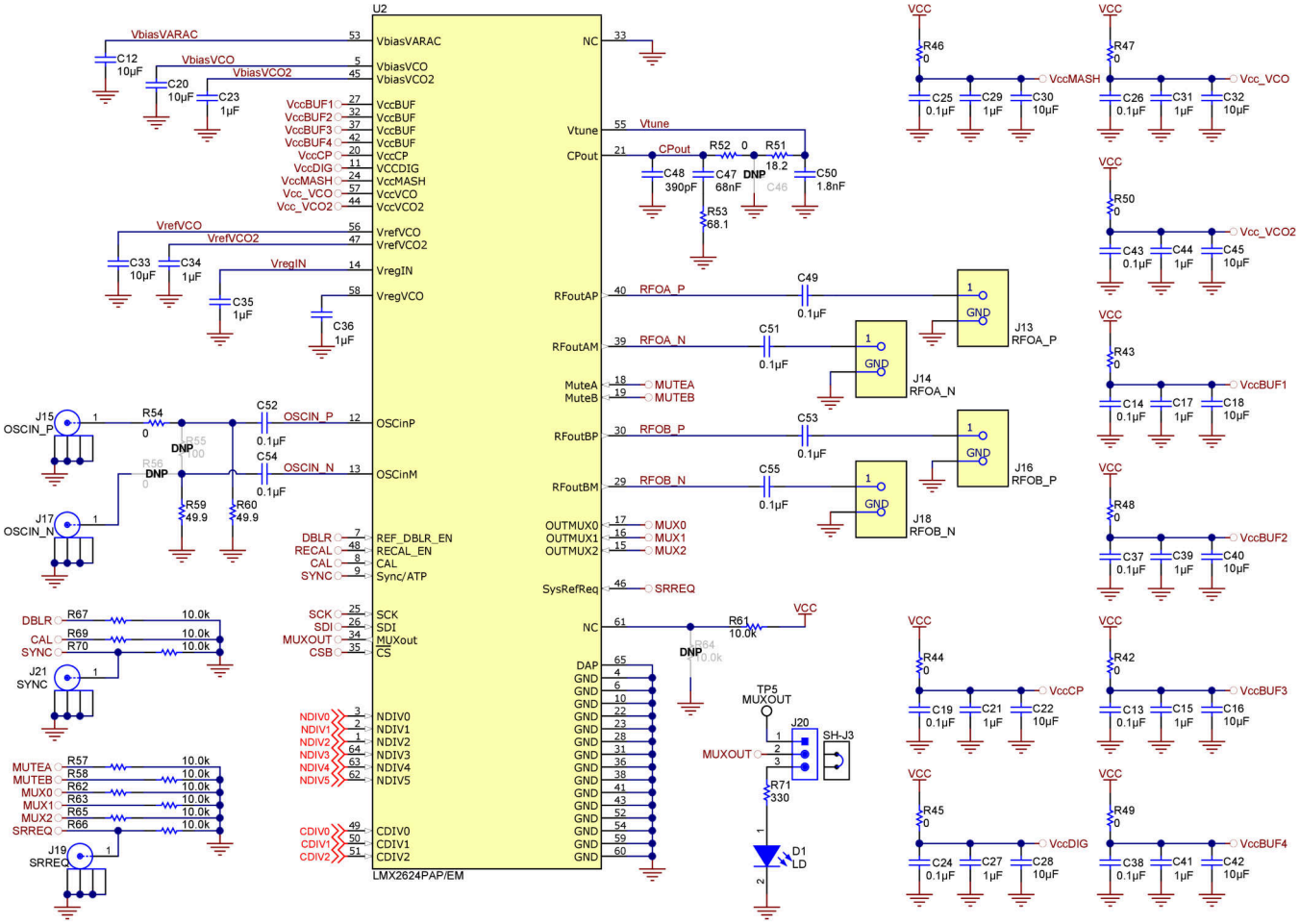

Figure 7-3. Typical Application Schematic

7.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLATINUM Sim software is an excellent resource for doing this and the design and simulation. In this case, an integer PLL design is assumed and this is being designed for optimal jitter, as is the case for many clocking applications. For this example, a 12GHz output is assumed to be generated from a 100MHz clock. From this, the engineer must select a VCO frequency and phase detector before proceeding to the loop filter design.

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The VCO frequency must be in the range of 7.5GHz to 15GHz, the output frequency must either divide into this, VCO or double the VCO frequency. In this case, this implies the VCO frequency is 12GHz. The next step is to select the phase detector frequency. The phase detector frequency must either divide the input frequency, or the frequency can be double if the OSC_2X feature is used. Also, if the phase detector frequency divides the VCO frequency, the spur performance is much better. So by choosing a 200MHz phase detector frequency and using the OSC_2X doubler, the device can be used in integer mode and the best phase noise performance can be achieved.

Table 7-1. Design Parameters

Parameter	Description	Value	Units
f_{OSC}	OSCin reference frequency	100	MHz
OSC_2X = "1"	Reference doubler enabled	x2	-
f_{PD}	Phase detector frequency	200	MHz
f_{OUT}	RFoutA output frequency	12	GHz
f_{VCO}	VCO frequency	12	GHz

7.2.2 Detailed Design Procedure

When the frequencies are known, the loop filter must be designed. The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if the loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The trade-off with this is that longer lock times and spurs must be considered in design as well.

The PLLatinum Sim software is very useful in designing the loop filter and is available on the TI website. Using this tool, the results in Table 7-2 are obtained.

Table 7-2. PLLatinum Sim Results

COMPONENT	VALUE	UNIT
C1	390	pF
C2	68	nF
C3	1.8	nF
R2	68.1	Ω
R3	18.2	Ω

The TICS Pro software is very useful in calculating the necessary register values and configuring the device. Figure 7-4 shows the TICS Pro configuration for 12GHz output at RFoutA channel.

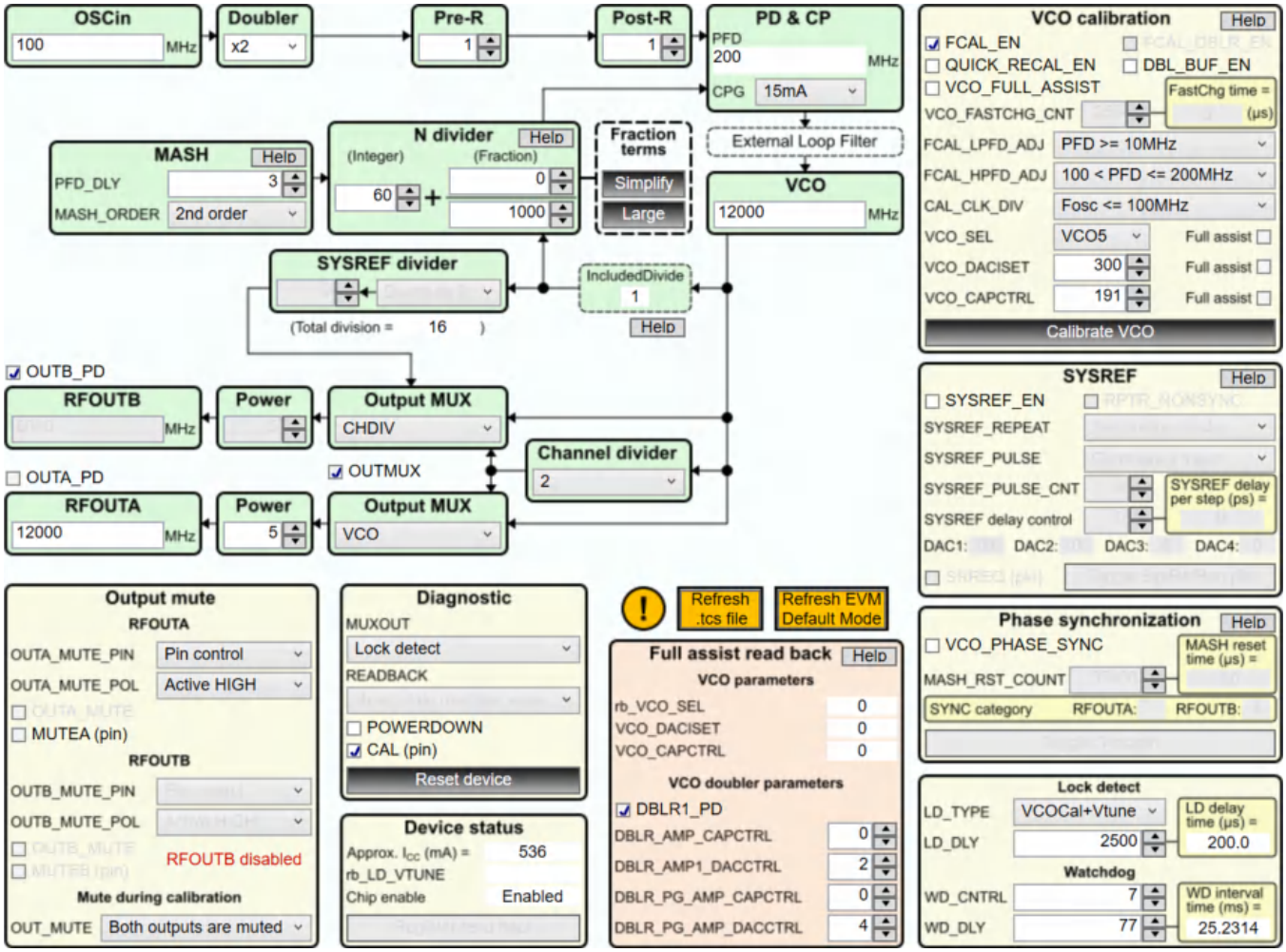

Figure 7-4. LMX2624-SP TICS Pro Setup

7.2.3 Application Curve

Using the settings described, the 12GHz performance measured using a clean 100MHz input reference is shown. Note the loop bandwidth is about 350kHz, as simulations predict.

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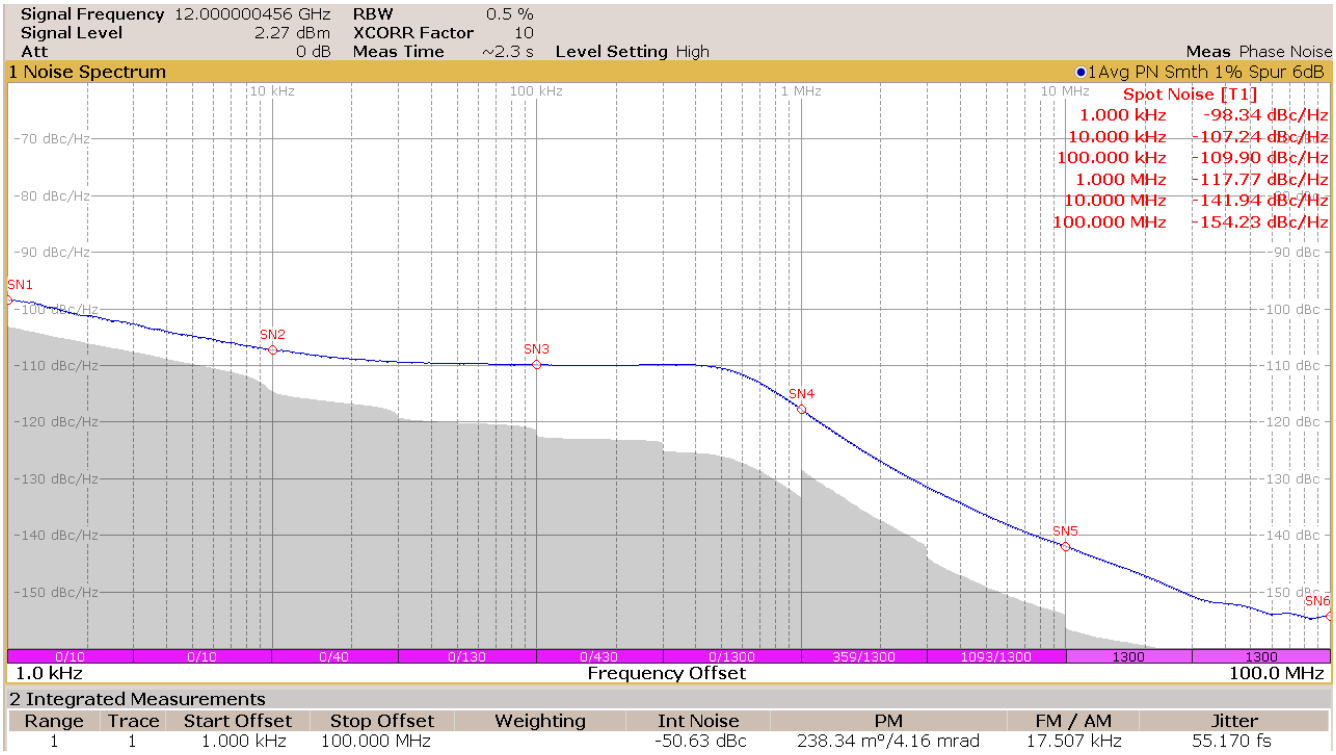

Figure 7-5. Results for Loop Filter Design

7.3 Power Supply Recommendations

TI recommends placement of bypass capacitors close to the pins. Consult the EVM instructions for layout examples. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise.

7.4 Layout

7.4.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins can be routed on the package back to the DAP.
- The OSCin pins, these are internally biased and must be AC coupled.
- If not used, the SysRefReq can be grounded to the DAP.
- For optimal VCO phase noise in the 200kHz – 1MHz range, place the capacitor closest to the Vtune pin be at least 3.3nF. As requiring this larger capacitor can restrict the loop bandwidth, this value can be reduced (to say 1.5nF) at the expense of VCO phase noise.
- If a single-ended output is needed, the other side must have the same loading. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, make the load look equivalent to the side that is used.
- Verify that DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2624-SP exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- Place voltage supply bypass capacitor close to the pin.

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7.4.2 Layout Example

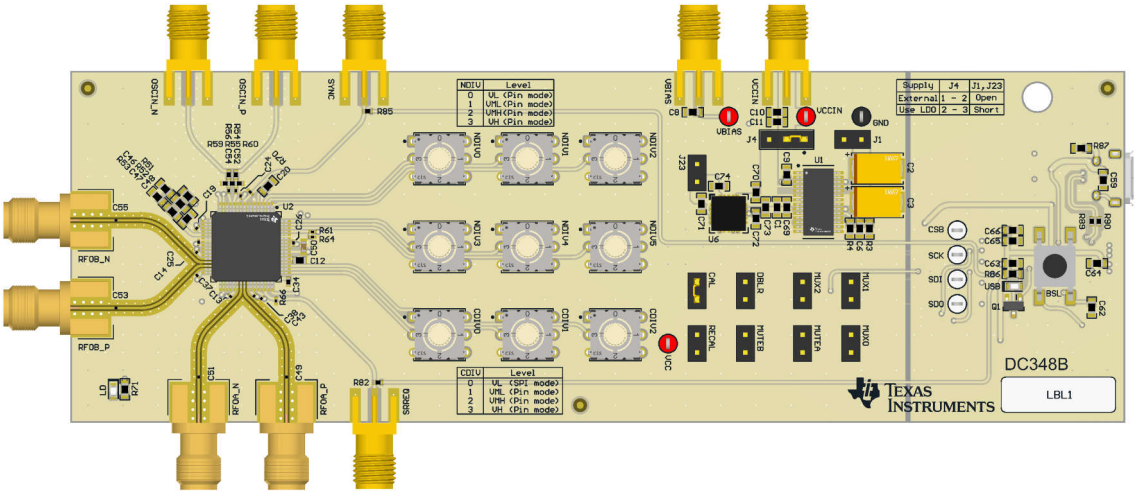

Figure 7-6. LMX2624-SP Layout Example

7.4.3 Footprint Example on PCB Layout

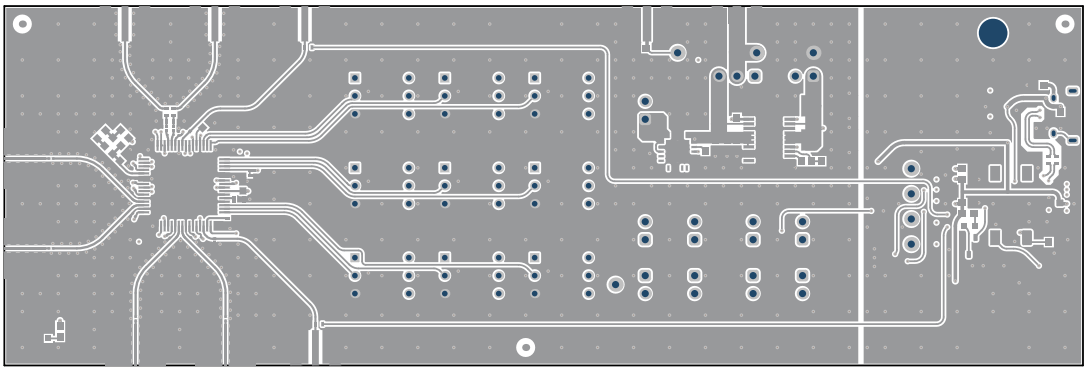

Figure 7-7. LMX2624-SP PCB Layout (Top Layer - RF signal)

7.4.4 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

7.4.4.1 Total Ionizing Dose

Radiation Hardness Assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the ordering information. Testing and qualification of these product is done on a wafer level according to MIL-STD-883, test method 1019. Wafer level TID data are available with lot shipments.

7.4.4.2 Single Event Effect

One time single event effect (SEE), including single event latch-up (SEL), single event functional interrupt (SEFI) and single event upset (SEU), testing is performed according to EIA/JEDEC Standard, EIA/JEDEC57. A test report is available upon request.

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

Texas Instruments has several software tools to aid in the development at www.ti.com. Among these tools are:

- EVM software to understand how to program the device and for programming the EVM board.
- EVM board instructions for seeing typical measured data with detailed measurement conditions and a complete design.
- PLLatinum Sim program for designing loop filters, simulating phase noise, and simulating spurs.

Table 8-1. Development Tools and Software

TOOL	TYPE	DESCRIPTION
PLLatinum™ Sim	Software	Simulates phase noise in all modes
TICS Pro	Software	Programs the device with a user-friendly GUI with interactive feedback and hex register export.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, LMX2624-SP Evaluation Module, EVM user's guide
- Texas Instruments, *AN-1879 Fractional N Frequency Synthesis* application note
- Texas Instruments, *PLL Performance, Simulation, and Design Handbook* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2026) to Revision B (September 2026)	Page
• Changed the RF output phase noise specs to the updated data	8
• Changed the tCWH spec from "6" to "10"	12
• Updated the Figure 5-20, Figure 5-21, and note for Figure 5-15	15
• Updated the description for Section 6.3.2.1	24
• Updated the description for VCO Calibration and Table 6-4	26
• Updated the description for RECAL Feature	29
• Updated the description for Section 6.3.8	29
• Updated the description for Section 6.3.13.1	31
• Updated the Table 6-13	35
• Updated the Table 6-15	36
• Updated the description for Section 6.3.14.2	37
• Updated the Table 6-23	42
• Changed the description for Register Maps, register R1 and register R2	45
• Changed the VOSCin value for Differential input clock in Figure 7-1	77
• Changed the parameter text for Table 7-1	78
• Updated the description for Power Supply Recommendations	81

Changes from Revision * (December 2024) to Revision A (July 2026)	Page
• Changed the device status from *Advanced* to *Production* Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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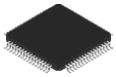
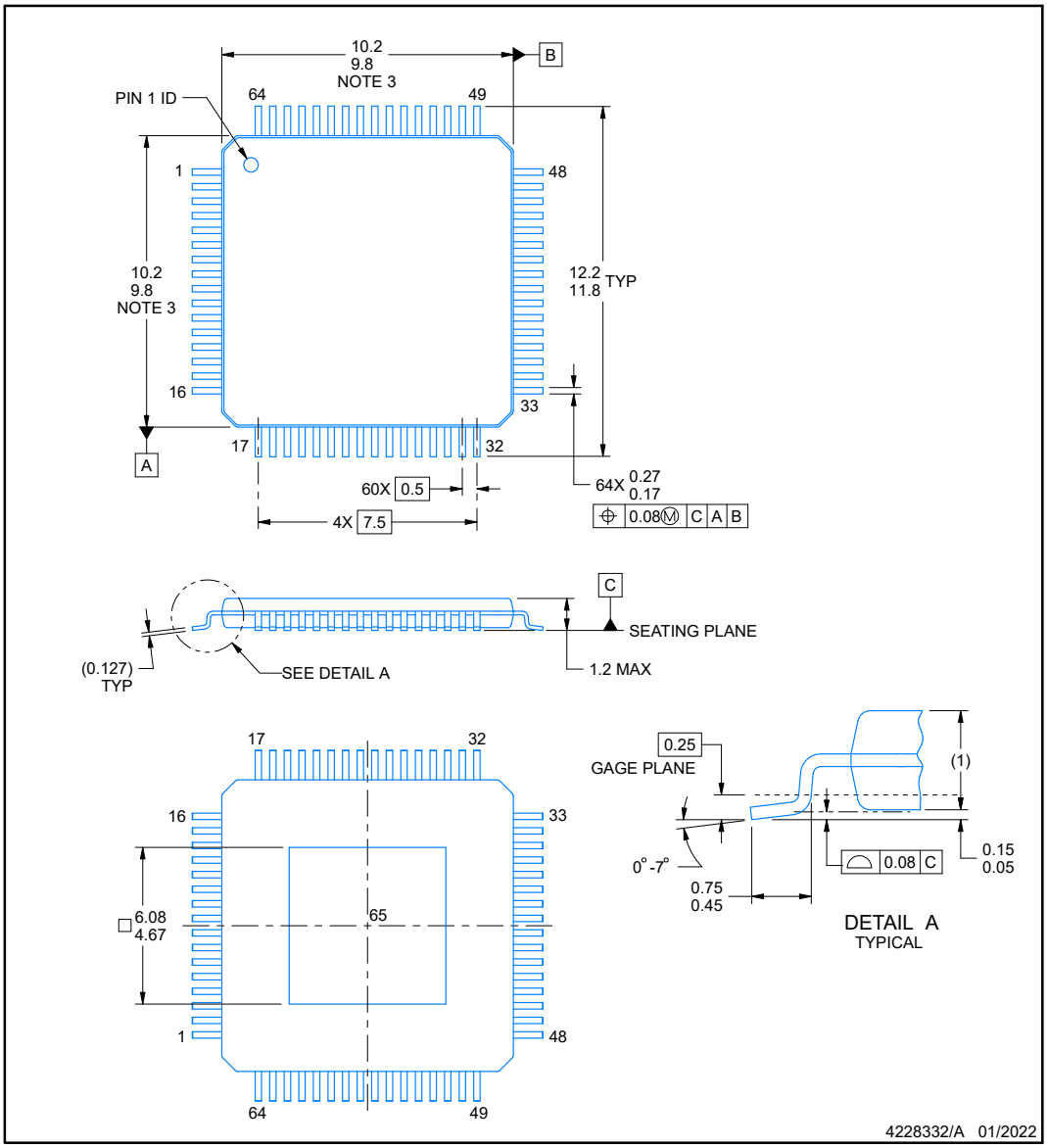
PACKAGE OUTLINE

PAP0064E



PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLAT PACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

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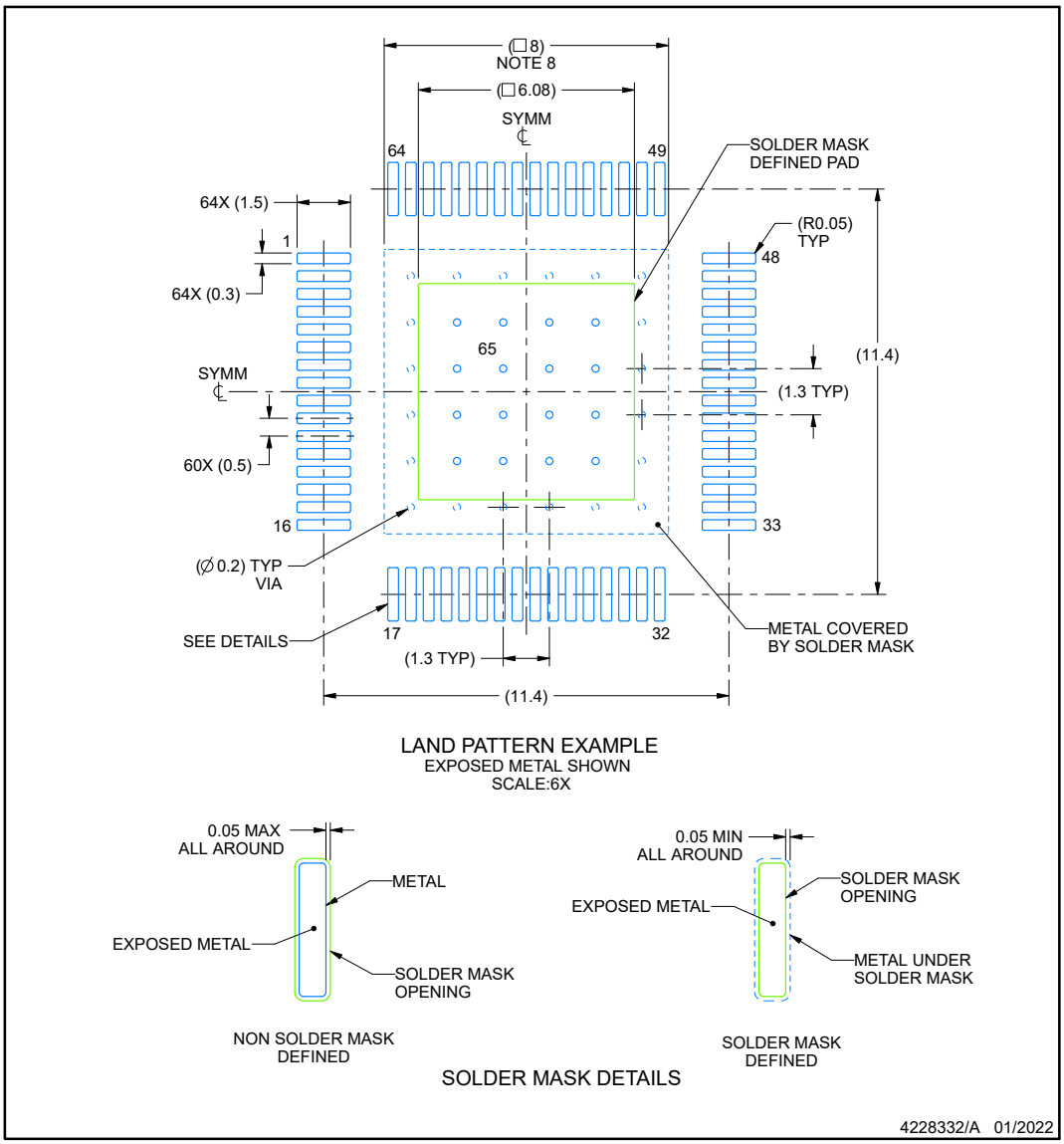
EXAMPLE BOARD LAYOUT

PAP0064E **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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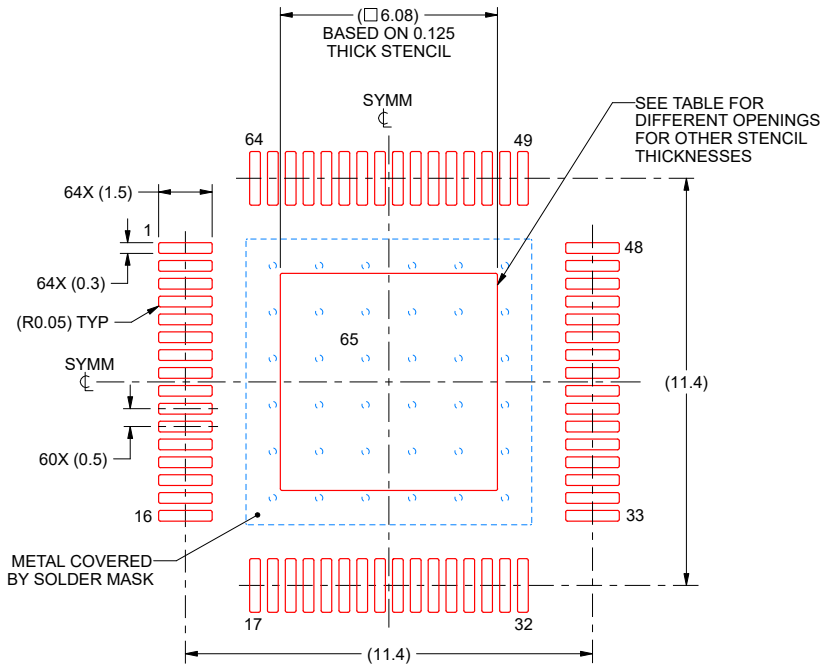
EXAMPLE STENCIL DESIGN

PAP0064E **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2321001PXE	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	5962R23210 01PXE
PLMX2624PAP/EM	Active	Preproduction	HTQFP (PAP) | 64	250 | SMALL T&R	-	Call TI	Call TI	25 to 25	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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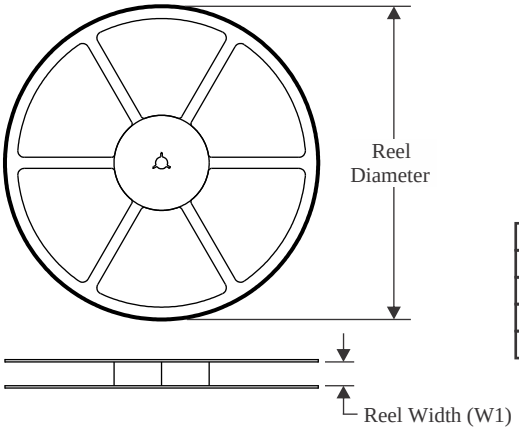
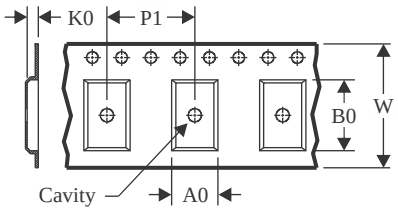
TAPE AND REEL INFORMATION

REEL DIMENSIONS

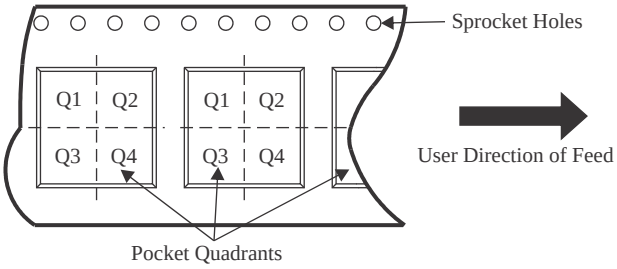


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

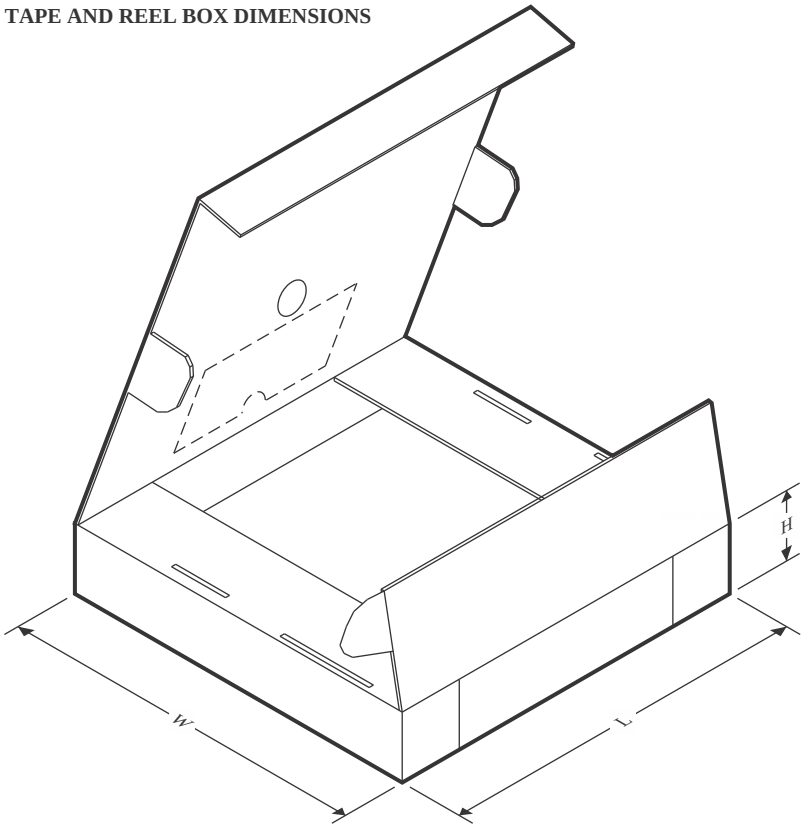
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962R2321001PXE	HTQFP	PAP	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962R2321001PXE	HTQFP	PAP	64	250	367.0	367.0	55.0

GENERIC PACKAGE VIEW

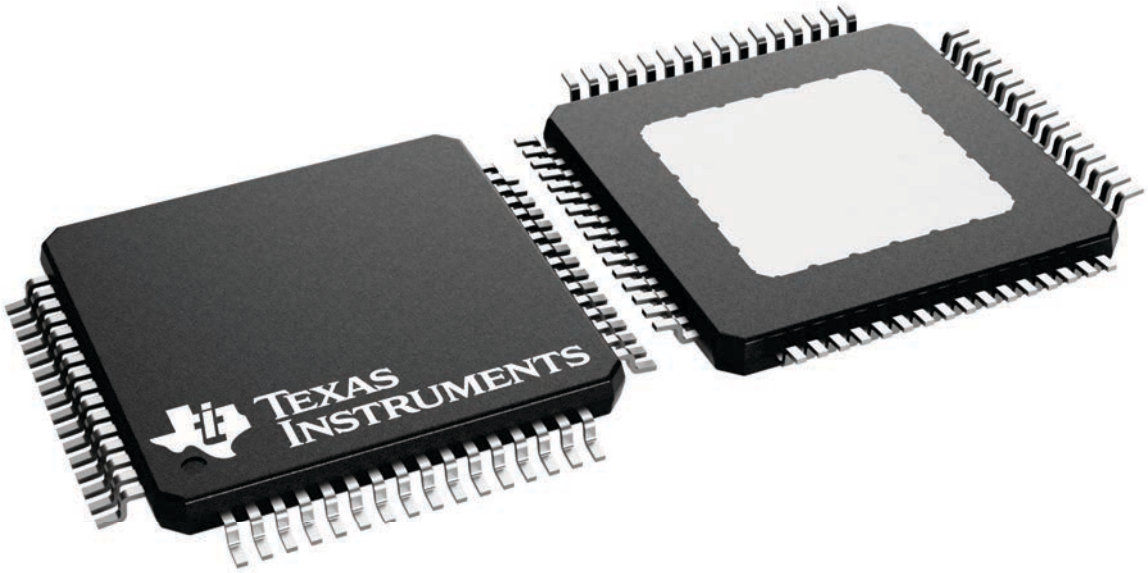
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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