Application Note

FPD-Link ADAS Power-Over-Coax Design Guidelines

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Abstract

Automotive applications continue to advance with new features such as 360-degree eye views and interior vehicle monitoring to check for driver awareness. To support these features multiple cameras must be installed around and within the vehicle, with each camera requiring additional hardware and cabling components. FPDLink devices can simplify automotive system designs by transmitting both video data and power over a single standard coaxial cable between the camera and serializer. This decreases weight, removes the need for separate power supplies, and minimizes cabling costs.

This application note outlines design requirements and guidelines for implementing an FPD-Link ADAS system based around a Power-over-Coax (PoC) network. The application note also provides several TI reviewed PoC networks for use with FPD-Link IV and III devices.

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1 Introduction

Advanced driver assistance systems (ADAS) have become increasingly more complex including applications such as driver monitoring, driver assistance features, and in some cases autonomous driving. These systems often use multiple types of sensors and cameras spread across various locations of the vehicle. As the number of sensors and cameras continue to increase, the total length and number of cables required to transfer the high-speed data and power signals will increase as well. This results in extensive cabling, which is costly and can complicate system implementation.

FPD-Link SerDes chipsets eliminate the need to have a separate cable to deliver power from the deserializer board to the serializer and sensor, which allows ADAS systems to support an increased number of sensors without an extensive amount of cabling. This is achieved by using Power over Coax (PoC) filters to separate DC power from the high speed FPD-Link signal, allowing power to be transferred over the same coax cable as the FPD-Link data.

2 Theory of Operation for Power Over Coax

The purpose of a Power over Coax network is to separate the high-speed data signal from the DC power signal. The high-speed signal content consists of a high-speed forward channel carrying video and control data to the deserializer and a lower speed back channel carrying control data to the serializer. Figure 2-1 shows a high-level overview of how FPD-Link and DC power share a single coax cable. For proper separation the DC component of the FPD-Link signal must be completely blocked from entering the DOUT pins of the serializer and the RIN pins of the deserializer. This is accomplished by placing AC Coupling capacitors in line with the FPD-Link signal path, which blocks the DC signal and passes the forward and back channel signals. A simple capacitor can work for this since a simple capacitor has very low impedance over the forward and back channel frequency and is an open circuit at DC.

The PoC network is a type of low pass filter circuit that is designed to pass the transmitted DC signal with minimal interference on the high-speed AC signal. For this low pass filter circuit to not interfere with the high-speed signal, the circuit needs to have an impedance much larger than the characteristic impedance of the channel. It is recommended that an impedance of 1 kΩ be met over the entire FPD-Link operational frequency band.

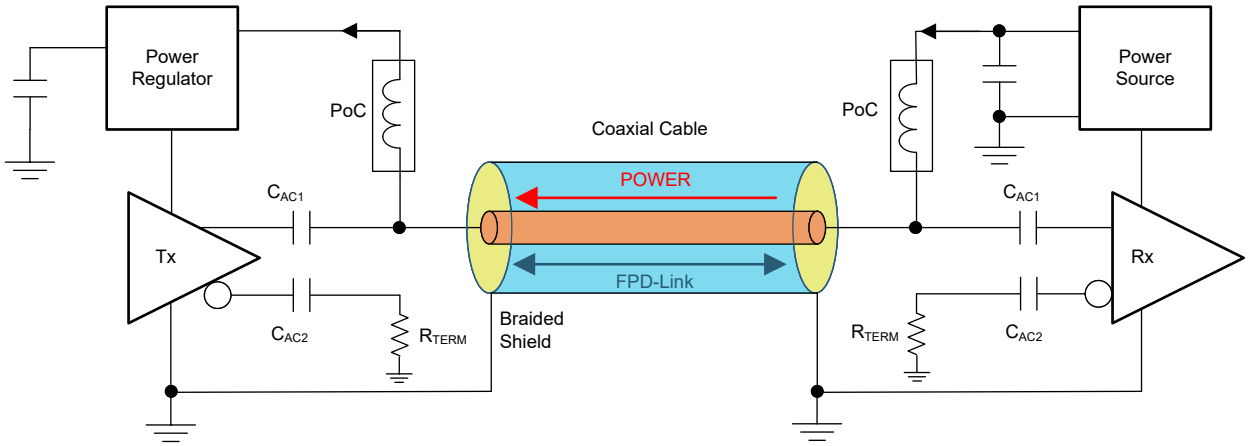


Figure 2-1. PoC Theory of Operation

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2.1 Inductor Characteristics

An ideal inductor is capable of blocking all AC frequencies and passing all DC power. However, inductors have characteristics that make them behave less like an inductor in extreme circumstances. Real-world inductors behave more closely to the circuit shown in Figure 2-2 with parasitic capacitance and resistance components. At low frequencies, the capacitor acts like an open circuit with high impedance, and the inductor acts like a short circuit with low impedance. At very high frequencies, the capacitor acts like a short circuit, at which point the impedance is equal to RL.

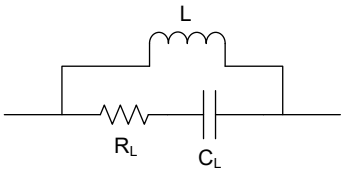


Figure 2-2. Real World Inductor

The impedance peaks at the self-resonant frequency (SRF) where the inductor and capacitor resonate. At frequencies past the SRF, the parasitic capacitance takes over and lowers the impedance. The SRF can be calculated using Equation 1, where L is the inductance, C is the parasitic capacitance, and F is the resonant frequency. These values are typically listed on the component's data sheet.

$$F = \frac{1}{\sqrt{LC}} \tag{1}$$

The impedance of a 100uH inductor is shown in Figure 2-3 where the black line shows the impedance of an ideal inductor before the SRF and the red line shows the impedance of the parasitic capacitance after the SRF.

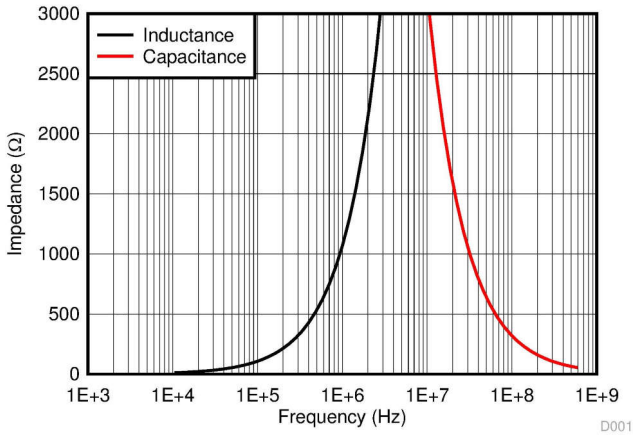


Figure 2-3. SRF Impedance Plot

Figure 2-3 shows that for a 100µH inductor, the impedance rises above 1kΩ at about 1 MHz and drops below 1kΩ above frequencies of about 30MHz. Although not strictly required, an impedance above 1kΩ is recommended as high impedance correlates to lower signal loss. For this reason, a more complex low pass filter is required to raise the impedance over the entire FPD-Link bidirectional signaling frequency range.

To increase the impedance of the circuit over the entire operational frequency range, additional inductive components of different values can be added in series. Compared to the 100µH inductor the 4.7µH inductor has a higher SRF but still does not achieve a high impedance across a large frequency range. However, when used in series, the impedance remains above 1kΩ from about 1MHz to well over 500MHz.

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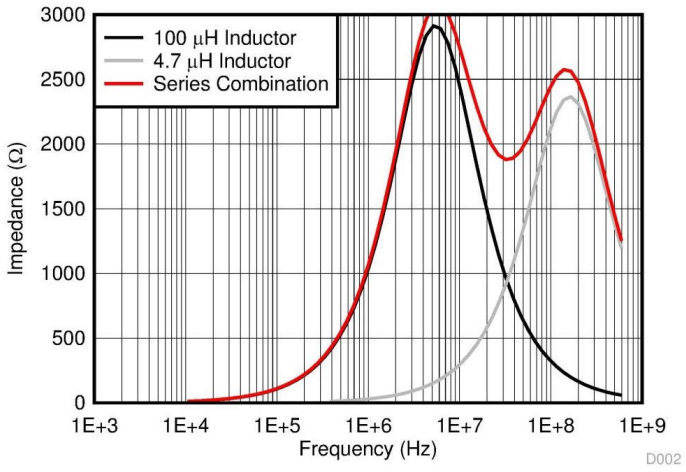


Figure 2-4. Impedance of Series Inductors

By cascading inductors in series, the user can build a wide-bandwidth inductor that can cover the frequency range of the back channel all the way to the frequency of the forward channel. This is demonstrated further in Figure 2-5 and Figure 2-6. Figure 2-5 shows impedance graphed for individual inductors of various values. The individual inductors do not provide an impedance of 1kΩ over a wide frequency range. However, Figure 2-6 shows that when combined, the inductors provide consistent impedance of 1kΩ over a large frequency range.

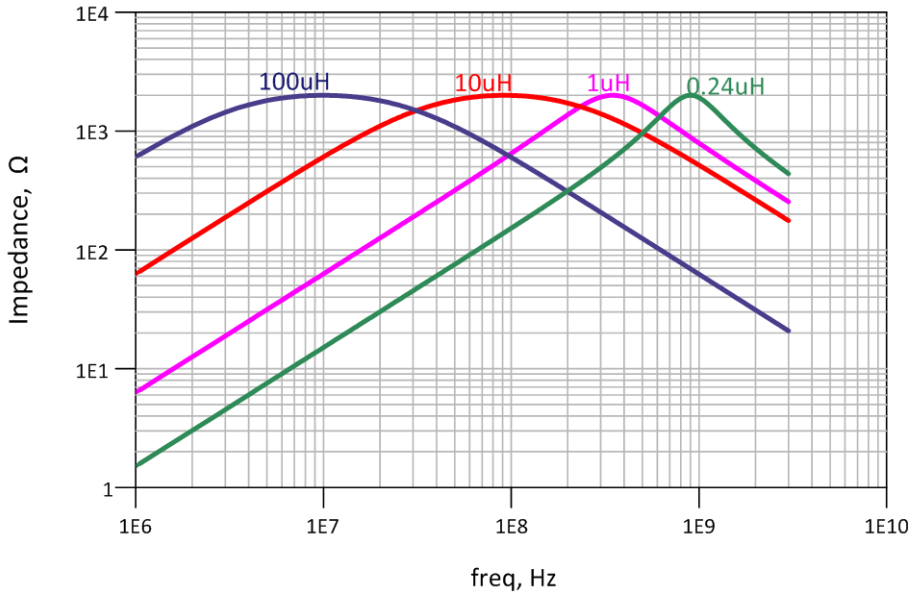


Figure 2-5. Impedance of Individual Inductors

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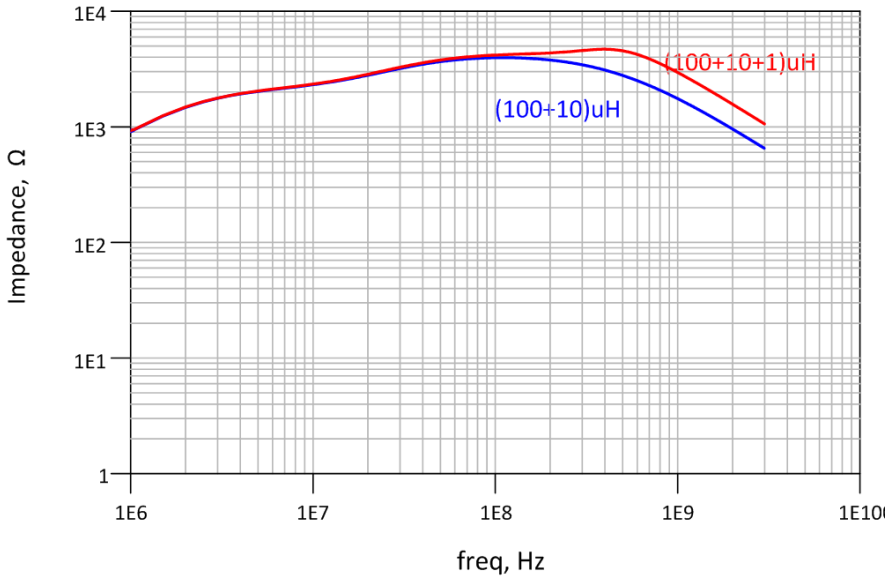


Figure 2-6. Impedance of Combined Inductors

An additional consideration when working with real-world inductors is the saturation current. Inductors store electrical energy in the form of a magnetic field. The strength of the magnetic field is correlated to the current flowing through the inductor. The saturation current is the maximum current that can be supported before the inductor ceases to behave like an ideal inductor. When implementing a PoC network, it is crucial to verify that the operating conditions do not exceed the max rated electrical characteristics of any component.

2.2 Capacitor Characteristics

Figure 2-7 shows a representative model of a real-world capacitor component. A capacitor has an accompanying parasitic resistance and inductance, and at very high frequencies the inductance takes over and the capacitor no longer behaves like a capacitor. If the impedance of the capacitor is plotted across a frequency range, the result looks similar to Figure 2-3 but flipped horizontally with the lowest impedance occurring at the resonant frequency

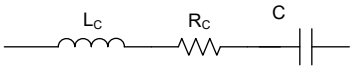


Figure 2-7. Real World Capacitor

Capacitors are used in the PoC network for decoupling the input of DC regulators on the serializer side of the link. The input capacitance of the DC regulator is based on both the FPD-Link serializer and DC regulator recommendations found in the device data sheets. The chosen capacitors must have appropriate voltage and temperature ratings for the system. Similarly to how the inductors are cascaded in series to create a wide-bandwidth inductor, capacitors can be cascaded in parallel to create a wide-bandwidth capacitor, or a capacitor that can pass a larger frequency range and better decouple the DC regulators. Often times when choosing a decoupling capacitor, the capacitor can be treated as an ideal capacitor because noise from the DC regulators is at a much lower frequency than the signal frequency trying to be blocked. Equation 2 shows the impedance of a capacitor as a function of frequency, where Z is the impedance in Ohms, f is the frequency in Hertz, and C is the capacitance in Farads.

$$Z = \frac{1}{\sqrt{2\pi f C}} \tag{2}$$

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2.3 Inductors versus Ferrite Beads

As the frequency of FPD-Link communications rise, the need for more complex PoC networks follows. Ferrite beads can help greatly when dealing with extremely high frequencies. Ferrite beads are considered a special kind of inductor that has a very low inductance but are rated for frequencies in the MHz to GHZ range. Where standard coil inductors typically begin behaving like a capacitor, a ferrite bead continues to provide high impedance. Figure 2-8 shows a real world ferrite bead that has an inductive component, capacitive component, and resistive components. The Ferrite bead is primarily inductive, therefore L_{FB} is the most dominant portion of this model. The parasitic capacitance C_{Par} does not become significant until very high frequencies.

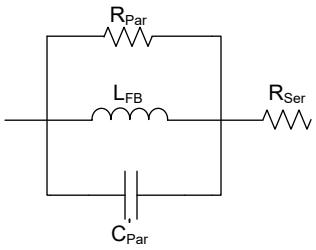


Figure 2-8. Real World Ferrite Bead

Adding ferrite beads to the PoC network can result in broader frequency coverage. However, a ferrite bead can have a higher resistive component at DC than a standard coil inductor. While the resistance is typically rather small (<1Ω), higher DC resistance can result in significant IR drop in applications where current is drawn.

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3 Design Considerations

There are two main functional factors to consider when selecting a PoC network: device operational frequency range and power consumption of the serializer or imager board.

3.1 Frequency Range

To design an appropriate PoC network, consider the frequency range that the network must be able to filter. For example, an FPD-Link IV system using the DS90UB971-Q1 and DS90UB9702-Q1 running in synchronous mode can support a forward channel rate of 7.55Gbps (3.775GHz) and a back-channel rate of 47.1875MHz. The PoC network must effectively filter a frequency range from half the back-channel frequency to the forward channel frequency.

Table 3-1 shows each serializer device compatible with the DS09UB9702-Q1 and their forward and back channel communication frequencies when paired with the DS90UB9702-Q1 using the default back-channel rate settings. The last column shows the frequency range that the PoC network must be able to filter.

Table 3-1. Serializer Frequency Ranges

Deserializer	Serializer	Mode	BC Frequency	FC Frequency	PoC Filter Frequency Range
DS90UB9702-Q1	DS90UB913A-Q1	Non-Synchronous	2.36MHz	700MHz	1.18MHz - 700MHz
	DS90UB933-Q1	Non-Synchronous	2.36MHz	933MHz	1.18MHz - 933MHz
	DS90UB951-Q1	Non-Synchronous	9.44MHz	2.43GHz	4.72MHz - 2.43GHz
	DS90UB935-Q1	Synchronous	47.19MHz	1.89GHz	23.59MHz - 1.89GHz
		Non-Synchronous	9.44MHz	2.08GHz	4.72MHz - 2.08GHz
	DS90UB953-Q1	Synchronous	47.19MHz	1.89GHz	23.59MHz - 1.89GHz
		Non-Synchronous	9.44MHz	2.08GHz	4.72MHz - 2.08GHz
	DS90UB971-Q1	Synchronous	47.19MHz	3.775GHz	23.59MHz - 3.775GHz
		Non-Synchronous	9.44MHz	3.775GHz	4.72MHz - 3.775GHz

3.2 Power Considerations

Each PoC network has a maximum current rating based on the saturation characteristics of the components. As discussed in Section 2.1, inductors saturate, dissipate heat, and pass very high frequencies when the maximum current rating is not respected. The individual operating specifications of every PoC component must be followed to provide proper filtering.

The PoC network must have a current rating that allows for an appropriate amount of power to be supplied to the serializer and sensor. The maximum power drawn by the serializer board can be calculated from the worst-case scenario power consumption of the serializer side of the link. An example of a potential maximum power consumption scenario is a period where the sensor is actively gathering data and all other remote devices are operating. Please note that the worst-case scenario and maximum power consumption is system dependent and can vary across designs. The IR drop due to the parasitic impedance of the individual components and cables must also be considered. TI recommends several different PoC networks capable of different levels of power delivery. The chosen PoC network must be capable of supplying enough current and power from the given PoC voltage for the serializer and sensor.

3.3 Resistance Considerations

Resistance in the PoC power path can cause significant power loss, especially when there is a large amount of current being drawn in the system. Power loss can be minimized by increasing the PoC voltage level and reducing the amount of current being sent through the PoC network. But for applications that do not have a high voltage rail available or do not include components that can handle high voltages, reducing current draw may not be possible. The only alternative is to reduce resistance in the PoC power path.

There are three main factors that contribute to resistance in the power path.

1. DC resistance (DCR) of the inductors in the PoC network
2. Resistance of the cables

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3. Resistance of the PCB traces

Each inductor has a max DCR specification in the data sheet. This DC resistance can add up to a significant total resistance across two PoC networks being used in a full system. Typically, smaller inductors have higher DCR than larger inductors. Check the data sheet of each inductor and choose components that have a balance between the desired size of the overall PoC network and the allowable loss in the total power system. See Section 6 for a list of PoC networks and inductors reviewed by TI.

Cables introduce a small amount of resistance in the total power path. Cable data sheets quantify resistance in units of ohms per kilometer. Depending on the cable type and the length of the cable, the total resistance of the cable can be calculated. Typically, thicker cables have less resistance per kilometer than thinner cables. Please check the cable data sheet for full details.

The PCB traces also add a small amount of resistance in the power path. The equations below can be used to estimate the resistance for the PCB portion of the system:

$$R_{ref} = \left(\rho * \mathrm{L}\right) / \left(\mathrm{t} * \mathrm{W}\right) \quad (3)$$

$$R_{op} = R_{ref} * \left[1 + \alpha * \left(T_{op} - T_{ref}\right)\right] \quad (4)$$

R_{ref} = The total electrical resistance of the PCB trace (assuming 20°C for room temperature)

ρ = The intrinsic electrical resistivity of the conducting material. This characteristic is affected by temperature. At 20°C, the resistivity of copper is typically 1.68x 10^{-8} Ω·m.

L = Length of the trace (meters)

t = Thickness of the trace. 1 ounce of copper thickness is typically 35µm thick (0.000035 meters)

W = Width of the trace (meters)

R_{op} = The total electrical resistance of the PCB trace at a specific operating temperature.

α = Temperature coefficient of resistivity for the conducting material (0.00393 for copper)

T_{op} = Operating temperature of the system

T_{ref} = Reference temperature (20°C for room temperature)

3.4 Inductor Size Considerations

Although not required for functionality, some systems have size constraints that must be considered when designing a PoC network. The values of the inductors used are based on the impedance and filtering needs of the system, but the physical size of the inductors is dependent on the ability of the device core to sustain the magnetic field. Physically smaller inductors have lower saturation currents and limit the current rating of the PoC network. One way to safely use an inductor with a lower saturation current is to reduce the current requirement of the circuit by increasing the voltage being carried by the coax cable. For example, if the camera or sensor requires 1.5W and a PoC voltage of 5V is used, a current of 300 mA must be supported. However, if a PoC voltage of 12V is used, a current of only 125mA must be supported. The lower current requirement allows for an inductor with a lower saturation current and potentially smaller footprint to be used.

3.5 Layout Considerations

The layout of the PoC network is equally important as the network design. Due to the PoC network components making direct contact with the high-speed signal trace, good layout techniques and component placement are crucial to maintain signal integrity and remain within the insertion loss and return loss requirements. Both the high-speed channel and PoC network require tightly controlled 50Ohms (+/-10%) impedance to minimize reflections. In addition to impedance, the PCB traces need to be thick enough to support the maximum expected current load.

Place the first inductive component of the PoC network orthogonally to be barely touching the high-speed RIN+ trace. An anti-pad must be added under the first component to keep the impedance as close to 50-Ohms as possible. The anti-pad is created by adding a cut-out to the ground plane directly underneath the component's

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landing pad. Since a continuous ground reference is required for the high-speed and PoC traces, the cut-out must not include any area under the connecting trace. Place the remaining PoC components close together to minimize the total footprint of the PoC network and limit 90-degree routing. For best EMI performance, do not route any high-frequency signals, including the PoC network, near the edge of the PCB board. Figure 3-1 shows an example PoC PCB layout with many of the previously described recommendations highlighted.

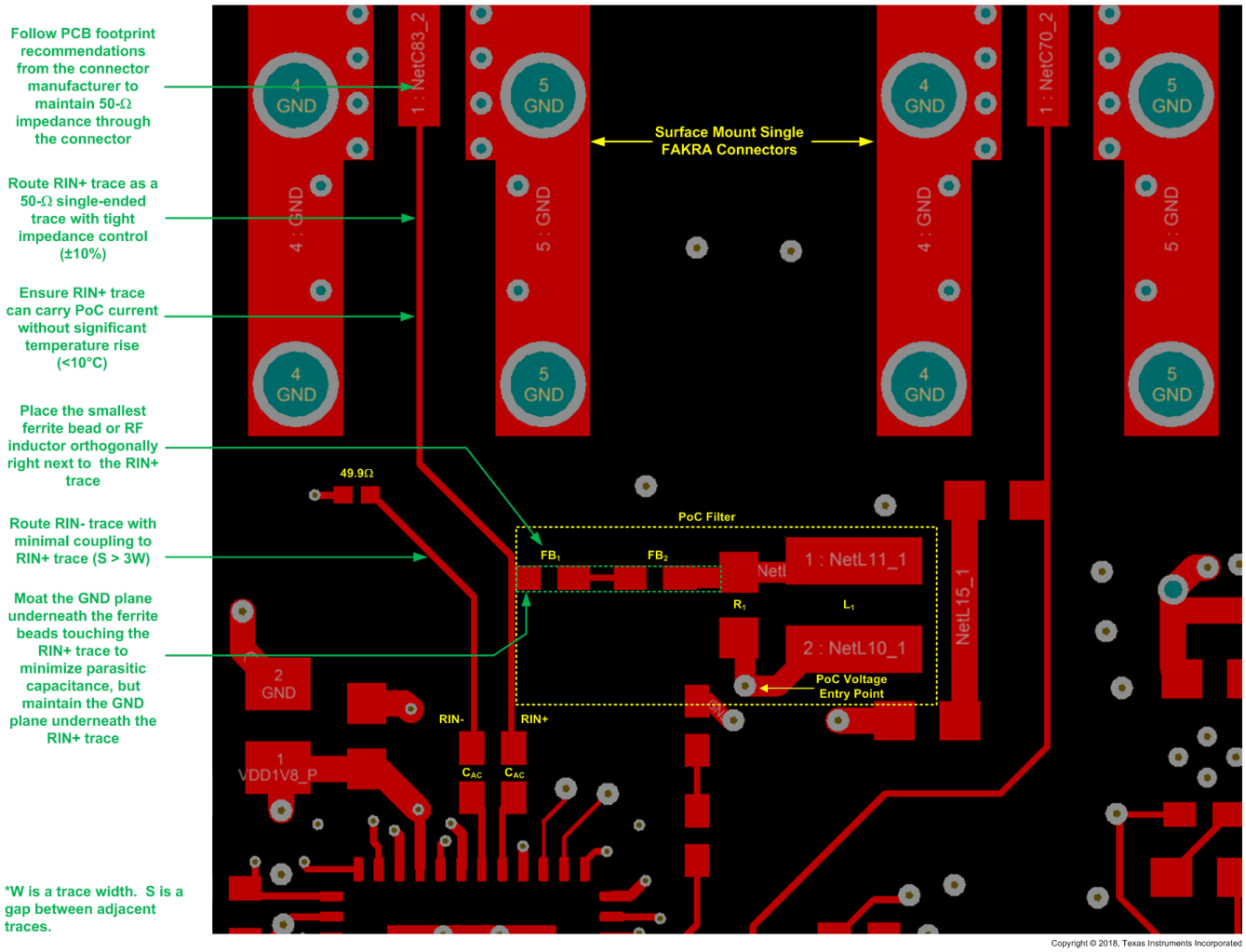


Figure 3-1. Example PoC Layout and Routing

Keeping the entire PoC network on the same layer as the high-speed RIN+ trace is recommended since vias can result in impedance discontinuities. However, if space constraints arise, all components other than the first inductive component can be routed to a layer other than the layer with the high-speed trace. To maintain the 50Ohm impedance, add ground reference vias near all signal vias. When sending signals between layers, care needs to be taken to avoid creating stubs. A stub is any transmission line that is only connected at one end. Stubs are commonly created by vias, routing, or through-hole connectors, which create reflections and degrade the signal quality.

For additional recommendations, refer to device datasheets.

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4 FPD-Link PoC Requirements

When incorporating a PoC network into a system, the user must make sure that any PoC network chosen meets TI's channel specifications and PoC noise requirements to provide robust operation across all component tolerances and operating conditions.

4.1 Channel Requirements

For error-free communication between FPD-Link devices, the return loss and insertion loss on the high-speed channel must be within the limits defined by TI under worst-case current load and temperature conditions. The high-speed channel includes the serializer PCB, cable, and deserializer PCB. A PoC network is only one part of the PCB budget and overall total channel requirement. The traces on each PCB, connectors, as well as any components touching the high-speed trace can all impact loss on the channel. For this reason the layout and quality of the selected components and cables are paramount.

TI defines the channel requirements in terms of budgets for the total channel, PCB, and cable, where total channel is a combination of the PCB and cable budgets. Although meeting both the PCB and cable budgets individually is recommended, the main requirement is meeting the total channel budget. This allows for some flexibility as a PoC network that slightly violates the PCB budget, can still meet the total channel budget if a shorter or more high-quality cable is used to compensate for the additional loss. Similarly, if a lossy cable violates the cable budget, the total channel loss requirement can still be met if the PCB design results in additional margin within the PCB budget. As long as the combined PCB and cable loss is within the total channel budget, the channel specifications are considered met. However, meeting each budget with as much margin as possible is recommended. When evaluating the insertion and return loss via simulation or measurements, the system must be stressed under the maximum temperature conditions and current load.

The return loss requirement protects against signal degradation. Return loss refers to the amount of reflections in the link seen by the transmitter. A network typically fails the return loss requirement when there is an impedance mismatch in the channel. A network can also fail when inductors and ferrite beads have been chosen incorrectly. Return loss can be calculated using the following equation:

$$Return\ Loss(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (5)$$

Following the FPD-Link and PoC layout guidelines from the data sheet is important to make sure the return loss requirement is met. If a board has already been designed and does not meet return loss requirements, a TDR test can be useful to help locate the area of the board where impedance mismatches occur. The return loss requirement for a FPD-Link III coax application is given in Table 4-1. For robust operation of the system, the return loss must be less than the listed values over the operating frequency range of the system. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device and mode of operation.

Please note that the Channel Specifications document defines the loss and noise limits for each individual FPD-Link device and mode of operation. It is subject to change without notice.

Table 4-1. FPD3 Return Loss Requirement

Frequency	PCB Budget (dB)	Total Budget (dB)	Cable Budget (dB)
1 – 100MHz	-20	-16	-20
0.1 – 1GHz	-12 + 8×log(f[GHz])	-9 + 7×log(f[GHz])	-12 + 8×log(f[GHz])
1 – 3.775GHz	-12	-9	-12

Insertion loss refers to the amount of power the signal loses as the signal travels through the channel. Causes of insertion loss requirements not being met are typically due to signal attenuation in the channel and can be calculated using Equation 6.

$$Insertion\ Loss(dB) = -10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (6)$$

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If meeting insertion loss requirements is an issue, verify that all board layout and PoC guidelines provided by TI are being followed and high quality components are used in the signal transmission and PoC. The insertion loss requirement for a FPD-Link III coax application is given in Table 4-2. For robust operation of the system, the insertion loss must be greater than the values listed over the operating frequency range of the system. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device and mode of operation.

Table 4-2. FPD3 Insertion Loss Requirement

Frequency	PCB Budget (dB)	Total Budget (dB)	Cable Budget (dB)
1MHz	-0.35	-1.4	-0.7
5MHz	-0.35	-2.3	-1.6
10MHz	-0.35	-2.5	-1.8
50MHz	-0.35	-3.5	-2.5
100MHz	-0.35	-4.5	-3.9
500MHz	-0.35	-9.5	-8.7
1GHz	-0.6	-14	-12.8
2.1GHz	-1.2	-21.6	-19.2

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5 PoC Noise

5.1 PoC Noise Requirements

PoC networks must be designed with the integrity of the high-speed signal in mind. The network cannot interfere with data transmission, and the DC signal must have as little noise as possible. Noise seen on the PoC voltage supply and the deserializer RIN+ pin are particularly important and must remain below the recommended conditions. Figure 5-1 shows the measurement nodes of the VPoC and RIN+ noise relative to the system.

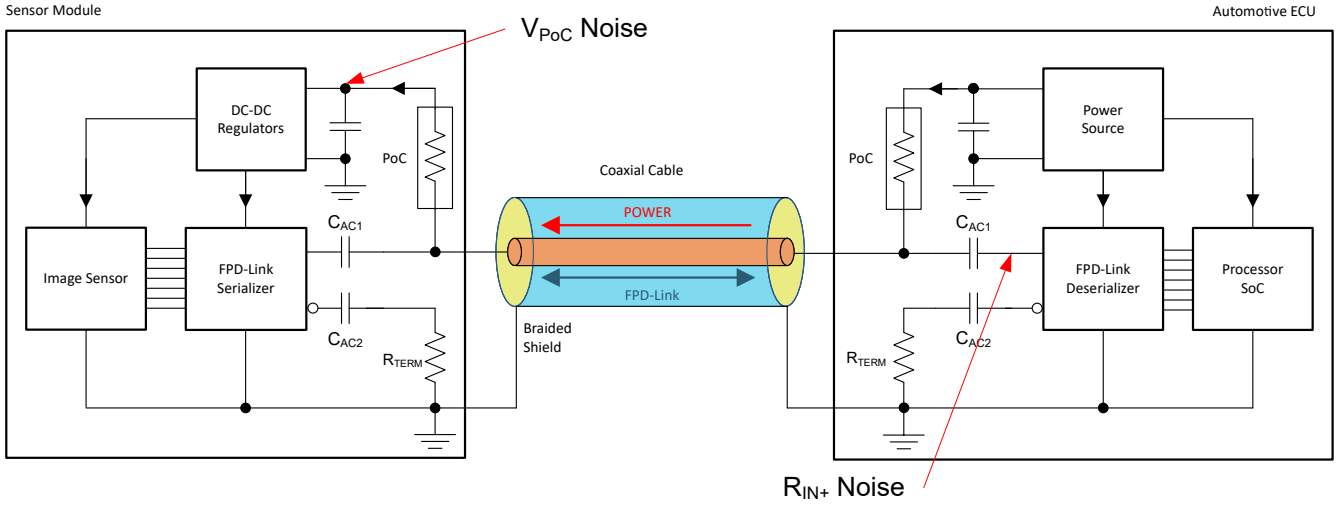


Figure 5-1. PoC Noise Measurement Nodes

5.2 Measuring V_{PoC} Noise and Pulse

V_{PoC} noise is the measurement of noise introduced into the system from serializer and sensor operation. Figure 5-2 shows a typical waveform measured from the input of the DC regulators. The supply noise is introduced from the switching of DC buck regulators, and the pulse is due to the switching of the sensor. During periods of blanking, the current draw from the sensor is significantly lower than during active periods, which causes the voltage to spike.

5.2.1 Requirements

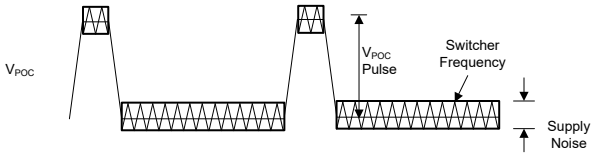


Figure 5-2. V_{PoC} Noise

The VPoC must meet the following requirements for proper FPD-Link operation.

- V_{PoC} supply noise must be less than 100mV peak-to-peak
- V_{PoC} pulse must be less than 500mV peak-to-peak (from image sensor blanking and valid periods)
- V_{PoC} pulse slew rate must be greater than 200us/V

5.2.2 Measurement Procedure

1. Connect serializer to deserializer through coax
2. Measure the noise floor of the oscilloscope by shorting the probe to ground
3. Power the entire system (sensor, serializer, deserializer, and so on)
   a. Verify the image sensor is configured to capture video data
4. Set oscilloscope bandwidth to 0 – 50MHz
5. Probe V_{PoC} at input of DC regulators on serializer board
6. Subtract noise floor measurement from V_{PoC} noise measurement

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5.3 Measuring R_{IN+} Noise

5.3.1 Requirements

RIN+ noise is the noise measured on the deserializer board at the input of the RIN+ pin.

- R_{IN+} noise must be less than 10mV peak-to-peak between 0 and 50MHz.

5.3.2 Measurement Procedures

To accurately measure RIN+ noise in the system, the image sensor and all other load carrying devices on the serializer side must be actively drawing current. The forward channel and back channel transmissions generated by the connected serializer and deserializer must also be disabled to prevent interference in the noise measurements. To disable the forward channel and back channel transmissions, the PDB pin on the serializer and deserializer devices must be pulled to GND. The image sensor is expected to contribute to the RIN+ noise when actively capturing video data. Therefore if the image sensor is not enabled at the time of measurement, the results do not accurately represent the RIN+ noise of the system. An example of the RIN+ noise measurement procedure is listed in the following:

1. Rework the serializer and deserializer boards such that the PDB pin on the serializer and deserializer are both pulled to GND for the duration of the measurement
2. Solder wire connections from the I2C bus (SCL, SDA, GND) on the serializer board to an external I2C Controller
3. Connect the serializer and deserializer boards using a coax cable
4. If not determined previously during VPoC measurement, measure the noise floor of the oscilloscope by shorting the probe to ground
5. Power the entire system (sensor, serializer, deserializer, and so on)
6. Configure the image sensor locally through the external I2C controller and confirm that video is being generated
7. Set oscilloscope bandwidth to 0 – 50MHz
8. Probe RIN+ noise at a point closest to the IC pin using a short probe tip for measuring ground
9. Account for noise floor by subtracting the noise floor measurement from the RIN+ noise measurement

5.4 Causes of PoC Noise

There are various system level factors that impact the noise seen on a PoC network. Some potential sources of PoC noise are listed below.

- Switching regulators – Switching regulators switch the output on and off at a high frequency to step a high voltage DC signal down to a lower voltage. This switching is back fed through the regulator to the input V_{PoC}. The switching frequency is typically in the range of kHz and can travel through the PoC network, degrading the signal-to-noise ratio.
- Image sensors – Sensors can introduce noise into the system at the frame rate of the sensor due to the varying power demands. This demand peaks during the gathering of valid frame data and drops during the blanking period. This low frequency noise can more easily travel through the PoC network which is designed to block frequencies in the MHz to GHz range.
- Poor Board Layout – Not following the guidelines in the data sheet for board layout can lead to signal degradation and extra noise in the system.
- Environmental Noise – Environmental noise is from the surroundings and can behave like white noise. This can impose noise at all frequencies across the spectrum.

5.5 Noise Measurement Best Practices

Proper probing technique is critical to minimize any potential interference or measurement noise when conducting PoC noise measurements. When probing the deserializer board to measure the RIN+ noise of the system, probing the RIN+ pin directly on the IC is recommended. Additionally, ground the probe by accessing the ground plane near the pin directly on the PCB board. Grounding close to the pin helps minimize the ground loop and reduces measurement noise. The probe used to collect noise measurements can also impact the results. Select a probe such that the path to ground is as short as possible. For example, ground the probe using a short ground spring rather than an alligator clip or other types of large clips. This minimizes the ground loop and reduces measurement noise. When measuring noise, it is important that the system under test is an

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accurate representation of the final operational system. The intended cable type and length must be used with the deserializer, serializer, and imager all configured to operate in the intended operational mode.

5.6 Reducing Effects of PoC Noise

Switching regulators are large contributors to PoC noise. To reduce the effect, TI recommends using low-dropout regulators (LDOs) wherever possible because an LDO does not generate any noise from switching. In the case where an LDO cannot be used and a switching regulator is required, switching noise introduced into the system must be taken into account. To reduce the switching noise, TI recommends using a high PoC voltage. As the PoC voltage rises, current consumption by the switching regulator is reduced, therefore reducing the noise introduced from switching.

Another way to reduce the effect of noise is to use a switching regulator with a higher switching frequency. A higher switching frequency increases the effectiveness of the decoupling capacitors because the impedance is lowered as frequency increases.

Figure 6-1 shows decoupling capacitors C1 and C2; with higher switching frequency these capacitors become more effective. Finally, increasing the decoupling capacitance at V_{PoC} can help to better filter any high frequency noise introduced by the regulator. Equation 2 shows the impedance of a capacitor as a function of frequency where Z is the impedance in Ohms, f is the frequency in Hertz and C is the capacitance in Farads. The capacitance and frequency are in the denominator, which means increasing either value decreases the impedance and therefore shorts high frequencies to ground. When choosing decoupling capacitors, select high quality capacitors rated for the voltage and temperature range required. Some capacitors can significantly degrade when operated near the rated voltage. Sometimes the capacity can drop as low as 20 – 40% of the nominal rating. For this reason, TI recommends selecting capacitors with a voltage rating 2x or 3x the voltage being used to avoid any unexpected drop in capacitance. The derating characteristics of the capacitor at DC bias voltage can be confirmed on the capacitor manufacturer website.

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6 TI Reviewed PoC Networks

This section provides all of the PoC networks that TI has reviewed. Each design is optimized to add minimal Insertion Loss and Return Loss onto the attached high-speed trace, within the listed operating frequency and stress conditions. TI recommends selecting one of the networks based on the desired frequency range, current rating, and temperature.

If there is not a suitable design listed in this application note, TI recommends reaching out to a coil vendor directly to request a customized PoC network that can meet specific system requirements. Below is a list of vendors that TI has partnered with:

- Murata
- TDK
- Coilcraft
- Cyntec
- Tai-Tech

Make sure to confirm that the high-speed PCB traces with the custom PoC network are still able to meet the defined loss and noise limits for FPD-Link devices. Contact TI for more information on the required Channel Specifications defined for each individual FPD-Link device. A separate Channel Specifications document is available, depending on the deserializer and serializer used in a system.

Table 6-1. Reviewed Networks Operating Ratings

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
N/A	FPD3	From FPD-Link III data sheet	25MHz – 2.1GHz	250mA	105°C
Murata	FPD3	Murata FPD3 Design 1	5MHz - 2.1GHz	800mA	105°C
				700mA	125°C
	FPD3	Murata FPD3 Design 2	5MHz - 2.1GHz	600mA	105°C
				500mA	125°C
	FPD3	Murata FPD3 Design 3	5MHz - 2.1GHz	550mA	105°C
				360mA	115°C
	FPD3	Murata FPD3 Design 4	5MHz - 2.1GHz	400mA	105°C
				360mA	125°C
	FPD3	Murata FPD3 Design 5	5MHz - 2.1GHz	300mA	105°C
				200mA	115°C
				100mA	125°C
	FPD3	Murata FPD3 Design 6	5MHz - 2.1GHz	300mA	105°C
				200mA	115°C
				100mA	125°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
TDK	FPD3	TDK FPD3 Design 1	1MHz - 2.1GHz	750mA	105°C
				500mA	115°C
	FPD3	TDK FPD3 Design 2	1MHz - 2.1GHz	400mA	105°C
	FPD3	TDK FPD3 Design 3	5MHz - 2.1GHz	750mA	105°C
				500mA	115°C
	FPD3	TDK FPD3 Design 4	5MHz - 2.1GHz	600mA	105°C
	FPD3	TDK FPD3 Design 5	5MHz - 2.1GHz	500mA	105°C
	FPD3	TDK FPD3 Design 6	5MHz - 2.1GHz	400mA	105°C
	FPD3	TDK FPD3 Design 7	25MHz - 2.1GHz	1000mA	105°C
	FPD3	TDK FPD3 Design 8	25MHz - 2.1GHz	600mA	105°C
				500mA	115°C
	FPD3	TDK FPD3 Design 9	5MHz – 2.1GHz	400mA	105°C
				300mA	115°C
	FPD3	TDK FPD3 Design 10	5MHz – 2.1GHz	500mA	105°C
Coilcraft	FPD3	Coilcraft FPD3 Design 1	1MHz - 2.1GHz	950mA	85°C
				850mA	105°C
	FPD3	Coilcraft FPD3 Design 2	1MHz - 2.1GHz	700mA	85°C
				650mA	105°C
				600mA	125°C
	FPD3	Coilcraft FPD3 Design 3	1MHz - 2.1GHz	300mA	105°C
	FPD3	Coilcraft FPD3 Design 4	5MHz - 2.1GHz	950mA	85°C
				850mA	105°C
	FPD3	Coilcraft FPD3 Design 5	5MHz - 2.1GHz	800mA	85°C
				700mA	105°C
	FPD3	Coilcraft FPD3 Design 6	5MHz - 2.1GHz	600mA	85°C
				500mA	105°C
				450mA	125°C
	FPD3	Coilcraft FPD3 Design 7	5MHz - 2.1GHz	600mA	85°C
				500mA	105°C
				400mA	125°C
	FPD3	Coilcraft FPD3 Design 8	5MHz - 2.1GHz	350mA	105°C
				300mA	125°C
	FPD3	Coilcraft FPD3 Design 9	25MHz - 2.1GHz	600mA	85°C
				500mA	105°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
Murata	FPD4	Design 1	23.59375MHz – 3.775GHz	800mA	105°C
			4.71875MHz – 3.775GHz	750mA	105°C
				400mA	115°C
	FPD4	Design 2	23.59375MHz – 3.775GHz	825mA	105°C
			4.71875MHz – 3.775GHz	700mA	105°C
				500mA	115°C
	FPD4	Design 3	4.71875MHz – 3.775GHz	300mA	105°C
	FPD4	Design 4	23.59375MHz – 3.775GHz	500mA	105°C
	FPD4	Design 5	4.71875MHz – 3.775GHz	500mA	105°C
	FPD4	Design 6	1MHz – 3.775GHz	1000mA	105°C
				850mA	115°C
	FPD4	Design 7	1MHz – 3.775GHz	800mA	105°C
				700mA	125°C
	FPD4	Design 8	1MHz – 3.775GHz	800mA	105°C
				700mA	115°C
				600mA	125°C
	FPD4	Design 9	1MHz – 3.775GHz	800mA	115°C
	FPD4	Design 10	1MHz – 3.775GHz	550mA	105°C
				360mA	115°C
	FPD4	Design 11	1MHz – 3.775GHz	480mA	105°C
				300mA	115°C
	FPD4	Design 12	1MHz – 3.775GHz	300mA	115°C
	FPD4	Design 13	1MHz – 3.775GHz	300mA	115°C
	FPD4	Design 14	1MHz – 3.775GHz	300mA	105°C
				180mA	115°C
	FPD4	Design 15	4.71875MHz – 3.775GHz	1400mA	105°C
				1200mA	115°C
				1100mA	125°C
	FPD4	Design 16	4.71875MHz – 3.775GHz	1000mA	105°C
				850mA	115°C
				700mA	125°C
	FPD4	Design 17	4.71875MHz – 3.775GHz	1000mA	105°C
				700mA	115°C
	FPD4	Design 18	4.71875MHz – 3.775GHz	1000mA	105°C
				500mA	115°C
	FPD4	Design 19	4.71875MHz – 3.775GHz	1000mA	105°C
				500mA	115°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
	FPD4	Design 20	4.71875MHz – 3.775GHz	800mA	105°C
				700mA	115°C
				600mA	125°C
	FPD4	Design 21	4.71875MHz – 3.775GHz	800mA	105°C
				500mA	115°C
	FPD4	Design 22	4.71875MHz – 3.775GHz	750mA	105°C
				500mA	115°C
	FPD4	Design 23	4.71875MHz – 3.775GHz	620mA	105°C
				360mA	115°C
	FPD4	Design 24	4.71875MHz – 3.775GHz	600mA	105°C
				500mA	115°C
				400mA	125°C
	FPD4	Design 25	4.71875MHz – 3.775GHz	600mA	105°C
				400mA	115°C
	FPD4	Design 26	4.71875MHz – 3.775GHz	550mA	105°C
				490mA	115°C
				360mA	125°C
	FPD4	Design 27	4.71875MHz – 3.775GHz	500mA	105°C
				250mA	115°C
	FPD4	Design 28	4.71875MHz – 3.775GHz	400mA	105°C
				300mA	125°C
	FPD4	Design 29	4.71875MHz – 3.775GHz	300mA	105°C
				200mA	115°C
				100mA	125°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
TDK	FPD4	Design 1	4.71875MHz – 3.775GHz	300mA	115°C
	FPD4	Design 2	4.71875MHz – 3.775GHz	600mA	105°C
				300mA	115°C
	FPD4	Design 3	4.71875MHz – 3.775GHz	300mA	105°C
				200mA	115°C
	FPD4	Design 4	4.71875MHz – 3.775GHz	1000mA	115°C
				900mA	125°C
	FPD4	Design 5	4.71875MHz – 3.775GHz	600mA	125°C
	FPD4	Design 6	1MHz – 3.775GHz	300mA	105°C
				200mA	115°C
	FPD4	Design 7	1MHz – 3.775GHz	400mA	105°C
				200mA	115°C
	FPD4	Design 8	4.71875MHz – 3.775GHz	500mA	105°C
	FPD4	Design 9	4.71875MHz – 3.775GHz	750mA	105°C
				500mA	115°C
	FPD4	Design 10	1MHz – 3.775GHz	750mA	105°C
				500mA	115°C
	FPD4	Design 11	23.59375MHz – 3.775GHz	1000mA	105°C
	FPD4	Design 12	4.71875MHz – 3.775GHz	500mA	105°C
				400mA	115°C
	FPD4	Design 13	23.59375MHz – 3.775GHz	600mA	105°C
				500mA	115°C
	FPD4	Design 14	4.71875MHz – 3.775GHz	600mA	105°C
	FPD4	Design 15	4.71875MHz – 3.775GHz	400mA	105°C
	FPD4	Design 16	4.71875MHz – 3.775GHz	500mA	105°C
				400mA	115°C
	FPD4	Design 17	4.71875MHz – 3.775GHz	700mA	105°C
				600mA	115°C
	FPD4	Design 18	23.59375MHz – 3.775GHz	1000mA	105°C
	FPD4	Design 19	4.71875MHz – 3.775GHz	1000mA	105°C
	FPD4	Design 20	1MHz – 3.775GHz	350mA	115°C
	FPD4	Design 21	1MHz – 3.775GHz	400mA	105°C
	FPD4	Design 22	1MHz – 3.775GHz	500mA	105°C
	FPD4	Design 23	1MHz – 3.775GHz	750mA	105°C
	FPD4	Design 24	4.71875MHz – 3.775GHz	400mA	105°C
				300mA	115°C
	FPD4	Design 25	4.71875MHz – 3.775GHz	500mA	105°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
Coilcraft	FPD4	Design 1	1MHz – 3.775GHz	300mA	125°C
	FPD4	Design 2	1MHz – 3.775GHz	300mA	125°C
	FPD4	Design 3	1MHz – 3.775GHz	900mA	105°C
				800mA	125°C
	FPD4	Design 4	1MHz – 3.775GHz	1400mA	85°C
				1300mA	105°C
				1200mA	125°C
	FPD4	Design 5	1MHz – 3.775GHz	300mA	105°C
	FPD4	Design 6	1MHz – 3.775GHz	300mA	105°C
	FPD4	Design 7	1MHz – 3.775GHz	700mA	85°C
				650mA	105°C
				600mA	125°C
	FPD4	Design 8	1MHz – 3.775GHz	950mA	85°C
				850mA	105°C
	FPD4	Design 9	4.71875MHz – 3.775GHz	350mA	105°C
				300mA	125°C
	FPD4	Design 10	4.71875MHz – 3.775GHz	600mA	85°C
				500mA	105°C
				400mA	125°C
	FPD4	Design 11	4.71875MHz – 3.775GHz	950mA	85°C
				850mA	105°C
	FPD4	Design 12	23.59375MHz – 3.775GHz	600mA	85°C
				500mA	105°C
				450mA	125°C
	FPD4	Design 13	23.59375MHz – 3.775GHz	600mA	85°C
				500mA	105°C
	FPD4	Design 14	23.59375MHz – 3.775GHz	800mA	85°C
				700mA	105°C
	FPD4	Design 15	23.59375MHz – 3.775GHz	1000mA	105°C
	FPD4	Design 16	4.71875MHz – 3.775GHz	700mA	85°C
				600mA	105°C
				500mA	125°C
	FPD4	Design 17	23.59375MHz – 3.775GHz	1000mA	85°C
				900mA	105°C
				650mA	125°C
	FPD4	Design 18	23.59375MHz – 3.775GHz	1200mA	105°C
				950mA	125°C
	FPD4	Design 19	23.59375MHz – 3.775GHz	390mA	105°C
				300mA	125°C
	FPD4	Design 20	4.71875MHz – 3.775GHz	400mA	105°C
				300mA	125°C
	FPD4	Design 21	23.59375MHz – 3.775GHz	600mA	105°C
				450mA	125°C
	FPD4	Design 22	4.71875MHz – 3.775GHz	1700mA	105°C
				1400mA	125°C

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Table 6-1. Reviewed Networks Operating Ratings (continued)

Vendor	FPD-Link Gen Compatible	Network	Frequency Range	Current Rating	Temperature Rating
Coilcraft	FPD4	Design 23	4.71875MHz – 3.775GHz	1100mA	85°C
				950mA	105°C
				800mA	125°C
Cyntec	FPD4	Design 1	4.71875MHz - 3.775GHz	400mA	125°C
	FPD4	Design 2	4.71875MHz - 3.775GHz	600mA	115°C
	FPD4	Design 3	4.71875MHz - 3.775GHz	700mA	115°C
	FPD4	Design 4	1MHz - 3.775GHz	850mA	115°C
	FPD4	Design 5	4.71875MHz - 3.775GHz	900mA	115°C
			23.59375MHz – 3.775GHz	1000mA	115°C
	FPD4	Design 6	4.71875MHz - 3.775GHz	920mA	115°C
Tai-Tech	FPD4	Design 1	4.71875MHz - 3.775GHz	300mA	105°C
	FPD4	Design 2	1MHz - 3.775GHz	400mA	115°C
	FPD4	Design 3	4.71875MHz - 3.775GHz	500mA	105°C
	FPD4	Design 4	4.71875MHz - 3.775GHz	800mA	105°C
	FPD4	Design 5	4.71875MHz - 3.775GHz	900mA	105°C
				650mA	115°C
				500mA	125°C
	FPD4	Design 6	4.71875MHz - 3.775GHz	1100mA	105°C
				800mA	115°C
				650mA	125°C

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6.1 PoC Network from FPD-Link III Data Sheet

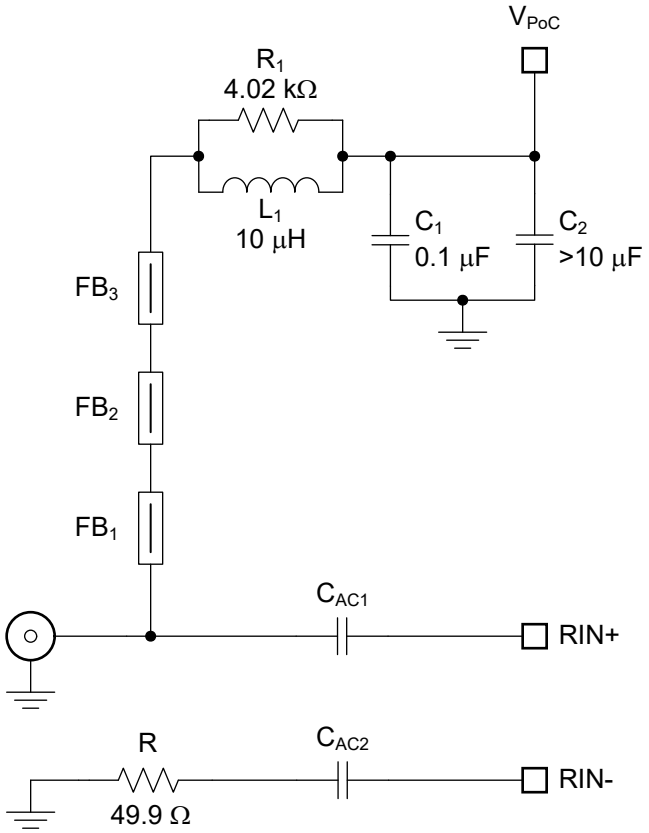


Figure 6-1. Recommended PoC Network from FPD-Link III Data Sheet

Table 6-2. Suggested PoC Network Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10µH, 0.288Ω max, 530mA MIN(Isat, Itemp) 30MHz SRF min, 3mm × 3mm, AEC-Q200	LQH3NPZ100MJR	Murata
	Inductor, 10µH, 0.360Ω max, 450mA MIN(Isat, Itemp) 30MHz SRF min, 3.2mm × 2.5mm, AEC-Q200	NLCV32T-100K-EFD	TDK
	Inductor, 10µH, 0.400Ω typ, 550mA MIN(Isat, Itemp) 39MHz SRF typ, 3mm × 3mm, AEC-Q200	TYS3010100M-10	Laird
	Inductor, 10µH, 0.325Ω max, 725mA MIN(Isat, Itemp) 41MHz SRF typ, 3mm × 3mm, AEC-Q200	TYS3015100M-10	Laird
FB1 – FB3	Ferrite Bead, 1.5kΩ at 1GHz, 0.5Ω max @ DC 500mA at 85°C, 0603 SMD , AEC-Q200	BLM18HE152SZ1	Murata

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6.2 Murata FPD3 Networks

6.2.1 Murata FPD3 Design 1

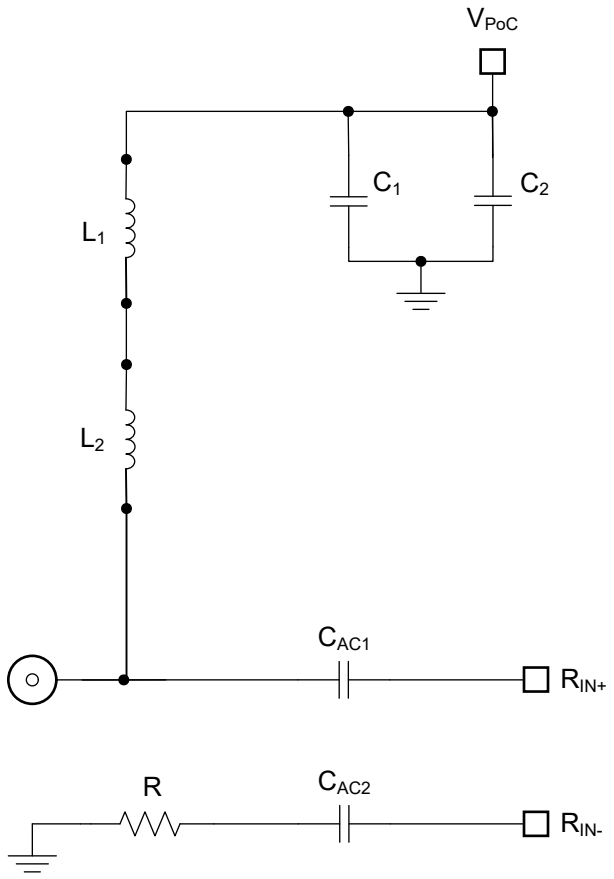


Figure 6-2. Murata FPD3 Design 1

Table 6-3. Murata FPD3 Design 1

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	Murata
L2			

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6.2.2 Murata FPD3 Design 2

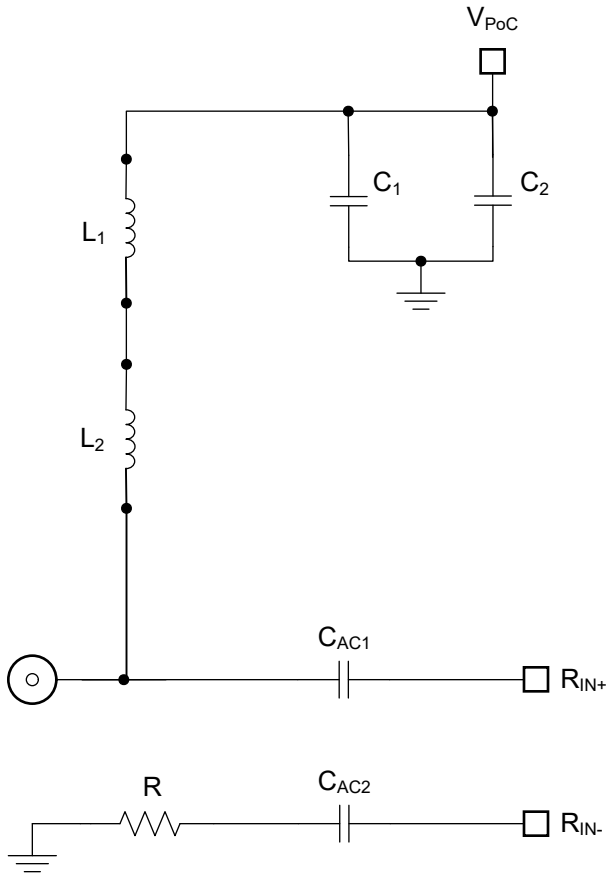


Figure 6-3. Murata FPD3 Design 2

Table 6-4. Murata FPD3 Design 2

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 4.5mm × 3.2mm x 3.5mm	LQW43FT180M0H	Murata
L2	Inductor, 3.3uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R3M0H	

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6.2.3 Murata FPD3 Design 3

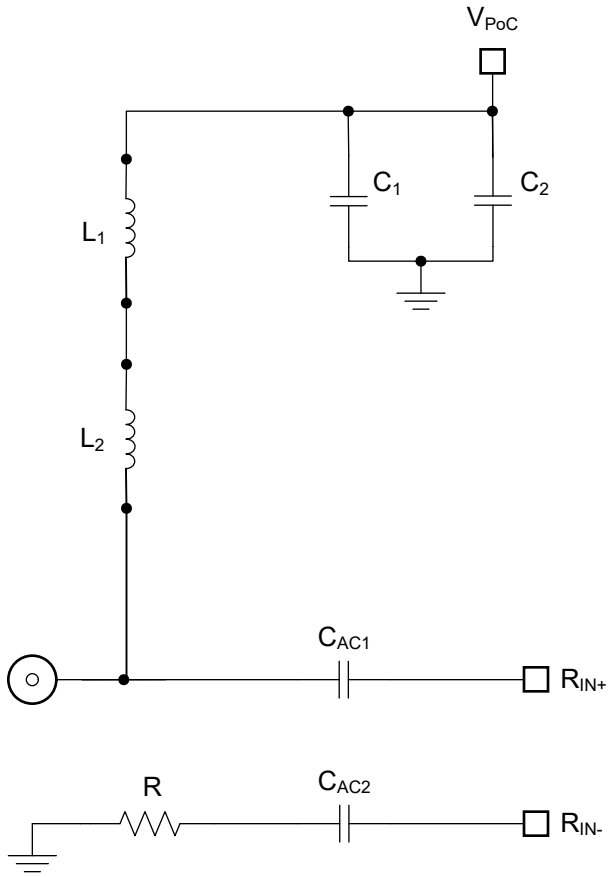


Figure 6-4. Murata FPD3 Design 3

Table 6-5. Murata FPD3 Design 3

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3mm × 3mm x 1.4mm	LQH3NPH150MME	Murata
L2	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	

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6.2.4 Murata FPD3 Design 4

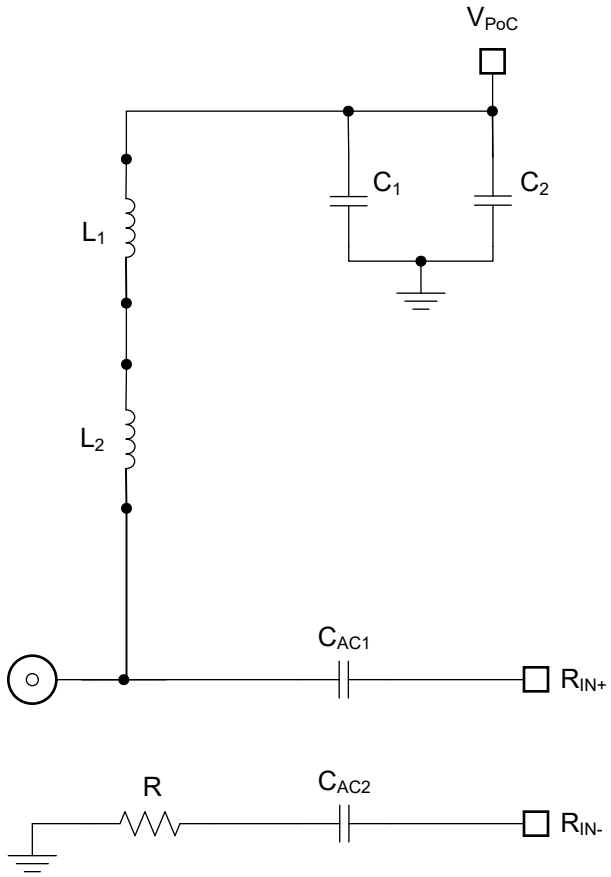


Figure 6-5. Murata FPD3 Design 4

Table 6-6. Murata FPD3 Design 4

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	Murata
L2			

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6.2.5 Murata FPD3 Design 5

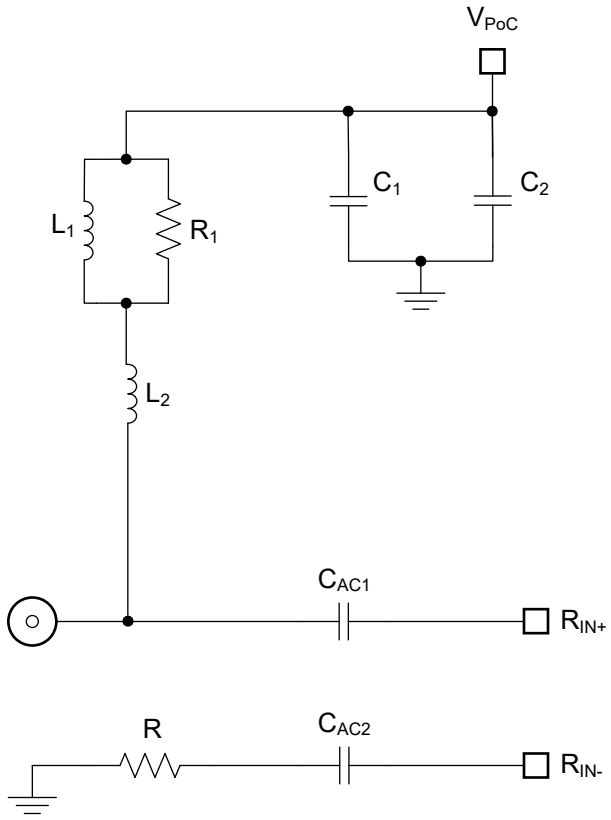


Figure 6-6. Murata FPD3 Design 5

Table 6-7. Murata FPD3 Design 5

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3.2mm × 2.5mm x 2.3mm	LQW32FT470M0H	Murata
L2	Inductor, 650nH 1.6mm × 0.8mm x 0.8mm	LQW18CNR65J0H	
R1	1kΩ		

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6.2.6 Murata FPD3 Design 6

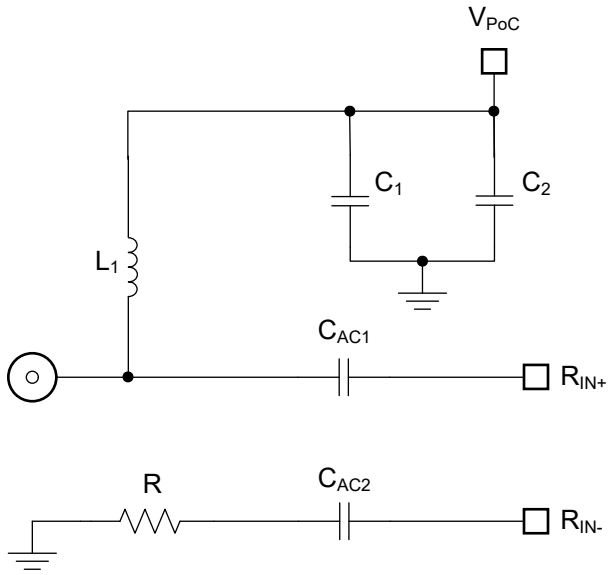


Figure 6-7. Murata FPD3 Design 6

Table 6-8. Murata FPD3 Design 6

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3.2mm × 2.5mm x 2.3mm	LQW32FT470M0H	Murata

6.3 TDK FPD3 Networks

6.3.1 TDK FPD3 Design 1

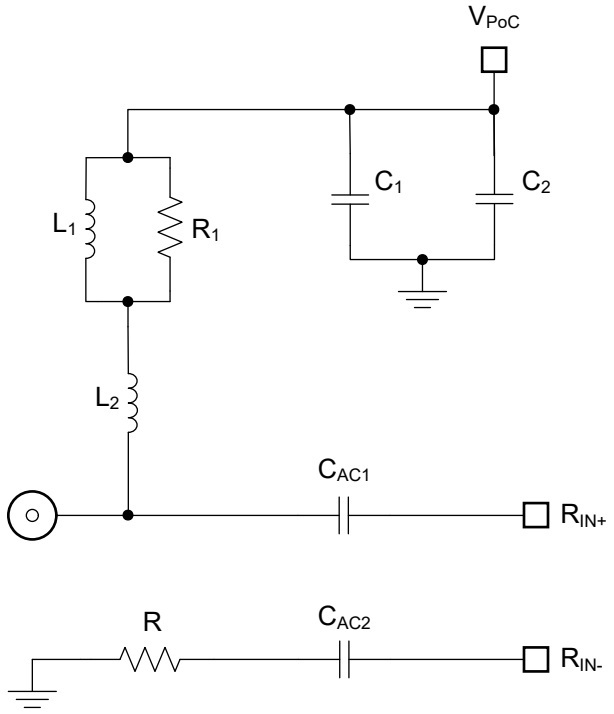


Figure 6-8. TDK FPD3 Design 1

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Table 6-9. TDK FPD3 Design 1

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm × 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 10uH 7.8mm × 2.7mm x 2.7mm	ADL8030VA-100M	
R1	1kΩ		

6.3.2 TDK FPD3 Design 2

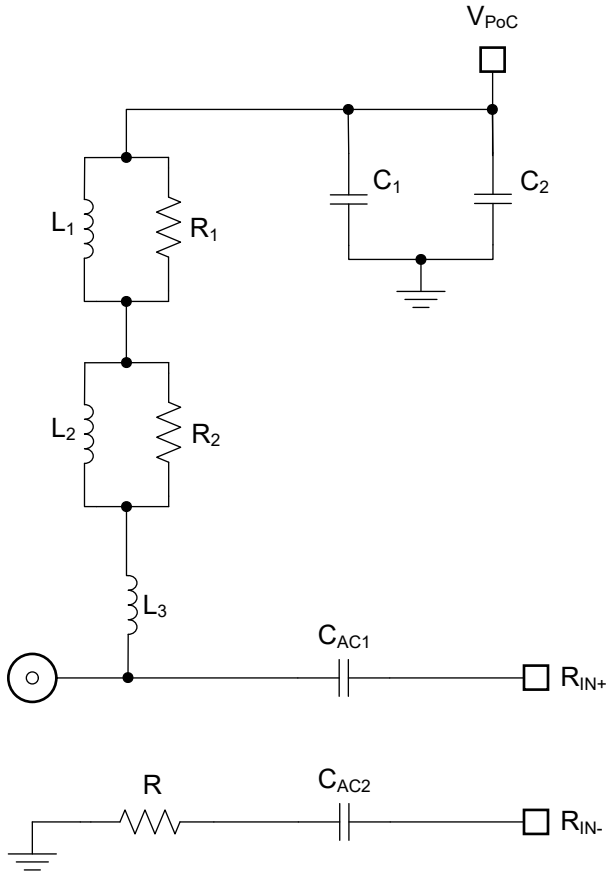


Figure 6-9. TDK FPD3 Design 2

Table 6-10. TDK FPD3 Design 2

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm × 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 3.3uH 3mm × 3mm x 1.5mm	VLS3015CX-3R3M-H	
L3	Inductor, 2.2uH 2.2mm × 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R2	1kΩ		
R1	1.5kΩ		

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6.3.3 TDK FPD3 Design 3

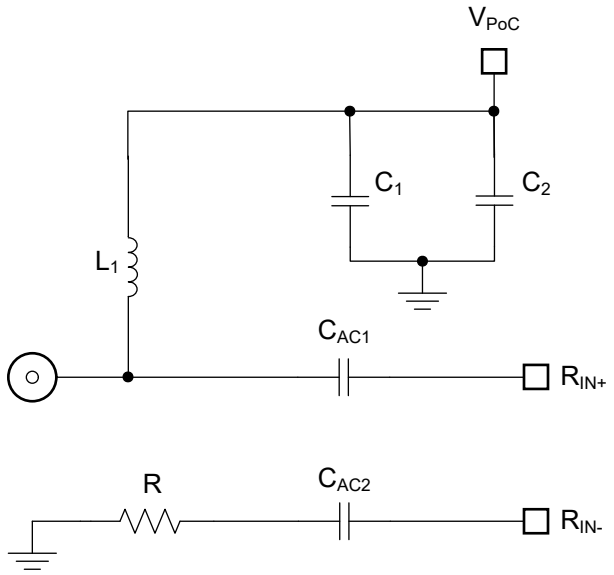


Figure 6-10. TDK FPD3 Design 3

Table 6-11. TDK FPD3 Design 3

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 7.8mm × 2.7mm x 2.7mm	ADL8030VA-100M	TDK

6.3.4 TDK FPD3 Design 4

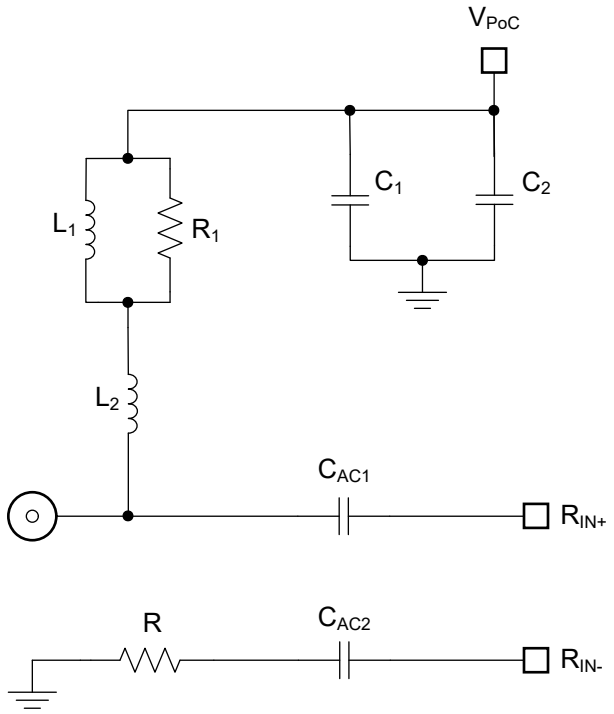


Figure 6-11. TDK FPD3 Design 4

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Table 6-12. TDK FPD3 Design 4

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3.2mm × 2.5mm x 2.5mm	ADL32VHC-150M	TDK
L2	Inductor, 1.5uH 2.2mm × 1.25mm x 1.65mm	ADL2012-1R5M-T01	
R1	1.5kΩ		

6.3.5 TDK FPD3 Design 5

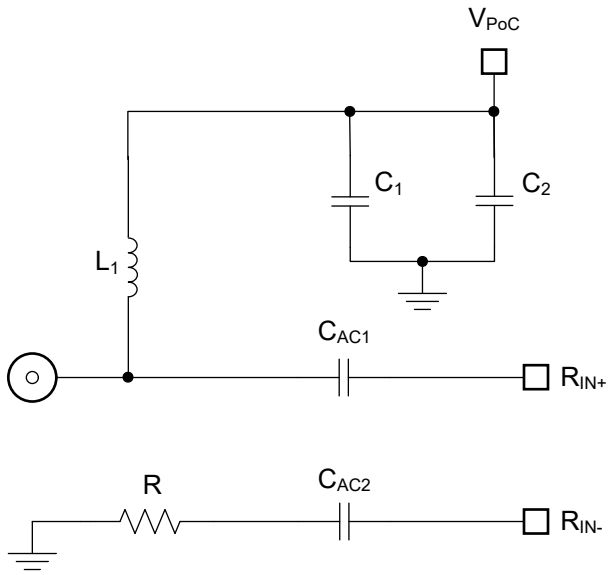


Figure 6-12. TDK FPD3 Design 5

Table 6-13. TDK FPD3 Design 5

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 4.5mm × 2.4mm x 2.8mm	ADL4524VL-180M-TL000	TDK

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6.3.6 TDK FPD3 Design 6

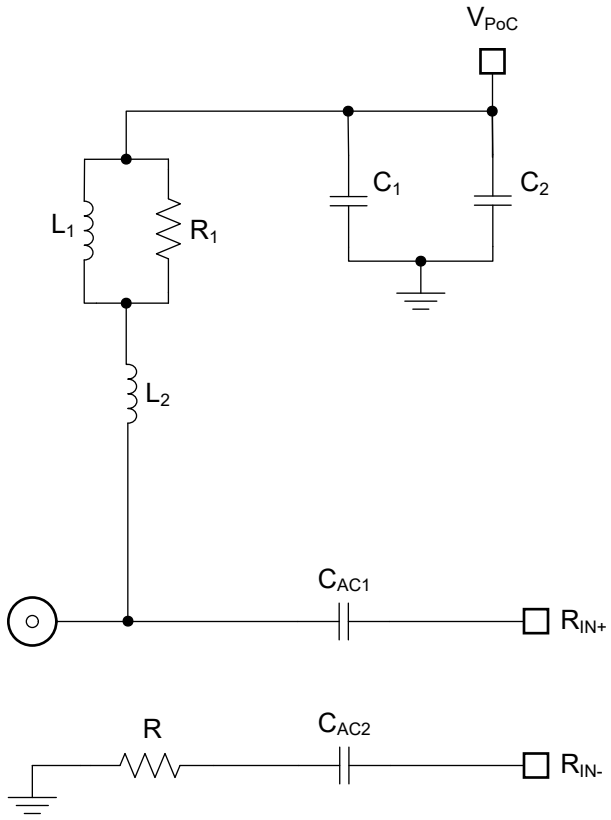


Figure 6-13. TDK FPD3 Design 6

Table 6-14. TDK FPD3 Design 6

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm × 3mm x 1.5mm	VLS3015CX-100M-H	TDK
L2	Inductor, 2.2uH 2.2mm × 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1kΩ		

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6.3.7 TDK FPD3 Design 7

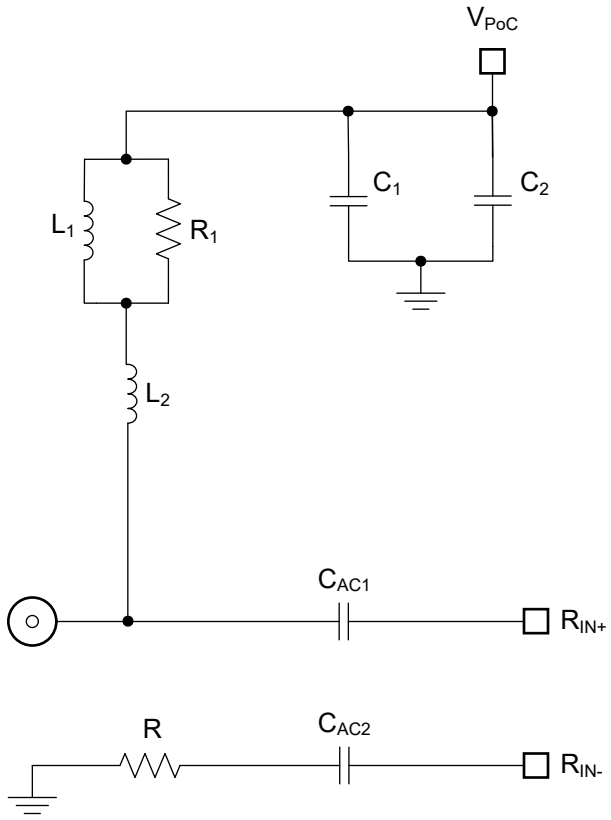


Figure 6-14. TDK FPD3 Design 7

Table 6-15. TDK FPD3 Design 7

Designator	Description	Part Number	Vendor
L1	Inductor, 2.2uH 3mm × 3mm x 1.5mm	VLS3015CX-2R2M-H	TDK
L2	Inductor, 2.2uH 3.2mm × 2.5mm x 2.5mm	ADL3225VM-2R2M-TL001	
R1	1kΩ		

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6.3.8 TDK FPD3 Design 8

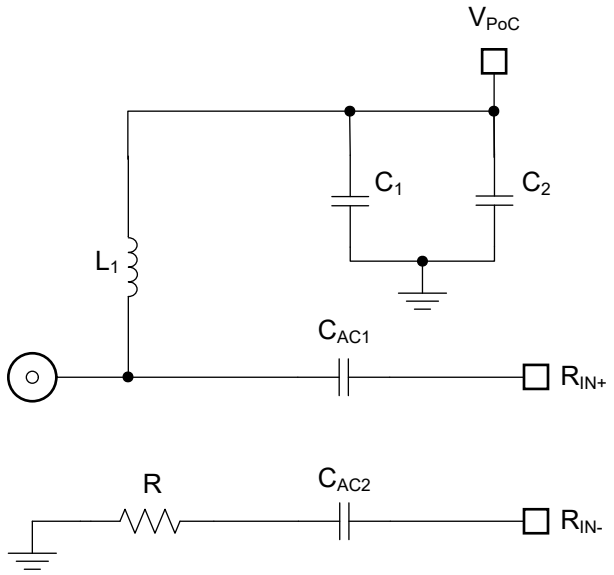


Figure 6-15. TDK FPD3 Design 8

Table 6-16. TDK FPD3 Design 8

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm × 2.4mm x 2.8mm	ADL4524VL-100M-TL000	TDK

6.3.9 TDK FPD3 Design 9

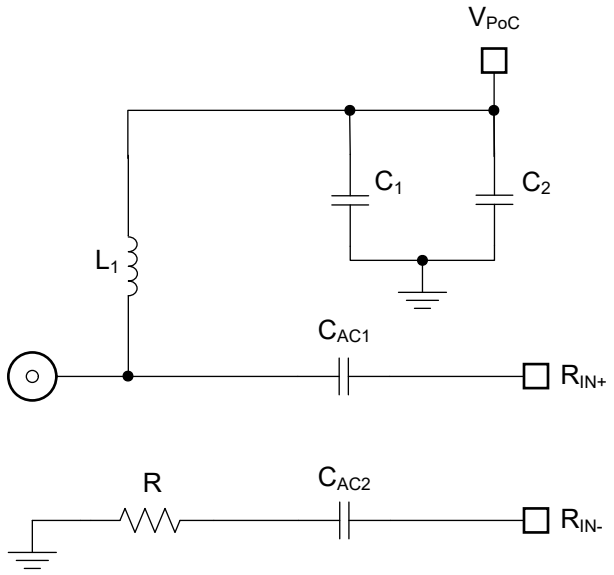


Figure 6-16. TDK FPD3 Design 9

Table 6-17. TDK FPD3 Design 9

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.2mm x 2.5mm x 2.3mm	ADL3225V-220MS-TL000	TDK

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6.3.10 TDK FPD3 Design 10

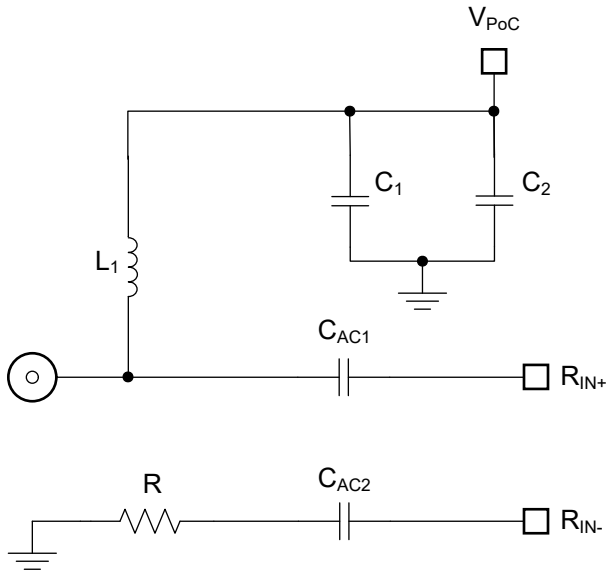


Figure 6-17. TDK FPD3 Design 10

Table 6-18. TDK FPD3 Design 10

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-180MF	TDK

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6.4 Coilcraft FPD3 Networks

6.4.1 Coilcraft FPD3 Design 1

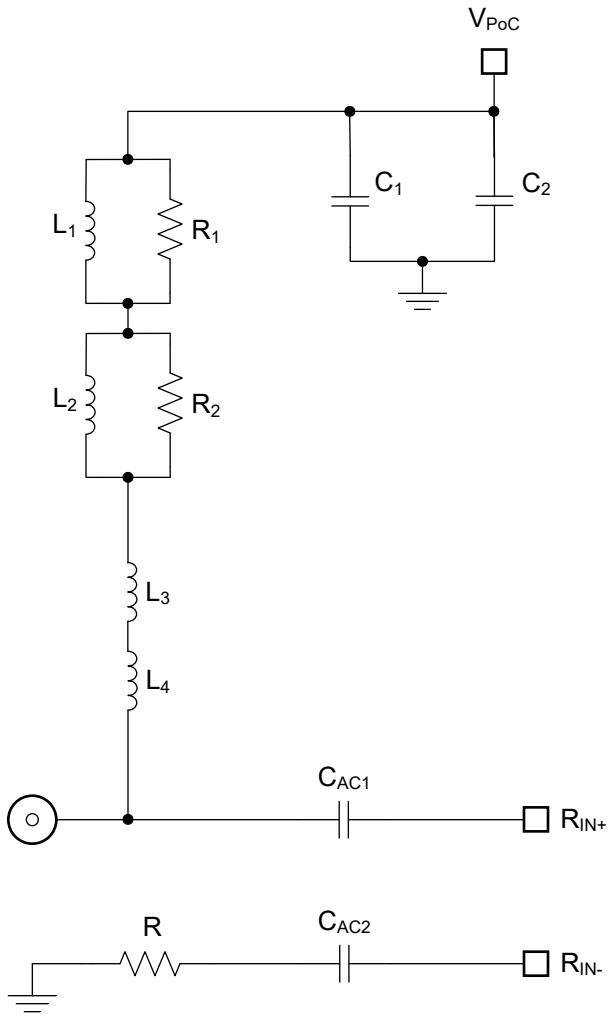


Figure 6-18. Coilcraft FPD3 Design 1

Table 6-19. Coilcraft FPD3 Design 1

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 10mm × 10mm x 4.8mm	MSS1048T-104	Coilcraft
L2	Inductor, 10uH 5.87mm × 4.98mm x 3.81mm	1812PS-103	
L3	Inductor, 1uH 2.2mm × 1.45mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.47uH 1.8mm × 1.07mm x 0.97mm	PFL1609-471	
R1	2.6kΩ		
R2	3kΩ		

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6.4.2 Coilcraft FPD3 Design 2

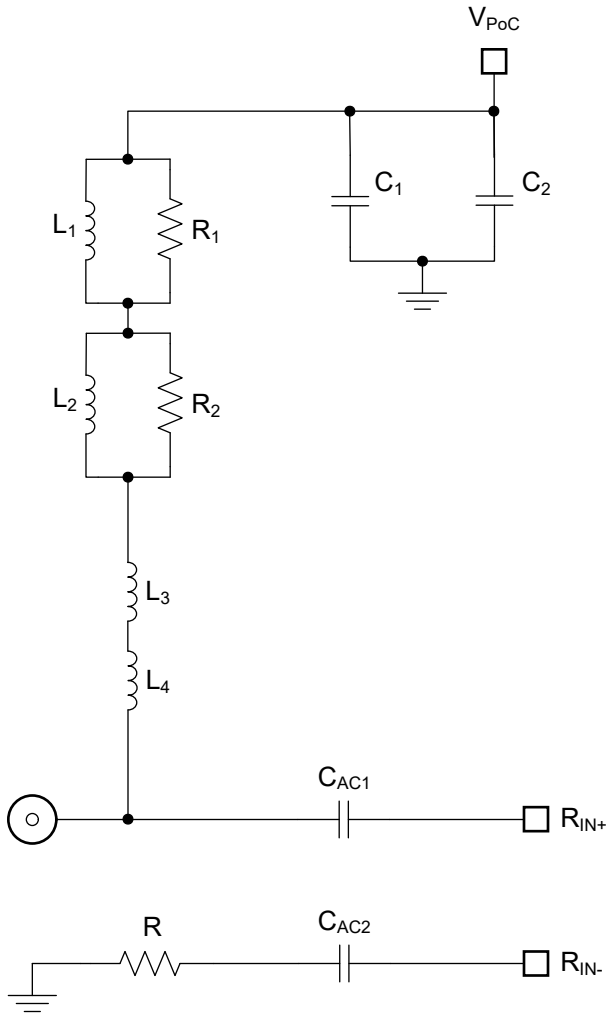


Figure 6-19. Coilcraft FPD3 Design 2

Table 6-20. Coilcraft FPD3 Design 2

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 7.3mm × 7.3mm x 4.1mm	MSS7341T-104	Coilcraft
L2	Inductor, 6.8uH 3.3mm × 2.67mm x 3mm	1210POC-682	
L3	Inductor, 1uH 2.2mm × 1.45 mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.18uH 1.14mm × 0.635mm x 0.71mm	PFL1005-181	
R1	4kΩ		
R2	4kΩ		

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6.4.3 Coilcraft FPD3 Design 3

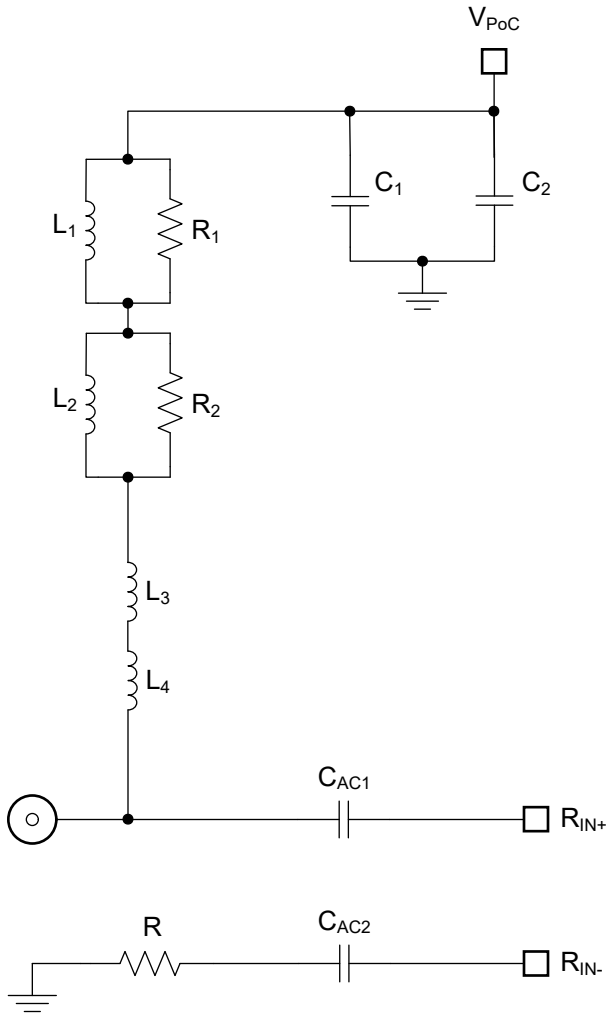


Figure 6-20. Coilcraft FPD3 Design 3

Table 6-21. Coilcraft FPD3 Design 3

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 3.9mm × 3.9mm x 4mm	LPS4040-104	Coilcraft
L2	Inductor, 6.8uH 3.3mm × 2.67mm x 3mm	1210POC-682	
L3	Inductor, 1uH 2.2mm × 1.45mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.47uH 1.8mm × 1.07mm x 0.95mm	PFL1609-471	
R1	2.61kΩ		
R2	3.6kΩ		

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6.4.4 Coilcraft FPD3 Design 4

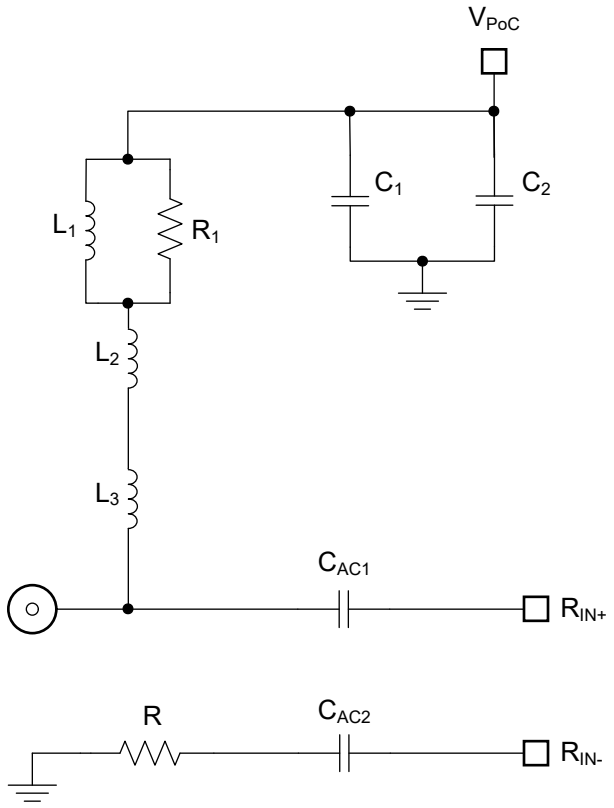


Figure 6-21. Coilcraft FPD3 Design 4

Table 6-22. Coilcraft FPD3 Design 4

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 5.87mm × 4.98mm x 3.81mm	1812PS-103	Coilcraft
L2	Inductor, 1uH 2.2mm × 1.45mm x 1.5mm	PFL2015-102	
L3	Inductor, 0.47uH 1.8mm × 1.07mm x 0.95mm	PFL1609-471	
R1	3kΩ		

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6.4.5 Coilcraft FPD3 Design 5

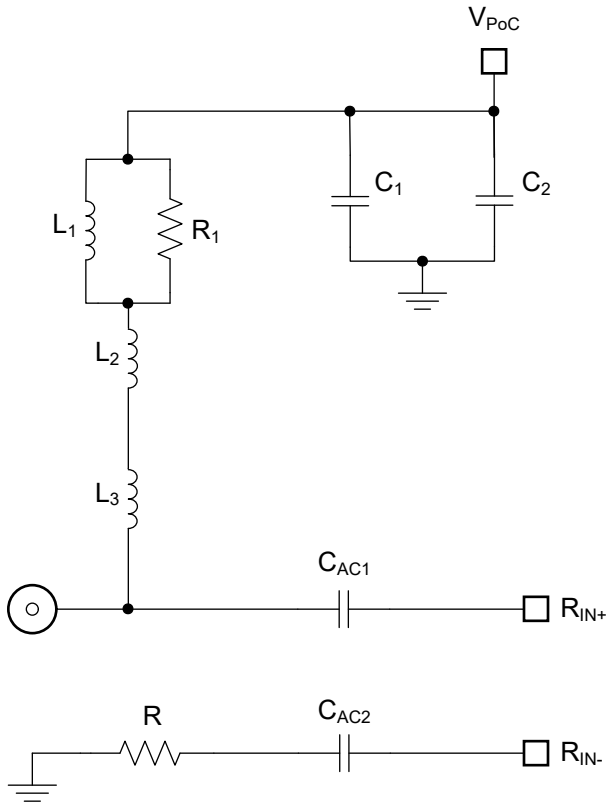


Figure 6-22. Coilcraft FPD3 Design 5

Table 6-23. Coilcraft FPD3 Design 5

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.3mm × 2.67mm x 3mm	1210POC-682	Coilcraft
L2	Inductor, 1uH 2.2mm × 1.45mm x 1.5mm	PFL2015-102	
L3	Inductor, 0.18uH 1.14mm × 0.635mm x 0.71mm	PFL1005-181	
R1	4kΩ		

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6.4.6 Coilcraft FPD3 Design 6

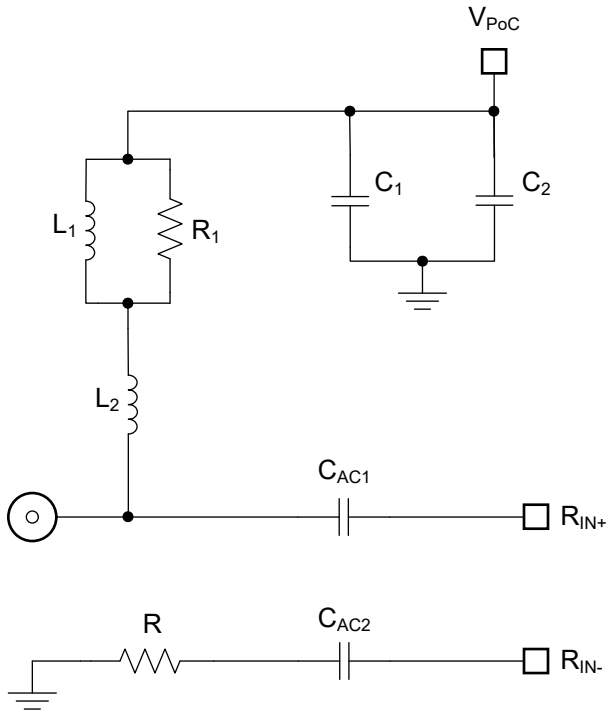


Figure 6-23. Coilcraft FPD3 Design 6

Table 6-24. Coilcraft FPD3 Design 6

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.2mm × 1.4mm x 2.36mm	1205POC-682	Coilcraft
L2	Inductor, 1uH 1.8mm × 1.07mm x 0.95mm	PFL1609-102	
R1	3.6kΩ		

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6.4.7 Coilcraft FPD3 Design 7

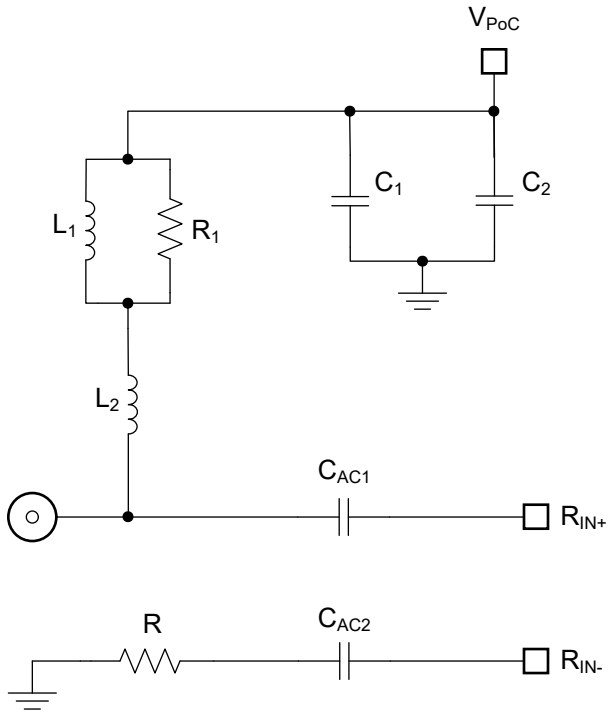


Figure 6-24. Coilcraft FPD3 Design 7

Table 6-25. Coilcraft FPD3 Design 7

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.3mm × 2.67mm x 3mm	1210POC-223	Coilcraft
L2	Inductor, 0.56uH 1.8mm × 1.07mm x 0.95mm	PFL1609-561	
R1	5.1kΩ		

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6.4.8 Coilcraft FPD3 Design 8

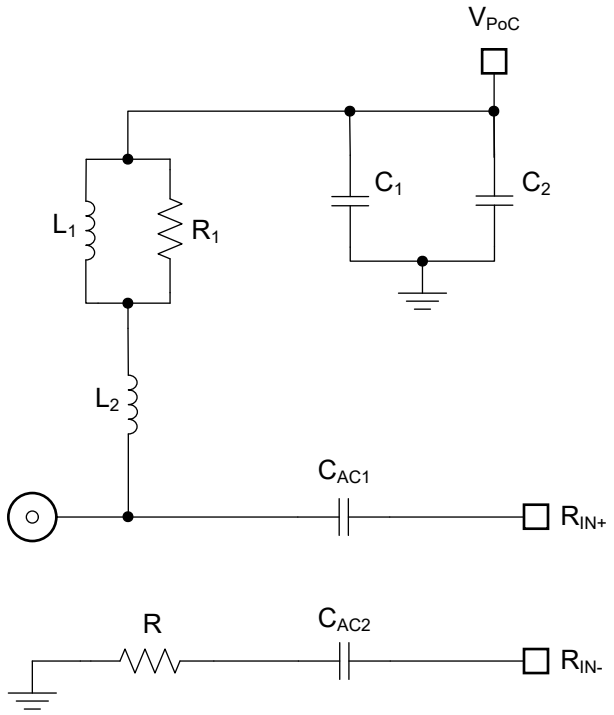


Figure 6-25. Coilcraft FPD3 Design 8

Table 6-26. Coilcraft FPD3 Design 8

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.3mm × 2.67mm x 3mm	1210POC-223	Coilcraft
L2	Inductor, 0.56uH 1.14mm × 0.635mm x 0.71mm	PFL1005-561	
R1	5.1kΩ		

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6.4.9 Coilcraft FPD3 Design 9

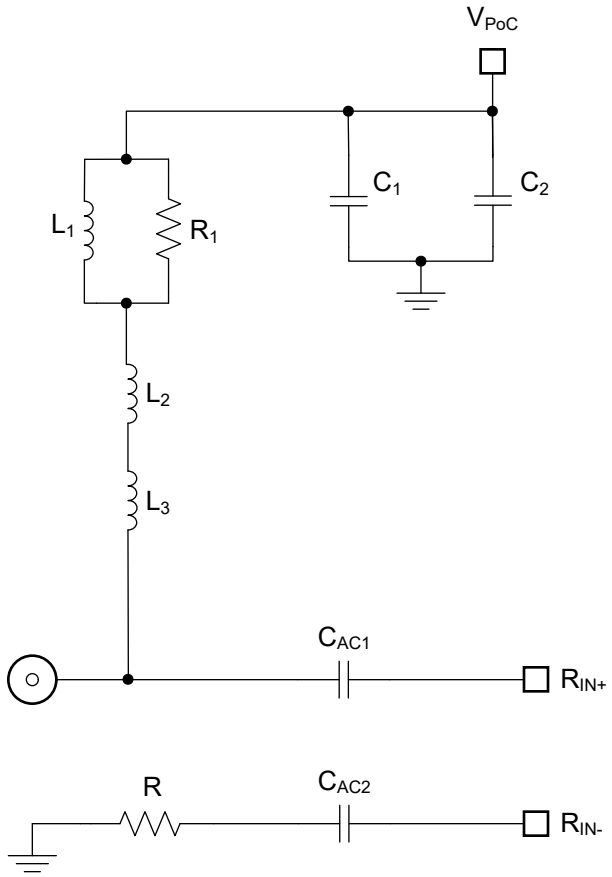


Figure 6-26. Coilcraft FPD3 Design 9

Table 6-27. Coilcraft FPD3 Design 9

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.2mm × 1.4mm x 2.36mm	1205POC-682	Coilcraft
L2	Inductor, 1uH 1.8mm × 1mm x 0.95mm	PFL1609-102	
L3	Inductor, 0.18uH 1.14mm × 0.635mm x 0.71mm	PFL1005-181	
R1	3.6kΩ		

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6.5 Murata FPD4 Networks

6.5.1 Design 1

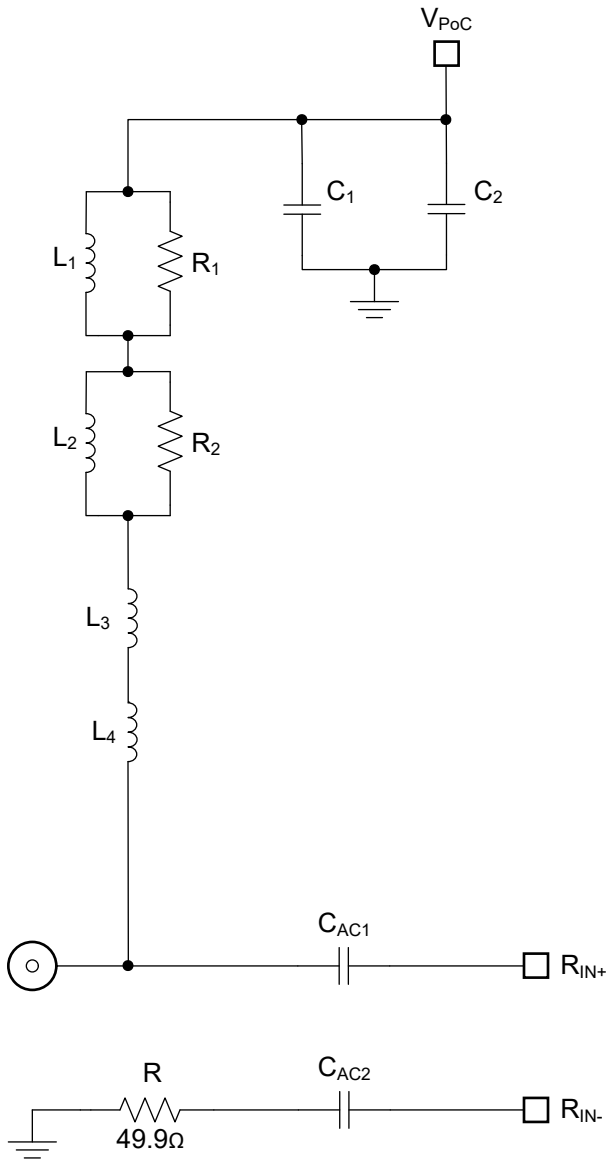


Figure 6-27. Murata PoC Network Number 1 Schematic

Table 6-28. Murata PoC Network 1 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm × 3 mm x 1.4mm	LQH3NPH100MME	Murata
L2	Inductor, 3.3uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R3M0H	
L3	Inductor, 120nH 1.6mm × 0.8mm x 0.8mm	LQW18CNR12J0H	
L4			
R1	1.5kΩ		
R2	3kΩ		

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6.5.2 Design 2

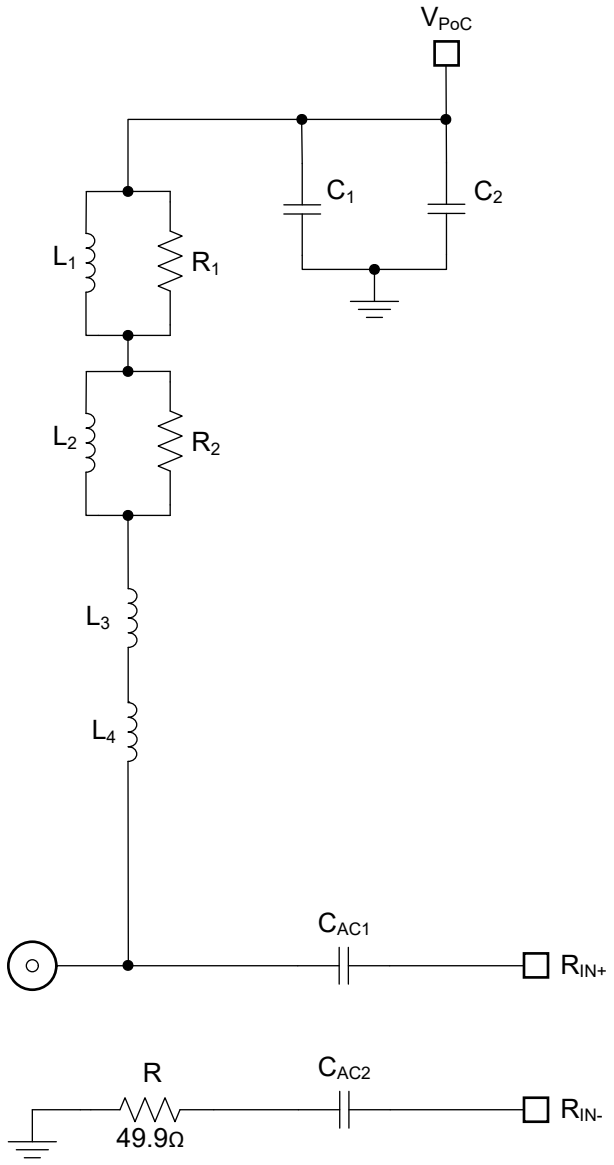


Figure 6-28. Murata PoC Network Number 2 Schematic

Table 6-29. Murata PoC Network 2 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3mm × 3mm x 1.4mm	LQH3NPH6R8MME	Murata
L2	Inductor, 3.3uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R3M0H	
L3	Inductor, 120nH 1.6mm × 0.8mm x 0.8mm	LQW18CNR12J0H	
L4			
R1	1.5kΩ		
R2	3kΩ		

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6.5.3 Design 3

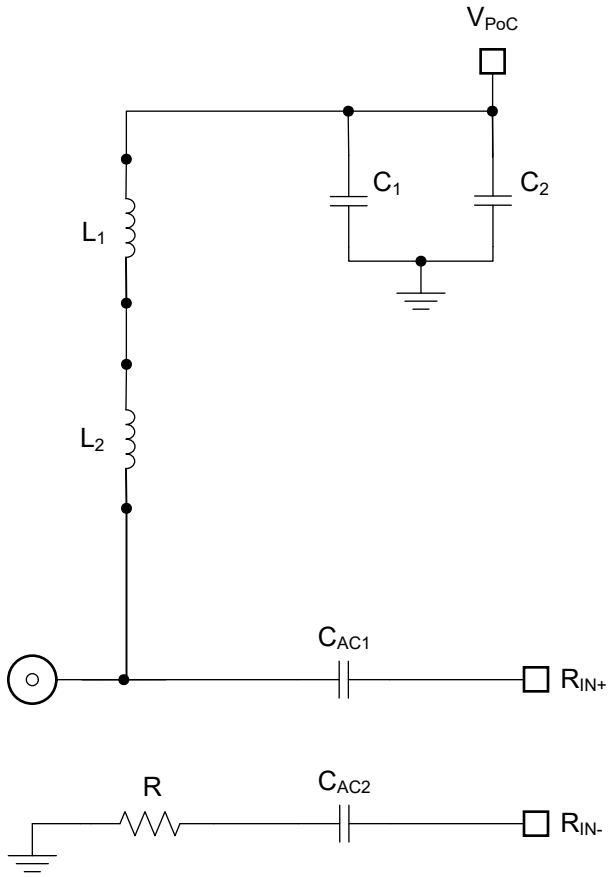


Figure 6-29. Murata PoC Network Number 3 Schematic

Table 6-30. Murata PoC Network 3 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3.2mm × 2.5mm x 2.3mm	LQW32FT470M0H	Murata
L2	Inductor, 2uH 2mm × 1.2mm x 1.6mm	LQW21FT2R0M0H	

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6.5.4 Design 4

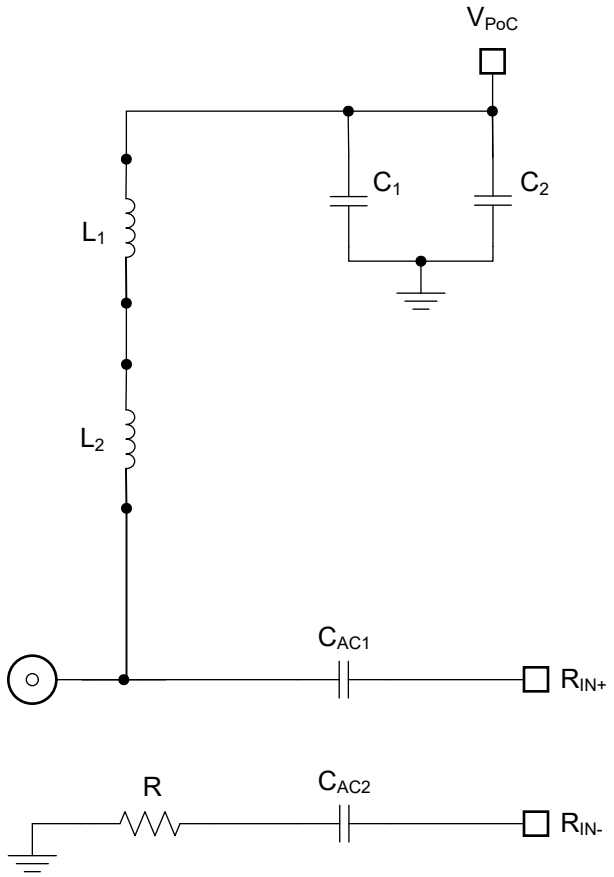


Figure 6-30. Murata PoC Network Number 4 Schematic

Table 6-31. Murata PoC Network 4 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.2mm × 2.5mm x 2.3mm	LQW32FT220M0H	Murata
L2	Inductor, 1.5uH 2mm × 1.2mm x 1.6mm	LQW21FT1R5M0H	

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6.5.5 Design 5

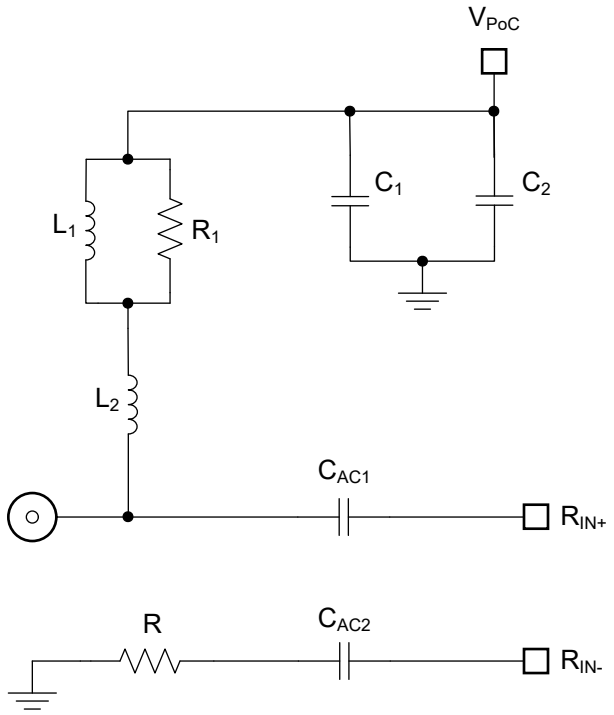


Figure 6-31. Murata PoC Network Number 5 Schematic

Table 6-32. Murata PoC Network 5 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3mm × 3mm x 1.4mm	LQH3NPH220MME	Murata
L2	Inductor, 1uH 2mm × 1.2mm x 1.6mm	LQW21FT1R0M0H	
R1	1.5kΩ		

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6.5.6 Design 6

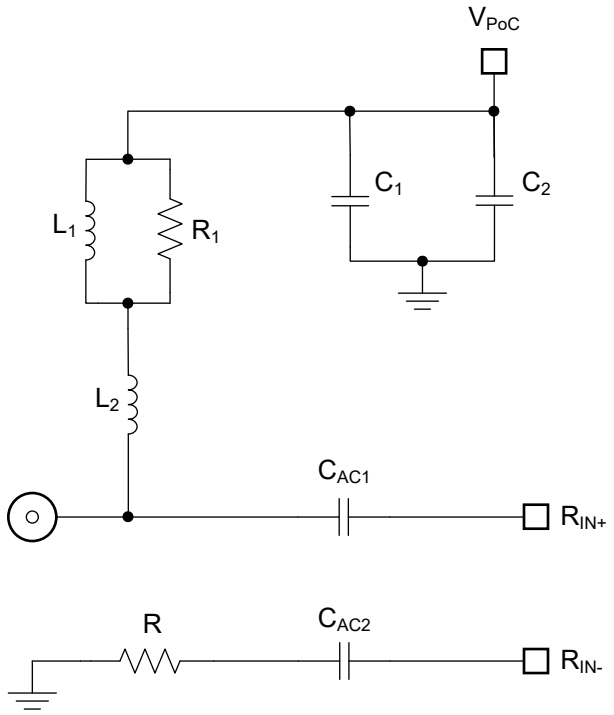


Figure 6-32. Murata PoC Network Number 6 Schematic

Table 6-33. Murata PoC Network 6 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 7.4mm × 7mm x 4.8mm	MDH7045C-470MA	Murata
L2	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	
R1	1.5kΩ		

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6.5.7 Design 7

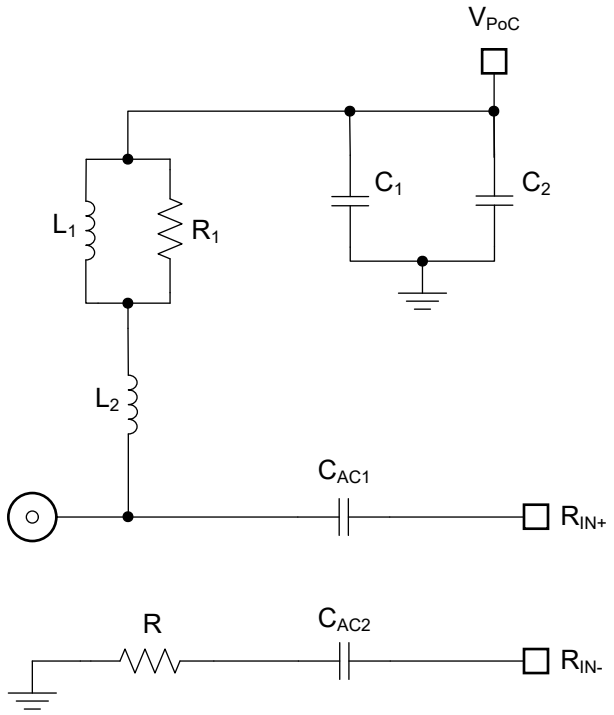


Figure 6-33. Murata PoC Network Number 7 Schematic

Table 6-34. Murata PoC Network 7 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 6.3mm × 6mm x 4.5mm	MDH6045C-470MA	Murata
L2	Inductor, 3.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R6M8H	
R1	1kΩ		

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6.5.8 Design 8

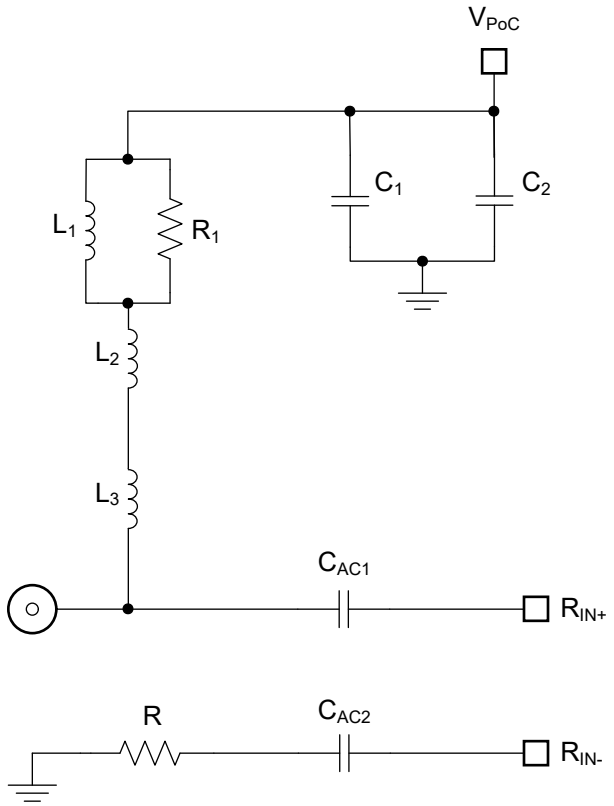


Figure 6-34. Murata PoC Network Number 8 Schematic

Table 6-35. Murata PoC Network 8 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 6.3mm × 6mm x 4.5mm	MDH6045C-470MA	Murata
L2	Inductor, 3.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R6M8H	
L3	Inductor, 0.47uH 2mm × 1.2mm x 1.6mm	LQW21FTR47M0H	
R1	1kΩ		

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6.5.9 Design 9

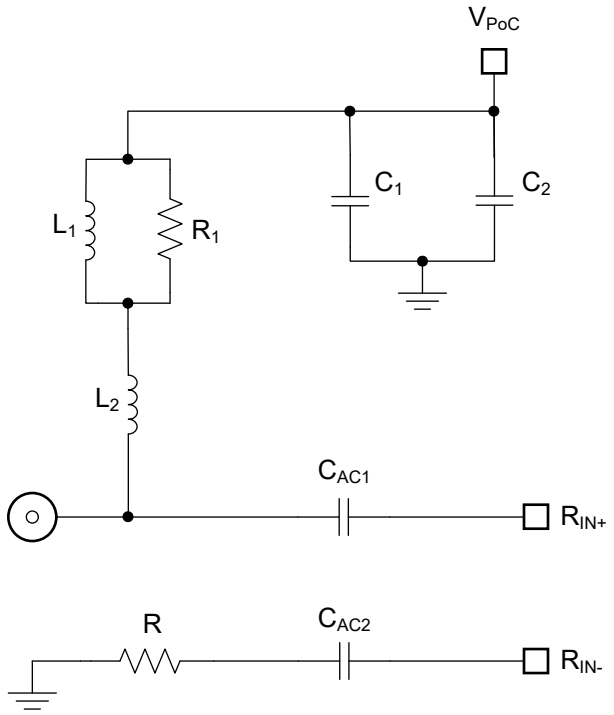


Figure 6-35. Murata PoC Network Number 9 Schematic

Table 6-36. Murata PoC Network 9 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 6.3mm × 6mm x 4.5mm	MDH6045C-470MA	Murata
L2	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	
R1	1.5kΩ		

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6.5.10 Design 10

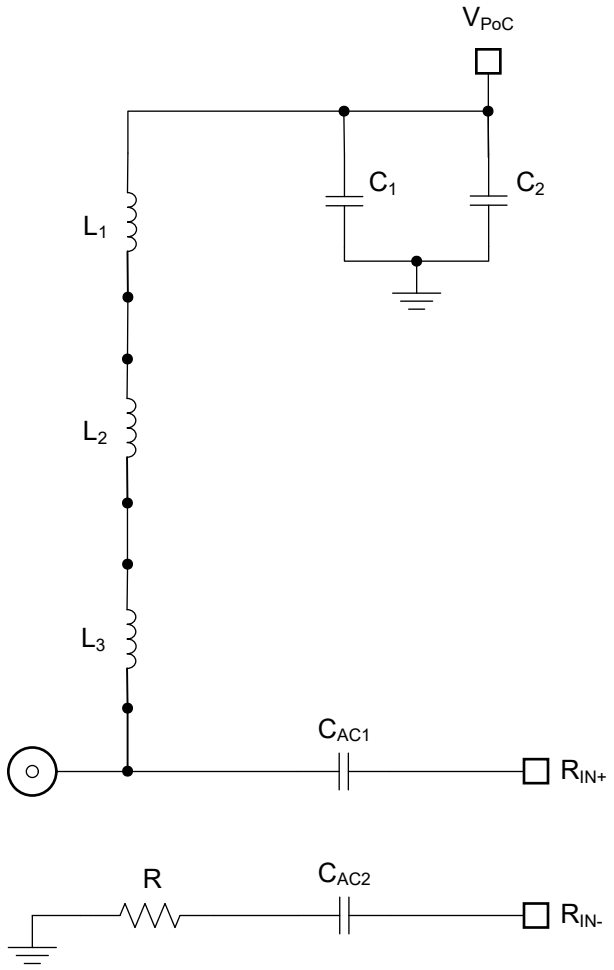


Figure 6-36. Murata PoC Network Number 10 Schematic

Table 6-37. Murata PoC Network 10 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 4mm × 4mm x 1.65mm	LQH44PH220MPR	Murata
L2	Inductor, 15uH 3mm × 3mm x 1.4mm	LQH3NPH150MME	
L3	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	

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6.5.11 Design 11

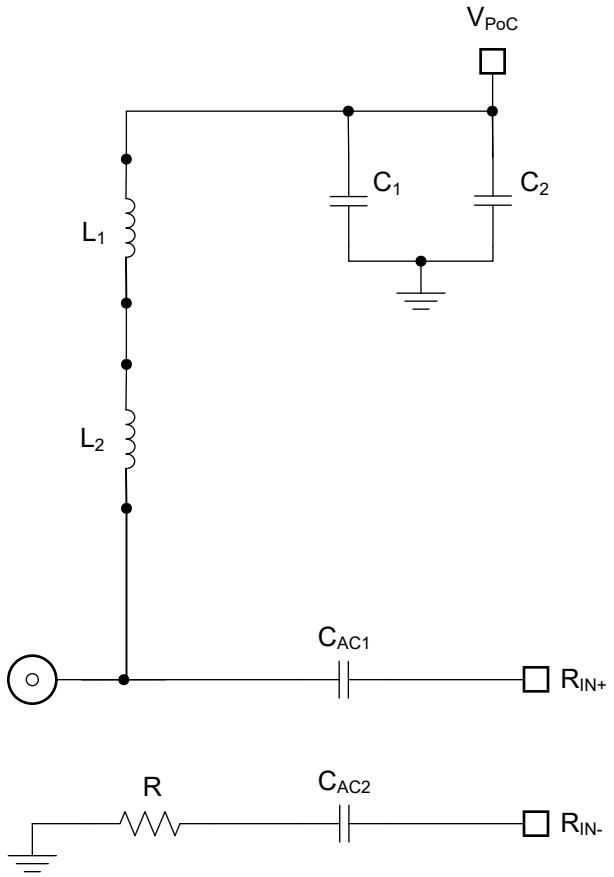


Figure 6-37. Murata PoC Network Number 11 Schematic

Table 6-38. Murata PoC Network 11 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 33uH 4mm × 4mm x 1.65mm	LQH44PH330MPR	Murata
L2	Inductor, 22uH 3.2mm × 2.5mm x 2.3mm	LQW32FT220M0H	

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6.5.12 Design 12

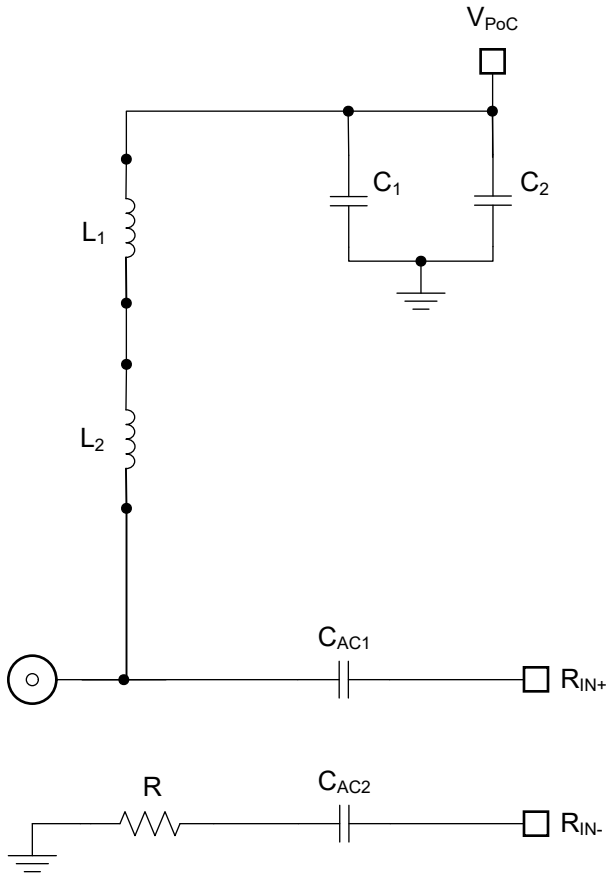


Figure 6-38. Murata PoC Network Number 12 Schematic

Table 6-39. Murata PoC Network 12 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3mm × 3mm x 1.4mm	LQH3NPH220MME	Murata
L2	Inductor, 22uH 3.2mm × 2.5mm x 2.3mm	LQW32FT220M0H	

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6.5.13 Design 13

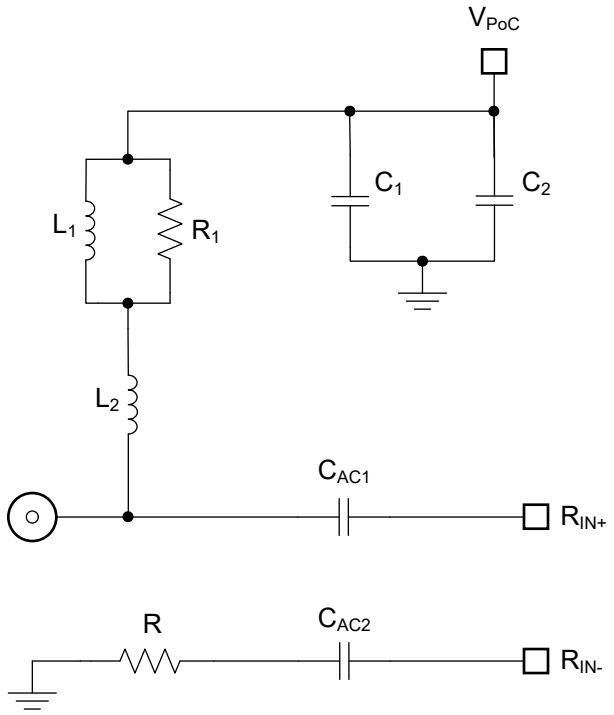


Figure 6-39. Murata PoC Network Number 13 Schematic

Table 6-40. Murata PoC Network 13 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 4mm × 4mm x 1.65mm	LQH44PH470MPR	Murata
L2	Ferrite Bead, 8kΩ at 100 MHz, 0.7Ω DCR, 0805 SMD, AEC-Q200	BLM21HE802SH1	
R1	1.5kΩ		

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6.5.14 Design 14

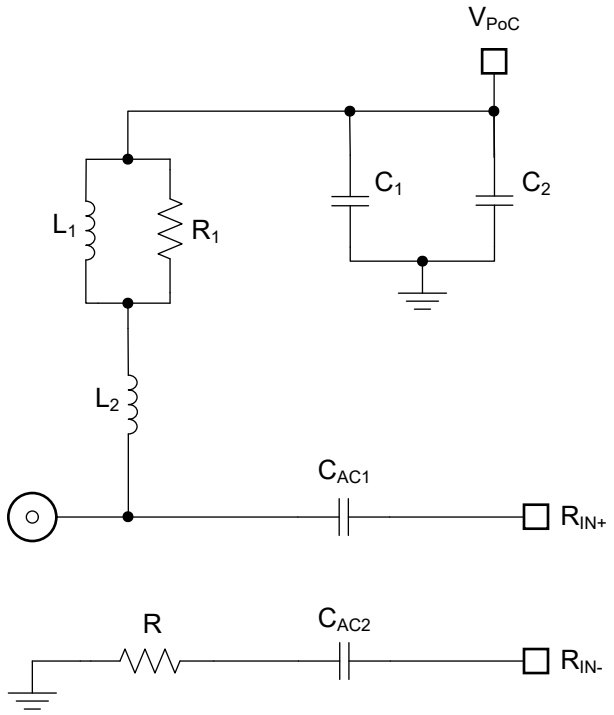


Figure 6-40. Murata PoC Network Number 14 Schematic

Table 6-41. Murata PoC Network 14 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 3mm × 3mm x 1.4mm	LQH3NPH680MME	Murata
L2	Inductor, 2uH 2mm × 1.2mm x 1.6mm	LQW21FT2R0M0H	
R1	1kΩ		

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6.5.15 Design 15

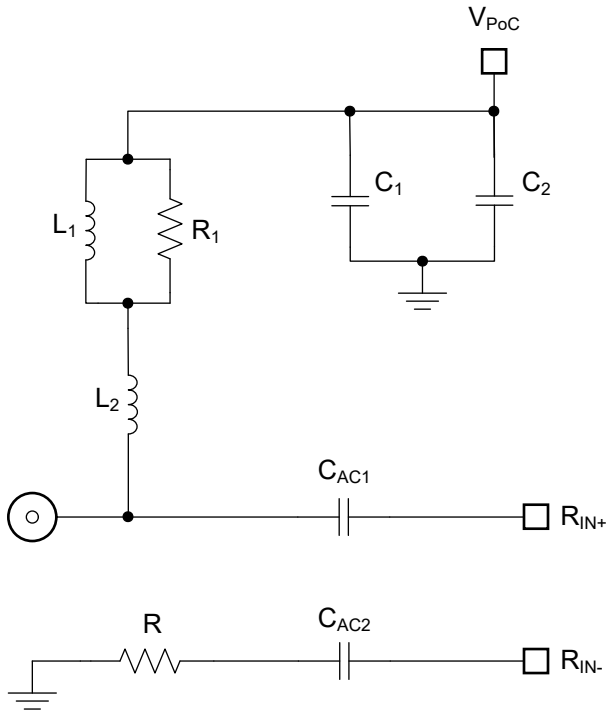


Figure 6-41. Murata PoC Network Number 15 Schematic

Table 6-42. Murata PoC Network 15 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 6.3mm × 6mm x 4.8mm	MDH6045C-220MA	Murata
L2	Inductor, 1.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT1R6M8H	
R1	1kΩ		

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6.5.16 Design 16

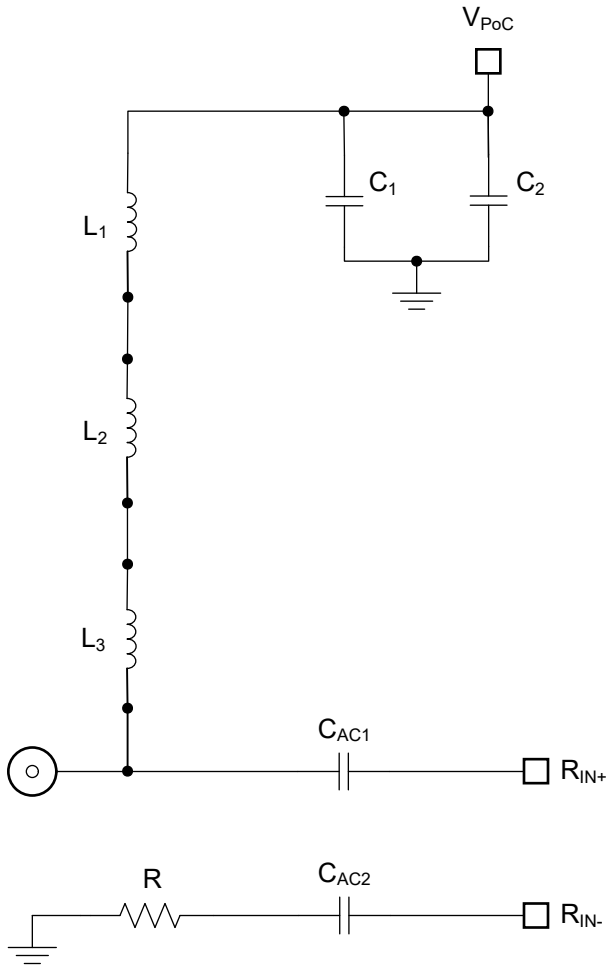


Figure 6-42. Murata PoC Network Number 16 Schematic

Table 6-43. Murata PoC Network 16 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	Murata
L2	Inductor, 3.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R6M8H	
L3			

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6.5.17 Design 17

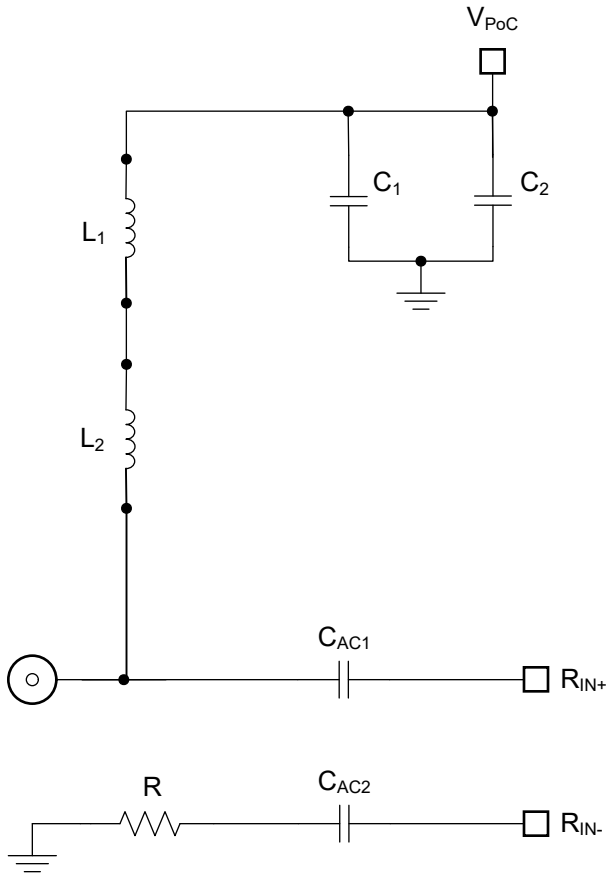


Figure 6-43. Murata PoC Network Number 17 Schematic

Table 6-44. Murata PoC Network 17 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	Murata
L2			

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6.5.18 Design 18

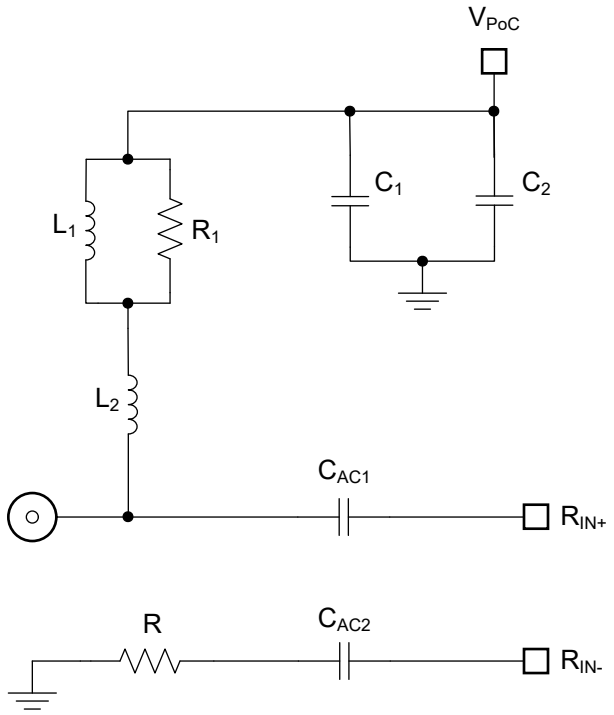


Figure 6-44. Murata PoC Network Number 18 Schematic

Table 6-45. Murata PoC Network 18 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4mm × 4mm x 1.65mm	LQH44PH100MPR	Murata
L2	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	
R1	1kΩ		

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6.5.19 Design 19

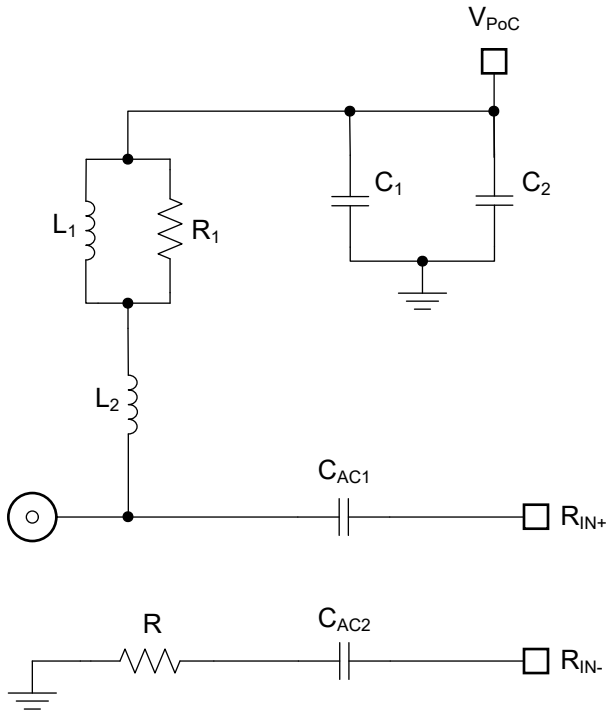


Figure 6-45. Murata PoC Network Number 19 Schematic

Table 6-46. Murata PoC Network 19 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4mm × 4mm x 1.65mm	LQH44PH100MPR	Murata
L2	Inductor, 1.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT1R6M8H	
R1	1kΩ		

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6.5.20 Design 20

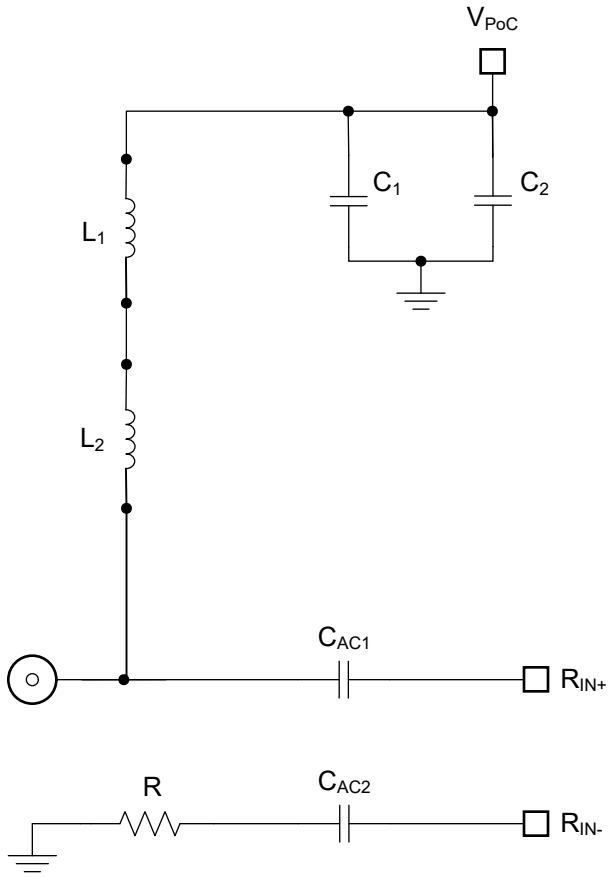


Figure 6-46. Murata PoC Network Number 20 Schematic

Table 6-47. Murata PoC Network 20 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 4.5mm × 3.2mm x 3.5mm	LQW43FT180M0H	Murata
L2	Inductor, 1.6uH 3.2mm × 2.5mm x 2.3mm	LQW32FT1R6M8H	

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6.5.21 Design 21

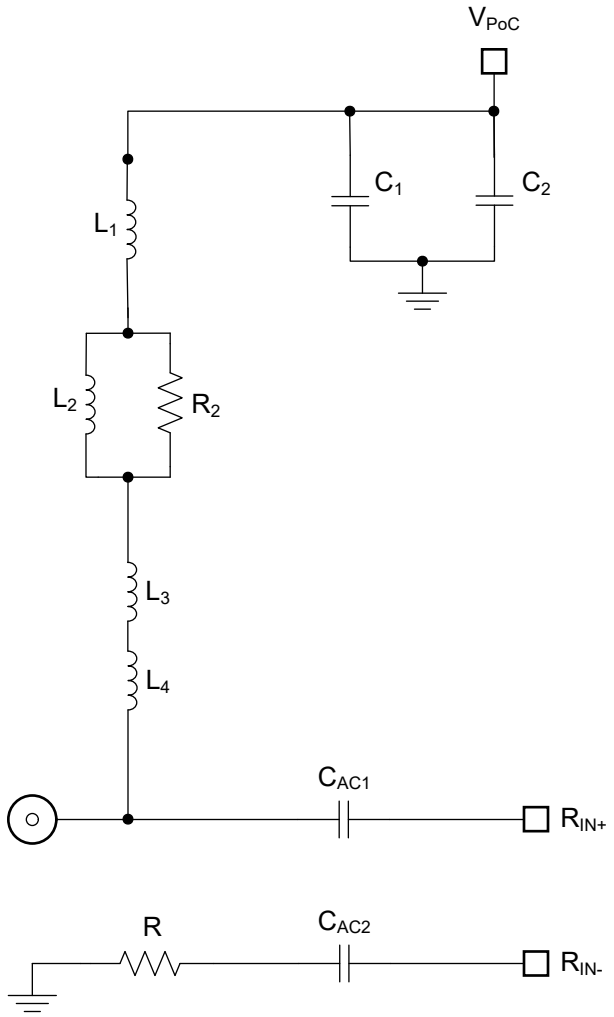


Figure 6-47. Murata PoC Network Number 21 Schematic

Table 6-48. Murata PoC Network 21 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4mm × 4mm x 1.65mm	LQH44PH100MPR	Murata
L2	Inductor, 3.3uH 3.2mm × 2.5mm x 2.3mm	LQW32FT3R3M0H	
L3	Inductor, 120nH 1.6mm × 0.8mm x 0.8mm	LQW18CNR12J0H	
L4			
R2	3kΩ		

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6.5.22 Design 22

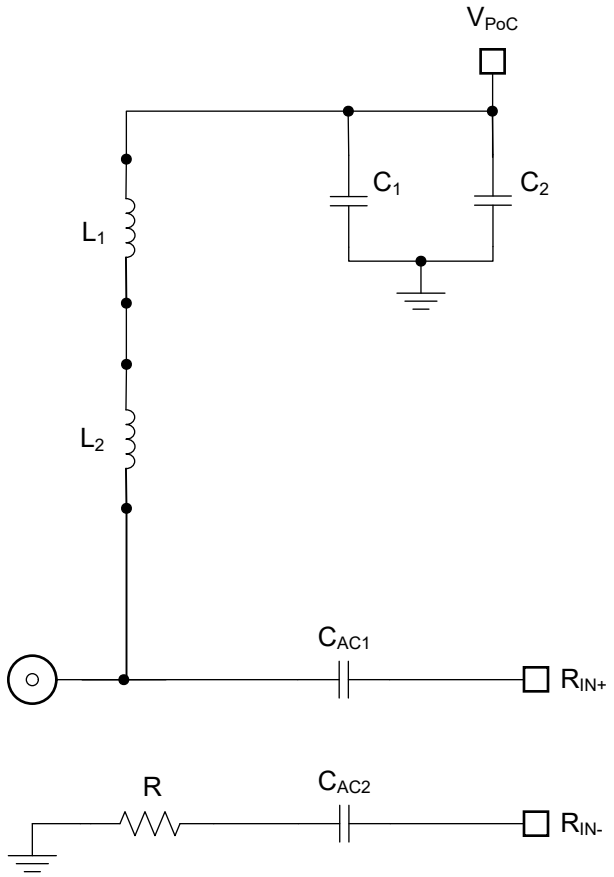


Figure 6-48. Murata PoC Network Number 22 Schematic

Table 6-49. Murata PoC Network 22 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm × 3.2mm x 3.5mm	LQW43FT100M0H	Murata
L2	Inductor, 0.82uH 2mm × 1.2mm x 1.6mm	LQW21FTR82M0H	

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6.5.23 Design 23

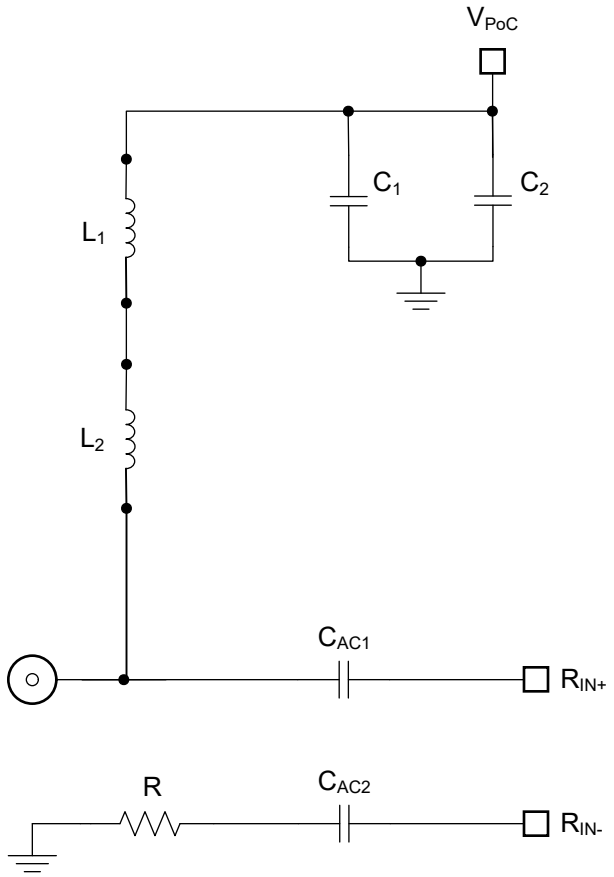


Figure 6-49. Murata PoC Network Number 23 Schematic

Table 6-50. Murata PoC Network 23 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3mm × 3mm x 1.4mm	LQH3NPH150MME	Murata
L2	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	

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6.5.24 Design 24

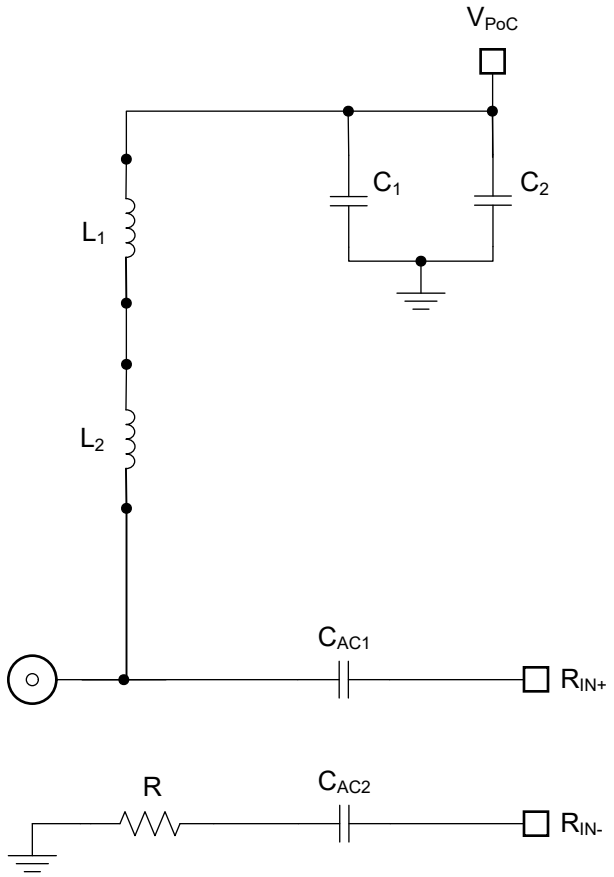


Figure 6-50. Murata PoC Network Number 24 Schematic

Table 6-51. Murata PoC Network 24 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 4.5mm × 3.2mm x 3.5mm	LQW43FT220M0H	Murata
L2	Inductor, 0.55uH 1.6mm × 0.94mm x 1.15mm	LQW18FTR55K0H	

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6.5.25 Design 25

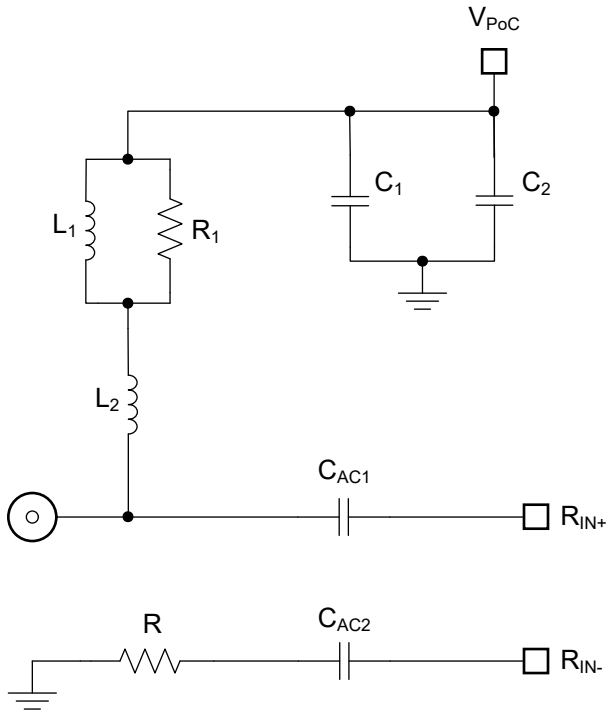


Figure 6-51. Murata PoC Network Number 25 Schematic

Table 6-52. Murata PoC Network 25 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm × 3mm x 1.4mm	LQH3NPH100MME	Murata
L2	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	
R1	1.5kΩ		

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6.5.26 Design 26

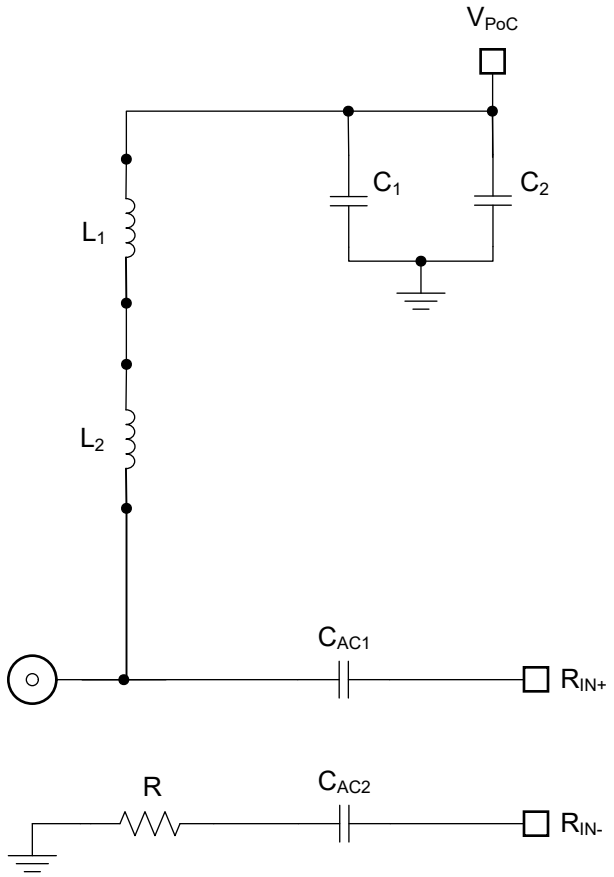


Figure 6-52. Murata PoC Network Number 26 Schematic

Table 6-53. Murata PoC Network 26 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm × 2.5mm x 2.3mm	LQW32FT100M0H	Murata
L2			

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6.5.27 Design 27

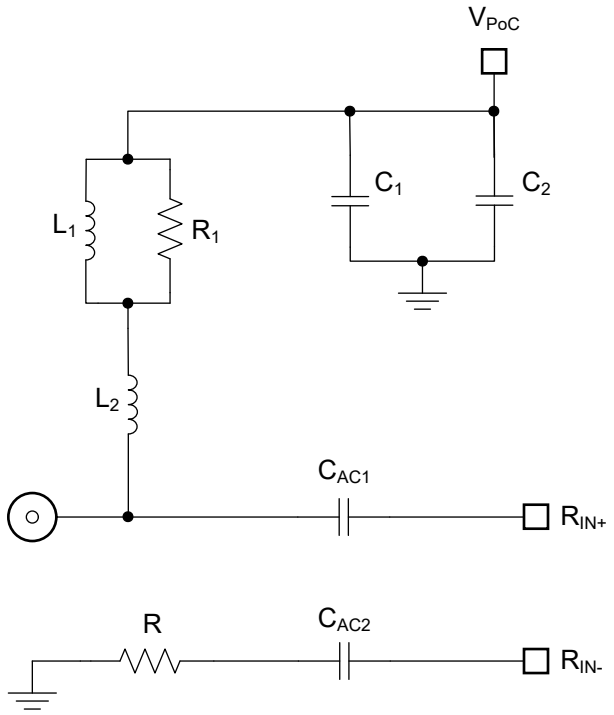


Figure 6-53. Murata PoC Network Number 27 Schematic

Table 6-54. Murata PoC Network 27 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3mm × 3mm x 1.4mm	LQH3NPH220MME	Murata
L2	Inductor, 1uH 2mm × 1.2mm x 1.6mm	LQW21FT1R0M0H	
R1	1.5kΩ		

6.5.28 Design 28

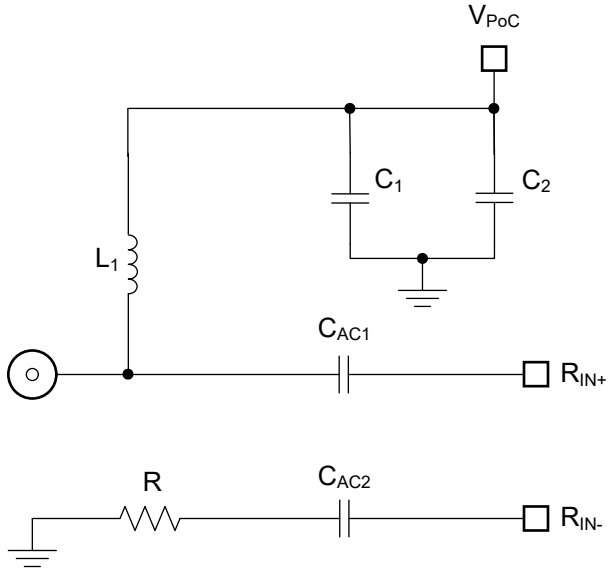


Figure 6-54. Murata PoC Network Number 28 Schematic

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Table 6-55. Murata PoC Network 28 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.2mm × 2.5mm x 2.3mm	LQW32FT220M2H	Murata

6.5.29 Design 29

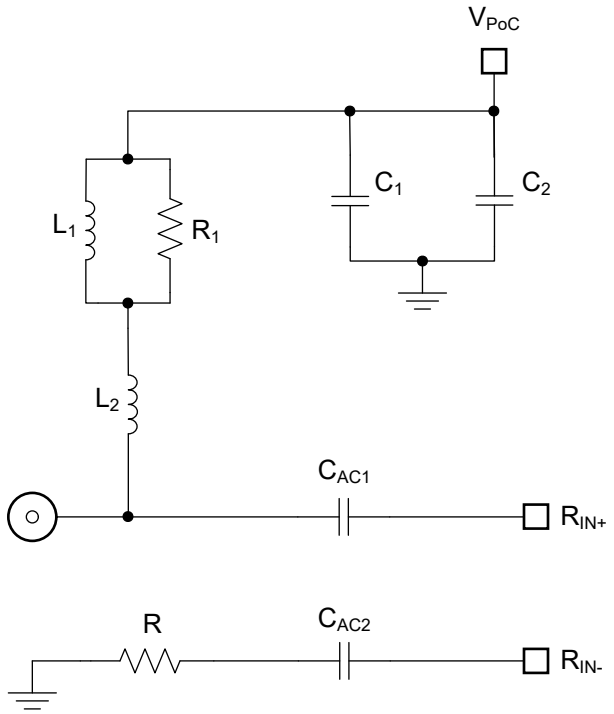


Figure 6-55. Murata PoC Network Number 29 Schematic

Table 6-56. Murata PoC Network 29 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3.2mm × 2.5mm x 2.3mm	LQW32FT470M0H	Murata
L2	Ferrite Bead, 8kΩ at 100 MHz, 0.7Ω DCR, 0805 SMD, AEC-Q200	BLM21HE802SH1	
R1	1kΩ		

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6.6 TDK FPD4 Networks

6.6.1 Design 1

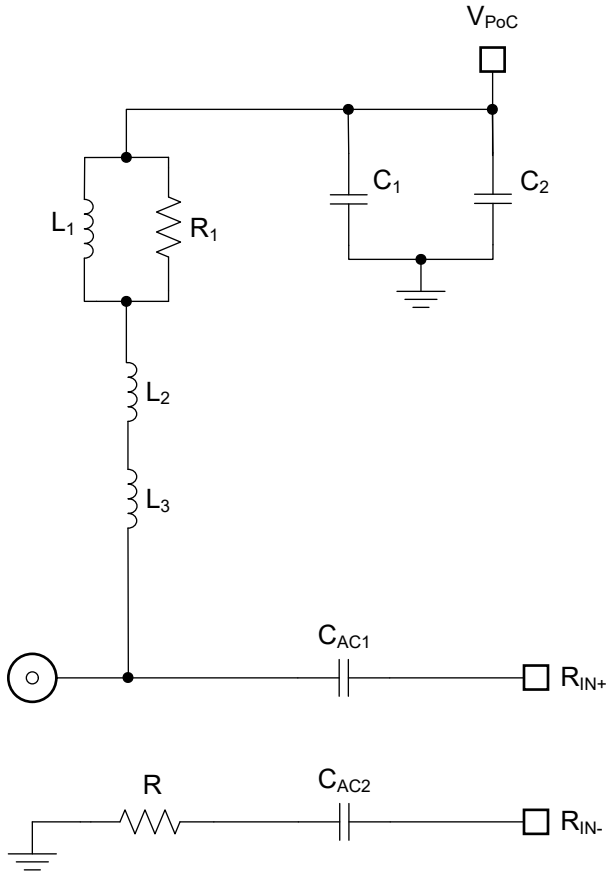


Figure 6-56. TDK PoC Network Number 1 Schematic

Table 6-57. TDK PoC Network 1 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL3225VT-100M -TL000	TDK
L2	Inductor, 1.5uH 2.2mm x 1.25mm x 1.65mm	ADL2012-1R5M-T01	
L3			
R1	1.2kΩ		

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6.6.2 Design 2

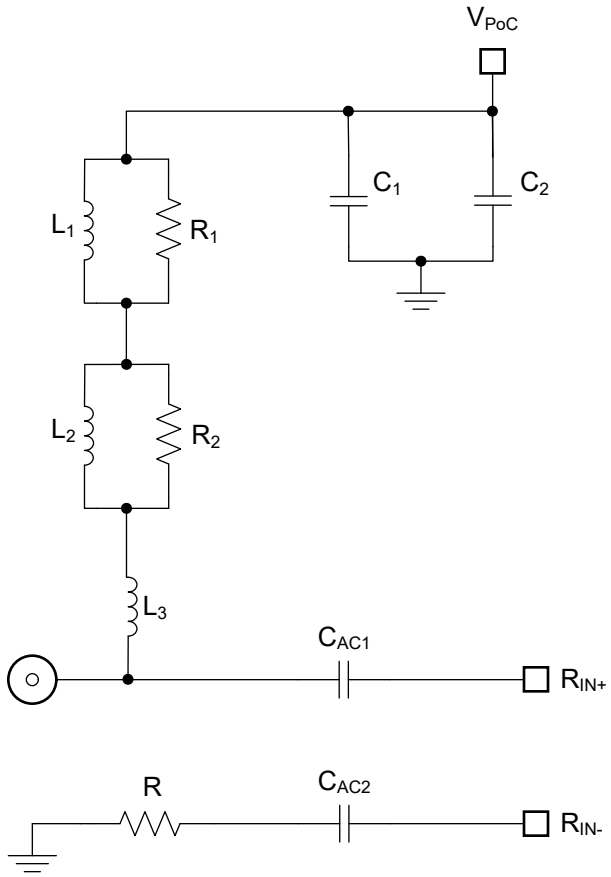


Figure 6-57. TDK PoC Network Number 2 Schematic

Table 6-58. TDK PoC Network 2 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADM32FSC-100M	TDK
L2	Inductor, 1.5uH 2.2mm x 1.25mm x 1.65mm	ADL2012-1R5M-T01	
L3			
R1	1.5kΩ		
R2			

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6.6.3 Design 3

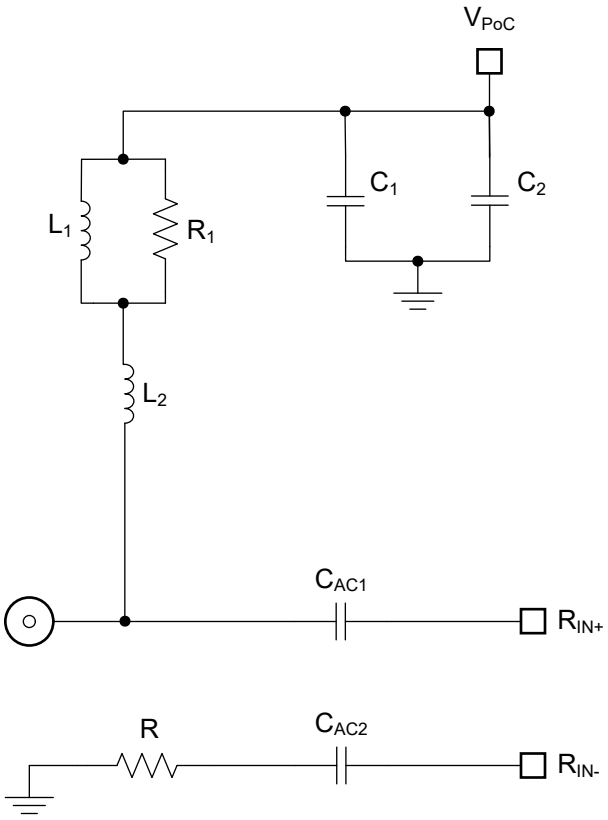


Figure 6-58. TDK PoC Network No. 3 Schematic

Table 6-59. TDK PoC Network 3 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL3225VT-100M	TDK
L2	Inductor, 2.2uH 2.2mm x 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1.2kΩ		

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6.6.4 Design 4

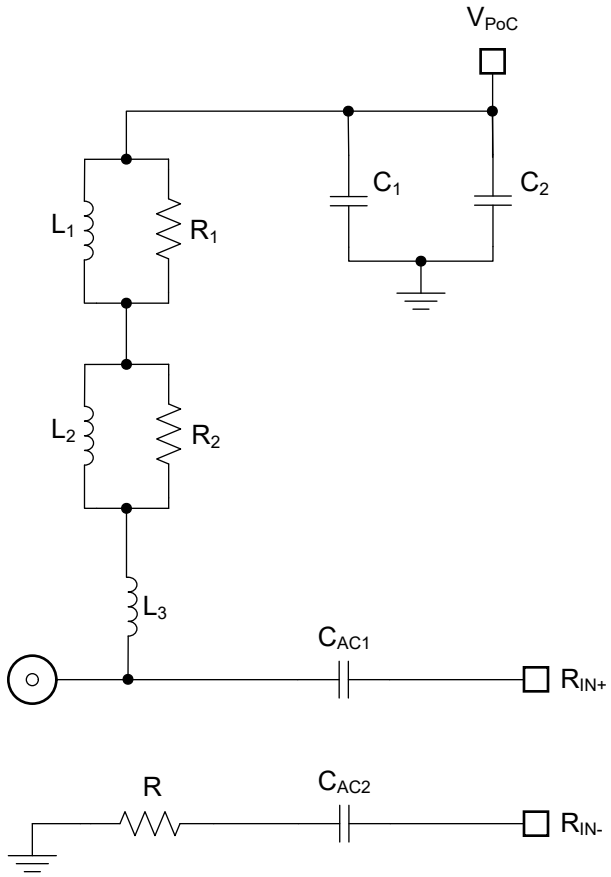


Figure 6-59. TDK PoC Network Number 4 Schematic

Table 6-60. TDK PoC Network 4 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm x 3.2mm x 3mm	ADM45FDC-100M	TDK
L2	Inductor, 2.2uH 3.2mm x 2.5mm x 2.5mm	ADL3225VM-2R2M-TL001	
L3			
R1	1.5kΩ		
R2			

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6.6.5 Design 5

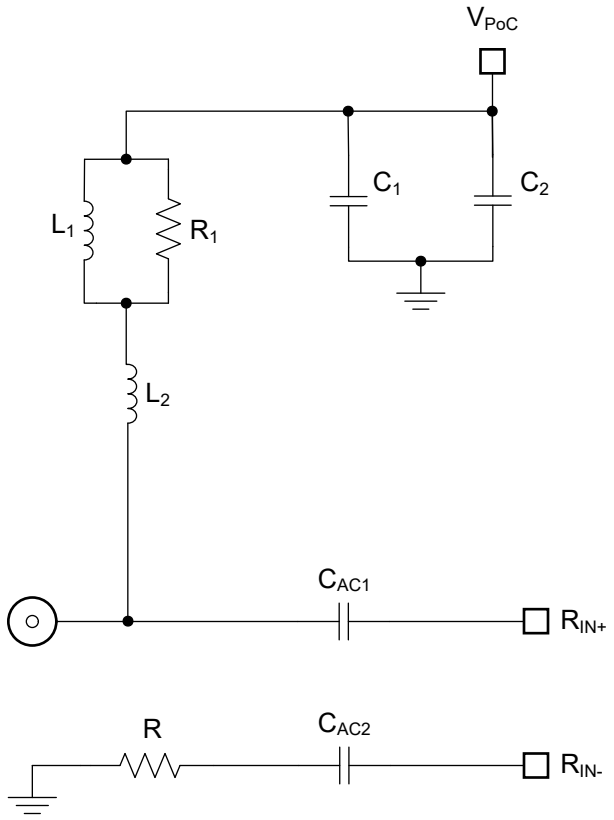


Figure 6-60. TDK PoC Network Number 5 Schematic

Table 6-61. TDK PoC Network 5 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADM32FSC-100M	TDK
L2	Inductor, 2.2uH 3.2mm x 2.5mm x 2.5mm	ADL3225VM-2R2M-TL001	
R1	1kΩ		

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6.6.6 Design 6

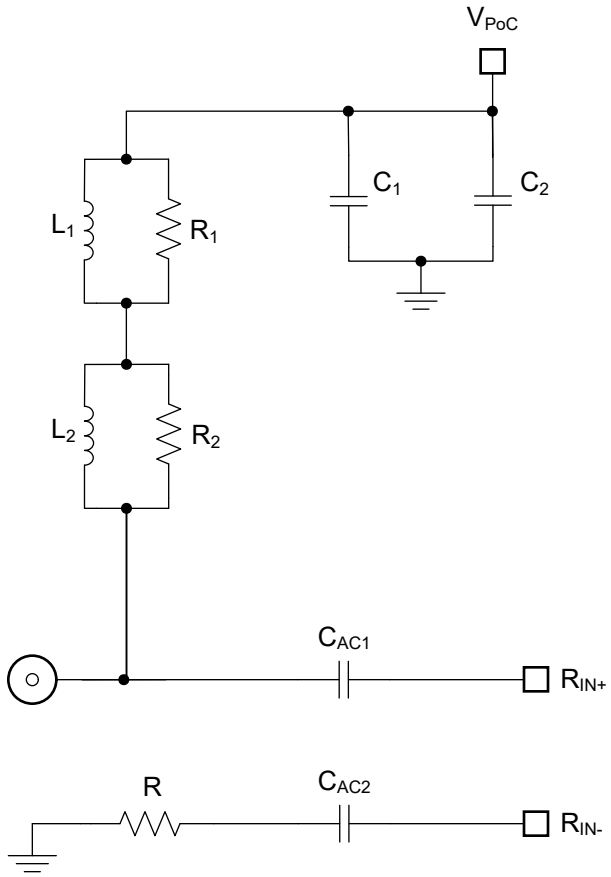


Figure 6-61. TDK PoC Network Number 6 Schematic

Table 6-62. TDK PoC Network 6 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3mm x 3mm x 1.5mm	VLS3015CX-470M-H	TDK
L2	Inductor, 2.2uH 2.2mm x 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1kΩ		
R2	2kΩ		

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6.6.7 Design 7

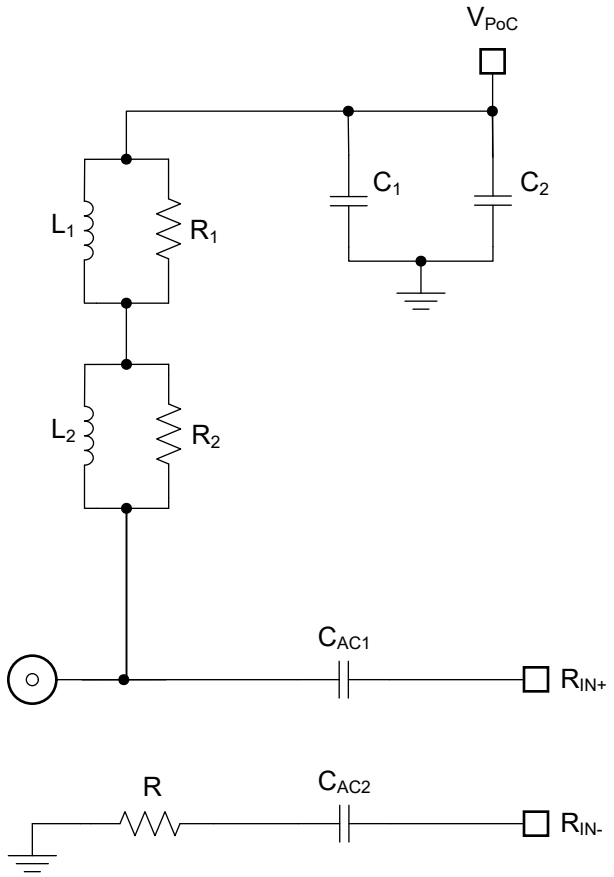


Figure 6-62. TDK PoC Network Number 7 Schematic

Table 6-63. TDK PoC Network 7 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 5mm x 5.3mm x 4.5mm	VLS5045EX-101M-H	TDK
L2	Inductor, 2.2uH 2.2mm x 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1kΩ		
R2	2kΩ		

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6.6.8 Design 8

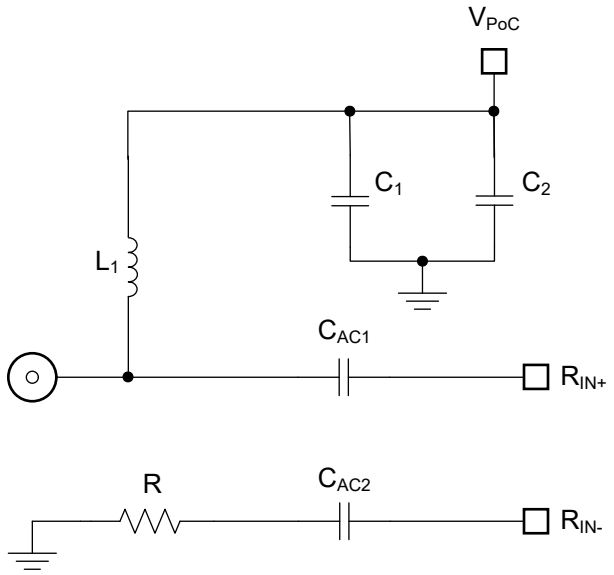


Figure 6-63. TDK PoC Network Number 8 Schematic

Table 6-64. TDK PoC Network 8 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 4.5mm x 2.4mm x 2.8mm	ADL4524VL-180M-TL000	TDK

6.6.9 Design 9

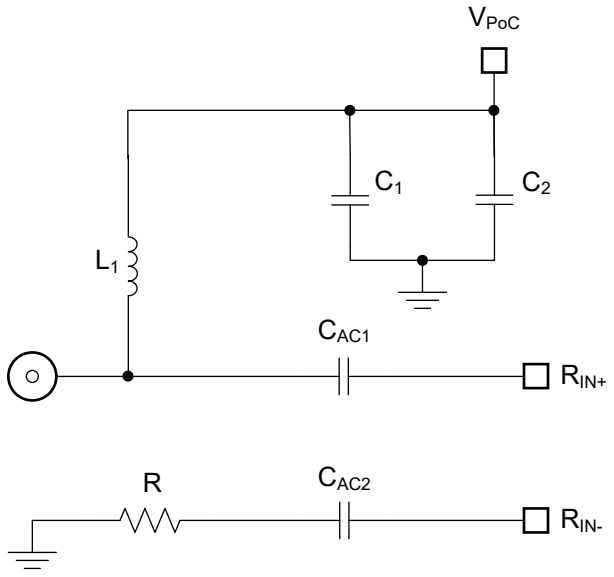


Figure 6-64. TDK PoC Network Number 9 Schematic

Table 6-65. TDK PoC Network 9 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 7.8mm x 2.7mm x 2.7mm	ADL8030VA-100M	TDK

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6.6.10 Design 10

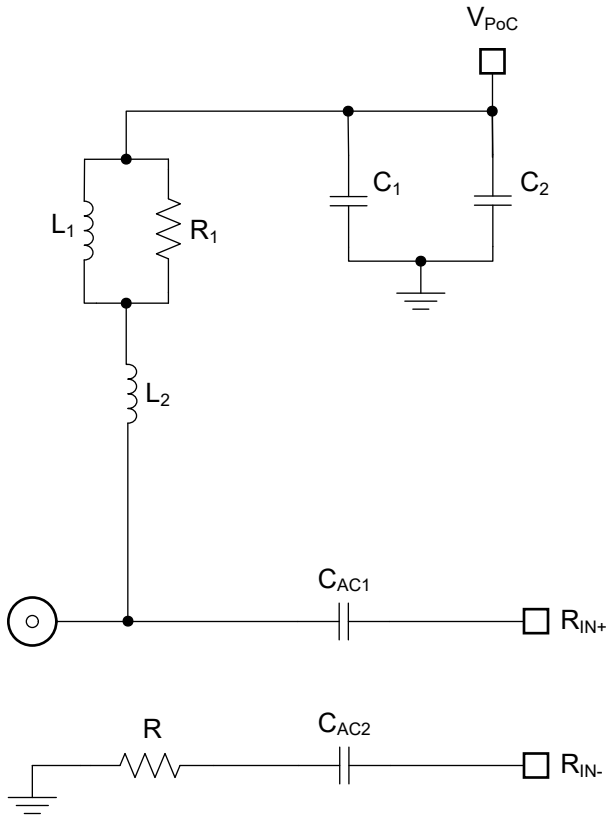


Figure 6-65. TDK PoC Network Number 10 Schematic

Table 6-66. TDK PoC Network 10 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm x 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 10uH 7.8mm x 2.7mm x 2.7mm	ADL8030VA-100M	
R1	1kΩ		

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6.6.11 Design 11

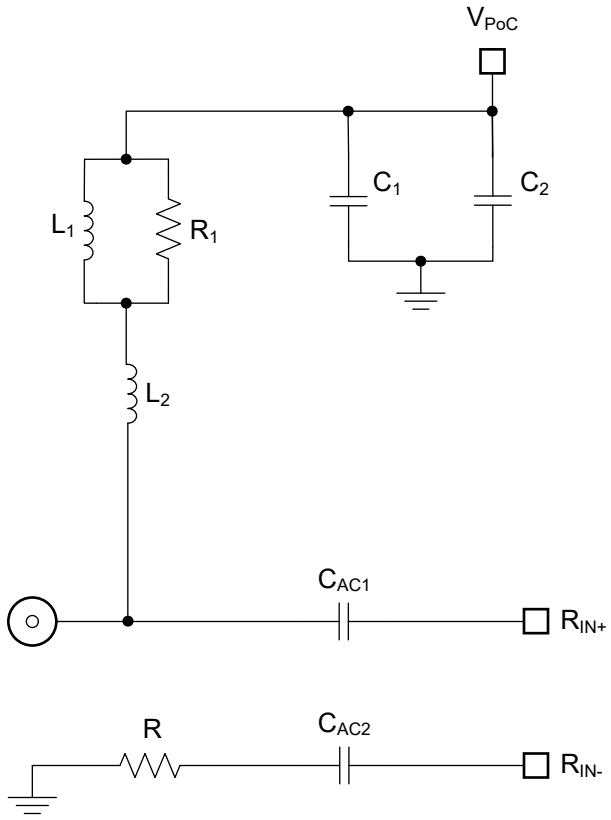


Figure 6-66. TDK PoC Network Number 11 Schematic

Table 6-67. TDK PoC Network 11 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 2.2uH 3mm x 3mm x 1.5mm	VLS3015CX-2R2M-H	TDK
L2	Inductor, 2.2uH 3.2mm x 2.5mm x 2.5mm	ADL3225VM-2R2M-TL001	
R1	1kΩ		

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6.6.12 Design 12

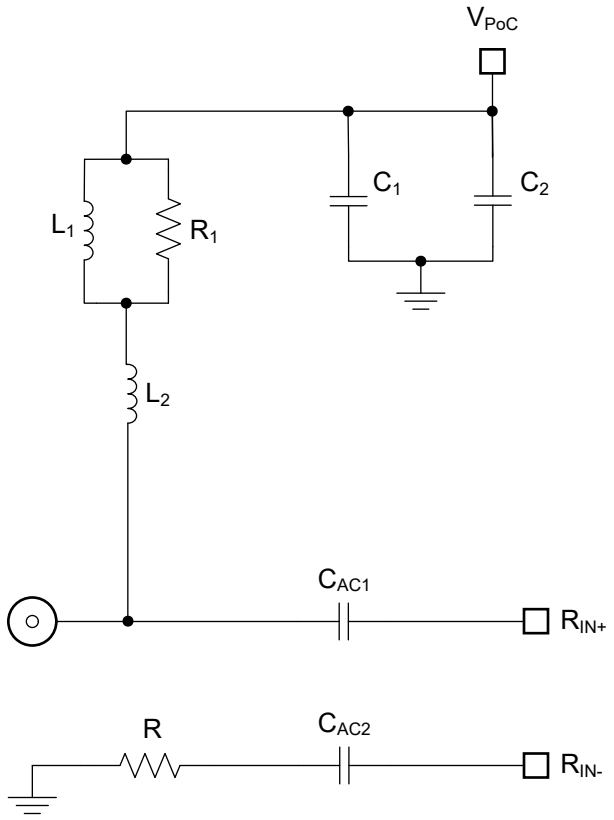


Figure 6-67. TDK PoC Network Number 12 Schematic

Table 6-68. TDK PoC Network 12 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-150M	TDK
L2	Inductor, 0.56uH 1.6mm x 0.8mm x 0.8mm	MLJ1608WGCR56NTD25	
R1	1.5kΩ		

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6.6.13 Design 13

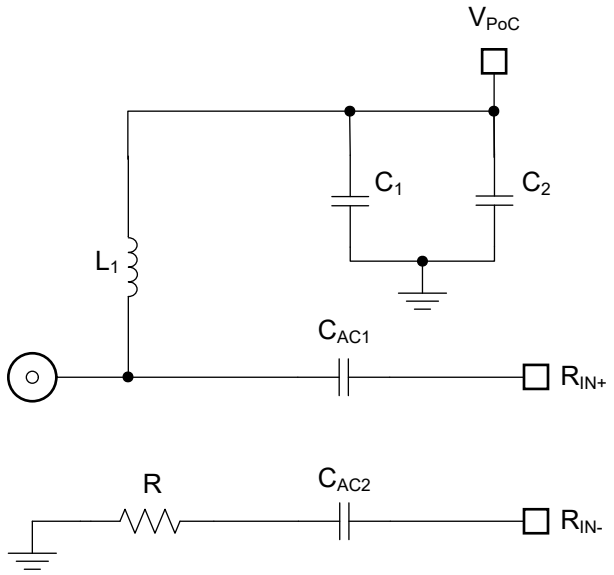


Figure 6-68. TDK PoC Network Number 13 Schematic

Table 6-69. TDK PoC Network 13 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm x 2.4mm x 2.8mm	ADL4524VL-100M-TL000	TDK

6.6.14 Design 14

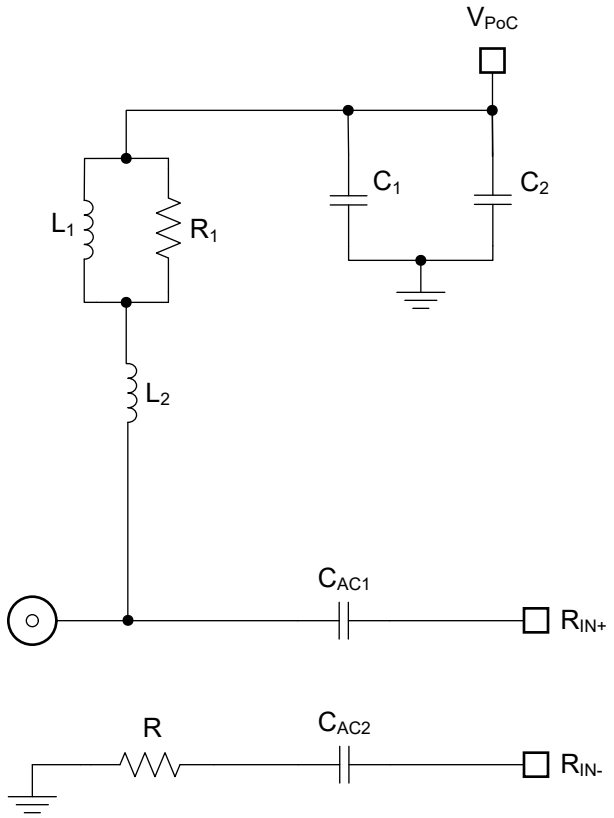


Figure 6-69. TDK PoC Network Number 14 Schematic

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Table 6-70. TDK PoC Network 14 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-150M	TDK
L2	Inductor, 1.5uH 2.2mm x 1.25mm x 1.65mm	ADL2012-1R5M-T01	
R1	1.5kΩ		

6.6.15 Design 15

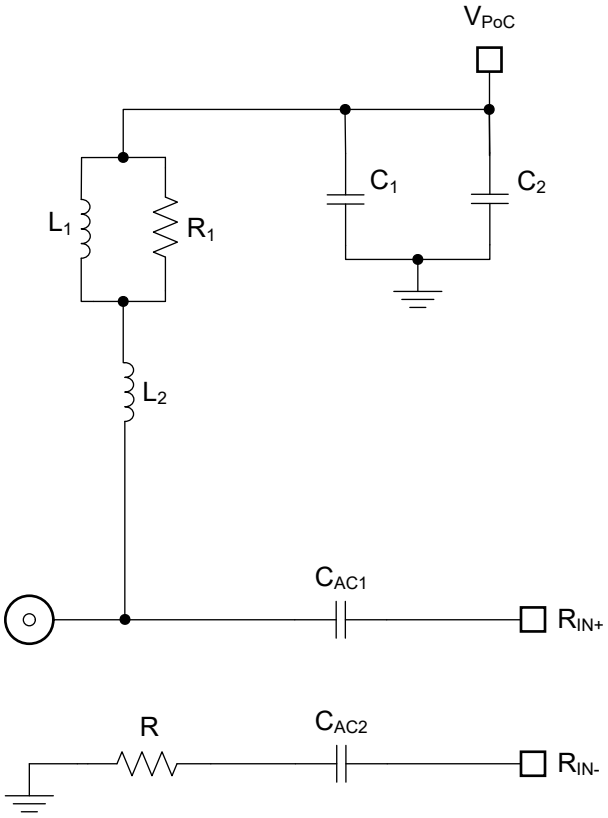


Figure 6-70. TDK PoC Network Number 15 Schematic

Table 6-71. TDK PoC Network 15 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm x 3mm x 1.5mm	VLS3015CX-100M-H	TDK
L2	Inductor, 2.2uH 2.2mm x 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1kΩ		

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6.6.16 Design 16

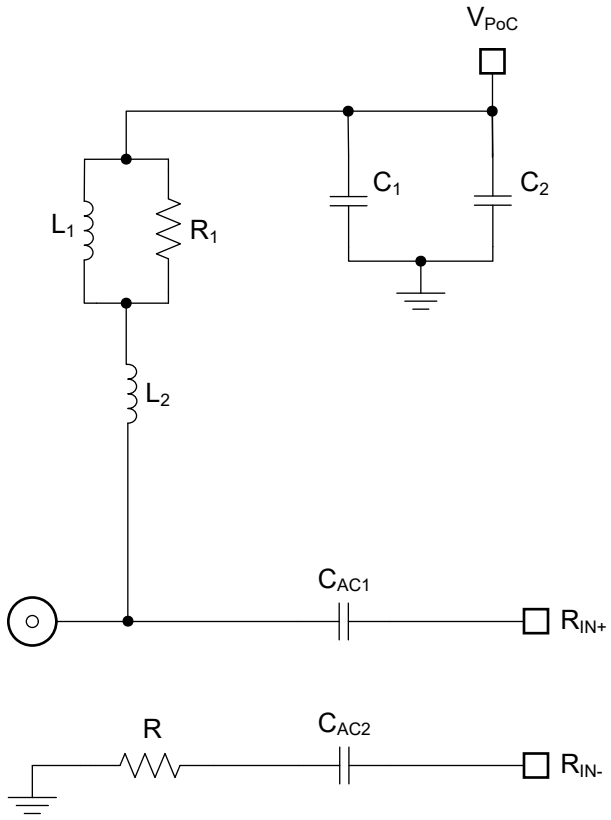


Figure 6-71. TDK PoC Network Number 16 Schematic

Table 6-72. TDK PoC Network 16 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-100M	TDK
L2	Inductor, 0.56uH 1.6mm x 0.8mm x 0.8mm	MLJ1608WGCR56NTD25	
R1	1.5kΩ		

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6.6.17 Design 17

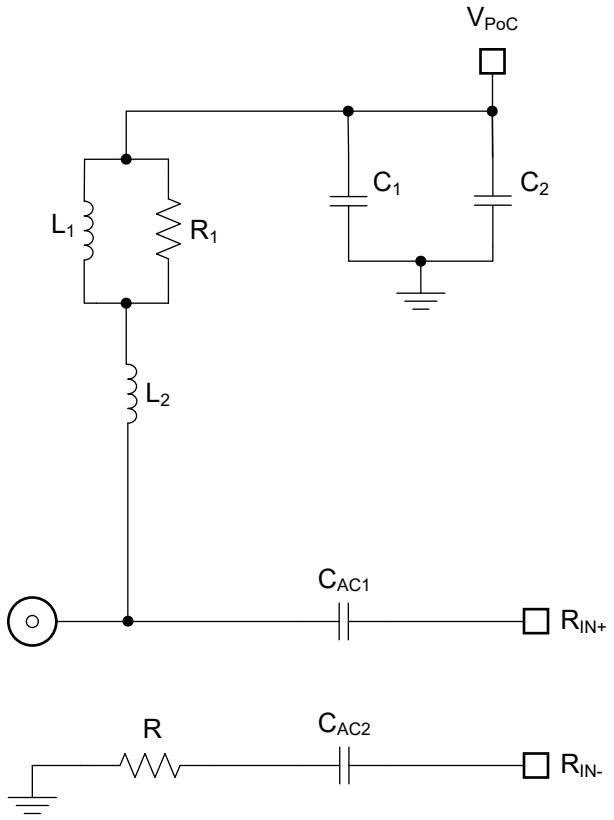


Figure 6-72. TDK PoC Network Number 17 Schematic

Table 6-73. TDK PoC Network 17 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-100M	TDK
L2	Inductor, 0.47uH 2.2mm x 1.25mm x 1.65mm	ADL2012-R47M-T01	
R1	1kΩ		

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6.6.18 Design 18

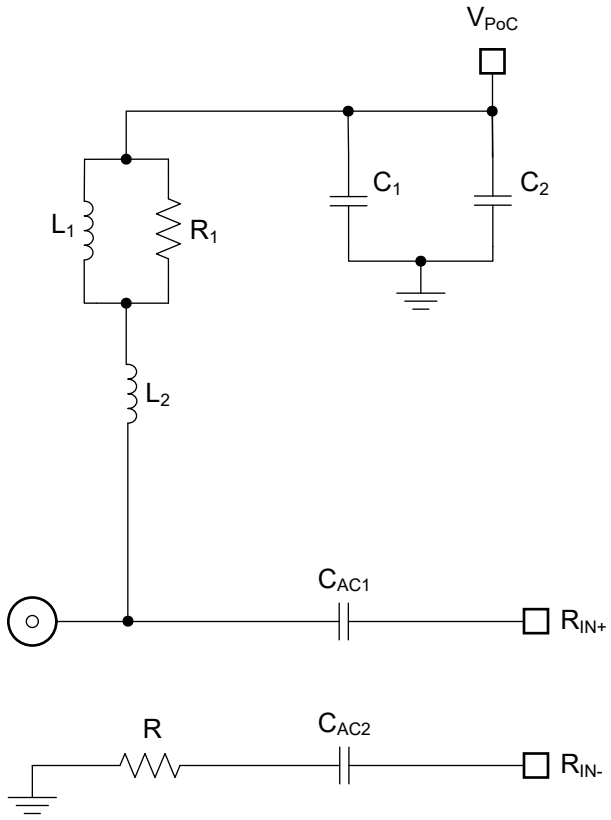


Figure 6-73. TDK PoC Network Number 18 Schematic

Table 6-74. TDK PoC Network 18 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4.5mm x 3.2mm x 3.2mm	ADL4532VK-100M-TL000	TDK
L2	Inductor, 0.47uH 2.2mm x 1.25mm x 1.65mm	ADL2012-R47M-T01	
R1	1kΩ		

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6.6.19 Design 19

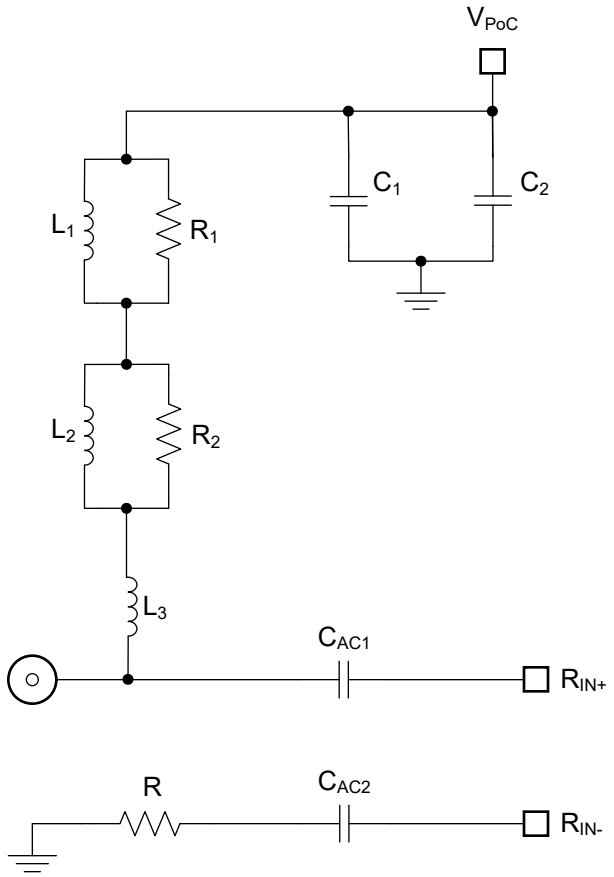


Figure 6-74. TDK PoC Network Number 19 Schematic

Table 6-75. TDK PoC Network 19 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 5mm x 5.3mm x 3mm	VLS5030EX-150M-D	TDK
L2	Inductor, 1.5uH 2mm x 1.25mm x 1mm	TFM201210ALMA1R5MTAA	
L3	Inductor, 0.8uH 2.2mm x 1.25mm x 1.75mm	ADL2012-R80M-T01	
R1	1.5kΩ		
R2	1kΩ		

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6.6.20 Design 20

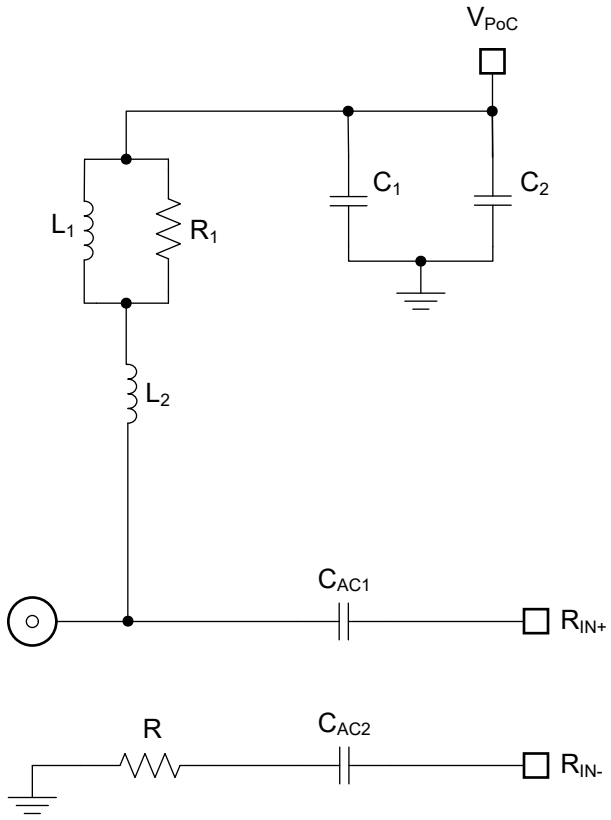


Figure 6-75. TDK PoC Network Number 20 Schematic

Table 6-76. TDK PoC Network 20 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 7.8mm x 2.7mm x 2.7mm	ADL8030VA-680M	TDK
L2	Inductor, 0.56uH 1.6mm x 0.8mm x 0.8mm	MLJ1608WGCR56NTD25	
R1	1kΩ		

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6.6.21 Design 21

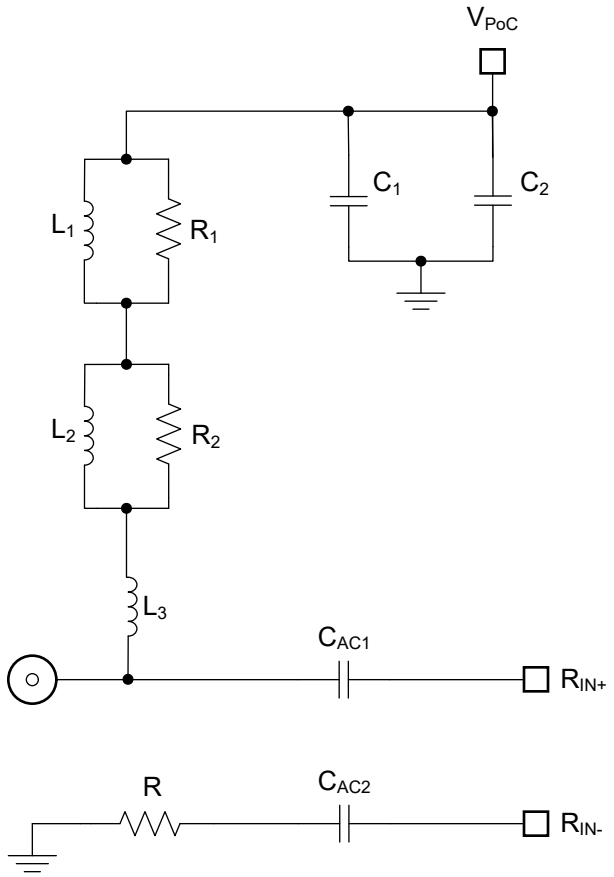


Figure 6-76. TDK PoC Network Number 21 Schematic

Table 6-77. TDK PoC Network 21 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm x 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 3.3uH 3mm x 3mm x 1.5mm	VLS3015CX-3R3M-H	
L3	Inductor, 2.2uH 2.2mm x 1.25mm x 1.65mm	ADL2012-2R2M-T01	
R1	1.5kΩ		
R2	1kΩ		

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6.6.22 Design 22

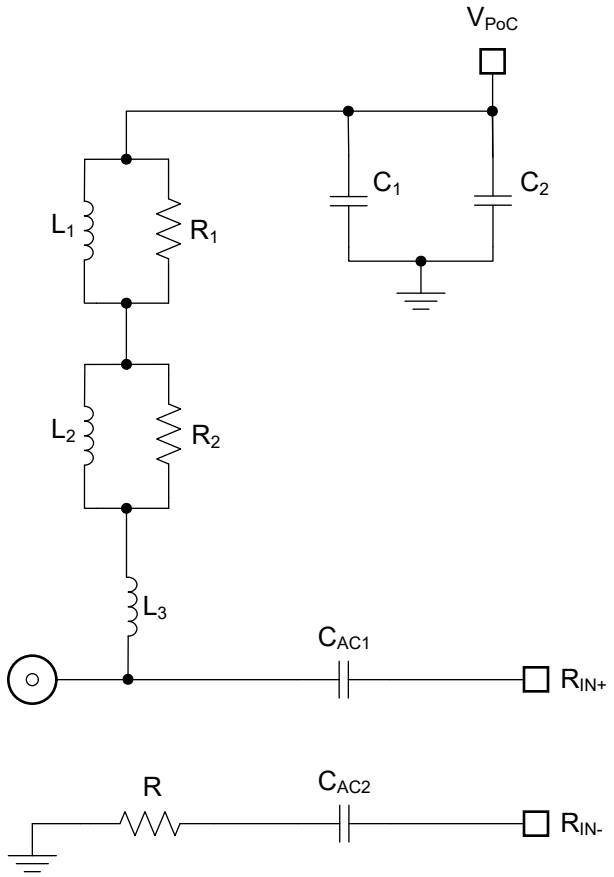


Figure 6-77. TDK PoC Network Number 22 Schematic

Table 6-78. TDK PoC Network 22 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm x 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-100M	
L3	Inductor, 0.56uH 1.6mm x 0.8mm x 0.95mm	MLJ1608WGCR56NTD25	
R1	1.5kΩ		
R2	1kΩ		

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6.6.23 Design 23

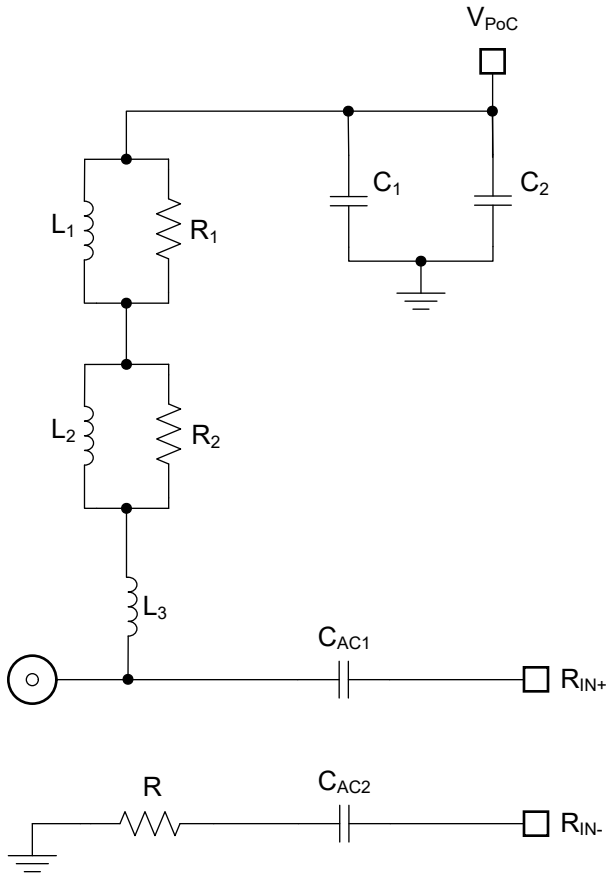


Figure 6-78. TDK PoC Network Number 23 Schematic

Table 6-79. TDK PoC Network 23 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 5.3mm x 5mm x 3mm	VLS5030EX-680M-D	TDK
L2	Inductor, 10uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-100M	
L3	Inductor, 0.47uH 2.2mm x 1.25mm x 1.65mm	ADL2012-R47M-T01	
R1	1.5kΩ		
R2	1kΩ		

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6.6.24 Design 24

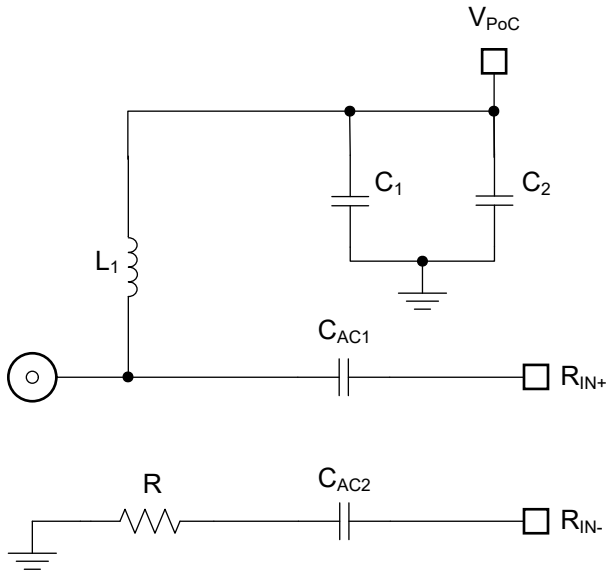


Figure 6-79. TDK PoC Network Number 24 Schematic

Table 6-80. TDK PoC Network 24 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.2mm x 2.5mm x 2.3mm	ADL3225V-220MS-TL000	TDK

6.6.25 Design 25

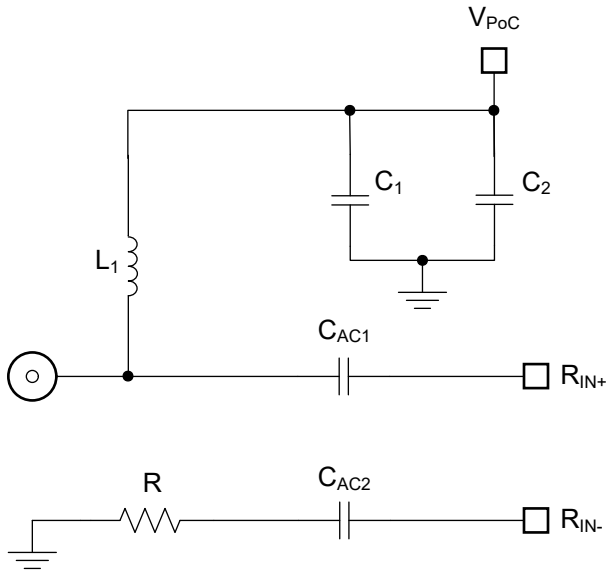


Figure 6-80. TDK PoC Network Number 25 Schematic

Table 6-81. TDK PoC Network 25 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 18uH 3.2mm x 2.5mm x 2.5mm	ADL32VHC-180MF	TDK

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6.7 Coilcraft FPD4 Networks

6.7.1 Design 1

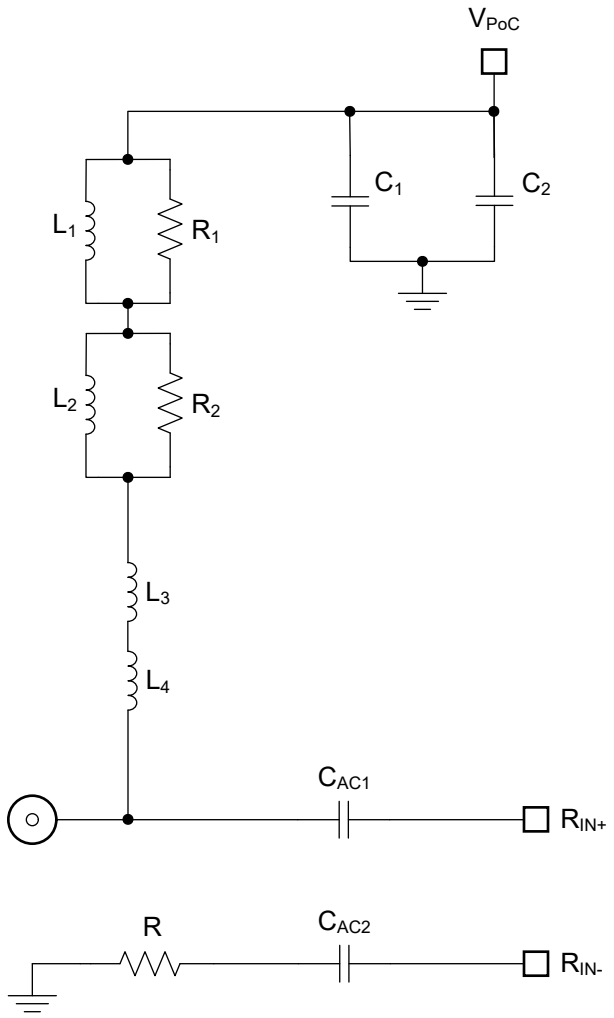


Figure 6-81. Coilcraft PoC Network Number 1 Schematic

Table 6-82. Coilcraft PoC Network 1 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 5.1mm x 5.1mm x 3.1mm	MSS5131H-104	Coilcraft
L2	Inductor, 6.8uH 3.3mm x 2.67mm x 3mm	1210POC-682	
L3	Inductor, 100nH 1.14mm x 0.635mm x 0.71mm	PFL1005-101	
L4			
R1	3kΩ		
R2	3.6kΩ		

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6.7.2 Design 2

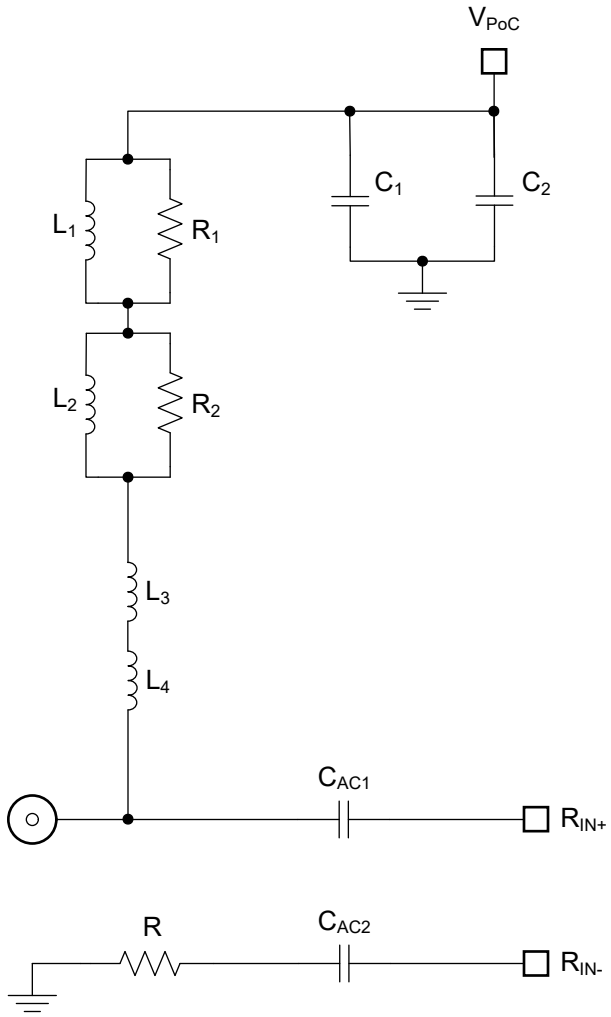


Figure 6-82. Coilcraft PoC Network Number 2 Schematic

Table 6-83. Coilcraft PoC Network 2 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 3.9mm x 3.9mm x 1.7mm	LPS4018-104	Coilcraft
L2	Inductor, 6.8uH 3.2mm x 1.4mm x 2.36mm	1205POC-682	
L3	Inductor, 0.18uH 1.14mm x 0.635mm x 0.71mm	PFL1005-181	
L4			
R1	2.61kΩ		
R2	3.6kΩ		

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6.7.3 Design 3

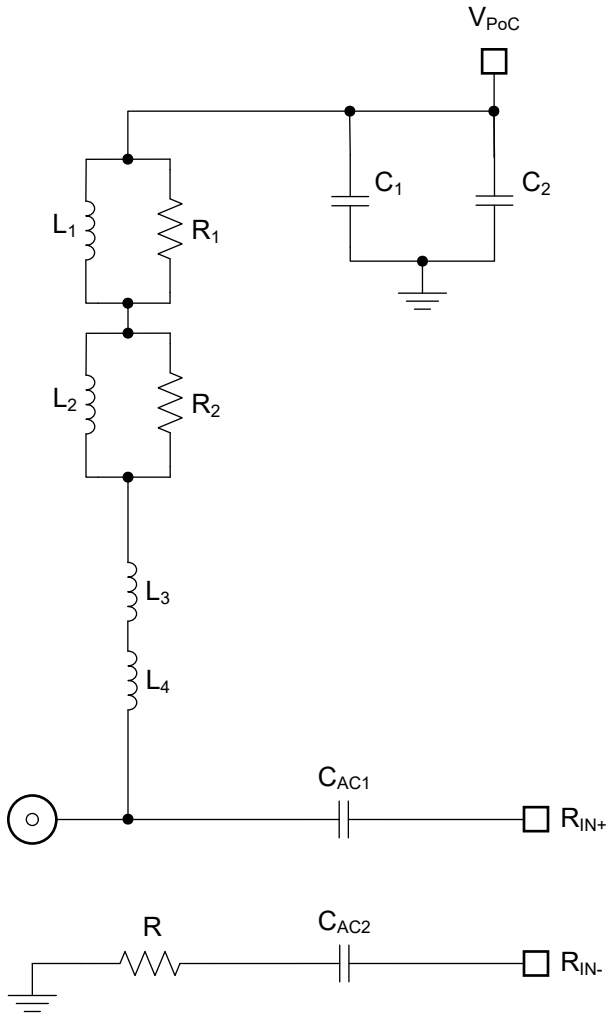


Figure 6-83. Coilcraft PoC Network Number 3 Schematic

Table 6-84. Coilcraft PoC Network 3 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 10mm x 10mm x 4.8mm	MSS1048T-104	Coilcraft
L2	Inductor, 10uH 5.87mm x 4.98mm x 3.81mm	1812PS-103	
L3	Inductor, 0.47uH 2.2mm x 1.45mm x 1mm	PFL2010-471	
L4	Inductor, 56nH 1.11mm x 0.66mm x 0.66mm	0402DF-560	
R1	2.61kΩ		
R2	3kΩ		

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6.7.4 Design 4

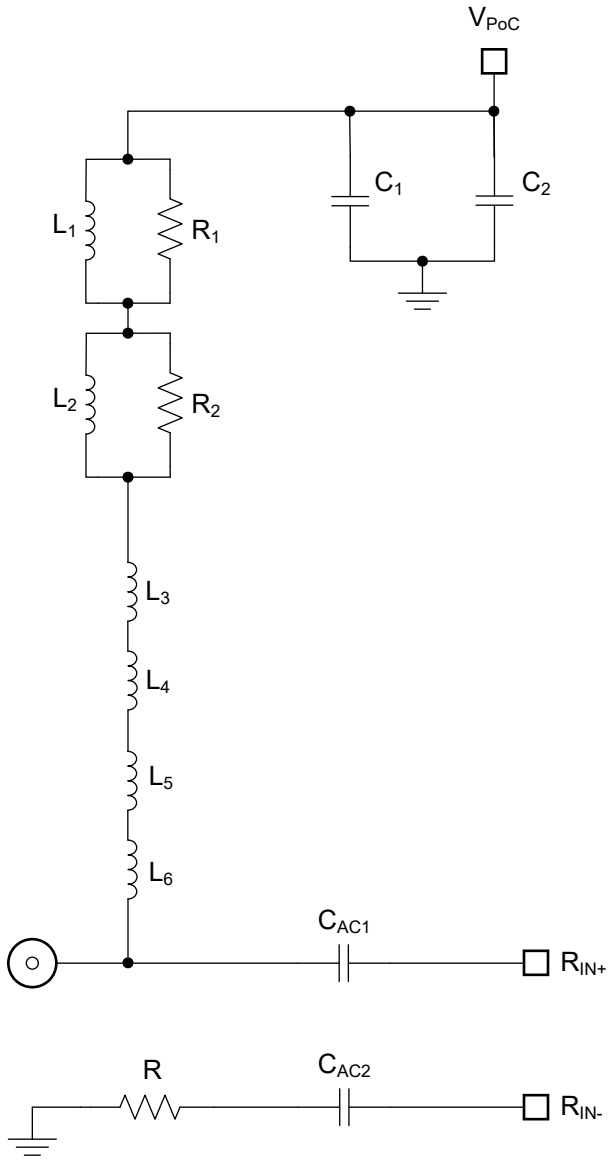


Figure 6-84. Coilcraft PoC Network Number 4 Schematic

Table 6-85. Coilcraft PoC Network 4 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 10mm x 10mm x 4.8mm	MSS1048T-104	Coilcraft
L2	Inductor, 22uH 6.1mm x 6.1mm x 2.85mm	MSS6132T-223	
L3	Inductor, 5.6uH 5.87mm x 4.98mm x 3.81mm	1812PS-562	
L4	Inductor, 0.47uH 2.2mm x 1.45mm x 1mm	PFL2010-471	
L5	Inductor, 20nH 1.11mm x 0.66mm x 0.66mm	0402DF-200	
L6			
R1	2kΩ		
R2	3kΩ		

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6.7.5 Design 5

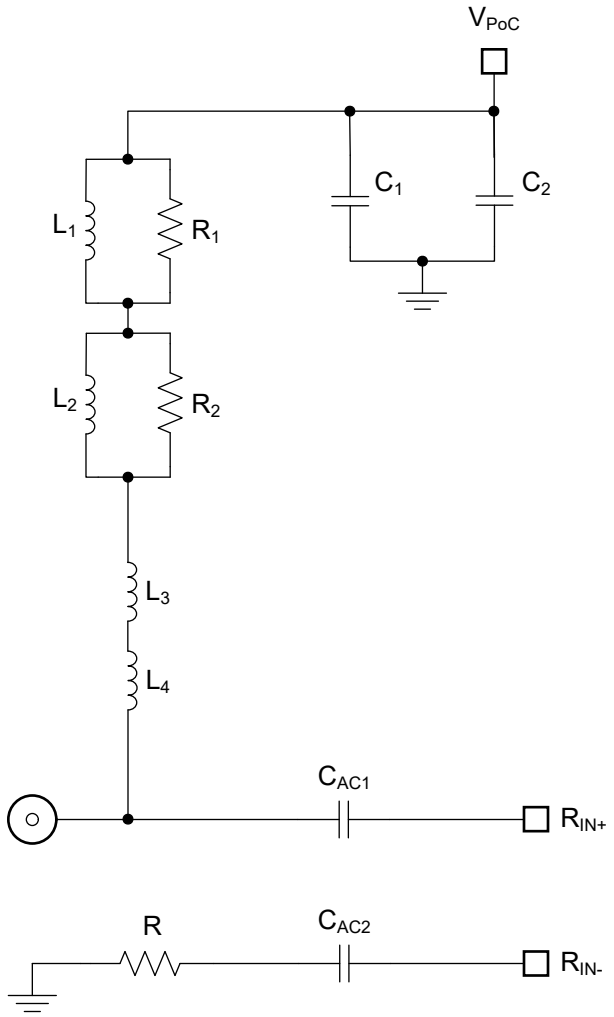


Figure 6-85. Coilcraft PoC Network Number 5 Schematic

Table 6-86. Coilcraft PoC Network 5 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 3.9mm x 3.9mm x 1.7mm	LPS4018-104	Coilcraft
L2	Inductor, 6.8uH 3.2mm x 1.4mm x 2.36mm	1205POC-682	
L3	Inductor, 1uH 1.8mm x 1.07mm 0.95mm	PFL1609-102	
L4	Inductor, 0.18uH 1.14mm x 0.635mm x 0.71mm	PFL1005-181	
R1	2.6kΩ		
R2	3.6kΩ		

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6.7.6 Design 6

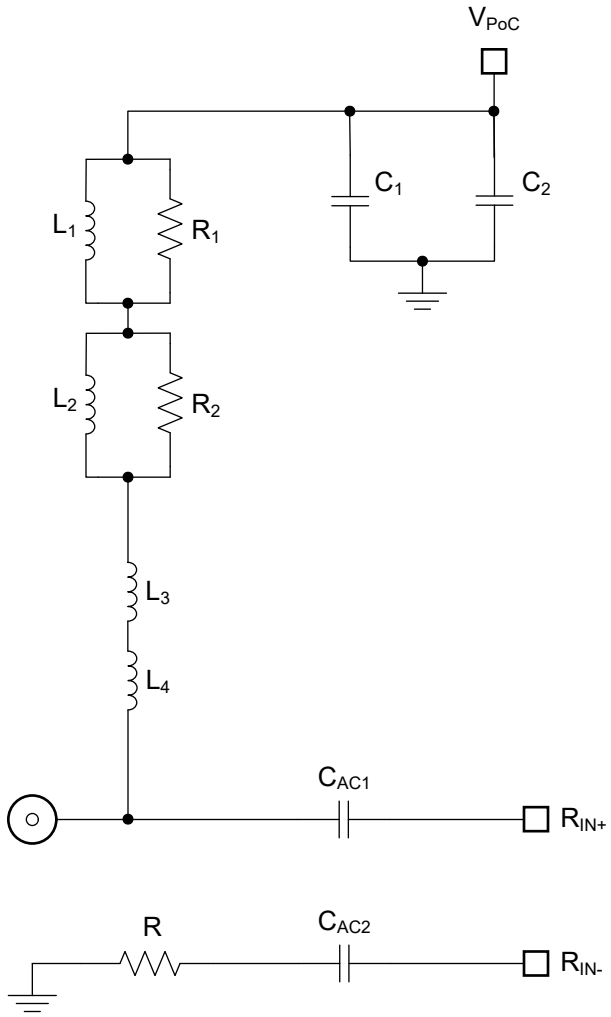


Figure 6-86. Coilcraft PoC Network Number 6 Schematic

Table 6-87. Coilcraft PoC Network 6 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 3.9mm x 3.9mm x 4mm	LPS4040-104	Coilcraft
L2	Inductor, 6.8uH 3.3mm x 2.67mm x 3mm	1210POC-682	
L3	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.47uH 1.8mm x 1.07mm x 0.95mm	PFL1609-471	
R1	2.61kΩ		
R2	3.6kΩ		

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6.7.7 Design 7

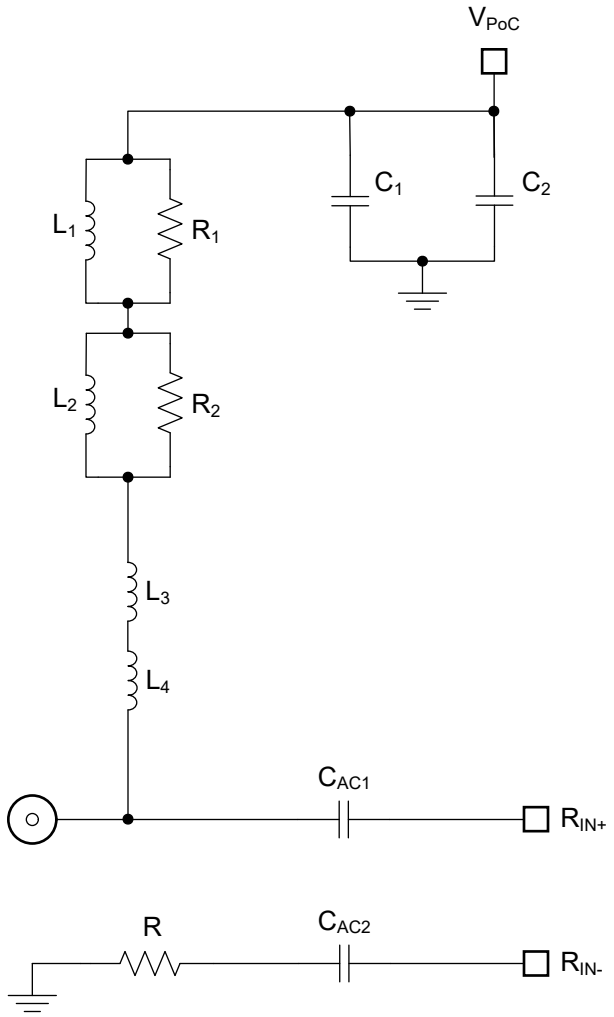


Figure 6-87. Coilcraft PoC Network Number 7 Schematic

Table 6-88. Coilcraft PoC Network 7 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 7.3mm x 7.3mm x 4.1mm	MSS7341T-104	Coilcraft
L2	Inductor, 6.8uH 3.3mm x 2.67mm x 3mm	1210POC-682	
L3	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.18uH 1.14mm x 0.635mm x 0.71mm	PFL1005-181	
R1	4kΩ		
R2	4kΩ		

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6.7.8 Design 8

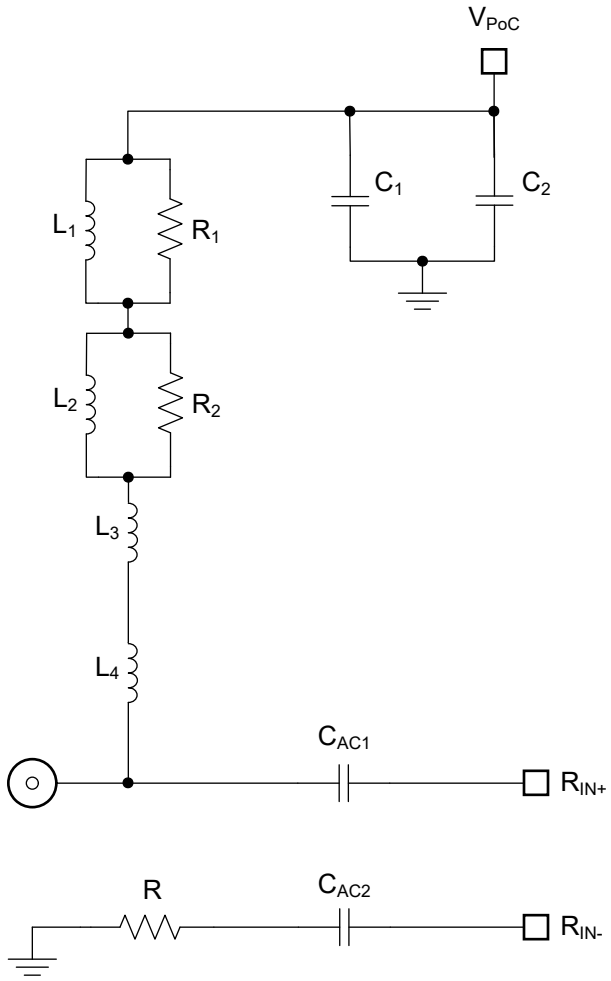


Figure 6-88. Coilcraft PoC Network Number 8 Schematic

Table 6-89. Coilcraft PoC Network 8 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 100uH 10mm x 10mm x 4.8mm	MSS1048T-104	Coilcraft
L2	Inductor, 10uH 5.87mm x 4.98mm x 3.81mm	1812PS-103	
L3	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
L4	Inductor, 0.47uH 1.8mm x 1.07mm x 0.95mm	PFL1609-471	
R1	2.61kΩ		
R2	3kΩ		

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6.7.9 Design 9

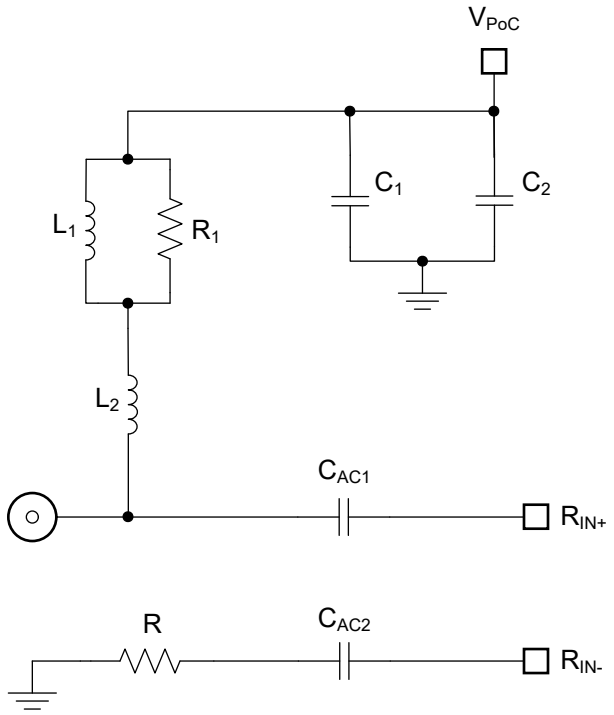


Figure 6-89. Coilcraft PoC Network Number 9 Schematic

Table 6-90. Coilcraft PoC Network 9 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.3mm x 2.67mm x 3mm	1210POC-223	Coilcraft
L2	Inductor, 0.56uH 1.14mm x 0.635mm x 0.71mm	PFL1005-561	
R1	5.1kΩ		

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6.7.10 Design 10

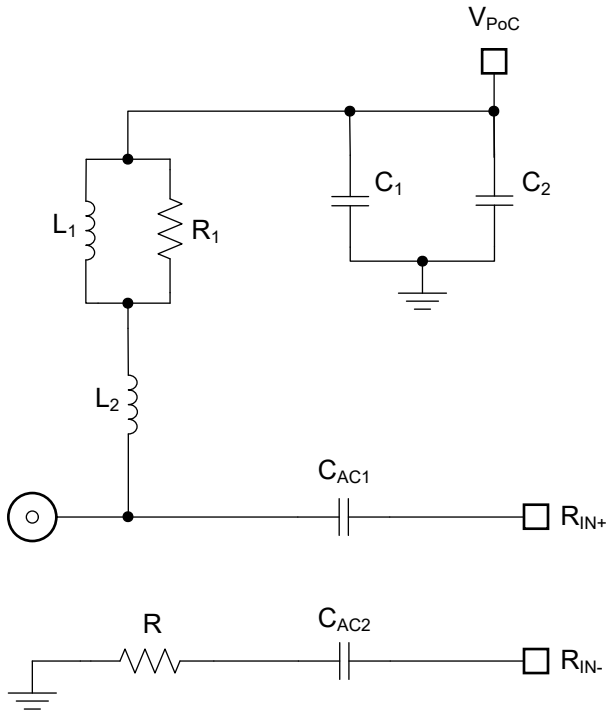


Figure 6-90. Coilcraft PoC Network Number 10 Schematic

Table 6-91. Coilcraft PoC Network 10 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.3mm x 2.67mm x 3mm	1210POC-223	Coilcraft
L2	Inductor, 0.56uH 1.8mm x 1.07mm x 0.95mm	PFL1609-561	
R1	5.1kΩ		

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6.7.11 Design 11

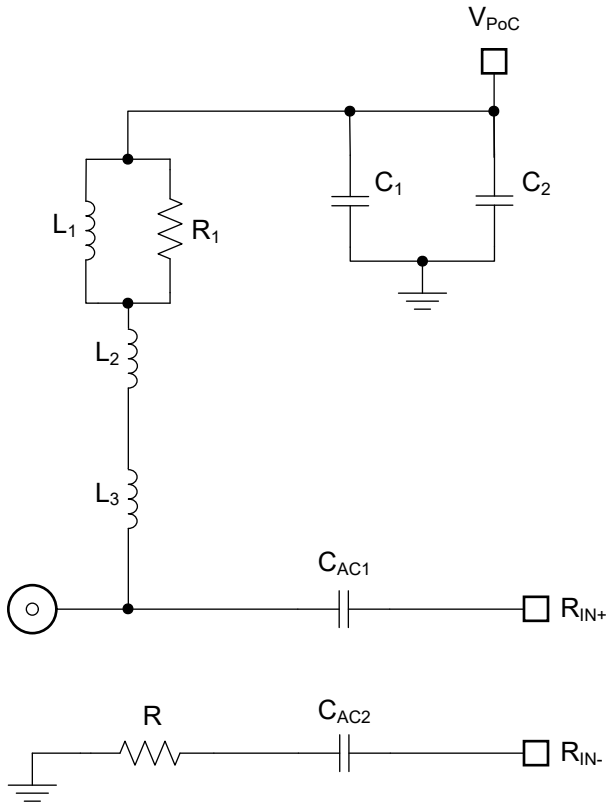


Figure 6-91. Coilcraft PoC Network Number 11 Schematic

Table 6-92. Coilcraft PoC Network 11 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 5.87mm x 4.98mm x 3.81mm	1812PS-103	Coilcraft
L2	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
L3	Inductor, 0.47uH 1.8mm x 1.07mm x 0.95mm	PFL1609-471	
R1	3kΩ		

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6.7.12 Design 12

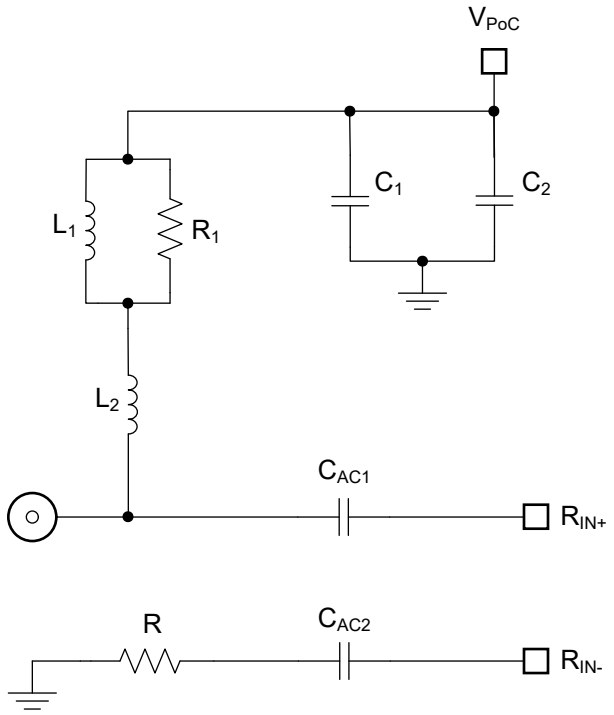


Figure 6-92. Coilcraft PoC Network Number 12 Schematic

Table 6-93. Coilcraft PoC Network 12 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.2mm x 1.4mm x 2.36mm	1205POC-682	Coilcraft
L2	Inductor, 1uH 1.8mm x 1.07mm x 0.95mm	PFL1609-102	
R1	3.6kΩ		

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6.7.13 Design 13

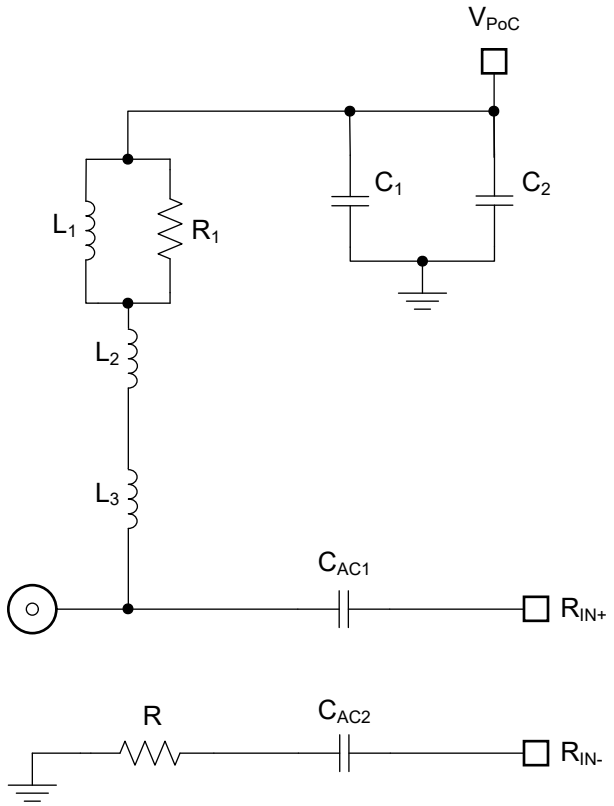


Figure 6-93. Coilcraft PoC Network Number 13 Schematic

Table 6-94. Coilcraft PoC Network 13 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.2mm x 1.4mm x 2.36mm	1205POC-682	Coilcraft
L2	Inductor, 1uH 1.8mm x 1.07mm x 0.95mm	PFL1609-102	
L3	Inductor, 0.18uH 1.14mm x 0.635mm x 0.71mm	PFL1005-181	
R1	3.6kΩ		

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6.7.14 Design 14

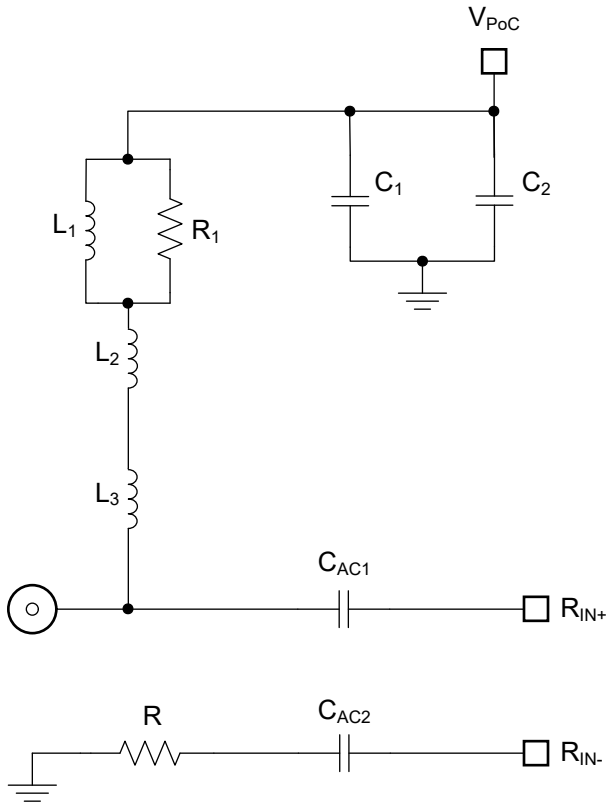


Figure 6-94. Coilcraft PoC Network Number 14 Schematic

Table 6-95. Coilcraft PoC Network 14 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.3mm x 2.67mm x 3mm	1210POC-682	Coilcraft
L2	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
L3	Inductor, 0.18uH 1.14mm x 0.635mm x 0.71mm	PFL1005-181	
R1	4kΩ		

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6.7.15 Design 15

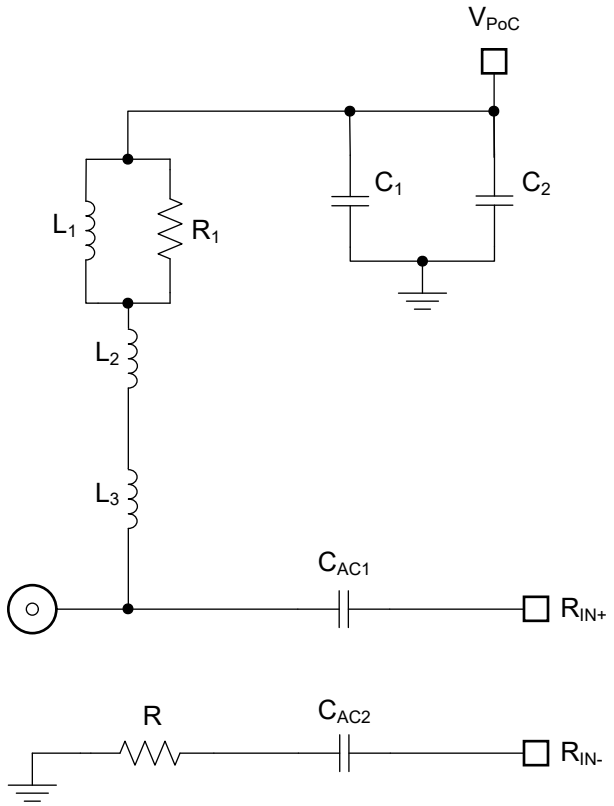


Figure 6-95. Coilcraft PoC Network Number 15 Schematic

Table 6-96. Coilcraft PoC Network 15 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 4.95mm x 3.43mm x 3.81mm	1812POC-682	Coilcraft
L2	Inductor, 0.68uH 2.2mm x 1.45mm x 1.5mm	PFL2015-681	
L3	Inductor, 0.56uH 2.2mm x 1.45mm x 1.5mm	PFL2015-561	
R1	3.1kΩ		

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6.7.16 Design 16

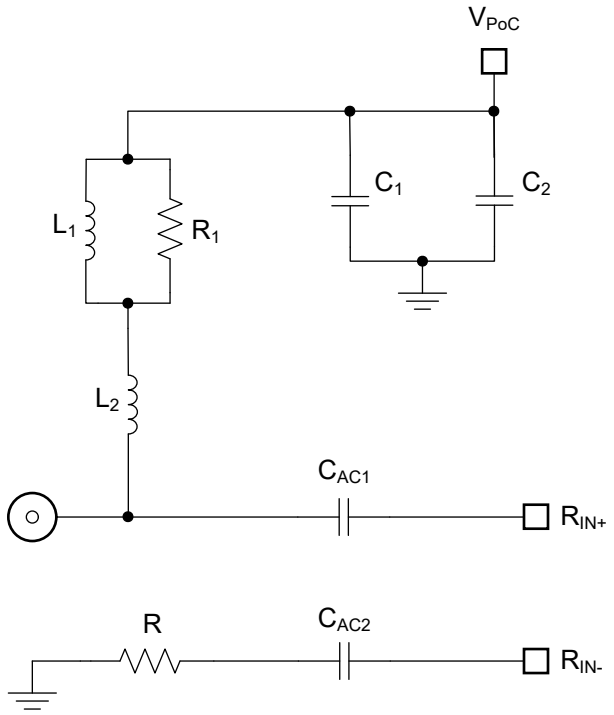


Figure 6-96. Coilcraft PoC Network Number 16 Schematic

Table 6-97. Coilcraft PoC Network 16 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 3.3mm x 2.67mm x 3.0mm	1210POC-153	Coilcraft
L2	Inductor, 0.56uH 1.8mm x 1.07mm x 0.95mm	PFL1609-561	
R1	5.1kΩ		

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6.7.17 Design 17

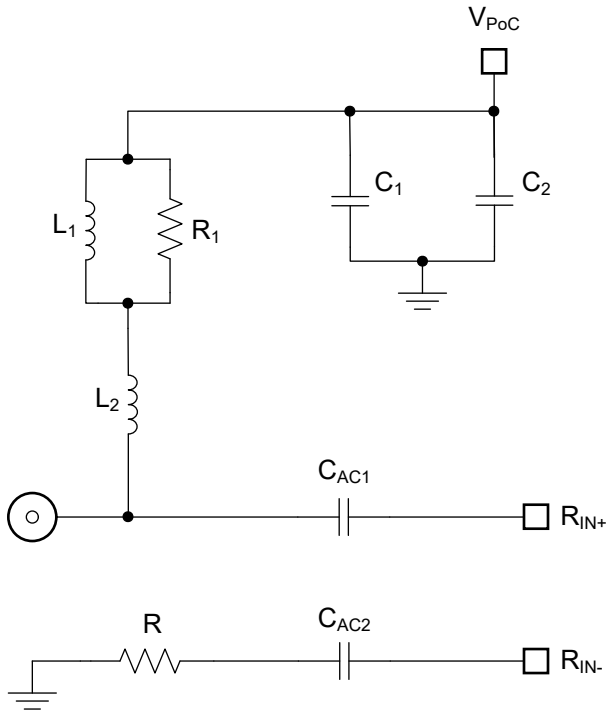


Figure 6-97. Coilcraft PoC Network Number 17 Schematic

Table 6-98. Coilcraft PoC Network 17 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.3mm x 2.67mm x 3.0mm	1210POC-682	Coilcraft
L2	Inductor, 1uH 2.2mm x 1.45mm x 1.5mm	PFL2015-102	
R1	4.1kΩ		

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6.7.18 Design 18

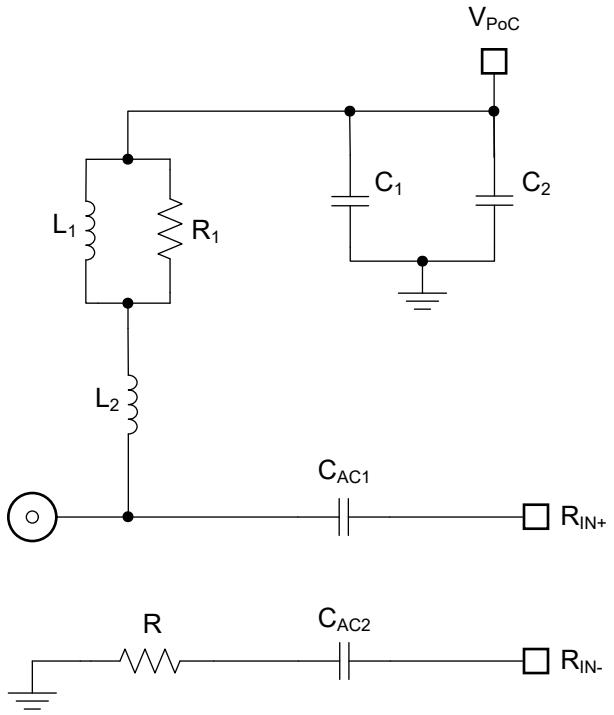


Figure 6-98. Coilcraft PoC Network Number 18 Schematic

Table 6-99. Coilcraft PoC Network 18 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 4.95mm x 3.4mm x 4.1mm	1812POC-682	Coilcraft
L2	Inductor, 0.56uH 2.2mm x 1.45mm x 1.5mm	PFL2015-561	
R1	5.1kΩ		

6.7.19 Design 19

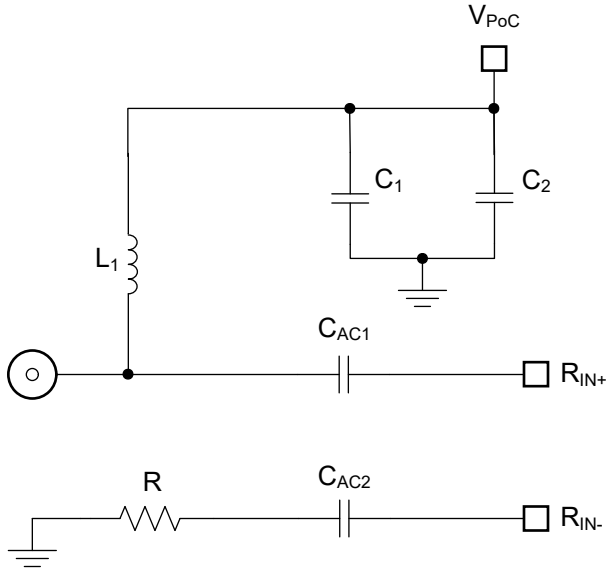


Figure 6-99. Coilcraft PoC Network Number 19 Schematic

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Table 6-100. Coilcraft PoC Network 19 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 3.5mm x 2.26mm x 1.8mm	1210POCM-682	Coilcraft

6.7.20 Design 20

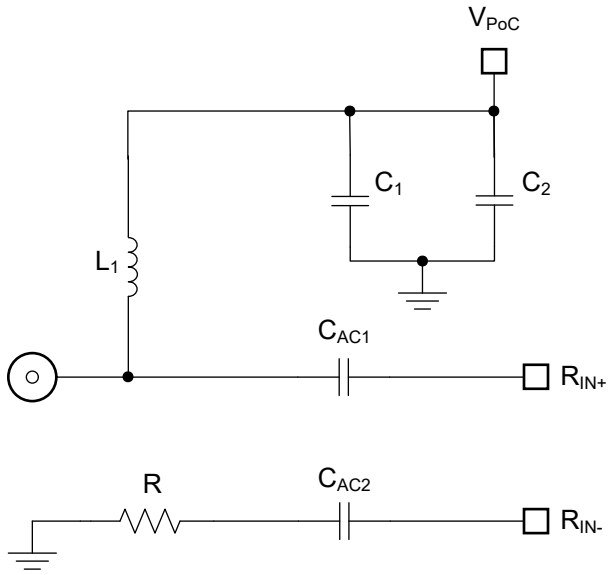


Figure 6-100. Coilcraft PoC Network Number 20 Schematic

Table 6-101. Coilcraft PoC Network 20 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 5.0mm x 3.05mm x 2.44mm	1812POCM-153	Coilcraft

6.7.21 Design 21

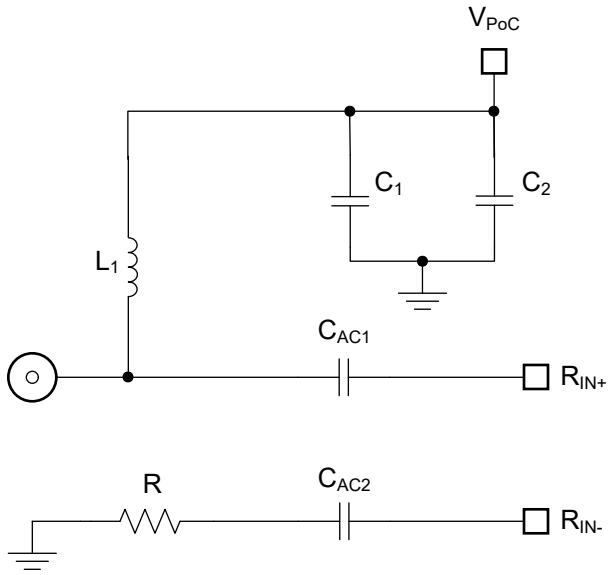


Figure 6-101. Coilcraft PoC Network Number 21 Schematic

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Table 6-102. Coilcraft PoC Network 21 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 6.8uH 5.0mm x 3.05mm x 2.44mm	1812POCM-682	Coilcraft

6.7.22 Design 22

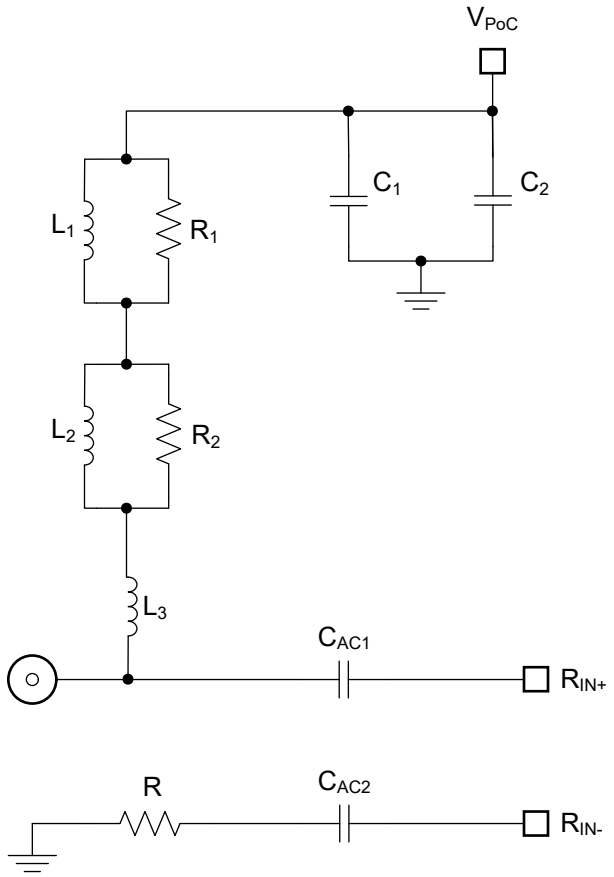


Figure 6-102. Coilcraft PoC Network Number 22 Schematic

Table 6-103. Coilcraft PoC Network 22 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 4.0mm x 4.0mm x 4.1mm	XAL4040-153	Coilcraft
L2	Inductor, 2.2uH 4.95mm x 3.4mm x 4.1mm	1812POC-222	
L3	Inductor, 180nH 2.2mm x 1.45mm x 1.5mm	PFL2015-181	
R1	1kΩ		
R2	5.1kΩ		

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6.7.23 Design 23

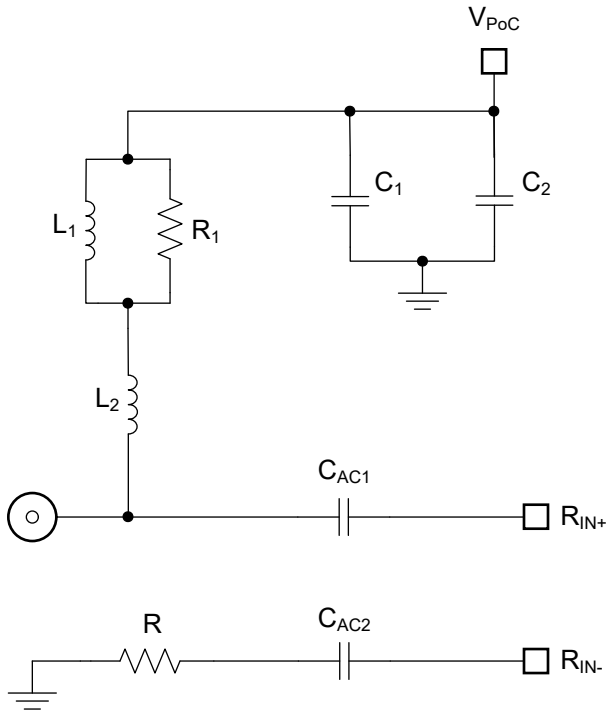


Figure 6-103. Coilcraft PoC Network Number 23 Schematic

Table 6-104. Coilcraft PoC Network 23 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 4.95mm x 3.4mm x 4.1mm	1812POC-153	Coilcraft
L2	Inductor, 0.56uH 2.2mm x 1.45mm x 1.5mm	PFL2015-561	
R1	5.1kΩ		

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6.8 Cyntec FPD4 Networks

6.8.1 Design 1

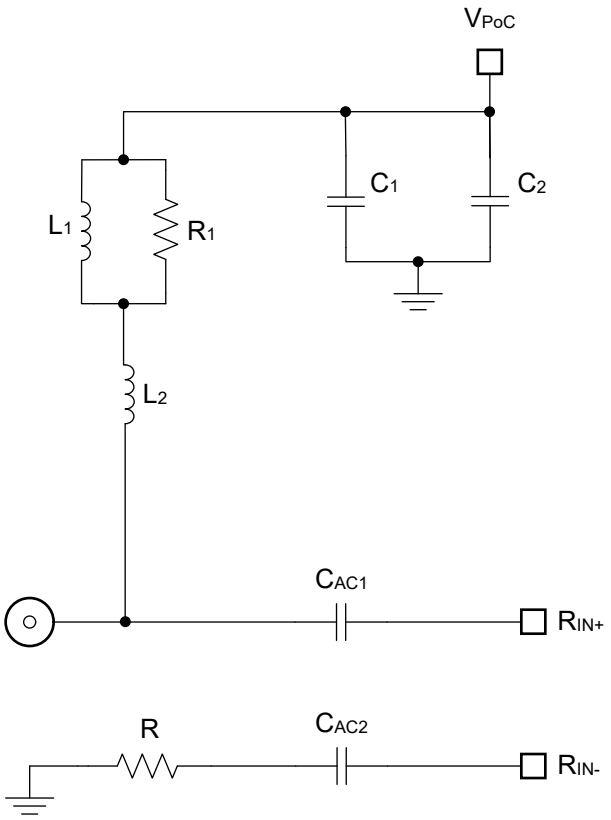


Figure 6-104. Cyntec PoC Network Number 1 Schematic

Table 6-105. Cyntec PoC Network 1 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.0mm x 3.0mm x 1.5mm	VCGA031E-220MS2	Cyntec
L2	Inductor, 1.5uH 2.1mm x 1.25mm x 1.8mm	VCSF20121H-1R5MS2	
R1	1kΩ		

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6.8.2 Design 2

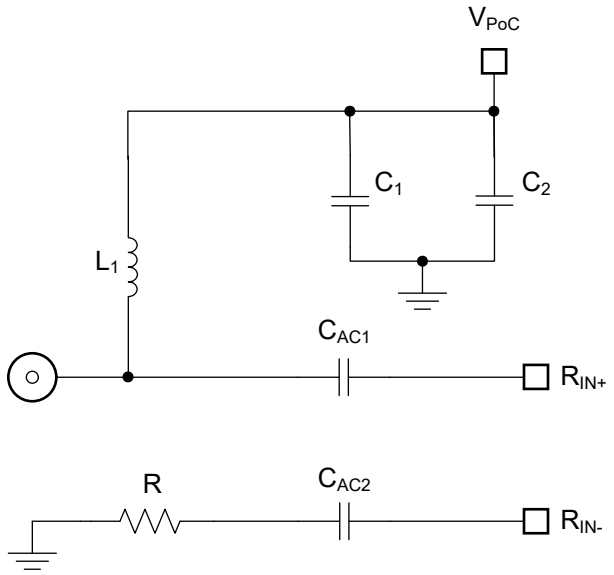


Figure 6-105. Cyntec PoC Network Number 2 Schematic

Table 6-106. Cyntec PoC Network 2 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 4.1mm x 2.7mm x 2.5mm	VCSF32252E-220MS5	Cyntec

6.8.3 Design 3

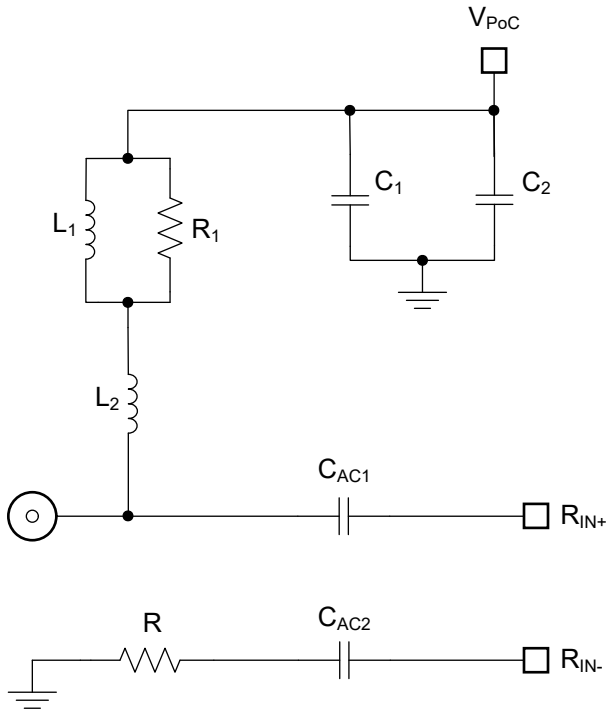


Figure 6-106. Cyntec PoC Network Number 3 Schematic

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Table 6-107. Cyntec PoC Network 3 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 4.1mm x 2.7mm x 2.5mm	VCSF32252E-150MS5	Cyntec
L2	Inductor, 1.5uH 2.1mm x 1.25mm x 1.8mm	VCSF20121H-1R5MS2	
R1	1kΩ		

6.8.4 Design 4

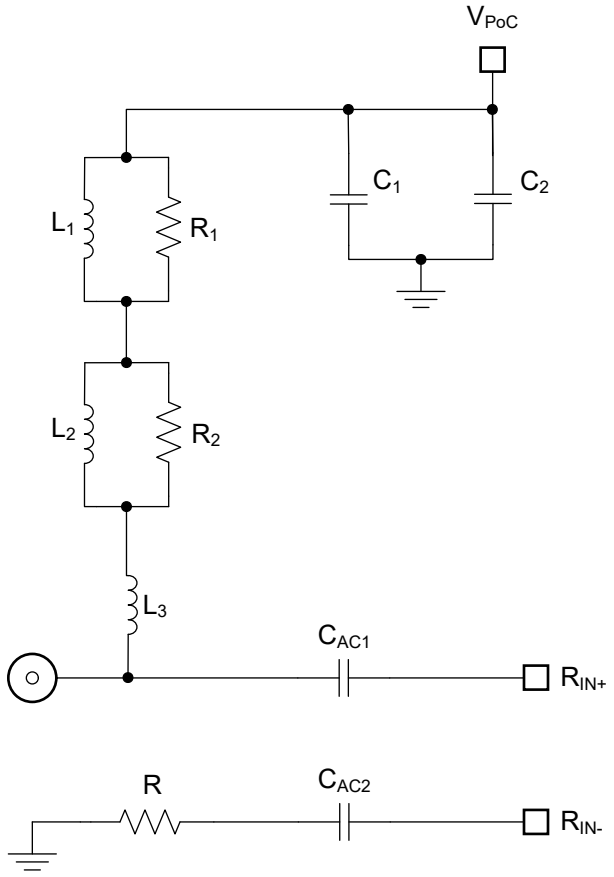


Figure 6-107. Cyntec PoC Network Number 4 Schematic

Table 6-108. Cyntec PoC Network 4 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 68uH 6mm x 6mm x 4.5mm	VCGA064G-680MS5	Cyntec
L2	Inductor, 15uH 4.1mm x 2.6mm x 3.1mm	VCSF32253A-150MS5	
L3	Inductor, 1.5uH 2.1mm x 1.25mm x 1.8mm	VCSF20121H-1R5MS2	
R1	1kΩ		
R2			

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6.8.5 Design 5

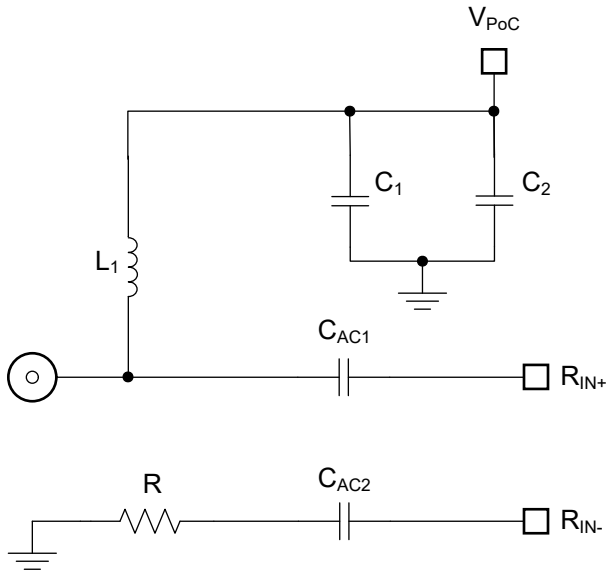


Figure 6-108. Cyntec PoC Network Number 5 Schematic

Table 6-109. Cyntec PoC Network 5 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 4.1mm x 2.6mm x 3.1mm	VCSF32253A-150MS5	Cyntec

6.8.6 Design 6

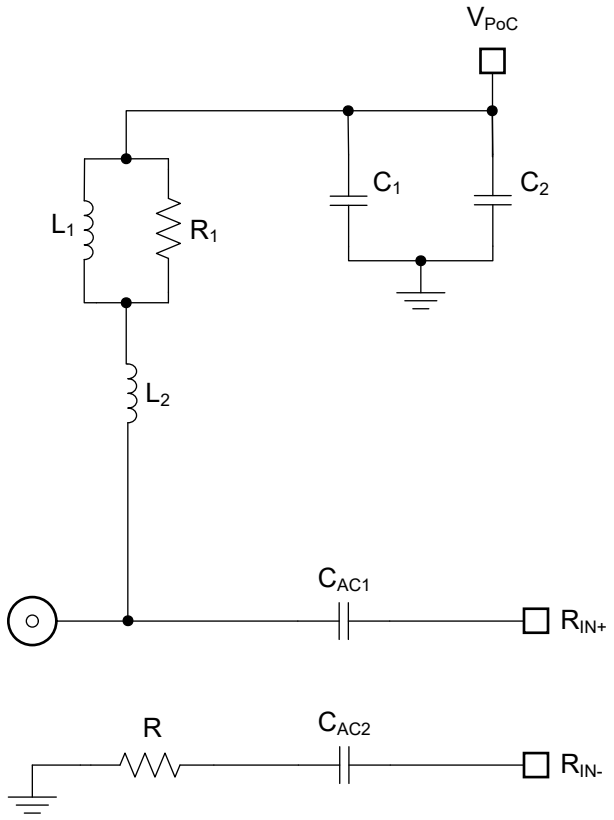


Figure 6-109. Cyntec PoC Network Number 6 Schematic

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Table 6-110. Cyntec PoC Network 6 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 15uH 4.1mm x 2.6mm x 3.1mm	VCSF32253A-150MS5	Cyntec
L2	Inductor, 1.5uH 2.1mm x 1.25mm x 1.8mm	VCSF20121H-1R5MS2	
R1	1kΩ		

6.9 Tai-Tech FPD4 Networks

6.9.1 Design 1

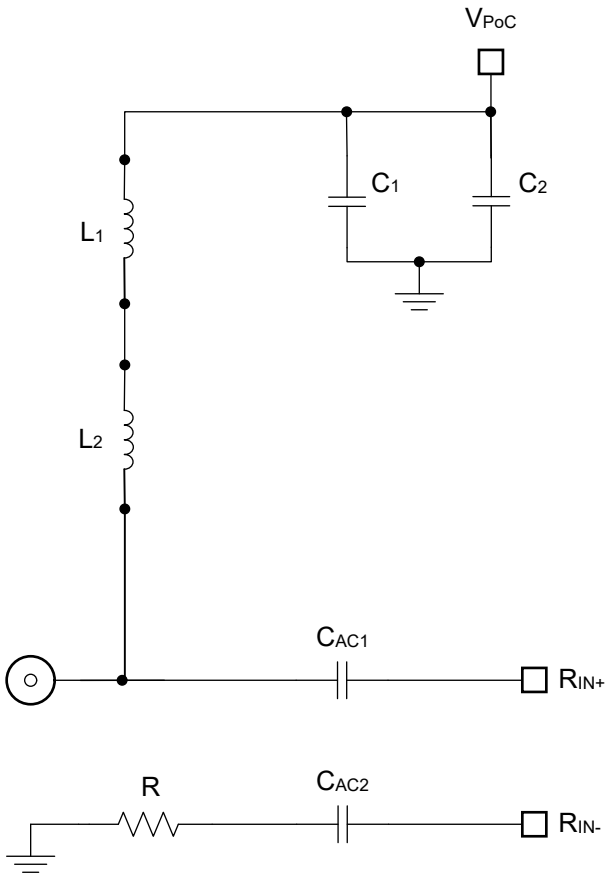


Figure 6-110. Tai-Tech PoC Network Number 1 Schematic

Table 6-111. Tai-Tech PoC Network 1 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3.2mm x 2.5mm x 2.5mm	APO322523NV-470M	Tai-Tech
L2	Inductor, 650nH 1.6mm x 1.0mm x 1.1mm	SWF1608RIV-R65K	

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6.9.2 Design 2

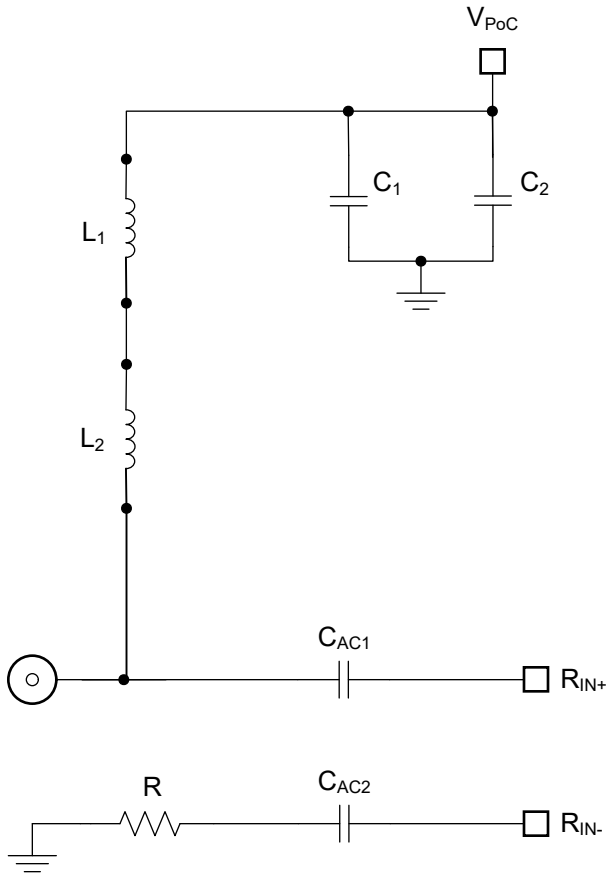


Figure 6-111. Tai-Tech PoC Network Number 2 Schematic

Table 6-112. Tai-Tech PoC Network 2 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 47uH 3mm x 3mm x 1.3mm	HPC3015BMV-470M	Tai-Tech
L2	Inductor, 2.2uH 2mm x 1.2mm x 1.6mm	APO201216NV-2R2M	

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6.9.3 Design 3

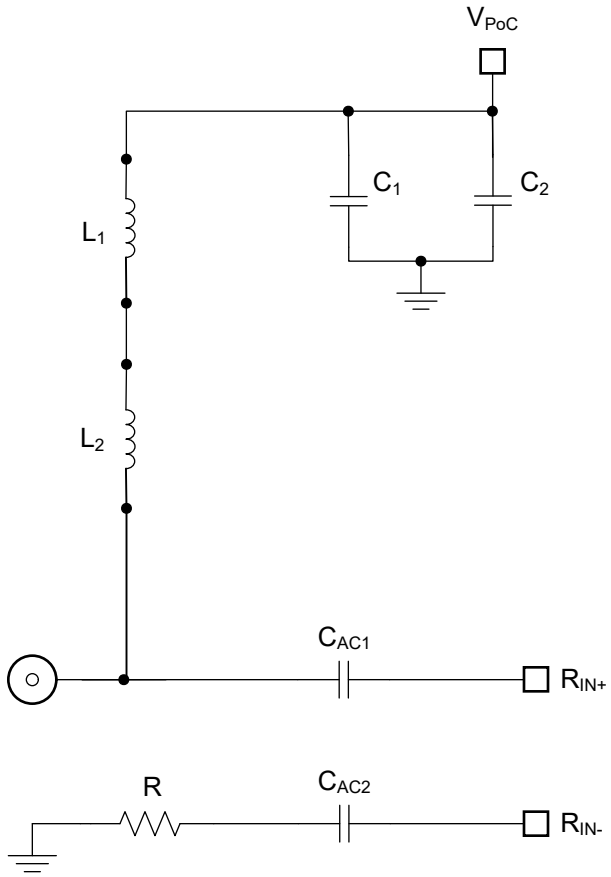


Figure 6-112. Tai-Tech PoC Network Number 3 Schematic

Table 6-113. Tai-Tech PoC Network 3 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 22uH 3.2mm x 2.5mm x 2.3mm	APO322523NV-220M	Tai-Tech
L2	Inductor, 1.5uH 2mm x 1.2mm x 1.6mm	APO201216NV-1R5M	

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6.9.4 Design 4

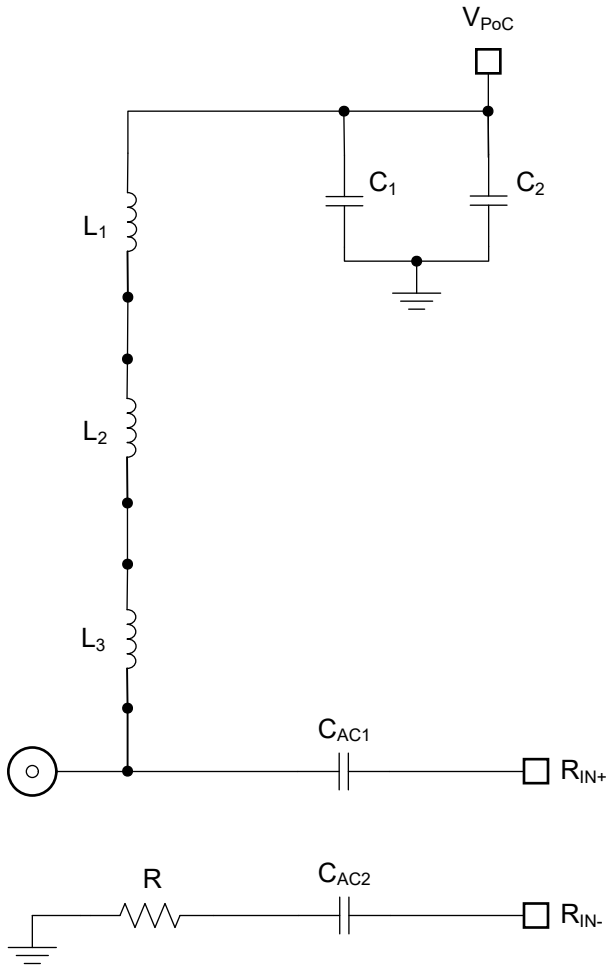


Figure 6-113. Tai-Tech PoC Network Number 4 Schematic

Table 6-114. Tai-Tech PoC Network 4 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm x 3mm x 1.3mm	HPC3015BMV-100M	Tai-Tech
L2	Inductor, 3.3uH 3.2mm x 2.5mm x 2.3mm	APO322523NV-3R3M	
L3	Inductor, 0.82uH 2mm x 1.2mm x 1.6mm	APO201216NV-R82M	

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6.9.5 Design 5

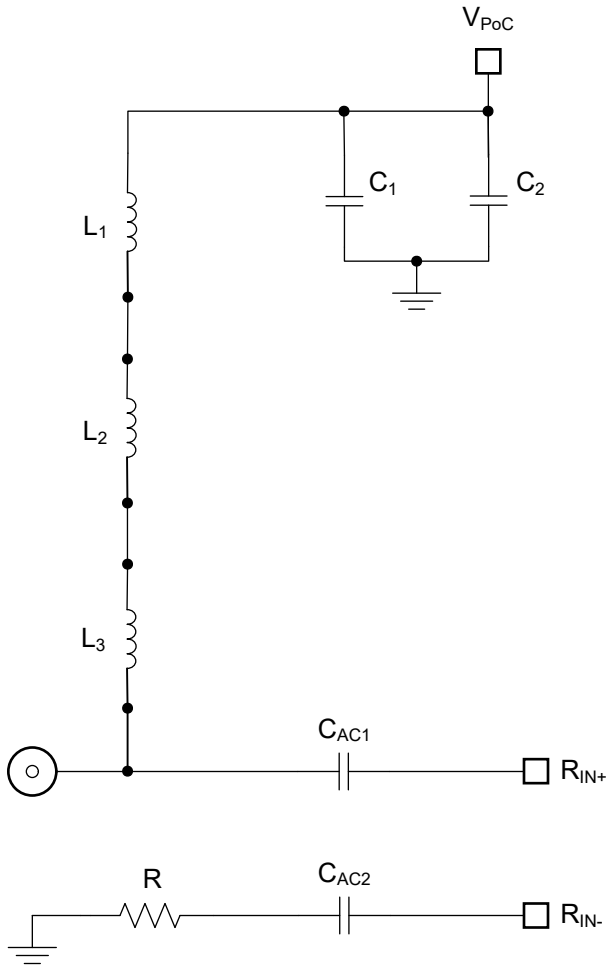


Figure 6-114. Tai-Tech PoC Network Number 5 Schematic

Table 6-115. Tai-Tech PoC Network 5 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 3mm x 3mm x 1.3mm	HPC3015BMV-100M	Tai-Tech
L2	Inductor, 4.7uH 3.2mm x 2.5mm x 2.3mm	APO322523TV-4R7M	
L3	Inductor, 0.82uH 3.2mm x 2.5mm x 2.3mm	APO322523NV-R82M	

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6.9.6 Design 6

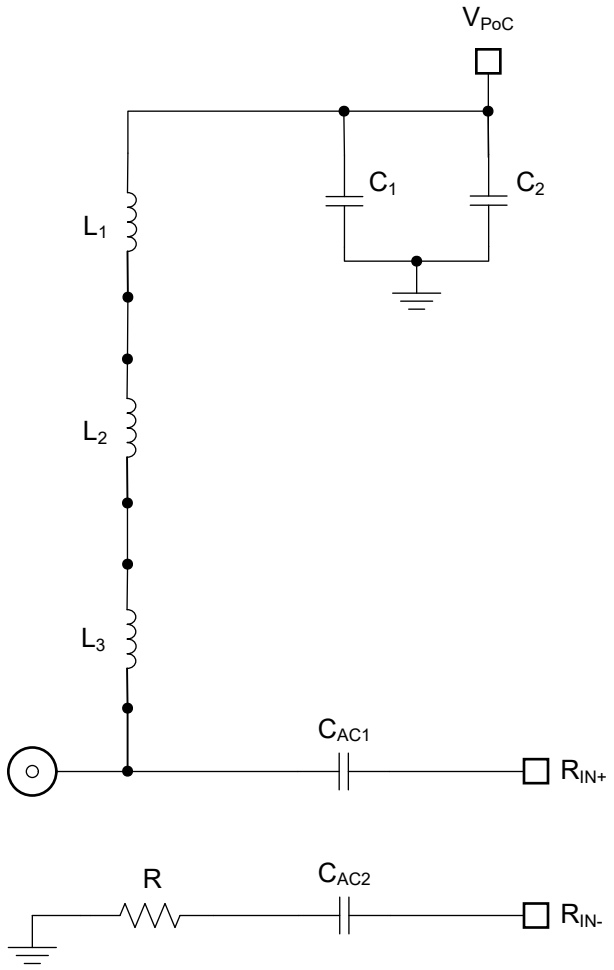


Figure 6-115. Tai-Tech PoC Network Number 6 Schematic

Table 6-116. Tai-Tech PoC Network 6 Components

Designator	Description	Part Number	Vendor
L1	Inductor, 10uH 4mm x 4mm x 1.6mm	HPC4018BMV-100M	Tai-Tech
L2	Inductor, 4.7uH 3.2mm x 2.5mm x 2.3mm	APO322523TV-4R7M	
L3	Inductor, 0.82uH 3.2mm x 2.5mm x 2.3mm	APO322523NV-R82M	

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7 Summary

PoC networks can be utilized in ADAS systems to send power from the deserializer board to the serializer board and camera, eliminating the need for a separate power cable. Although PoC networks simplify the overall system architecture, careful consideration must be given to the selected components and network design. Systems that implement a PoC network must be validated to meet TI's channel specifications and noise requirements. Additionally, the PoC network must be designed to properly filter the system's entire FPD-Link operating frequency range, while fulfilling all power consumption requirements of the system and temperature ratings of the individual components. These factors must be considered when selecting a PoC network to implement in an FPD-Link system to provide reliable communication across all operating conditions.

8 References

- Texas Instruments, *DS90UB9702-Q1 Automotive FPD-Link IV Deserializer Hub With D-PHY CSI-2 Output Ports for 8MP+ Cameras & Other Sensors*, data sheet.
- Texas Instruments, *DS90UB960-Q1 Quad 4.16Gbps FPD-Link III Deserializer Hub With Dual MIPI CSI-2 Ports*, data sheet.
- Texas Instruments, DS90UB934-Q1 12 Bit,100-MHz FPD-Link III Deserializer for 1MP/60fps and 2MP/30fps Cameras, data sheet.
- Texas Instruments, *FPD-Link Learning Center*, video series.
- Texas Instruments, Automotive 1-MP Camera Module Reference Design With YUV422, FPD-Link III, and 4-V to 36-V Power Over Coax, design guide
- Texas Instruments, Automotive 2-MP Camera Module Reference Design With MIPI CSI-2 Video Interface, FPD-Link III and POC, design guide
- Texas Instruments, Automotive 2.6-MP Camera Module Reference Design With POL PMIC, FPD-Link III, Supervisor, and POC, design guide.
- Texas Instruments, Automotive 8.3-MP POC Camera Module Reference Design with PMIC and FPD-Link III, design guide.

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9 Revision History

Changes from Revision B (October 2025) to Revision C (April 2026) **Page**

- Added FPD4 Cyntec PoC Networks....21
- Added FPD4 Tai-Tech PoC Networks....21
- Added FPD3 TDK Design 9/10 and FPD4 TDK Design 24/25....21
- Added FPD4 Coilcraft PoC Network Designs 16 - 23....21
- Added height of each component in the PoC networks....21
- Added reference link to the DS90UB9702-Q1 one-page datasheet....132

Changes from Revision A (January 2024) to Revision B (October 2025) **Page**

- Updated document title and Abstract description to clarify that this document contains PoC networks for all ADAS FPD-Link devices....1
- Added names of contributors....1
- Updated document to reflect latest PoC recommendations and requirements for all FPD-Link III devices....8
- Clarified that 1kΩ impedance through the PoC network is recommended, but not required....8
- Added *capacitor characteristics* section....11
- Updated Frequency Range section based on FPD4 examples....13
- Updated language to reflect how TI reviews PoC networks....13
- Added new section describing factors that affect resistance in a PoC network design that can have significant impact on IR loss in high power applications....13
- Added more details on the derating characteristics of capacitors at DC bias voltage....20
- Updated the current and temperature ratings of PoC networks, based on new test data....21
- Updated the current and temperature ratings of PoC networks, based on new test data....21
- Added new Murata PoC networks for the FPD-Link IV generation of devices....21
- Updated the FPD-Link III table to show PoC networks that pass loss limit lines within the FPD-Link III generation....21
- Removed TDK Design 6, since the network was similar to Design 5. Numbering of TDK PoC designs was updated accordingly....21
- Added new TDK PoC networks for the FPD-Link IV generation of devices....21
- Added new Coilcraft PoC networks for the FPD-Link IV generation of devices....21
- Changed "Approved" to "Reviewed"....21
- Added tables that show which PoC designs can pass the PCB Budget loss limit lines defined in the FPD3 Channel Specifications document....21
- Included the size of each inductor in the Descriptions column of each PoC network....21
- Updated resistor values for TDK#2 for optimized loss performance on the link....80
- Updated resistor values for TDK#4 for optimized loss performance on the link....82
- Changed this network to TDK Design 6....84
- Changed this network to TDK Design 7....85
- Updated components for Coilcraft Design 3 for optimized performance....103
- Updated components for Coilcraft Design 4 for optimized performance....104

Changes from Revision * (June 2014) to Revision A (January 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added *ferrite bead characteristics* section....12
- Added *layout considerations* section....14
- Added *channel requirements* section....16
- Added *noise requirements* section....18
- Added additional recommended PoC network example schematics....21

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