

LM27761 Low-Noise, Regulated, Switched-Capacitor Voltage Inverter

1 Features

- Inverts and regulates the input supply voltage
- Low output ripple
- Shutdown lowers quiescent current to 7µA (typical)
- Up to 250mA output current
- 2.5Ω inverter output impedance, $V_{IN} = 5V$
- ±4% regulation at peak load
- 370µA quiescent current
- 2MHz (typical) low-noise fixed-frequency operation
- 35dB (typical) LDO PSRR at 2MHz with 80mA load current
- 30mV LDO dropout voltage at 100mA, $V_{OUT} = -5V$
- Current limit and thermal protection

2 Applications

- Operational amplifier power
- Wireless communication systems
- Cellular-phone power-amplifier biasing
- Interface power supplies
- Handheld instrumentation
- Hi-Fi headphone amplifiers
- Powering data converters

3 Description

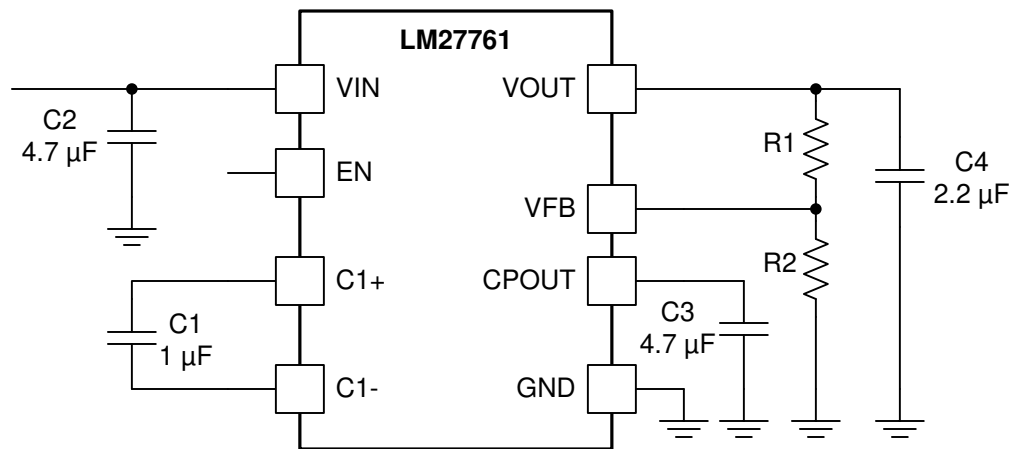
The LM27761 low-noise regulated switched-capacitor voltage inverter delivers a very low-noise adjustable output for an input voltage in the range of 2.7V to 5.5V. Four low-cost capacitors are used in the application design to provide up to 250mA of output current. The regulated output for the device is adjustable between -1.5V and -5V. The LM27761 operates at 2MHz (typical) switching frequency to reduce output resistance and voltage ripple. With an operating current of only 370µA (charge-pump power efficiency greater than 80% with most loads) and 7µA typical shutdown current, the LM27761 provides excellent performance when driving power amplifiers, DAC bias rails, and other high-current, low-noise voltage applications.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LM27761	DSG (WSON, 8)	2.00mm × 2.00mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application



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4 Pin Configuration and Functions

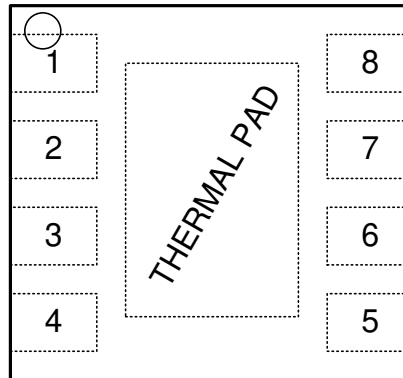


Figure 4-1. DSG Package 8-Pin WSON With Thermal Pad Top View

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NUMBER	NAME		
1	VIN	P	Positive power supply input.
2	GND	G	Ground
3	CPOUT	P	Negative unregulated output voltage.
4	VOUT	P	Regulated negative output voltage.
5	VFB	P	Feedback input. Connect VFB to an external resistor divider between VOUT and GND. <i>DO NOT</i> leave unconnected.
6	EN	I	Active high enable input.
7	C1–	P	Negative terminal for C1.
8	C1+	P	Positive terminal for C1.
—	Thermal Pad	G	Ground. <i>DO NOT</i> leave unconnected.

(1) P: Power; G: Ground; I: Input.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

	MIN	MAX	UNIT
Ground voltage, VIN to GND or GND to VOUT		5.8	V
EN	(GND – 0.3 V)	(VIN + 0.3 V)	
Continuous output current, CPOUT and VOUT		300	mA
T _{JMAX} ⁽³⁾		150	°C
Storage temperature, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military, Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
- (3) The maximum power dissipation must be derated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), T_A (ambient temperature) and R_{θJA} (junction-to-ambient thermal resistance). The maximum power dissipation at any temperature is: P_{DissMAX} = (T_{JMAX} – T_A)/R_{θJA} up to the value listed in the *Absolute Maximum Ratings*.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature, T _A	–40	85	°C
Operating junction temperature, T _J	–40	125	°C
Operating input voltage, V _{IN}	2.7	5.5	V
Operating output current, I _{OUT}	0	250	mA

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM27761	UNIT
		WSON (DSG)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	67.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	89.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	2.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	38	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	9.4	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) application note.

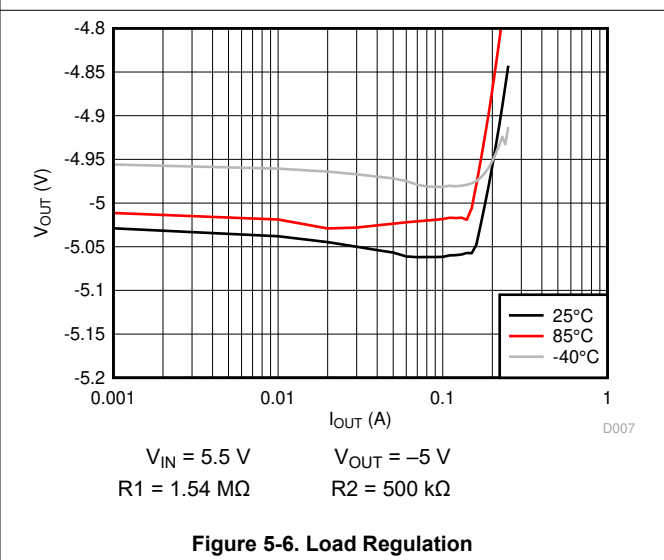
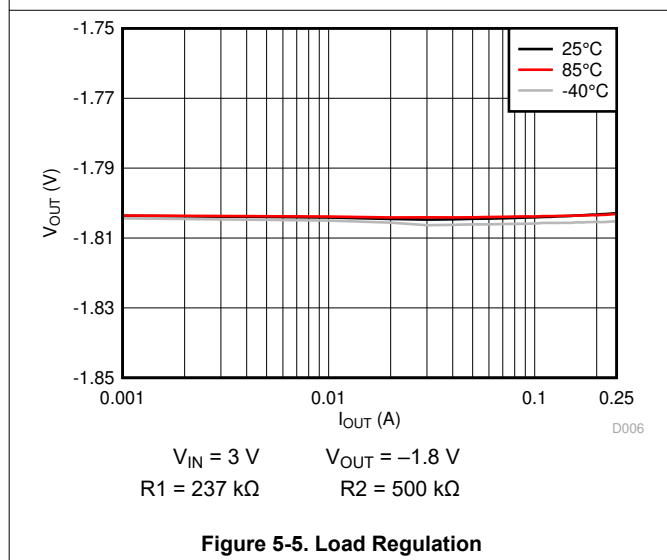
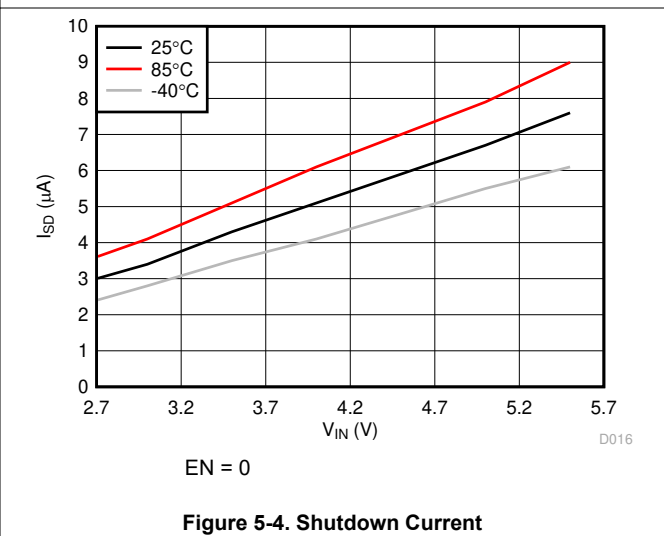
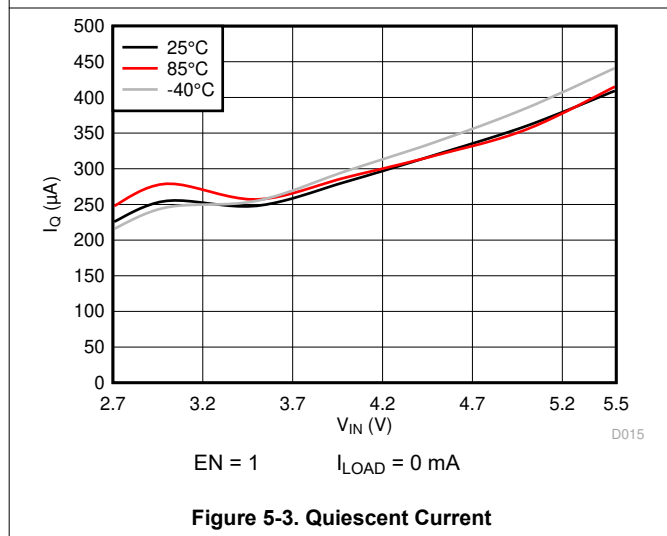
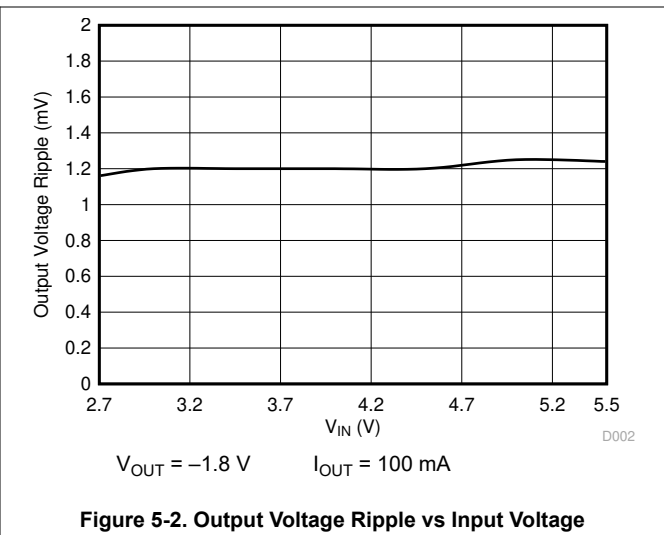
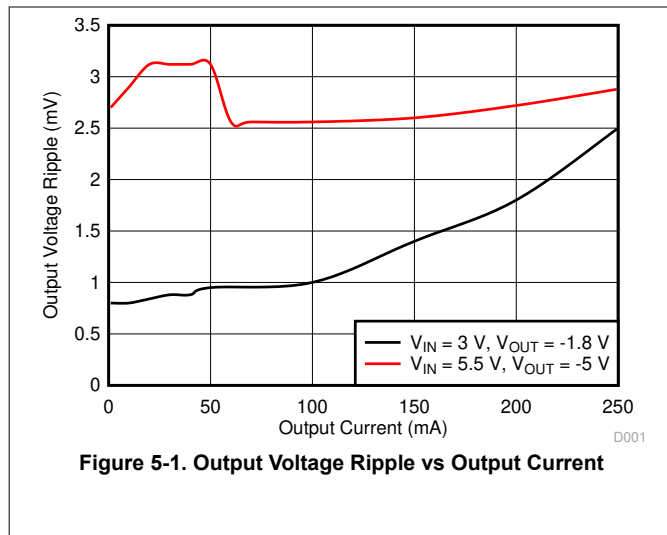
5.5 Electrical Characteristics

Typical limits apply for $T_A = 25^\circ\text{C}$, and minimum and maximum limits apply over the full temperature range. Unless otherwise specified, $V_{IN} = 5\text{ V}$ and values for C1 to C4 are as shown in the [Typical Application](#).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_q	Supply current	Open circuit, no load		370	600	μA
I_{SD}	Shutdown supply current			7	12	μA
f_{SW}	Switching frequency	$V_{IN} = 3.6\text{ V}$	1.7	2	2.3	MHz
R_{NEG}	Output resistance to C_{POUT}	$V_{IN} = 5.5\text{ V}$		2		Ω
V_{DO}	LDO dropout voltage	$I_{LOAD} = 100\text{ mA}$, $V_{OUT} = -5\text{ V}$		30		mV
PSRR	Power supply rejection ratio	$I_{LOAD} = 80\text{ mA}$, $V_{CPOUT} = -5\text{ V}$		35		dB
V_N	Output noise voltage	$I_{LOAD} = 80\text{ mA}$, 10 Hz to 100 kHz		20		μV_{RMS}
V_{FB}	Feedback pin reference voltage		1.202	1.22	1.238	V
V_{OUT}	Adjustable output voltage	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$	-5		-1.5	V
	Load regulation	0 to 250 mA, $V_{OUT} = -1.8\text{ V}$		4.6		$\mu\text{V}/\text{mA}$
	Line regulation	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$, $I_{LOAD} = 50\text{ mA}$		1.5		mV/V
V_{IH}	Enable pin input voltage high	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$	1.2			V
V_{IL}	Enable pin input voltage low	$5.5\text{ V} \geq V_{IN} \geq 2.7\text{ V}$			0.4	V
UVLO	Undervoltage lockout	V_{IN} falling		2.6		V
		V_{IN} rising		2.4		

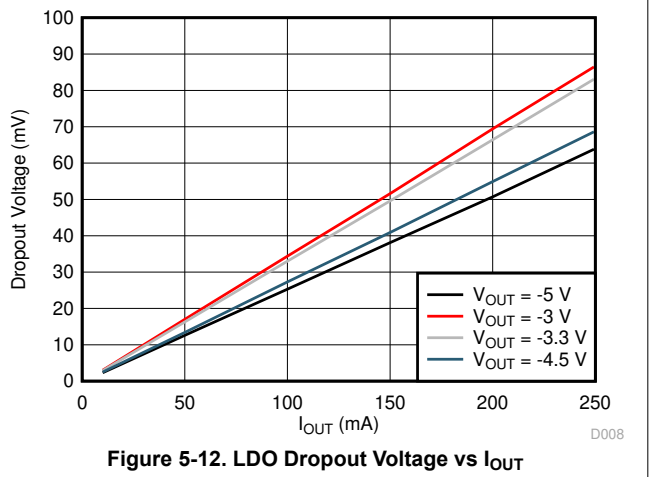
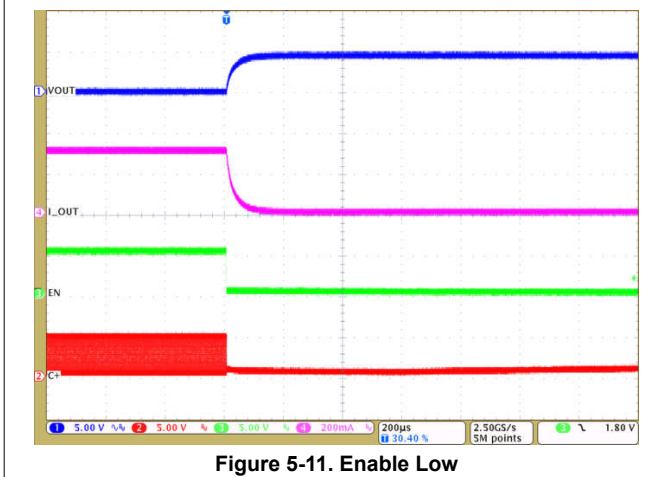
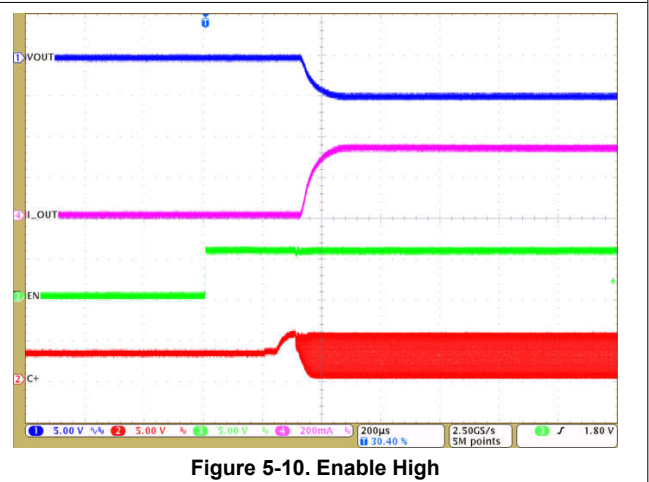
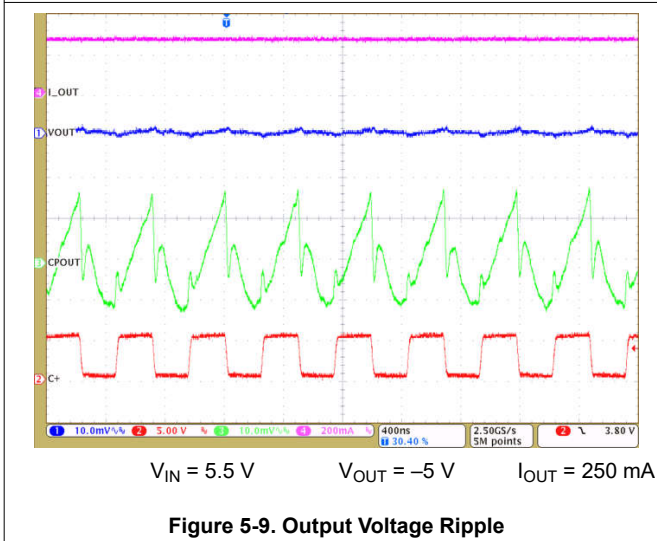
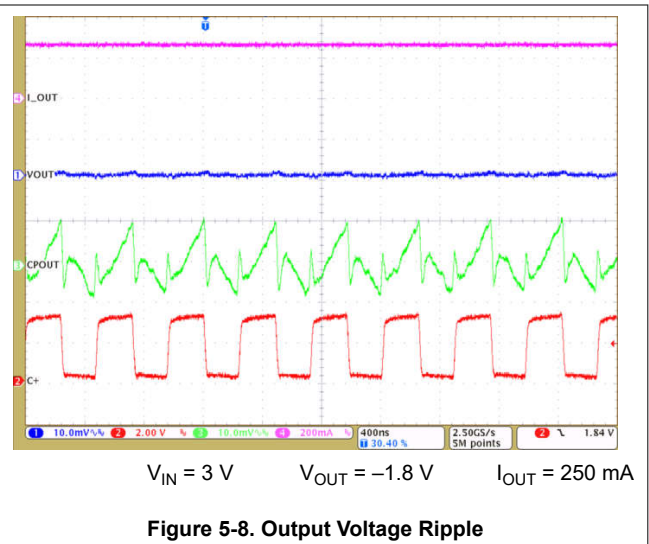
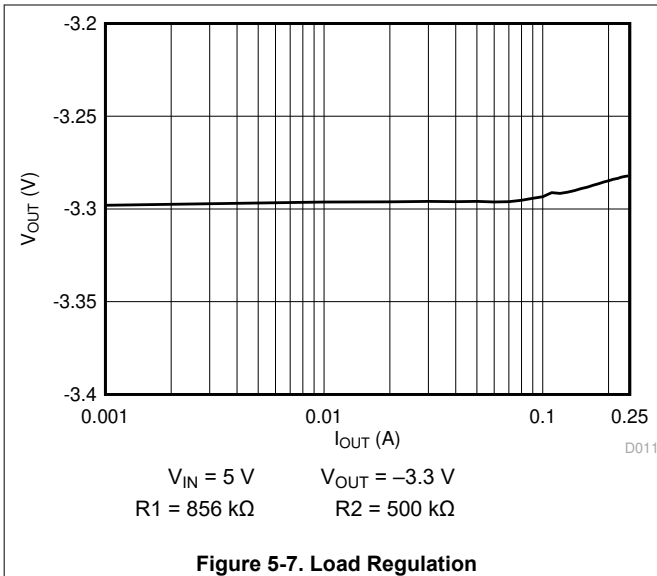
5.6 Typical Characteristics

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$, and values for C1 to C4 are as shown in the [Typical Application](#).



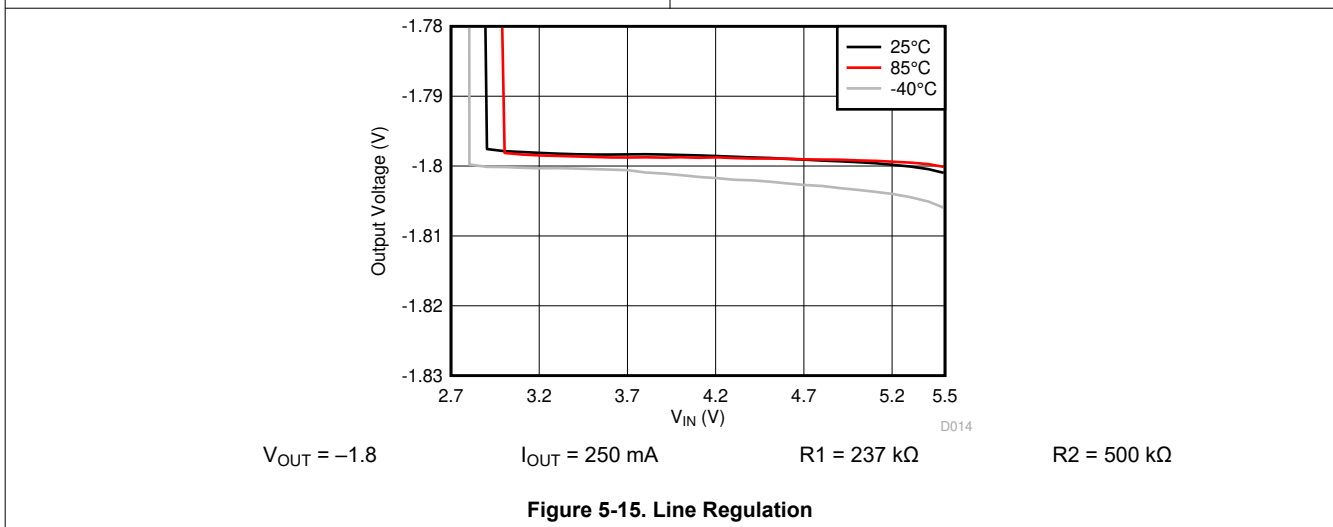
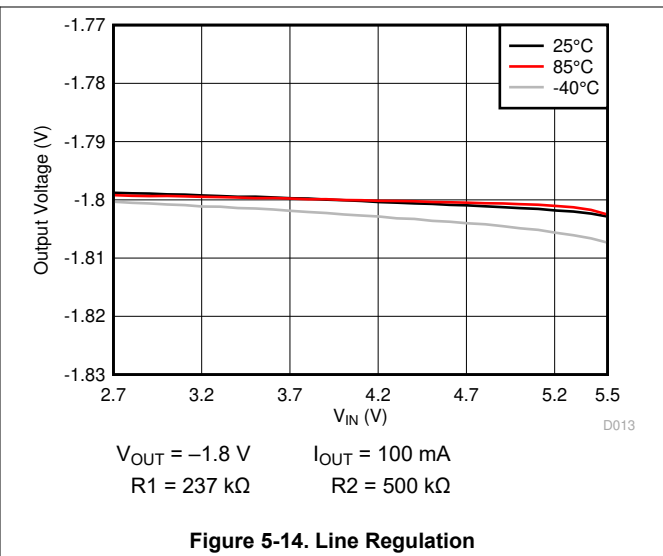
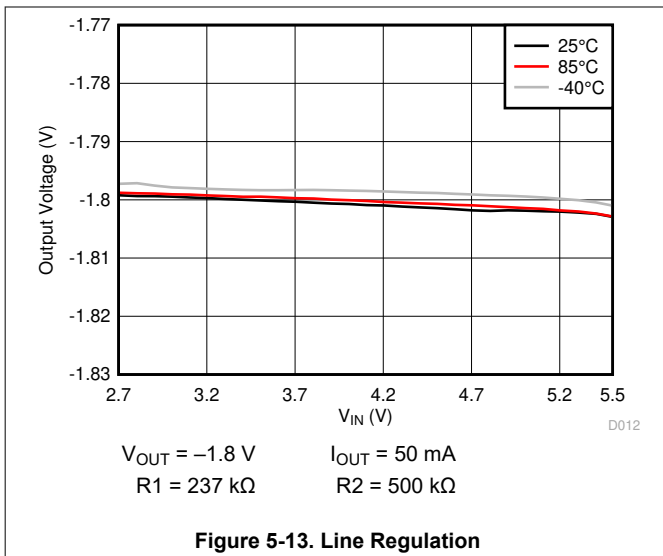
5.6 Typical Characteristics (continued)

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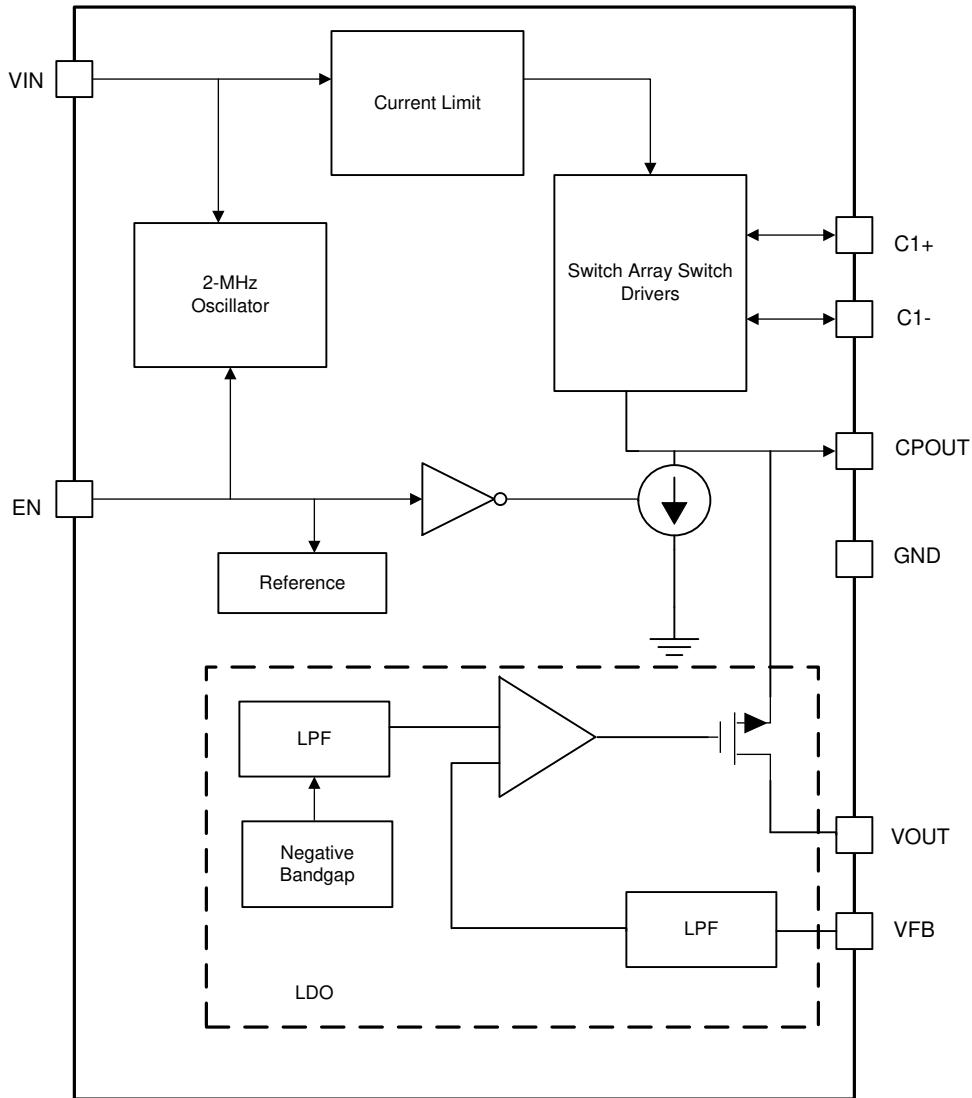


6 Detailed Description

6.1 Overview

The LM27761 regulated charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to a negative voltage in the range of -1.5 V to -5 V. The negative LDO (low drop-out regulator), at the output of the charge-pump voltage converter, allows the device to provide a very low noise output, low output-voltage ripple, high PSRR, and low line and load transient responses. The output is externally configurable with gain-setting resistors. The LM27761 uses four low-cost capacitors to deliver up to 250 mA of output current.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Undervoltage Lockout

The LM27761 has an internal comparator that monitors the voltage at V_{IN} and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM27761 resumes normal operation.

6.3.2 Input Current Limit

The LM27761 contains current limit circuitry that protects the device in the event of excessive input current and output shorts to ground. The input current is limited to 500 mA (typical) when the output is shorted directly to ground. When the LM27761 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

6.3.3 PFM Operation

To minimize quiescent current during light load operation, the LM27761 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is low, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-2-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency in the LM27761 is 2 MHz.

6.3.4 Output Discharge

In shutdown, the LM27761 actively pulls down on the output of the device until the output voltage reaches GND. In this mode, the current drawn from the output is approximately 1.85 mA.

6.3.5 Thermal Shutdown

The LM27761 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the device switches into shutdown mode. The LM27761 releases thermal shutdown when the junction temperature is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and insufficient thermal dissipation. The LM27761 device power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped by reducing the internal power dissipation (reduce input voltage and output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the device.

6.4 Device Functional Modes

6.4.1 Shutdown Mode

An enable pin (EN) pin is available to disable the device and place the LM27761 into shutdown mode reducing the quiescent current to 7 μ A. In shutdown, the output of the LM27761 is pulled to ground by an internal pullup current source (approximately 1.85 mA).

6.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN pin brings the device into enable mode. When unloaded, the input current during operation is 370 μ A. As the load current increases, so does the quiescent current. When enabled, the output voltage is equal to the inverse of the input voltage minus the voltage drop across the charge pump.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM27761 low-noise charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to a negative output voltage configurable with external gain setting resistors. The device uses four low-cost capacitors to provide up to 250 mA of output current. The LM27761 operates at a 2-MHz oscillator frequency to reduce charge-pump output resistance and voltage ripple under heavy loads. With an operating current of only 370 μ A and 7- μ A typical shutdown current, the LM27761 provides ideal performance for battery-powered systems.

7.2 Typical Application - Regulated Voltage Inverter

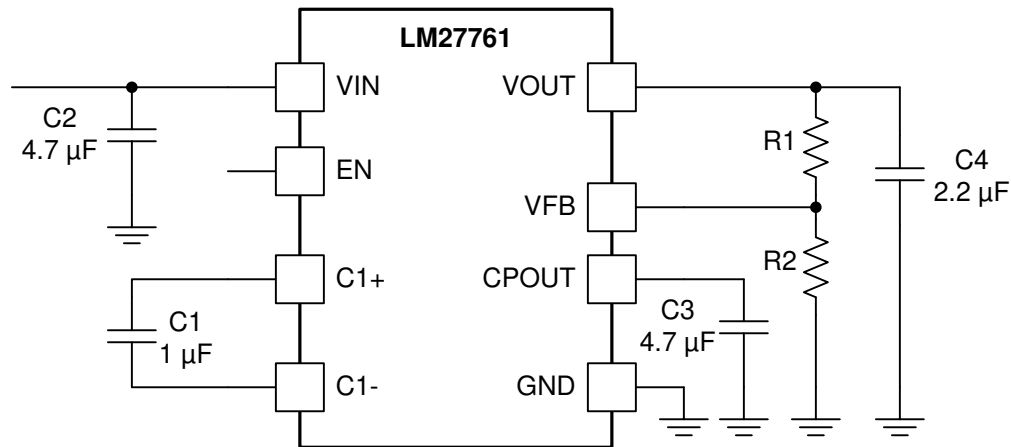


Figure 7-1. LM27761 Typical Application

7.2.1 Design Requirements

Example requirements for typical applications using the LM27761 device are listed in [Table 7-1](#):

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	-1.5 V to -5 V
Output current	0 mA to 250 mA
Boost switching frequency	2 MHz

7.2.2 Detailed Design Procedure

7.2.2.1 Charge-Pump Voltage Inverter

The main application of the LM27761 is to generate a regulated negative supply voltage. The voltage inverter circuit uses only three external capacitors, and the LDO regulator circuit uses one additional output capacitor.

The voltage inverter portion of the LM27761 contains four large CMOS switches which are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 7-2 shows the voltage switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, and C1 is charging C3. After a number of cycles, the voltage across C3 is pumped into V_{IN} . Because the anode of C3 is connected to ground, the output at the cathode of C3 equals $-(V_{IN})$ when there is no load current. When a load is added the output voltage drop is determined by the parasitic resistance ($R_{DS(ON)}$ of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between the capacitors.

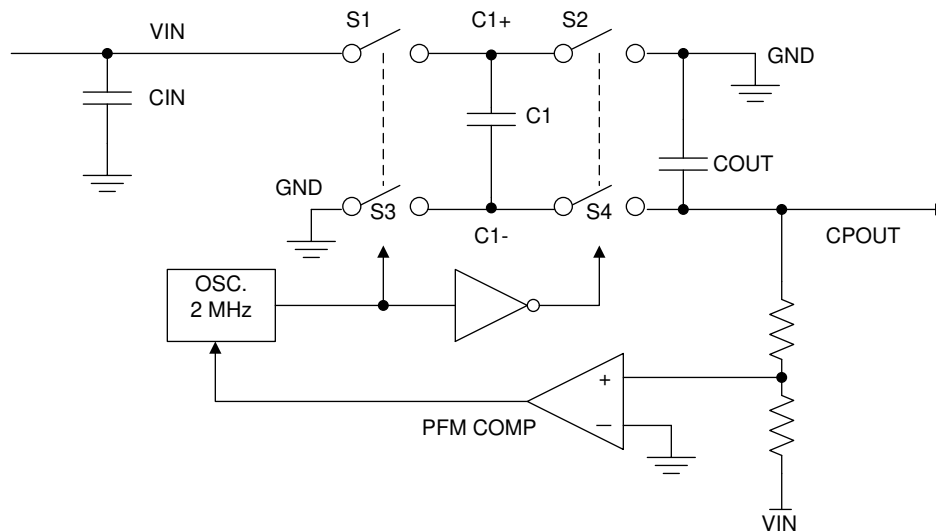


Figure 7-2. Voltage Inverting Principle

The output characteristic of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals $-(V_{IN})$. The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance, and the ESR of C1 and C3. Because the switching current charging and discharging C1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C1 is multiplied by four in the output resistance. The charge-pump output capacitor C3 is charging and discharging at a current approximately equal to the output current; therefore, the ESR only counts once in the output resistance. A good approximation of charge-pump R_{OUT} is shown in Equation 1:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C)] + (4 \times ESR_{C1}) + ESR_{COUT} \quad (1)$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 7-2.

High capacitance and low-ESR ceramic capacitors reduce the output resistance.

7.2.2.2 Negative Low-Dropout Linear Regulator

At the output of the inverting charge-pump the LM27761 features a low-dropout, linear negative voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This negative LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

7.2.2.3 Power Dissipation

The allowed power dissipation for any package is a measure of the ability of the device to pass heat from the junctions of the device to the heatsink and the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation can be calculated by [Equation 2](#):

$$P_{D-MAX} = (T_{J-MAX} - T_A) / R_{\theta JA} \quad (2)$$

The actual power being dissipated in the device can be represented by [Equation 3](#):

$$P_D = P_{IN} - P_{OUT} = [V_{IN} \times (-I_{OUT} + I_Q) - (V_{OUT} \times I_{OUT})] \quad (3)$$

[Equation 2](#) and [Equation 3](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These equations must be used to determine the optimum operating conditions for the device in a given application.

In lower power dissipation applications the maximum ambient temperature (T_{A-MAX}) can be increased. In higher power dissipation applications the maximum ambient temperature (T_{A-MAX}) can have to be derated. T_{A-MAX} can be calculated using [Equation 4](#):

$$T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX}) \quad (4)$$

where

- $T_{J-MAX-OP}$ = maximum operating junction temperature (125°C)
- P_{D-MAX} = the maximum allowable power dissipation
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the package

Alternately, if T_{A-MAX} cannot be derated, the power dissipation value must be reduced. This can be accomplished by reducing the input voltage as long as the minimum V_{IN} is not violated, or by reducing the output current, or some combination of the two.

7.2.2.4 Output Voltage Setting

The output voltage of the LM27761 is externally configurable. The value of R1 and R2 determines the output voltage setting. The output voltage can be calculated using [Equation 5](#):

$$V_{OUT} = -1.22 \text{ V} \times (R1 + R2) / R2 \quad (5)$$

The value for R2 must be no less than 50 kΩ.

7.2.2.5 External Capacitor Selection

The LM27761 requires 4 external capacitors for proper operation. TI recommends surface-mount multi-layer ceramic capacitors. These capacitors are small, inexpensive, and have very low ESR ($\leq 15\text{-m}\Omega$ typical). TI does not recommend Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally for use with the LM27761 due to the high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferable for use with the LM27761. These capacitors have tight capacitance tolerances (as good as $\pm 10\%$) and hold the value over temperature (X7R: $\pm 15\%$ over -55°C to $+125^\circ\text{C}$; X5R $\pm 15\%$ over -55°C to $+85^\circ\text{C}$).

TI does not recommend sing capacitors with a Y5V or Z5U temperature characteristic for the LM27761. These capacitors typically have wide capacitance tolerance (80%, ...20%) and vary significantly over temperature (Y5V: 22%, -82% over -30°C to $+85^\circ\text{C}$ range; Z5U: 22%, -56% over 10°C to 85°C range). Under some conditions a 1- μF -rated Y5V or Z5U capacitor can have a capacitance as low as 0.1 μF . Such detrimental

deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27761.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower-than-expected capacitance on the input and output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. TI strongly recommends that the LM27761 circuit be evaluated thoroughly early in the design-in process with the mass-production capacitor of choice. This action helps make sure that any such variability in capacitance does not negatively impact circuit performance.

7.2.2.5.1 Charge-Pump Output Capacitor

In typical applications, TI recommends a 4.7- μ F low-ESR ceramic charge-pump output capacitor (C3). Different output capacitance values can be used to reduce charge pump ripple, shrink the design size, and cut the cost of the solution. However, changing the output capacitor can also require changing the flying capacitor or input capacitor to maintain good overall circuit performance.

In higher-current applications, TI recommends a 10- μ F, 10-V low-ESR ceramic output capacitor. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, TI recommends a 2- μ F capacitance. For example, 10- μ F, 10-V output capacitor in a 0402 case size typically has only 2- μ F capacitance when biased to 5 V.

7.2.2.5.2 Input Capacitor

The input capacitor (C2) is a reservoir of charge that aids in a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. The input capacitor also filters noise on the input pin, keeping this noise out of the sensitive internal analog circuitry that is biased off the input line.

Input capacitance has a dominant and first-order effect on the input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, TI recommends a 4.7- μ F low-ESR ceramic capacitor on the input. When operating near the maximum load of 250 mA, after taking into account the DC bias derating, a minimum recommended input capacitance is 2 μ F or larger. Different input capacitance values can be used to reduce ripple, shrink the design size, and cut the cost of the design.

7.2.2.5.3 Flying Capacitor

The flying capacitor (C1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM27761 can not be able to regulate the output voltage when load currents are high. If the flying capacitance is too large, the flying capacitor can overwhelm the input and charge pump output capacitors, resulting in increased input and output ripple.

In typical high-current applications, TI recommends 0.47- μ F or 1- μ F 10-V low-ESR ceramic capacitors for the flying capacitors. Polarized capacitors (tantalum, aluminum, electrolytic, and so forth.) must not be used for the flying capacitor, as polarized capacitors can become reverse-biased during LM27761 operation.

7.2.2.5.4 LDO Output Capacitor

The LDO output capacitor (C4) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27761 only requires the use of a 2.2- μ F ceramic output capacitor for stable operation. For typical applications, a 2.2- μ F ceramic output capacitor located close to the output is sufficient.

7.2.3 Application Curves

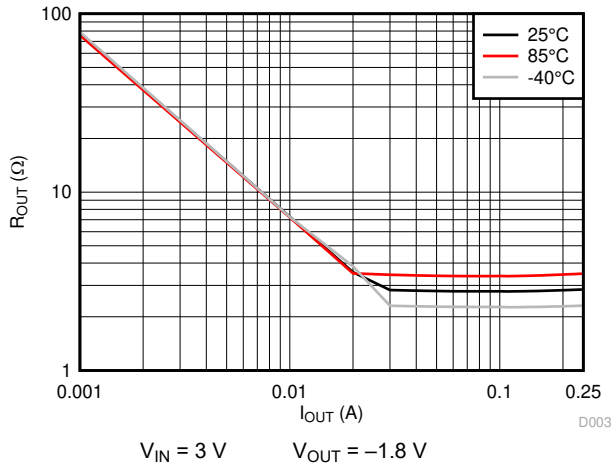


Figure 7-3. Charge-Pump Output Impedance vs Output Current

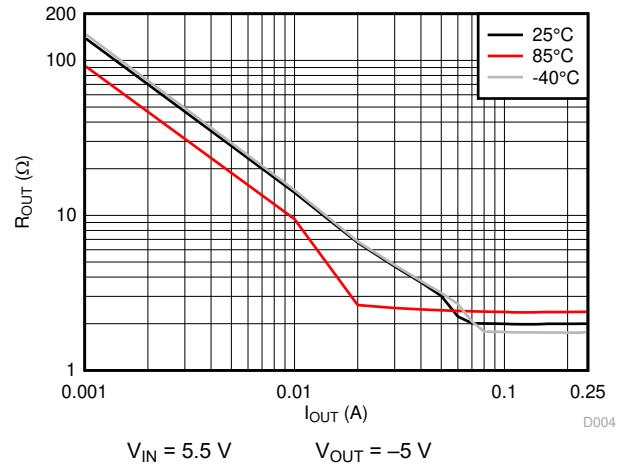


Figure 7-4. Charge-Pump Output Impedance vs Output Current

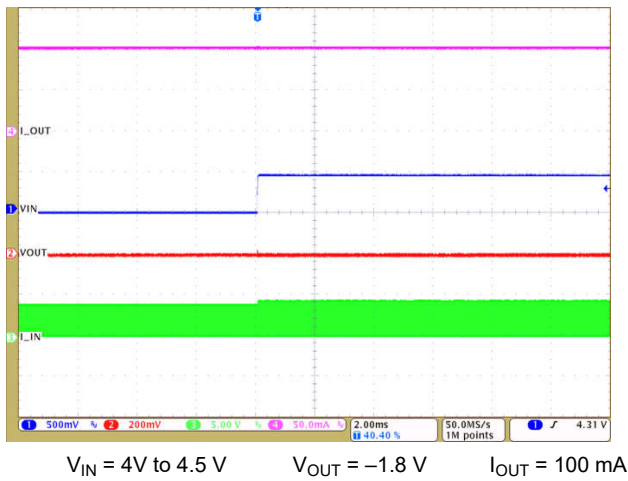


Figure 7-5. Line Step

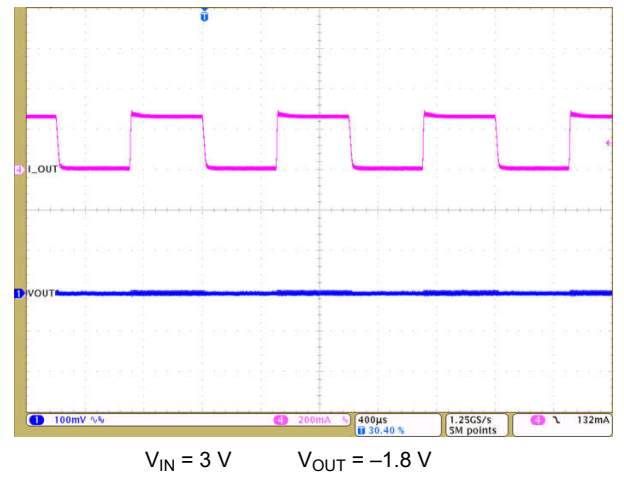


Figure 7-6. Load Step

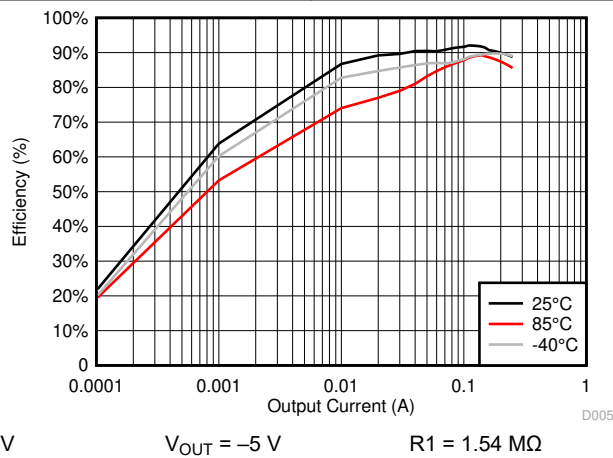


Figure 7-7. Efficiency vs Output Current

7.3 Power Supply Recommendations

The LM27761 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the LM27761, additional bulk capacitance can be required in addition to the ceramic bypass capacitors.

7.4 Layout

7.4.1 Layout Guidelines

The high switching frequency and large switching currents of the LM27761 make the choice of layout important. Use the following steps as a reference to make sure the device is stable and maintains proper LED current regulation across the intended operating voltage and current range:

- Place CIN on the top layer (same layer as the LM27761) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the VIN line.
- Place CCPOUT on the top layer (same layer as the LM27761) and as close to the VOUT and GND pins as possible. The returns for both CIN and CCPOUT must come together at one point, as close to the GND pin as possible. Connecting CCPOUT through short, wide traces reduces the series inductance on the VCPOUT and GND pins that can corrupt the VCPOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on top layer (same layer as the LM27761) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.
- Place COUT on the top layer (same layer as the LM27761) and as close to the VOUT pin as possible. For best performance the ground connection for COUT must connect back to the GND connection at the thermal pad of the device.
- Place R1 and R2 on the top layer (same layer as LM27761) and as close to the VFB pin as possible. For best performance the ground connection of R2 must connect back to the GND connection at the thermal pad of the device.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

7.4.2 Layout Example

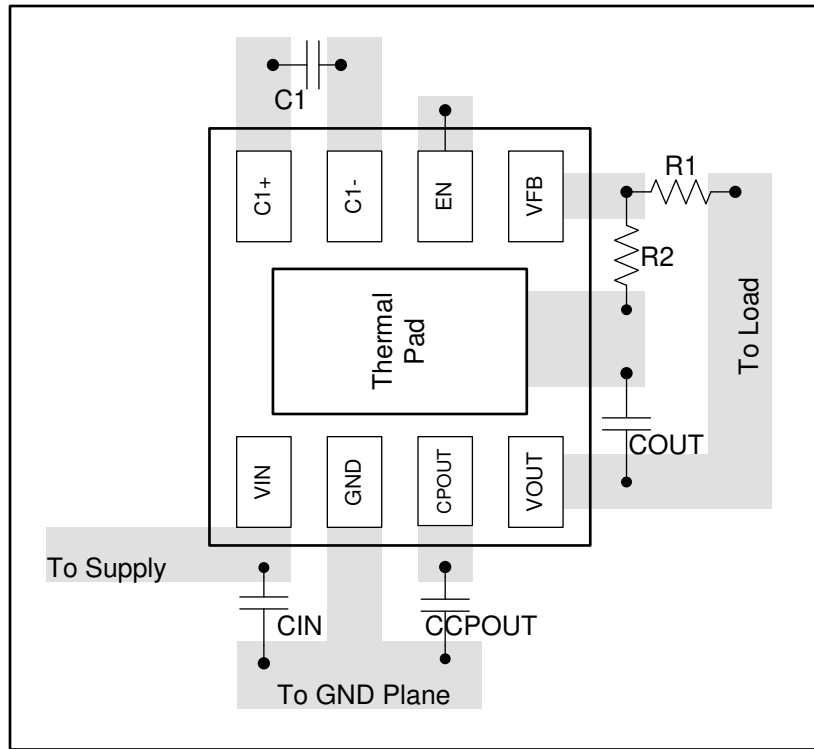


Figure 7-8. LM27761 Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision C (January 2017) to Revision D (October 2025) Page

- Deleted all WEBENCH information from the data sheet..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision B (February 2016) to Revision C (January 2017) Page

- Added links for WEBENCH 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM27761DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGLI
LM27761DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGLI
LM27761DSGRG4	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGLI
LM27761DSGRG4.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGLI
LM27761DSGT	Active	Production	WSON (DSG) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGLI
LM27761DSGT.A	Active	Production	WSON (DSG) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGLI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27761DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM27761DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM27761DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27761DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM27761DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
LM27761DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

DSG0008A



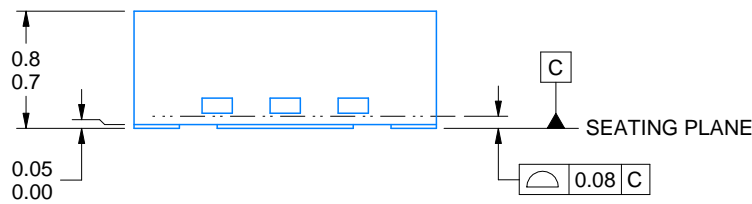
PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE
TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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