LM5125-Q1, Wide-VIN, Dual-Phase, Automotive, Boost Controller With V_{OUT} Tracking

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: T_A = –40°C to +125°C
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage 4.5V to 42V
  - Minimum 2.5V for $V_{(BIAS)}$ ≥ 4.5V or V_{OUT} ≥ 6V
- Output Voltage 6V to 60V
  - 2% accuracy, internal feedback resistors
  - Bypass operation for V_I > V_{OUT}
  - Dynamic output voltage tracking
    - Digital PWM tracking (DTRK)
    - Analog tracking (ATRK)
  - Overvoltage protection (64V, 50V, 35V, 28.5V)
- Low shutdown I_Q of 2µA
- Low operating I_Q of 1.4mA
- Switching frequency from 100kHz to 2.2MHz
  - Synchronization to external clock (SYNCIN)
  - Dynamically selectable switching modes (FPWM, diode emulation)
  - Spread spectrum (DRSS)
- Selectable dead time (14ns to 200ns)
- Current sense resistor or DCR sensing
- Average inductor current monitor
- Average input current limit
  - Programmable current limit
  - Selectable delay time
- Power-good indicator
- Programmable V_I undervoltage lockout (UVLO)
- Lead-less VQFN-32 package with wettable flanks

2 Applications

- High-end audio power supply
- Voltage stabilizer module
- Start-stop application

3 Description

The LM5125-Q1 is a dual-phase, synchronous boost controller. The device provides a regulated output voltage for lower or equal input voltage also supporting V_I to V_{OUT} bypass mode to save power.

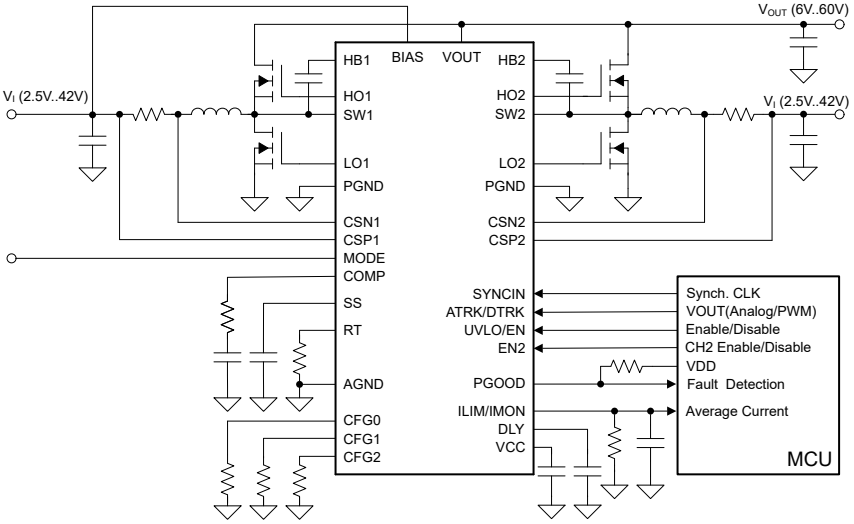
Dynamically program V_{OUT} using the analog or digital ATRK/DTRK function. V_I is supported down to 2.5V after start-up as the internal VCC supply is automatically switched from V_{BIAS} to V_{OUT} for V_{BIAS} < 4.5V. The fixed switching frequency is set between 100kHz and 2.2MHz through a resistor on the RT pin or the SYNCIN clock. The switching modes FPWM or diode emulation can be changed during operation.

The implemented protections peak current limit, average input current limit, average inductor current monitor, over and undervoltage protection, and the thermal shutdown protect the device and the application.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM5125-Q1	RHB (VQFN, 32)	5mm × 5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Pin Configuration and Functions

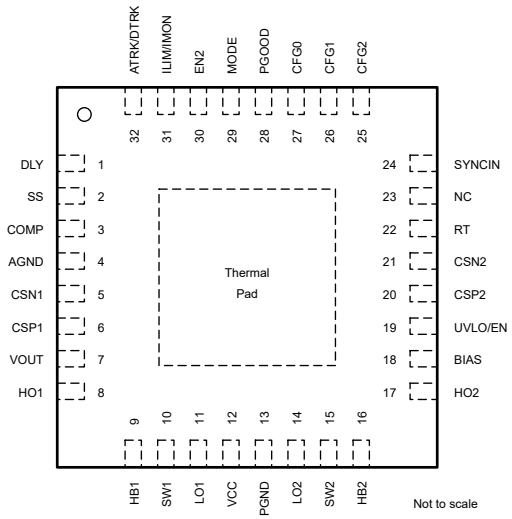


Figure 4-1. LM5125-Q1 RHB Package, 32-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	4	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
ATRK/DTRK	32	I	Output regulation target programming pin. Program the output voltage regulation target by connecting the pin through a resistor to AGND, or by controlling the pin voltage directly with a voltage in the recommended operating range of the pin from 0.2V to 2.0V. A digital PWM signal between 8% to 80% duty cycle is automatically detected at startup and enables the digital output voltage regulation, which programs V_{OUT} in the recommended operating range.
BIAS	18	P	Supply voltage input to the VCC regulator. Connect a 1µF local BIAS capacitor from the pin to ground.
CFG0	27	I/O	Device configuration pin. Sets the dead time and enables the 20µA ATRK current.
CFG1	26	I/O	Device configuration pin. Sets the overvoltage protection level, spread spectrum mode, PGOOD configuration and 120% peak current limit latch off.
CFG2	25	I/O	Device configuration pin. Sets if the device is using the internal or external clock and the Overvoltage Protection Level.
COMP	3	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
CSN1	5	I	Current sense amplifier input of phase 1. The pin operates as the negative input pin.
CSN2	21	I	Current sense amplifier input of phase 2. The pin operates as the negative input pin.
CSP1	6	I	Current sense amplifier input of phase 1. The pin operates as the positive input pin. Supply for the internal V_I undervoltage lockout circuit.
CSP2	20	I	Current sense amplifier input of phase 2. The pin operates as the positive input pin.
DLY	1	O	Average input current limit delay setting pin. A capacitor from DLY to AGND sets the delay from when V_{IMON} reaches 1V until the average input current limit is enabled.
EN2	30	I	Enable pin for phase 2.
EP	-	G	Exposed pad of the package. Connect the exposed pad to AGND and solder it to a large ground plane to reduce thermal resistance.

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
HB1	9	P	High-side driver supply for bootstrap gate drive for phase 1. Boot diode is internally connected from VCC to this pin. Connect a 0.1µF capacitor between the pin and SW1.
HB2	16	P	High-side driver supply for bootstrap gate drive for phase 2. Boot diode is internally connected from VCC to this pin. Connect a 0.1µF capacitor between the pin and SW2.
HO1	8	O	High-side gate driver output for phase 1. Connect to the gate of the high-side N-channel MOSFET through a short, low inductance path.
HO2	17	O	High-side gate driver output for phase 2. Connect to the gate of the high-side N-channel MOSFET through a short, low inductance path.
ILIM/IMON	31	O	Input current monitor and average input current limit setting pin. Sources a current proportional to phase 1 and phase 2 differential current sense voltage. A resistor is connected from this pin to AGND.
LO1	11	O	Low-side gate driver output for phase 1. Connect to the gate of the low-side N-channel MOSFET through a short, low inductance path.
LO2	14	O	Low-side gate driver output for phase 2. Connect to the gate of the low-side N-channel MOSFET through a short, low inductance path.
MODE	29	I	Operation mode selection pin selecting DEM or FPWM.
NC	23	-	Non Connect pin. Connect this pin to GND.
PGND	13	G	Power ground connection pin for low-side gate drivers and VCC bias supply.
PGOOD	28	O	Power-good indicator with open-drain output stage. The pin is pulled low when the output voltage is less than the undervoltage threshold or great than the overvoltage threshold based on the CFG1-pin setting. The pin is also pulled low indicating faults (see Power-Good Indicator (PGOOD-pin)). Connet the pin to AGND or leave the pin floating if not in use.
RT	22	I/O	Switching frequency setting pin. The switching frequency is programmed by a resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
SS	2	O	Soft start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft start time.
SW1	10	I	Switching node connection for phase 1. Connect directly to the source of the phase 1 high-side N-channel MOSFET.
SW2	15	I	Switching node connection for phase 2. Connect directly to the source of the phase 2 high-side N-channel MOSFET.
SYNCIN	24	I	External clock synchronization pin. Input for an external clock that overrides the free-running internal oscillator. Connect the SYNCIN pin to ground when not used.
UVLO/EN	19	I	Undervoltage lockout programming pin. Program the converter start-up and shutdown levels by connecting this pin to the supply voltage through a resistor divider. If greater than $V_{UVLO-RISING}$, phase 1 is enabled.
VCC	12	P	Output of the internal VCC regulator and supply voltage input of the internal MOSFET drivers. Connect a 10µF capacitor between the pin and PGND.
VOUT	7	P	Output voltage sensing pin. An internal feedback resistor voltage divider is connected from the pin to AGND. Connect a 0.1µF local VOUT capacitor from the pin to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)[1]

		MIN	MAX	UNIT
Input[2]	BIAS to AGND	–0.3	50	V
	UVLO/EN to AGND	–0.3	BIAS + 0.3	
	CSPx to AGND	–0.3	50	
	CSPx to CSNx	–0.3	0.3	
	VOUT to AGND	-0.3	65	
	HBx to AGND	–0.3	71	
	HBx to SWx	–0.3	5.8[3]	
	SWx to AGND	–0.3	65	
	SWx to AGND (10ns)	–5	65	
	CFG0, CFG1, CFG2, SYNCIN, ATRK/DTRK, DLY, MODE, EN2 to AGND	–0.3	5.5	
	RT to AGND	–0.3	2.5	
	PGND to AGND	–0.3	0.3	
Output[2]	VCC to AGND	–0.3	5.8[3]	V
	HOx to SWx (50ns)	–1	HBx + 0.3	
	LOx to AGND (50ns)	–1	VCC + 0.3	
	PGOOD, SS, COMP, ILIM/IMON to AGND	–0.3	5.5	
Operating junction temperature, T_J [4]		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) It is not allowed to apply an external voltage directly to CFG0, CFG1, CFG2, COMP, SS, RT, LOx, HOx pins.
(3) Operating lifetime is derated when the pin voltage is greater than 5.5V.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
V_I	Boost Controller Input Voltage (when BIAS ≥ 4.5V or VOUT ≥ 6V)	2.5		42	V
V_{OUT}	Boost Controller Output Voltage	6		60	V
V_{BIAS}	BIAS Input Voltage	4.5		42	V
$V_{UVLO/EN}$	UVLO/EN Input Voltage	0		42	V
V_{EN2}	EN2 Input Voltage	0		5.25	V
V_{MODE}	MODE Input Voltage	0		5.25	V
V_{CSP1}, V_{CSN1}, V_{CSP2}, V_{CSN2}	Current Sense Input Voltage	2.5		42	V
V_{ATRK}	ATRK Input Voltage	0.2		2	V
V_{DTRK}	DTRK Input Voltage	0		5.25	V
V_{DLY}	DLY Voltage	0		5.25	V
V_{PGOOD}	PGOOD Voltage	0		5.25	V
$V_{ILIM/IMON}$	ILIM/IMON Voltage	0		3	V
V_{SYNCIN}	Synchronization Pulse Input Voltage	0		5.25	V
f_{SW}	Switching Frequency Range	100		2200(2)	kHz
f_{SYNCIN}	Synchronization Pulse Frequency Range	100		2200(2)	kHz
f_{DTRK}	DTRK Frequency Range	100		2200	kHz
T_J	Operating Junction Temperature	–40		150(3)	°C

(1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*
(2) Maximum switching frequency is programmed by R_{RT}. The device supports up to 2200kHz switching.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		LM5125-Q1 RHB(VQFN) 32 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	33.9	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	24.8	°C/W
R_{qJB}	Junction-to-board thermal resistance	14.1	°C/W
y_{JT}	Junction-to-top characterization parameter	0.4	°C/W
y_{JB}	Junction-to-board characterization parameter	14.0	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, V_I = V_{BIAS} = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (BIAS, VCC, VOUT)						
I_{SD}	V_I current in shutdown state (BIAS connected to V_I). Current into BIAS, CSP1, CSN1, CSP2, CSN2, SW1, SW2.	$V_{EN/UVLO}$ = 0 V, V_{OUT} = 12V, T_J = –40°C to 125°C		2	5	µA

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_I = V_{BIAS}$ = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD_BIAS}	BIAS-pin current in shutdown state	$V_{EN/UVLO}$ = 0V, V_{OUT} = 12V, T_J = –40°C to 125°C		2	5	µA
I_{SD_VOUT}	VOUT-pin current in shutdown state	$V_{EN/UVLO}$ = 0V, V_{OUT} = 12V, T_J = –40°C to 125°C		0.001	0.5	µA
$I_{Q\_BIAS\_FPWM}$	BIAS-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching, RT and IMON current is excluded)	1-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 0V, V_{CFG2} = 0V, V_{ATRK} = 0.667V, T_J = –40°C to 125°C		1.1	1.5	mA
		2-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 2V, V_{CFG2} = 0V, V_{ATRK} = 0.667V, T_J = –40°C to 125°C		1.6	2	mA
$I_{Q\_BIAS\_DEM}$	BIAS-pin quiescent current in active state, DEM-Mode, internal clock (not-switching, RT and IMON current is excluded)	1-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 0V, V_{CFG2} = 0V, V_{ATRK} = 0.667V, T_J = –40°C to 125°C		1.1	1.5	mA
		2-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 2V, V_{CFG2} = 0V, V_{ATRK} = 0.667V, T_J = –40°C to 125°C		1.6	2	mA
$I_{Q\_VOUT\_FPWM}$	VOUT-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching)	2-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 2V, V_{CFG2} = 0V, V_{ATRK} = 0.667V, T_J = –40°C to 125°C		250	300	µA
$I_{Q\_BIAS\_BYP}$	BIAS-pin current in bypass state (RT and IMON current is excluded)	1-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 0V, V_{CFG2} = 0V, V_{OUT} = 12V, T_J = –40°C to 125°C		1	1.5	mA
	BIAS-pin current in bypass state (RT and IMON current is excluded)	2-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 2V, V_{CFG2} = 0V, V_{OUT} = 12V, T_J = –40°C to 125°C		1.5	2.0	mA
$I_{Q\_VOUT\_BYP}$	VOUT-pin current in bypass state	2-phase, $V_{EN/UVLO}$ = 2.0V, V_{EN2} = 2V, V_{CFG2} = 0V, V_{OUT} = 12V, T_J = –40°C to 125°C, no resistor between HO and SW.		280	330	µA
I_{BIAS}	BIAS-pin bias current	V_{BIAS} = 12V, I_{VCC} = 200mA		200	210	mA
I_{VOUT}	VOUT-pin bias current when VCC is supplied by VOUT	V_{BIAS} = 3.3V, I_{VCC} = 200mA		200	230	mA
VCC REGULLATOR (VCC)						
$V_{BIAS-RISING}$	Threshold to switch VCC supply from VOUT-pin to BIAS-pin	V_{BIAS} rising	4.25	4.35	4.45	V
$V_{BIAS-FALLING}$	Threshold to switch VCC supply from BIAS-pin to VOUT-pin	V_{BIAS} falling	4.1	4.2	4.3	V
$V_{BIAS-HYS}$	VCC supply threshold hysteresis		100	150		mV
$V_{VCC-REG1}$	VCC regulation	No load	4.75	5	5.25	V
$V_{VCC-REG2}$	VCC regulation during dropout	V_{BIAS} = 4.5V, I_{VCC} = 110mA	4	4.3		V
$V_{VCC-UVLO-RISING}$	VCC UVLO threshold	VCC rising	3.4	3.5	3.6	V
$V_{VCC-UVLO-FALLING}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V
$V_{VCC-UVLO-HYS}$	VCC UVLO threshold hysteresis	VCC falling		215		mV
I_{VCC-CL}	VCC sourcing current limit	V_{VCC} = 4V	200			mA
ENABLE (EN/UVLO)						
$V_{EN-RISING}$	Enable threshold	EN rising	0.50	0.55	0.6	V
$V_{EN-FALLING}$	Enable threshold	EN falling	0.40	0.45	0.50	V
V_{EN-HYS}	Enable hysteresis	EN falling		100		mV
R_{EN}	EN pulldown resistance	V_{EN} = 0.2V	30	37	50	kΩ

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_I = V_{BIAS}$ = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO-RISING}$	UVLO threshold		UVLO rising	1.05	1.1	1.15	V
$V_{UVLO-FALLING}$	UVLO threshold		UVLO falling	1.025	1.075	1.125	V
$V_{UVLO-HYS}$	UVLO hysteresis		UVLO falling		25		mV
$I_{UVLO-HYS}$	UVLO pulldown hysteresis current		V_{UVLO} = 0.7V	9	10	11	µA
$I_{UVLO/EN}$	UVLO/EN-pin bias current		$V_{UVLO/EN}$ = 0.3V, pull-down resistor = active.		8	11	µA
			$V_{UVLO/EN}$ = 0.7V, 10µA current = active.	9	10	11	µA
			$V_{UVLO/EN}$ = 3.3V			1	µA
CH2 ENABLE (EN2)							
V_{EN2_H}	Enable 2 high level input voltage		EN2 rising	1.19		5.25	V
V_{EN2_L}	Enable 2 low level input voltage		EN2 falling	–0.3		0.41	V
I_{EN2}	Enable 2 bias current		EN1 = EN2 = 3.3V		0.01	1	µA
CONFIGURATION (CFG0, CFG1, CFG2)							
R_{CFGx_1}	Level 1 resistance				0	0.1	kΩ
R_{CFGx_2}	Level 2 resistance			0.496	0.51	0.526	kΩ
R_{CFGx_3}	Level 3 resistance			1.11	1.15	1.19	kΩ
R_{CFGx_4}	Level 4 resistance			1.81	1.9	1.93	kΩ
R_{CFGx_5}	Level 5 resistance			2.65	2.7	2.82	kΩ
R_{CFGx_6}	Level 6 resistance			3.71	3.8	3.94	kΩ
R_{CFGx_7}	Level 7 resistance			4.95	5.1	5.26	kΩ
R_{CFGx_8}	Level 8 resistance			6.29	6.5	6.68	kΩ
R_{CFGx_9}	Level 9 resistance			8.00	8.3	8.50	kΩ
R_{CFGx_10}	Level 10 resistance			10.18	10.5	10.81	kΩ
R_{CFGx_11}	Level 11 resistance			12.90	13.3	13.70	kΩ
R_{CFGx_12}	Level 12 resistance			15.71	16.2	16.69	kΩ
R_{CFGx_13}	Level 13 resistance			19.88	20.5	21.11	kΩ
R_{CFGx_14}	Level 14 resistance			24.15	24.9	25.65	kΩ
R_{CFGx_15}	Level 15 resistance			29.20	30.1	31.00	kΩ
R_{CFGx_16}	Level 16 resistance			35.40	36.5	38.60	kΩ
SWITCHING FREQUENCY							
V_{RT}	RT regulation			0.7	0.75	0.8	V
f_{SW1}	Switching frequency		R_T = 316kΩ	85	100	115	kHz
f_{SW2}	Switching frequency		R_T = 14kΩ	1980	2200	2420	kHz
t_{ON-MIN}	Minimum controllable on-time		R_T = 14kΩ	14	20	50	ns
$t_{OFF-MIN}$	Minimum forced off-time		R_T = 14kΩ	55	80	105	ns
D_{MAX1}	Maximum duty cycle limit		R_T = 316kΩ	98.7%	99.4%		
D_{MAX2}	Maximum duty cycle limit		R_T = 14kΩ	75%	87%		
SYNCHRONIZATION (SYNCIN)							
	Minimum SYNCIN frequency activity detection	Spread Spectrum = off	RT = 316kΩ	60			kHz
	SYNCIN frequency activity detection vs RT set switching frequency	Spread Spectrum = off	RT = 14kΩ to 210kΩ	–60%			
	SYNCIN activity detection cycles				3		cycles

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_I = V_{BIAS}$ = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYNC}	Syncing frequency range from RT set frequency during synchronization	Frequency synchronized to ext. clock min. = 100kHz, max. = 2200kHz	–50%		50%	
V_{SYNCIN_H}	SYNCIN high level input voltage	SYNCIN rising	1.19		5.25	V
V_{SYNCIN_L}	SYNCIN low level input voltage	SYNCIN falling	–0.3		0.41	V
I_{SYNCIN}	SYNCIN bias current	SYNCIN = 3.3V		0.01	1	µA
	Minimum SYNCIN pullup / pulldown pulse width		135			ns
VOUT PROGRAMMING (ATRK/DTRK)						
V_{OUT_REG}	V_{OUT} regulation with ATRK voltage	ATRK = 0.2V, V_I = 4.5V	5.88	6	6.12	V
		ATRK = 0.4V, V_I = 10V	11.82	12	12.18	V
		ATRK = 0.8V	23.64	24	24.36	V
		ATRK = 1.6V	47.28	48	48.72	V
		ATRK = 2V	59.10	60	60.90	V
G_{DTRK}	Conversion ratio of DTRK duty cycle to V_{ATRK}	F_{DTRK} = 100kHz, 440kHz		25		mV / %
	DTRK duty cycle range		8%		80%	
V_{ATRK}	ATRK voltage for given DTRK duty cycle	f_{DTRK} = 100kHz, DC = 8%	0.19	0.2	0.21	V
		f_{DTRK} = 100kHz, DC = 40%	0.98	1	1.02	V
		f_{DTRK} = 100kHz, DC = 80%	1.98	2	2.02	V
		f_{DTRK} = 440kHz, DC = 8%	0.188	0.2	0.212	V
		f_{DTRK} = 440kHz, DC = 40%	0.98	1	1.02	V
		f_{DTRK} = 440kHz, DC = 80%	1.98	2	2.02	V
V_{DTRK_H}	DTRK high level input voltage	DTRK rising	1.19		5.25	V
V_{DTRK_L}	DTRK low level input voltage	DTRK falling	–0.3		0.41	V
I_{ATRK}	Source current when activated through CFG0		19.8	20	20.2	µA
$I_{ATRK/DTRK}$	ATRK/DTRK-pin bias current	20µA current is disabled, $V_{ATRK/DTRK}$ = 2V		0.01	1	µA
	Minimum DTRK pullup / pulldown pulse width		25			ns
SOFT START (SS)						
I_{SS}	Soft-start current		42.5	50	57.5	µA
$V_{SS-DONE}$	Soft-start done threshold		2.15	2.2	2.25	V
R_{SS}	SS pulldown switch R_{DSON}			26	70	Ω
V_{SS-DIS}	SS discharge detection threshold		20	45	70	mV
CURRENT SENSE (CSPx, CSNx)						
A_{CS}	Current sense amplifier gain	V_{CSP} = 2.5V		10		V/V
V_{CLTH}	Positive peak current limit threshold	Referenced to CS input	54	60	66	mV
V_{NCLTH}	Negative peak current limit threshold	Referenced to CS input, FPWM mode	–34	–28	–22	mV
V_{ICL}	Input current limit	Referenced to CS input	65	72	80	mV
ΔV_{ICL_CLTH}	Delta voltage between ICL and positive peak current threshold		6	12		mV
	Peak current limit trip delay			100		ns
V_{ZCD}	ZCD threshold (CSPx – CSNx)	CS input falling, f_{SW} = 100kHz, DEM	0	3	6	mV
V_{ZCD}	ZCD threshold (CSPx – CSNx)	CS input falling, f_{SW} = 100kHz, DEM, T_J = 0°C to 85°C	0	3	5	mV

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, V_I = V_{BIAS} = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ZCD_BYP}	ZCD threshold for phase 1 in bypass mode (CSP1 – CSN1)			–6	–2.5	0	mV
	ZCD threshold for phase 2 in bypass mode (CSP2 – CSN2)			–6	–2.5	0	mV
V_{SLOPE}	Peak slope compensation amplitude		Referenced to CS input, f_{SW} = 100kHz	40	48	55	mV
I_{CSNx}	CSNx current		Device in Standby state, V_I = V_{BIAS} = V_{OUT} = 12V			1.2	µA
I_{CSPx}	CSPx current				150	170	µA
ΔI_{ph1_ph2}	Peak Inductor Current unbalance (Phase 1 to Phase 2)		V_{CL} = 60mV	–10	0	10	%
CURRENT MONITOR / LIMITER WITH DELAY (IMON/ILIM)							
G_{IMON}	Transconductance Gain			0.320	0.333	0.346	µA/mV
I_{OFFSET}	Offset current			3	4	5	µA
V_{ILIM}	ILIM regulation target			0.93	1	1.07	V
V_{ILIM_th}	ILIM activation threshold			0.95	1	1.25	V
V_{ILIM_reset}	DLY reset threshold		ILIM falling, referenced to V_{ILIM}	85%	88%	91%	
I_{DLY}	DLY sourcing/sinking current			4	5	6	µA
$V_{DLY\_peak\_rise}$			V_{DLY} rising	2.45	2.6	2.75	V
$V_{DLY\_peak\_fall}$			V_{DLY} falling	2.25	2.4	2.55	V
V_{DLY_valley}					0.2		V
ERROR AMPLIFIER (COMP)							
Gm	Transconductance			700	1000	1300	uS
$A_{COMP-PWM}$	COMP-to-PWM gain				1		V/V
$V_{COMP-MAX}$	COMP maximum clamp voltage		COMP rising	2.3	2.6	2.9	V
$V_{COMP-MIN}$	COMP minimum clamp voltage, active in DEM		COMP falling	0.38	0.48	0.55	V
	COMP minimum clamp voltage, active in FPWM		COMP falling	0.13	0.16	0.19	V
$V_{COMP-offset}$	Offset in respect to min clamp		COMP falling	0.01	0.03	0.06	V
$I_{SOURCE-MAX}$	Maximum COMP sinking current		V_{COMP} = 0V	90			µA
$I_{SINK-MAX}$	Maximum COMP sourcing current		V_{COMP} = 2.6V	100			µA
OPERATION MODES							
V_{MODE_H}	MODE-pin high level	FPWM		1.19		5.25	V
V_{MODE_L}	MODE-pin low level	DEM		–0.3		0.41	V
I_{MODE}	MODE-pin bias current		MODE = 3.3V		0.01	1	µA
OVER / UNDER VOLTAGE MONITOR							
V_{OVP-H}	Overvoltage threshold		V_{OUT} rising (referenced to error amplifier reference)	108%	110%	112%	
V_{OVP-L}	Overvoltage threshold		V_{OUT} falling (referenced to error amplifier reference)	101%	103%	105%	
V_{OVP_max-H}	Overvoltage threshold	64V	V_{OUT} rising (referenced to error amplifier reference)	63	64	65	V
		50V		49	50	51	V
		35V		34	35	36	V
		28.5V		27	28.5	30	V

5.5 Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 150°C. Unless otherwise stated, $V_I = V_{BIAS}$ = 12V, V_{OUT} = 24V, R_T = 14kΩ

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_max-L}	Overvoltage threshold	64V	V_{OUT} falling (referenced to error amplifier reference)	62	63	64	V
		50V		48	49	50	V
		35V		33	34	35	V
		28.5V		26	27.5	29	V
V_{UVP-H}	Undervoltage threshold		V_{OUT} rising (referenced to error amplifier reference)	91%	93%	95%	
V_{UVP-L}	Undervoltage threshold		V_{OUT} falling (referenced to error amplifier reference)	88%	90%	92%	
PGOOD							
R_{PGOOD}	PGOOD pulldown switch R_{DSON}		1mA sinking		90	180	Ω
	Minimum BIAS for valid PGOOD			2			V
MOSFET DRIVER (HBx, HOx, SWx, LOx)							
	High-state on resistance (HO driver)		100mA sinking, HB – SW = 5V		1.1	2	Ω
	Low-state on resistance (HO driver)		100mA sourcing, HB – SW = 5V		0.6	1.2	Ω
	High-state on resistance (LO driver)		100mA sinking, VCC = 5V		1.1	2	Ω
	Low-state on resistance (LO driver)		100mA sourcing, VCC = 5V		0.7	1.4	Ω
$V_{HB-UVLO}$	HB – SW UVLO threshold		HB – SW rising	2.85	3.05	3.25	V
$V_{HB-UVLO}$	HB – SW UVLO threshold		HB – SW falling	2.6	2.8	3	V
V_{HB-HYS}	HB – SW UVLO threshold hysteresis				250		mV
$I_{HB-SLEEP}$	HB quiescent current in bypass		HB – SW = 5V		8	15	µA
I_{CP}	HB charge pump current available at HBx-pin		BIAS = 4.5V, VOUT = 6V	55	75	100	µA
DEAD TIME CONTROL							
DT1	HO off to LO on and LO off to HO on dead time	Setting 1		7	14	30	ns
DT2		Setting 2		17	30	50	ns
DT3		Setting 3		32	50	75	ns
DT4		Setting 4		50	75	110	ns
DT5		Setting 5		68	100	140	ns
DT6		Setting 6		85	125	180	ns
DT7		Setting 7		105	150	215	ns
DT8		Setting 8		135	200	285	ns
THERMAL SHUTDOWN (TSD)							
$T_{TSD-RISING}$	Thermal shutdown threshold		Temperature rising		175		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis				15		°C
TIMINGS							
$STANDBY_{timer}$	STANDBY timer			130	150	170	µs

5.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H	1			µs

5.7 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

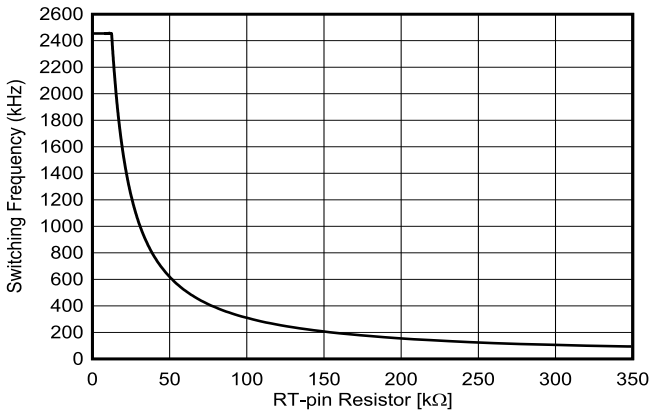


Figure 5-1. Switching Frequency Versus RT Resistance

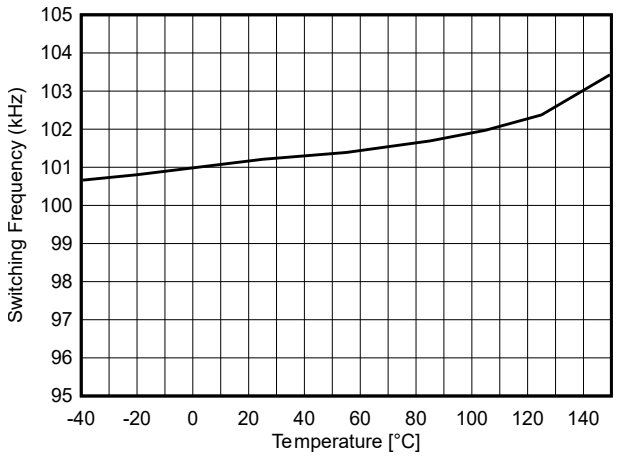


Figure 5-2. Switching Frequency (100kHz, RT = 316kΩ) vs Temperature

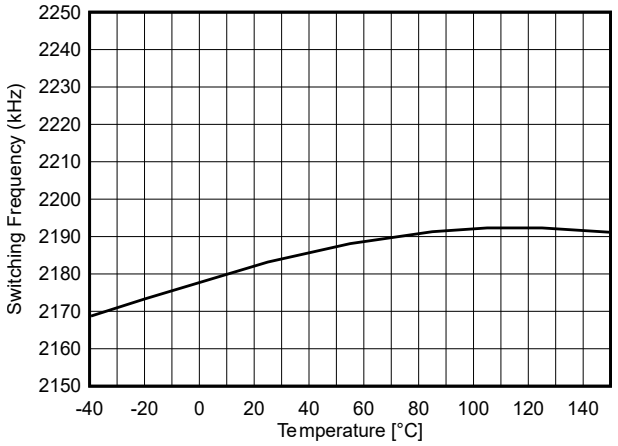


Figure 5-3. Switching Frequency (2200kHz, RT = 14kΩ) vs Temperature

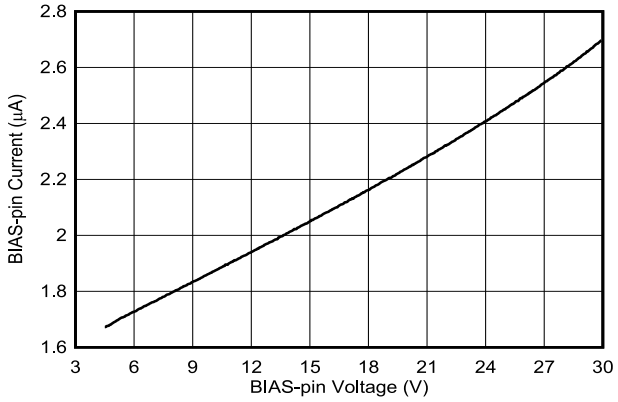


Figure 5-4. BIAS-pin Current vs BIAS-pin Voltage during shutdown

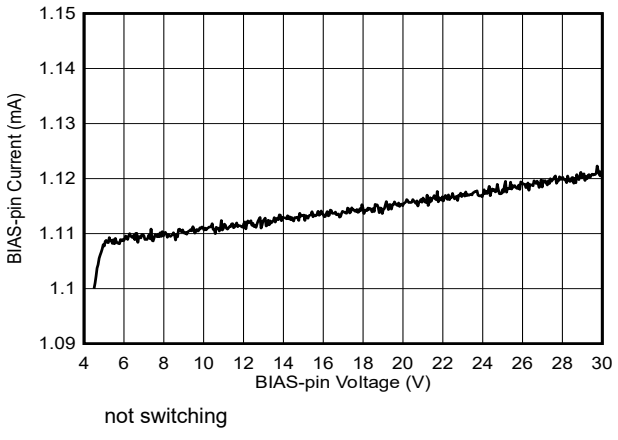


Figure 5-5. BIAS-pin Current vs BIAS-pin Voltage (Active, 1ph, DEM)

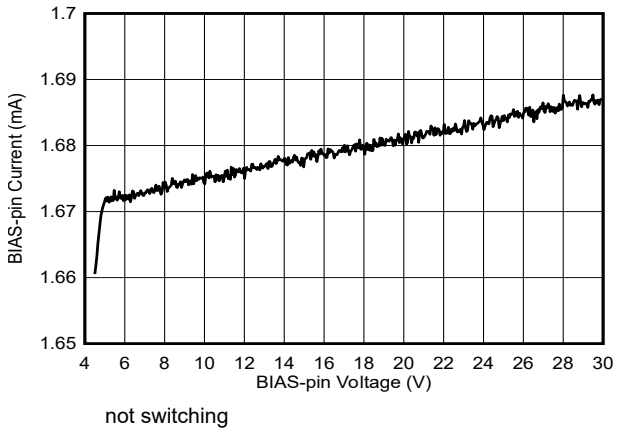


Figure 5-6. BIAS-pin Current vs BIAS-pin Voltage (Active, 2ph, DEM)

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

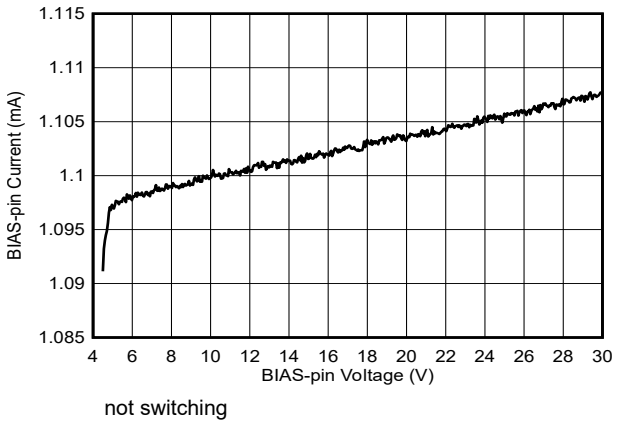


Figure 5-7. BIAS-pin Current vs BIAS-pin Voltage (Active, 1ph, FPWM)

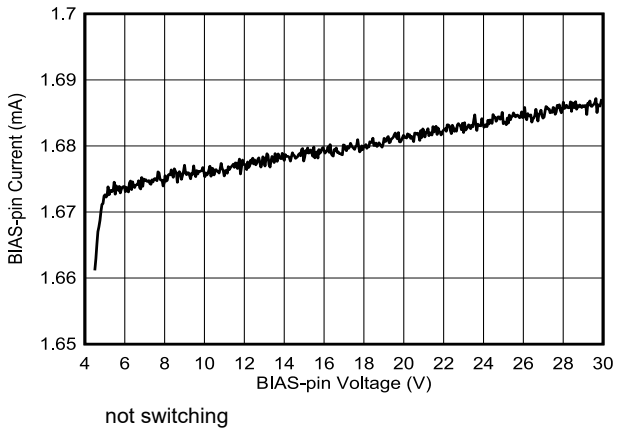


Figure 5-8. BIAS-pin Current vs BIAS-pin Voltage (Active, 2ph, FPWM)

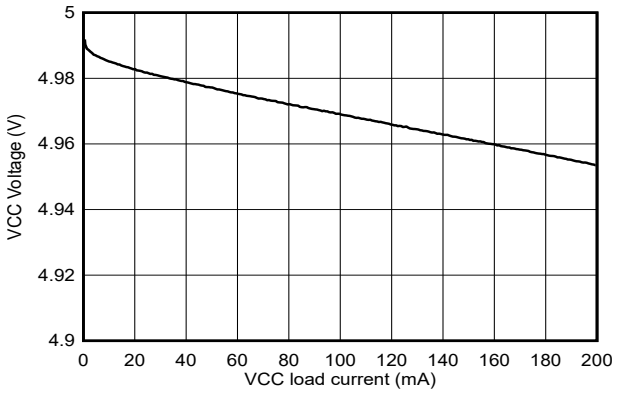


Figure 5-9. VCC Voltage vs VCC Load Current

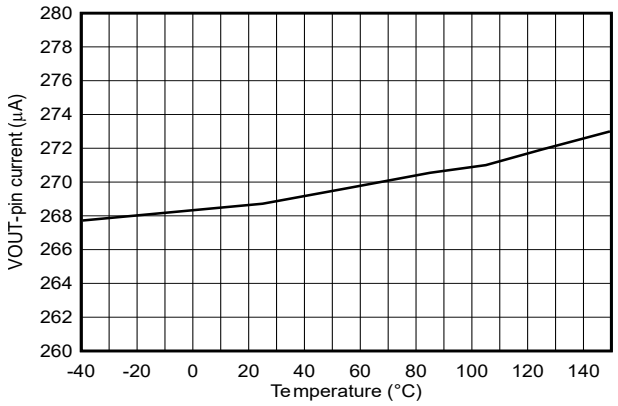


Figure 5-10. VOUT-pin Current vs Temperature (Bypass, 2ph)

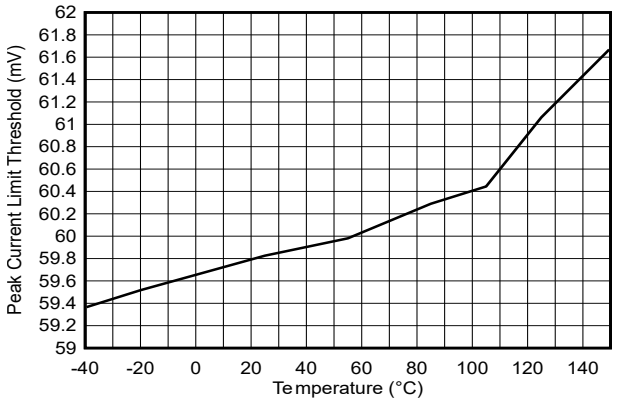


Figure 5-11. Peak Current Limit Threshold V_{CLTH} vs Temperature

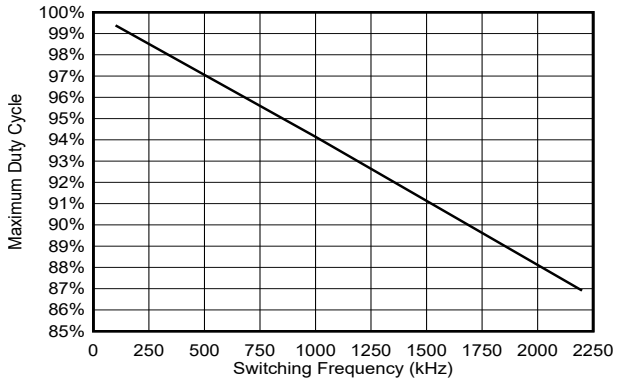


Figure 5-12. Maximum Duty Cycle vs Switching Frequency

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

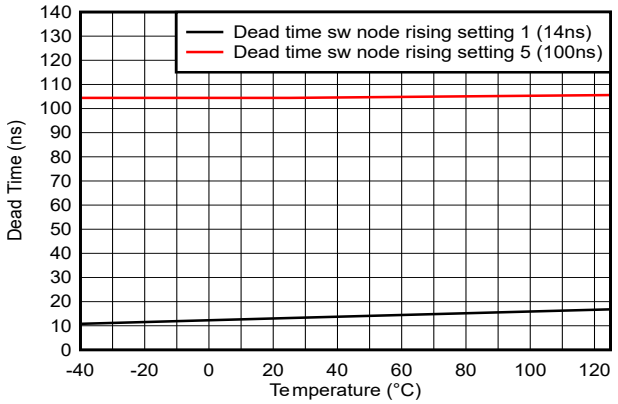


Figure 5-13. Dead Time Switch Node Rising vs Temperature

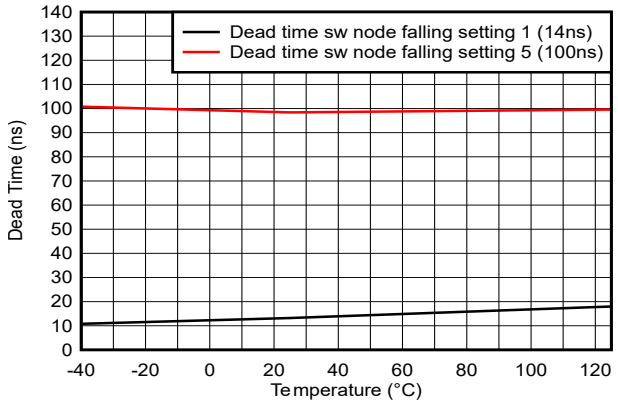


Figure 5-14. Dead Time Switch Node Falling vs Temperature

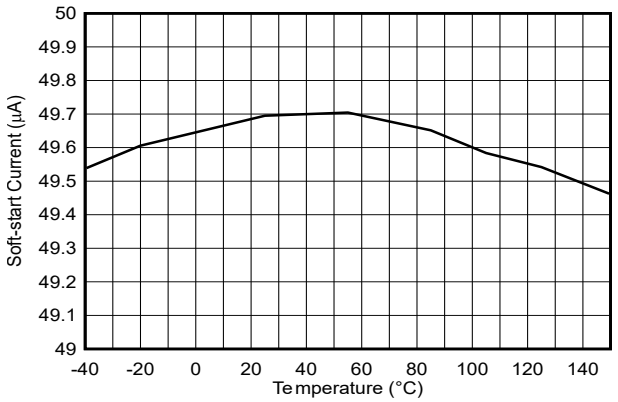


Figure 5-15. Soft-start Current vs Temperature

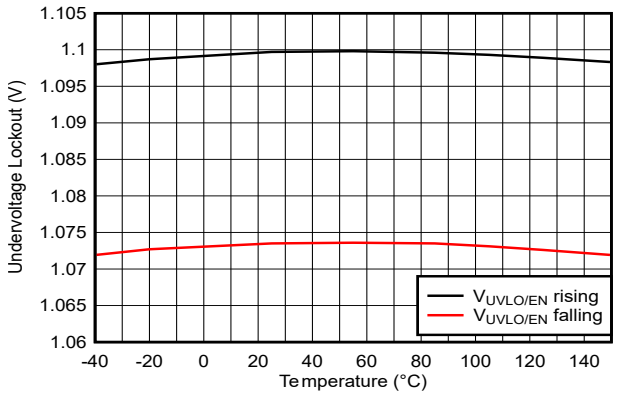


Figure 5-16. Undervoltage Lockout (UVLO) vs Temperature

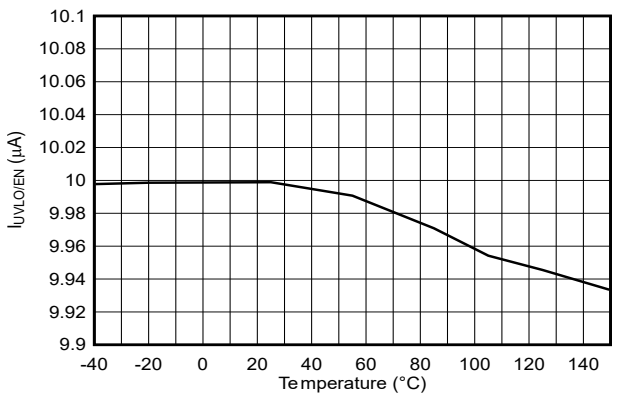


Figure 5-17. UVLO/EN-pin Current vs Temperature

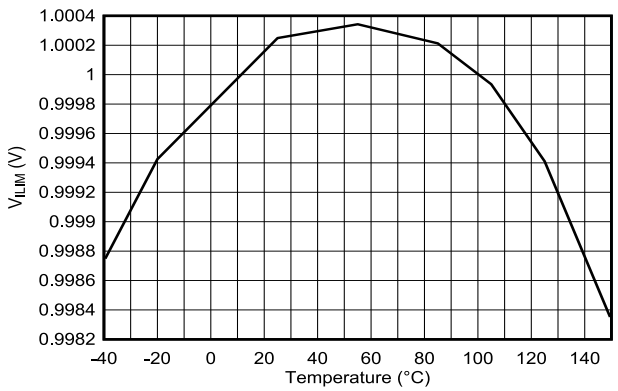


Figure 5-18. Average Current Limit Regulation Voltage vs Temperature

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

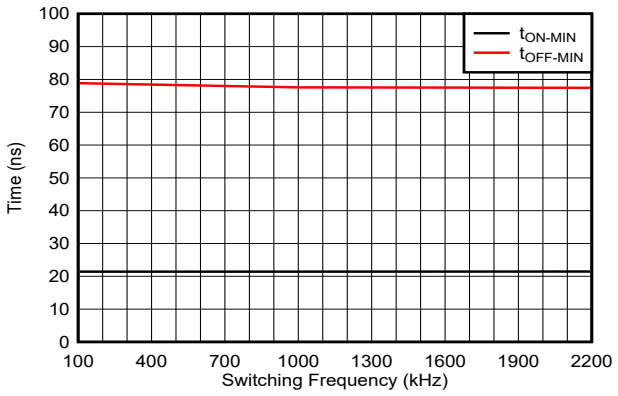


Figure 5-19. Minimum t_{ON} and t_{OFF} Time vs Switching Frequency

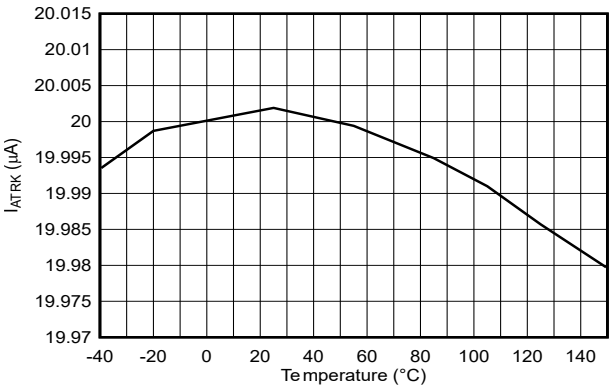
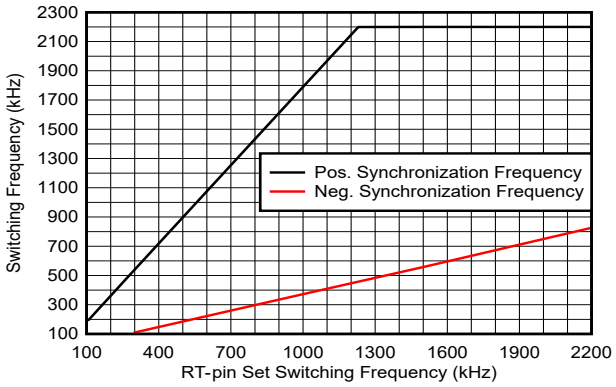


Figure 5-20. ATRK-pin Current vs Temperature



Spread Spectrum = off

Figure 5-21. Synchronization Switching Frequency (SYNCIN) vs RT-pin Set Switching Frequency

6 Detailed Description

6.1 Overview

The LM5125-Q1 is a wide input range dual phase boost controller. The device provides a regulated output voltage if the input voltage is equal or lower than the adjusted output voltage. The resistor-to-digital (R2D) interface offers the user a simple and robust selection of the device functionality.

The operation modes DEM (Diode Emulation Mode) and FPWM (Forced Pulse Width Modulation) are on-the-fly pin-selectable during operation. The peak current mode control operates with fixed switching frequency set by the RT-pin. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

The integrated average current monitor helps to monitor or limit the input current. The output voltage can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). Adjusting V_{OUT} is possible by changing the analog reference voltage of the ATRK/DTRK-pin or with a PWM input signal on the ATRK/DTRK pin.

The internal wide input LDOs provide a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltage selection (V_{BIAS} or V_{OUT}), the power losses are kept at a minimum. Connect the separate BIAS-pin to V_I, V_{OUT} or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The device integrates a half bridge N-channel MOSFET driver. The gate driver circuit has a high driving capability to drive a wide range of MOSFETs. The gate driver features an integrated high voltage low dropout bootstrap diode. The internal bootstrap circuit has a protection against an overvoltage that is injected by negative spikes and an undervoltage lockout protection to avoid a linear operation of the external power FET. An integrated charge pump enables 100% duty cycle operation in BYPASS mode.

The built-in protection features provide a safe operation under different fault conditions. There is a V_I undervoltage lockout protection to avoid brownout situations. Brownout is avoided under different designs because the input UVLO threshold and hysteresis is configured through an external feedback divider. The device also incorporates an output overvoltage protection. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition of the internal VCC regulators. All output-related fault events are monitored and indicated at the open-drain PGOOD-pin.

6.2 Functional Block Diagram

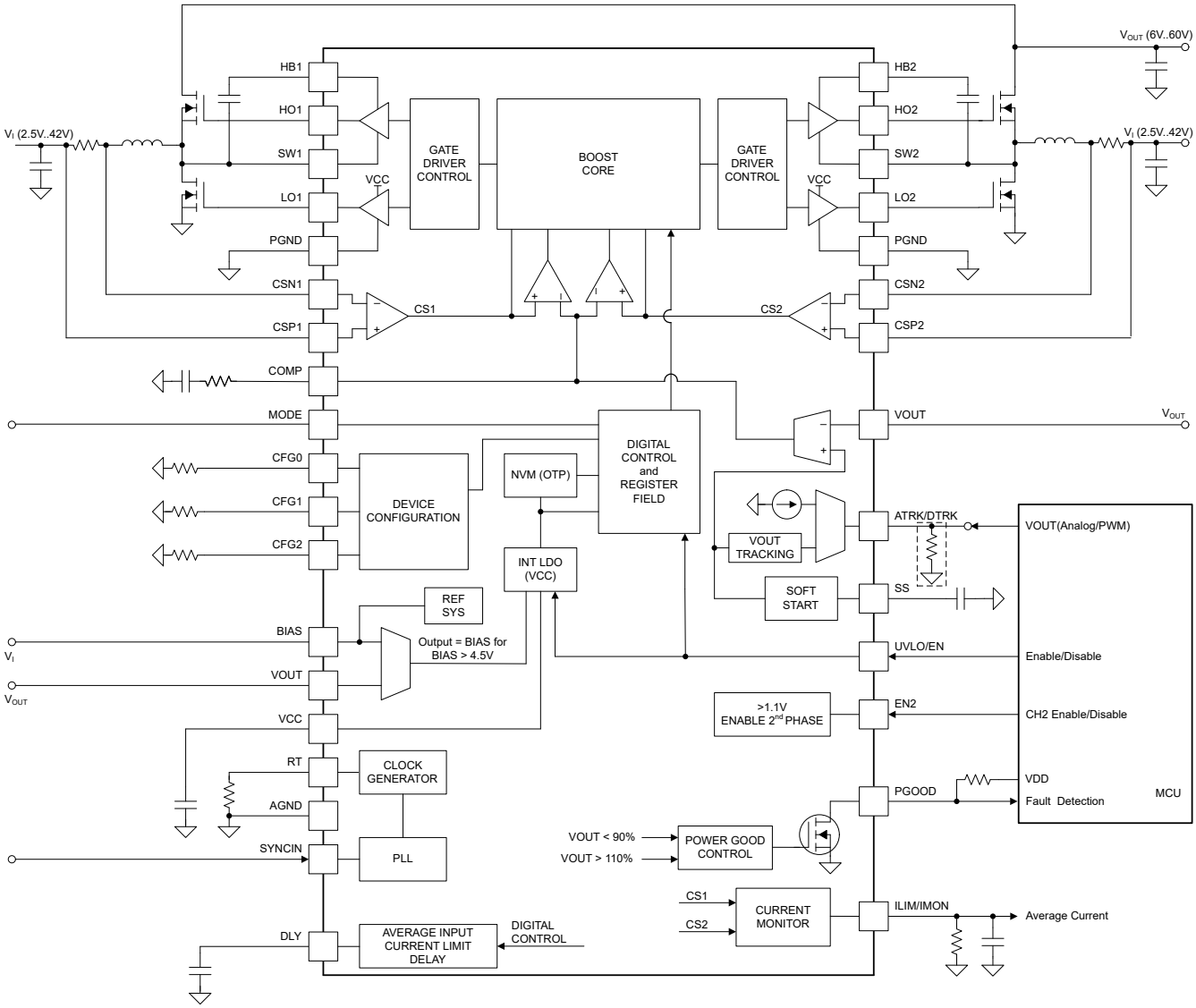


Figure 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Device Configuration (CFG0-pin, CFG1-pin, CFG2-pin)

The CFG0-pin defines the minimum dead time and the ATRK/DTRK-pin 20µA current. The levels shown in Table 6-1 are selected by the specified resistors in the Specifications section. When V_{OUT} is programmed with a resistor turn the 20µA ATRK-pin current on, for voltage tracking turn the ATRK-pin current off.

Table 6-1. CFG0-pin Settings

Level	Dead Time [ns]	20µA ATRK Current
1	14	on
2	30	on
3	50	on
4	75	on
5	100	on
6	125	on
7	150	on
8	200	on
9	14	off
10	30	off
11	50	off
12	75	off
13	100	off
14	125	off
15	150	off
16	200	off

The CFG1-pin setting defines the V_{OUT} overvoltage protection level, Clock Dithering, the 120% input current limit protection (I_{CL_latch}) operation, and the power-good pin behavior.

OVP bit 0: OVP bit 1 and 0 set the V_{OUT} overvoltage protection level. [00] = 64V, [01] = 50V, [10]= 35V or [11] = 28.5V.

Clock Dithering: Enables dual random spread spectrum (DRSS) clock dithering or disables clock dithering.

I_{CL_latch}: When I_{CL_latch} is enabled and the peak current limit is exceeded by 20% the device goes to the Shutdown State (turns off and is latched). If I_{CL_latch} is disabled the device stays active and tries to limit the inductor current at peak current limit.

$PGOOD_{OVP\_enable}$: When $PGOOD_{OVP\_enable}$ is enabled the PGOOD-pin is pulled low for V_{OUT} above OVP (Overvoltage Protection) or below the UV (Undervoltage) threshold. If $PGOOD_{OVP\_enable}$ is disabled the PGOOD-pin is only pulled low when V_{OUT} is below UV (Undervoltage) threshold.

Table 6-2. Overvoltage Protection Level Selection

OVP Level	OVP Bit 1	OVP Bit 0
64V	0	0
50V	0	1
35V	1	0
28.5V	1	1

Table 6-3. CFG1-pin Settings

Level	OVP Bit 0	Clock Dithering Mode	I_{CL_latch}	$PGOOD_{OVP\_enable}$
1	0	enabled (DRSS)	disabled	disabled
2	1	enabled (DRSS)	disabled	disabled
3	0	enabled (DRSS)	disabled	enabled
4	1	enabled (DRSS)	disabled	enabled
5	0	enabled (DRSS)	enabled	disabled
6	1	enabled (DRSS)	enabled	disabled
7	0	enabled (DRSS)	enabled	enabled
8	1	enabled (DRSS)	enabled	enabled
9	0	disabled	disabled	disabled
10	1	disabled	disabled	disabled
11	0	disabled	disabled	enabled
12	1	disabled	disabled	enabled
13	0	disabled	enabled	disabled
14	1	disabled	enabled	disabled
15	0	disabled	enabled	enabled
16	1	disabled	enabled	enabled

The CFG2-pin defines the V_{OUT} overvoltage protection level and if the device uses the internal clock generator or an external clock applied at the SYNCIN-pin. During clock synchronization, the clock dither function is disabled.

OVP bit 1:	OVP bit 1 and 0 set the V_{OUT} overvoltage protection level. [00] = 64V, [01] = 50V, [10]= 35V or [11] = 28.5V.
Internal clock:	The device uses the internal clock.
External clock:	The device uses the internal clock and synchronizes to an external clock if applied.
SYNCIN:	Defines if the clock syncing function at the SYNCIN-pin is active (on) or disabled (off). The device is only syncing to an external clock applied to the SYNCIN-pin when SYNCIN is active.
Clock Dithering:	In case the internal oscillator is used the clock dithering is set according to the CFG1-pin setting Clock Dithering Mode. When external clock is selected the clock dithering function is disabled ignoring the CFG1-pin setting.

Table 6-4. CFG2-pin Settings

Level	OVP Bit 1	Clock	SYNCIN	Clock Dithering
1	0	Internal	off	CFG1-pin
2	1	Internal	off	CFG1-pin
3	0	Internal	off	CFG1-pin
4	1	External	on	disabled
≥5	0	External	on	disabled

6.3.2 Device and Phase Enable/Disable (UVLO/EN, EN2)

During shutdown the UVLO/EN-pin is pulled low by the internal resistor R_{EN}. When $V_{UVLO/EN}$ rises above $V_{EN\text{-}RISING}$, R_{EN} is disabled and the $I_{UVLO/EN}$ (typically 10µA) current source is enabled to provide the UVLO functionality. The device boots up, reads the configuration and enters STANDBY state (see Functional State Diagram). When $V_{UVLO/EN}$ rises above $V_{UVLO\text{-}RISING}$ the $I_{UVLO/EN}$ current source is disabled and the device enters START PHASE 1 and 2 state executing the soft-start ramping up V_{OUT} in DEM operation. A hysteresis $V_{EN\text{-}HYS}$ and $V_{UVLO\text{-}HYS}$ is implemented. Select the external UVLO resistor voltage divider (R_{UVLOT} and R_{UVLOB}) according to Equation 1 and Equation 2.

$$R_{UVLOT} = \frac{\left(V_{ON} - \frac{V_{UVLO-RISING}}{V_{UVLO-FALLING}} \times V_{OFF}\right)}{I_{UVLO-HYS}} \quad (1)$$

$$R_{UVLOB} = \frac{V_{UVLO-FALLING} \times R_{UVLOT}}{V_{OFF} - V_{UVLO-FALLING}} \quad (2)$$

A UVLO capacitor (C_{UVLO}) is required in case V_I drops below V_{OFF} momentarily during startup or a load transient at low V_I. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO-pin when $I_{UVLO-HYS}$ is disabled.

The 2nd phase is enabled when V_{EN2} rises above V_{EN2_H} and disabled when V_{EN2} falls below V_{EN2_L}. Enable and disable the 2nd phase at or before startup as well as during operation. The 2nd phase is 180° phase shifted towards phase 1 for lowest input and output ripple.

The UVLO/EN-pin voltage is not allowed to exceed the BIAS-pin voltage +0.3V (see Absolute Maximum Ratings) as the ESD-diode between UVLO/EN-pin and BIAS-pin gets conducting. However, a higher voltage up to 42V (Recommended Operating Conditions) is applicable at the UVLO/EN-pin when the current is limited to maximum 100µA with a series resistor.

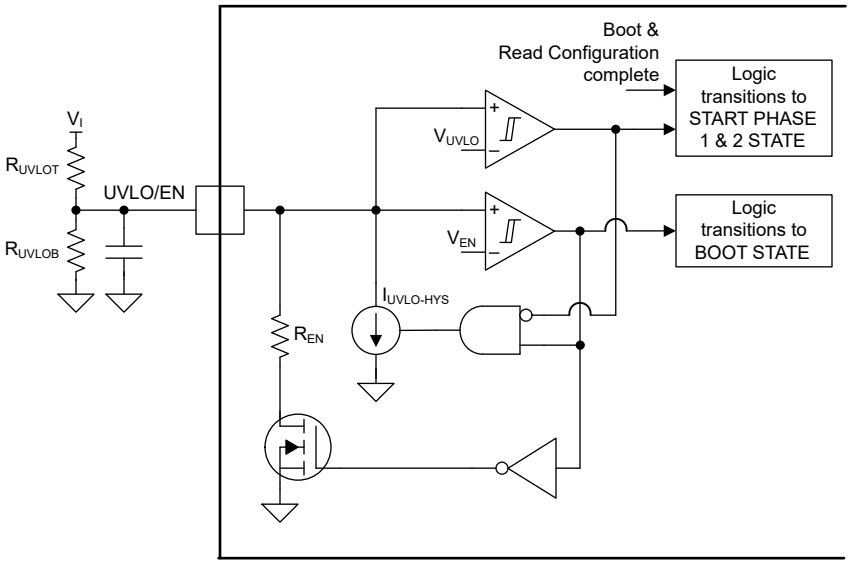


Figure 6-2. Functional Block Diagram UVLO and EN

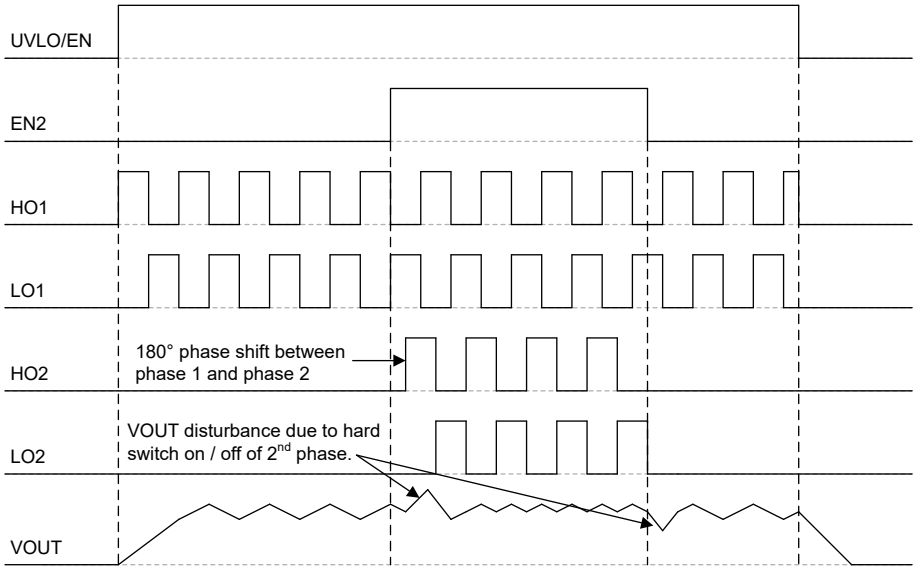


Figure 6-3. Dual-phase Operation

6.3.3 Switching Frequency and Synchronization (SYNCIN)

The switching frequency of 100kHz to 2.2MHz is set by the RT resistor connected between the RT-pin and AGND. The RT resistor is selected between 14kΩ and 316kΩ according to Equation 4. If configured to use an external clock the device uses the RT-pin to set the internal oscillator and synchronizes the switching frequency within ±50% to an external clock applied at the SYNCIN-pin. Set the external clock within the SYNCIN frequency activity detection range to be detected. The internal clock is synchronized at the rising edge of the external clock signal applied at the SYNCIN-pin. The CFG1-pin Spread Spectrum setting is ignored when external clock synchronization is selected, clock dithering is disabled.

The device always starts with the internal clock and starts synchronizing to an applied external clock during the START PHASE 1 and 2 and the ACTIVE state (see Functional State Diagram). The device synchronizes to the external clock as soon as the clock is applied and switches back to the internal clock in case the external clock stops.

$$f_{SW} = \frac{1}{\frac{R_{RT} \times s}{31.5\ G\Omega} + 18ns} \tag{3}$$

$$R_{RT} = \left(\frac{1}{f_{SW}} - 18ns\right) \times 31.5\frac{G\Omega}{s} \tag{4}$$

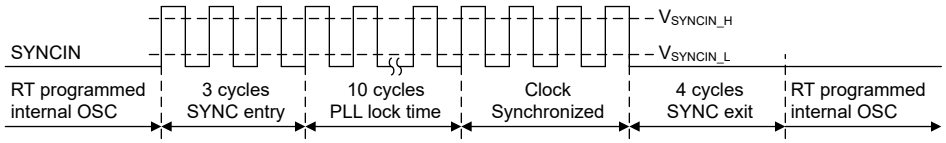


Figure 6-4. Clock Synchronization

6.3.4 Dual Random Spread Spectrum (DRSS)

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. Enable the spread spectrum by the CFG1-pin setting. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When the device is configured to use an external clock applied at the SYNCIN-pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example FM band).

In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

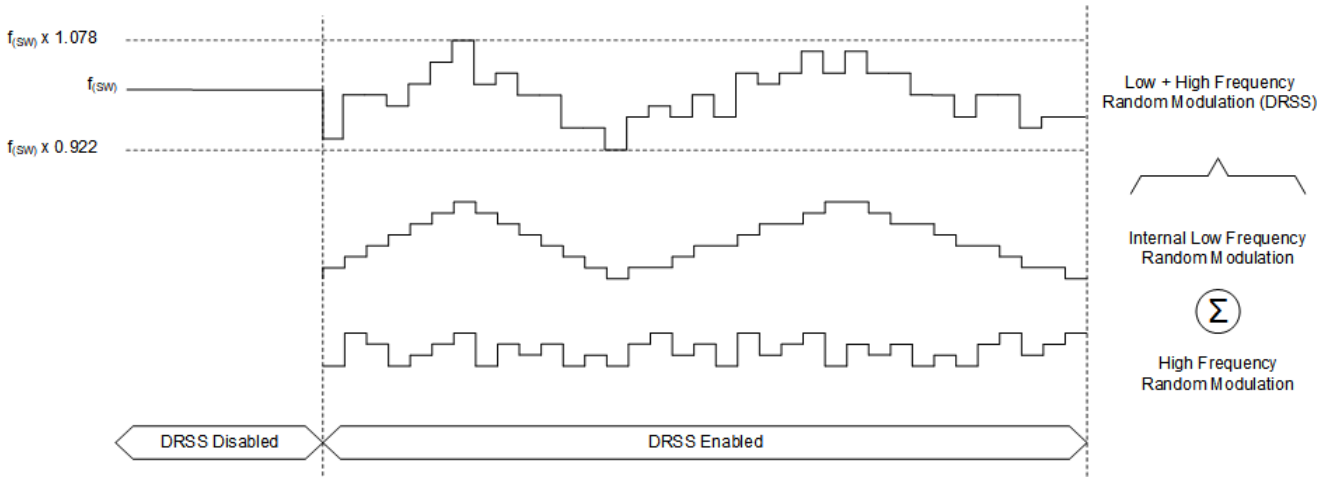


Figure 6-5. Dual Random Spread Spectrum

6.3.5 Operation Modes (BYPASS, DEM, FPWM)

The device supports bypass mode, forced PWM (FPWM) and diode emulation mode (DEM) operation. The mode can be changed on the fly and is set by the MODE-pin. Bypass mode is automatically activated for $V_{OUT} < V_I$. The device operation mode is set to DEM for $V_{MODE} < 0.4V$ and to FPWM for $V_{MODE} > 1.2V$.

Table 6-5. Mode-pin Settings

Operation Mode	MODE-pin
DEM	$V_{MODE} < 0.4V$
FPWM	$V_{MODE} > 1.2V$

In Diode Emulation Mode (DEM) current flow from V_{OUT} to V_I is prevented. The SW-pin voltage for each phase is monitored during the high-side on time and the high-side switch is turned off when the voltage falls below the zero current detection threshold V_{ZCD}. The device works in Discontinuous Conduction Mode (DCM) for light load and finally skips pulses, which improves light load efficiency. When both phases are active (EN2 = high), both phases work in DCM at light load and finally skip pulses. In DEM operation when COMP falls below typically 460mV the controller starts skipping pulses. Calculate the skip entry point for the input current with formula Equation 5 and for the output current with formula Equation 6.

$$I_{I\_skip} = \frac{1.5\mu \times \frac{V_I}{L}}{0.48 \times \frac{f_{SW}}{40K} + 250\mu \times R_{SNS} \times \frac{V_I}{L}} \quad (5)$$

$$I_{OUT\_skip} = \frac{\frac{V_I}{V_{OUT}} \times \frac{V_I}{L} \times 1.5\mu}{0.48 \times \frac{f_{SW}}{40K} + 250\mu \times R_{SNS} \times \frac{V_I}{L}} \quad (6)$$

In Forced Pulse With Modulation Mode (FPWM) the converter keeps switching also for light load with fixed frequency in continuous conduction mode (CCM). This mode improves light load transient response.

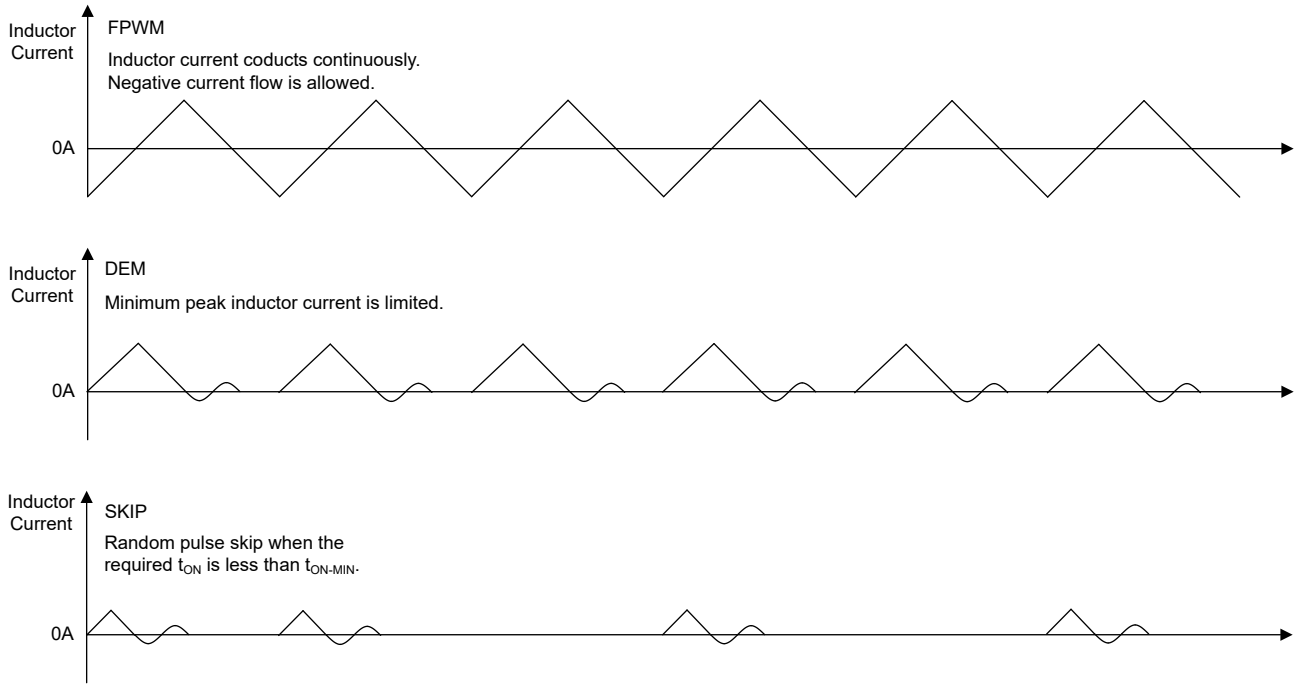


Figure 6-6. Inductor Current Waveform for the Different Operation Modes

In Bypass Mode (BYPASS) V_I is connected to V_{OUT} (no regulation) by turning on the high side FETs. Positive current flowing from V_I to V_{OUT} is not controlled while current flow from V_{OUT} to V_I is prevented for DEM setting and limited to V_{NCLTH} for FPWM setting. An integrated charge pump provides a minimum voltage of 3.75V at HOx − SWx and drives 55uA (I_{CP}) per phase. For EN2 = low only the high-side FET of phase 1 is turned on, for EN2 = high phase 1 and phase 2 high-side FETs are turned on. In case a MOSFET gate pull-down resistor is used, make sure the charge pump is able to drive the leakage current of the MOSFET and the pull-down resistor. The device starts switching in case the charge pump is overloaded to keep a minimum gate voltage of $V_{HB-UVLO}$.

The device enters and exits Bypass mode when the conditions in table Bypass Mode Entry, Exit are met.

Table 6-6. Bypass Mode Entry, Exit

Operation Mode	Bypass	Conditions
DEM / FPWM	Entry	$V_{OUT} < V_I - 100mV$ and $V_{COMP} < V_{COMP-MIN} + 100mV$
DEM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ or $((V_{CSP1} - V_{CSN1}) < V_{ZCD\_BYP} \| \| (V_{CSP2} - V_{CSN2}) < V_{ZCD\_BYP})$
FPWM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ or $((V_{CSP1} - V_{CSN1}) < V_{NCLTH} \| \| (V_{CSP2} - V_{CSN2}) < V_{NCLTH})$

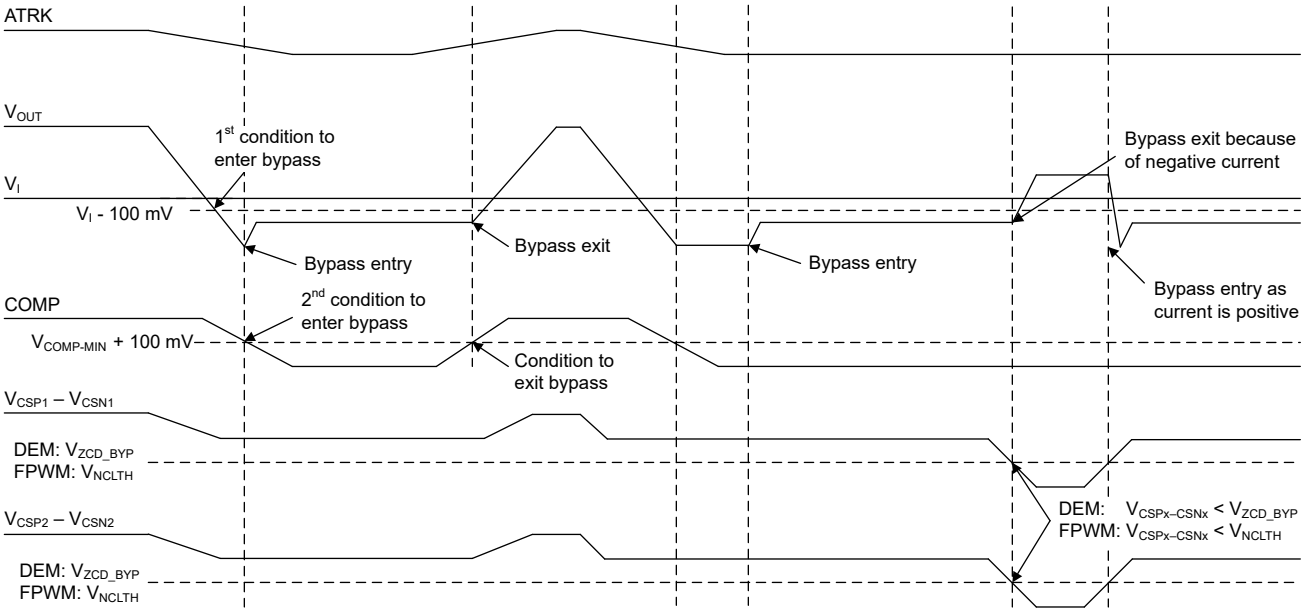


Figure 6-7. Bypass Mode Entry, Exit

6.3.6 VCC Regulator, BIAS (BIAS-pin, VCC-pin)

The gate drivers are powered by an internal 5V VCC regulator. The VCC regulator is sourced from the BIAS-pin supporting up to 42V for V_{BIAS} > $V_{BIAS-RISING}$ or the VOUT-pin for V_{BIAS} < $V_{BIAS-FALLING}$. Connect the BIAS-pin to a voltage ≥2.5V (for example V_I or 5V) as the reference system is permanently supplied by the BIAS-pin and shuts down for voltages <2V. The recommended VCC capacitor value is 10µF.

The integrated current limit prevents device damage when VCC is overloaded or the VCC-pin is shorted to ground. VCC sources up to 200mA (I_{VCC-CL}). Calculate the consumed VCC current of the external MOSFETs by Equation 7.

$$I_{VCC} = n \times 2 \times Q_{G@5V} \times f_{SW} \quad (7)$$

where

- n is the number of active phases.
- $Q_{G@5V}$ is the MOSFET gate charge at 5V gate-source voltage.

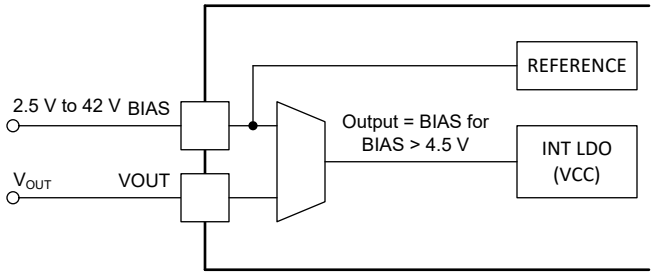


Figure 6-8. On the Fly BIAS Supply Selection

6.3.7 Soft Start (SS-pin)

At start-up during the START PHASE 1 and 2 state (see FSM) the device regulates the error amplifiers reference to the SS-pin voltage or the ATRK/DTRK-pin voltage, whichever is lower. The regulated reference results in a gradual rise of the output voltage V_{OUT}. During soft start the device forces diode emulation mode (DEM) until the soft start done signal is generated.

The external soft start capacitor is first discharged to the V_{SS-DIS} voltage, then charged by the I_{SS} current and the soft start done signal is generated when $V_{SS-DONE}$ is reached. In boost topology the soft start time (t_{SS}) varies with the input supply voltage as V_{OUT} is equal to V_I at startup. In figure Soft Start at the time t_1 the soft start current is activated. At t_2 the soft start voltage reached the V_I voltage level and V_{OUT} starts to rise until V_{OUT} reaches the programmed V_{OUT} value at t_3. The soft start done signal is generated at t_4 when the SS-pin voltage reaches $V_{SS-DONE}$. The SS-pin voltage continues to rise until V_{VCC} is reached where the soft start current is deactivated.

$$t_{SS\_t1\_t4} = 2.2 \times \frac{C_{SS}}{I_{SS}} \quad (8)$$

$$t_{SS\_t2\_t3} = \frac{C_{SS}}{I_{SS}} \times \frac{V_{OUT} - V_I}{30} \quad (9)$$

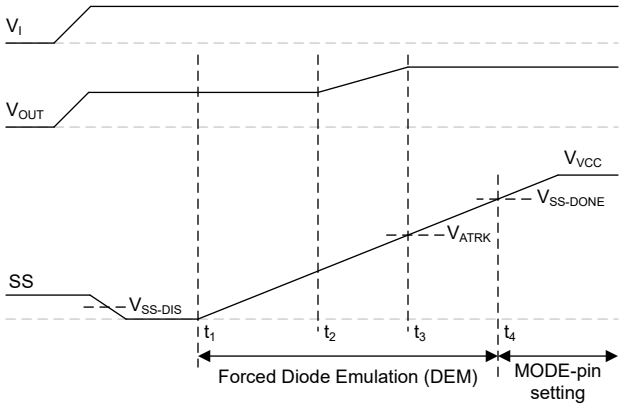


Figure 6-9. Soft Start

6.3.8 V_{OUT} Programming (VOUT, ATRK, DTRK)

The output voltage V_{OUT} is sensed at the VOUT-pin. Program V_{OUT} between 6V and 60V by connecting a 10kΩ to 100kΩ resistor at the ATRK/DTRK-pin, applying a voltage between 0.2V and 2V or a digital signal between 8% and 80% duty cycle. At startup during the STANDBY state (Functional State Diagram) the ATRK/DTRK-pin programming method analog signal or digital signal is detected. At the transition to the START PHASE 1 and 2 state the ATRK/DTRK-pin programming method is latched and is unchangeable during operation. Allow a DTRK signal to be present for at least three cycles so that it is detected before the programming method is latched. ATRK supports up to 10kHz signals, however, change the ATRK-pin voltage or the DTRK duty cycle slow enough that V_{OUT} is able to follow. In case the ATRK/DTRK-pin set reference voltage is changed faster than the bandwidth of the converter, the inductor current exceeds peak current limit until the slope compensation settles. The inductor peak current overshoot is limited to 90mV CSPx − CSNx sense resistor voltage. The device tries to regulate V_{OUT} as well for ATRK < 0.2V or >2V, but performance is not endured. Enable the 20µA current by CFG0 setting for V_{OUT} programming by resistor. The 20µA current is sourced through the ATRK-pin and generates the required ATRK voltage for the target VOUT voltage via the external resistor. For analog tracking (ATRK) or digital tracking (DTRK), TI recommends disabling the 20uA current.

Equation for programming V_{OUT} by resistor:

$$R_{ATRK} = \frac{V_{OUT}}{6\,V} \times 10\,k\Omega \quad (10)$$

Equation for programming V_{OUT} by voltage (ATRK):

$$V_{OUT} = V_{ATRK} \times 30 \quad (11)$$

Equation for programming V_{OUT} by digital signal (DTRK):

$$V_{OUT} = 0.75 \frac{V}{\%} \times Duty\ Cycle \quad (12)$$

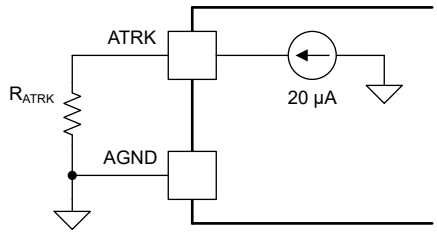


Figure 6-10. V_{OUT} Programming by Resistor

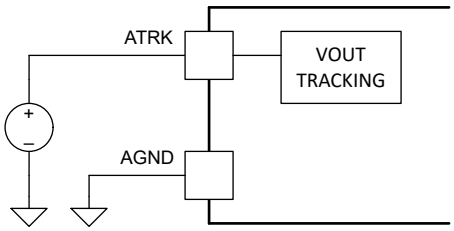


Figure 6-11. V_{OUT} Tracking by Analog Voltage

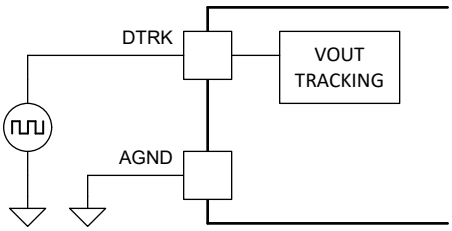


Figure 6-12. V_{OUT} Tracking by Digital Signal

6.3.9 Protections

The device has the following protections implemented. Figure 6-13 shows in which state of the Functional State Diagram which protection is active. The protection is active for the grey shaded states having the same grey shading, for example TSD is active in STANDBY state including THERMAL SHUTDOWN state but not in ICL LATCH state.

- Thermal shutdown (TSD) turning off the device at high temperature.
- Undervoltage Lockout (UVLO) turning off the device at low supply voltage.
- VCC Undervoltage Lockout (VCC UVLO) avoiding too low low-side gate driver voltage. The device stops switching until VCC is recovered.
- HBx Undervoltage Lockout (HBx UVLO) avoiding too low high-side gate driver voltage. The device initiates refresh pulses (512 cycles hiccup mode off time). See MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LOx, HOx, HBx-pin) for details.
- Overvoltage Protection (OVP), when triggered the device stops switching until V_{OUT} is back on target. There are two OVPs implemented:
  - OVP_{max}, which is a programmable absolute value (typically 64V, 50V, 35V or 28.5V).
  - OVP, which triggers when V_{OUT} is 110% of the programmed value.
- Undervoltage Protection (UVP), when triggered the device continues operation but pulls the PGOOD-pin low.
- Peak Current Limit (PCL), limiting the switch peak current. See Current Sense Setting and Switch Peak Current Limit (CSP1, CSP2, CSN1, CSN2) for details.
- Input Current Limit (ICL), limiting the switch peak current to 120% of the peak current limit. This protection is enabled and disabled by I_{CL_latch} programming.
- Average Input Current Limit (ILIM), limiting the average input current to the programmed value by R_{ILIM}. See Input Current Limit and Monitoring (ILIM, IMON, DLY) for details.

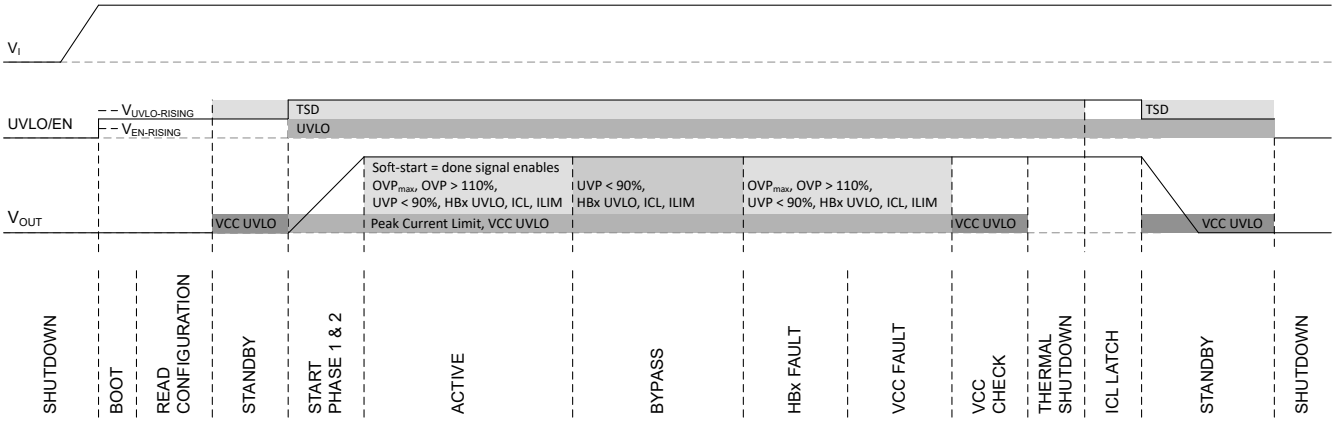


Figure 6-13. Protections

6.3.9.1 V_{OUT} Overvoltage Protection (OVP)

The Overvoltage Protection (OVP) monitors the VOUT-pin using two thresholds. The programmable threshold V_{OVP_max-H} limiting V_{OUT} to 64V, 50V, 35V or 28.5V, and the V_{OVP-H} threshold limiting the programmed V_{OUT} to 110% of the programmed voltage. In BYPASS state the 110% $_{OVP-H}$ detection is disabled, but the V_{OVP_max-H} is active.

When V_{OUT} rises above the V_{OVP_max-H} or the V_{OVP-H} threshold (not active during Bypass), the low-side driver is turned off and the high-side driver is turned on. Current flow from V_I to V_{OUT} is monitored through CSP1 - CSN1 and when phase 2 is active also through CSP2 - CSN2 allowing current flow from V_I to V_{OUT}. The high-side driver is turned off when the current from V_I to V_{OUT} is zero or negative preventing current flow from V_{OUT} to V_I. When V_{OUT} falls below the V_{OVP_max-L} or V_{OVP-L} threshold the device continues normal operation.

6.3.9.2 Thermal Shutdown (TSD)

An internal thermal shutdown (TSD) protects the device by disabling the MOSFET drivers and VCC regulator if the junction temperature (T_J) exceeds the $T_{TSD-RISING}$ threshold. After the junction temperature (T_J) is reduced by the $T_{TSD-HYS}$ hysteresis, the device continues operation according to the Functional State Diagram.

6.3.10 Power-Good Indicator (PGOOD-pin)

The device provides a power-good indicator (PGOOD) to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor can be externally connected. The PGOOD switch opens when the VOUT pin voltage is higher than the V_{UVP-H} undervoltage threshold. PGOOD is pulled low under the following conditions:

- The VOUT-pin voltage is below the V_{OUT} falling undervoltage threshold V_{UVP-L}.
- The VOUT-pin voltage is above the 110% V_{OVP_H} or the programmed V_{OVP_max-H} rising threshold and the $PGOOD_{OVP\_enable}$ function is enabled (see CFG1-pin Settings). PGOOD is not pulled low for an OVP event when the $PGOOD_{OVP\_enable}$ function is disabled.
- The device is in SHUTDOWN state and V_{BIAS} is greater than approximately 1.7V (see Functional State Diagram).
- The EN/UVLO-pin voltage is falling below the undervoltage lockout threshold voltage $V_{UVLO-FALLING}$.
- The VCC regulator voltage VCC falls below the undervoltage lockout threshold $V_{VCC-UVLO-FALLING}$.
- Thermal Shutdown is triggered (see Functional State Diagram).
- The HBx-pin voltage is below the V_{HBx} falling $V_{HB-UVLO}$ threshold and boot refresh enters the 512 cycles hiccup mode off time (see MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LOx, HOx, HBx-pin)). PGOOD is only pulled low during the Hiccup off-time.
- The switch peak current limit is exceeded by 20% and the I_{CL_latch} function is enabled (see CFG1-pin Settings).
- An OTP memory fault occurred (CRC fault).

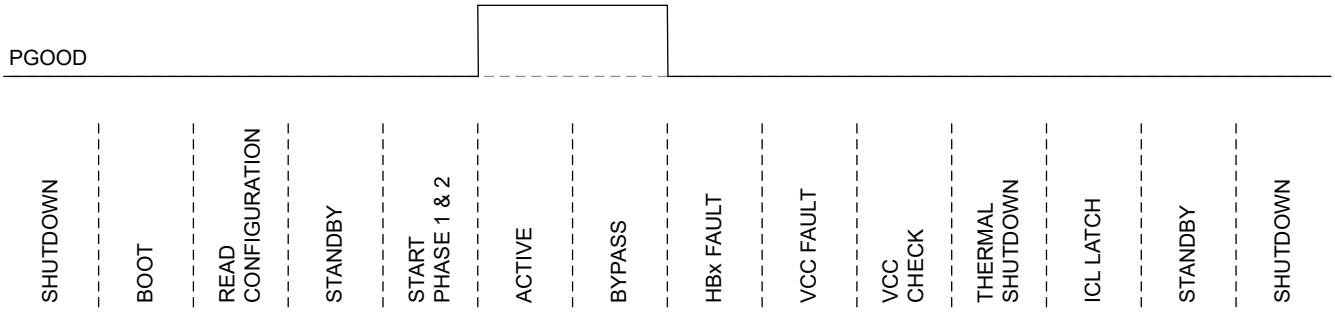


Figure 6-14. PGOOD status for all device states

6.3.11 Slope Compensation (CSP1, CSP2, CSN1, CSN2)

The current sense amplifier has a gain of 10 (ACS) and an internal slope compensation ramp is added to prevent subharmonic oscillation at high duty cycles. The slope of the compensation ramp must be greater than at least half of the sensed inductor current falling slope, which is fulfilled when Margin in Equation 13 is >1.

$$\frac{V_{OUT} - V_I}{2 \times L} \times R_{SNS} \times Margin < V_{SLOPE} \times f_{SW} \quad (13)$$

6.3.12 Current Sense Setting and Switch Peak Current Limit (CSP1, CSP2, CSN1, CSN2)

The peak current limit for each phase is set by the sense resistors R_{SNS1} and R_{SNS2}. The positive peak current limit for phase 1 is active when CSP1 − CSN1 reaches the threshold V_{CLTH} (typical 60mV), for phase 2 when CSP2 − CSN2 reaches the threshold. The negative peak current limit is active when V_{NCLTH} (typical −28mV) is reached. R_1, R_2, R_4, R_5 in Figure 6-15 are 0Ω and R_3, R_6 are open.

$$R_{SNS} = \frac{I_{peak\_lim}}{V_{CLTH}} \quad (14)$$

Adjust the peak current limit by adding the resistors R_1, R_2, R_3, R_4, R_5 and R_6. Resistors R_1, R_2, R_4 and R_5 need to have the same value. Select the resistors <1Ω because the CSx amplifiers are supplied by the CSPx pins. Select R_3 and R_6 between 1Ω and 20Ω. The negative current limit for FPWM mode is adjusted accordingly.

$$I_{peak\_lim\_ph1} = \left(\frac{R_1 + R_2}{R_3} + 1\right) \times \frac{V_{CLTH}}{R_{SNS1}} \quad (15)$$

$$I_{peak\_lim\_ph2} = \left(\frac{R_4 + R_5}{R_6} + 1\right) \times \frac{V_{CLTH}}{R_{SNS2}} \quad (16)$$

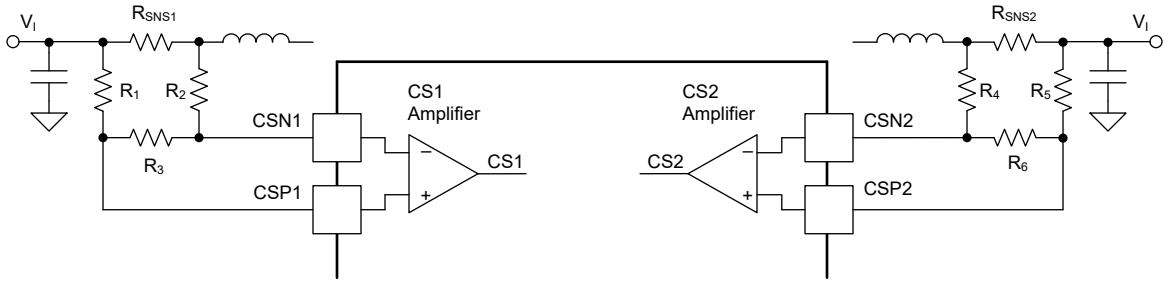


Figure 6-15. Peak Limit Adjustment Through Additional Resistors

The negative peak current limit of typically −28mV is an additional safety protection and usually not reached as the negative current is already limited by the COMP-pin voltage. V_{COMP} is clamped at typically 200mV, which limits the switch current at around −20mV sense voltage.

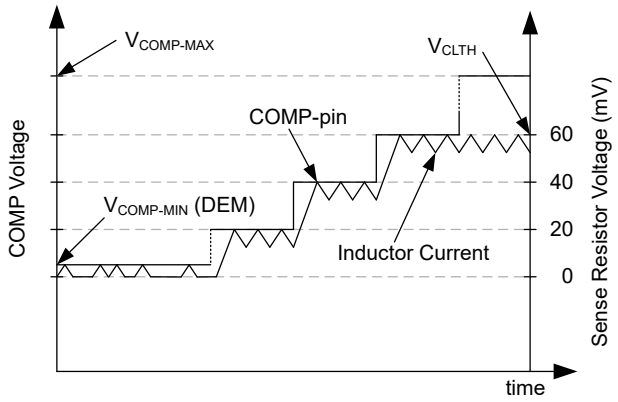


Figure 6-16. COMP-pin and Sense Resistor Voltage Limiting the Switch Current (DEM)

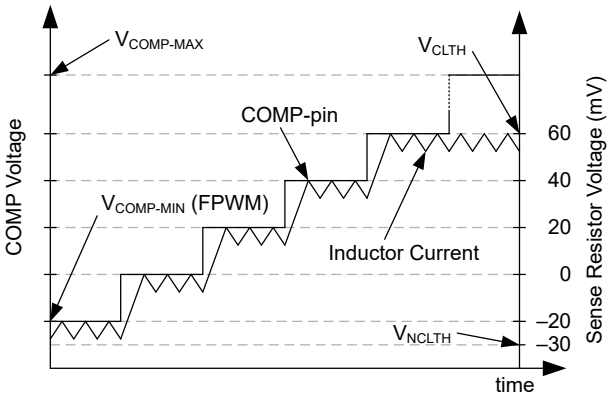


Figure 6-17. COMP-pin and Sense Resistor Voltage Limiting the Switch Current (FPWM)

6.3.13 Input Current Limit and Monitoring (ILIM, IMON, DLY)

Monitor the average V_I input current at the IMON-pin. The average sensed current of each active phase is summed up generating a source current at the IMON-pin, which is converted to a voltage by the resistor R_{IMON}. The resulting voltage V_{IMON} is calculated according to Equation 18, the required resistor R_{IMON} according to Equation 17. V_{IMON} regulates up to 3V and is self-protecting not reaching the absolute maximum value.

$$R_{IMON} = \frac{V_{IMON}}{(R_{CS1} + R_{CS2}) \times n \times I_{IN} \times G_{IMON} + n \times I_{OFFSET}} \quad (17)$$

$$V_{IMON} = ((R_{CS1} + R_{CS2}) \times n \times I_{IN} \times G_{IMON} + n \times I_{OFFSET}) \times R_{IMON} \quad (18)$$

R_{CS1} and R_{CS2} are the respective phase sense resistors. For a disabled phase use 0Ω as sense resistor value. I_{IN} is the input current, G_{IMON} the transconductance gain, n the number of active phases and I_{OFFSET} the offset current given in the electrical characteristics table.

Limit the average input current by choosing an appropriate resistor connected to the ILIM-pin. When the input current limit is active, V_{OUT} is regulated down until the set average input current limit is reached. In case V_{OUT} is regulated below the V_I voltage the current is unlimited. The DLY-pin capacitor C_{DLY} adds an additional delay time t_{DLY} to activate and deactivate the average input current limit (see Figure 6-18). When the ILIM-pin voltage reaches the threshold V_{ILIM} (typical 1V) the source current I_{DLY} is activated charging up the DLY-pin capacitor C_{DLY}. The DLY-pin voltage V_{DLY} rises until $V_{DLY\_peak\_rise}$ is reached, which activates the average input current limit. The ILIM-pin voltage is regulated to V_{ILIM} and the input current is regulated down to the average input current limit set by R_{ILIM} resulting in a V_{OUT} drop. To exit the average current limit regulation the output load has to decrease, which causes V_{OUT} to rise and V_{ILIM} to fall below V_{ILIM_reset} (typical 0.88V). V_{ILIM_reset} activates the sink current I_{DLY}, which discharges the DLY-pin capacitor C_{DLY}. When V_{DLY} reaches $V_{DLY\_peak\_fall}$ the average input current limit is deactivated and the DLY-pin is discharged to V_{DLY_valley}. The required resistor R_{ILIM} is calculated according to Equation 19.

$$R_{ILIM} = \frac{1V}{(R_{CS1} + R_{CS2}) \times n \times I_{IN\_LIM} \times G_{IMON} + n \times I_{OFFSET}} \quad (19)$$

$$t_{DLY} = \frac{2.6 \times C_{DLY}}{5 \times 10^{-6}} \quad (20)$$

$$C_{DLY} = t_{DLY} \times \frac{5 \times 10^{-6}}{2.6} \quad (21)$$

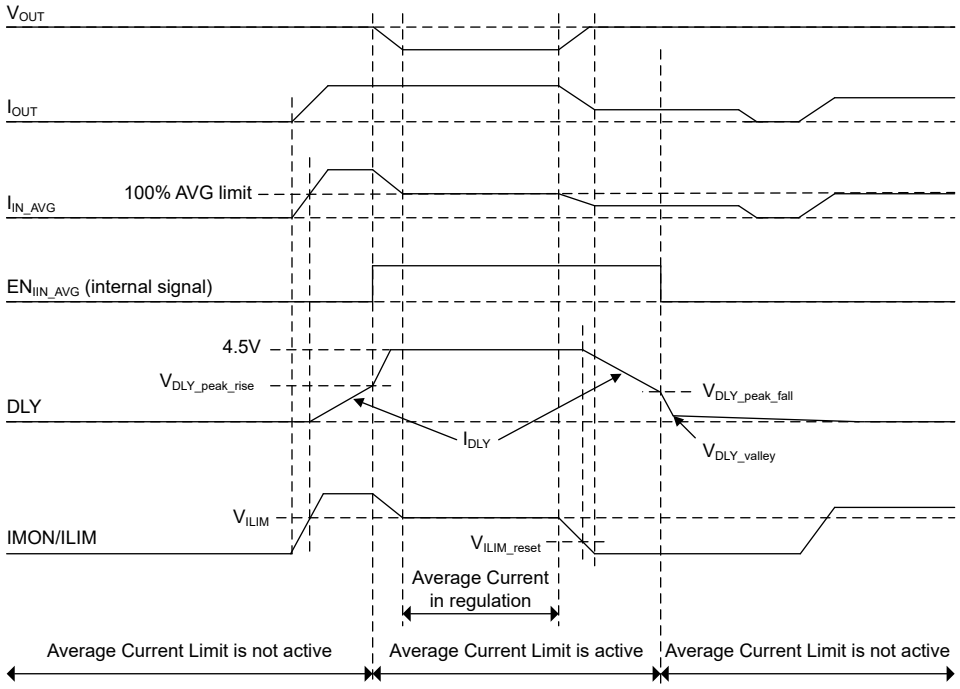


Figure 6-18. Average Current Limit

While a constant delay is added by the DLY-pin capacitor a V_{OUT} load dependent delay can be added by adding a RC tank to the ILIM/IMON-pin in parallel to the R_{ILIM} resistor. The RC tank resistor R_{C_IMON} is calculated according to Equation 22 and the capacitor C_{IMON} according to Equation 23.

$$R_{C\_IMON} = \frac{1}{20\pi \times C_{IMON}} \tag{22}$$

$$C_{IMON} = \frac{t_{delay}}{R_{IMON} \times \ln\left(\frac{R_{IMON} \times I_{MON} - V_{IMON\_0A}}{R_{IMON} \times I_{MON} - V_{ILIM}}\right)} \tag{23}$$

6.3.14 Maximum Duty Cycle and Minimum Controllable On-time Limits

To cover the non-ideal factors caused by resistive elements, a maximum duty cycle limit D_{MAX} and a minimum forced off-time is implemented. In CCM operation the minimum supported input voltage V_{I_MIN} for a programmed output voltage V_{OUT} is defined by the maximum duty cycle D_{MAX} (see Equation 24). In DEM operation the minimum input voltage V_{I_MIN} is not limited by D_{MAX}.

$$V_{I\_MIN} \approx V_{OUT} \times (1 - D_{MAX}) + I_{I\_MAX} \times (R_{DCR} + R_{SNS} + R_{DS(ON)}) \tag{24}$$

where

- I_{I_MAX} is the maximum input current at minimum input voltage V_{I_MIN}
- R_{DCR} is the DC resistance of the inductor
- R_{SNS} is the resistance of the sense resistor
- $R_{DS(ON)}$ is the on resistance of the MOSFET

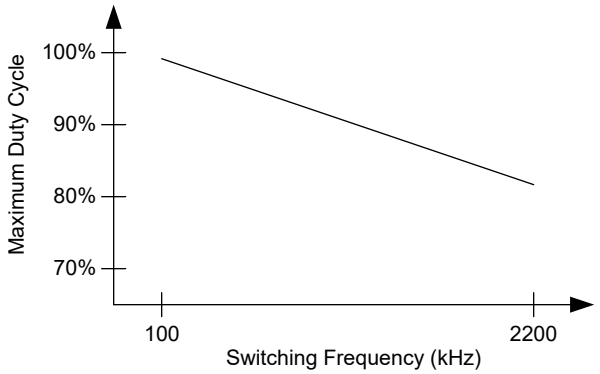


Figure 6-19. Switching Frequency vs Maximum Duty Cycle

At very light load condition or when V_I is close to V_{OUT} the device skips the low-side driver pulses if the required on-time is less than t_{ON-MIN} to avoid V_{OUT} runaway. This pulse skipping appears as a random behavior. If V_I is further increased to the voltage higher than V_{OUT}, the required on-time becomes zero and eventually the device enters bypass operation which turns on the high-side driver 100%.

6.3.15 Signal Deglitch Overview

The following image shows the signal deglitching. For all signals, the rising and falling edge is deglitched with the same deglitch time.

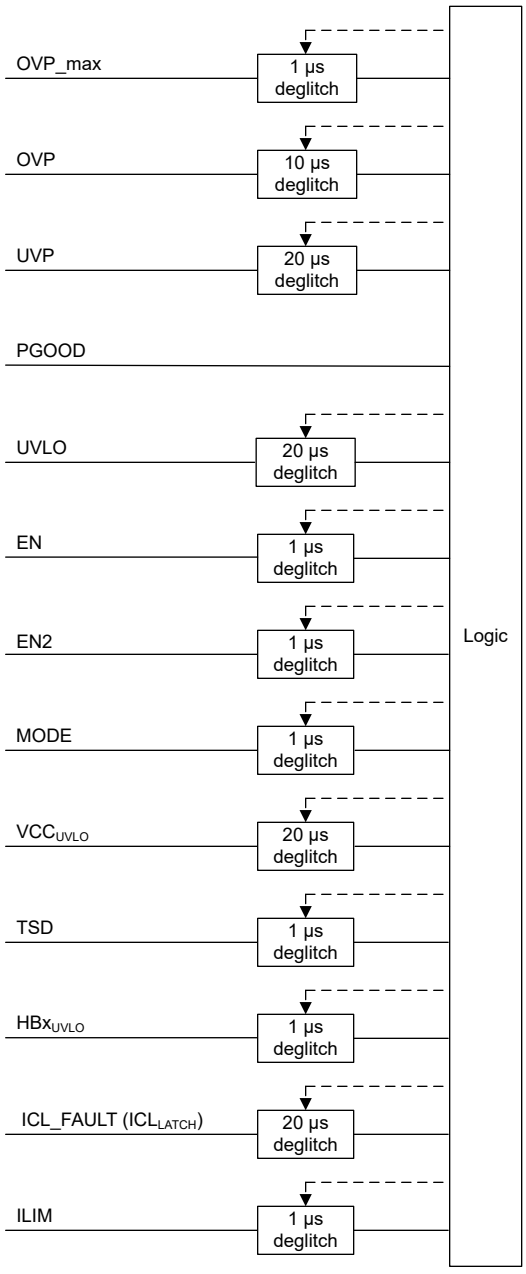


Figure 6-20. Signal Deglitching

6.3.16 MOSFET Drivers, Integrated Boot Diode, and Hiccup Mode Fault Protection (LOx, HOx, HBx-pin)

The device integrates N-channel logic MOSFET drivers. The LOx driver is powered by VCC and the HOx driver is powered by HBx. When the SWx-pin voltage is approximately 0V by turning on the low-side MOSFET, the capacitor C_{HBx} is charged from VCC through the internal boot diode. The recommended value of C_{HBx} is 0.1µF. During shutdown, the gate drivers outputs are high impedance.

The LOx and HOx outputs are controlled with an adaptive dead-time methodology, which makes sure that both outputs are not turned on at the same time to prevent shoot through. When the device turns on LOx the adaptive dead-time logic turns off HOx and waits for the HOx − SWx voltage to drop below typically 1.5V, then LOx is turned on after a small programmable dead-time delay t_{DHL}. Also the HOx driver turn-on is delayed until the LOx − PGND voltage has discharged below typically 1.5V. HOx is then turned on after the same programmable dead-time delay t_{DLH}.

If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter does not start up properly and becomes stuck at the maximum duty cycle in a high-power dissipation state. Avoid this condition by selecting a lower threshold MOSFET or by turning on the device when the BIAS-pin voltage is sufficient. During bypass operation the minimum HOx − SWx voltage is 3.75V.

The hiccup mode fault protection is triggered by $V_{HB-UVLO}$. If the HBx − SWx voltage is less than the HBx UVLO threshold ($V_{HB-UVLO}$), LOx turns on by force for 75ns to replenish the boost capacitor. The device allows up to four consecutive replenish switching cycles. After the maximum four consecutive boot replenish switching cycles, the device skips switching for 12 cycles. If the device fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching cycles, the device stops switching and enters 512 cycles of hiccup mode off-time. During the hiccup mode off-time PGOOD = low and the SS-pin is grounded.

If required adjust the slew rate of the switching node voltage by adding a gate resistor in parallel with pull-down PNP transistor. The resistor decreases the effective dead-time.

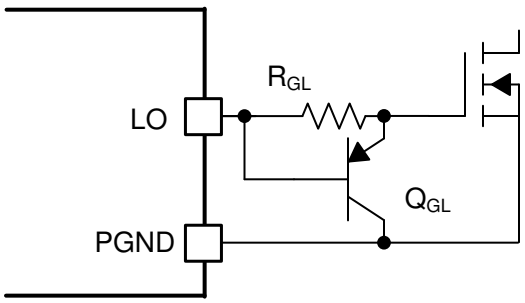


Figure 6-21. Slew Rate Control

6.4 Device Functional Modes

The different operation modes are shown in the Functional State Diagram (FSM).

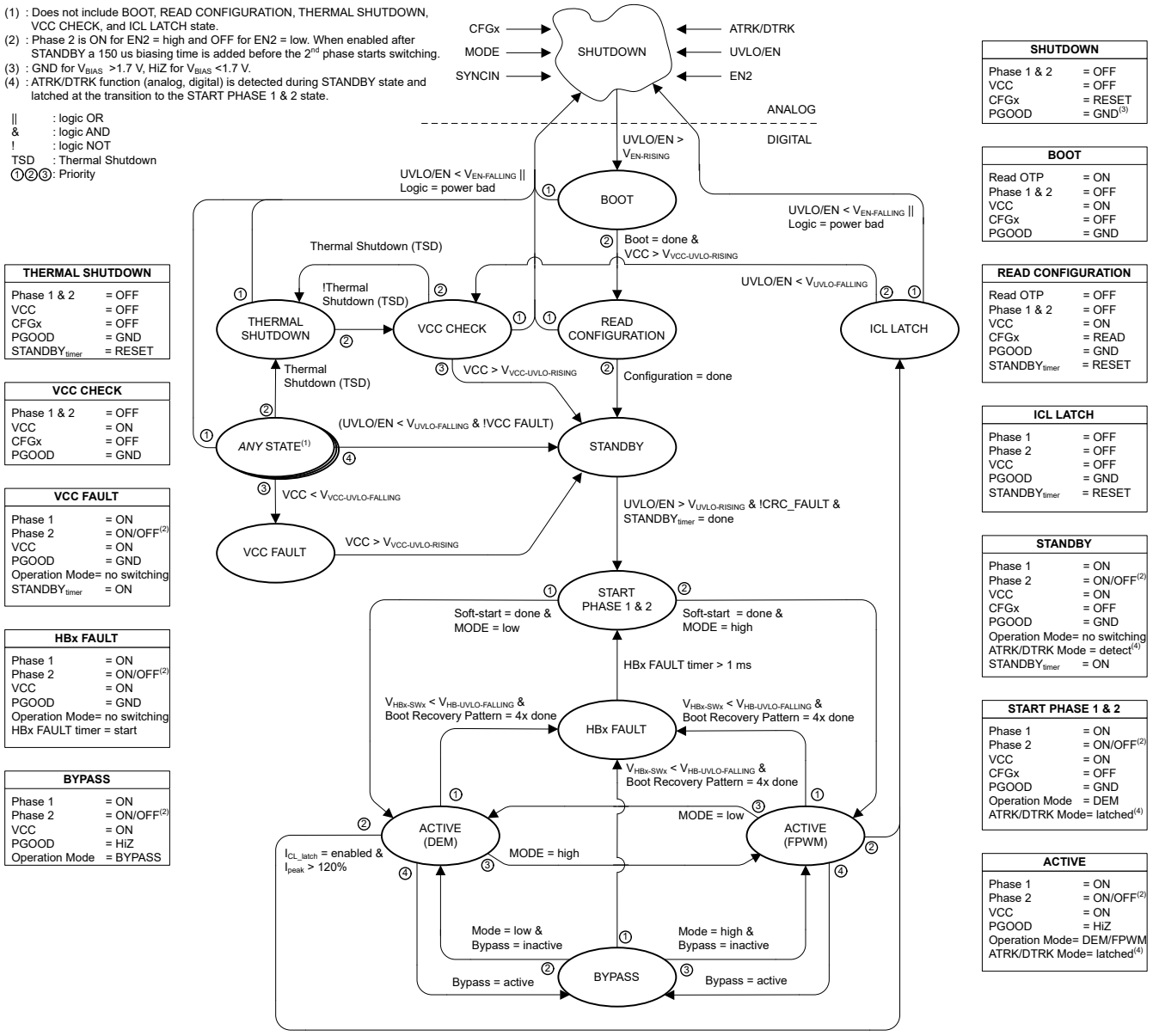


Figure 6-22. Functional State Diagram

6.4.1 Shutdown State

The device shuts down for UVLO/EN pin = low consuming typically 2µA from the BIAS-pin and 0.001µA from the VOUT-pin. In shutdown, COMP, SS, and PGOOD are grounded. The VCC regulator is disabled.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

is a dual-phase interleaved boost converter. Use the following design procedure to select component values for .

Refer to LM5125 evaluation module for a typical application and curves.

Use the LM5125 Quick Start Calculator to expedite designing a regulator for a given application.

Alternatively, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

This section presents a simplified discussion of the design process.

7.1.1 Feedback Compensation

The open-loop response of a boost regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator includes a power stage transfer function with an embedded current loop. The transfer function is simplified as one pole, one zero, and one right-half-plane zero (RHPZ) system.

The modulator transfer function is defined as follows:

$$\frac{\hat{v}_{out}}{\hat{v}_{comp}} = A_M \times \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{P\_LF}}} \times F_{ACB}\left(s\right) \quad (25)$$

where

- Modulator DC gain, $A_M = \frac{R_{out} \times D'}{2 \times A_{cs} \times R_{cs\_eq}}$
- Load pole, $\omega_{P\_LF} = \frac{2}{R_{out} \times C_{out}}$
- ESR zero, $\omega_{Z\_ESR} = \frac{1}{R_{ESR} \times C_{out}}$
- RHPZ, $\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m\_eq}}$
- The equivalent load resistance, $R_{out} = \frac{V_{out}^2}{P_{out\_total}}$
- The equivalent inductance, $L_{m\_eq} = \frac{L_m}{N_p}$
- The equivalent current sense resistor, $R_{cs\_eq} = \frac{R_{cs}}{N_p}$
- N_p is the number of the phases.
- Active current balancing circuit transfer function, $F_{ACB}(s) = \frac{1}{2} \times \frac{s \times 4 \times 10^{-6} + 1}{s \times 2 \times 10^{-6} + 1}$. An active current balancing circuit is employed in LM5125-Q1 to reduce the average current error caused by the difference of the two inductors.

If the equivalent series resistance (ESR) of C_{out} (R_{ESR}) is small enough and the RHPZ frequency is far away from the target crossover frequency, the modulator transfer function is further simplified to a one pole system and the voltage loop is closed with only two loop compensation components, R_{COMP} and C_{COMP}, leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

As shown in Figure 7-1, a g_m amplifier is utilized as the output voltage error amplifier. The feedback transfer function includes the feedback resistor divider gain and loop compensation of the error amplifier. R_{COMP}, C_{COMP}, and C_{HF} configure the error amplifier gain and phase characteristics, create a pole at origin, a low frequency zero and a high frequency pole.

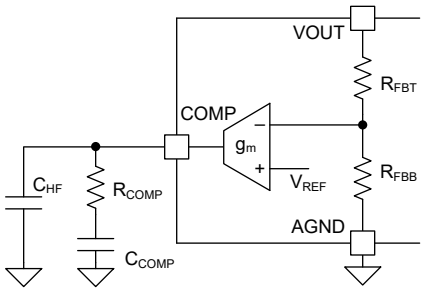


Figure 7-1. Type II g_m Amplifier Compensation

Feedback transfer function is defined as follows:

$$-\frac{\hat{v}_{comp}}{\hat{v}_{out}} = \frac{A_{VM} \times \omega_{Z\_EA}}{s} \times \frac{1 + \frac{s}{\omega_{Z\_EA}}}{1 + \frac{s}{\omega_{P\_EA}}} \quad (26)$$

where

- The middle-band voltage gain, $A_{VM} = K_{FB} \times g_m \times R_{COMP}$
- g_m = 1mA/V.
- The feedback resistor divider gain $K_{FB} = \frac{R_{FBB}}{R_{FBT} + R_{FBB}}$. $K_{FB} = \frac{1}{30}$ for the internal feedback resistor divider.
- Low frequency zero, $\omega_{Z\_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$
- High frequency pole, $\omega_{P\_EA} \approx \frac{1}{R_{COMP} \times C_{HF}}$

The pole at the origin minimizes the output steady state error. Place the low frequency zero to cancel the load pole of the modulator. Use the high frequency pole to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost is achieved at the crossover frequency. Place the high frequency pole beyond the crossover frequency because the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is usually limited to one fifth of the RHPZ frequency.

Increase R_{COMP} and proportionally decreasing C_{COMP} for higher crossover frequency. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

7.1.2 Non-synchronous Application

Please follow below instructions when operating in nonsynchronous mode. Check also the application note Asynchronous Operation of LM5125x Boost Controller.

- Connect SWx to GND and HBx to VCC.

- Keep HOx floating.

The diagram is shown below.

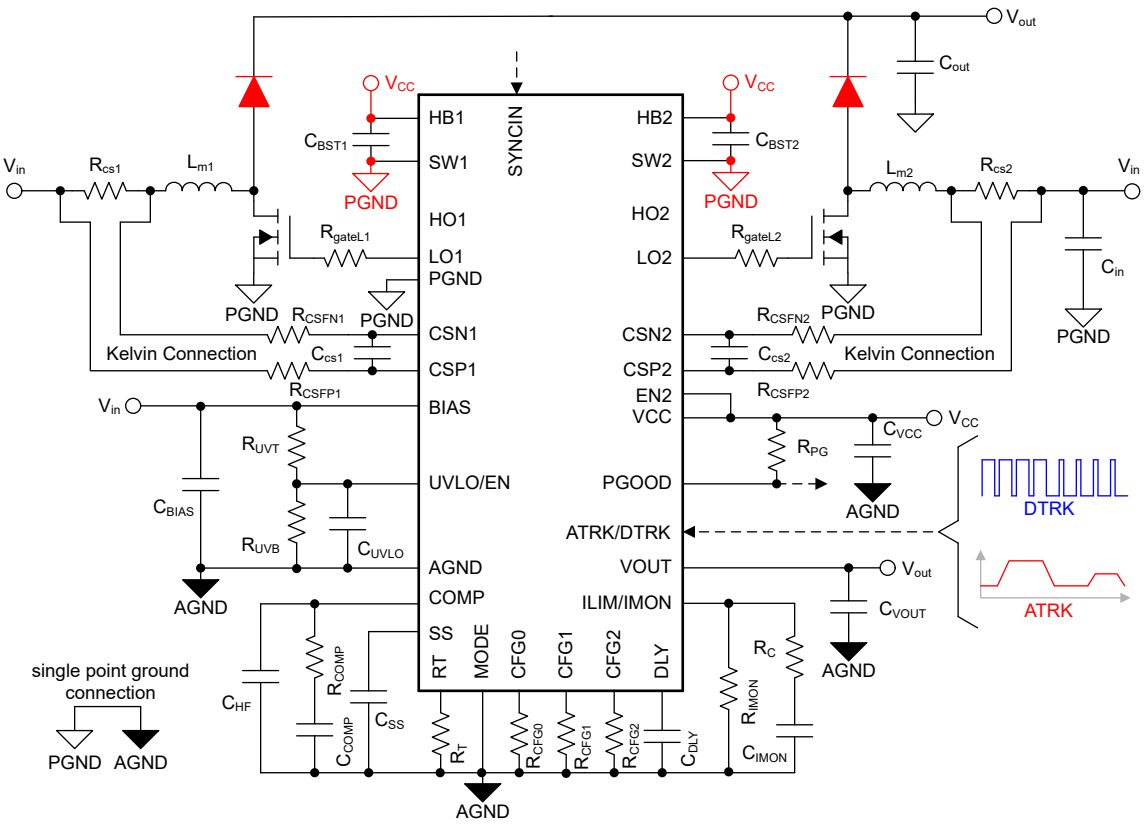


Figure 7-2. Schematic of a Dual-phase Non-synchronous Boost Converter

7.2 Typical Application

A typical application example is a dual-phase boost converter as shown below. This converter is designed for Class-H audio amplifier. The output voltage is adjustable up to 45V. The peak power is 1kVA with an input average current limit of 26A.

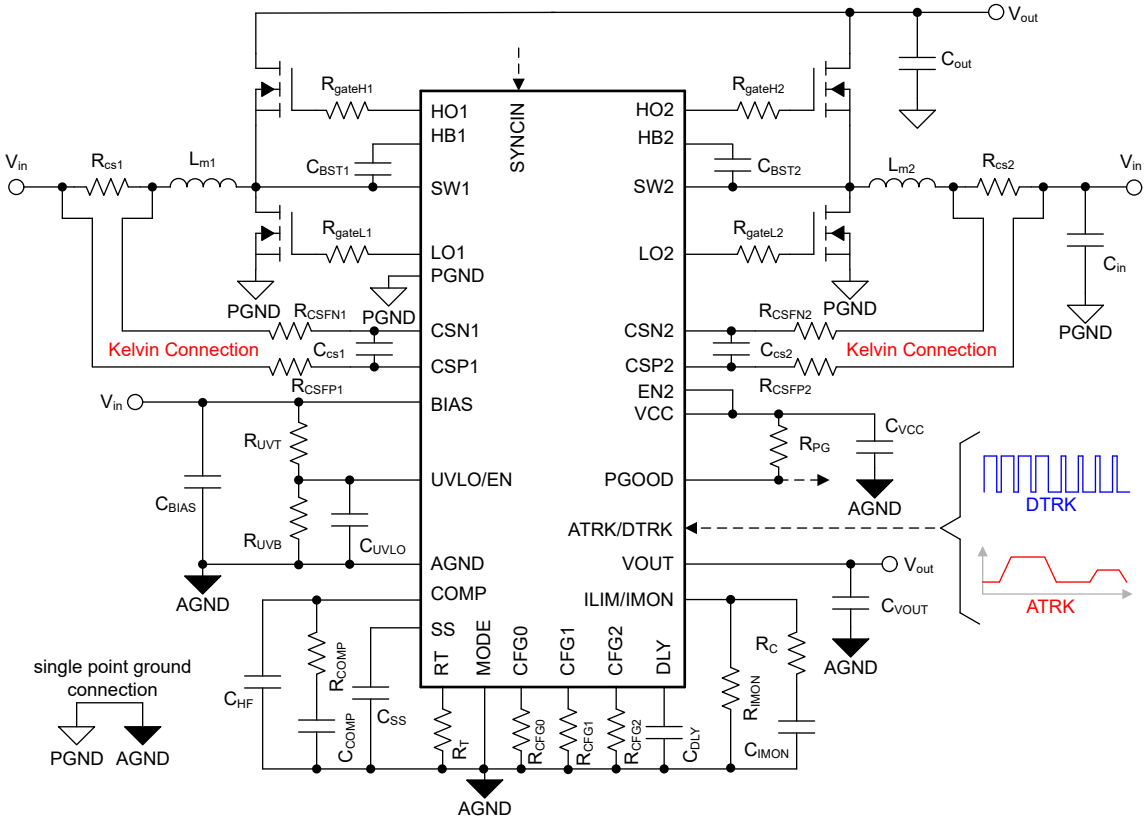


Figure 7-3. Schematic of a Dual-phase Boost Converter

7.2.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Minimum input voltage, V_{in_min}	9V
Typical input voltage, V_{in_typ}	14.4V
Maximum input voltage, V_{in_max}	18V
Minimum output voltage, V_{out_min}	8V
Maximum output voltage, V_{out_max}	45V
Maximum output power at maximum output voltage and typical input voltage, P_{out_total}	1000W
Rated output power, P_{rated_total}	300W
Maximum delay at twice rated output power and typical input voltage, t_{delay}	100ms
Estimated efficiency, η	95%

7.2.2 Detailed Design Procedure

7.2.2.1 Determine the Total Phase Number

Interleaved operation offers many advantages in high current applications such as higher efficiency, lower component stresses and reduced input and output ripple. For dual phase interleaved operation, the output

power path is split reducing the input current in each phase by one-half. Ripple currents in the input and output capacitors are reduced significantly since each channel operates 180 degrees out of phase from the other. As shown in Figure 7-4, the input current ripple is reduced significantly.

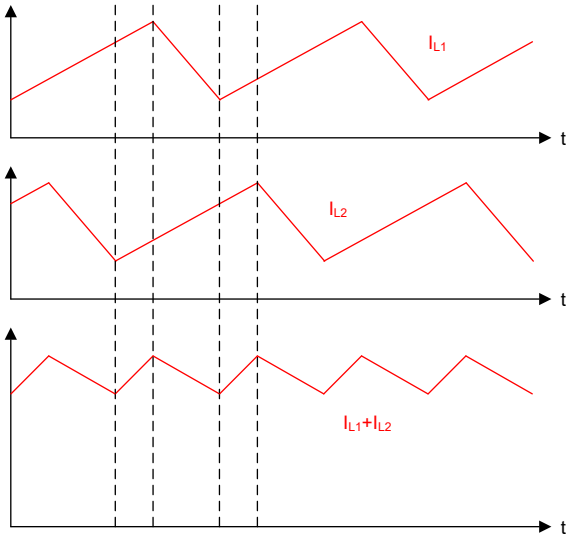


Figure 7-4. Input Current Ripple Reduced With Dual Phase Interleaving

Here, 2 phase is selected for the design:

$$N_p = 2 \tag{27}$$

The total power P_{out_total} is shared among phases, the power of each phase is found as:

$$P_{out} = \frac{P_{out\_total}}{N_p} = 500W \tag{28}$$

7.2.2.2 Determining the Duty Cycle

In CCM, The duty cycle is defined as:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \tag{29}$$

$$D' = 1 - D \tag{30}$$

In this application, the maximum duty cycle is found as:

$$D_{max} = \frac{V_{out\_max} - V_{in\_min}}{V_{out\_max}} = 0.8 \tag{31}$$

7.2.2.3 Timing Resistor R_T

Generally, higher switching frequency (f_{sw}) leads to smaller size and higher losses. Operation around 400kHz is a reasonable compromise considering size, efficiency and EMI. The value of R_T for 400kHz switching frequency is calculated as follows:

$$R_T = \left(\frac{1}{f_{sw}} - 18ns\right) \times 31.5\frac{\Omega}{ns} = 78.2k\Omega \tag{32}$$

A standard value of 78.7kΩ is chosen for R_T.

7.2.2.4 Inductor Selection L_m

Three main parameters are considered when selecting the inductance value: Inductor current ripple ratio (RR), falling slope of the inductor current and the RHPZ frequency of the control loop.

- The inductor current ripple ratio is selected to balance the winding loss and core loss of the inductor. As the ripple current increases the core loss increases and the copper loss decreases.
- It is necessary for the falling slope of the inductor current to be small enough to prevent sub-harmonic oscillation. A larger inductance value results in a smaller falling slope of the inductor current.
- Place the RHPZ at high frequency to allow a higher crossover frequency of the control loop. As the inductance value decreases the RHPZ frequency increases.

According to peak current mode control theory, it is necessary that the slope compensation ramp is greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle, that is:

$$V_{slope} \times f_{sw} > \frac{V_{out\_max} - V_{in\_min}}{2 \times L_m} \times R_{cs} \tag{33}$$

where

- V_{slope} is a 48mV peak (at 100% duty cycle) slope compensation ramp at the input of the current sense amplifier.

The lower limit of the inductance is found as,

$$L_m > \frac{V_{out\_max} - V_{in\_min}}{2 \times V_{slope} \times f_{sw}} \times R_{cs} \tag{34}$$

R_{cs} is estimated to be 1.5mΩ, so the following is found,

$$L_m > 1.4\mu H \tag{35}$$

The RHPZ frequency is found as,

$$\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m\_eq}} \tag{36}$$

It is necessary that the crossover frequency is lower than 1/5 of RHPZ frequency,

$$f_c < \frac{1}{5} \times \frac{\omega_{RHPZ}}{2\pi} \tag{37}$$

Assume a crossover frequency of 1kHz is desired, the upper limit of the inductance is found as,

$$L_m < 5.2\mu H \tag{38}$$

The inductor ripple current is typically set between 30% and 70% of the full load current, known as a good compromise between core loss and winding loss of the inductor.

Per phase input current is calculated as,

$$I_{in\_vinmax} = \frac{P_{out}}{\eta \times V_{in\_max}} = 29.2A \tag{39}$$

In continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33%. The input voltage that result in a maximum ripple ratio is found as,

$$V_{in\_RRmax} = V_{out\_max} \times (1 - 0.33) = 30V \tag{40}$$

Thus, it is necessary to use the maximum input voltage V_{in_max} to calculate the maximum ripple ratio.

For this example, a ripple ratio of 0.3, 30% of the input current was chosen. Knowing the switching frequency and the typical output voltage, the inductor value is calculated as follows,

$$L_m = \frac{V_{in\_max}}{I_{in} \times RR} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_max}}{V_{out\_max}}\right) = \frac{18V}{29.2A \times 0.3} \times \frac{1}{400kHz} \times 0.6 = 3.1\mu H \quad (41)$$

The closest standard value of 3.3µH was chosen for L_m.

The inductor ripple current at typical input voltage is calculated as:

$$I_{pp} = \frac{V_{in\_typ}}{L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_typ}}{V_{out}}\right) = 7.4A \quad (42)$$

If a ferrite core inductor is selected, make sure the inductor does not saturate at peak current limit. The inductance of a ferrite core inductor is almost constant until saturation. Ferrite core has low core loss with a big size.

For powder core inductor, the inductance decreases slowly with increased DC current. This action leads to higher ripple current at high inductor current. For this example, the inductance drops to 70% at peak current limit compared to 0A. The current ripple at peak current limit is found as,

$$I_{pp\_bias} = \frac{V_{in\_typ}}{0.7 \times L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_typ}}{V_{out}}\right) = 10.6A \quad (43)$$

7.2.2.5 Current Sense Resistor R_{cs}

The maximum per phase average input current at typical input voltage and maximum output voltage is calculated as:

$$I_{in\_vintyp} = \frac{P_{out}}{\eta \times V_{in\_typ}} = 36.5A \quad (44)$$

The peak current is calculated as:

$$I_{pk\_vintyp} = I_{in\_vintyp} + \frac{I_{pp\_bias}}{2} = 36.5A + \frac{10.6A}{2} = 41.8A \quad (45)$$

The current sense resistor is found as:

$$R_{cs} = \frac{V_{CLTH}}{I_{pk\_vintyp}} = \frac{60mV}{41.8A} = 1.43m\Omega \quad (46)$$

A standard value of 1.5mΩ is chosen for R_{cs}.

7.2.2.6 Current Sense Filter R_{CSFP}, R_{CSFN}, C_{CS}

RC filters are suggested for current sensing. 100pF of C_{CS} and 1Ω of R_{CSFP}, R_{CSFN} are normal recommendations. Place C_{CS} close to the device.

Route CSPx and CSNx traces together with Kelvin connections to the current sense resistors.

Increase C_{CS} and R_{CSFN} to increase the RC time constant. Increasing R_{CSFP} brings significant current sensing error.

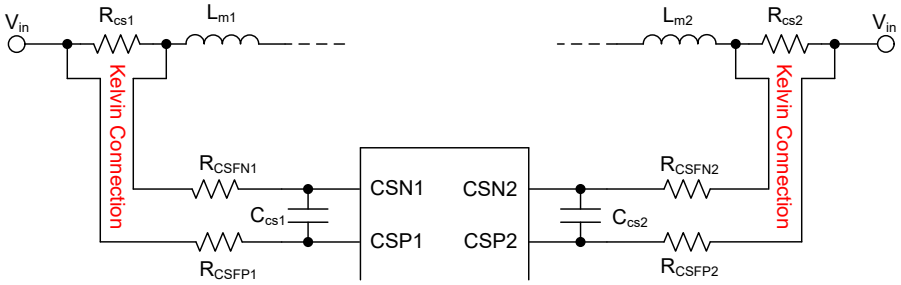


Figure 7-5. Current Sense Filter

7.2.2.7 Low-Side Power Switch Q_L

Select a logic level N-channel MOSFET that 5V VCC is sufficient to completely enhance the MOSFET. Also, note the minimum HOx-SWx voltage is 3.75V during bypass operation. Make sure the MOSFET is turned on at this voltage.

Selection of the power MOSFET devices by breaking down the losses is one way to compare the relative efficiencies of different devices. Losses in the low-side MOSFET device is separated into conduction loss and switching loss.

Low-side conduction loss is approximately calculated as follows:

$$P_{COND\_LS} = D \times I_{in}^2 \times R_{DS(on)} \times 1.3 \quad (47)$$

Where, the factor of 1.3 accounts for the increase in the MOSFET on-resistance due to heating. Alternatively, estimate the high temperature on-resistance of the MOSFET using the $R_{DS(ON)}$ vs temperature curves in the MOSFET datasheet.

Switching loss occurs during the brief transition period as the low-side MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET device. The low-side switching loss is approximately calculated as follows:

$$P_{SW\_LS} = 0.5 \times V_{out} \times I_{in} \times (t_R + t_F) \times f_{sw} \quad (48)$$

t_R and t_F are the rise and fall times of the low-side MOSFET. The rise and fall times are usually mentioned in the MOSFET data sheet or are empirically observed with an oscilloscope.

Reverse recovery of the high-side MOSFET increases the fall time and turn on current of the low-side MOSFET resulting in higher turn on loss.

Place an additional Schottky diode in parallel with the low-side MOSFET, with short connections to the source and drain in order to minimize negative voltage spikes at the SW node.

7.2.2.8 High-Side Power Switch Q_H

Losses in the high-side MOSFET device is separated into conduction loss, dead-time loss, and reverse recovery loss. Switching loss is calculated for the low-side MOSFET device only. Switching loss in the high-side MOSFET device is negligible because the body diode of the high-side MOSFET device turns on before and after the high-side MOSFET device switches.

High-side conduction loss is approximately calculated as follows:

$$P_{COND\_HS} = D' \times I_{in}^2 \times R_{DS(on)} \times 1.3 \quad (49)$$

Dead-time loss is approximately calculated as follows:

$$P_{DT\_HS} = V_D \times I_{in} \times (t_{DLH} + t_{DHL}) \times f_{sw} \quad (50)$$

where

- V_D is the forward voltage drop of the high-side MOSFET body diode.
- t_{DLH} is the deadtime between low side switch turn-off and high side switch turn-on.
- t_{DHL} is the deadtime between high side switch turn-off and low side switch turn-on.

Reverse recovery characteristics of the high-side MOSFET switch strongly affect efficiency, especially when the output voltage is high. Small reverse recovery charge helps to increase the efficiency while also minimizes switching noise.

Reverse recovery loss is approximately calculated as follows:

$$P_{RR\_HS} = V_{out} \times Q_{RR} \times f_{sw} \quad (51)$$

where

- Q_{RR} is the reverse recovery charge of the high-side MOSFET body diode.

Place a 100kΩ gate resistor between MOSFET gate and source. The resistance is determined by the charge pump source current (I_{CP}) in bypass mode. If too low of a resistance is chosen, the gate voltage is too low to fully turn on the high side MOSFET.

Place an additional Schottky diode in parallel with the high-side switch to improve efficiency. Usually, the power rating of this parallel Schottky diode is less than the high-side switch because the diode conducts only during dead-times. It is necessary that the power rating of the parallel diode is high enough to handle inrush current at startup, any load exists before switching, hiccup mode operation, and so forth.

7.2.2.9 Snubber Components

A resistor-capacitor snubber network across the high-side N-channel MOSFET device reduces ringing and spikes at the switching node. Excessive ringing and spikes cause erratic operation and couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50Ω. Increasing the value of the snubber capacitor results in more damping, but this action also results higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber is not necessary with an optimized layout.

7.2.2.10 Vout Programming

For fixed output voltage, program V_{OUT} by connecting a resistor to ATRK/DTRK and turn on precise internal 20μA current source.

$$R_{ATRK} = \frac{V_{out\_max}}{6V} \times 10k\Omega = 75k\Omega \quad (52)$$

For class-H audio application, adjust V_{out} to optimize the efficiency. Apply analog tracking or digital tracking with ATRK/DTRK.

Program the output voltage by digital PWM signal (DTRK). The duty cycle D_{TRK} is found as:

$$D_{TRK\_max} = \frac{V_{out\_max}}{75V} = 60\% \quad (53)$$

$$D_{TRK\_min} = \frac{V_{out\_min}}{75V} = 10.7\% \quad (54)$$

Make sure the DTRK frequency is between 100kHz and 2200kHz. Apply the DTRK PWM signal when the IC is enabled.

For analog tracking, apply a voltage to ATRK/DTRK to program Vout. The voltage is found as:

$$V_{ATRK\_max} = \frac{V_{out\_max}}{30} = 1.5V \quad (55)$$

$$V_{ATRK\_min} = \frac{V_{out\_min}}{30} = 0.267V \quad (56)$$

Use a two stage RC filter with offset to convert a digital PWM signal to analog voltage as shown in Figure 7-6.

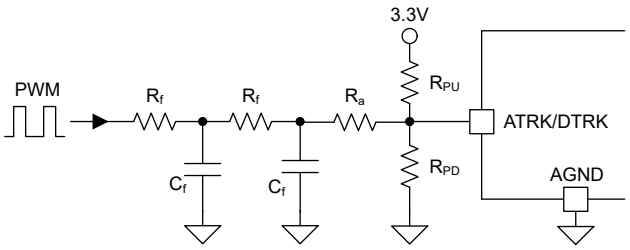


Figure 7-6. Two Stage RC Filter to ATRK/DTRK

The two stage RC filter is used to filter the PWM signal into a smooth analog voltage. The two stage RC filter is selected considering voltage ripple and settling time on ATRK/DTRK.

100% PWM duty cycle sets the output voltage to V_{out_max} and 0% PWM duty cycle sets the output voltage to V_{out_min}. R_t and R_b are used to adjust ATRK/DTRK offset voltage.

The V_{trk_max} and V_{trk_min} is found as,

$$V_{ATRK\_max} = V_{dd}\frac{R_b}{(2R_f + R_a)\|R_t + R_b} \quad (57)$$

$$V_{ATRK\_min} = V_{dd}\frac{(2R_f + R_a)\|R_b}{(2R_f + R_a)\|R_b + R_t} \quad (58)$$

Where V_{dd} is the amplitude of the PWM signal; d is the PWM duty cycle.

The AC transfer function from input to V_{ATRK} can be found as,

$$G_{trk}(s) = \frac{\frac{R_L}{2R_f + R_L}}{1 + 2\zeta\frac{s}{\omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad (59)$$

Where

$$R_L = R_a + R_b\|R_t \quad (60)$$

$$\omega_n = \frac{1}{R_f \times C_f\sqrt{\frac{R_L}{2R_f + R_L}}} \quad (61)$$

$$\zeta = \frac{1}{2}\left(\frac{R_f}{R_L} + 3\right)\sqrt{\frac{R_L}{2R_f + R_L}} \quad (62)$$

The roots of the denominator are found as,

$$s_1 = -\zeta\omega_n + \omega_n\sqrt{\zeta^2 - 1} \quad (63)$$

$$s_2 = -\zeta\omega_n - \omega_n\sqrt{\zeta^2 - 1} \quad (64)$$

As ζ>1, this is an overdamped second order system. s_1 is the dominate pole. 2% settling time t_s is estimated as,

$$t_s = \frac{1}{s_1} \cdot \ln\left(-\frac{0.02 \cdot 2s_1\sqrt{\zeta^2 - 1}}{\omega_n}\right) \quad (65)$$

In this application, 400kHz PWM frequency is used. R_f=4.99kΩ, C_f=47nF, R_a=1.5kΩ, R_t=51kΩ, R_b=7.87kΩ are selected. The 2% settling time is around 1.3ms.

7.2.2.11 Input Current Limit (ILIM/IMON)

The transient power is high in audio applications. For this application 1000W is selected as peak output power. But the average power is typically much lower than the peak power. 300W is selected as average power. With proper ILIM/IMON setting, the average input current is limited to less than 300W while allowing 1000W peak for 100ms. When the average current loop is triggered, V_{OUT} drops till the input and output power is balanced.

The per phase input current at average output power and typical input voltage is found as,

$$I_{avg} = \frac{P_{avg\_total}}{2 \times \eta \times V_{in\_typ}} = 11.0A \quad (66)$$

13A is selected as the average input current limit.

$$I_{lim} = 13A \quad (67)$$

The current out of ILIM/IMON is found as,

$$I_{MON\_lim} = 2 \times (R_{cs} \times I_{lim} \times G_{IMON} + I_{OFFSET}) = 2 \times (1.5m\Omega \times 13A \times 0.333mA/V + 4\mu A) = 21\mu A \quad (68)$$

R_{ILIM} is calculated as:

$$R_{IMON} = \frac{V_{ILIM}}{I_{MON}} = \frac{1V}{21\mu A} = 47.6k\Omega \quad (69)$$

A standard value of 47.5kΩ is chosen for R_{IMON}.

As shown in Figure 7-7, use C_{IMON} and R_c to create a proper delay before the average current loop is triggered.

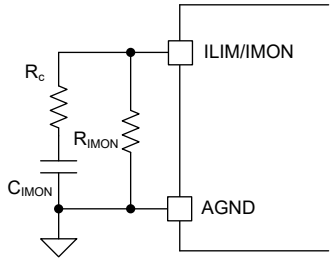


Figure 7-7. ILIM/IMON Pin Configuration

In this application 100ms delay at twice rated power is required.

At zero load current out of ILIM/IMON is found as,

$$I_{MON\_0A} = 2 \times I_{OFFSET} = 8\mu A \quad (70)$$

The ILIM/IMON voltage at zero load is calculated as,

$$V_{IMON\_0A} = R_{IMON} \times I_{MON\_0A} = 0.38V \quad (71)$$

At twice rated power, current out of ILIM/IMON is found as,

$$I_{MON\_tr} = 2 \times (R_{cs} \times 2 \times I_{lim} \times G_{IMON} + I_{OFFSET}) = 2 \times (1.5m\Omega \times 26A \times 0.333mA/V + 4\mu A) = 34\mu A \quad (72)$$

C_{IMON} is determined by,

$$C_{IMON} = \frac{t_{delay}}{R_{IMON} \times \ln\left(\frac{R_{IMON} \times I_{MON\_tr} - V_{IMON\_0A}}{R_{IMON} \times I_{MON\_tr} - V_{ILIM}}\right)} = 3.0\mu F \quad (73)$$

A standard value of 3.3µF is chosen for C_{IMON}.

R_c is determined by,

$$R_c = \frac{1}{20\pi \times C_{IMON}} = 4.8k \quad (74)$$

A standard value of 4.99kΩ is chosen for R_c.

7.2.2.12 UVLO Divider

The desired start-up voltage and the hysteresis are set by the voltage divider R_{UVT}, R_{UVB}. For this design, the start-up voltage (V_{in_on}) is set to 8.5V which is 0.5V below V_{in_min}. UVLO hysteresis voltage is set to 1V. This action results UVLO shutdown voltage (V_{in_off}) of 7.5V. The values of R_{UVT}, R_{UVB} are calculated as follows:

$$R_{UVT} = \frac{V_{in\_on} - \frac{V_{UVLO\_RISING}}{V_{UVLO\_FALLING}} \times V_{in\_off}}{I_{UVLO\_HYS}} = \frac{8.5V - \frac{1.1V}{1.075V} \times 7.5V}{10\mu A} = 82.6k\Omega \quad (75)$$

A standard value of 82.5kΩ is chosen for R_{UVT}.

$$R_{UVB} = \frac{V_{UVLO\_FALLING} \times R_{UVT}}{V_{in\_off} - V_{UVLO\_FALLING}} = \frac{1.075V \times 82.5k\Omega}{7.5V - 1.075V} = 13.8k\Omega \quad (76)$$

A standard value of 13.8kΩ is chosen for R_{UVB}.

A 100nF UVLO capacitor (C_{UVLO}) is selected in case V_{in} drops below V_{in_off} momentarily during the start-up or during a severe load transient at the low input voltage.

7.2.2.13 Soft Start

The soft-start time at maximum output voltage is the longest. To obtain a 6ms soft-start time, the soft-start capacitor is found as,

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ATRK\_max}}\left(\frac{V_{out\_max}}{V_{out\_max} - V_{in\_typ}}\right) = \frac{50\mu A \times 6ms}{1.5V}\left(\frac{45V}{45V - 14.4V}\right) = 0.29\mu F \quad (77)$$

A standard value of 0.33µF is chosen for C_{SS}.

7.2.2.14 CFG Settings

CFG0 is chosen based on deadtime and turn on or turn off ATRK/DTRK pin 20µA current source referring to CFG0-pin Settings (LM5125-Q1).

Here, 50ns deadtime and turning on 20µA current source are selected. Level 3 (1.3kΩ) is selected for CFG0.

CFG1 is selected considering OVP, DRSS, peak current limit latch and PGOOD OVP enable.

Here, 50V OVP (OVP bit 0), DRSS off, I_{CL_latch} disabled, PGOOD OVP disabled are selected. Level 10 (10.5kΩ) is selected for CFG1.

CFG2 is selected considering OVP, SYNCIN, and clock dithering referring to CFG2-pin Settings (CFG2_7_LVL = 0), LM5125-Q1 .

Here, 50V OVP (OVP bit 1), SYNCIN disabled, DRSS set according to CFG1 are selected. Level 1 (0Ω) is selected for CFG2.

7.2.2.15 Output Capacitor C_{out}

The output capacitors smooth the output voltage ripple and provide a source of charge during load transient conditions.

Carefully select the output capacitor ripple current rating. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement is dramatically reduced by placing high-quality ceramic capacitors earlier than the bulk aluminum capacitors close to the power switches.

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors.

The single phase boost output RMS ripple current is expressed as,

$$I_{1p\_rms} \approx I_{out} \times \sqrt{\frac{D}{D'}} \tag{78}$$

The output RMS current is reduced with interleaving as shown in Figure 7-8. Dual phase interleaved boost output RMS ripple current is expressed as,

$$I_{out\_2p\_rms} \approx \begin{cases} \frac{I_{out}}{\sqrt{2}} \times \frac{\sqrt{D \times (1-2D)}}{D'}, & D < 0.5 \\ \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{2D-1}{D'}}, & D \geq 0.5 \end{cases} \tag{79}$$

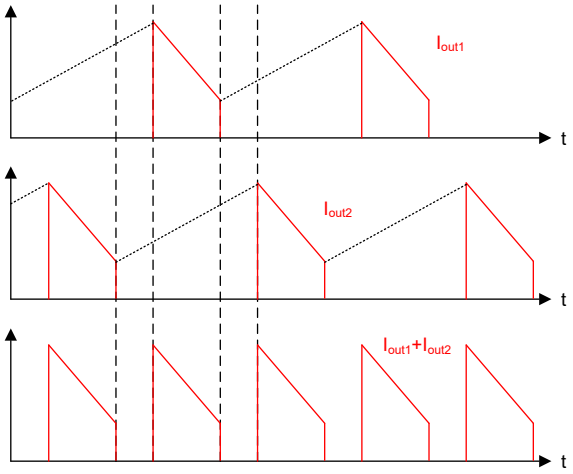


Figure 7-8. Normalized Output Capacitor RMS Ripple Current

Decoupling capacitors are critical to minimize voltage spikes of the MOSFETs and improve EMI performance. Quite a few 0603/100nF ceramic capacitors are placed close to the MOSFETs following "vertical loop" concept. Refer to *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief for more details.

A few 10µF ceramic capacitors are also necessary to reduce the output voltage ripple and split the output ripple current.

Typically, aluminum capacitors are required for high capacitance. In this example, four 150µF aluminum capacitors are selected.

The output transient response is closely related to the bandwidth of the loop gain and the output capacitance. According to *How to Determine Bandwidth from the Transient-response Measurement* technical article, the overshoot or undershoot V_p is estimated as,

$$V_p = \frac{\Delta I_{tran}}{2\pi \times f_c \times C_{out}} \tag{80}$$

where ΔI_{tran} is the transient load current step.

Please be aware that Equation 80 is valid only if the converter is always operating in CCM or FPWM during load step. If the converter enters DCM or pulsing skip mode at light load, the overshoot is worse.

Due to the inherent path from input to output, unlimited inrush current flows when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising need to be controlled by a hot-swap or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side MOSFET.

7.2.2.16 Input Capacitor C_{in}

Input capacitors are always required to provide a stable input voltage. It is necessary that the input capacitors is able to handle the inductor ripple current.

The single phase boost input RMS ripple current is expressed as,

$$I_{in\_1p\_rms} = \frac{I_{pp}}{\sqrt{12}} \tag{81}$$

The input RMS current is reduced with interleaving as shown in Figure 7-9. Dual phase interleaved boost input RMS ripple current is expressed as,

$$I_{in\_2p\_rms} = \begin{cases} \frac{I_{pp}}{\sqrt{12}} \times \frac{1-2D}{D'}, & D < 0.5 \\ \frac{I_{pp}}{\sqrt{12}} \times \frac{2D-1}{D}, & D \geq 0.5 \end{cases} \tag{82}$$

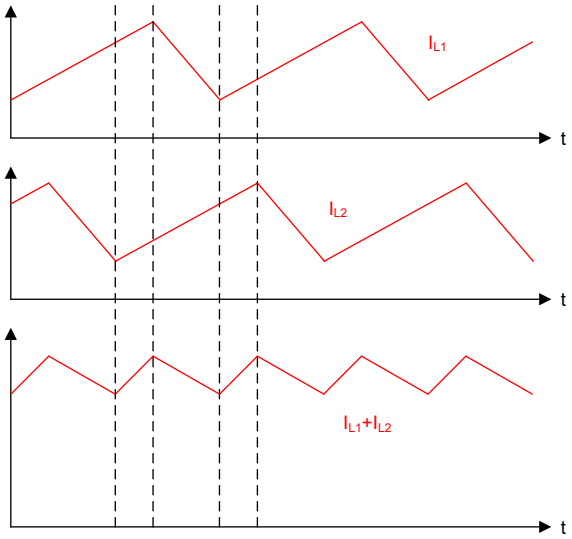


Figure 7-9. Normalized Input Capacitor RMS Ripple Current

The input capacitor is also an important part of the input filter. Higher capacitance and ESR help damping the input filter better. Aluminum electrolytic capacitor is a good choice for input capacitor with high capacitance and ESR. Refer to *Input Filter Design for Switching Power Supplies* application note for more details.

7.2.2.17 Bootstrap Capacitor

The bootstrap capacitor between the HBx and SWx pin supplies the gate current to charge the high-side MOSFET device gate during each turn-on cycle and also supplies recovery charge for the bootstrap diode. These current peaks are several amperes. The recommended value of the bootstrap capacitor is 0.1µF. Use good-quality, low-ESR, ceramic capacitor for C_{BST}. Place C_{BST} close to the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. The minimum value for the bootstrap capacitor is calculated as follows,

$$C_{BST} = \frac{Q_G}{\Delta V_{BST}} \tag{83}$$

where

- Q_G is the high-side MOSFET gate charge at VCC = 5V
- ΔV_{BST} is the tolerable voltage droop on C_{BST}, which is typically less than 5% of VCC or 0.15V, conservatively

In this example, the value of the bootstrap capacitors (C_{BST}) are 0.1µF.

7.2.2.18 VCC Capacitor C_{VCC}

The primary purpose of the VCC capacitor is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. Choose C_{VCC} at least 10 times greater than the value of C_{BST}. Use good-quality, low-ESR, ceramic capacitor for C_{VCC}. Place C_{VCC} close to the pins of the device.

A value of 10µF was selected for this design example.

7.2.2.19 BIAS Capacitor

Use a high-quality, ceramic capacitor for C_{BIAS}. Place C_{BIAS} physically close to the device.

A value of 1µF is selected for this design example.

7.2.2.20 VOUT Capacitor

Use a high-quality, ceramic capacitor for C_{OUT}. Place C_{OUT} physically close to the device.

A value of 0.1µF is selected for this design example.

7.2.2.21 Loop Compensation

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the following four steps:

1. Select crossover frequency, f_C. Select the cross over frequency (f_C) at one fifth of the RHPZ frequency or one tenth of the switching frequency whichever is lower. Choose RHPZ with minimum input voltage and maximum output voltage.

$$\frac{f_{SW}}{10} = 40\text{kHz} \tag{84}$$

$$\frac{f_{RHPZ}}{5} = \frac{R_{out} \times D'^2}{5 \times 2\pi \times L_{m\_eq}} = 1.6\text{kHz} \tag{85}$$

   Crossover frequency f_c=1.6kHz is selected.
2. Determine required R_{COMP}

   Knowing f_c, R_{COMP} is calculated as follows:

$$R_{COMP} = \frac{2\pi \times f_c \times C_{out} \times A_{CS} \times R_{cs\_eq}}{D' \times K_{FB} \times g_m \times G_{ACB}(2\pi \times f_c)} = \frac{2\pi \times 1.6\text{kHz} \times 900\mu\text{F} \times 10 \times 0.75\text{m}\Omega}{0.2 \times \frac{1}{30} \times 1\frac{\text{mA}}{\text{V}} \times \frac{1}{2}} = 20.4\text{k}\Omega \tag{86}$$

   A standard value of 20kΩ is selected for R_{COMP}

3. Determine C_{COMP}

   Place ω_{Z_EA} at the load pole frequency ω_{P_LF} to cancel load pole. Knowing R_{COMP}, C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{R_{COMP} \times \omega_{P\_LF}} = \frac{1}{20k\Omega \times \frac{2}{2.025\Omega \times 900\mu F}} = 45nF \quad (87)$$

   A standard value of 47nF is selected for C_{COMP}

4. Determine C_{HF}.

   Place ω_{HF} at ω_{RHPZ} or ω_{Z_ESR} zero whichever is lower. Knowing R_{COMP}, RHPZ and ESR zero, C_{HF} is calculated as follows:

$$C_{HF} = \frac{1}{R_{COMP} \times \omega_{HF}} = \frac{1}{20k\Omega \times 49kHz} = 1nF \quad (88)$$

   A standard value of 1nF is selected for C_{HF}.

7.2.3 Application Curves

7.2.3.1 Efficiency

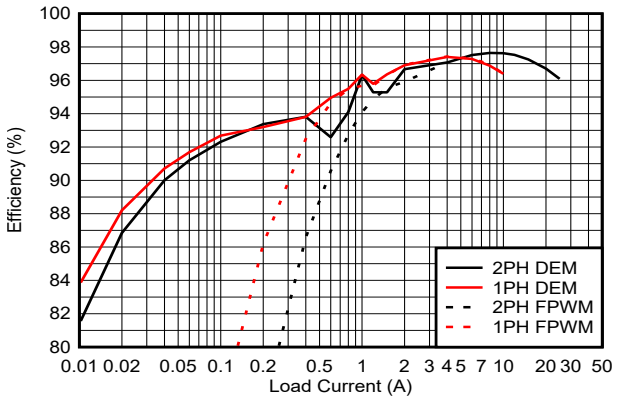


Figure 7-10. Efficiency vs Output Current, V_{IN} = 14.4V, V_{OUT} = 24V

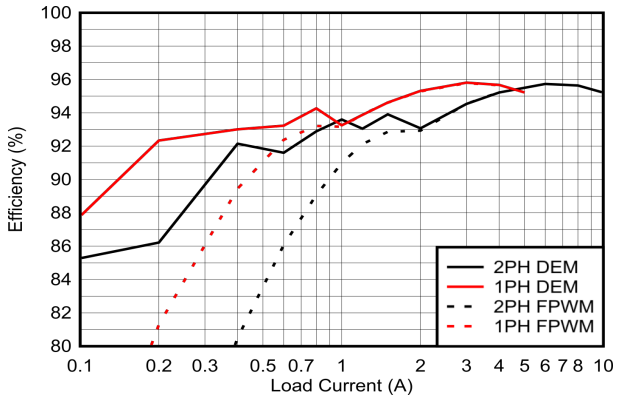


Figure 7-11. Efficiency vs Output Current, V_{IN} = 14.4V, V_{OUT} = 45V

7.2.3.2 Steady State Waveforms

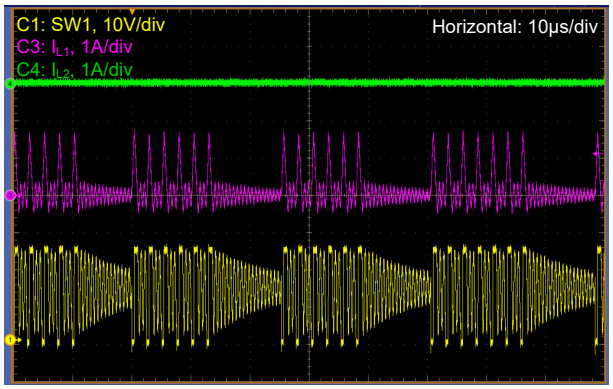


Figure 7-12. V_{IN} = 14.4V, V_{OUT} = 24V, DEM, I_{LOAD}= 0.1A

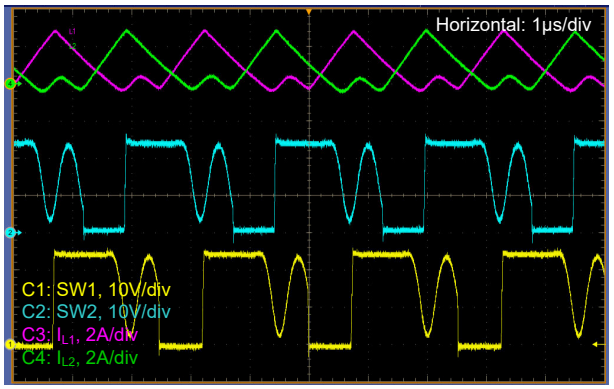


Figure 7-13. V_{IN} = 14.4V, V_{OUT} = 24V, DEM, I_{LOAD}= 1A

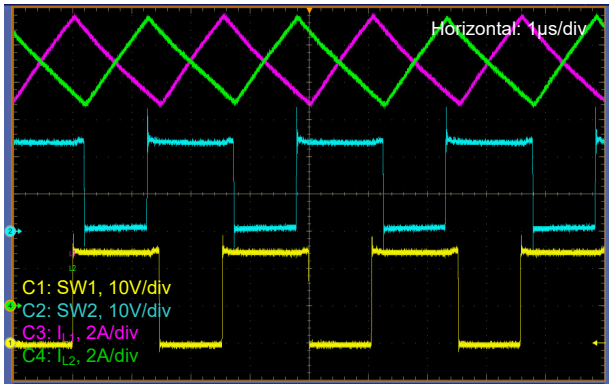


Figure 7-14. V_{IN} = 14.4V, V_{OUT} = 24V, DEM, I_{LOAD}= 15A

7.2.3.3 Step Load Response

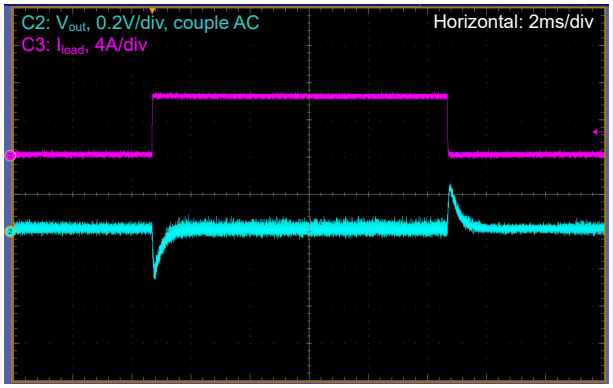


Figure 7-15. Load Transient, V_{IN} = 14.4V, V_{OUT} = 24V, FPWM, I_{LOAD} = 0A to 6.25A at 1A/µs

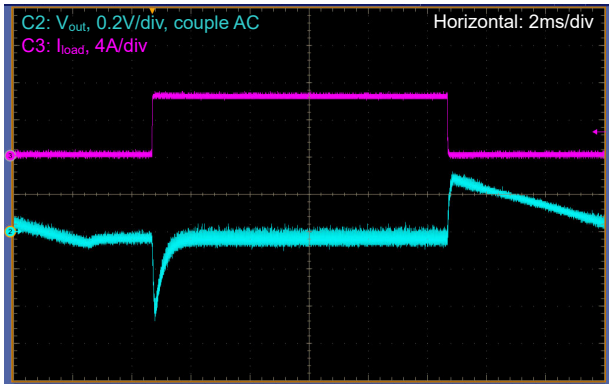


Figure 7-16. Load Transient, V_{IN} = 14.4V, V_{OUT} = 24V, DEM, I_{LOAD} = 0A to 6.25A at 1A/µs

7.2.3.4 Sync Operation

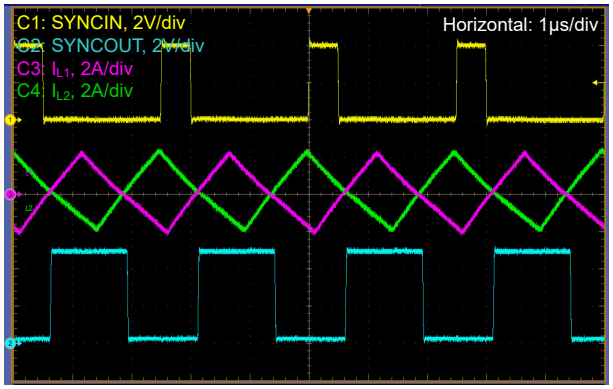


Figure 7-17. V_{IN} = 14.4V, V_{OUT} = 24V, FPWM, I_{LOAD} = 0A, CFG2 = Level 13

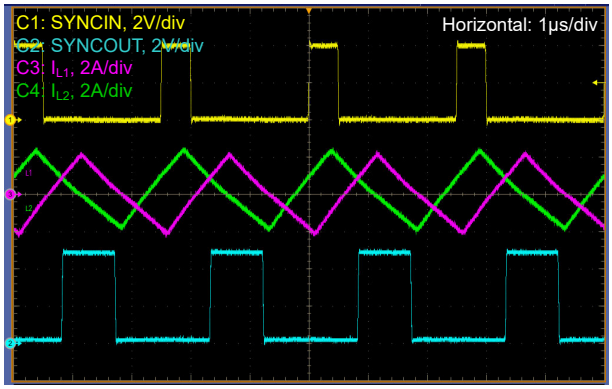


Figure 7-18. V_{IN} = 14.4V, V_{OUT} = 24V, FPWM, I_{LOAD} = 0A, CFG2 = Level 11

7.2.3.5 AC Loop Response Curve

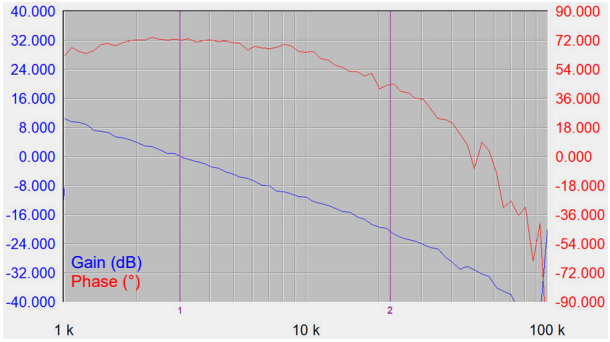


Figure 7-19. Bode Plot, V_{IN}=14.4V, V_{OUT}=40V, I_{OUT}=10A (Average Current Loop Disabled)

7.2.3.6 Thermal Performance

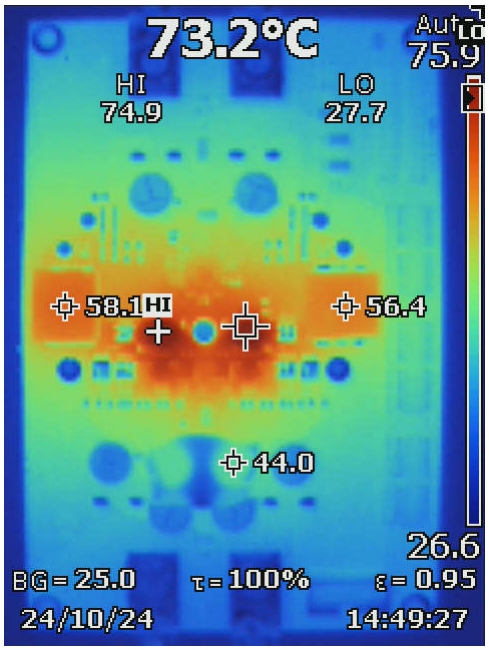


Figure 7-20. V_{IN} = 14.4V, V_{OUT} = 24V, P_{OUT} = 300W, Natural Convection

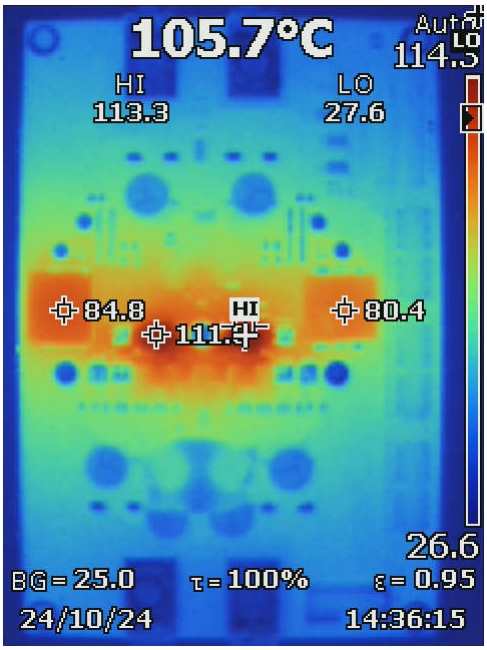


Figure 7-21. V_{IN} = 14.4V, V_{OUT} = 45V, P_{OUT} = 300W, Natural Convection

7.3 Power Supply Recommendations

The LM5125-Q1 is designed to operate over a wide input voltage range. It is necessary that the characteristics of the input supply is compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. It is also necessary that the input supply is capable of delivering the required input current to the fully loaded regulator. Use Equation 89 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{89}$$

where η is the efficiency.

Use the graphs in the *Efficiency* section to obtain the value for the efficiency in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit causes overvoltage transients at V_I each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the controller power stage. Design the EMI input filter carefully to avoid instability as well as some of the previously mentioned affects.

7.4 Layout

7.4.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. Poor PCB design causes among others, converter instability, load regulation problems, noise or EMI issues. Do not use thermal relieved connections in the power path, for VCC or the bootstrap capacitor as thermal relieved connections add significant inductance.

- Place the VCC, BIAS, HB1 and HB2 capacitors close to the corresponding device pins and connect them with short and wide traces to minimize inductance, as the capacitors carry high peak currents.
- Place CSN1, CSP1, CSN2, and CSP2 filter resistors and capacitors close to the corresponding device pins to minimize noise coupling between the filter and the device. Route the traces to the sense resistors R_{CS1} and R_{CS2}, which are placed close to the inductor, as differential pair and surrounded by ground to avoid noise coupling. Use Kelvin connections to the sense resistors.
- Place the compensation network R_{COMP} and C_{COMP} as well as the frequency setting resistor R_{RT} close to the corresponding device pins and connect them with short traces to avoid noise coupling. Connect the analog ground pin AGND to these components.
- Place the ATRK resistor R_{ATRK} (when used) close to the ATRK pin and connect to AGND.
- Note the layout of following components is not so critical:
  - Soft-start capacitor C_{SS}
  - DLY capacitor C_{DLY}
  - ILIM/IMON resistor and capacitor R_{ILIM} and C_{ILIM}
  - CFG0, CFG1 and CFG2 resistors
  - UVLO/EN resistors
- Connect the AGND and PGND pin directly to the exposed pad (EP) to form a star connection at the device.
- Connect the device exposed pad (EP) with several vias to a ground plane to conduct heat away.
- Separate power and signal traces and use a ground plane to provide noise shielding.

The gate drivers incorporate short propagation delays, automatic dead time control, and low-impedance output stages capable of delivering high peak currents. Fast rise, fall times make sure of rapid turn-on and turn-off transitions of the power MOSFETs enabling high efficiency. Minimize stray and parasitic gate loop inductance to avoid high ringing.

- Place the high-side and low-side MOSFETs close to the device.
- Connect the gate driver outputs HO1, HO2, LO1 and LO2 with a short trace to minimize inductance.
- Route HO1, HO2 and SW1, SW2 to the MOSFETs as a differential pair using the flux cancellation effect reducing the loop area.
- Place the V_{OUT} capacitors close to the high-side MOSFETs. Use short and wide traces to minimize the power stage loop C_{OUT} to high-side MOSFET drain connection to avoid high voltage spikes at the MOSFET.
- Connect the low-side MOSFET source connection with short and wide traces to the V_{OUT} and V_I capacitors ground to minimize inductance causing high voltage spikes at the MOSFET.
- Use copper areas for cooling at the MOSFETs thermal pads.

To spread the heat generated by the MOSFETs and the inductor, place the inductor away from the power stage (MOSFETs). However, the longer the trace between the inductor and the low-side MOSFET (switch node) the

higher the EMI and noise emissions. For highest efficiency, connect the inductor by wide and short traces to minimize resistive losses.

7.4.2 Layout Example

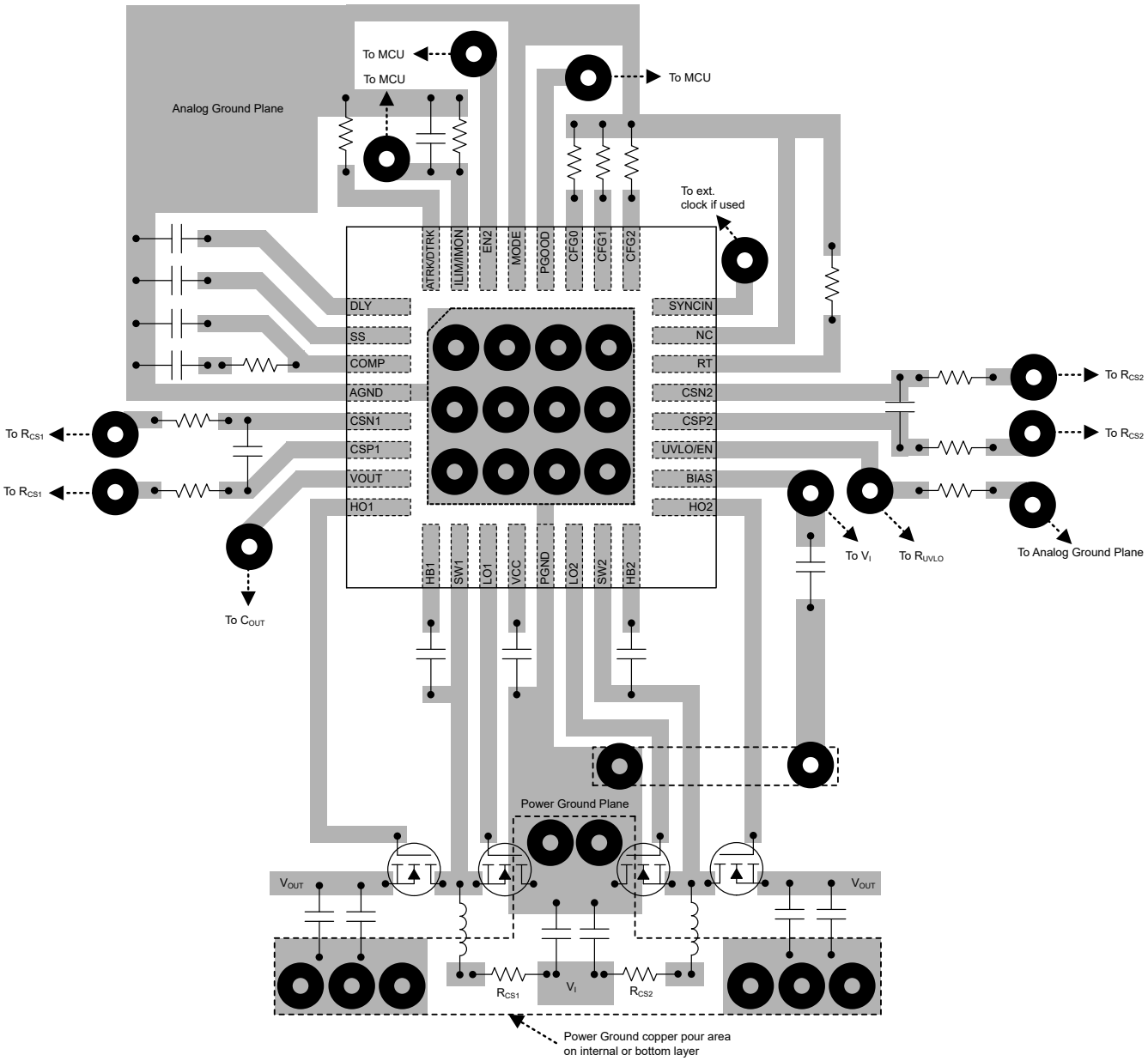


Figure 7-22. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Input Filter Design for Switching Power Supplies* application note
- Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *How to Determine Bandwidth from the Transient-response Measurement* technical article

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision B (April 2025) to Revision C (January 2026)	Page
• Changed minimum SYNCIN frequency detection limit from: 55kHz to: 60kHz	6
• Changed DTRK 100kHz 8% duty cycle limit minimum from: 0.192V to: 0.19V	6
• Changed DTRK 100kHz 8% duty cycle limit maximum from: 0.208V to: 0.21V	6
• Changed DTRK 440kHz 8% duty cycle limit minimum from: 0.19V to: 0.188V	6
• Changed DTRK 440kHz 8% duty cycle limit maximum from: 0.21V to: 0.212V	6
• Changed V_{ZCD} ZCD threshold (CSPx – CSNx) typical from: 1.5mV to: 3mV	6
• Changed V_{ZCD} ZCD threshold (CSPx – CSNx) maximum from: 5mV to: 6mV	6
• Changed V_{ZCD_BYP} ZCD threshold for phase 1 in bypass mode (CSP1 – CSN1) minimum from: -4mV to: -6mV	6
• Changed V_{ZCD_BYP} ZCD threshold for phase 2 in bypass mode (CSP1 – CSN1) minimum from: -4mV to: -6mV	6
• Changed G_{IMON} Transconductance Gain minimum from: 0.283µA/mV to: 0.320µA/mV	6
• Changed G_{IMON} Transconductance Gain maximum from: 0.383µA/mV to: 0.346µA/mV	6

- Changed $I_{SOURCE-MAX}$ Maximum COMP sinking current minimum from: 100µA to: 90µA....6
- Changed $I_{SOURCE-MAX}$ Maximum COMP sourcing current minimum from: 90µA to: 100µA....6
- Changed N-channel MOSFET driver from: full-bridge to: half-bridge....16
- Updated Block Diagram from: Buck-Boost to: Boost Core....17
- Updated V_{OUT} Programming (VOUT, ATRK, DTRK) section....25
- Updated PGOOD reacting on OVP description....27
- Added COMP-pin and Sense Resistor Voltage Limiting the Switch Current (DEM) and (FPWM) figures....28
- Deleted COMP-pin and Sense Resistor Voltage limiting the switch current figure....28
- Updated COMP-pin figures....28
- Added Equation 22 and Equation 23 29
- Added RC tank information....29
- Updated Equation 17, Equation 18, and Equation 19 to include *n* variable....29
- Updated Equation 25 from: G_{ACB} to: F_{ACB} 35
- Updated VOUT programming section....43
- Updated Figure 7-9 title from: Normalized Output Capacitor RMS Ripple Current to: Normalized Input Capacitor RMS Ripple Current....48
- Added Sync Operation section....51

Changes from Revision A (March 2025) to Revision B (April 2025)	Page
• Changed the device status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5125QRHBRQ1	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM 5125Q
LM5125QRHBRQ1.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	LM 5125Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

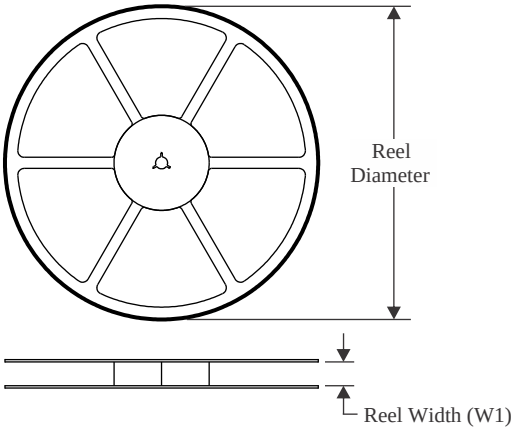
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

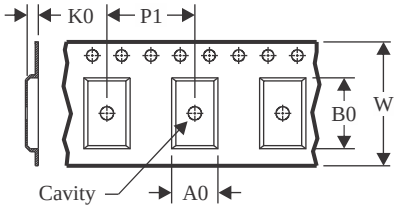
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

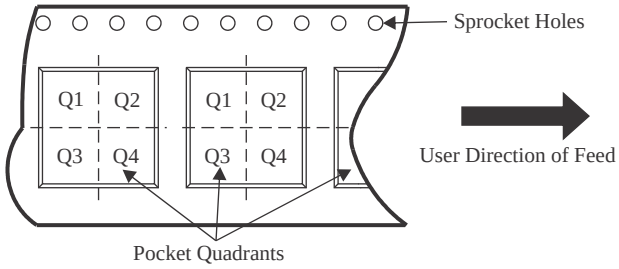


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

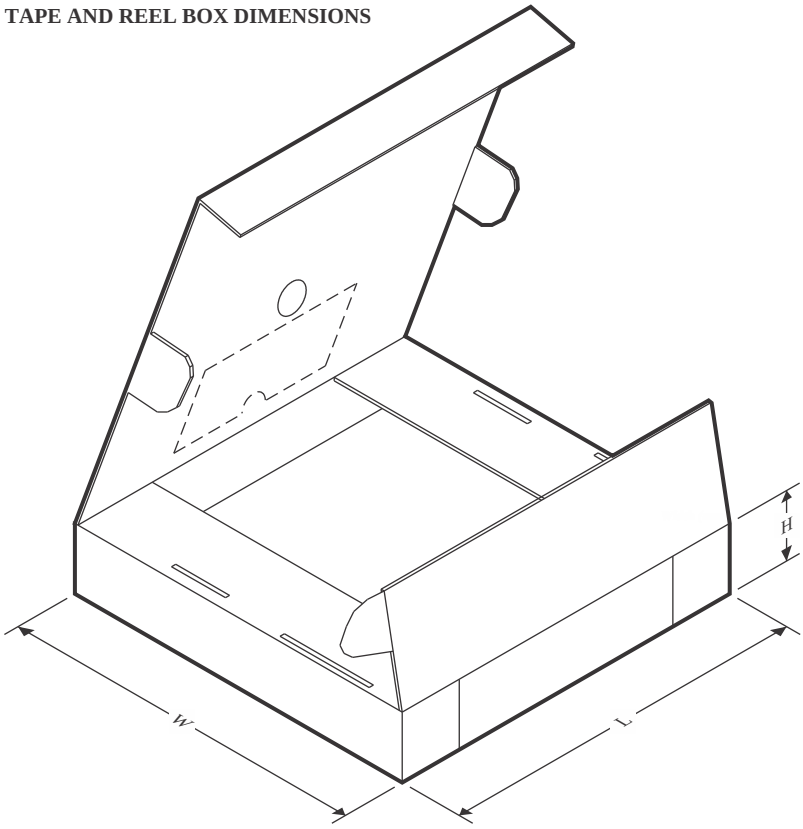
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5125QRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5125QRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0

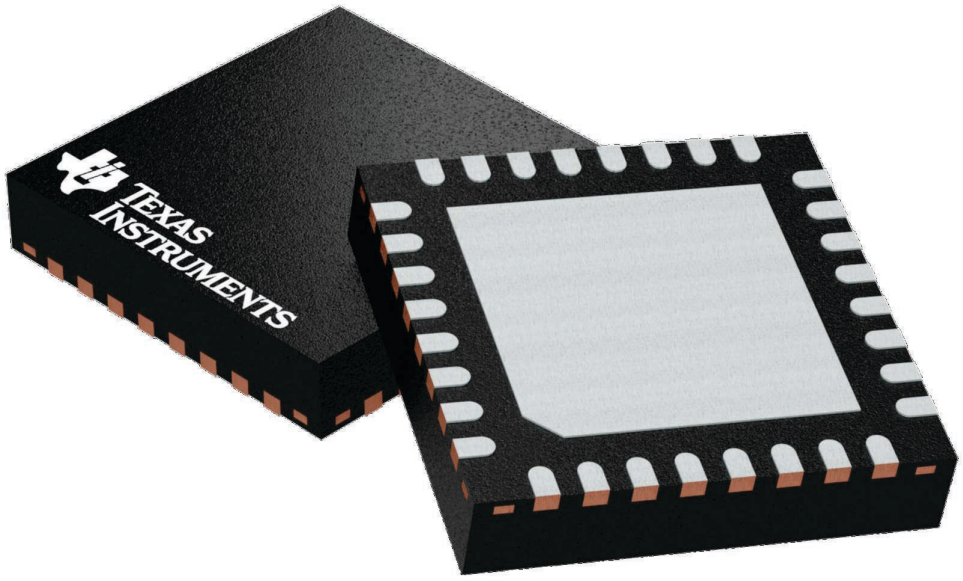
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

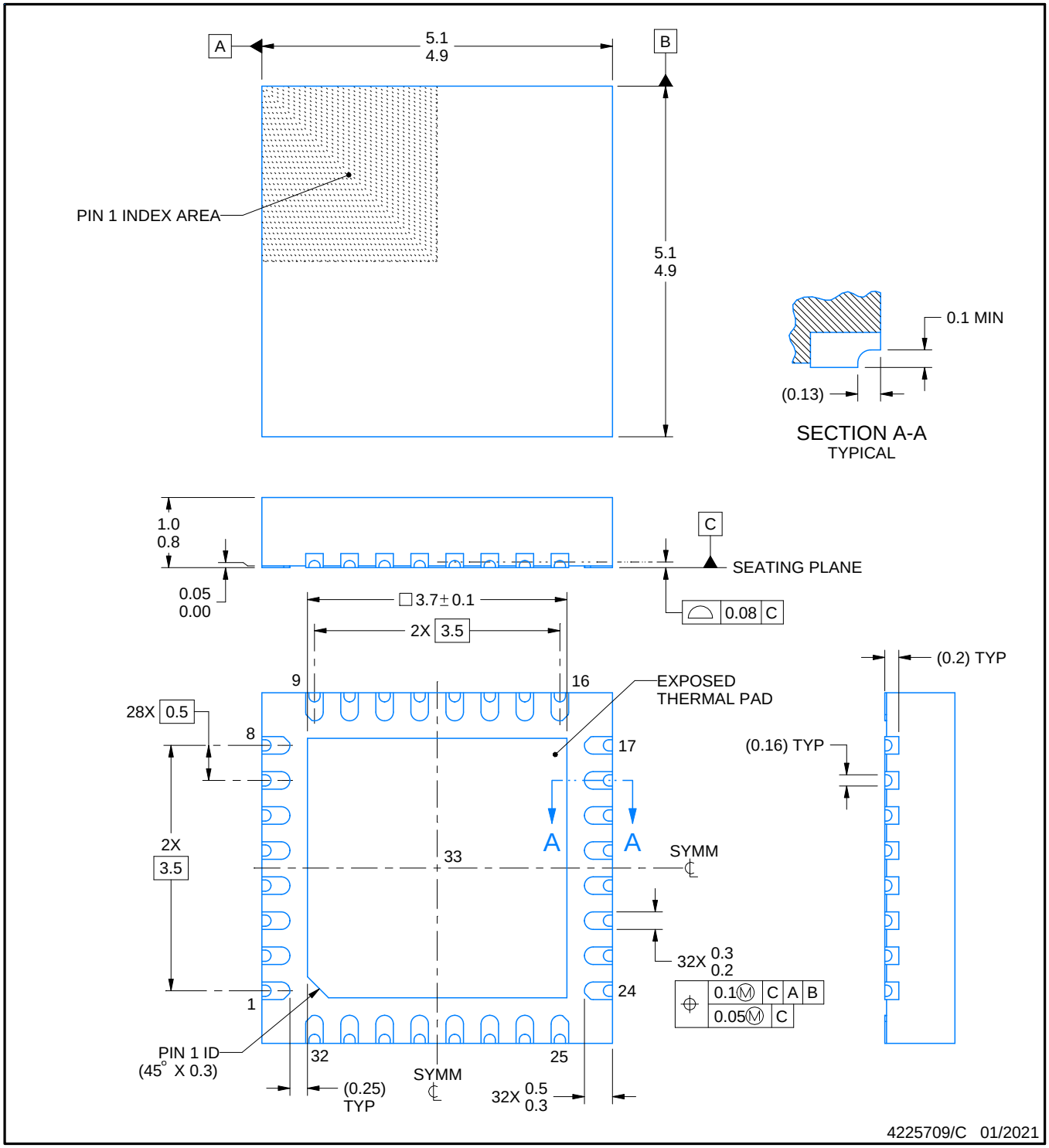
4224745/A

RHB0032U

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

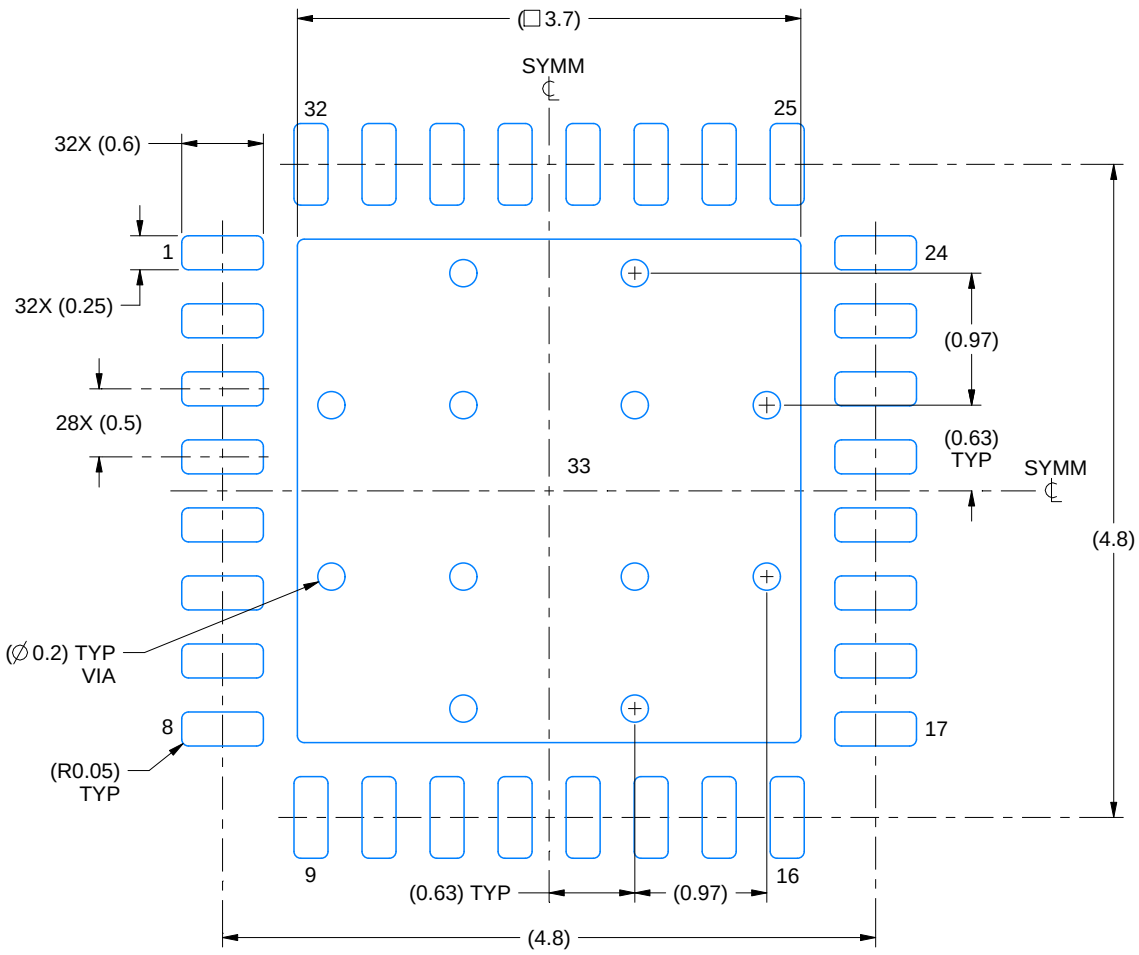
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

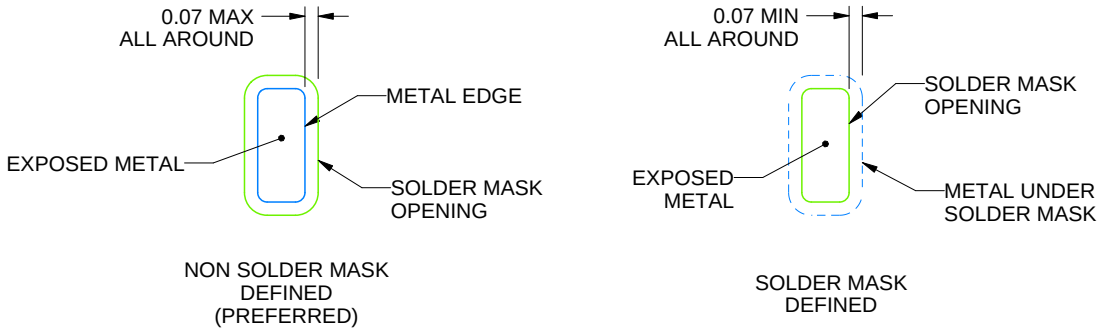
RHB0032U

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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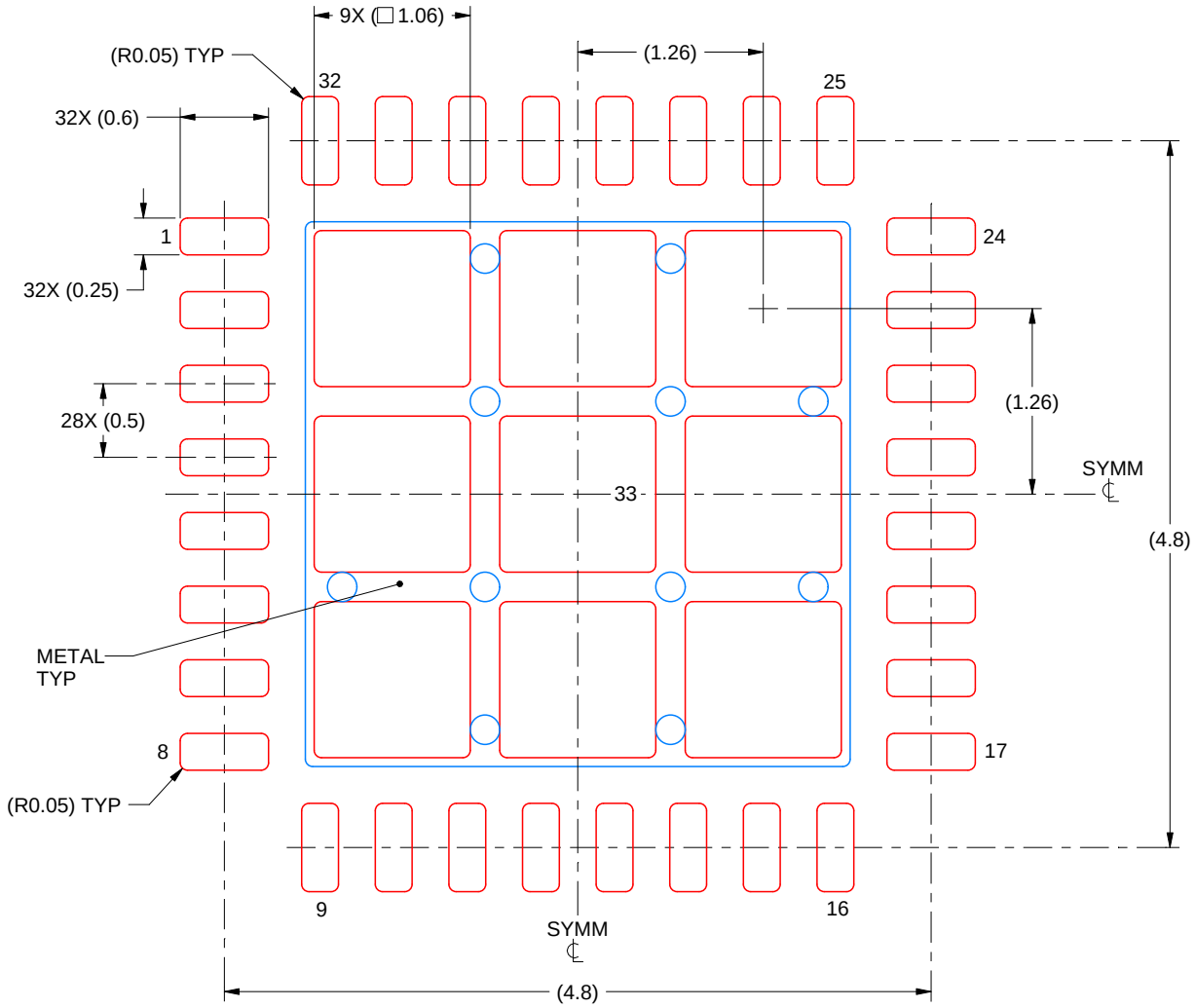
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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