LP5810 4-Channel RGBW LED Driver with Autonomous Control

1 Features

- Operating voltage range:
  - V_{CC} range: 2.7V to 5.5V
  - Logic pins compatible with 1.8V, 3.3V, and 5V
- 4 constant current sinks with high precision:
  - 0.1mA to 51mA per current sink
  - Device-to-device error: max ±5%
  - Channel-to-channel error: max ±5%
  - Ultra-low headroom voltage: 110mV (typ.) at 25.5mA; 210mV (typ.) at 51mA
  - PWM phase shift configurable for each LED
- Ultra-low power consumption:
  - Standby: I_{STB} = 26µA (typical) when CHIP_EN = 0 (data retained)
  - Active: I_{NOR} = 0.4mA (typical) when LED current = 25.5mA
- Analog dimming (current gain control)
  - Global 1-bit Maximum Current (MC): 25.5mA or 51mA
  - Individual 8-bit Dot Current (DC) setting
- PWM dimming up to audible-noise-free 24kHz
  - Individual 8-bit PWM dimming resolution
  - Linear or exponential dimming curves
- Autonomous animation engine control
- Individual LED dot open/short detection
- Integrated de-ghosting function
- 1MHz (max.) I^2C interface
- –40°C to 85°C operating temperature range

2 Applications

LED animation and indication for:

- Portable and wearable electronics - earbud and charging case, E-cigarette, smart watch
- Gaming and home entertainment - smart speaker, RGB mouse, VR headset, and controller
- Internet-of-Things (IOT) - E-tag, video doorbell
- Networkings - router, access point
- Industrial HMI - EV charger, factory automation

3 Description

The LP5810 is a 4-channel RGBW LED driver with autonomous animation engine control. The device has ultra-low normal operation current with 0.4mA (typical) when illuminate LEDs.

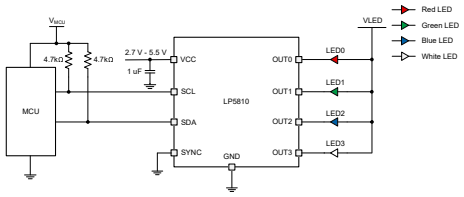
Both analog dimming and PWM dimming methods are adopted to achieve powerful dimming performance. The output current of each LED can be adjusted with 256 steps from 0.1mA to 25.5mA or 0.2mA to 51mA. The 8-bit PWM generator enables smooth and audible-noise-free dimming control for LED brightness.

The autonomous animation engine can significantly reduce the real-time loading of controller. Each LED can be configured through the related registers to realize vivid and fancy lighting effects. The device can generate 6MHz clock signal and use the signal for synchronizing the lighting effects among multiple devices.

Package Information

PART NUMBER[2]	PACKAGE	PACKAGE SIZE (NOM)[3]
LP5810	DSBGA (9)	1.43mm × 1.34mm
	WSON (8)	3mm × 3mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable



Simplified Schematic

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4 Device Comparison

PART NUMBER	Max LED Number	Power Stage	PACKAGE	MATERIAL	I²C Chip Address		SOFTWARE COMPATIBLE
					Bit 4	Bit 3	
LP5813	12	Boost	DSBGA-12	LP5813AYBHR	0	0	Yes
				LP5813BYBHR	0	1	
				LP5813CYBHR	1	0	
				LP5813DYBHR	1	1	
			WSON-12	LP5813ADRRR	0	0	
				LP5813BDRRR	0	1	
				LP5813CDRRR	1	0	
				LP5813DDRRR	1	1	
LP5812	12	Linear	DSBGA-9	LP5812AYBHR	0	0	
				LP5812BYBHR	0	1	
				LP5812CYBHR	1	0	
				LP5812DYBHR	1	1	
			WSON-8	LP5812ADSDR	0	0	
				LP5812BDSDR	0	1	
				LP5812CDSDR	1	0	
				LP5812DDSDR	1	1	
LP5811	4	Boost	DSBGA-12	LP5811AYBHR	0	0	
				LP5811BYBHR	0	1	
				LP5811CYBHR	1	0	
				LP5811DYBHR	1	1	
			WSON-12	LP5811ADRRR	0	0	
				LP5811BDRRR	0	1	
				LP5811CDRRR	1	0	
				LP5811DDRRR	1	1	
LP5810	4	Linear	DSBGA-9	LP5810AYBHR	0	0	
				LP5810BYBHR	0	1	
				LP5810CYBHR	1	0	
				LP5810DYBHR	1	1	
			WSON-8	LP5810ADSDR	0	0	
				LP5810BDSDR	0	1	
				LP5810CDSDR	1	0	
				LP5810DDSDR	1	1	

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5 Pin Configuration and Functions

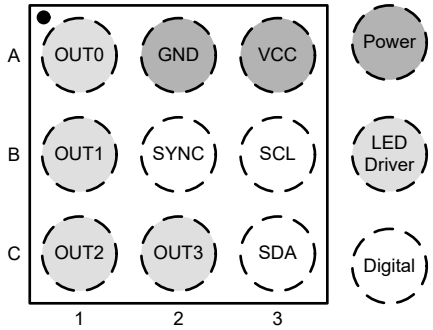

Figure 5-1. LP5810 YBH Package 9-Pin DSBGA Top View

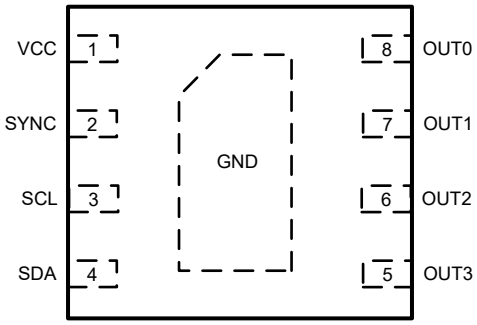

Figure 5-2. LP5810 DSD Package 8-Pin WSON Top View

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Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	YBH	DSD		
OUT0	A1	8	O	Output 0 which contains current sink 0 and high-side scan FET 0. If not used, this pin must be floating.
GND	A2	Thermal Pad	G	Ground. Must be connected to the common ground plane
VCC	A3	1	P	Boost converter output. A 22uF capacitor is recommended to be connected between this pin with GND and be placed as close to the device as possible.
OUT1	B1	7	O	Output 1 which contains current sink 1 and high-side scan FET 1. If not used, this pin must be floating.
SYNC	B2	2	I/O	Synchronous between multiple devices. If not used, this pin can be connected to ground to save power.
SCL	B3	3	I	I^2C serial interface clock input.
OUT2	C1	6	O	Output 2 which contains current sink 2 and high-side scan FET 2. If not used, this pin must be floating.
OUT3	C2	5	O	Output 3 which contains current sink 3 and high-side scan FET 3. If not used, this pin must be floating.
SDA	C3	4	I/O	I^2C serial interface data input/output.

(1) P: Power Pin; I: Input Pin; I/O: Input/Output Pin; O: Output Pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range at terminals	VCC	–0.3	6	V
	OUT0, OUT1, OUT2, OUT3	-0.3	6	V
	SCL, SDA, SYNC	-0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage range	0.5		5.5	V
C_{IN}	Effective input capacitance range	1	4.7		µF
OUT0, OUT1, OUT2, OUT3	Voltage on OUT0, OUT1, OUT2, OUT3 pins	0		5.5	V
SCL, SDA, SYNC	Voltage on SCL, SDA, SYNC pins	0		5.5	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LP5810/2		LP5811/3		UNIT
		YBH (DSBGA)	DSD (WSON)	YBH (DSBGA)	DRR (WSON)	
		9 PINS	8 PINS	12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.1	50.8	92.1	47.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	51.1	0.4	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	22.9	25.9	20.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	1.1	0.2	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.8	22.8	25.8	20.9	°C/W

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THERMAL METRIC[1]		LP5810/2		LP5811/3		UNIT
		YBH (DSBGA)	DSD (WSON)	YBH (DSBGA)	DRR (WSON)	
		9 PINS	8 PINS	12 PINS	12 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	8.5	n/a	6.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C), V_{IN} = 3.6V, VOUT = 5V, C_{IN} = 1µF, C_{OUT} = 1µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
VCC	Input voltage range		2.5		5.5	V
V_{CC_UVLO}	Under-voltage lockout threshold	VCC rising		2.4	2.5	V
	Under-voltage lockout threshold	VCC falling		2.1	2.2	V
I_{STB}	Standby current into VCC pin	CHIP_EN = 0 (bit), VCC = 3.6V		25	28	µA
I_{NOR}	Normal operation current into VCC pin	CHIP_EN = 1 (bit), VCC = 5V, I_{OUT0} = I_{OUT1} = I_{OUT2} = I_{OUT3} = 25.5mA (MC = 0, DC = 255, PWM = 255)		0.4	0.6	mA
LED Driver Output						
I_{CS}	Constant current sink output range	VCC = 3.6V, MC = 0, manual_pwm_x = FFh (100% ON)	0.1		25.5	mA
		VCC = 3.6V, MC = 1, manual_pwm_x = FFh (100% ON)	0.2		51	mA
I_{CS_LKG}	Constant current sink leakage current	VCC = 3.6V, OUTx = 1V, manual_pwm_x = 0 (0%)		0.1	1	µA
I_{ERR_D2D}	Device to device current error, I_{ERR_D2D} = (I_{AVE}-I_{SET})/I_{SET}×100%	All LEDs turn ON. Current set to 0.1mA (max_current = 0, manual_dc_x = 01h, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 0.2mA (max_current = 1, manual_dc_x = 01h, manual_pwm_x = FFh)	–3		3	%
		All LEDs turn ON. Current set to 1mA (max_current = 0, manual_dc_x = 0Ah, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 1mA (max_current = 1, manual_dc_x = 05h, manual_pwm_x = FFh)	–3		3	%
		All LEDs turn ON. Current set to 25.5mA (max_current = 0, manual_dc_x = FFh, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 51mA (max_current = 1, manual_dc_x = FFh, manual_pwm_x = FFh)	–3		3	%

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Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C), V_{IN} = 3.6V, VOUT = 5V, C_{IN} = 1µF, C_{OUT} = 1µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ERR_C2C}	Channel to Channel current error $I_{ERR_C2C} = (I_{OUTX}-I_{AVE})/I_{AVE}\times100\%$	All LEDs turn ON. Current set to 0.1mA (max_current = 0, manual_dc_x = 01h, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 0.2mA (max_current = 1, manual_dc_x = 01h, manual_pwm_x = FFh)	–3		3	%
		All LEDs turn ON. Current set to 1mA (max_current = 0, manual_dc_x = 0Ah, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 1mA (max_current = 1, manual_dc_x = 05h, manual_pwm_x = FFh)	–3		3	%
		All LEDs turn ON. Current set to 25.5mA (max_current = 0, manual_dc_x = FFh, manual_pwm_x = FFh)	–5		5	%
		All LEDs turn ON. Current set to 51mA (max_current = 1, manual_dc_x = FFh, manual_pwm_x = FFh)	–3		3	%
V_{HR}	LED driver output hearroom voltage	All LEDs turn ON. Current set to 25.5mA (max_current = 0, manual_dc_x = FFh)		0.11	0.15	V
		All LEDs turn ON. Current set to 51mA (max_current = 1, manual_dc_x = FFh)		0.21	0.28	V
f_{LED_PWM}	LED PWM frequency	pwm_fre = 0		24		kHz
		pwm_fre = 1		12		kHz
f_{OSC}	Internal oscillator frequency	vsync_out_en = 1		6		MHz
Logic Interface						
V_{IH_LOGIC}	High level input voltage of SDA, SCL, SYNC		1.4			V
V_{IL_LOGIC}	Low level input voltage of SDA, SCL, SYNC				0.4	V
V_{OH_LOGIC}	High level output voltage of SYNC		VCC - 0.2			V
V_{OL_LOGIC}	Low level output voltage of SDA, SYNC				0.4	V
Protection						
T_{SD}	Thermal shutdown threshold for LED driver part	T_J rising		150		°C
	Thermal shutdown threshold for Boost converter part	T_J rising		155		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		15		°C
V_{LOD_TH}	LED open detection threshold	Current set to 25.5mA (max_current = 0, manual_dc_x = FFh)	70	90	110	mV
		Current set to 51mA (max_current = 1, manual_dc_x = FFh)	150	180	220	mV
V_{LSD_TH}	LED short detection threshold	lsd_th = 00h	0.32 × VCC	0.35 × VCC	0.38 × VCC	V
		lsd_th = 01h	0.42 × VCC	0.45 × VCC	0.48 × VCC	V
		lsd_th = 10h	0.52 × VCC	0.55 × VCC	0.58 × VCC	V
		lsd_th = 11h	0.62 × VCC	0.65 × VCC	0.68 × VCC	V

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6.6 Timing Requirements

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C), V_{IN} = 3.6V, V_{CC} = 5V, C_{IN} = 1µF, C_{OUT} = 1µF.

I²C Timing Requirements		MIN	NOM	MAX	UNIT
Standard-mode					
f_{SCL}	SCL clock frequency	0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
t_{SU_STA}	Set-up time for a repeated START condition	4.7			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	250			ns
t_r	Rise time of both SDA and SCL signals			1000	ns
t_f	Fall time of both SDA and SCL signals			300	ns
t_{SU_STO}	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
Fast-mode					
f_{SCL}	SCL clock frequency	0		400	kHz
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition	0.6			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	100			ns
t_r	Rise time of both SDA and SCL signals			300	ns
t_f	Fall time of both SDA and SCL signals			300	ns
t_{SU_STO}	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF
Fast-mode Plus					
f_{SCL}	SCL clock frequency	0		1000	kHz
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	LOW period of the SCL clock	0.5			µs
t_{HIGH}	HIGH period of the SCL clock	0.26			µs
t_{SU_STA}	Set-up time for a repeated START condition	0.26			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	50			ns
t_r	Rise time of both SDA and SCL signals			120	ns
t_f	Fall time of both SDA and SCL signals			120	ns
t_{SU_STO}	Set-up time for STOP condition	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs
C_b	Capacitive load for each bus line			550	pF
Misc. Timing Requirements					

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Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C), V_{IN} = 3.6V, V_{CC} = 5V, C_{IN} = 1µF, C_{OUT} = 1µF.

I²C Timing Requirements		MIN	NOM	MAX	UNIT
f_{CLK_EX}	VSYNC input clock frequency		6		MHz

6.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), VCC = 3.6V, C_{IN} = 1µF

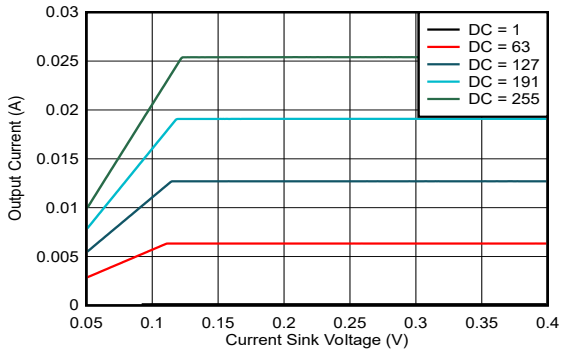

Figure 6-1. Current Sinks Voltage vs Current (MC = 0)

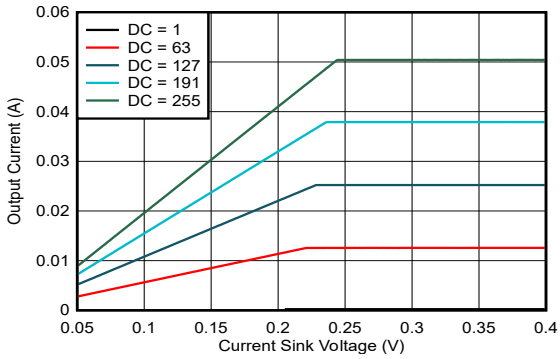

Figure 6-2. Current Sinks Voltage vs Current (MC = 1)

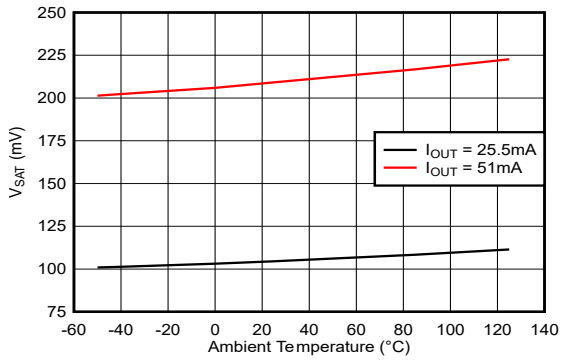

Figure 6-3. V_{SAT} vs Temperature

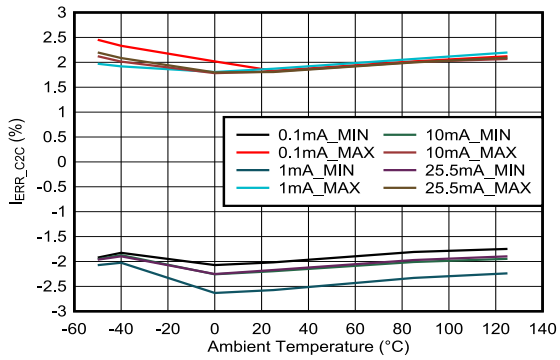

Figure 6-4. Channel-to-Channel Current Accuracy vs Temperature (MC = 0)

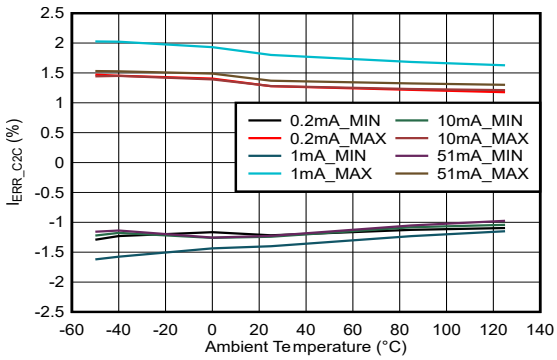

Figure 6-5. Channel-to-Channel Current Accuracy vs Temperature (MC = 1)

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7 Detailed Description

7.1 Overview

The LP5810 is a 4-channel RGBW LED driver with autonomous animation engine control.

The LP5810 has ultra-low operation current at active mode, consuming about 0.4mA when LED maximum current setting is 25.5mA. If all LEDs are turned off, the device enters standby state to reduce power consumption with data retained. When 'chip_enable' bit setting is 0, initial state is entered with minimum power consumption to save power.

The LP5810 supports both analog dimming and PWM dimming. In analog dimming, the output current of each LED can be adjusted with 256 steps. In PWM dimming, the integrated 8-bit configurable PWM generator enables smooth brightness dimming control. Optional exponential PWM dimming can be activated for individual LED to achieve a human-eye-friendly visual performance.

The LP5810 integrates autonomous animation engine, with no need for brightness control commands from controller. Each LED has an individual animation engine which can be configured through the related registers. The device can generate a 6MHz clock signal, which synchronizes the lighting effects among multiple devices.

The LP5810 has 4 different material versions with different I^2C chip address. Up to 4 LP581x devices can be connected to the same I^2C bus and controlled individually. The LP5810 materials and corresponding chip addresses are shown in Section 4.

7.2 Functional Block Diagram

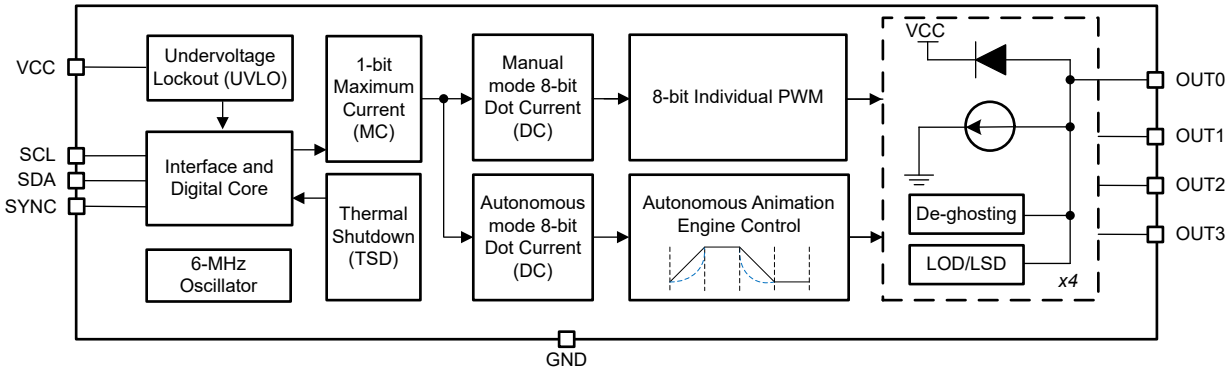

Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Analog Dimming

The current gain of each LED can be controlled by 2 methods to achieve analog dimming in the LP5810.

- Global 1-bit Maximum Current (MC) control for all LEDs without external resistor
- Individual 8-bit Dot Current (DC) control for each LED

The maximum output current I_{OUT_max} of each current sink can be programmed by the 1-bit max_current. The default value of max_current is 0h, which means the LED maximum current is set to 25.5mA in default.

Table 7-1. Maximum Current (MC) Bit Setting

1 bit Maximum Current (MC)		I_{OUT_MAX} (mA)
Binary	Decimal	
0 (default)	0 (default)	25.5 (default)
1	1	51

The LP5810 can individually adjust the peak current of each LED by using Dot Current (DC) function. The brightness deviation among the LED bins can be miminized, to achieve uniform display performance. The

current is adjusted with 256 steps from 0 to 100% of $I_{OUT_MAX.}$, which is programmed in an 8-bit register whose default value is 80h.

Table 7-2. Dot Current (DC) Bits Setting

8-bits Dot Current (DC) Register		Ratio of I_{OUT_MAX}
Binary	Decimal	
0000 0000	0	0%
0000 0001	1	0.39%
0000 0010	2	0.78%
---	---	---
1000 0000 (default)	128 (default)	50.2% (default)
---	---	---
1111 1101	253	99.2%
1111 1110	254	99.6%
1111 1111	255	100%

By configuring the MC and DC, the peak current of each current sink can be calculated as Equation 1:

$$I_{OUT}\left(mA\right) = I_{OUT_max} \times \frac{DC}{255} \tag{1}$$

The average current of each LED in TCM drive mode and mix drive mode is shown as Equation 2:

$$I_{AVE}\left(mA\right) = \frac{I_{OUT}}{N} \times \frac{DC}{255} \times D_{PWM} \tag{2}$$

- N is the total scan number setting.
- D_{PWM} is the PWM duty.

7.3.2 PWM Dimming

The LP5810 supports 8-bit PWM dimming with 24kHz or 12kHz frequency, which is configured by 'PWM_Fre' bit in Dev_config_1 register. An internal 6MHz oscillator is used to generate the PWM clock. SYNC pin can be configured as PWM clock input or output by configure 'vsync_out_en' bit in Dev_Config_11 register. If multiple LP5810 are used in the system with autonomous animation engine control, all devices can refer the same clock signal, which comes from one of LP5810 or external controller, to avoid animation mismatch in long time operation.

Each LED can be configured into 3 different PWM alignment phases: Forward, Middle, and Backward. The alignment phase of each LED is set by 'phase_align' bits in Dev_Config_7 to Dev_Config_10 registers. By turning on the LEDs in different phase, the peak current load from the system power supply is greatly decreased. The input current ripple and ceramic-capacitor audible ringing can also be reduced. Figure 7-2 shows the PWM alignment phases. In the forward alignment, the rising edge of PWM pulse is fixed at the beginning of PWM period. In the middle alignment, the middle point of PWM pulse is fixed at the middle of PWM period, while the pulse spreads to both directions. In the backward alignment, the falling edge of PWM pulse is fixed at the end of PWM period.

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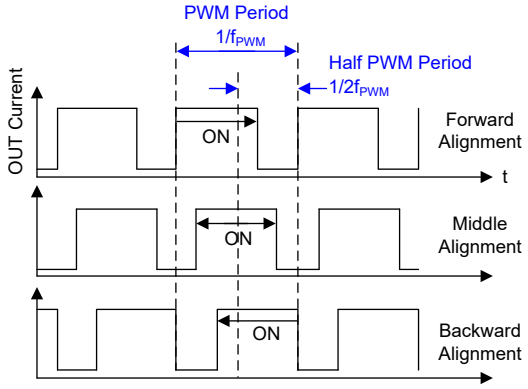

Figure 7-2. PWM Alignment Scheme

The LP5810 allow users to configure the dimming scale as exponential curve or linear curve, through the 'exp_en' bits in Dev_Config_5 and Dev_Config_6 registers. A human-eye-friendly visual performance can be achieved by using the internal exponential scale. The linear scale has great linearity between PWM duty cycle and PWM setting value, which provides flexible approach for external controlled gamma correction algorithm. The 8-bit linear and exponential curves are shown as Figure 7-3.

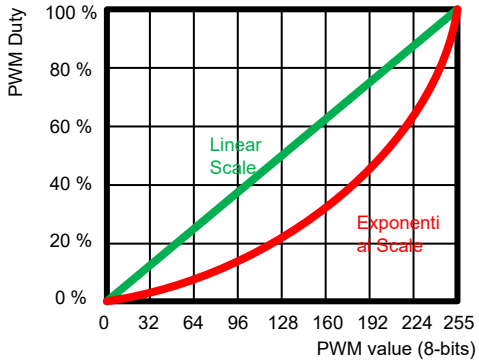

Figure 7-3. Linear and Exponential PWM Dimming Curves

7.3.3 Autonomous Animation Engine Control

The LP5810 supports both manual mode and autonomous mode to control the DC and PWM of each LED. In manual mode, the LEDs are directly controlled by the related configuration registers and reflect the value immediately. In autonomous mode, the autonomous animation engine is applied for each LED, which can realize vivid lighting effects without external processor control. The animation engine pattern is composed by 3 animation engine units (AEU) and 2 animation pause units (APU) for complex and flexible control. One AEU is formed by 4 slopers, which is used for fading effect.

After setting up all animation engine pattern configurations, sending start_cmd to the device can let the animation running autonomously, to free external controller real-time loading. The PWM value and unit status of each LED can be read from PWM_value registers and pattern_status registers. To make sure the precision of reading results, sending pause_cmd to pause the animation firstly is recommended.

7.3.3.1 Animation Engine Pattern

Each LED of the LP5810 has own animation engine, to achieve premium visual lighting effects. One whole animation engine pattern is defined as Figure 7-4. 3 animation engine units (AEU) and 2 animation pause units (APU) compose the animation engine pattern. AEU2 and AEU3 can be skipped by setting the playback times to 0. The LED current of each LEDs in the autonomous mode is set through the Autonomous_DC registers.

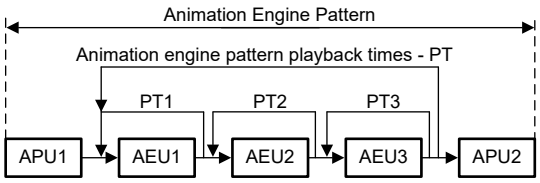

Figure 7-4. Animation engine pattern

The whole animation pattern includes two APUs and three AEUs with several playback times:

- APUx (x = 1, 2): Animation pause unit, each unit includes one timing value T.
- AEUx (x = 1, 2, 3): Animation engine unit, including 5 PWM values PWM1 to PWM5 and 4 time values T1 to T4.
- PT: Playback times of AEU1+AEU2+AEU3, which has 2-bit value to set 0/1/2/Infinite times.
- PTx: Playback times of AEUx (x=1/2/3), which has 2-bit value to set 0/1/2/Infinite times.

7.3.3.2 Sloper

Sloper is the basic element to achieve autonomous fade-in and fade-out animations. It can achieve 256 steps fade-in or fade-out effects from 'PWM_Start' to 'PWM_End' within a target time period T as Figure 7-5. The 8-bit PWM steps, which is configurable in animation pattern PWM setting registers, help to achieve extremely smooth effects. Exponential dimming curve can also be supported in the sloper.

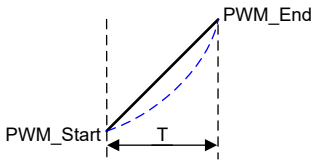

Figure 7-5. Sloper curve demonstration

The programable time T is selectable from 0 to around 8s with 16 levels shown in Table 7-3.

Table 7-3. Programable time options

Register value	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
Time (Typ.)	0s	0.09s	0.18s	0.36s	0.54s	0.80s	1.07s	1.52s	2.06s	2.50s	3.04s	4.02s	5.01s	5.99s	7.06s	8.05s

7.3.3.3 Animation Engine Unit (AEU)

The AEU is the most important unit to achieve autonomous animation effects. One AEU is formed by 4 slopers. There are 5 PWM values and 4 time values can be configured in the AEU. Each PWMx (x = 1, 2,…, 5) can be arbitrarily programmed from 0 to 255, The Tx (x = 1, 2, 3, 4) is selectable from 0 to 8s with 16 levels referring to Table 7-3. If two adjacent PWM values are equal, the brightness keeps unchange within the time setting. When a Tx is set to 0, this sloper is skipped. To avoid flicker happens due to PWM value suddenly changes, the begin and end PWM of this sloper need to be the same.

Typical breathing effect example is illustrated as Figure 7-6.

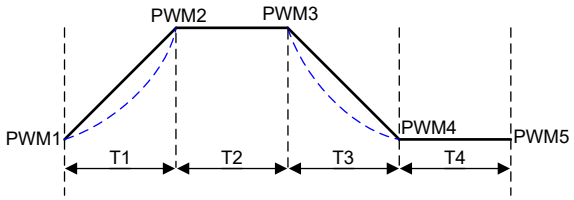

Figure 7-6. Animation engine unit - Example 1

Advanced breathing effect example is shown in Figure 7-7. 2 different fading speeds are set in the PWM rising and falling phases, to achieve a complex animation.

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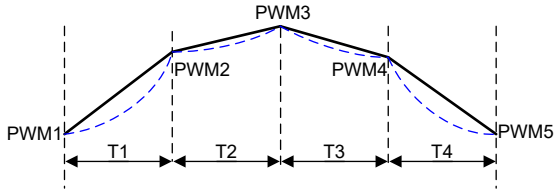

Figure 7-7. Animation engine unit - Example 2

7.3.3.4 Animation Pause Unit (APU)

The APU is defined as the pausing time at the beginning and the end of the animation pattern. The APU contains 1 time value which is selectable from 0 to 8s with 16 levels referring to Table 7-3. If the value is set as 0, the APU is skipped. The brightness of APU1 uses the PWM1 value of the AEU following the APU1, while the brightness of APU2 uses the PWM5 value of the AEU in front of APU2. One animation pattern example is shown in Figure 7-8. Only AEU2 is enabled in the pattern, so that the brightness of APU1 uses the PWM1 value of AEU2, and the brightness of APU2 uses PWM5 value of AEU2.

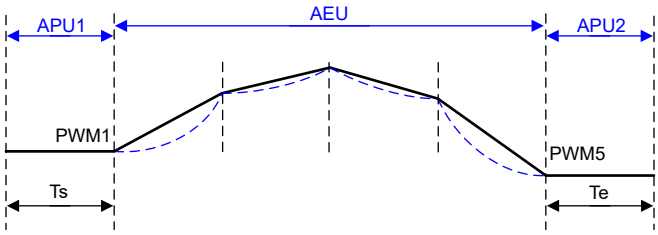

Figure 7-8. APU example

7.3.4 Protections and Diagnostics

7.3.4.1 LED Open Detections

The LP5810 integrates LED open detection (LOD) for the fault caused by any open LED. The threshold for LOD is 90mV when max current is set as 25.5mA, and 180 mV when max current is set as 51mA. To have enough detection time, LOD can only be performed when the PWM setting of this LED is above 25. If the voltage on the cathode of this LED is lower than the LOD threshold in continuously 3 cycles, LED open of this LED is reported to the corresponding LOD_status register.

The LOD flags can be cleared by writing 1h to 'lod_clear' bit in Fault_Clear register. If the LED open status is removed, the related 'lod_status' bit is set to 0 automatically.

The 'lod_action' bit in Dev_config_12 register can determine the action once open fault is detected. When the 'lod_action' bit is set to 1h, the dot where LED open happens is turned off to avoid any unpredictable issue. When the 'lod_action' bit is 0, no additional action is taken after LOD is detected. LED open fault detection and action is only executed in NORMAL state.

7.3.4.2 LED Short Detections

The LP5810 integrates LED short detection (LSD) for the fault caused by any short LED. The threshold of LSD is able to configure from (0.35 × VCC) V to (0.65 × VCC) V by configuring lsd_threshold in Dev_config_12 register. To have enough detection time, LSD can only be performed when the PWM setting of this LED is above 25. If the voltage on the cathode of this LED is higher than the LSD threshold in continuously 3 cycles, LED short of this LED is reported to the corresponding LSD_status register.

The LSD flags can be cleared by writing 1h to lsd_clear in Fault_CLR register. If the LED short status is removed, the related lsd_status bit is set to 0 automatically.

The 'lsd_action' bit in Dev_config_12 register can determine the reaction once open fault is detected. When the 'lsd_action' bit is set to 1h, all LEDs are turned off which is called one fails all fail (OFAF) action, to prevent potential damage caused by the short issue. The device enters to STANDBY state after sending 'lsd_clear' command. When the 'lsd_action' bit is 0, no additional action is taken after LSD is detected. LSD detecion is only executed in NORMAL state.

7.3.4.3 Thermal Shutdown

The LED driver of LP5810 goes into thermal shutdown state once the junction temperature exceeds 150°C. All LEDs turn off to avoid damaging the device. When the junction temperature drops below the thermal shutdown recovery temperature 130°C, the LED driver starts operating again.

7.4 Device Functional Modes

The Figure 7-9 shows the main state machine of the LED driver.

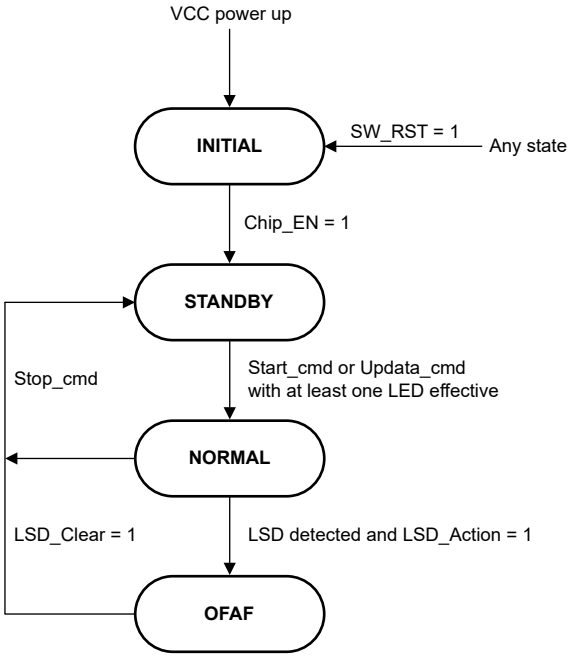

Figure 7-9. LP5810 functional modes

- INITIAL: The device enters into INITIAL after VCC power up.
- STANDBY: The device enters into STANDBY state from INITIAL when Chip_EN is set to 1. The device can also enter into STANDBY from NORMAL when no LED is effective, or Stop_cmd is received, or from OFAF when LSD_Clear = 1.
- NORMAL: The device enters NORMAL state from STANDBY when one or more LEDs are effective: for manual mode, at least one LED is enable (PWM and DC setting is not 0); for autonomous mode, at lease one LED is enable and Start_cmd is received.

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- OFAF: The device enters OFAF (one fail all fail) state when LED short is detected and LSD_Action =1. In OFAF mode, all LEDs are turned off. Once LSD_Clear is writen to 1, the device enters back to STANDBY state.

7.5 Programming

The LP5810 is compatible with I^{2}C standard specification. The device supports standard mode (100kHz maximum), fast mode (400kHz maximum), and fast plus mode (1MHz maximum). The device has 4 different chip address versions, which allows connecting up to four parallel devices in one I^{2}C bus.

I^{2}C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, the receiver must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

I^{2}C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5 bits of the chip address, 2 higher bits of the register address, and 1 read/write bit. The other 8 lower bits of register address are put in Address Byte 2.The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started. The Bit 4 and Bit 3 are determined by the device, which can refer to Section 4.

Table 7-4. I^{2}C Data Format

Address Byte1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	1	Bit 4	Bit 3	9th bit	8th bit	R: 1W: 0
Broadcast	1	1	0	1	1			
Address Byte2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit	0 bit

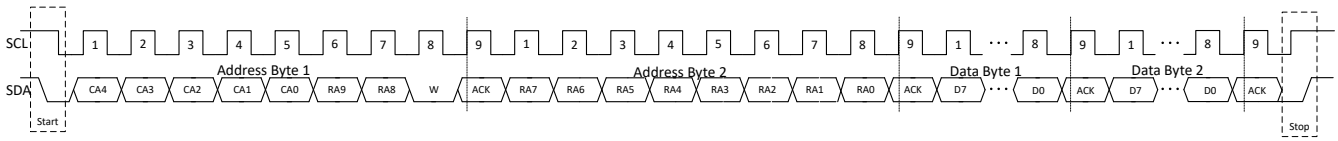

Figure 7-10. I^{2}C Write Timming

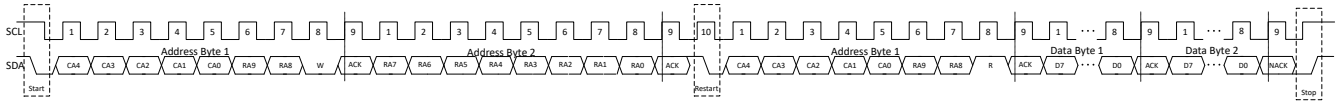

Figure 7-11. I^{2}C Read Timing

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7.5.1 I²C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, the receiver must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

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7.5.2 I²C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5 bits of the chip address, 2 higher bits of the register address, and 1 read/write bit. The other 8 lower bits of register address are put in Address Byte 2.The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started. The Bit 4 and Bit 3 are determined by the device, which can refer to Section 4.

Table 7-5. I²C Data Format

Address Byte1	Chip Address					Register Address		R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Independent	1	0	1	Bit 4	Bit 3	9th bit	8th bit	R: 1 W: 0
Broadcast	1	1	0	1	1			
Address Byte2	**Register Address**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit	0 bit

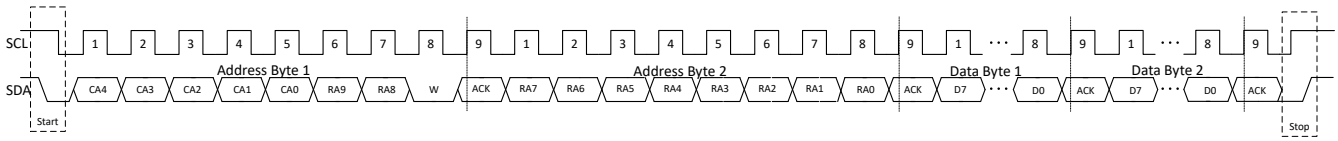

Figure 7-12. I²C Write Timming

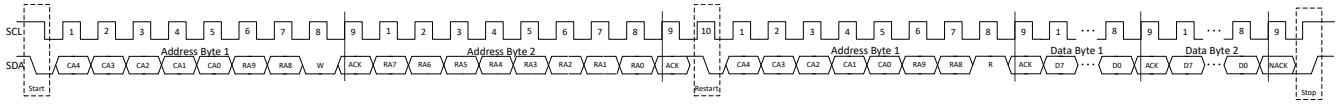

Figure 7-13. I²C Read Timing

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8 Register Maps

This section provides a summary of the LP5810 register maps.

Table 8-1. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Table 8-2. LP5810 Registers Map

Register Group	Register Acronym	Address(Hex.)	Function	Type
ChipEN	Chip_en	000	Chip enable	R/W
CONFIG	Dev_config0 ~ Dev_config12	001 ~ 00D	Device configuration registers	R/W
Update CMD	Update_cmd	010	Configuration update command: CONFIG registers will ONLY be effective by sending this command	R/W
Start CMD	Start_cmd	011	Autonomous control start command or restart with the latest setting	R/W
Stop CMD	Stop_cmd	012	LED driver stop command, LED driver goes to INITIAL state with this command from all the other states	R/W
Pause CMD	Pause_cmd	013	Autonomous control pause command	R/W
Continue CMD	Continue_cmd	014	Autonomous control continue command	R/W
LED EN	LED_EN1	020	LED enable registers	R/W
Fault CLR	Fault_Clear	022	Fault clear registers to clear TSD/LOD/LSD faults	R/W
RESET	Reset	023	Software reset	W
DC_Manual	DC0 ~ DC3	030 ~ 033	LED current setting at manual mode	R/W
PWM_Manual	PWM0 ~ PWM3	040 ~ 043	LED PWM setting at manual mode	R/W
DC_Auto	DC_Auto0 ~ DC_Auto3	050 ~ 053	LED current setting at autonomous mode	R/W
LED0 AEP	Tp, PT, PWM1 ~ PWM5, T1 ~ T4	080 ~ 099	LED0 Animation Engine Pattern parameters	R/W
LED1 AEP	Tp, PT, PWM1 ~ PWM5, T1 ~ T4	09A ~ 0B3	LED1 Animation Engine Pattern parameters	R/W
LED2 AEP	Tp, PT, PWM1 ~ PWM5, T1 ~ T4	0B4 ~ 0CD	LED2 Animation Engine Pattern parameters	R/W
LED3 AEP	Tp, PT, PWM1 ~ PWM5, T1 ~ T4	0CE ~ 0E7	LED3 Animation Engine Pattern parameters	R/W

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Table 8-2. LP5810 Registers Map (continued)

STATUS	TSD_Config_Status	300	TSD status and Configuration error indication register	R
	LOD_Status1 ~ LOD_Status2	301 ~ 302	LOD status registers	R
	LSD_Status1 ~ LSD_Status2	303 ~ 304	LSD status registers	R
	PWM_Internal0 ~ PWM_Internal_D2	305 ~ 314	Internal PWM values for LED0 ~ LED_D2	R
	PATTERN_Status1 ~ PATTERN_Status8	315 ~ 31C	AEP status registers to indicate pattern progress for LED0 ~ LED_D2	R

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LP5810 is a 4ch RGB LED driver with autonomous animation engine control. The LP5810 has ultra-low operation current at active mode, and it only consumes 0.4mA when LED current is set at 25mA. In battery powered applications like e-tag, earbud, e-cigarettes, VR headset, RGB mouse, smart speaker, and other handheld devices, LP5810 is designed to provide premium LED lighting effects with low power consumption and small package.

9.2 Typical Application

9.2.1 Application

Figure 9-1 shows an example of typical application, which uses one LP5810 to drive RGBW LEDs through I^2C communication.

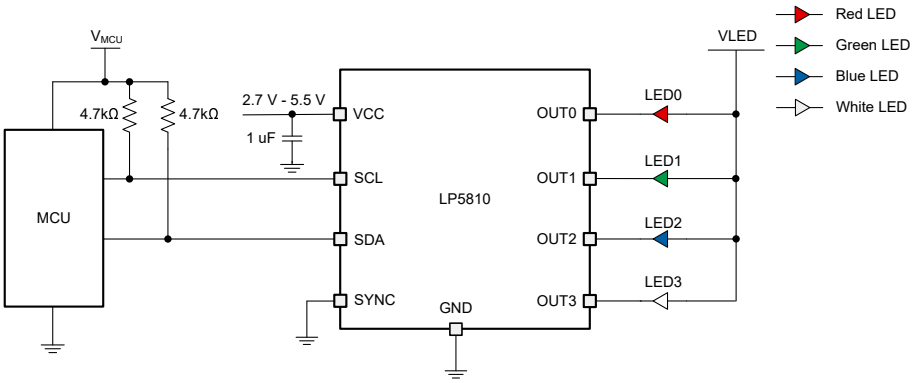

Figure 9-1. Typical Application - LP5810 Driving RGBW LEDs

9.2.2 Design Parameters

Design Parameters shows the typical design parameters of Figure 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input voltage	3.6V to 4.2V by one Li-on battery cell
LED count	4
LED maximum average current (red, green, blue, white)	51mA, 40.8mA, 40.8mA, 40.8mA
LED PWM frequency	24kHz

9.2.3 Detailed Design Procedure

This section showcases the detailed design procedures for LP5810 including components selection, LED driver manual and autonomous modes application examples.

9.2.3.1 Input Capacitor Selection

Input capacitors must be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, large capacitance is used to reduce input current ripple. When the input power is supplied through long wire and only ceramic capacitor is put, the load step at the output induces ringing at the VCC pin. This ringing couples back to the output and influence loop stability or even damage the device. In this circumstance, placing additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power supply can reduce the ringing

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9.2.3.2 Program Procedure

After VCC powering up, the device can be initialized by configuring chip_en = 1 after executing I^{2}C target addressing. Then the CONFIG registers can be set to the excepted configuration. After updating the CONFIG registers, one update command must to be sent to make the configuration effective. Either manual mode or autonomous mode can be selected for each LED. A new configuration is only effective once update command is received.

The detailed program procedure is illustrated as:

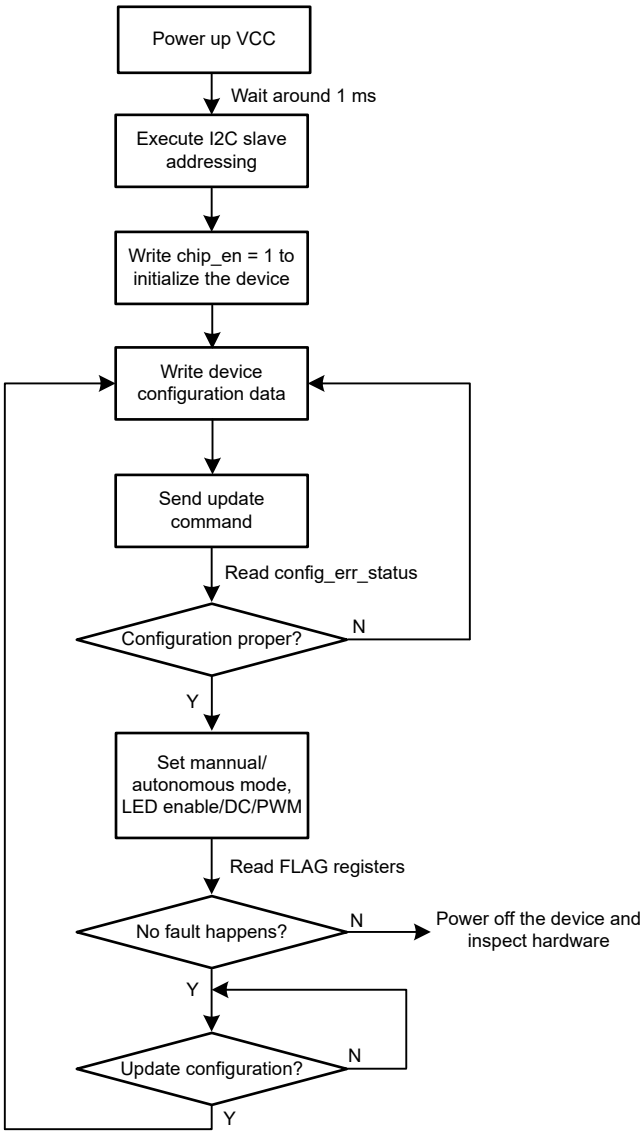

Figure 9-2. Program Procedure

9.2.3.3 Programming Example

To get the design parameters in Section 9.2.2, the following program steps can be referred.

After VCC powering up and waiting around 1ms,

1. Execute I^{2}C target addressing, for details refer to the sample code
2. Set chip_en = 1 to enable the device (**Write 01h to register 000h**)

3. Set max_current = 1h to set 51mA maximum output LED current (**Write 01h to register 001h**)
4. Set lsd_threshold = 3h is recommended to avoid incorrect LSD detection (**Write 0Bh to register 00Dh**). Leave the PWM frequency, manual or autonomous mode, linear or exponential dimming curve, phase align method, vsync mode settings as default (In other application requirements, these functions can be set)
5. Send update command to complete configuration settings (**Write 55h to register 010h**)
6. Read back config_err_status to check if the configuration is proper (**Read register 300h**)
7. Enable all 4 LEDs (**Write 0Fh to register 020h**)
8. Set 51mA peak current for red LEDs, 40mA peak current for green, blue and white LEDs (**write FFh to register 30h, write CCh to registers 031h - 033h**)
9. Set 100% duty cycle to illuminate the LEDs (**Write FFh to registers 040h - 043h**)

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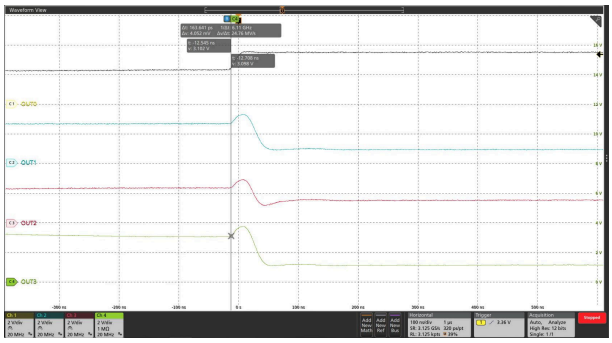
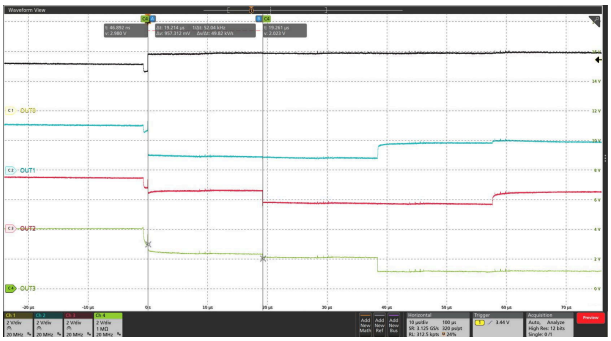
9.2.4 Application Performance Plots

The following figures show the application performance plots.



phase_align_a0 = 0h, phase_align_a1 = 0h, phase_align_a2 = 0h, PWM = 127

Figure 9-3. PWM Alignment Disabled



phase_align_a0 = 1h, phase_align_a1 = 2h, phase_align_a2 = 3h, PWM = 127

Figure 9-4. PWM Alignment Enabled

9.3 Power Supply Recommendations

The LP5810 can also work normally by powering from VCC with 2.7V to 5.5V voltage range and an external LED supply with 2.7V to 5.5V voltage range is supported to power up the LEDs in direct drive configurations.

9.4 Layout

9.4.1 Layout Guidelines

The input capacitor needs not only to be close to the VCC pin, but also to the GND pin in order to reduce input supply ripple. For OUTx (x = 0, 1, 2, 3), low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of adjacent outputs must be short and wide and avoid parallel wiring and narrow trace. For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

9.4.2 Layout Example

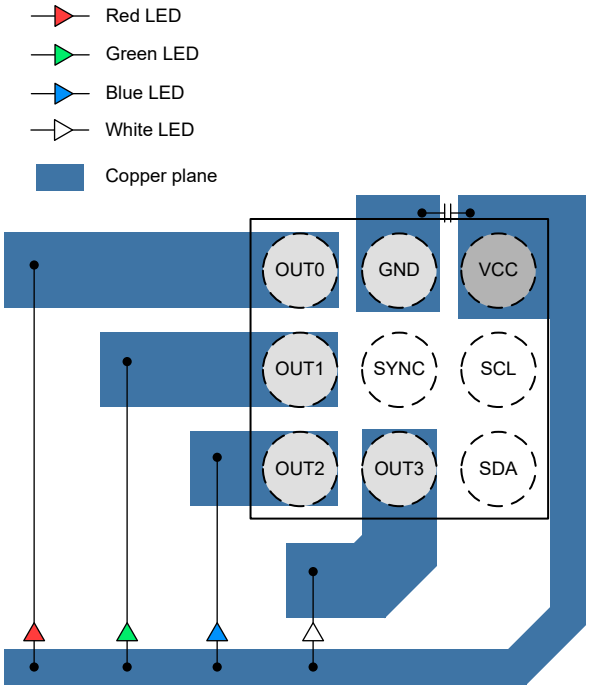


Figure 9-5. LP5810 DSBGA Package Layout Example

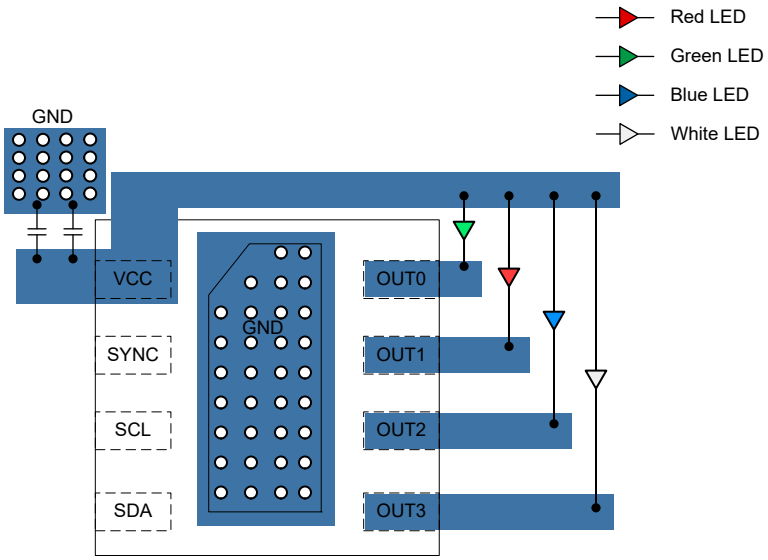


Figure 9-6. LP5810 WSON Package Layout Example

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2025) to Revision E (September 2026)	Page
• Add the body diode of the scan switch FET	11

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Changes from Revision C (December 2024) to Revision D (February 2025)	Page
• Added URL to Sample Code	25

Changes from Revision B (September 2024) to Revision C (December 2024)	Page
• Added Pin Configuration Section	4
• Removed EN on parameter from Reccomended Operating Conditions Table	6
• Removed V_{EN_H} and V_{EN_L} on parameter from Electrical Characteristics Table	6
• Updated Functional Modes image	16
• Updated parameters in Design Parameters table	24
• Changed Program Procedure	25
• Changed Program Example	25
• Removed Scan Lines and Current Sinks Waveforms of OUT0, OUT1, OUT2, OUT3, removed Scan Lines Switching Waveforms of OUT0, OUT1, OUT2, OUT3	27

Changes from Revision A (November 2023) to Revision B (September 2024)	Page
• Updated Body size from 1.43mm to 1.43mm to 1.43mm to 1.34mm	1
• Updated Absolute Maximum Ratings Table	6
• Updated Reccomended Operating Conditions Table	6
• Updated Thermal Information Table	6
• Updated Electrical Specifications Table	6

Changes from Revision * (November 2023) to Revision A (November 2023)	Page
• Changed document status from "Advance Information" to "Production Data"	1
• Added Programming Example	25

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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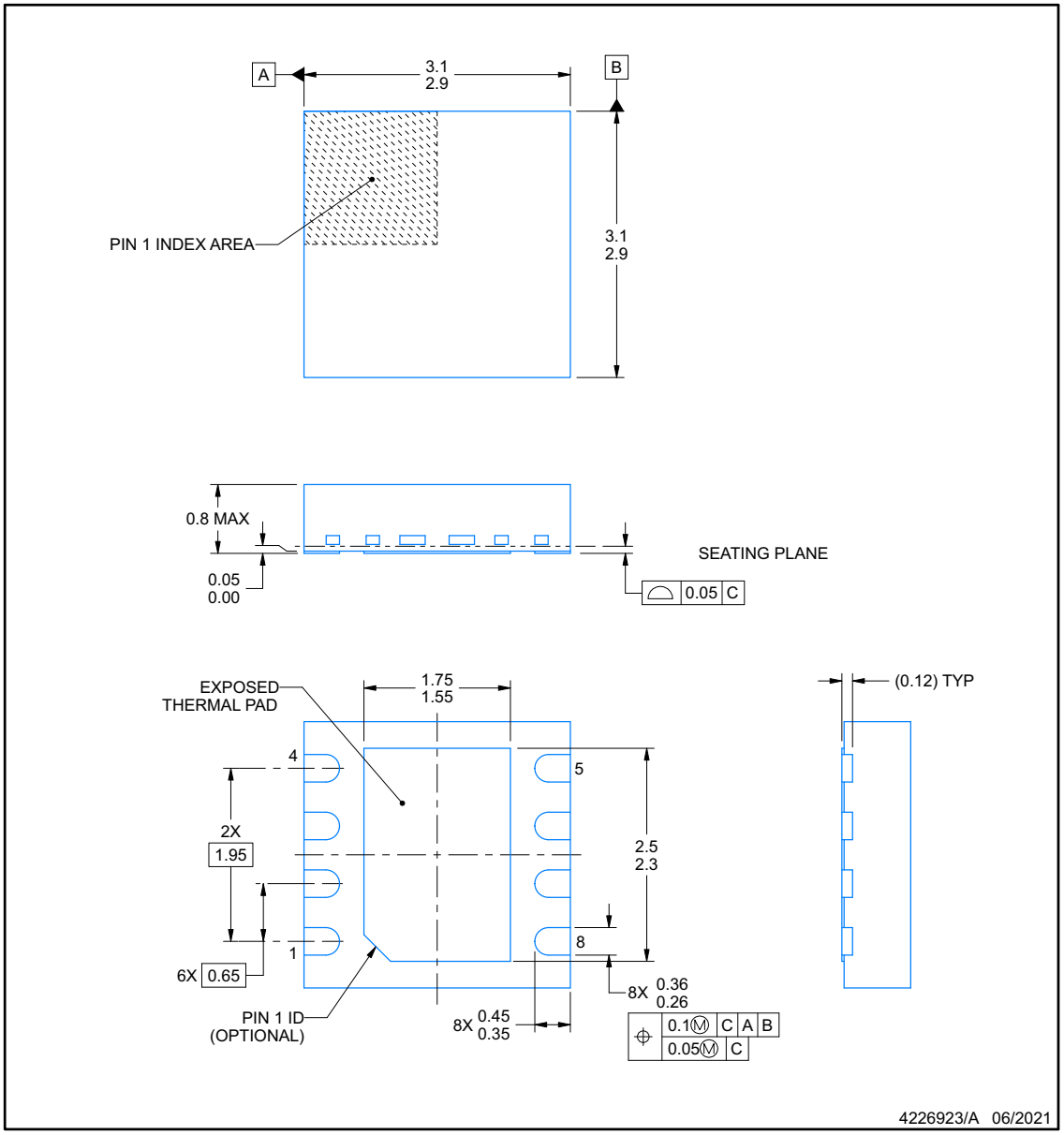
PACKAGE OUTLINE

DSD0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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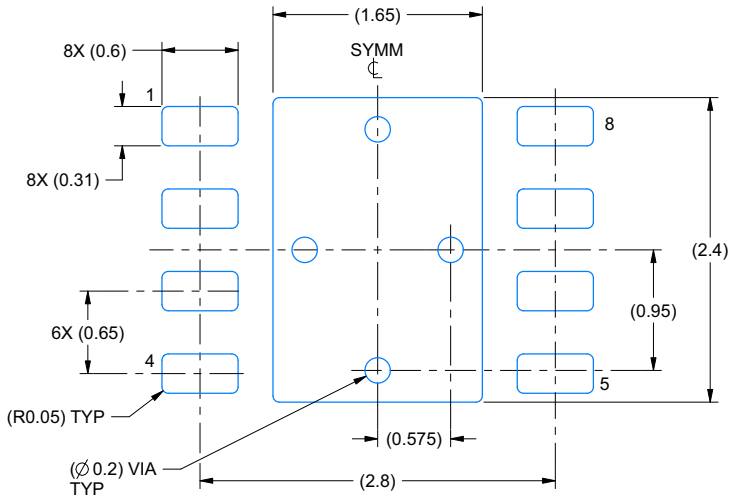
EXAMPLE BOARD LAYOUT

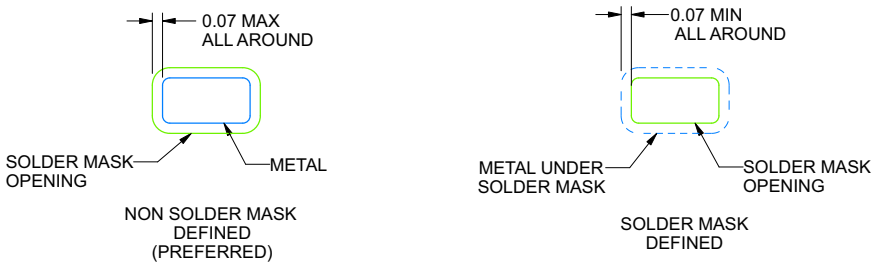
DSD0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4226923/A 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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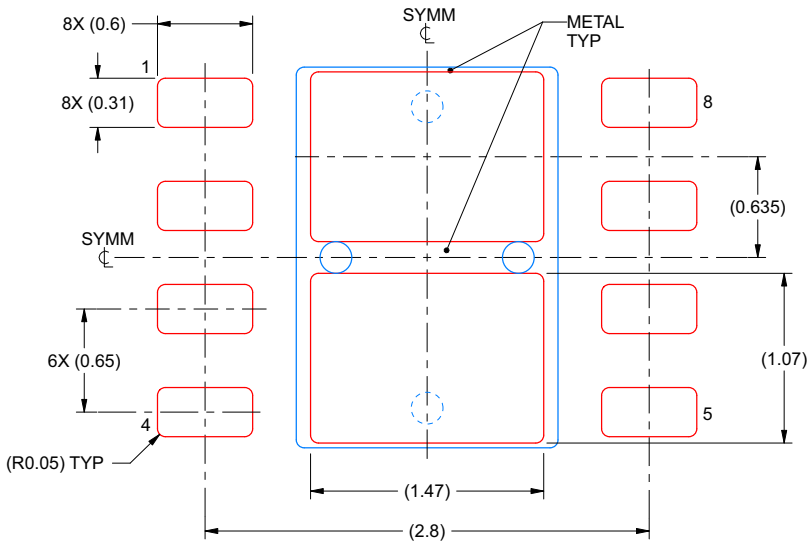
EXAMPLE STENCIL DESIGN

DSD0008B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226923/A 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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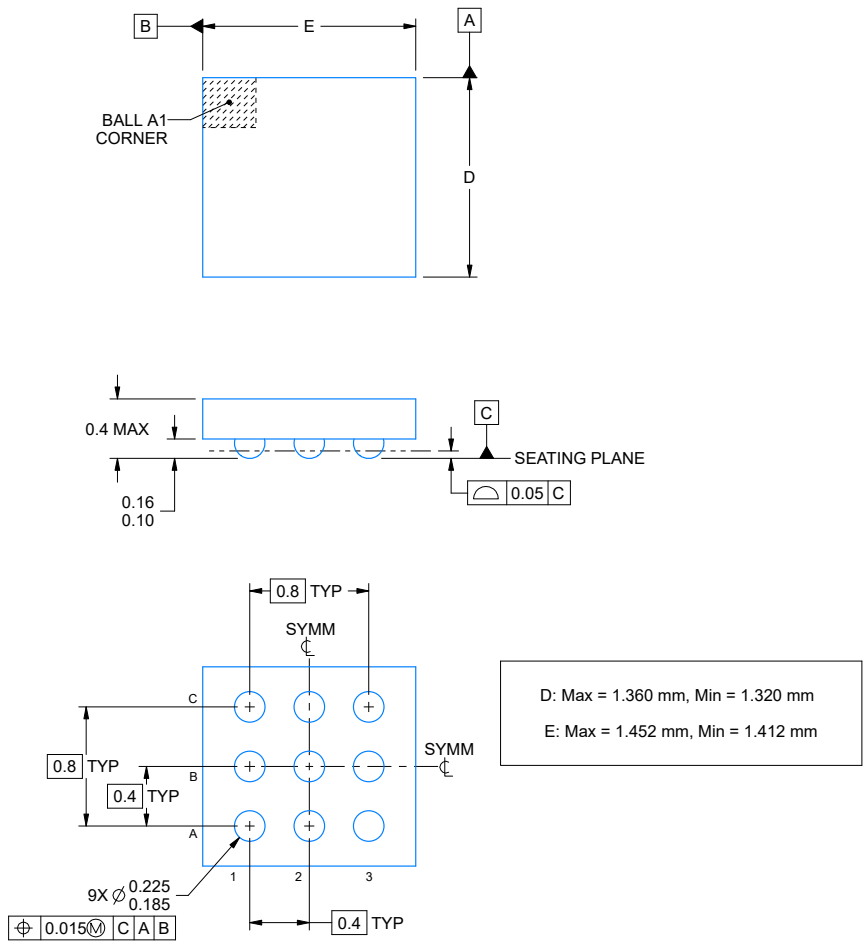
PACKAGE OUTLINE

YBH0009-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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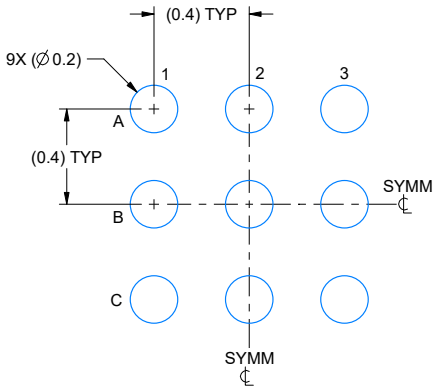
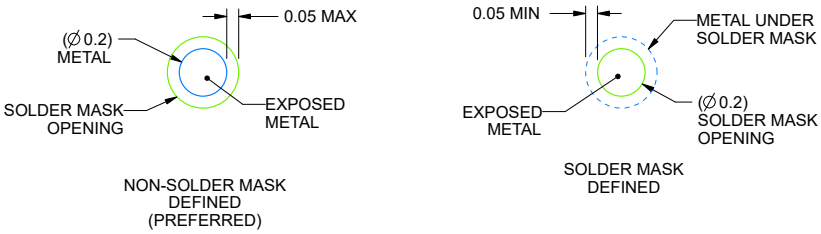
EXAMPLE BOARD LAYOUT

YBH0009-C01 **DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4228370/C 01/2023

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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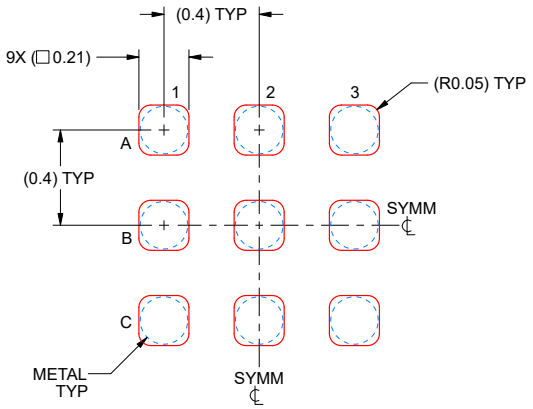
EXAMPLE STENCIL DESIGN

YBH0009-C01 **DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4228370/C 01/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5810ADSDR	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810A
LP5810ADSDR.A	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810A
LP5810AYBHR	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810A
LP5810AYBHR.A	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810A
LP5810BDSDR	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810B
LP5810BDSDR.A	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810B
LP5810BYBHR	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810B
LP5810BYBHR.A	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810B
LP5810CDSDR	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810C
LP5810CDSDR.A	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810C
LP5810CYBHR	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810C
LP5810CYBHR.A	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810C
LP5810DDSDR	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810D
LP5810DDSDR.A	Active	Production	SON (DSD) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5810D
LP5810DYBHR	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810D
LP5810DYBHR.A	Active	Production	DSBGA (YBH) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5810D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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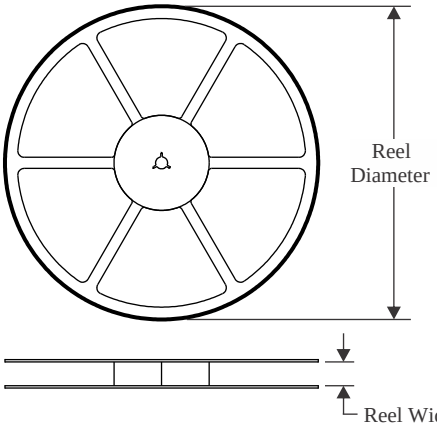
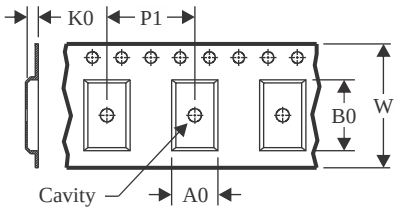
TAPE AND REEL INFORMATION

REEL DIMENSIONS

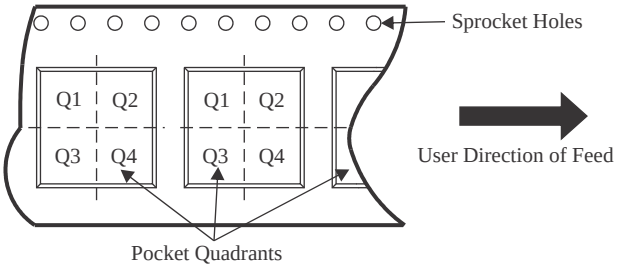


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

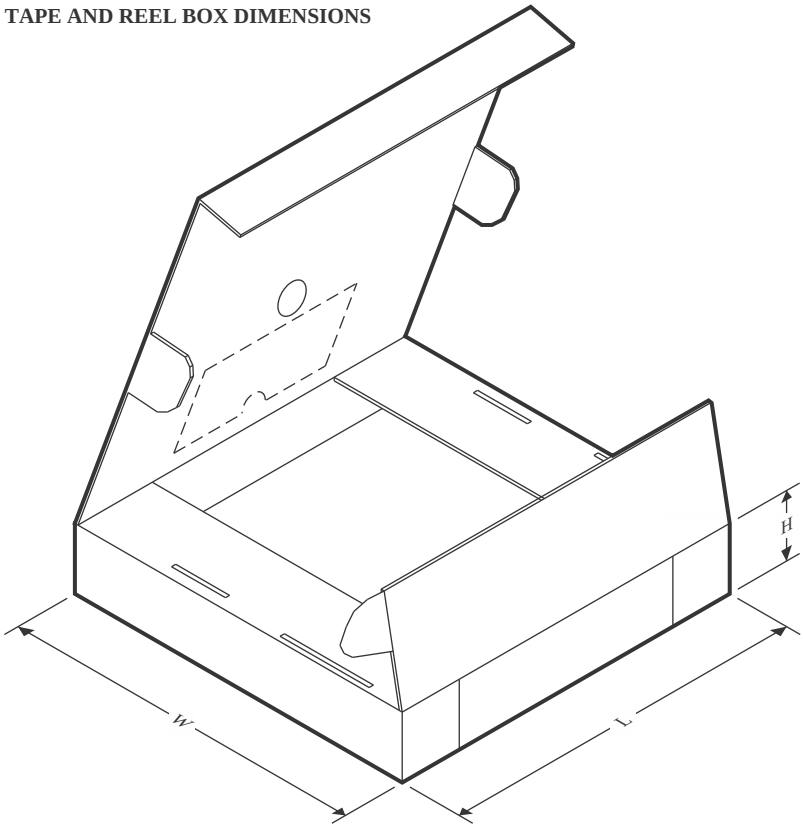
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5810ADSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5810AYBHR	DSBGA	YBH	9	3000	180.0	8.4	1.47	1.56	0.51	4.0	8.0	Q2
LP5810BDSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5810BYBHR	DSBGA	YBH	9	3000	180.0	8.4	1.47	1.56	0.51	4.0	8.0	Q2
LP5810CDSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5810CYBHR	DSBGA	YBH	9	3000	180.0	8.4	1.47	1.56	0.51	4.0	8.0	Q2
LP5810DDSDR	SON	DSD	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP5810DYBHR	DSBGA	YBH	9	3000	180.0	8.4	1.47	1.56	0.51	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5810ADSDR	SON	DSD	8	3000	360.0	360.0	36.0
LP5810AYBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0
LP5810BDSDR	SON	DSD	8	3000	360.0	360.0	36.0
LP5810BYBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0
LP5810CDSDR	SON	DSD	8	3000	360.0	360.0	36.0
LP5810CYBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0
LP5810DDSDR	SON	DSD	8	3000	360.0	360.0	36.0
LP5810DYBHR	DSBGA	YBH	9	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

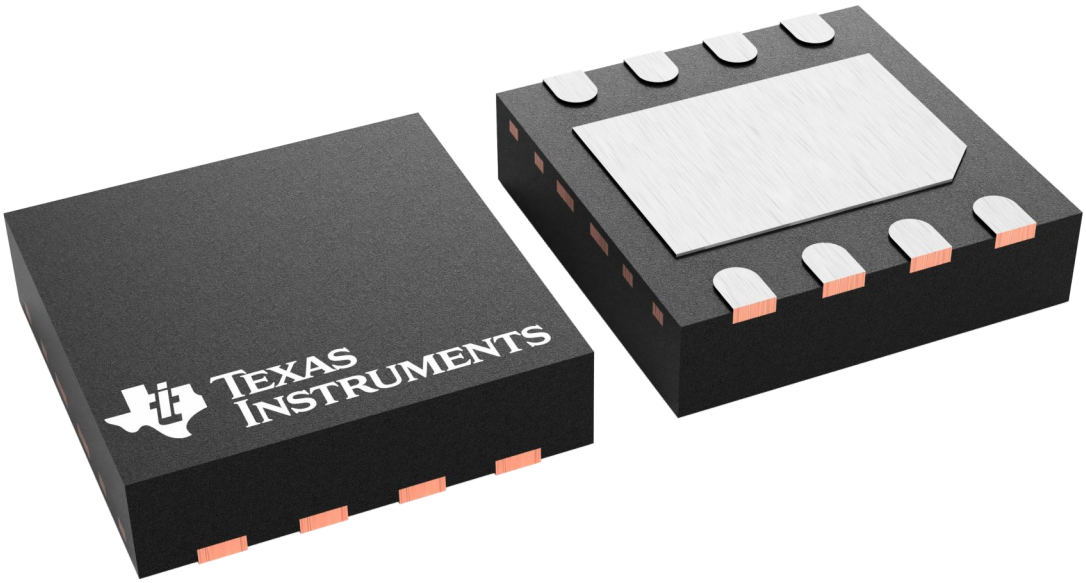
DSD 8

WSON - 0.8 mm max height

3 X 3, 0.8 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227007/A

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