LM656x0-Q1 Automotive, 65V, 8A/6A/4A, Synchronous Buck DC/DC Converter Family With Mitigated Interference and Noise Technology (MINT)

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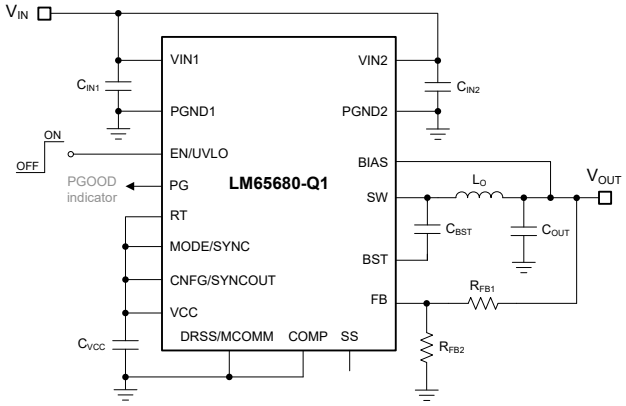
1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid ISO 26262 system design
- Versatile synchronous buck converter family
  - Wide V_{IN} range of 3.5V to 65V (70V transients)
  - Meets LV148 / ISO21780 requirements
  - 4A, 6A, and 8A output current options
  - Adjustable output voltage from 0.8V to 60V, or fixed output options of 3.3V and 5V
- Mitigated interference and noise technology – architecture 1 (MINT 1)
  - Facilitates CISPR 25 Class 5 compliance
  - Enhanced HotRod™ QFN (eQFN) package with symmetrical pinout design and minimal L_{LOOP}
  - Spread Spectrum (DRSS) and switching slew-rate control reduce peak emissions
  - Switching frequency from 300kHz to 2.2MHz
- High efficiency across the full load current range
  - 95% at 48V_{IN}, 12V_{OUT}, 8A, 400kHz
  - Multiphase stackable for higher output current
  - Dual-input VCC subregulator with BIAS option
- Improved reliability with optimized pinout design and clearance for short-circuit-to-adjacent-pin test
- Create a custom design using the LM656x0-Q1 with the WEBENCH® Power Designer

2 Applications

- LIDAR, ADAS, automotive display
- Automotive infotainment and cluster
- Hybrid, electric, and powertrain systems



Typical Schematic

3 Description

The LM656x0-Q1 is a synchronous buck DC/DC converter offered from a family of devices with mitigated interference and noise technology using architecture 1 features (MINT 1) that enable low EMI, high power density, and excellent conversion efficiency. Integrated power MOSFETs with low $R_{DS(on)}$ enable up to 8A of output current across a wide V_{IN} range of 3.5V to 65V (with transients to 70V).

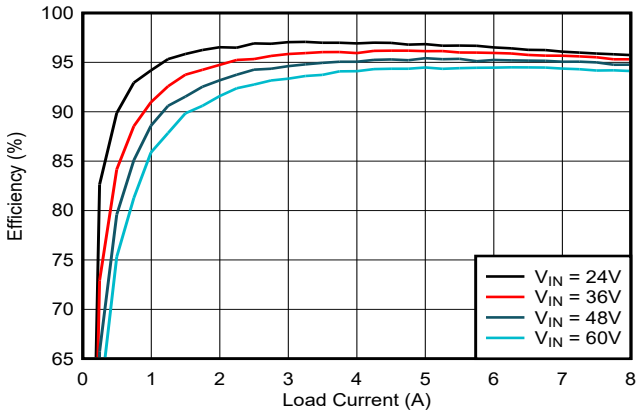
Phase stackable with synchronized interleaving, the peak current-mode control architecture of the LM656x0-Q1 supports accurate current sharing with paralleled phases for higher output currents. AUTO mode enables frequency foldback during light-load operation, giving high light-load efficiency and a no-load input current as low as 2.2µA, which extends operating run-time in battery-powered systems.

A high-side switch minimum on-time of 36ns facilitates large step-down ratios, enabling the direct conversion from 24V or 48V automotive inputs to low-voltage rails for reduced system cost and complexity. The package has several NC pins between critical power pins, which improve the Failure Modes and Effects Analysis (FMEA) result.

Device Information

PART NUMBER	PACKAGE(1)	RATED CURRENT(2)
LM65680-Q1	RZY (WQFN-FCRLF, 26)	8A
LM65660-Q1 (3)		6A
LM65640-Q1 (3)		4A

(1) For more information, see Section 11.
(2) See the *Related Products* table.
(3) Preview information (not Advance Information).



LM65680-Q1 Efficiency, V_{OUT} = 12V, F_{SW} = 400kHz

The LM656x0-Q1 includes several features to simplify compliance with CISPR 25 and automotive emissions requirements. First, a symmetrical pinout provides excellent input capacitor placement and enables an ultra-low effective value for the power-loop parasitic inductance, which reduces switching losses and improves EMI performance at high input voltage and high switching frequency. A pin-selectable switch-node slew-rate control feature further reduces emissions at high frequencies. To lower input capacitor ripple current and EMI filter size, interleaved operation using a SYNCOUT signal with 180° phase shift works well for cascaded, multichannel or multiphase designs. Resistor-adjustable switching frequency as high as 2.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. Finally, the LM656x0-Q1 has dual-random spread spectrum (DRSS), a unique EMI-reduction feature that combines low-frequency triangular and high-frequency random modulations to mitigate disturbances across lower and higher frequency bands, respectively.

Additional features of the LM656x0-Q1 include 150°C maximum junction temperature operation, open-drain power-good (PG) indicator for fault reporting and output voltage monitoring, precision enable input for input UVLO protection, monotonic start-up into prebiased loads, dual-input VCC bias subregulator powered from VIN or BIAS, hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The LM656x0-Q1 is qualified to AEC-Q100 grade 1 for automotive applications and comes in a 4.5mm × 4.5mm, thermally enhanced, 26-pin eQFN package with additional pin clearance for increased reliability. Also included are wettable-flank pins to facilitate optical inspection during manufacturing. Leveraging a flip-chip routable leadframe (FCRLF) packaging technique, the LM656x0-Q1 with useable current, lifetime reliability, and cost advantages targets applications requiring high power density. The wide input voltage range, low quiescent current consumption, high-temperature operation, cycle-by-cycle current limit, low EMI signature, and small design size provide an excellent point-of-load regulator design for applications requiring enhanced robustness and durability.

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4 Related Products

Table 4-1. Orderable Part Numbers

GENERAL PART NUMBER	ORDERABLE PART NUMBER	INPUT VOLTAGE RANGE	RATED CURRENT	TI FUNCTIONAL-SAFETY CLASSIFICATION(2)	LEVEL SHIFTERS FOR IBB
LM65680-Q1	LM65680RZYRQ1	3.5V to 65V	8A	Functional safety-capable	No
LM65660-Q1(1)	LM65660RZYRQ1		6A		
LM65640-Q1(1)	LM65640RZYRQ1		4A		
LM68680-Q1(1)	LM68680FRZYRQ1	3.5V to 65V	8A	ASIL C functional safety-compliant	No
LM68660-Q1(1)	LM68660FRZYRQ1		6A		
LM68640-Q1(1)	LM68640FRZYRQ1		4A		
LM68580-Q1(1)	LM68580FRZYRQ1	3.5V to 42V	8A		
LM68580-Q1(1)	LM68560FRZYRQ1		6A		
LM67680-Q1	LM67680RZYRQ1	3.8V to (65V – $\lvert V_{OUT} \rvert$)	8A	Functional safety-capable	Yes
LM67660-Q1(1)	LM67660RZYRQ1		6A		
LM67640-Q1	LM67640RZYRQ1		4A		

(1) Preview information (not Advance Information). For more information, please contact TI.
(2) Refer to the functional safety homepage to understand the TI functional safety classifications (in terms of the development process, analysis report, and diagnostics description).

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5 Pin Configuration and Functions

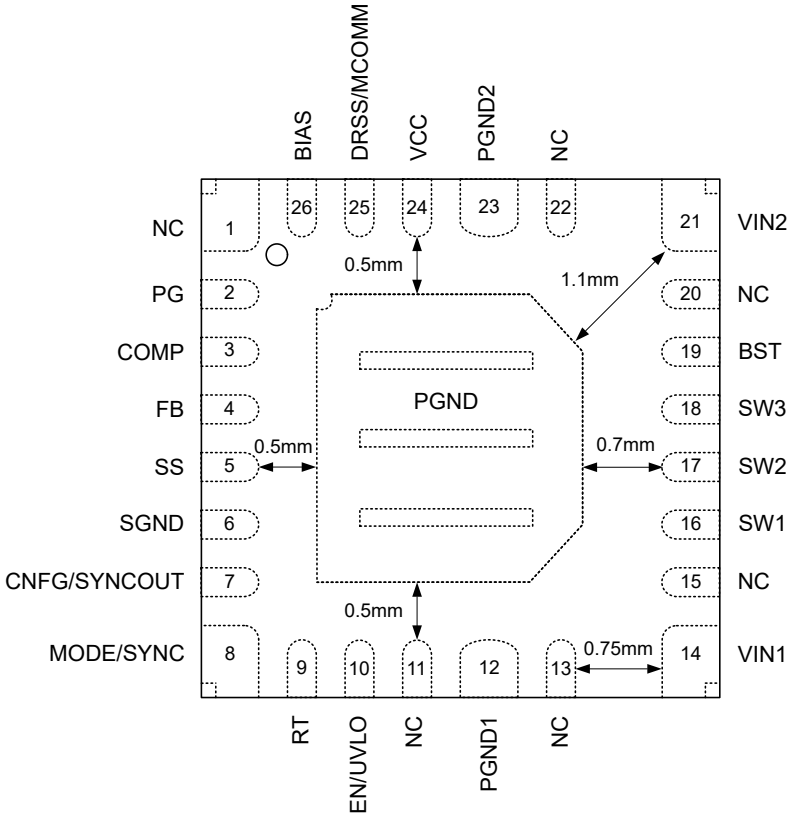

Figure 5-1. RZY 26-Pin WQFN-FCRLF Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1	—	No connect pin. Leave open.
PG	2	O	Power-Good output pin. PG is an open-drain output that goes low if the output voltage is outside of the specified regulation window.
COMP	3	A	External compensation pin. COMP is the output of the transconductance error amplifier. If used, connect a compensation network from COMP to PGND. If unused, tie COMP to PGND or leave open.
FB	4	A	Feedback pin. Connect a resistor divider from VOUT to PGND to set the output voltage setpoint between 0.8V and 60V. Connect FB to VCC or PGND to configure 5V or 3.3V fixed output voltage, respectively. The FB regulation voltage is 0.8V.
SS	5	A	Soft-start ramp programming pin. If SS is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 5.3ms. Set the soft-start time to a higher value by connecting a capacitor from SS to PGND.
SGND	6	G	System GND pin. Connect to the system ground.
CNFG/SYNCOUT	7	I/O	Configuration pin. CNFG/SYNCOUT configures the device as a primary (single-phase or two-phase operation) or a secondary (two-phase operation) and selects internal (single-phase operation only) or external compensation (single-phase or two-phase operation). When configured as a primary for two-phase operation, the pin becomes a SYNCOUT pin after start-up.
MODE/SYNC	8	I	Mode and synchronization input pin. Tie MODE/SYNC to PGND or drive low to operate in AUTO mode. Tie MODE/SYNC to VCC or drive high, or send a synchronization clock signal to operate in FPWM mode. When synchronized to an external clock, use RT to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off.

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Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RT	9	A	Switching frequency programming pin. Connect RT to PGND using a resistor with a value between 6.81kΩ and 54.2kΩ to set the switching frequency between 300kHz and 2.2MHz. Connect to VCC or PGND for fixed 400kHz or 2.2MHz operation, respectively. Do not leave RT open.
EN/UVLO	10	I	Precision enable pin. Drive EN/UVLO high or low to enable or disable the device, respectively. EN/UVLO can directly connect to VIN. Use EN/UVLO with a resistor divider from VIN for adjustable input voltage UVLO. Do not leave EN/UVLO open.
NC	11	—	No connect pin. Leave open.
PGND1	12	G	Power ground to the internal low-side MOSFET. Connect this pin to the system ground. Provide a low-impedance connection to PGND2. Connect a high-quality bypass capacitor from VIN1 to PGND1.
NC	13	—	No connect pin. Leave open to maintain 1mm clearance between the VIN1 and PGND1 pins. Tying NC to PGND1 is possible provided that the 0.75mm clearance between VIN1 and PGND1 meets the system pin-clearance requirements.
VIN1	14	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from VIN1 to PGND1. Provide a low-impedance connection to VIN2.
NC	15	—	No connect pin. Leave open to maintain 0.5mm clearance between VIN1 and SW1.
SW1	16	P	Device switch pins and the switch node of the regulator. Connect to the power-stage inductor.
SW2	17		
SW3	18		
BST	19	P	High-side driver supply rail. Connect a 100nF capacitor between SW and BST. An internal diode charges the capacitor while SW is low.
NC	20	—	No connect pin. Leave floating to maintain 0.5mm clearance between VIN2 and BST.
VIN2	21	P	Input supply to the regulator. Connect a high-quality bypass capacitor from VIN2 to PGND2. Provide a low-impedance connection to VIN1.
NC	22	—	No connect pin. Leave open to maintain 1mm clearance between VIN2 and PGND2 pins. Tying NC to PGND2 is possible provided that the 0.75mm clearance between VIN2 and PGND2 pins meets the system pin-clearance requirements.
PGND2	23	G	Power ground to the internal low-side MOSFET. Connect to the system ground. Provide a low-impedance connection to PGND1. Connect a high-quality bypass capacitor from VIN2 to PGND2.
VCC	24	P	Internal regulator output. Used as a supply to the internal control circuits. Connect a high-quality 1µF capacitor from VCC to PGND. Do not connect VCC to any external loads.
DRSS/MCOMM	25	I/O	Dual Random Spread Spectrum (DRSS) select pin. See *Dual-Random Spread Spectrum (DRSS)* for available DRSS options. When configured for two-phase operation, DRSS/MCOMM becomes a mode communication pin between the primary and secondary devices. Connect the DRSS/MCOMM pins of the primary and secondary.
BIAS	26	P	Input to the internal VCC regulator. For fixed output configurations of 3.3V or 5V, connect BIAS to the V_{OUT} node for output voltage sensing. For adjustable output configurations, connect BIAS to the V_{OUT} node or to an external bias supply from 3.3V to 30V. If the output voltage is above 30V and an external bias supply is not available, tie BIAS to PGND.
PGND	—	G	Exposed PGND pad. Connect to system GND on the PCB. This pad is a major heat dissipation path for the device. Use the pad for heatsinking by soldering to a large copper area on the PCB. Implement as many thermal vias as suggested in the example board layout to reduce package thermal resistance and improve thermal performance.

(1) P = Power, G = Ground, A = Analog, I = Input, O = Output.

5.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (QFN) packages do not have solderable or exposed pins and terminals that are easily viewed. Visually determining whether or not the package is successfully soldered onto the printed-circuit board (PCB) is therefore difficult. The wettable-flank process is developed to resolve the issue of side-lead wetting of leadless packaging. The LM656x0-Q1 is assembled using a 26-pin Enhanced HotRod WQFN package with dimple wettable flanks that allow side-lead solder inspection during manufacturing. This visual indicator of solderability reduces inspection time and manufacturing costs.

5.2 Pinout Design for Clearance and FMEA

As shown in Figure 5-1, the LM656x0-Q1 has a carefully designed pinout arrangement that provides clearance spacing of at least 0.7mm between high-voltage pins (VIN, SW, and BST) and ground (PGND) to meet IPC-2221B and IPC-9592B external conductor clearance rules. The clearance from VIN1 and VIN2 to the PGND DAP is 1.1mm. The clearance from SW1, SW2, SW3, and BST to the PGND DAP is 0.7mm. In addition, NC (no-connect) pins separate VIN1 and PGND1, VIN2 and PGND2, VIN2 to BST, and BIAS to PG.

Moreover, the pinout is designed for critical automotive applications with stricter quality, safety, and reliability requirements. In terms of pin FMEA (failure mode effects analysis), the typical failure scenarios considered include short circuit to ground, short circuit to input supply (VIN), short circuit to an adjacent pin, and if a pin is left open circuit. These faults are considered as applied external to the IC and therefore designated as board-level failures rather than IC-level reliability failures. Example sources of such faults are stray conductive filaments causing pin-to-pin shorts or a board manufacturing defect causing an open-circuit track.

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	72	V
	EN/UVLO TO PGND	–0.3	72	V
	RT to PGND	–0.3	72	V
	DRSS/MCOMM to PGND	–0.3	40	V
	BIAS TO PGND	–0.3	40	V
	CNFG/SYNCOUT to PGND	–0.3	5.5	V
Output voltage	SW to PGND	–0.6	V_{VIN}	V
	SW to PGND, <10ns transient	–5	V_{VIN}	V
	PG to PGND	–0.3	40	V
	BST to SW	–0.3	5.5	V
	VCC to PGND	–0.3	5.5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).(1)

		MIN	MAX	UNIT
Input voltage	VIN (DC)	3.5	65	V
	EN/UVLO (DC)	0	65	V
Input voltage	VIN (≤ 100ms transients, ≤ 1% duty) (2)	3.5	70	V
Input voltage	EN/UVLO (≤ 100ms transients, ≤ 1% duty) (2)	0	70	V
Input voltage	BIAS, PG	0	30	V
	MODE/SYNC, RT, FB	0	5.5	V
Pullup resistance	R_{PG}	4		kΩ
Output voltage	V_{OUT}	0.8	60	V
Output current	I_{OUT}, 8A option	0	8	A
	I_{OUT}, 6A option	0	6	A
	I_{OUT}, 4A option	0	4	A

(1) Recommended operating conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) Operation at the maximum transient voltage is limited to ≤1% of device operating lifetime.

6.4 Thermal Information

THERMAL METRIC[1] [1]		LM65640/60/80-Q1		UNIT
		eQFN (JESD 51-7)	eQFN (EVM)	
		26 PINS	26 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7[2]	18[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.9	5.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.6	–	°C/W

(1) For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. $R_{\theta JA}$ was calculated in accordance with JESD 51-7, simulated with a 4-layer JEDEC board, and does not represent the performance obtained in an actual application. Refer to the *Maximum Ambient Temperature* section for thermal design information.
(3) Refer to the LM65680-Q1 EVM user's guide for board layout and additional information.

6.5 Electrical Characteristics

Typical values are at T_J = 25°C. Minimum and maximum limits apply at T_J = –40°C to 150°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold voltage	V_{IN} rising (needed to start up)	3.25	3.4	3.5	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold voltage	V_{IN} falling (once operating)		2.5	2.55	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis voltage			0.9		V
I_{VIN}	VIN sleep quiescent current, internal COMP, no switching	V_{IN} = 48V, V_{BIAS} = 5V + 2%, CNFG tied to VCC, T_J = 25°C		0.9	1.4	µA
$I_{BIAS(FIX-3.3V)}$	BIAS quiescent current, fixed 3.3V output, internal COMP, no switching	V_{BIAS} = 3.3V + 2%, CNFG tied to VCC, AUTO mode, T_J = 25°C		8	10	µA
$I_{Q(FIX-3.3V)}$	VIN sleep quiescent current, fixed 3.3V output, internal COMP, no switching	V_{IN} = 24V, V_{BIAS} = 3.3V + 2%, CNFG tied to VCC, T_J = 25°C, AUTO mode		2.1	2.7	µA
		T_J = 125°C		2.1	6.4	µA
$I_{BIAS(FIX-5V)}$	BIAS quiescent current, fixed 5V output, internal COMP, no switching	V_{BIAS} = 5V + 2%, CNFG tied to VCC, AUTO mode, T_J = 25°C		9	12	µA
$I_{Q(FIX-5V)}$	VIN total sleep quiescent current, fixed 5V output, internal COMP, no switching	V_{IN} = 48V, V_{BIAS} = 5V + 2%, CNFG tied to VCC, T_J = 25°C, AUTO mode		1.8	2.4	µA
		T_J = 125°C		1.8	5.8	µA
$I_{BIAS(ADJ-3.3V)}$	BIAS quiescent current, adjustable 3.3V output, internal COMP, no switching	V_{FB} = 0.8V + 2%, CNFG tied to V_{CC}, AUTO mode, T_J = 25°C		6.8	8.1	µA
$I_{Q(ADJ-3.3V)}$	VIN total sleep quiescent current, adjustable 3.3V output, internal COMP, no switching	V_{IN} = 24V, V_{FB} = 0.8V + 2%, CNFG tied to VCC, AUTO mode, T_J = 25°C		1.9	2.5	µA
$I_{BIAS(ADJ-3.3V-EXT)}$	BIAS quiescent current, adjustable 3.3V output, external COMP, no switching	V_{FB} = 0.8V + 2%, R_{CNFG} = 49.9kΩ, AUTO mode, T_J = 25°C		37	44	µA
$I_{Q(ADJ-3.3V-EXT)}$	VIN total sleep quiescent current, adjustable 3.3V output, external COMP, no switching	V_{IN} = 24V, V_{FB} = 0.8V + 2%, R_{CNFG} = 49.9kΩ, AUTO mode, T_J = 25°C		6	7.4	µA
I_{Q-SHD}	VIN shutdown quiescent current	V_{IN} = 48V, $V_{EN/UVLO}$ = 0V, T_J = 25°C		0.8	1.2	µA
		V_{IN} = 48V, $V_{EN/UVLO}$ = 0V, T_J = 125°C		0.8	1.8	µA
PRECISION ENABLE (EN/UVLO)						
$V_{EN-TH(R)}$	EN/UVLO rising threshold	$V_{EN/UVLO}$ rising	1.15	1.25	1.35	V
$V_{EN-TH(F)}$	EN/UVLO falling threshold	$V_{EN/UVLO}$ falling	0.9	1	1.1	V
V_{EN-HYS}	EN/UVLO hysteresis			0.25		V
$V_{EN-HYS\%}$	Ratio of EN/UVLO hysteresis to rising threshold	$V_{EN-HYS}/V_{EN-TH(R)}$	18	20	22	%
I_{EN-LKG}	Enable input leakage current	EN/UVLO tied to VIN		0.16	3.5	µA
INTERNAL LDO (VCC)						

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6.5 Electrical Characteristics (continued)

Typical values are at T_J = 25°C. Minimum and maximum limits apply at T_J = –40°C to 150°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC1}	VCC regulation voltage	3.4V ≤ V_{IN} ≤ 65V, V_{BIAS} = 0V		3.3		V
V_{VCC2}		3.4V ≤ V_{BIAS} ≤ 30V		3.2		V
$V_{BIAS(ON)}$	BIAS switchover rising threshold (VIN to BIAS)	V_{BIAS} rising		3.175	3.25	V
$V_{BIAS(OFF)}$	BIAS switchover falling threshold (BIAS to VIN)	V_{BIAS} falling		3	3.05	V
$V_{VCC-UVLO(R)}$	VCC UVLO rising threshold	I_{VCC} = 0A	3.27	3.4	3.5	V
$V_{VCC-UVLO(F)}$	VCC UVLO falling threshold	I_{VCC} = 0A		2.5		V
REFERENCE VOLTAGE (FB)						
V_{FB1}	Feedback reference voltage, external COMP	FPWM mode, R_{CNFG} = 49.9kΩ	0.792	0.8	0.808	V
V_{FB2}	Feedback reference voltage, internal COMP	FPWM mode, CNFG tied to VCC	0.792	0.8	0.808	V
I_{FB-LKG}	Feedback pin input leakage current	V_{FB} = 0.8V, adjustable V_{OUT} setting		1.8	90	nA
FIXED OUTPUT VOLTAGE (BIAS)						
$V_{OUT-3.3V-INT}$	3.3V fixed output voltage, internal COMP	FB tied to GND, CNFG tied to VCC	3.267	3.3	3.337	V
$V_{OUT-3.3V-EXT}$	3.3V fixed output voltage, external COMP	FB tied to GND, R_{CNFG} = 49.9kΩ	3.267	3.3	3.337	V
$V_{OUT-5V-INT}$	5V fixed output voltage, internal COMP	FB tied to VCC, CNFG tied to VCC	4.94	5	5.06	V
$V_{OUT-5V-EXT}$	5V fixed output voltage, external COMP	FB tied to VCC, R_{CNFG} = 49.9kΩ	4.94	5	5.06	V
SOFT START (SS)						
t_{EN-SW}	Enable HIGH to start of switching delay	V_{FB} = V_{RT} = V_{MODE} = GND, V_{BIAS} = V_{OUT}	1.9	2.5	3.1	ms
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{FB} at 90% of setpoint	2.9	5.3	8.1	ms
I_{SS}	SS charge current	V_{SS} = 0V		20		µA
R_{SS}	SS discharge resistance	$V_{EN/UVLO}$ = 0V		7		Ω
ERROR AMPLIFIER (COMP)						
g_m	EA transconductance	V_{COMP} = 0.8V, V_{FB} = 0.8V ±5%		1		mS
$V_{COMP-EXT(h-clamp)}$	External COMP – high clamp voltage	V_{FB} = 0V, adjustable V_{OUT} setting		1.056		V
POWER STAGE (SW)						
$R_{DS(on)HS}$	High-side FET on-state resistance	I_{SW} = 500mA, V_{BST} – V_{SW} = 3.3V		42		mΩ
$R_{DS(on)LS}$	Low-side FET on-state resistance			23		mΩ
$t_{ON(min)}$	Minimum on-time[1]	I_{OUT} = 2A, R_{RT} = 6.81kΩ		36	48	ns
$t_{OFF(min)}$	Minimum off-time	V_{IN} = 4V, F_{SW} = 2.2MHz		82	118	ns
$t_{ON(max)}$	Maximum on-time	F_{SW} = 300kHz		13.3		µs
CURRENT LIMITS AND HICCUP MODE						
$I_{HS-LIM1}$	High-side peak current limit, 8A option	Duty cycle approaches 0%	10.7	12.5	13.7	A
$I_{LS-LIM1}$	Low-side valley current limit, 8A option		8.5	9.9	10.9	A
$I_{L-PK1(AUTO-minD)}$	AUTO-mode peak inductor current at minimum duty cycle, 8A option	t_{ON} ≤ 100ns	1.9	3	4.1	A
$I_{L-PK1(AUTO-maxD)}$	AUTO-mode peak inductor current at maximum duty cycle, 8A option	t_{ON} ≥ 1µs		1.1		A
$I_{HS-LIM2}$	High-side peak current limit, 6A option	Duty cycle approaches 0%	8.2	9.5	10.6	A
$I_{LS-LIM2}$	Low-side valley current limit, 6A option		6.6	7.4	8.2	A
$I_{L-PK2(AUTO-minD)}$	AUTO-mode peak inductor current at minimum duty cycle, 6A option	t_{ON} ≤ 100ns	1.1	1.9	2.8	A
$I_{L-PK2(AUTO-maxD)}$	AUTO-mode peak inductor current at maximum duty cycle, 6A option	t_{ON} ≥ 1µs		0.95		A
$I_{HS-LIM3}$	High-side peak current limit, 4A option	Duty cycle approaches 0%	5.9	7	8	A
$I_{LS-LIM3}$	Low-side valley current limit, 4A option		4.2	5.4	6.3	A
$I_{L-PK3(AUTO-minD)}$	AUTO-mode peak inductor current at minimum duty cycle, 4A option	t_{ON} ≤ 100ns	1	1.8	2.7	A

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6.5 Electrical Characteristics (continued)

Typical values are at T_J = 25°C. Minimum and maximum limits apply at T_J = –40°C to 150°C, unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{L-PK3(AUTO-maxD)}$	AUTO-mode peak inductor current at maximum duty cycle, 4A option	t_{ON} ≥ 1µs		0.65		A
$I_{LS-NEG-LIM}$	Low-side negative current limit	Sinking current limit, FPWM mode	–9.6	–6.9	–4.9	A
I_{L-ZC}	Zero-cross threshold	AUTO mode		100		mA
V_{HIC}	FB voltage hiccup threshold	Low-side FET on-time > 165ns, after soft start		0.32		V
t_{HICDLY}	Hiccup mode activation delay			64		cycles
t_{HIC}	Hiccup mode duration time	Internal soft start		48		ms
POWER GOOD (PG)						
$V_{PG-OV(R)}$	PG OV rising threshold	% of FB voltage (ADJ output) or BIAS voltage (fixed output)	103	105	107	%
$V_{PG-OV(F)}$	PG OV falling threshold		101	104	106	%
$V_{PG-UV(R)}$	PG UV rising threshold		94	96	98.5	%
$V_{PG-UV(F)}$	PG UV falling threshold		92.5	95	97	%
$t_{PG-DEGLITCH(R)}$	Deglitch filter delay on PG rising edge		1.2	2	3	ms
$t_{PG-DEGLITCH(F)}$	Deglitch filter delay on PG falling edge		55	130	175	µs
$V_{IN(PG-VALID)}$	Minimum V_{IN} for valid PG output	$V_{PG(OL)}$ < 0.4V, R_{PG} = 49.9kΩ, V_{PG} = 5V			1.25	V
$V_{PG(OL)}$	PG low-state voltage	I_{PG} = 1mA, V_{IN} = 1.25V			0.4	V
$R_{PG(on)}$	PG switch on resistance	I_{PG} = 1mA		51	110	Ω
SWITCHING FREQUENCY (RT)						
f_{SW1}	Switching frequency	RT tied to PGND	1.98	2.2	2.42	MHz
		R_{RT} = 6.81kΩ ±1%	1.98	2.2	2.42	MHz
f_{SW2}		R_{RT} = 15.8kΩ ±1%	900	1000	1100	kHz
f_{SW3}		R_{RT} = 40.2kΩ ±1%	360	400	440	kHz
		RT tied to VCC	360	400	440	kHz
SYNCHRONIZATION (MODE/SYNC)						
$V_{SYNC(IL)}$	SYNC input low-level threshold		0.45			V
$V_{SYNC(IH)}$	SYNC input high-level threshold				1.3	V
$V_{SYNCOUT(OL)}$	SYNCOUT output low-level threshold	$I_{SYNCOUT}$ = 2mA			0.4	V
$V_{SYNCOUT(OH)}$	SYNCOUT output high-level threshold	$I_{SYNCOUT}$ = –2mA	2.4			V
$f_{SYNC-RANGE1}$	Synchronization frequency range for set 2.2MHz	R_{RT} = 6.81kΩ ±1%	1.76		2.64	MHz
$f_{SYNC-RANGE2}$	Synchronization frequency range for set 300kHz	R_{RT} = 54.2kΩ ±1%	240		360	kHz
$t_{SYNC-LOW(min)}$	Minimum low pulse width of external SYNC signal				80	ns
$t_{SYNC-HIGH(min)}$	Minimum high pulse width of external SYNC signal				80	ns
$t_{SYNC-SW-DLY}$	SYNC to SW delay time(1)		–22		22	ns
$t_{MODE-DLY}$	MODE change delay time(1)				20	µs
DUAL RANDOM SPREAD SPECTRUM (DRSS/MCOMM)						
Δf_{SS-LF}	Low-frequency triangular spread spectrum modulation range	DRSS/MCOMM open		17		%
f_{m-LF}	Triangular modulation frequency	DRSS/MCOMM open	3.6	6	8.4	kHz
Δf_{SS-HF}	High-frequency pseudo-random spread spectrum modulation range	DRSS/MCOMM open		2		%
THERMAL SHUTDOWN						
T_{SHD}	Thermal shutdown(1)	Shutdown threshold	155	165	177	ºC
		Recovery threshold		156		ºC

(1) Specified by design.

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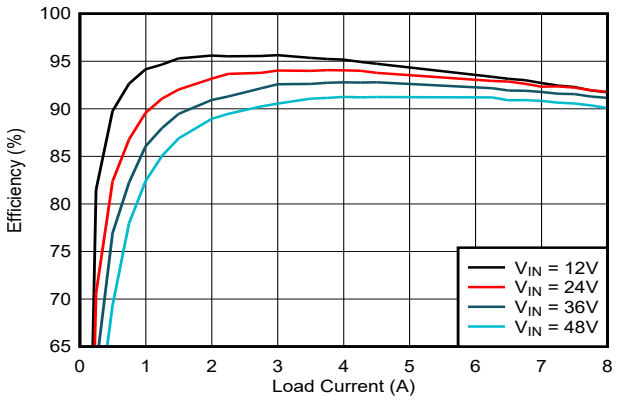
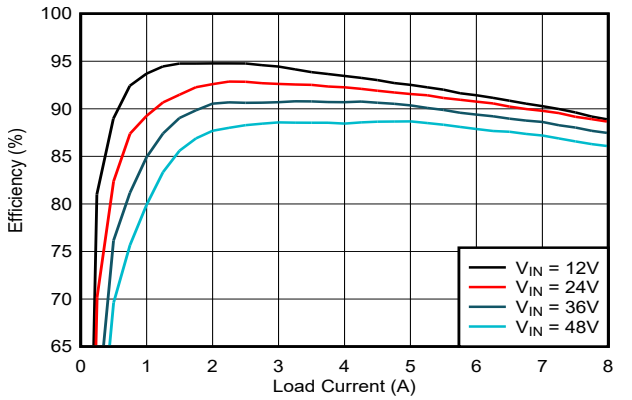
6.6 Typical Characteristics

Unless otherwise specified, T_A = 25°C.



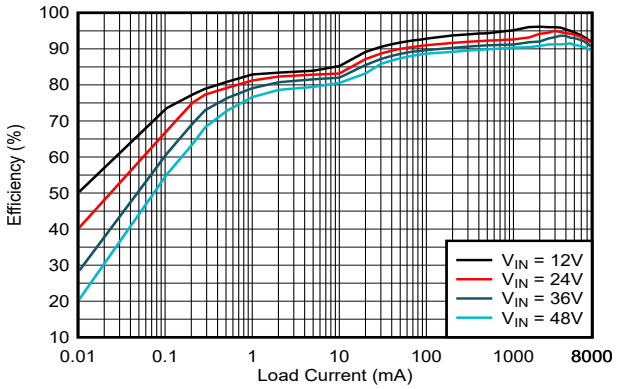
See Figure 8-7 F_{SW} = 400kHz L_O = XGL6060, 3.3µH

Figure 6-1. Efficiency, FPWM, V_{OUT} = 5V



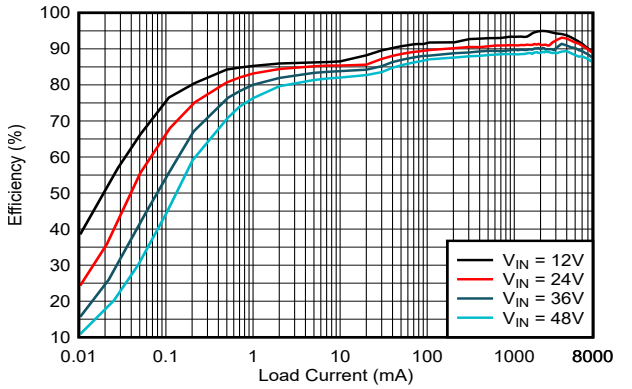
V_{OUT} = 3.3V F_{SW} = 400kHz L_O = XGL6060, 3.3µH

Figure 6-2. Efficiency, FPWM, V_{OUT} = 3.3V



See Figure 8-7 F_{SW} = 400kHz L_O = XGL6060, 5.6µH

Figure 6-3. Efficiency, AUTO Mode, V_{OUT} = 5V



V_{OUT} = 3.3V F_{SW} = 400kHz L_O = XGL6060, 5.6µH

Figure 6-4. Efficiency, AUTO Mode, V_{OUT} = 3.3V

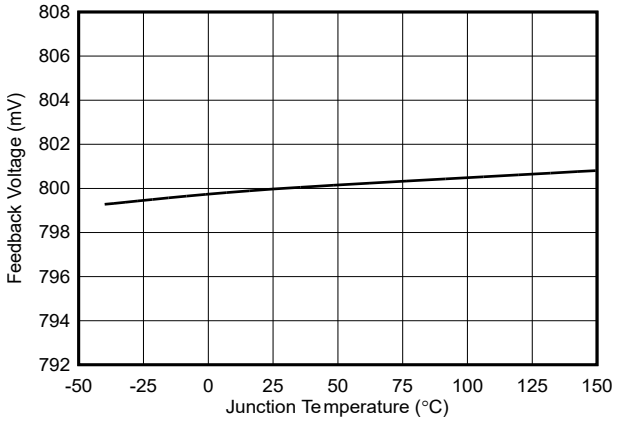


Figure 6-5. FB Voltage, Internal Compensation

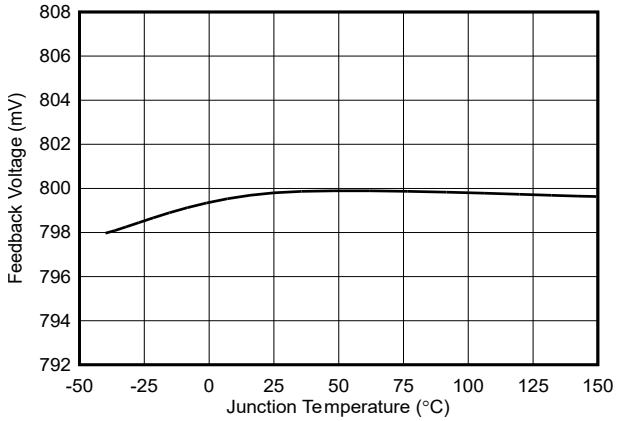


Figure 6-6. FB Voltage, External Compensation

6.6 Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

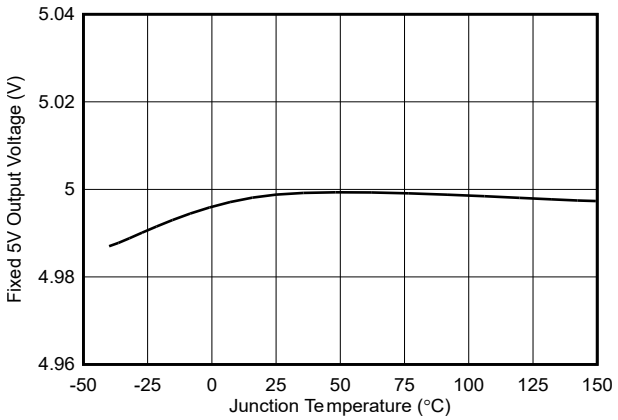


Figure 6-7. Fixed 5V Output Voltage Setpoint

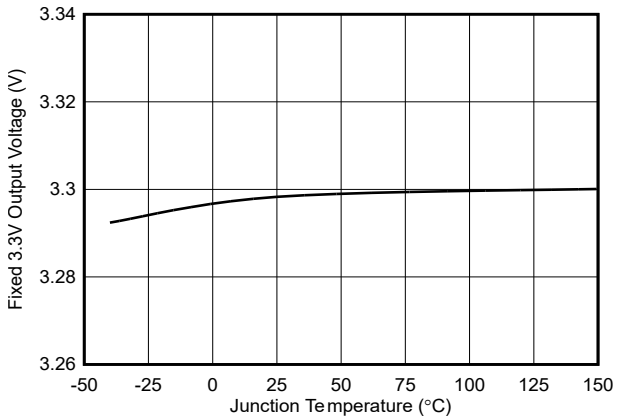


Figure 6-8. Fixed 3.3V Output Voltage Setpoint

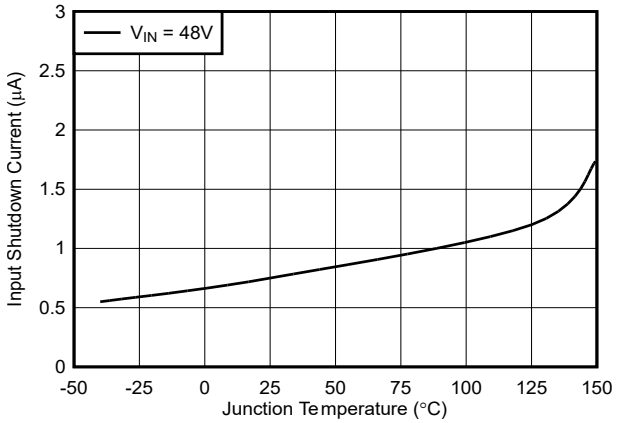


Figure 6-9. VIN Shutdown Quiescent Current

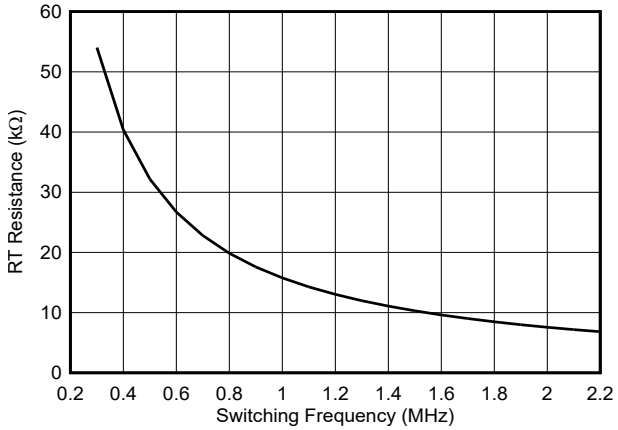


Figure 6-10. RT Resistance vs Switching Frequency

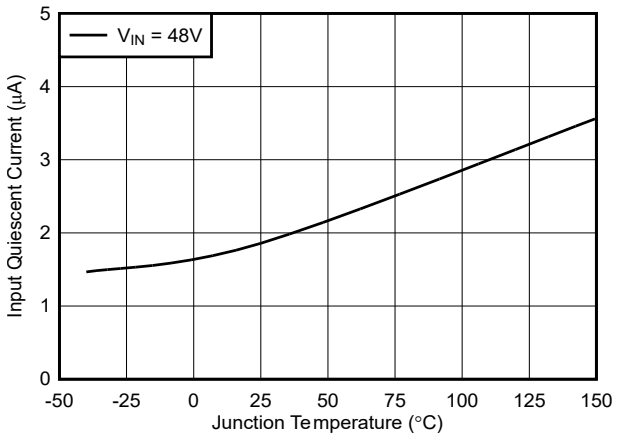


Figure 6-11. VIN Sleep Quiescent Current, 5V Fixed Output

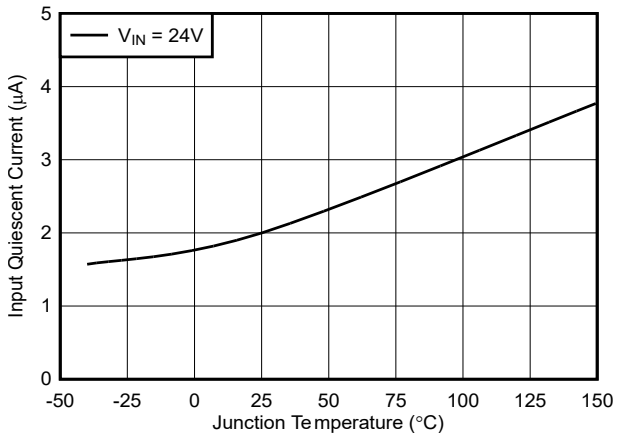


Figure 6-12. VIN Sleep Quiescent Current, 3.3V Fixed Output

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6.6 Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

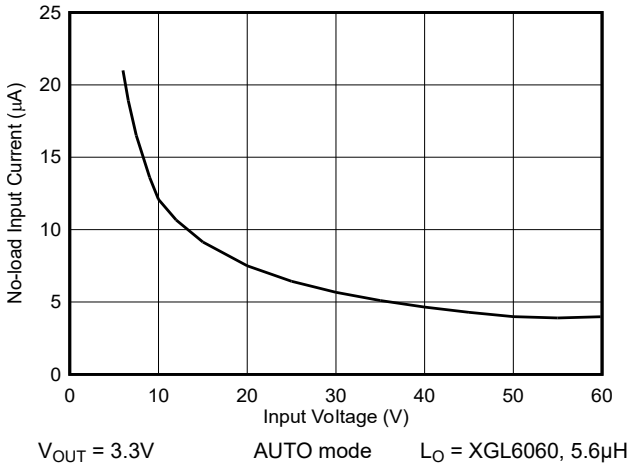

Figure 6-13. No-Load Input Current, 3.3V Fixed Output, External Compensation

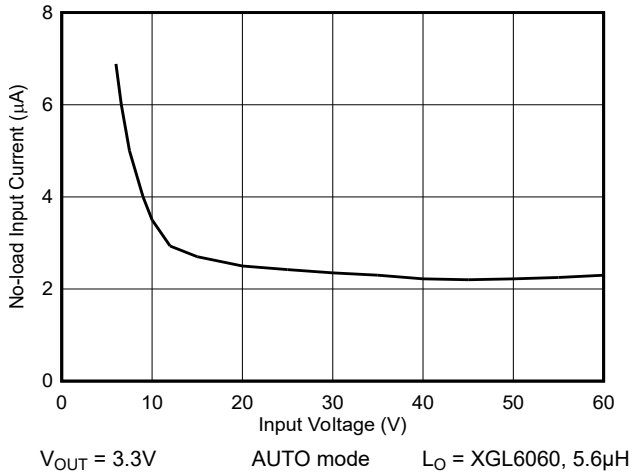

Figure 6-14. No-Load Input Current, 3.3V Fixed Output, Internal Compensation

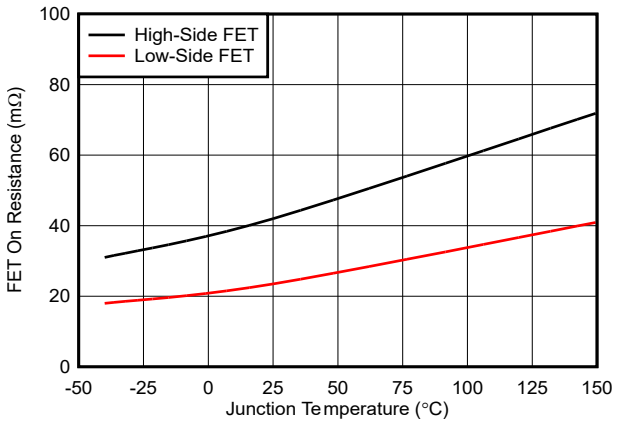

Figure 6-15. High-side and Low-side MOSFET $R_{DS(on)}$

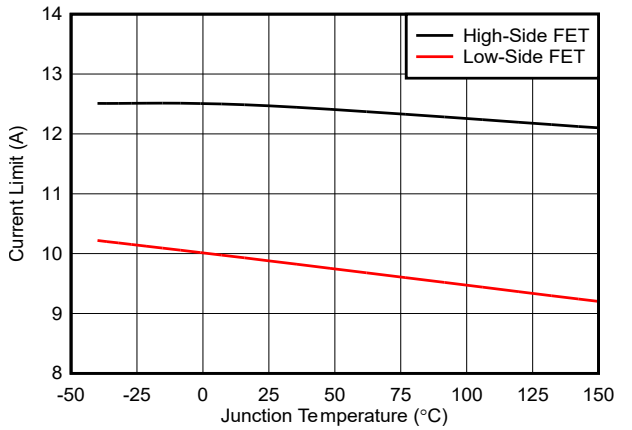

Figure 6-16. MOSFET Current Limits – 8A Option

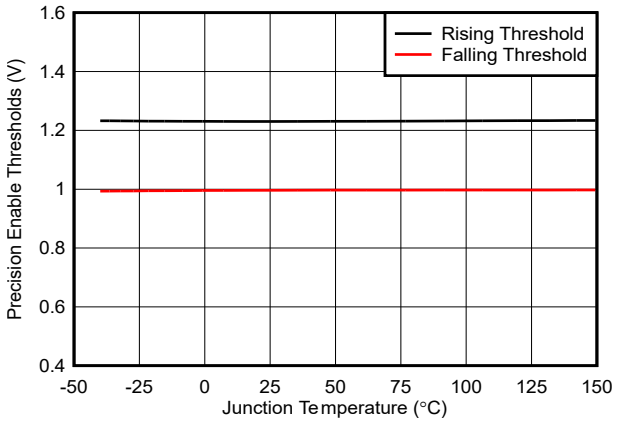

Figure 6-17. Precision Enable Thresholds

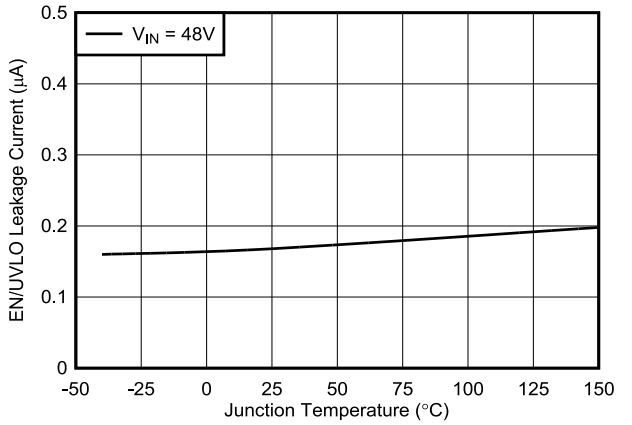

Figure 6-18. EN/UVLO Input Leakage Current

6.6 Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

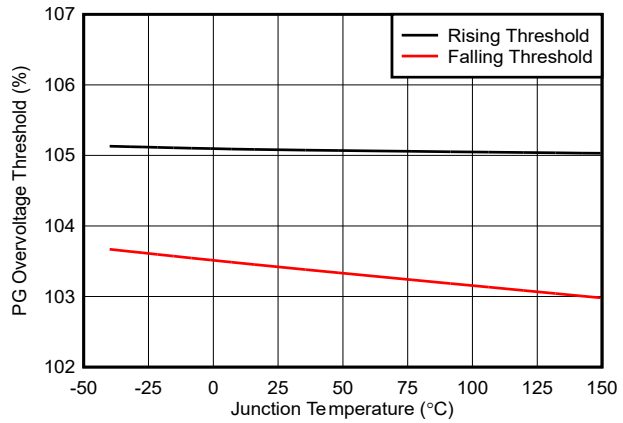

Figure 6-19. PG OV Thresholds

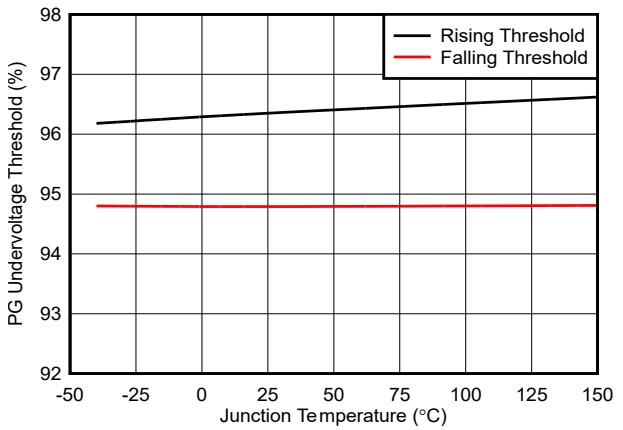

Figure 6-20. PG UV Thresholds

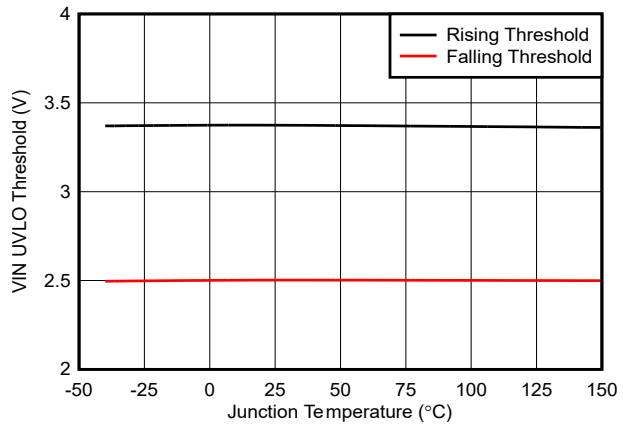

Figure 6-21. VIN UVLO Thresholds

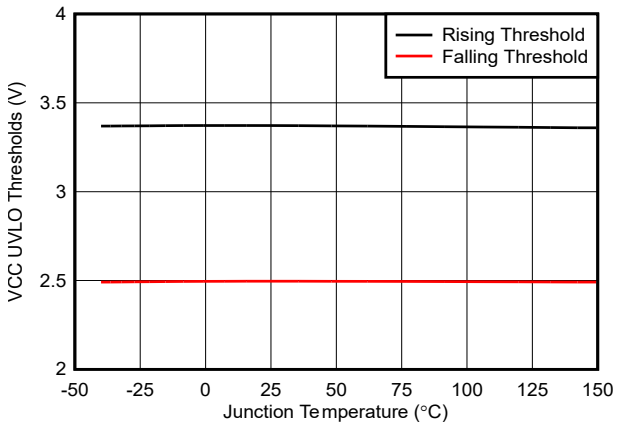

Figure 6-22. VCC UVLO Thresholds

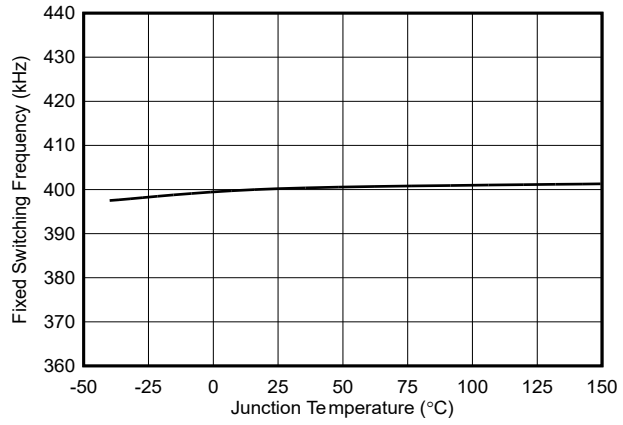

Figure 6-23. Fixed Switching Frequency – 400kHz

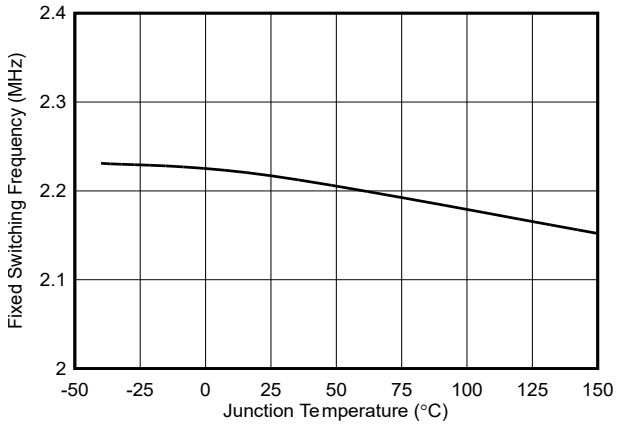

Figure 6-24. Fixed Switching Frequency – 2.2MHz

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7 Detailed Description

7.1 Overview

The LM656x0-Q1 is a family of high efficiency, high power density, low-EMI buck IBB converters. These converters operate over a wide input voltage range of 3.5V to 65V (70V transient) with pin-selectable fixed output voltages of 3.3V and 5V, or an adjustable output voltage from 0.8V to 60V. Up to two converters can be set up in interleaved mode (paralleled outputs) with accurate current sharing to support up to 16A of output current.

The peak current-mode control architecture with 36ns minimum on-time allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the switching frequency automatically reduces. This feature allows regulation to be maintained during line transients events, such as load dump and cold crank.

The LM656x0-Q1 is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. The device has a resistor-programmable switching frequency from 300kHz to 2.2MHz. Internal compensation and an accurate current limit scheme minimize BOM cost and component count.

Designed for low conducted and radiated emissions, the LM656x0-Q1 includes the following features:

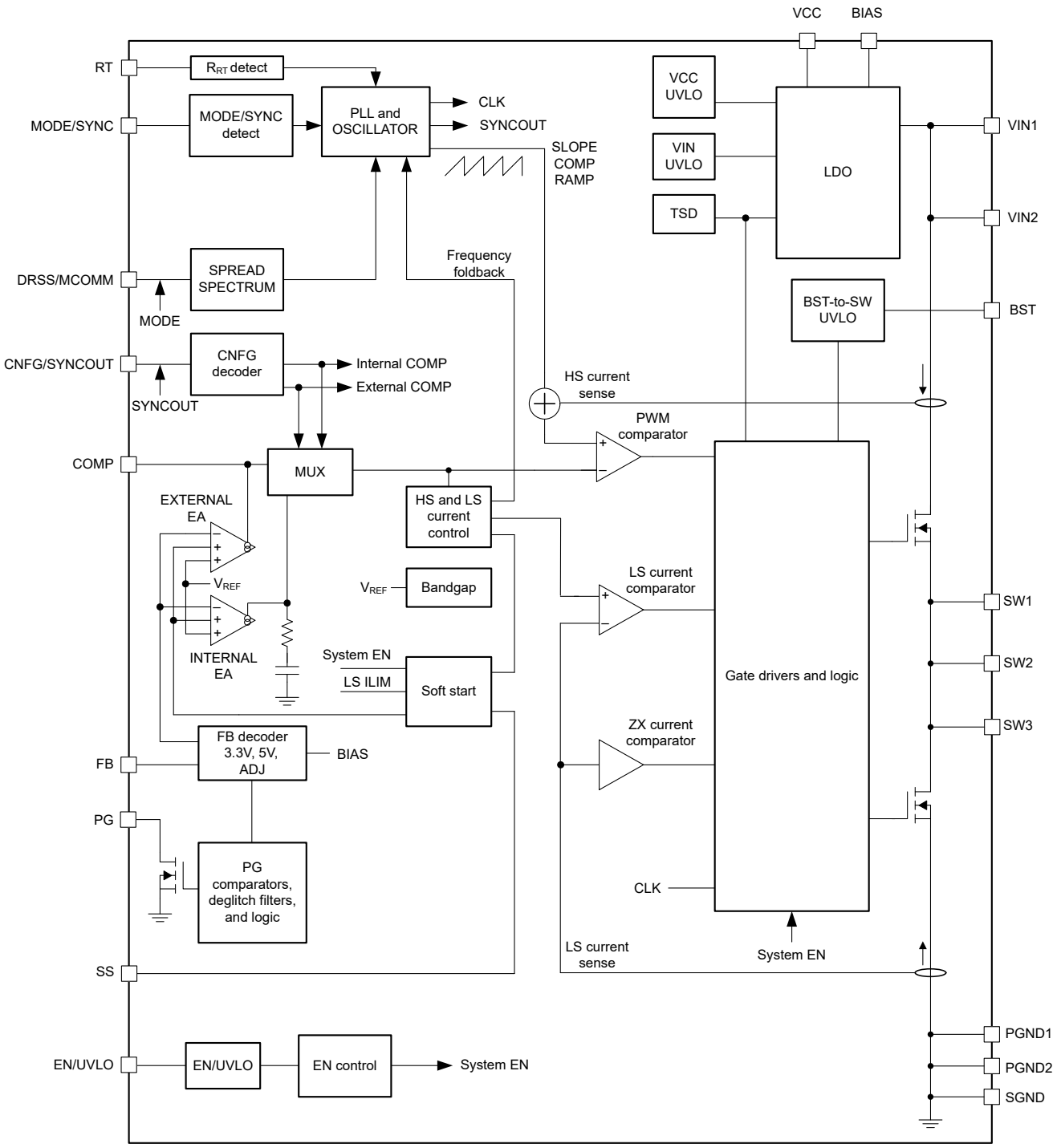
- Pin-configurable switch node slew-rate control
- Dual-random spread spectrum (DRSS) frequency modulation
- Symmetrical pinout that enables low parasitic inductance in the input power loops
- Operation over a switching frequency range above or below AM radio band
- Pin-configurable AUTO or FPWM mode along with external clock synchronization capability

Together, these features can eliminate shielding and other expensive EMI mitigation measures.

Additional features of the LM656x0-Q1 include 150°C maximum junction temperature operation, open-drain power-good (PG) indicator referenced to system ground (SGND) for fault reporting and output voltage monitoring, monotonic start-up into prebiased loads, dual-input VCC bias subregulator powered from VIN or BIAS, hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

To use the device in reliability-conscious environments, the LM656x0-Q1 has a package with enlarged corner terminals for improved board-level reliability and wettable flanks that facilitate optical inspection during manufacturing.

7.2 Functional Block Diagram



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7.3 Feature Descriptions

7.3.1 Input Voltage Range (VIN1, VIN2)

The LM656x0-Q1 operational input voltage range is from 3.5V to 65V (70V transient). The device is intended for step-down conversions from 24V, 48V, and 60V supply rails. Figure 7-1 shows all the necessary components to implement an LM656x0-Q1-based wide-V_{IN} step-down regulator from a single input supply. The LM656x0-Q1 uses an internal LDO subregulator to provide a VCC bias rail of 3.3V for the gate drive and control circuits.

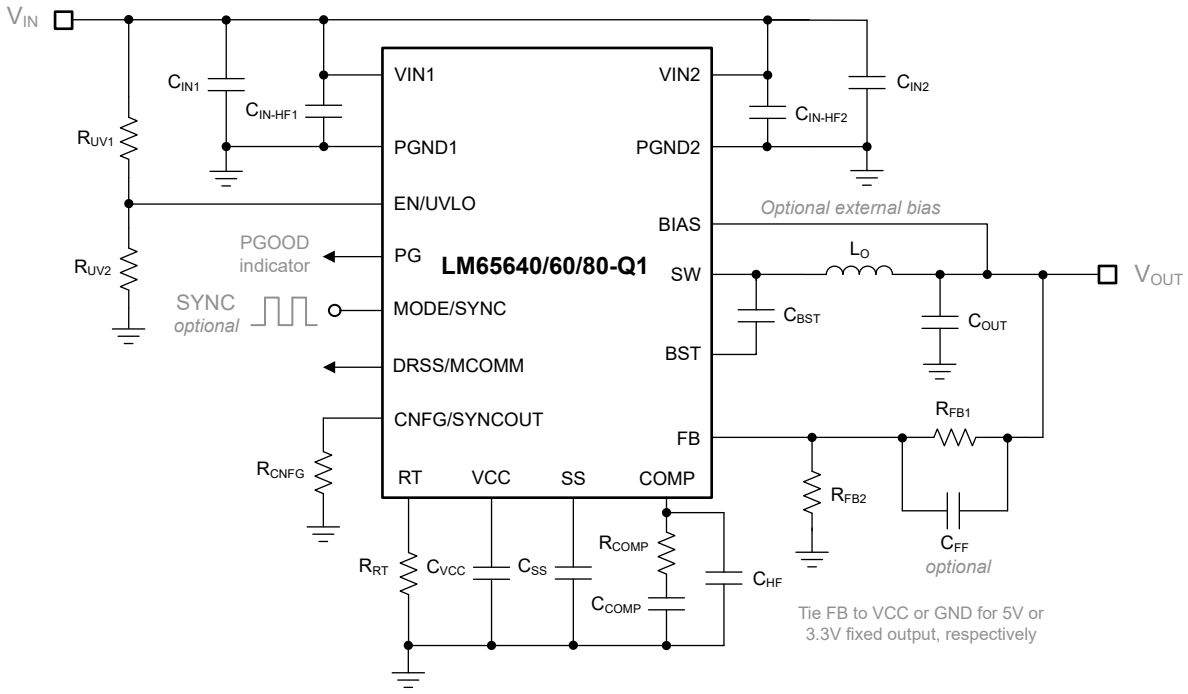

Figure 7-1. LM656x0-Q1 Regulator Schematic

In applications with high input voltage, take extra care to make sure that the VIN pins (VIN1 and VIN2) and the SW pins (SW1, SW2, SW3) of the converter do not exceed the absolute maximum voltage rating of 72V during line or load transient events. Voltage excursions that exceed the applicable voltage specifications can damage the device.

7.3.2 High-Voltage Bias Supply Subregulator (VCC, BIAS)

The LM656x0-Q1 contains an internal high-voltage subregulator for VCC that is supplied from either VIN or BIAS. Tie a low-voltage supply, such as the buck converter output voltage (V_{OUT}) or another applicable system rail as high as 30V, to BIAS. Powering VCC from a lower voltage rail reduces the internal power dissipation of the LM656x0-Q1. Tie BIAS to PGND if unused.

Once the LM656x0-Q1 is active, bias current derives from VIN if BIAS is less than 3V. The VCC subregulator switches over to use BIAS as the input once the BIAS voltage exceeds the switchover threshold of 3.175V. The switchover voltage hysteresis is 175mV.

During start-up, VCC momentarily exceeds the normal operating voltage until the voltage exceeds the VCC UVLO rising threshold of 3.4V. VCC then drops to an operating voltage of 3.3V when powered from VIN or 3.2V when powered from BIAS. To prevent unsafe operation, VCC has UVLO protection that prevents switching if the VCC voltage falls below 2.5V. Connect a 1µF ceramic capacitor (rated for 10V with X7R dielectric) from VCC to PGND.

7.3.3 Precision Enable and Adjustable Input Voltage UVLO (EN/UVLO)

Enable the LM656x0-Q1 converter with a EN/UVLO voltage greater than the rising threshold of 1.25V, which allows the device to initiate soft start. If EN/UVLO is brought below the falling threshold of 1V, the regulator stops

switching, discharges the output with an internal discharge switch (approximately 5mA discharge current), and enters shutdown mode, resulting in a shutdown quiescent current of less than 1µA. Connect EN/UVLO directly to VIN if this feature is not required. EN/UVLO must not be left open, as floating the pin forces the device off.

The EN/UVLO input supports adjustable input undervoltage lockout (UVLO) programmed by resistor values for application-specific power-up and power-down requirements. Install resistors R_{UV1} and R_{UV2} as shown in Figure 7-2 to establish a precision input voltage UVLO that is different from the fixed UVLO levels internal to the device. Adjustable UVLO is useful for sequencing, to prevent re-triggering of the device when used with long input cables, or to avoid deep discharge of a battery input source. The precision enable threshold has a 20% hysteresis to prevent ON/OFF re-triggering. An external logic signal from another IC (such as an MCU) is useful to toggle the output ON or OFF and to implement system power sequencing or protection.

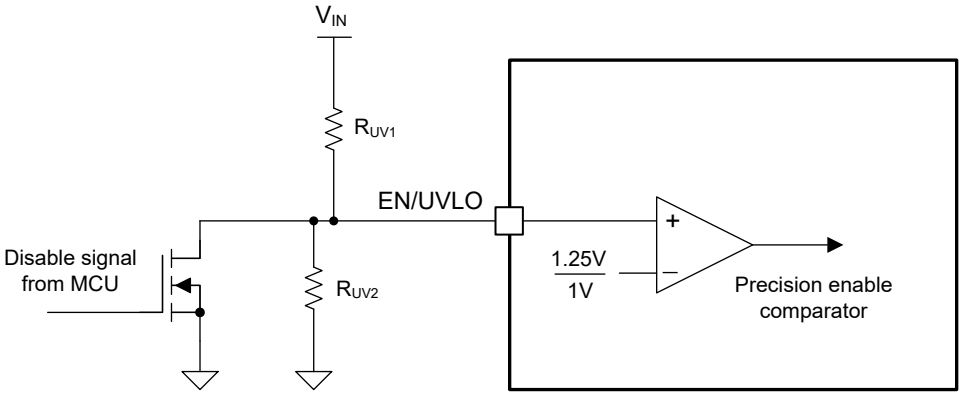

Figure 7-2. Programmable Input Voltage UVLO

To maximize accuracy, the current in the divider must be greater than the EN/UVLO input leakage current, $I_{EN\text{-}LKG}$. Select the lower UVLO divider resistor R_{UV2} between 10kΩ and 50kΩ. Then use Equation 1 and Equation 2 to calculate R_{UV1} and $V_{IN(off)}$, respectively, where $V_{IN(on)}$ and $V_{IN(off)}$ are the input voltage turn-on and turn-off thresholds.

$$R_{UV1} = R_{UV2} \times \left(\frac{V_{IN(on)}}{V_{EN-TH(R)}} - 1 \right) \quad (1)$$

$$V_{IN(off)} = V_{IN(on)} \times \left(1 - V_{EN-HYS\%} \right) \quad (2)$$

Keep in mind that the internal VIN UVLO protection overrides the EN/UVLO input. The LM656x0-Q1 does not start up unless the input voltage exceeds the UVLO rising threshold of 3.4V. Conversely, the device shuts down when the input voltage falls below the UVLO falling threshold of 2.5V.

7.3.4 Output Voltage Setpoint (FB, BIAS)

While dependent on switching frequency and load current levels, the LM656x0-Q1 buck converter is generally capable of providing an output voltage in the range of 0.8V to a maximum of slightly less than the input voltage. The rated maximum output voltage is 60V. The LM656x0-Q1 features pin-selectable fixed and adjustable output voltage settings.

Connect FB to VCC or PGND to select a fixed 5V or 3.3V output, respectively, and connect BIAS directly to the regulator output for output voltage sensing. As such, BIAS closes the voltage feedback loop and provides power to the internal VCC subregulator.

Alternatively, define the output voltage setpoint with feedback resistors designated as R_{FB1} and R_{FB2}, as shown in Figure 7-1. The LM656x0-Q1 has a 0.8V reference, and the internal voltage-loop error amplifier regulates the FB voltage to be equal to this reference voltage. Use Equation 3 to determine R_{FB2} for a desired output voltage setpoint and a given value of R_{FB1}.

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$$R_{FB2} = R_{FB1} \times \frac{0.8V}{V_{OUT} - 0.8V} \quad (3)$$

$$4k\Omega \leq \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} \leq 100k\Omega \quad (4)$$

Make sure that the selected values for R_{FB1} and R_{FB2} meet the requirement set by Equation 4. Best practice is to choose a value for R_{FB1} lower than 200kΩ, as higher values of resistance are often susceptible to parasitic leakage currents (for example, caused by environmental contamination of the PCB) that can shift the desired output voltage. In cases where leakage currents are not significant, use feedback resistances as high as 1MΩ to reduce the no-load current consumption and improve light-load efficiency. With the adjustable output setting, a feedforward capacitor in parallel with the upper feedback resistor is an option to improve the loop phase margin.

7.3.5 Switching Frequency (RT)

Program the LM656x0-Q1 oscillator with a resistor from RT to PGND to set the free-running switching frequency between 300kHz and 2.2MHz. Use Equation 5 or refer to Figure 7-3 for the resistor values.

$$R_{RT}[k\Omega] = \frac{16.4}{F_{SW}[MHz]} - 0.633 \quad (5)$$

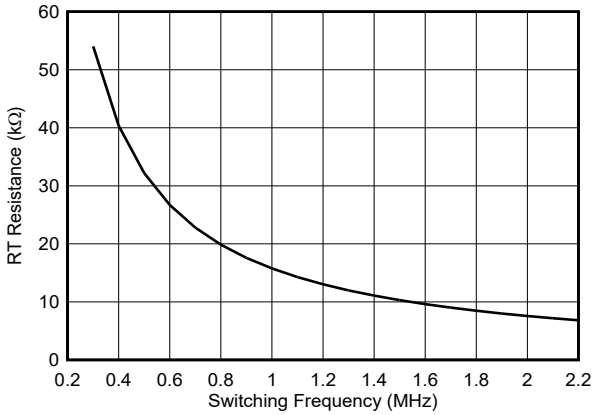

Figure 7-3. Setting the Switching Frequency

For example, F_{SW} set for 300kHz in Equation 5 gives R_{RT} of 54.03kΩ. Select 53.6kΩ as the closest standard value. Alternatively, connect RT to VCC or PGND for fixed 400kHz or 2.2MHz operation, respectively, as shown in Table 7-1.

Table 7-1. Switching Frequency Settings

RT	SWITCHING FREQUENCY
Tie to VCC	400kHz
Tie to PGND	2.2MHz
RT resistor to PGND	300kHz to 2.2MHz

Note that if the RT resistance falls outside of the recommended range, the LM656x0-Q1 reverts to 400kHz or 2.2MHz. Do not apply a pulsed signal to RT to force synchronization. If the converter requires synchronization to an external clock signal, refer to Section 7.3.6.

7.3.6 Mode Selection and Clock Synchronization (MODE/SYNC)

MODE/SYNC is a multifunction pin that configures the mode of operation and serves as an input for an external clock synchronization signal.

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As shown in Table 7-2, if MODE/SYNC is grounded or driven to a logic low, the converter operates in AUTO mode. If the pin is tied to VCC or driven to a logic high, or synchronized to an external clock source, the converter operates in FPWM mode.

Table 7-2. Mode Selection

MODE/SYNC	MODE	DYNAMIC MODE CHANGE
Tied to PGND or driven low	AUTO	Enabled
Tied to VCC or driven high (> 2.5V above PGND)	FPWM	
External clock signal applied		

Transitioning the device from AUTO to FPWM mode requires driving the pin from low to high or applying a synchronization signal. Transitioning from FPWM to AUTO mode requires driving the pin from high to low or stopping the synchronization signal.

Note

Changing the mode of operation or synchronizing the device to an external clock is possible only after start-up, once PG transitions high.

7.3.6.1 Clock Synchronization

Use MODE/SYNC to synchronize the internal oscillator to an external clock signal running between 300kHz and 2.2MHz. The amplitude of the external clock must meet the SYNC input thresholds, $V_{SYNC(IH)}$ and $V_{SYNC(IL)}$, to reliably trigger the internal synchronization pulse detector. The minimum SYNC ON and OFF pulse durations must exceed $t_{SYNC-ON(min)}$ and $t_{SYNC-OFF(min)}$, respectively.

Note that an external clock signal can only be applied after power up, when PG transitions to high. If applied before power up (or during pin detection), the LM656x0-Q1 can not detect the clock signal.

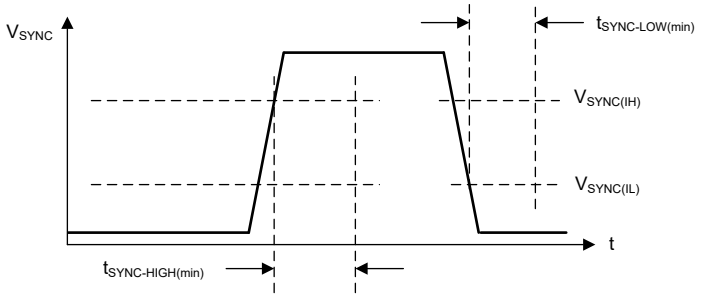

Figure 7-4. Typical SYNC Waveform With Conditions Required for Clock Signal Detection

7.3.6.2 Clock Locking

Upon detection of a valid synchronization signal, the LM656x0-Q1 initiates a clock locking procedure. After approximately 2048 pulses, the internal oscillator frequency changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, the LM656x0-Q1 maintains the phase such that the clock cycle lying between operation at the free-running and synchronization frequencies is of intermediate length. There are no very long or very short pulses. Once the frequency locks, the phase adjusts over tens of cycles such that rising synchronization edges correspond to switch-node rising pulses. Refer to Figure 7-5.

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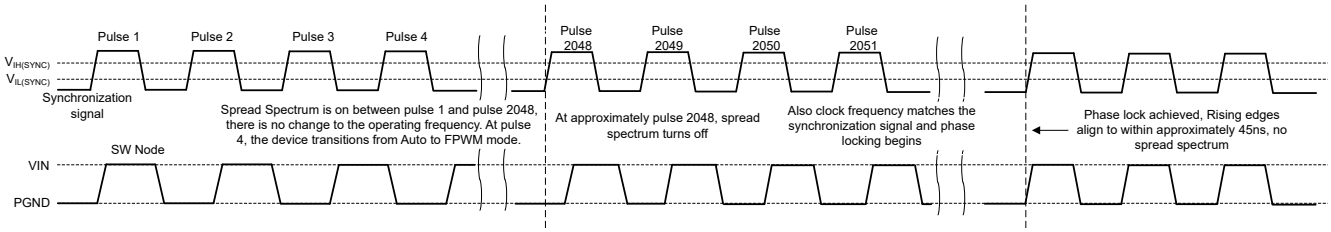

At pulse 4, the synchronization signal is detected. After approximately pulse 2048, the signal is ready to synchronize and the frequency is adjusted using a glitch-free technique until the phase is locked.

Figure 7-5. Synchronization Process

7.3.7 Device Configuration (CNFG/SYNCOUT)

The LM656x0-Q1 can operate as a standalone converter with internal or external compensation, or as a two-phase converter with external compensation. CNFG/SYNCOUT serves as a device configuration pin.

CNFG/SYNCOUT configures the device as a primary or a secondary device, selects either internal compensation (single-phase operation) or external compensation (single-phase or two-phase operation), and affects DRSS/MCOMM functionality, as shown in Table 7-3.

Table 7-3. Device Configuration

CNFG/SUNCOUT	CONFIGURATION	DRSS/MCOMM FUNCTIONALITY
Short to PGND	Secondary device, SYNCOUT disabled	MCOMM input
49.9kΩ to PGND	Primary device, external COMP, SYNCOUT enabled	DRSS control, MCOMM output
Short to VCC	Primary device, internal COMP, SYNCOUT disabled	DRSS control

7.3.8 Dual-Random Spread Spectrum (DRSS)

The LM656x0-Q1 provides a Dual-Random Spread Spectrum (DRSS) function, which reduces EMI of the power supply over a wide frequency range. As shown in Figure 7-6, DRSS combines a low-frequency triangular modulation profile with a high-frequency cycle-by-cycle pseudo-random modulation profile. The low-frequency triangular modulation improves performance in the lower radio-frequency bands, while the high-frequency random modulation improves performance in the higher radio-frequency bands.

Spread spectrum functions by converting a narrowband signal into a wideband signal that spreads the energy over multiple frequencies. Because industry standards require different EMI receiver resolution bandwidth (RBW) settings for different frequency bands, the RBW has an impact on the spread spectrum performance. For example, the CISPR 25 spectrum analyzer RBW in the frequency band from 150kHz to 30MHz is 9kHz. For frequencies greater than 30MHz, the RBW is 120kHz. DRSS is able to simultaneously improve the EMI performance with low and high RBWs through the low-frequency triangular and high-frequency cycle-by-cycle random modulation profiles, respectively. DRSS can reduce conducted emissions by up to 10dBµV in the low-frequency band (150kHz to 30MHz) and 5dBµV in the high-frequency band (30MHz to 108MHz) for CISPR 25. Applying an external clock signal to MODE/SYNC disables DRSS.

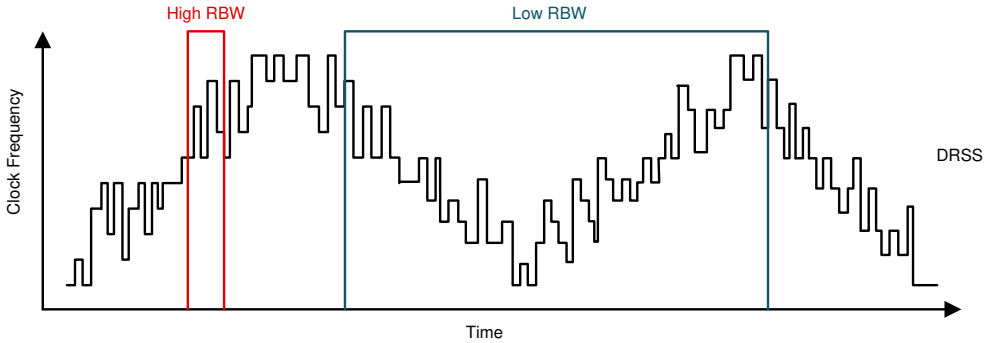

Figure 7-6. Dual Random Spread Spectrum Implementation

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The device provides a wide low-frequency modulation profile that spreads the switching frequency by ±10% with a 6kHz average modulation frequency. As shown in Table 7-4, the LM656x0-Q1 also provides a switch-node waveform shaping feature that, when enabled, adjusts the switch-node voltage rising transition for reduced ringing and overshoot.

Table 7-4. DRSS and Slew-Rate Control

DRSS/MCOMM	DRSS	SLEW RATE CONTROL
Short to VCC(1)	Enabled, ±10%, 6kHz	Enabled
Leave open	Enabled, ±10%, 6kHz	Enabled
150kΩ to PGND	Enabled, ±10%, 6kHz	Disabled
49.9kΩ to PGND	Disabled	Enabled
Short to PGND(1)	Disabled	Disabled

(1) Only valid for single-phase operation.

7.3.9 High-Side MOSFET Gate Drive (BST)

The gate driver for the high-side power MOSFET requires a bias voltage higher than VIN when the MOSFET is on. A capacitor from BST to SW behaves as a bootstrap supply to boost the voltage on BST to V_{SW} + V_{VCC}. The LM656x0-Q1 has an integrated bootstrap diode to minimize the external component count. TI recommends a BST capacitor of 100nF rated for 10V with X7R dielectric.

7.3.10 Configurable Soft Start (SS)

The LM656x0-Q1 converter has a soft-start feature that slowly ramps the target regulation voltage to gradually reach the steady-state operating point, thus preventing output voltage overshoot and high inrush current at the input during start-up. The device initiates soft start based on any of these conditions:

- Power applied to the VIN pins of the IC, releasing UVLO for both VIN and VCC
- EN/UVLO goes high, turning on the device
- Recovery from a hiccup-waiting period
- Recovery from thermal shutdown protection.

The simplest way to use the LM656x0-Q1 is to leave the SS pin open for a fixed soft-start time of 5.3ms. In applications with high output capacitance, high output voltage, or other special requirements, extend the soft-start time with a capacitor from SS to PGND. Use Equation 6 or refer to Figure 7-7 to select a value for C_{SS} based on a desired soft-start time, t_{SS}.

$$C_{SS}[nF] = 16.7 \times t_{SS}[ms] \quad (6)$$

For example, for a desired soft-start time of 12ms, Equation 6 gives the a value for C_{SS} of 200nF. Select 220nF as the closest standard value.

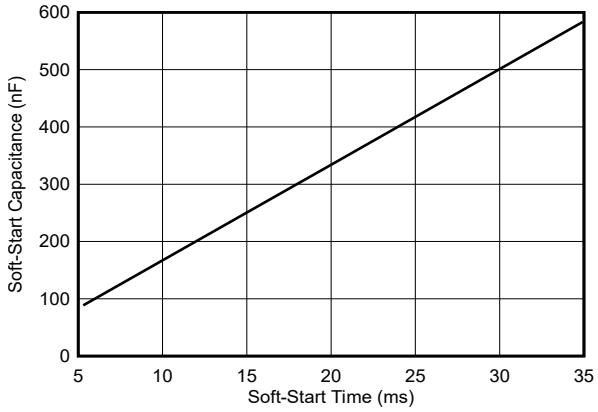

Figure 7-7. Setting the Soft-Start Time

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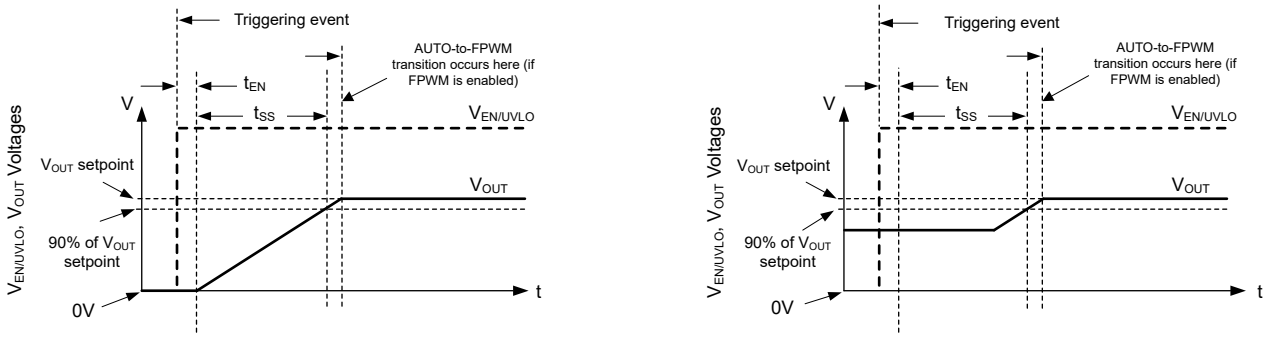
Upon initiating soft start, the device takes the following actions:

- The internal reference to regulate the output voltage slowly ramps from zero. The net result is that the output voltage takes t_{SS} to reach 90% of the desired value.
- The operating mode sets to AUTO, activating diode emulation such that a prebiased start-up occurs without pulling down on the output voltage.
- Hiccup-mode protection remains disabled for the duration of soft start; see Section 7.3.11.3.

Together, these actions provide a start-up profile with limited inrush current and allow high output capacitance and high loading conditions such that the device can approach current limit during start-up without triggering hiccup. See Figure 7-8.



After soft start initiates, the output voltage reaches 90% of the output setpoint after a time interval, t_{SS}. The device disables FPWM and hiccup during the soft-start interval, and subsequently enables these modes once the output voltage reaches regulation.

Figure 7-8. Output Voltage Soft Start: No Prebias (a), With Prebias (b)

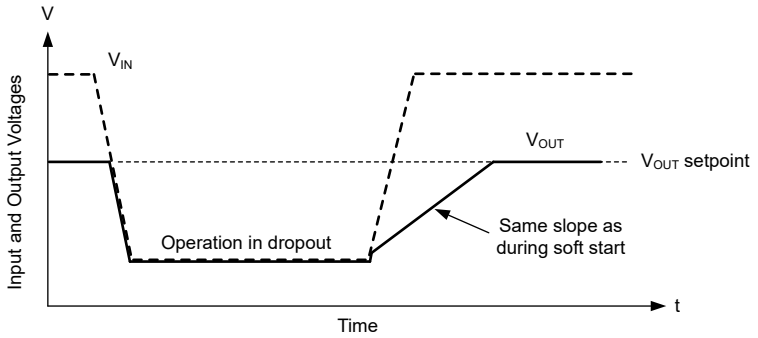
7.3.10.1 Recovery From Dropout

Any time the output voltage falls more than a few percent (for example, when the input voltage falls below the output voltage setpoint), the output voltage ramps up slowly during the recovery. Known as recovery from dropout, this condition differs from soft start in three important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the output voltage setpoint. The reference voltage is not started from zero.
- Hiccup is allowed only if output voltage is less than 40% of the setpoint. As described in Section 7.3.11.3, the device inhibits hiccup when operating in dropout.
- FPWM mode is allowed during recovery from dropout. If the output voltage is suddenly pulled up by an external supply, the converter can pull down on the output. Note that all the protections present during normal operation are in place, protecting the device if the output gets shorted to a high voltage or ground.

Despite being called recovery from dropout, this feature is active whenever the output voltage drops to a few percent lower than the output setpoint. This action primarily occurs under the following conditions:

- Dropout: When there is insufficient input voltage to maintain the desired output voltage
- Overcurrent: When there is an overcurrent event that is not severe enough to trigger hiccup



Whether the output voltage falls due to high load or low input voltage, upon removal of the condition that caused the output to fall below the setpoint, the output voltage climbs at the same rate as during start-up. Even though hiccup does not trigger due to dropout, hiccup can in principal be triggered during recovery if the output voltage is below 40% of the output voltage setpoint for more than 64 clock cycles during recovery.

Figure 7-9. Recovery From Dropout

7.3.11 Protection Features

The LM656x0-Q1 includes a comprehensive set of safety features:

- Power-Good monitor with output UV and OV detection
- Overcurrent and short-circuit protection with HICCUP mode
- Thermal shutdown (TSD) protection

7.3.11.1 Power-Good Monitor (PG)

The LM656x0-Q1 includes a power-good function to simplify supply sequencing and supervision in a system. Use the power-good function to enable downstream circuits supplied by the LM656x0-Q1, to control downstream protection circuits such as load switches, or to turn on sequenced supplies.

PG monitors the output voltage with a window comparator through FB for adjustable-output settings and through BIAS for fixed-output configurations. PG switches to a high impedance, open-drain state when the output voltage is in regulation. When the output voltage is outside of a ±5% range from the voltage setpoint, PG is driven low, thus warning the system of an output overvoltage or undervoltage condition. A 130µs deglitch filter on the PG falling edge prevents false tripping of PG during transients. When the output voltage recovers to within the regulation window, a 2ms filter on the PG rising edge provides additional processing time for downstream components.

TI recommends using a 100kΩ pullup resistor from PG to the relevant rail, which is less than 30V. PG asserts low during soft start and when the LM656x0-Q1 is disabled.

7.3.11.2 Overcurrent and Short-Circuit Protection

The LM656x0-Q1 protects from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side power MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The high-side current is sensed when the high-side MOSFET turns on after a short blanking time. The high-side current is compared to the minimum of a fixed current setpoint, or the output of the voltage regulation loop minus slope compensation, every switching cycle.

When the low-side MOSFET is turned on, the current going through the MOSFET is also sensed and monitored. Like the high-side MOSFET, the low-side MOSFET turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if the current limit is exceeded, even if the oscillator normally starts a new switching cycle. Also, like the high-side device, there is a limit on the turn-off current amplitude. This is called the low-side current limit; see the *Electrical Characteristics* for values. Upon engaging low-side current limit, the low-side MOSFET stays on and the high-side MOSFET does not turn on. The low-side MOSFET turns off after

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the low-side current falls below the limit. The high-side MOSFET turns on again as long as at least one clock period has passed since the last time the high-side MOSFET turned on.

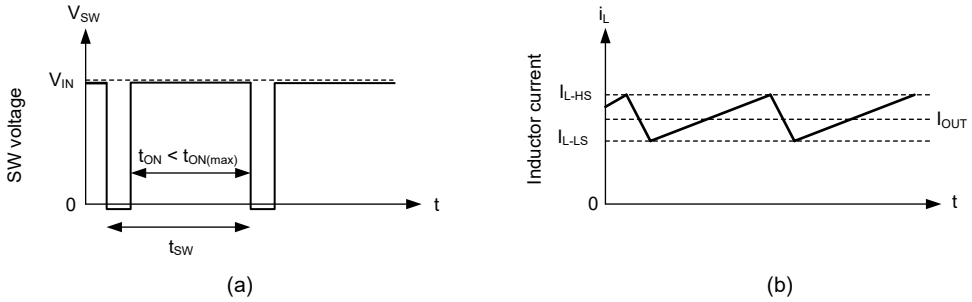

Figure 7-10. Current Limit Waveforms: Switch Voltage (a), Inductor Current (b)

The net effect of the operation of high-side and low-side current limits is that the IC operates in hysteretic control. Because the current waveform assumes values between I_{L-HS} and I_{L-LS}, the output current is close to the average of these two values unless the duty cycle is very high. After operating in current limit, hysteretic control is used and current does not increase as the output voltage approaches zero.

Upon removal of the overload condition, the device recovers as though in soft start; see Section 7.3.10.1 . Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.11.3 Hiccup-Mode Protection

The LM656x0-Q1 employs hiccup-mode protection when the following conditions are met for 64 consecutive clock cycles, corresponding to the hiccup-mode activation delay, t_{HICDLY}:

- A time interval greater than 5.3ms passes since soft start began. See Section 7.3.10.1.
- The output voltage is less than approximately 40% of the output voltage setpoint.
- The device does not operate in dropout (defined as having the PWM off-time controlled by COMP).

In hiccup mode, the device shuts down and attempts to restart after a delay of approximately 48ms when using internal soft start. When using external soft start, the delay increases by six times the increase in soft-start time. Hiccup mode helps to reduce the device power dissipation under severe overcurrent and short-circuit conditions.

7.3.11.4 Thermal Shutdown

Thermal shutdown limits the power dissipation of the LM656x0-Q1 by turning off the internal switches when the IC junction temperature exceeds 165°C (typical). Thermal shutdown does not trigger below 155°C. Once thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops by approximately 9°C. When the junction temperature falls below 156°C (typical), the LM656x0-Q1 attempts to soft start.

Even if the LM656x0-Q1 is in shutdown due to high junction temperature, VCC is still in regulation. To prevent overheating from a short circuit applied to VCC, the VCC bias supply subregulator has a reduced current limit while the device is in thermal shutdown. The VCC subregulator can only provide a few milliamperes of current during this shutdown condition.

7.3.12 Two-Phase, Single-Output Operation

Use two LM656x0-Q1 converter ICs for two-phase, single-output operation. Additional phases cannot be added. Configure the first and second devices as primary and secondary, respectively, according to Figure 7-11. This action disables the feedback error amplifier of the secondary IC, placing feedback error amplifier in a high-impedance state. As shown in Figure 7-11, connect FB of the secondary device to VCC. Furthermore, connect the COMP pins of the primary and secondary ICs together with minimal trace length. Add an external compensation network near the primary device. The internal compensation feature is not available when operating in a two-phase configuration.

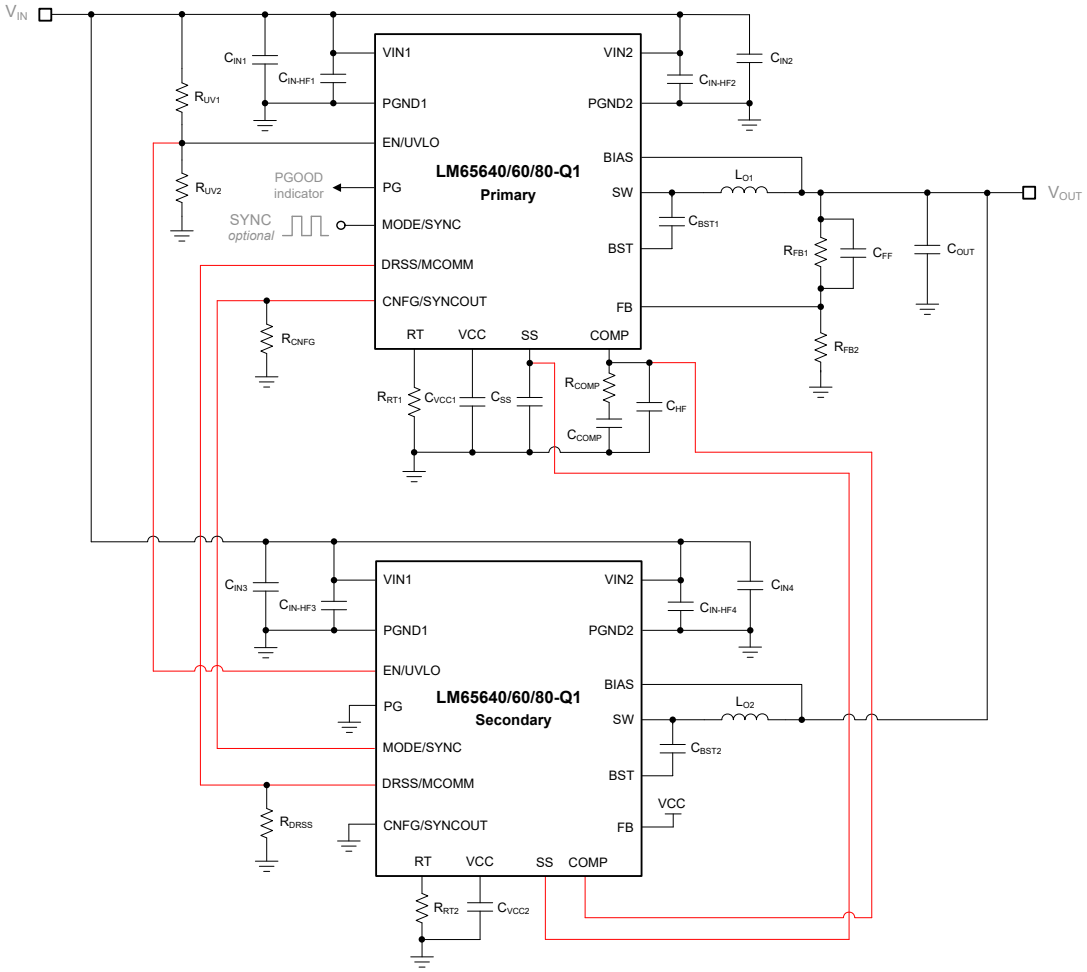

Figure 7-11. Simplified Schematic for Single-Output Dual-Phase Operation

Connect CNFG/SYNCOUT of the primary device to the MODE/SYNC of the secondary device. The SYNCOUT signal from the primary is 180° out-of-phase and facilitates interleaved operation. When operating in a two-phase configuration, enable both devices at the same time for start-up.

When configured for two-phase operation, DRSS/MCOMM conveys the mode information from the primary to the secondary device. A MCOMM high signal from the primary causes the secondary to operate in FPWM mode. Conversely, a MCOMM low signal from the primary sets the secondary in PFM mode. Tie the MCOMM pins of the primary and secondary devices together. Connect the SS pins of both primary and secondary devices to achieve fault communication.

See also *Benefits of a Multiphase Buck Converter* analog design journal and *Multiphase Buck Design From Start to Finish* application note.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

EN/UVLO provides electrical on and off control of the device. When the EN/UVLO voltage is below 0.9V, the device is in shutdown mode with an input quiescent current of less than 1µA.

7.4.2 Active Mode

The LM656x0-Q1 is in active mode when the following occur:

- EN/UVLO is above $V_{EN-TH(R)}$.
- V_{IN} is above $VIN_{UVLO(R)}$.

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- No fault conditions are present.

See Section 7.3.11 for protection features. The simplest way to enable the operation is to connect EN/UVLO to VIN, allowing start-up when the applied input voltage exceeds the $VIN_{UVLO(R)}$ of 3.4V (typical).

In active mode, the LM656x0-Q1 is in one of six sub-modes depending on the load current, input voltage, and output voltage:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current-mode operation
- Discontinuous conduction mode (DCM) while in AUTO mode when the load current is less than half of the inductor peak-to-peak ripple current. If the current continues to reduce, the device enters pulse frequency modulation (PFM) mode, which reduces the switching frequency to maintain regulation (this reduces switching losses, thus achieving higher efficiency at light loads).
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by $t_{ON(min)}$.
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load.
- A current-limiting condition where the output voltage remains above 40% of the output setpoint.
- Dropout mode when the switching frequency reduces to minimize dropout.
- Recovery from dropout – similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM656x0-Q1 is a family of buck converters that require relatively few external components to convert from a wide range of input voltages to a regulated output voltage at output currents up to 8A. A comprehensive quickstart calculator is available by download to expedite and streamline the process of designing of a LM656x0-Q1-based regulator circuit.

8.1.1 Power Train Components

A comprehensive understanding of the regulator power-train components is critical to successfully completing a synchronous buck regulator design. The following sections discuss the inductor, input and output capacitors, and the EMI input filter.

8.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 7 based on a peak inductor current given by Equation 8.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

$$I_{L(pk)} = I_{OUT} + \frac{\Delta I_L}{2} \quad (8)$$

Check the inductor data sheet to verify that the saturation current of the inductor is above the peak inductor current of a particular design. Ferrite designs have very low core loss and are often preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evident by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic where the inductance collapses abruptly upon exceeding the saturation current. This action results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

8.1.1.2 Output Capacitors

The output capacitor, C_{OUT}, conducts the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide very low ESR to reduce the output voltage ripple and noise, while polymer electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events. Equation 9 gives the output capacitance based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times F_{SW} \sqrt{\Delta V_{OUT}^2 + \left(R_{ESR} \times \Delta I_L\right)^2}} \quad (9)$$

The capacitor data sheet provides the ESR either explicitly as a specification or implicitly in the impedance vs. frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 10mΩ and above, and relatively high ESL, above 10nH. PCB traces contribute some parasitic resistance and

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inductance as well. Ceramic output capacitors have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Equation 10 gives an estimate for the output capacitance to meet output voltage limits during dynamic load current changes when the response is small-signal limited and set by the crossover frequency, f_C.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{2 \times \pi \times f_C \times \Delta V_{OUT}} \tag{10}$$

Ignoring the ESR term in Equation 9 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Then use Equation 10 to determine the capacitance is necessary to meet the load transient specification. Two to four 47µF, 10V, X7R, 1210, ceramic capacitors is a common choice for a 5V output with the LM656x0-Q1 converter. A 12V output often typically two to four 22µF, 25V, X7R, 1210 capacitors.

8.1.1.3 Input Capacitors

Use input capacitors to limit the input ripple voltage at the buck power stage due to high-di/dt switching currents. TI recommends using 1210 ceramic capacitors with X7R dielectric to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching power loop, position the input capacitors as close as possible to the VIN and PGND pin pairs. Equation 11 calculates the input capacitor RMS current for a single-phase buck regulator.

$$I_{CIN(rms)} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{\Delta I_L{}^2}{12} \right)} \tag{11}$$

The RMS current reaches a maximum of $I_{OUT}/2$ at D = 0.5. Ideally, the input voltage source provides the DC component of input current and the input capacitors provide the AC component. Neglecting inductor ripple current, the input capacitors for a buck regulator source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sink I_{IN} during the 1−D interval. Thus, the input capacitors conduct a squarewave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 12 calculates the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \tag{12}$$

Equation 13 calulcates the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \tag{13}$$

The LM656x0-Q1 provides VIN and PGND pins placed symmetrically on both sides of the package. This allows the input capacitors to be split and placed optimally with respect to the integrated power MOSFETs, thus improving the effectiveness of the input bypassing. The opposing current loops create self-cancelling fields, thus helping to mitigate both conducted and radiated emissions. Four 4.7µF or 10µF ceramic capacitors are sufficient for most applications. In addition, use a small case size (0402 or 0603) ceramic capacitor positioned at each input pin pair, [VIN1, PGND1] and [VIN2, PGND2], to reduce the effective impedance at high frequencies.

Using a two-phase regulator with 180° out-of-phase interleaved switching provides input ripple current cancellation and reduced input capacitor current stress. The above equations represent valid calculations with one phase disabled and the other phase fully loaded.

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8.1.1.4 EMI Filter

Switching regulators exhibit a negative input impedance, which is lowest at the minimum input voltage and maximum load. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the output impedance of the EMI filter must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \quad (14)$$

Based on the EMI filter in Figure 8-1, the design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the converter input.
- Select an input filter inductor L_{IN} between 1µH and 10µH. Use a lower value to reduce DC losses in a high-current design.
- Calculate input-side filter capacitance C_F.

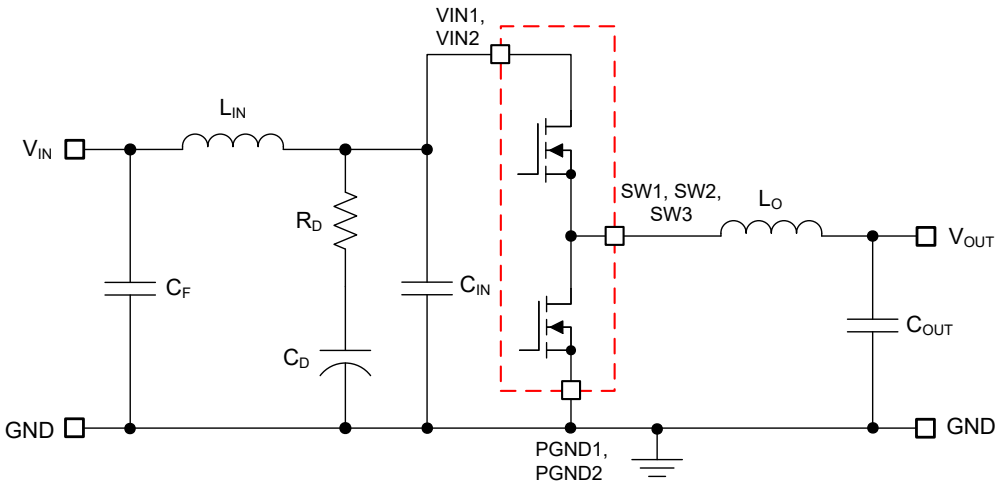

Figure 8-1. Passive π-Stage EMI Filter for a Buck Regulator

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying the result by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), Equation 15 calculates the required filter attenuation at the switching frequency as

$$Attn = 20\log\left(\frac{I_{L(pk)}}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \quad (15)$$

where

- V_{MAX} is the allowed emission level in dBµV from the applicable conducted EMI standard, for example, CISPR 25 Class 5.
- C_{IN} is the existing input capacitance of the regulator.
- D_{MAX} is the maximum duty cycle.
- $I_{L(pk)}$ is the peak inductor current.

In terms of EMI filter design, model the current at the input as a square-wave. Use Equation 16 to determine the EMI filter capacitance C_F.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \times F_{SW}}\right)^2 \quad (16)$$

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Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently low such that the input filter does not significantly affect the regulator loop gain. The impedance peaks at the filter resonant frequency. Equation 17 calculates the resonant frequency of the filter.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \quad (17)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Add damping when the output impedance of the filter is high at the resonant frequency (Q of the filter formed by L_{IN} and C_{IN} is too high). Use an electrolytic capacitor C_D for damping with a value given by Equation 18.

$$C_D \geq 4 \times C_{IN} \quad (18)$$

Use Equation 19 to select the damping resistor R_D.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (19)$$

8.1.2 Error Amplifier and Compensation

Figure 8-2 shows a Type-II compensator using a transconductance error amplifier (EA). The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{OEA}, and effective bandwidth-limiting capacitance, C_{BW}, as shown by Equation 20.

$$G_{EA(openloop)}(s) = -\frac{g_m \times R_{OEA}}{1 + s \times R_{OEA} \times C_{BW}} \quad (20)$$

The EA high-frequency pole is neglected in the above expression. Equation 21 expresses the compensator transfer function from output voltage to COMP, including the gain contribution from the feedback divider.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \times \frac{g_m \times R_{OEA} \times \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (21)$$

where

- V_{REF} is the feedback voltage reference
- g_m is the EA transconductance
- R_{OEA} is the EA output impedance

$$\omega_{z1} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (22)$$

$$\omega_{p1} = \frac{1}{R_{OEA} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{OEA} \times C_{COMP}} \quad (23)$$

$$\omega_{p2} = \frac{1}{R_{COMP} \times (C_{COMP} \,||\, (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \quad (24)$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, $R_{COMP} << R_{OEA}$ and $C_{COMP} >> C_{BW}$ and C_{HF}, so the approximations are valid. Figure 8-2 circles the poles in red and the zero in blue.

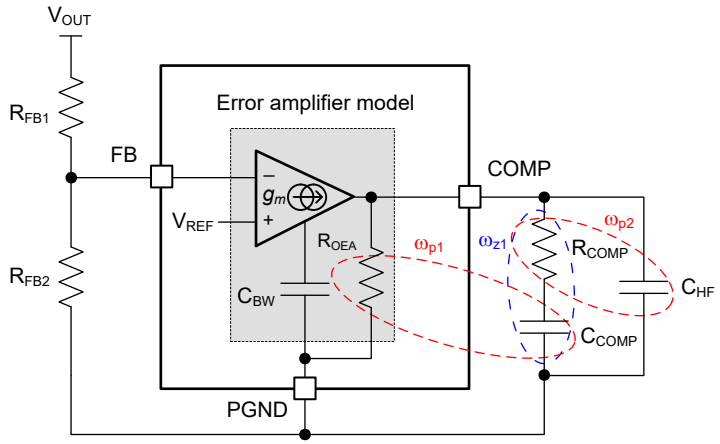

Figure 8-2. Error Amplifier and Compensation Network

8.1.3 Maximum Ambient Temperature

The junction temperature of the LM656x0-Q1 has a specified maximum of 150°C, which limits the power dissipation and thus the available load current. Equation 25 shows the relationships between the important parameters.

$$I_{OUT(max)} = \frac{T_J - T_A}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \quad (25)$$

where

- η = converter efficiency (not including the inductor loss)
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance from the IC junction to the local ambient, mainly through the PCB.

Clearly, higher values of T_A and $R_{\theta JA}$ reduce the available output current. The effective $R_{\theta JA}$ is a critical parameter and depends on numerous factors, including:

- IC power dissipation
- Air temperature and airflow
- PCB and copper heatsink areas
- Number of thermal vias under or near the package
- Adjacent component placement.

Estimate the IC power loss using the LM656x0-Q1 quickstart calculator. Alternatively, adjust the EVM to match the desired application requirements and the measure the power loss and resultant temperature rise. The JESD 51-7 value of $R_{\theta JA}$ reported in the Section 6.4 table was measured under a specific set of conditions rarely applicable to an actual application. As such, the value is not useful to estimate the thermal performance of the IC in a real application.

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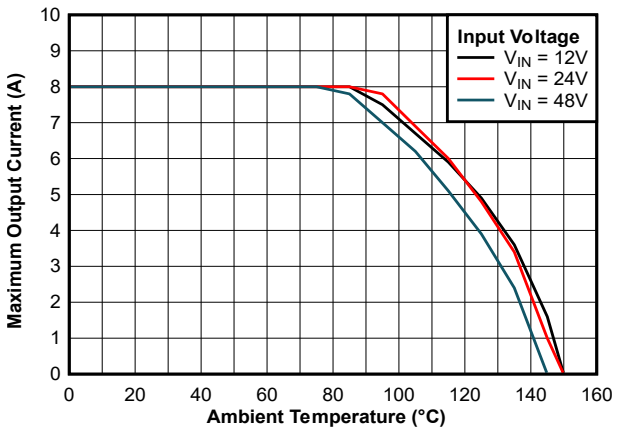
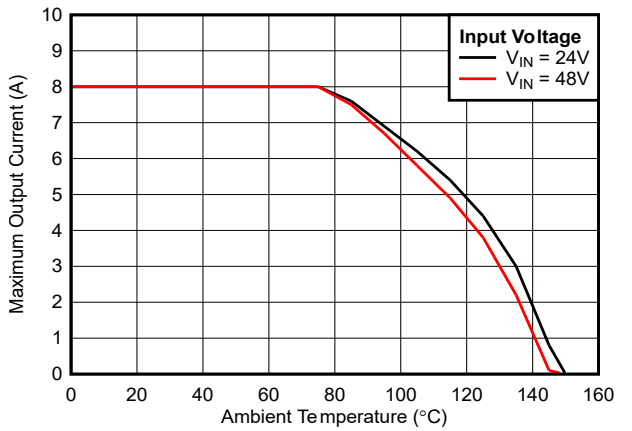
8.1.3.1 Derating Curves

Figure 8-3 to Figure 8-6 provide derating curves obtained using the LM65680-Q1 buck regulator EVM, giving an $R_{\theta JA}$ of approximately 18°C/W. The actual performance for a given application depends on the previously mentioned factors. Use the *Thermal Design Resources* as a guide for thermal design of the PCB and to estimate $R_{\theta JA}$ for a given application environment.



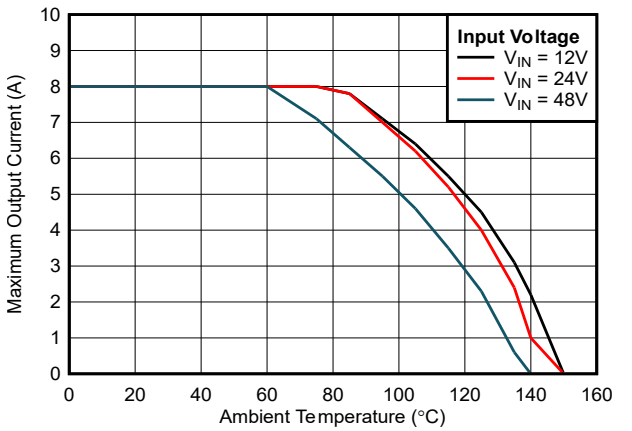
V_{IN} = 12V, 24V, 48V
V_{OUT} = 5V
F_{SW} = 400kHz
$R_{\theta JA}$ = 18°C/W

Figure 8-3. LM65680-Q1 Output Current Derating vs Ambient Temperature ($5V_{OUT}$, 400kHz)



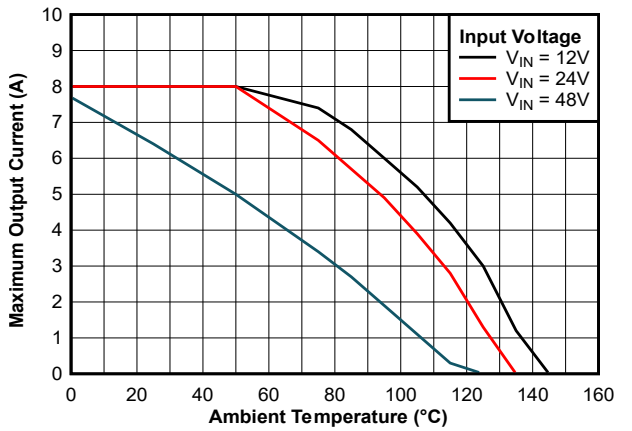
V_{IN} = 24V, 48V
V_{OUT} = 12V
F_{SW} = 400kHz
$R_{\theta JA}$ = 18°C/W

Figure 8-4. LM65680-Q1 Output Current Derating vs Ambient Temperature ($12V_{OUT}$, 400kHz)



V_{IN} = 12V, 24V, 48V
V_{OUT} = 5V
F_{SW} = 800kHz
$R_{\theta JA}$ = 18°C/W

Figure 8-5. LM65680-Q1 Output Current Derating vs Ambient Temperature ($5V_{OUT}$, 800kHz)



V_{IN} = 12V, 24V, 48V
V_{OUT} = 5V
F_{SW} = 2.1MHz
$R_{\theta JA}$ = 18°C/W

Figure 8-6. LM65680-Q1 Output Current Derating vs Ambient Temperature ($5V_{OUT}$, 2.1MHz)

8.2 Typical Applications

The LM656x0-Q1 family of synchronous buck converters function over a wide range of external components and system parameters. Connecting CNFG/SYNCOUT to VCC sets the converter to use internal compensation, allowing COMP to be left open circuit or tied to PGND. However, the internal compensation requires a minimum amount of output capacitance for stability. Use Equation 26 to find a suitable value for the output capacitance as

$$C_{OUT(INTCOMP)} = \frac{K_{INTCOMP}}{f_C \times V_{OUT}} \quad (26)$$

where

- f_C is the target loop crossover frequency, typically set at 10% to 15% of switching frequency (up to a maximum of 100kHz);
- $K_{INTCOMP}$ = 36.5, 27.2 and 20.1 for the LM65680-Q1, LM65660-Q1 and LM65640-Q1, respectively.

As a quick reference, Table 8-1 provides typical component values for a range of application parameters when using internal compensation and 3.3V or 5V fixed output setting. Meanwhile, Table 8-2, Table 8-3 and Table 8-4 provide typical component values for the 8A, 6A and 4A devices, respectively, when using a feedback divider to set the output voltage.

The tables outline designs that correspond to a typical input voltage of 48V and reference minimum *effective* output capacitance values (derated for voltage and temperature).

Table 8-1. Typical Component Values for Fixed Output Voltage (3.3V or 5V) and Internal Compensation

OUTPUT VOLTAGE	SWITCHING FREQUENCY	FB	LM65640-Q1, 4A		LM65660-Q1, 6A		LM65680-Q1, 8A	
			L_O	C_{OUT}	L_O	C_{OUT}	L_O	C_{OUT}
3.3V	400kHz	GND	5.6µH	130µF	4.7µH	180µF	3.3µH	220µF
5V		VCC	8.2µH	80µF	5.6µH	120µF	3.9µH	150µF
3.3V	2.2MHz	GND	1µH	55µF	0.82µH	75µF	0.56µH	100µF
5V		VCC	1.5µH	40µF	1µH	50µF	0.82µH	70µF

Table 8-2. Typical Component Values for the LM65680-Q1 8A Device With Adjustable Output Voltage and Internal Compensation

OUTPUT VOLTAGE	SWITCHING FREQUENCY	L_O	C_{OUT}	R_{FB1}	R_{FB2}	C_{FF}
3.3V	400kHz	3.3µH	220µF	78.7kΩ	24.9kΩ	10pF
5V		3.9µH	150µF		15kΩ	10pF
12V		8.2µH	60µF	210kΩ	15kΩ	3.3pF
3.3V	2.2MHz	0.56µH	100µF	78.7kΩ	24.9kΩ	2.2pF
5V		0.82µH	70µF		15kΩ	2.2pF
12V		1µH	30µF	210kΩ	15kΩ	–

Table 8-3. Typical Component Values for the LM65660-Q1 6A Device With Adjustable Output Voltage and Internal Compensation

OUTPUT VOLTAGE	SWITCHING FREQUENCY	L_O	C_{OUT}	R_{FB1}	R_{FB2}	C_{FF}
3.3V	400kHz	4.7µH	150µF	78.7kΩ	24.9kΩ	10pF
5V		5.6µH	100µF		15kΩ	10pF
12V		10µH	44µF	210kΩ	15kΩ	2.2pF
3.3V	2.2MHz	0.82µH	75µF	78.7kΩ	24.9kΩ	4.7pF
5V		1µH	50µF		15kΩ	4.7pF
12V		2.2µH	22µF	210kΩ	15kΩ	–

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Table 8-4. Typical Component Values for the LM65640-Q1 4A Device With Adjustable Output Voltage and Internal Compensation

OUTPUT VOLTAGE	SWITCHING FREQUENCY	L_O	C_{OUT}	R_{FB1}	R_{FB2}	C_{FF}
3.3V	400kHz	6.8µH	120µF	78.7kΩ	24.9kΩ	10pF
5V		8.2µH	80µF		15kΩ	10pF
12V		15µH	35µF	210kΩ	15kΩ	3.3pF
3.3V	2.2MHz	1µH	50µF	78.7kΩ	24.9kΩ	4.7pF
5V		1.5µH	35µF		15kΩ	4.7pF
12V		3.3µH	15µF	210kΩ	15kΩ	–

Note

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM656x0-Q1-powered implementation, see the *TI Designs* reference design library.

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8.2.1 Design 1 – 5V, 8A Synchronous Buck Regulator With Wide Input Voltage Range and High Efficiency

Figure 8-7 shows a typical buck regulator circuit with the LM65680-Q1 that provides a regulated 5V output at 8A from a nominal 48V input.

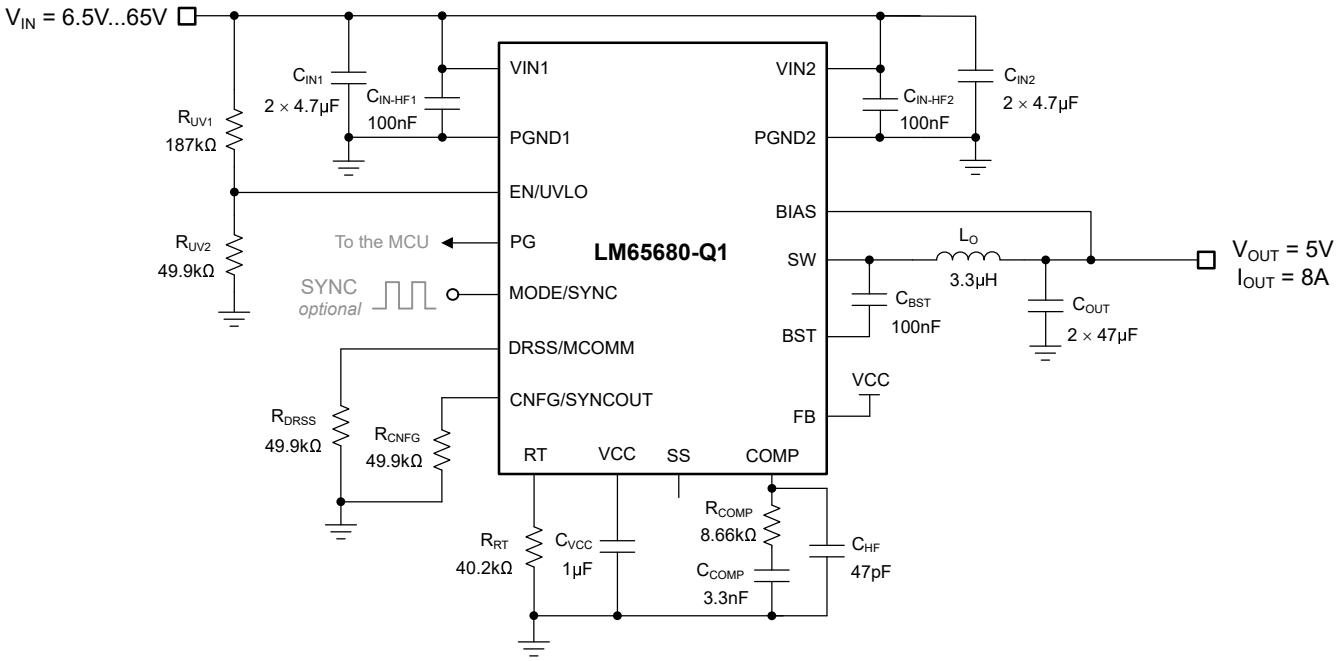

Figure 8-7. Application Circuit 1 With the LM65680-Q1 8A Buck Converter at 400kHz

Note

This and subsequent design examples are provided herein to showcase the LM656x0-Q1 converter in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to provide stability, particularly at low input voltage and high output current operating conditions. See also Section 8.4.

8.2.1.1 Design Requirements

Table 8-5 shows the specifications for a 5V, 8A buck regulator with a switching frequency of 400kHz. In this example, the target half-load and full-load efficiencies are 92% and 90%, respectively, based on a nominal input voltage of 48V that ranges from 9V to 60V steady state, with short-term transients as low as 6.5V and as high as 70V.

Table 8-5. Detailed Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	9V to 60V
Minimum transient input voltage (cold crank)	6.5V
Maximum transient input voltage (load dump)	65V
Input UVLO turn-on threshold	5.9V
Output voltage	5V
Output current	0A to 8A
Switching frequency	400kHz
Soft-start time	5.3ms (default internal setting)
EMI mitigation	DRSS off, slew-rate control on
Ambient temperature range	–40°C to 85°C

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Resistor R_{RT} of 40.2kΩ sets the free-running switching frequency at 400kHz, and an optional SYNC input signal allows adjustment of the switching frequency from 320kHz to 480kHz for this specific application. Leaving the SS pin open sets the soft-start time to the fixed internal setting of 5.3ms. In terms of control loop performance, the target loop crossover frequency is 60kHz with a phase margin greater than 50°.

Table 8-6 cites the selected buck regulator powertrain components, with many of the components available from multiple vendors. This design uses a low-DCR inductor with composite core material and an all-ceramic output capacitor implementation.

Table 8-6. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	VENDOR(1)	PART NUMBER
C_{IN1}, C_{IN2}	4	4.7µF, 100V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32DC72A475K
			TDK	CGA6M3X7S2A475K
C_{IN-HF1}, C_{IN-HF2}	2	100nF, 100V, X7R, 0603, ceramic, AEC-Q200	Murata	GCJ188R72A104M
C_{OUT}	2	47µF, 10V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71A476K
			TDK	CNA6P1X7S1A476M
L_O	1	3.3µH, 5.9mΩ, 13.4A, 6.71 × 6.51 × 6.1mm, AEC-Q200	Coilcraft	XGL6060-332MEC
		3.3µH, 6mΩ, 15.6A, 6.6 × 6.4 × 6.1mm, AEC-Q200	Würth Elektronik	744393465033
		3.3µH, 6.3mΩ, 16A, 6.6 × 6.4 × 6mm, AEC-Q200	XFMRS	XFHCL6060HC-3R3M
		3.3µH, 8.4mΩ, 18.6A, 8.05 × 7.5 × 5.4mm, AEC-Q200	Cyntec	VCHD075D-3R3MS6
		4.7µH, 5.7mΩ, 26.5A, 11.3 × 10 × 6mm, AEC-Q200	Würth Elektronik	744393665047
U_1	1	LM65680-Q1 65V, 8A synchronous buck converter, AEC-Q100	Texas Instruments	LM65680

8.2.1.2 Detailed Design Procedure

The following design procedure applies to Figure 8-7 and Table 8-5.

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM656x0-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and typically results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors in the power stage, and hence a more compact design. For this application example, connect a standard resistor value of 40.2kΩ from RT to PGND to set a frequency of 400kHz. Alternatively, tie RT to PGND. See also Section 7.3.5.

$$R_{RT}[k\Omega] = \frac{16.4}{F_{SW}[MHz]} - 0.633 = \frac{16.4}{0.4} - 0.633 = 40.36k\Omega \quad (27)$$

8.2.1.2.3 Buck Inductor Selection

1. Use Equation 28 to calculate the buck inductance based on an inductor peak-to-peak ripple current of 30% to 40% of the converter maximum-rated current. Select a standard value for L_O of 3.3µH.

$$L_O = \frac{V_{OUT}}{F_{SW} \times \Delta I_{LO}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{5V}{400kHz \times 3.2A} \times \left(1 - \frac{5V}{48V}\right) = 3.5\mu H \quad (28)$$

2. Use Equation 29 to calculate the peak inductor current at maximum steady-state input voltage. Subharmonic oscillation occurs with peak current-mode control at a duty cycle greater than 50%. For design simplification, the LM65680-Q1 has an internal slope compensation ramp proportional to the switching frequency that adds to the current-sense signal to damp any tendency toward subharmonic oscillation.

$$I_{LO(pk)} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L_O} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = 8A + \frac{5V}{2 \times 400kHz \times 3.3\mu H} \times \left(1 - \frac{5V}{65V}\right) = 9.75A \quad (29)$$

3. To avoid subharmonic oscillation, choose a buck inductance greater than that given by Equation 30. An effective maximum inductance value sets the minimum ripple current amplitude required for current-mode control to perform correctly. As a general rule, the minimum inductor ripple current must be no less than approximately 10% of the converter maximum-rated current under nominal conditions. This limit applies to applications where the switch duty cycle becomes greater than or equal to 50% under any operating condition.

$$L_{O,min} \geq M \times \frac{V_{OUT}}{F_{SW}} \quad (30)$$

where

- M = 0.16, 0.21 and 0.29 for the LM65680-Q1, LM65660-Q1 and LM65640-Q1, respectively.

8.2.1.2.4 Input Capacitor Selection

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage. In general, the ripple current splits between the input capacitors based on the relative impedance of the capacitors at the switching frequency.

1. Select the input capacitors with sufficient voltage and RMS current ratings. Use Equation 31 to calculate the RMS current in the input capacitors, where the worst-case operating point is at an input voltage of 10V, corresponding to 50% duty cycle.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{D \times (1 - D)} = 8A \times \sqrt{0.5 \times (1 - 0.5)} = 4A \quad (31)$$

2. Use Equation 32 to find the required input capacitance, assuming an approximate 10% duty cycle for 48V-to-5V conversion:

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR,Cin} \times I_{OUT})} = \frac{0.1 \times (1 - 0.1) \times 8A}{400kHz \times (480mV - 2m\Omega \times 8A)} = 4.8\mu F \quad (32)$$

where

- ΔV_{IN} is the specification for the peak-to-peak input ripple voltage.
- $R_{ESR,Cin}$ is the effective ESR of the input capacitors.

3. Recognizing the voltage coefficient of ceramic capacitors, select four 4.7µF, 100V, X7R, 1210 ceramic input capacitors. Each capacitor has an effective capacitance value of approximately 1.3µF at 48VDC. Place these capacitors adjacent to the input pin pairs, [VIN1, PGND1] and [VIN2, PGND2].
4. Use Equation 33 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{C_{IN} \times F_{SW}} + R_{ESR,Cin} \times I_{OUT} = \frac{8A \times 0.1 \times (1 - 0.1)}{4.2\mu F \times 400kHz} + 2m\Omega \times 8A = 0.44V \quad (33)$$

5. Connect 100nF, 100V, X7R, 0603 ceramic capacitors directly across [VIN1, PGND1] and [VIN2, PGND2] to supply the high-di/dt current during switching transitions. Such capacitors offer high self-resonant frequency

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(SRF) and low effective impedance above 100MHz. The result is low power-loop parasitic inductance, which reduces switch-node voltage overshoot and ringing. See also Section 8.5.1.

8.2.1.2.5 Output Capacitors

1. Given a load transient deviation specification of 4% V_{OUT} and a loop crossover frequency of 60kHz, use Equation 34 to estimate the output capacitance required for a 50% load step.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{2\pi \times f_C \times \Delta V_{OUT}} = \frac{4A}{2\pi \times 60kHz \times 0.2} = 53\mu F \quad (34)$$

2. Noting the voltage coefficient of ceramic capacitors (where the effective capacitance decreases significantly with applied voltage), select two 47µF, 10V, X7S, 1210 ceramic output capacitors, which gives an effective capacitance of 56µF at 5VDC.
3. Use Equation 35 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \frac{\Delta I_{LO}}{8 \times C_{OUT} \times F_{SW}} + R_{ESR,Cout} \times \Delta I_{LO} = \frac{3.2A}{8 \times 56\mu F \times 400kHz} + 1m\Omega \times 3.2A = 21mV \quad (35)$$

where

- ΔI_{LO} is the peak-to-peak inductor ripple current. For this example, 40% inductor ripple current corresponds to 3.2A.
- 56µF is the total effective (derated) output capacitance at 5V.
- $R_{ESR,Cout}$ of 1mΩ is the effective ESR of the output capacitors.

8.2.1.2.6 Output Voltage Setpoint

Connect FB to VCC to establish a 5V fixed output setting with the LM65680-Q1. Use BIAS for voltage sensing by connecting directly to the regulator output at the point of load. Note that bode plot measurement is possible only with the adjustable-output implementation where signal injection occurs at the top of the feedback divider.

8.2.1.2.7 Compensation Components

Choose compensation components for a stable control loop using the following procedure.

1. Set the crossover frequency between 10% and 20% of the switching frequency. With f_C specified as 60kHz in this example, and assuming an effective output capacitance of 56µF (two 47µF, 10V ceramic capacitors derated for an applied voltage of 5VDC) and negligible ESR, use Equation 36 to calculate R_{COMP}. Choose a standard value for R_{COMP} of 8.66kΩ.

$$R_{COMP} = 2\pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{C_{OUT}}{g_m \times G} = 2\pi \times 60kHz \times \frac{5V}{0.8V} \times \frac{56\mu F}{1mS \times 14.6A/V} = 9.04k\Omega \quad (36)$$

where

- G = 14.6A/V, 10.9A/V and 8.1A/V for the LM65680-Q1, LM65660-Q1 and LM65640-Q1, respectively, is a factor related to the internal currrent-sense gain.

2. Calculate C_{COMP} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 3.3nF.

$$C_{COMP} = \frac{10}{2\pi \times f_C \times R_{COMP}} = \frac{10}{2 \times \pi \times 60kHz \times 8.66k\Omega} = 3.1nF \quad (37)$$

In general, set the time constant of R_{COMP} and C_{COMP} at approximately 25µs to maintain a fast settling time of the output voltage following a load transient.

3. Calculate C_{HF} to create a pole at the lower of the ESR zero frequency or at half switching frequency (to attenuate high-frequency noise coupling from the output to COMP). C_{BW} is the parasitic capacitance of the error amplifier at COMP. Select a standard value for C_{HF} of 47pF.

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$$C_{HF} = \frac{1}{2\pi \times \frac{F_{SW}}{2} \times R_{COMP}} - C_{BW} = \frac{1}{2\pi \times \frac{400kHz}{2} \times 8.66k\Omega} - 40pF = 51pF \quad (38)$$

As an alternative, use internal compensation by connecting CNFG/SYNCOUT to VCC. Leave COMP open circuit or connected to PGND.

Note

With external compensation, set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout (when the input voltage is less than the output voltage setpoint and the COMP voltage rails high).

8.2.1.2.8 Setting the Input Voltage UVLO

Calculate the input UVLO divider resistors, designated as R_{UV1} and R_{UV2} in Figure 8-7, given an input voltage turn-on threshold specified as 5.9V. First, choose a value for R_{UV2} of 49.9kΩ (within the typical range of 10kΩ to 100kΩ) and then use Equation 39 and Equation 40 to calculate R_{UV1} and $V_{IN(off)}$.

$$R_{UV1} = R_{UV2} \times \left(\frac{V_{IN(on)}}{V_{EN-TH(R)}} - 1\right) = 49.9k\Omega \times \left(\frac{5.9V}{1.25V} - 1\right) = 187k\Omega \quad (39)$$

$$V_{IN(off)} = V_{IN(on)} \times (1 - V_{EN-HYS\%}) = 5.9V \times (1 - 0.2) = 4.72V \quad (40)$$

where $V_{IN(on)}$ and $V_{IN(off)}$ are the input UVLO turn-on and turn-off thresholds, and $V_{EN-TH(R)}$ and $V_{EN-HYS\%}$ are the rising threshold and hysteresis of the precision enable comparator.

8.2.1.2.9 EMI Mitigation, R_{DRSS}

Connect a 49.9kΩ resistor from DRSS/MCOMM to PGND to enable slew-rate control and disable DRSS. Alternatively, leave the pin open circuit to enable both features or tie to GND to disable both features. See also Table 7-4.

8.2.1.2.10 Bootstrap Capacitor, C_{BST}

The LM656x0-Q1 requires a bootstrap capacitor connected between BST and SW. This capacitor stores energy used to supply the gate driver for the high-side power MOSFET, along with other critical control circuits. Use a 100nF, X7R ceramic capacitor rated at 10V or higher.

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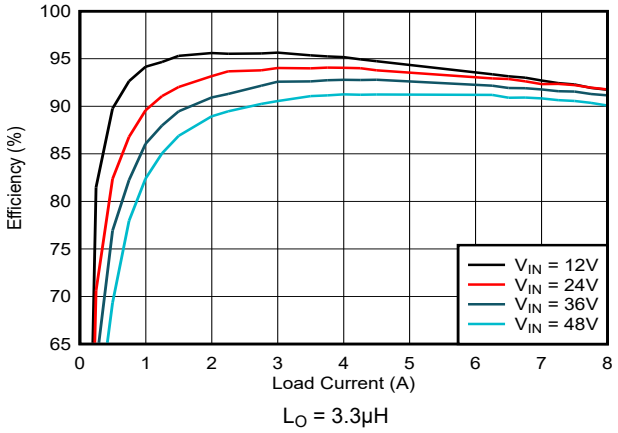
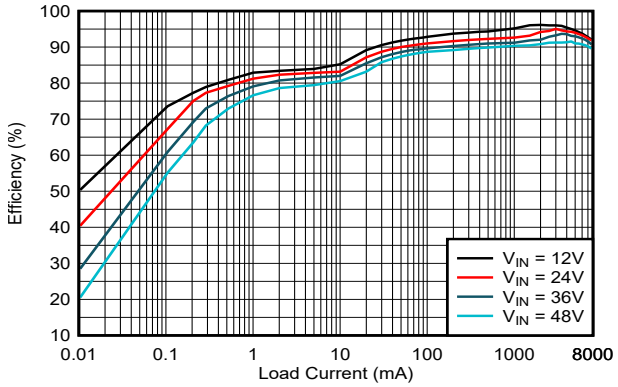
8.2.1.3 Application Curves

Unless otherwise specified, V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 8A, F_{SW} = 400kHz, T_A = 25°C, FPWM.



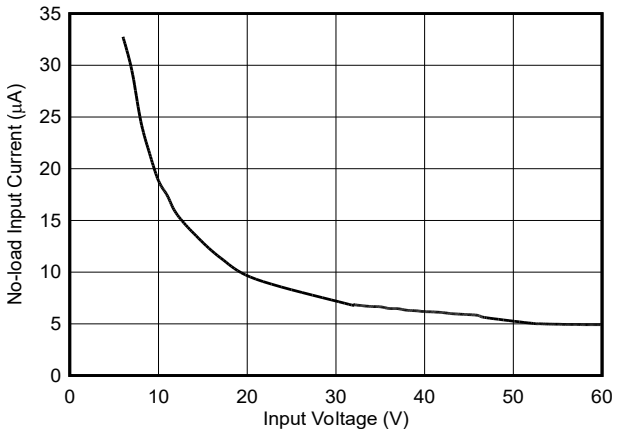
L_O = 3.3µH

Figure 8-8. Efficiency vs I_{OUT}



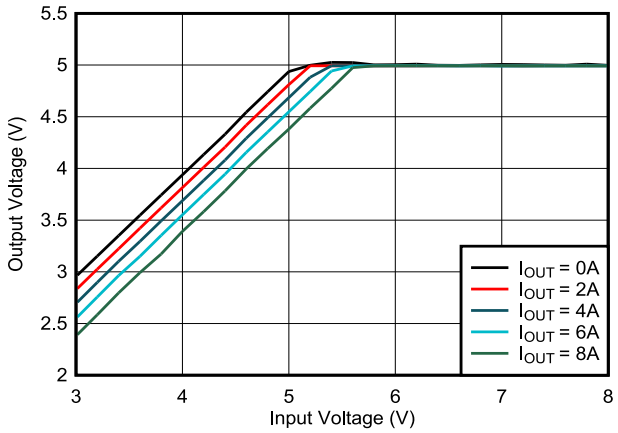
L_O = 5.6µH

Figure 8-9. Efficiency vs I_{OUT}, AUTO



AUTO mode External compensation L_O = 5.6µH

Figure 8-10. No-Load Input Current



L_O = 3.3µH

Figure 8-11. Output Voltage Behavior in Dropout

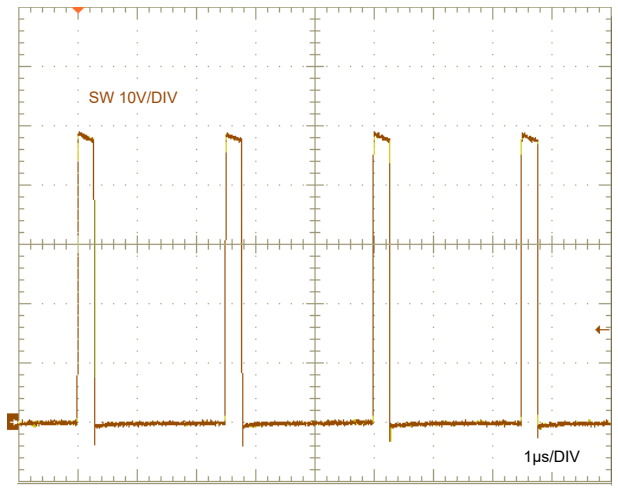


Figure 8-12. Full-Load Switching

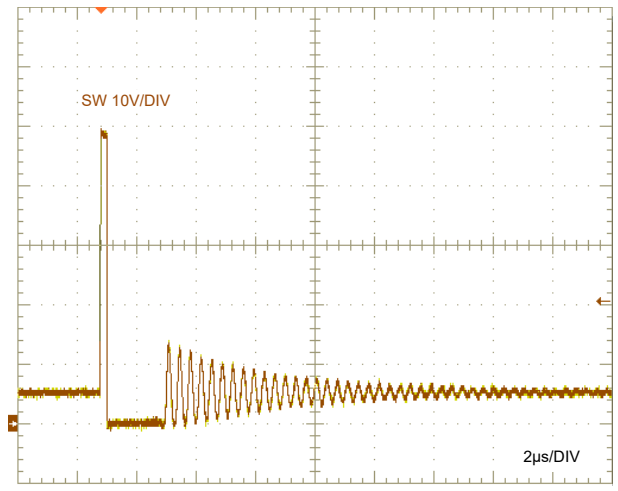


Figure 8-13. No-Load Switching, AUTO

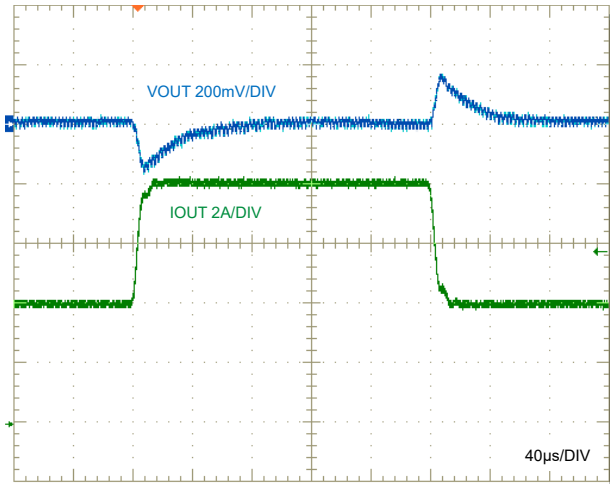


Figure 8-14. Load Transient Response, 4A to 8A

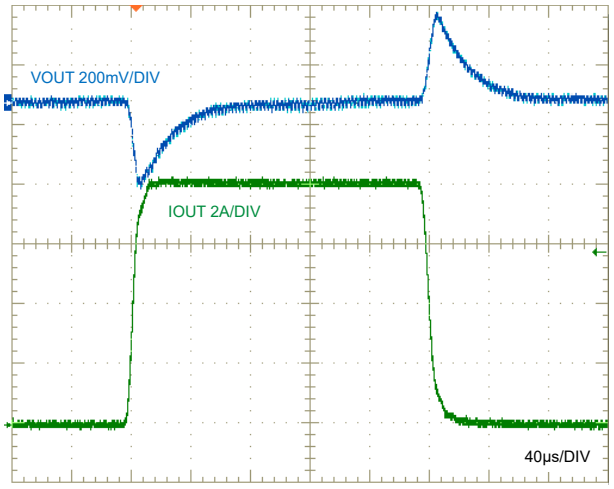
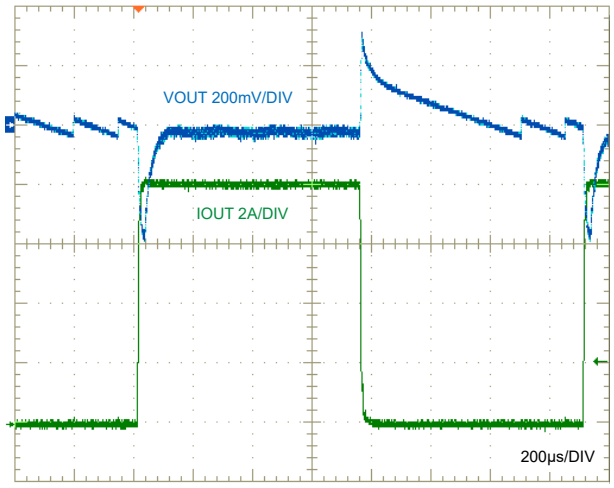
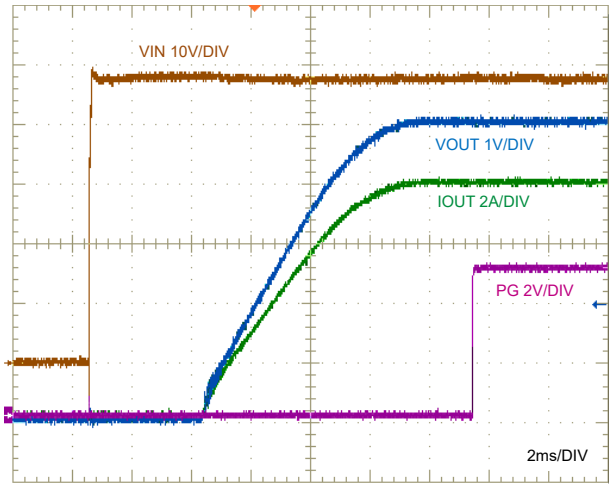


Figure 8-15. Load Transient Response, 0A to 8A



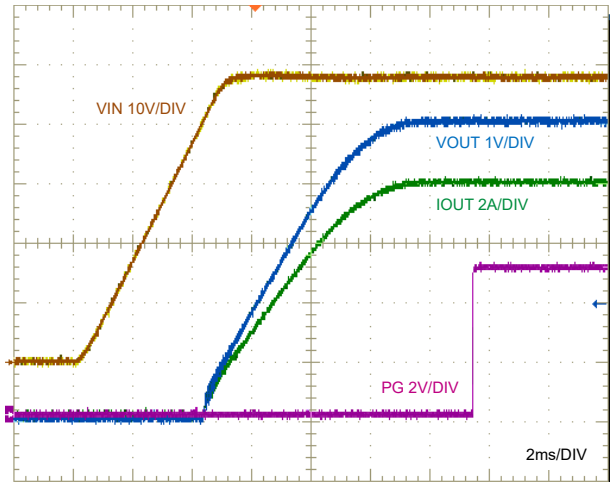
AUTO mode

Figure 8-16. Load Transient Response, 0A to 8A



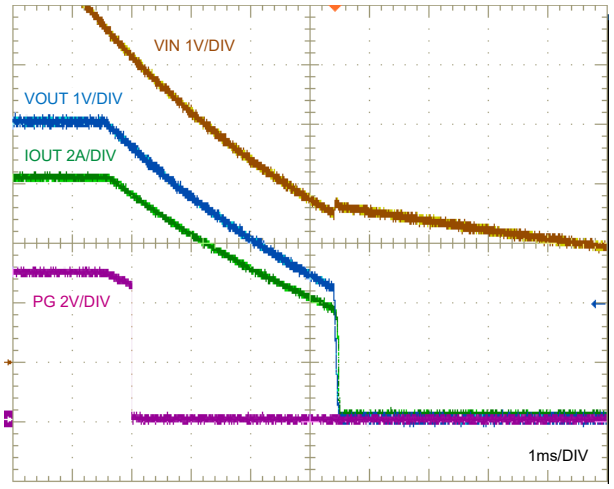
V_{IN} stepped to 48V 0.62Ω load

Figure 8-17. V_{IN} Start-up Characteristic



V_{IN} ramped at 10V/ms 0.62Ω load

Figure 8-18. V_{IN} Start-up Characteristic



0.62Ω load

Figure 8-19. V_{IN} Shutdown Characteristic

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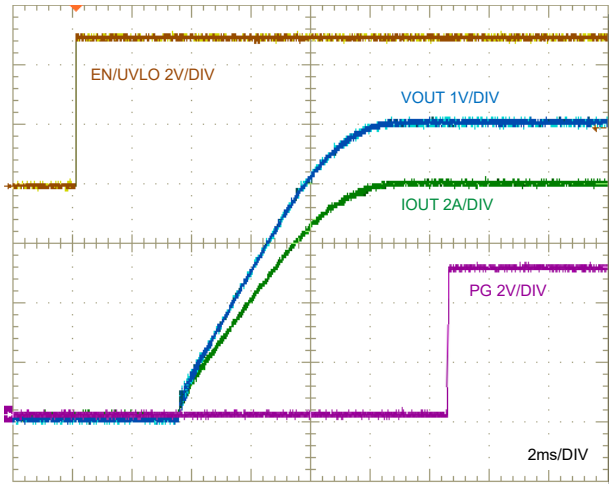
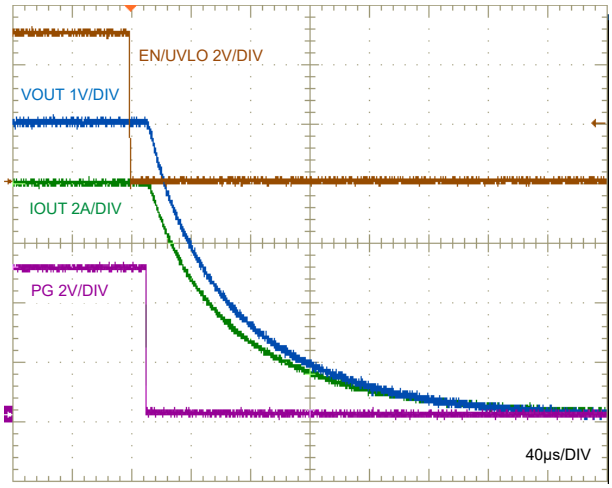


0.62Ω load

Figure 8-20. Enable ON Characteristic



0.62Ω load

Figure 8-21. Enable OFF Characteristic

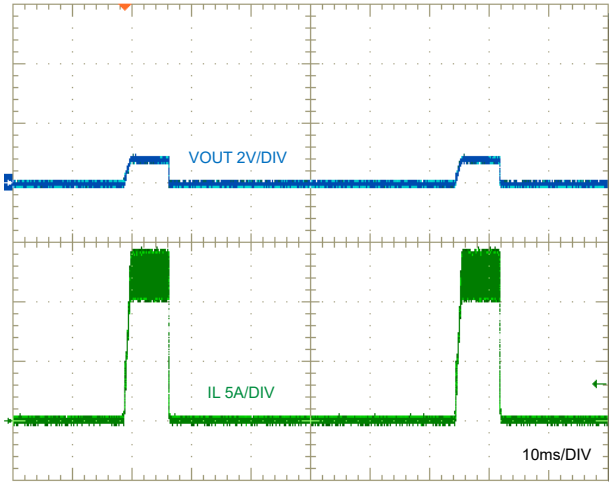


Figure 8-22. Hiccup in an Overload Condition

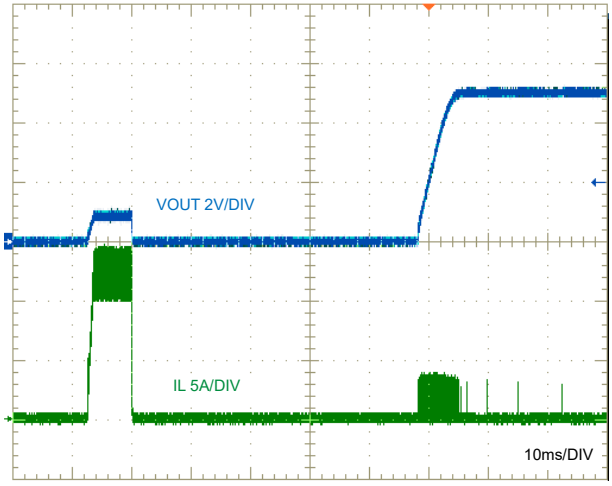
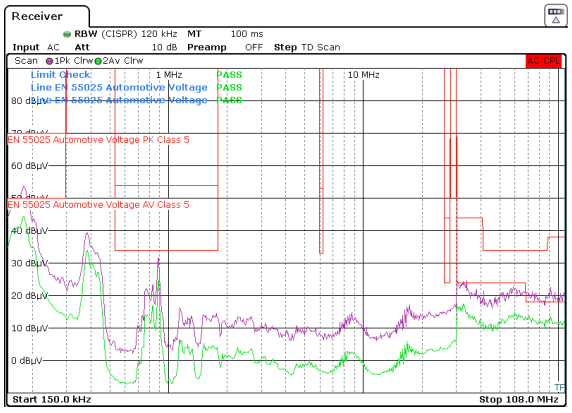


Figure 8-23. Recovery From an Overload Condition



Purple: PK detect
Green: AVG detect

DRSS and SR Control ON

Figure 8-24. CISPR 25 Class 5 Conducted Emissions, 150kHz to 108MHz

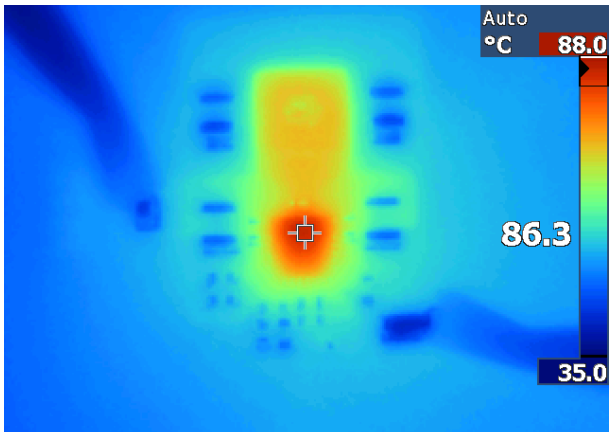


Figure 8-25. Thermal Performance, No Airflow

8.2.2 Design 2 – High Efficiency, 48V to 12V, 8A, 400kHz Synchronous Buck Regulator

Figure 8-26 shows the schematic diagram of a single-output synchronous buck regulator with an output voltage of 12V and a rated load current of 8A. Based on a nominal input voltage of 48V that ranges from 18V to 65V, the target full-load efficiency for this example is 95%.

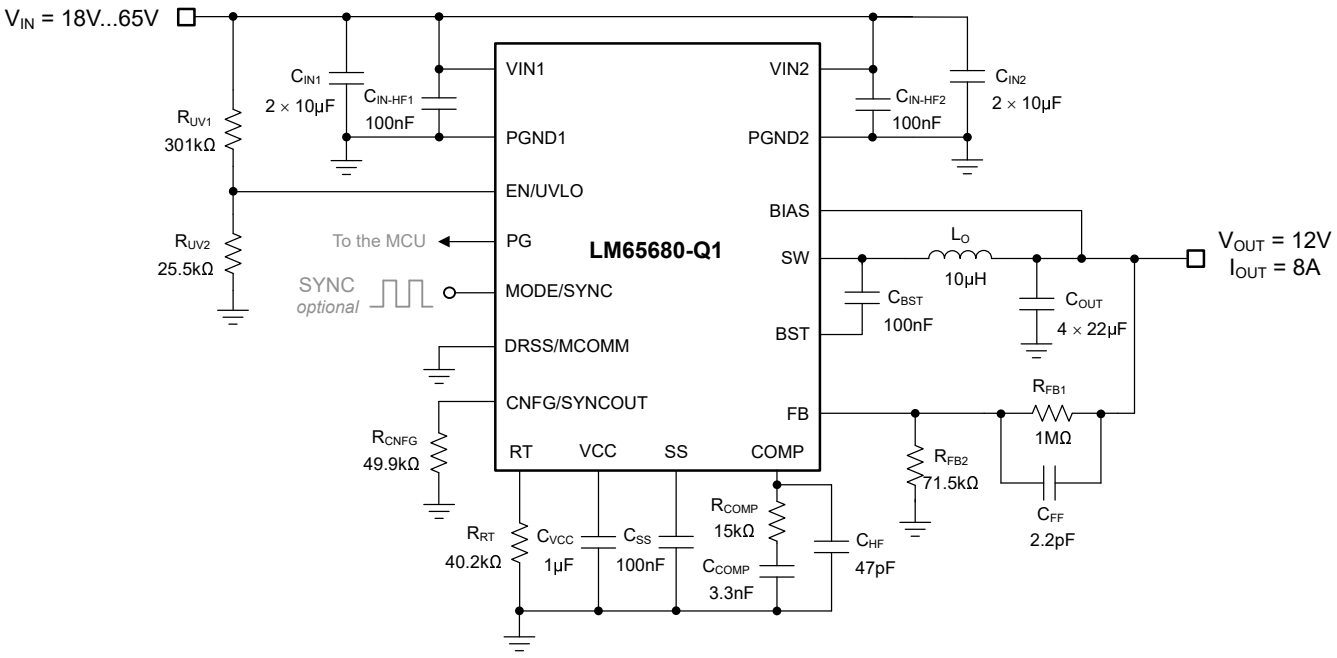


Figure 8-26. Application Circuit 2 With a 12V Output Voltage Using the LM65680-Q1

8.2.2.1 Design Requirements

The following example provides design information based on the specifications in Table 8-7.

Table 8-7. Detailed Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady state)	24V to 60V
Minimum transient input voltage (cold crank)	18V
Maximum transient input voltage (load dump)	65V
Input voltage UVLO turn on	16V
Output voltage	12V
Output current	0A to 8A
Output voltage regulation	±1%
Switching frequency	400kHz
Loop crossover frequency, phase margin	50kHz, 55°
Soft-start time	6ms

The switching frequency is set at 400kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 50kHz with a phase margin greater than 55°.

Table 8-8 cites the selected buck regulator powertrain components, with many of the components available from multiple vendors. This design uses a low-DCR inductor with composite core material and an all-ceramic output capacitor implementation.

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Table 8-8. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	VENDOR(1)	PART NUMBER
C_{IN1}, C_{IN2}	4	10µF, 100V, X7R, 1210, ceramic, AEC-Q200	Murata	GCM32EC72A106KEC2
			TDK	CGA6P1X7R2A106K
C_{IN-HF1}, C_{IN-HF2}	2	100nF, 100V, X7R, 0603, ceramic, AEC-Q200	Murata	GCJ188R72A104M
C_{OUT}	4	22µF, 25V, X7S, 1210, ceramic, AEC-Q200	Murata	GCM32EC71E226KE36
		22µF, 25V, X7R, 1210, ceramic, AEC-Q200	TDK	CGA6P3X7R1E226M
L_O	1	6.8µH, 12.5mΩ, 10.9A, 6.6 × 6.4 × 6.1mm, AEC-Q200	Würth Elektronik	744393465068
		6.8µH, 12.7mΩ, 10.5A, 6.6 × 6.4 × 6mm, AEC-Q200	XFMRS	XFHCL6060HC-6R8M
		8.2µH, 10.7mΩ, 19.5A, 11.3 × 10 × 6mm, AEC-Q200	Würth Elektronik	744393665082
		U_1	1	LM65680-Q1 65V, 8A synchronous buck converter, AEC-Q100

(1) See the *Third-Party Products Disclaimer*.

8.2.2.2 Detailed Design Procedure

The following design procedure applies to Figure 8-26 and Table 8-8.

8.2.2.2.1 Buck Inductor Selection

Use Equation 41 to calculate the required buck inductance based on a 40% inductor ripple current specification at nominal input voltage. Select a standard value for L_O of 6.8µH.

$$L_O = \frac{V_{OUT}}{F_{SW} \times \Delta I_{LO}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{12V}{400kHz \times 3.2A} \times \left(1 - \frac{12V}{48V}\right) = 7\mu H \quad (41)$$

8.2.2.2.2 Input Capacitor Selection

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings. Use Equation 42 to calculate the RMS current in the input capacitors, where the worst-case operating point is at an input voltage of 24V, corresponding to 50% duty cycle.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{D \times (1 - D)} = 8A \times \sqrt{0.5 \times (1 - 0.5)} = 4A \quad (42)$$

2. Use Equation 43 to find the required input capacitance, assuming a 25% duty cycle for 48V-to-12V conversion:

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR,Cin} \times I_{OUT})} = \frac{0.25 \times (1 - 0.25) \times 8A}{400kHz \times (480mV - 2m\Omega \times 8A)} = 8.1\mu F \quad (43)$$

3. Recognizing the voltage coefficient of ceramic capacitors, select four 10µF, 100V, X7R, 1210 ceramic input capacitors. Each capacitor has an effective capacitance value of approximately 2.3µF at 48VDC. Place these capacitors adjacent to the input pin pairs, [VIN1, PGND1] and [VIN2, PGND2].
4. Use Equation 44 to calculate the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{C_{IN} \times F_{SW}} + R_{ESR,\,Cin} \times I_{OUT} = \frac{8A \times 0.25 \times (1 - 0.25)}{9.2\mu F \times 400kHz} + 2m\Omega \times 8A = 0.42V \quad (44)$$

5. Connect 100nF, 100V, X7R, 0603 ceramic capacitors directly across [VIN1, PGND1] and [VIN2, PGND2] to supply high-di/dt current during switching transitions.

8.2.2.2.3 Output Capacitors

1. Given a specification for the load transient deviation of 3% V_{OUT} and a loop crossover frequency of 50kHz, use Equation 45 to estimate the output capacitance required for a 50% load step.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{2\pi \times f_C \times \Delta V_{OUT}} = \frac{4A}{2\pi \times 50kHz \times 0.36V} = 35\mu F \quad (45)$$

2. Noting the voltage coefficient of ceramic capacitors (where the effective capacitance decreases significantly with applied voltage), select four 22µF, 25V, X7R, 1210 ceramic output capacitors to give an effective capacitance of 32µF at 12VDC.
3. Use Equation 46 to estimate the peak-to-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \frac{\Delta I_{LO}}{8 \times C_{OUT} \times F_{SW}} + R_{ESR,Cout} \times \Delta I_{LO} = \frac{3.2A}{8 \times 32\mu F \times 400kHz} + 1m\Omega \times 3.2A = 34.5mV \quad (46)$$

where

- ΔI_{LO} is the peak-to-peak inductor ripple current, where 40% in this example corresponds to 3.2A.
- $R_{ESR,Cout}$ of 1mΩ is the effective ESR of the four paralleled output capacitors.

8.2.2.2.4 Output Voltage Setpoint

The adjustable output version of the LM656x0-Q1 uses a feedback divider network to set the output voltage. The divider network comprises upper and lower feedback resistors designated as R_{FB1} and R_{FB2}, respectively. The feedback divider resistances are a compromise between excessive noise pickup and quiescent current consumption. Lower resistances reduce noise sensitivity but impact light-load efficiency. A recommended starting value for R_{FB2} is 10kΩ with a maximum value of 100kΩ.

According to Equation 47, the parallel combination of R_{FB1} and R_{FB2} must be greater than 4kΩ and less than 100kΩ. This limit is set as the converter must reliably detect the state of FB during the start-up sequence to establish the output voltage configuration (fixed or adjustable output voltage setting).

$$4k\Omega \leq R_{FB1} \| R_{FB2} \leq 100k\Omega \quad (47)$$

Setting R_{FB1} and R_{FB2} to 210kΩ and 15kΩ, respectively, gives an output voltage setpoint of exactly 12V.

$$R_{FB1} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{FB2} = \left(\frac{12V}{0.8V} - 1\right) \times 15k\Omega = 210k\Omega \quad (48)$$

8.2.2.2.5 Compensation Components

Choose components for external compensation using the following procedure.

1. Set the crossover frequency between 10% and 20% of the switching frequency. With f_C specified as 50kHz in this example, and assuming an effective output capacitance of 32µF (four 22µF, 25V ceramic capacitors derated for an applied voltage of 12VDC) and negligible ESR, use Equation 49 to calculate R_{COMP}

$$R_{COMP} = 2\pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{C_{OUT}}{g_m \times G} = 2\pi \times 50kHz \times \frac{12V}{0.8V} \times \frac{32\mu F}{1mS \times 14.6S} = 10.3k\Omega \quad (49)$$

where

- G = 14.6A/V, 10.9A/V and 8.1A/V for the LM65680-Q1, LM65660-Q1 and LM65640-Q1, respectively, is a factor related to the internal currrent-sense gain.

Choose a standard value for R_{COMP} of 10kΩ.

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2. Calculate C_{COMP} to create a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Choose a standard value for C_{COMP} of 3.3nF.

$$C_{COMP} = \frac{10}{2\pi \times f_C \times R_{COMP}} = \frac{10}{2\pi \times 50kHz \times 10k\Omega} = 3.18nF \quad (50)$$

   In general, set the time constant of R_{COMP} and C_{COMP} at approximately 25µs to maintain a fast settling time of the output voltage following a load transient.
3. Calculate C_{HF} to create a pole at the lower of the ESR zero frequency or at half switching frequency (to attenuate high-frequency noise coupling from the output to COMP). Select a standard value for C_{HF} of 47pF.

$$C_{HF} = \frac{1}{2\pi \times \frac{F_{SW}}{2} \times R_{COMP}} - C_{BW} = \frac{1}{2\pi \times \frac{400kHz}{2} \times 10k\Omega} - 40pF = 39pF \quad (51)$$

Alternatively, use internal compensation by connecting CNFG/SYNCOUT to VCC. Leave COMP open circuit or connected to PGND.

8.2.2.2.6 Feedforward Capacitor

While the addition of feedforward capacitor C_{FF} does not change the response of the system at DC or lower frequencies, the capacitor helps reduce the impedance from V_{OUT} to FB at higher frequencies. A high-frequency deviation of the output voltage (due to a fast load transient) couples to the FB node, allowing the error amplifier to respond immediately.

Addition of the C_{FF} capacitor creates an additional pole and zero in the frequency domain. The zero contributes phase boost at crossover to improve the phase margin. Meanwhile, the pole helps to rolloff the gain above crossover and increase the gain margin. Equation 52 and Equation 53 give the zero and pole frequencies as:

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (52)$$

$$f_P = \frac{1}{2\pi \times (R_{FB1} || R_{FB2}) \times C_{FF}} \quad (53)$$

Optimize the value of C_{FF} to provide optimal phase boost at crossover. Position the the zero and pole frequencies according to Equation 54 such that $f_{C,NO-FF}$, the crossover frequency without feedforward, is between the zero and pole frequencies created by C_{FF}.

$$f_{C,NO-FF} = \sqrt{f_Z \times f_P} \quad (54)$$

Substituting Equation 52 and Equation 53 into Equation 54 results in Equation 55, which is now a function of R_{FB1}, R_{FB2}, and $f_{C,NO-FF}$.

$$C_{FF,OPT} = \frac{\sqrt{R_{FB1} + R_{FB2}}}{2\pi \times f_{C,NO-FF} \times R_{FB1} \times \sqrt{R_{FB2}}} = \frac{\sqrt{\frac{V_{OUT}}{V_{REF}}}}{2\pi \times f_{C,NO-FF} \times R_{FB1}} \quad (55)$$

where $C_{FF,OPT}$ is the feedforward capacitance that provides maximum phase boost.

As this design requires only 10° of phase boost, a value for C_{FF} of 2.2pF is sufficient. Use the quickstart calculator to check the bode plot and stability parameters, and then verify the final design during bench evaluation. In any event, TI recommends to leave a placeholder for C_{FF} in the PCB layout for added design flexibility.

8.2.2.2.7 Soft-Start Capacitor

The soft-start feature of the LM656x0-Q1 allows the converter to gradually reach the steady-state operating point, thus reducing start-up stresses and inrush current. If the SS pin is left open, the soft-start time defaults to 5.3ms. Alternatively, set a soft-start time greater than 5.3ms with a capacitor from SS to PGND. Use Equation 56

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to calculate the SS capacitance for the 6ms time specified in this example. Choose a standard value for C_{SS} of 100nF.

$$C_{SS}[nF] = 16.7 \times t_{SS}[ms] = 16.7 \times 6ms = 100.2nF \quad (56)$$

8.2.2.3 Application Curves

Unless otherwise specified, V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 8A, F_{SW} = 400kHz, T_A = 25°C, FPWM.

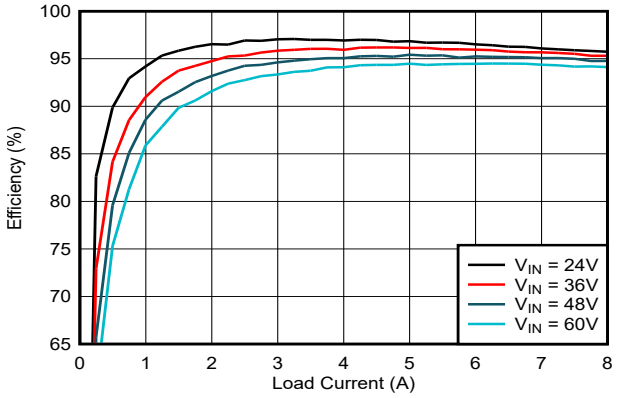
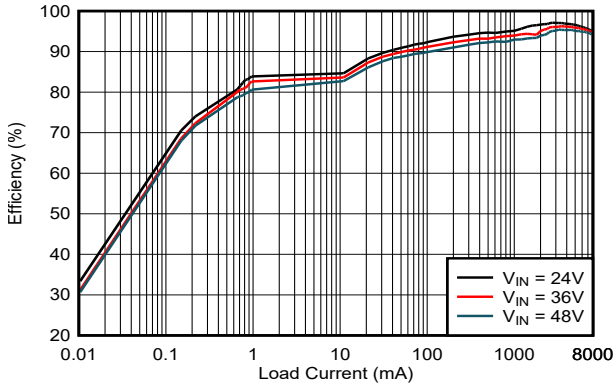


Figure 8-27. Efficiency vs I_{OUT}



L_O = 10µH

Figure 8-28. Efficiency vs I_{OUT}, AUTO

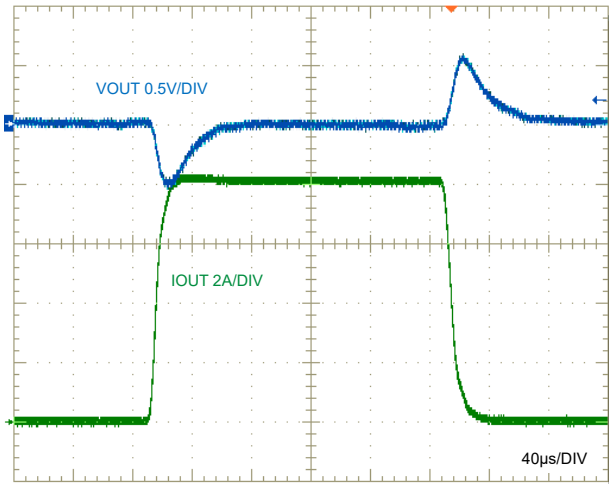


Figure 8-29. Load Transient Response, 0A to 8A

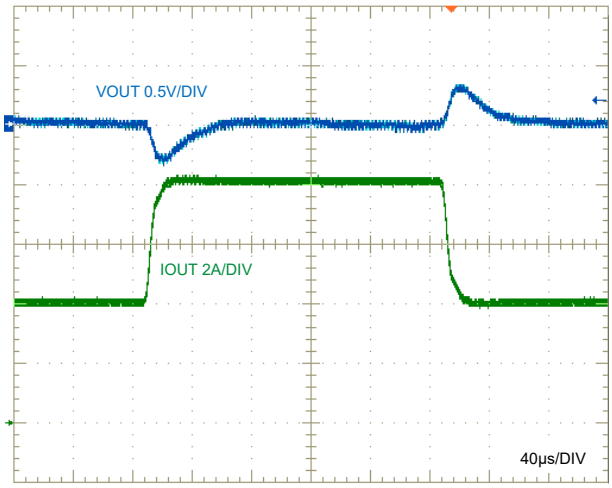
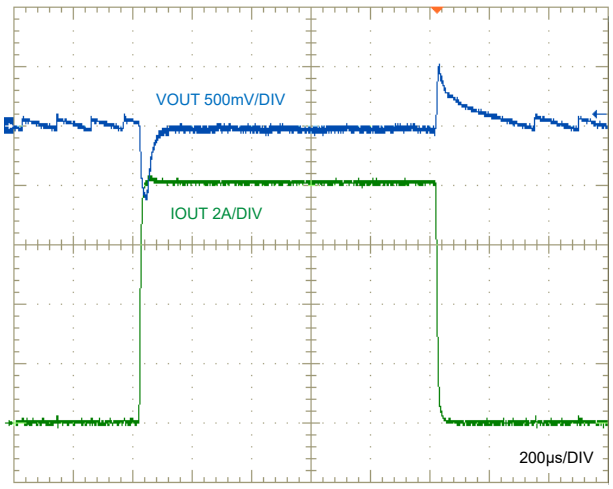


Figure 8-30. Load Transient Response, 4A to 8A



AUTO mode

Figure 8-31. Load Transient Response, 0A to 8A

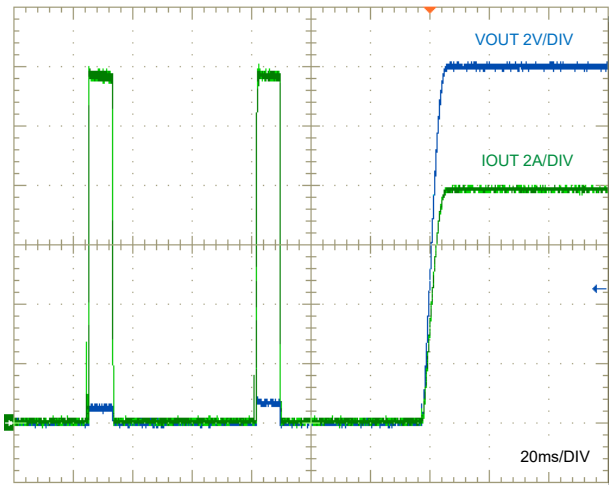


Figure 8-32. Hiccup Mode and Short-Circuit Recovery

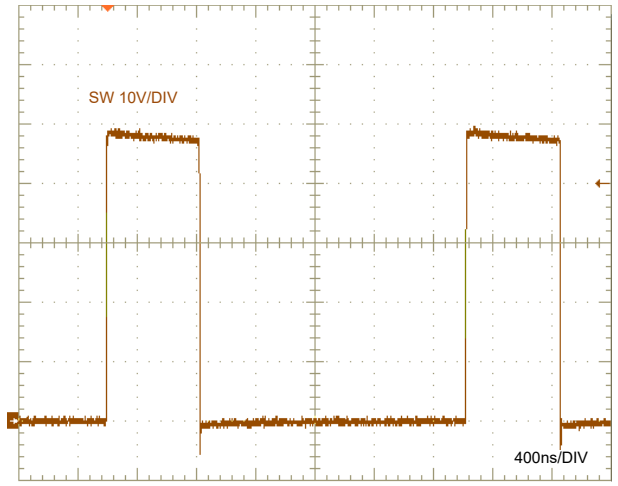


Figure 8-33. Full-Load Switching

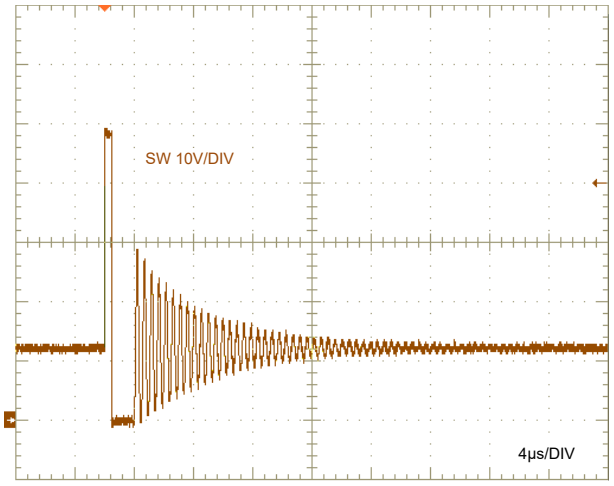


Figure 8-34. No-Load Switching, AUTO

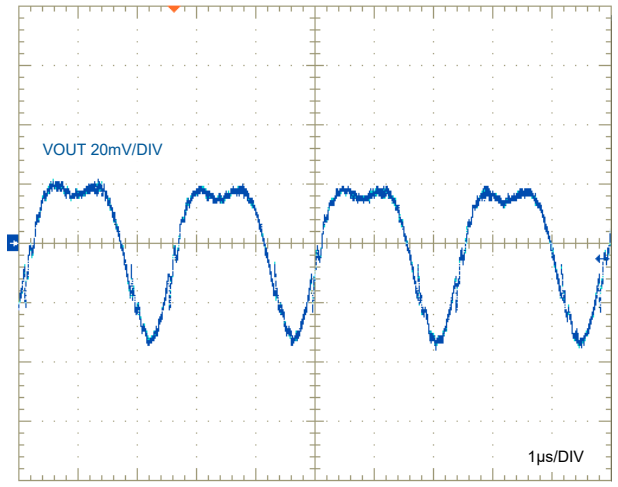


Figure 8-35. V_{OUT} Ripple

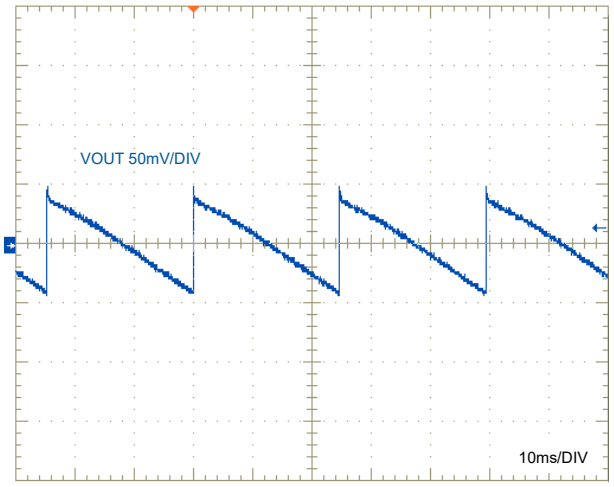
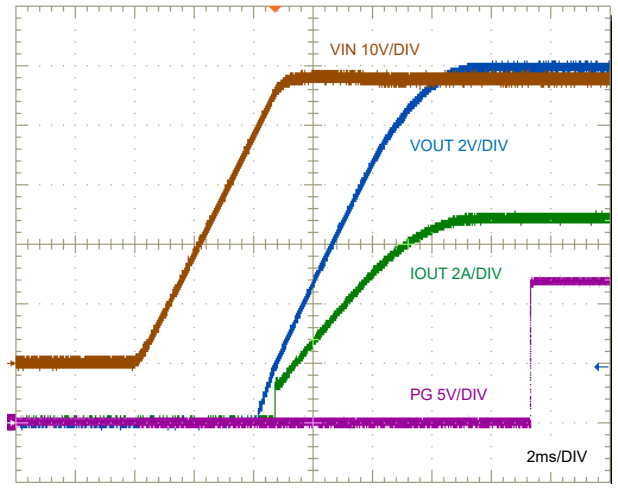
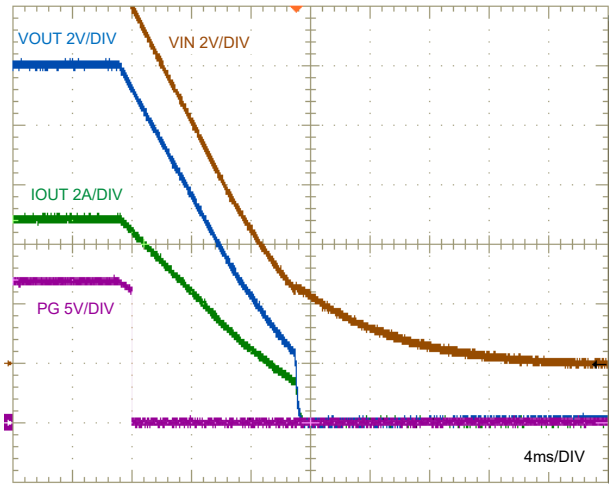


Figure 8-36. V_{OUT} Ripple, No Load, AUTO



V_{IN} ramped at 10V/ms 1.5Ω constant-resistance load

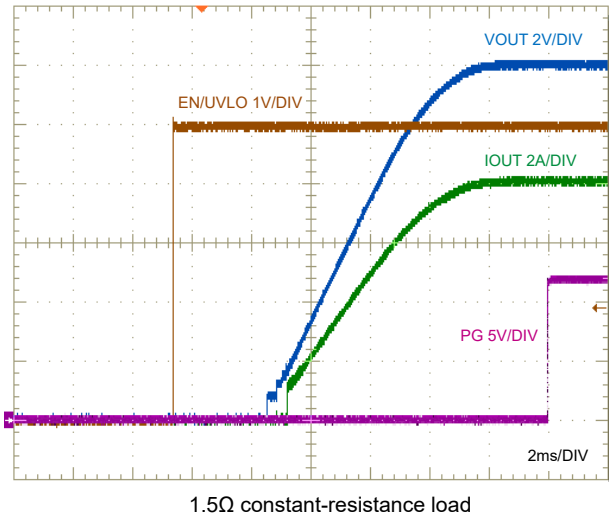
Figure 8-37. V_{IN} Start-up Characteristic



1.5Ω constant-resistance load

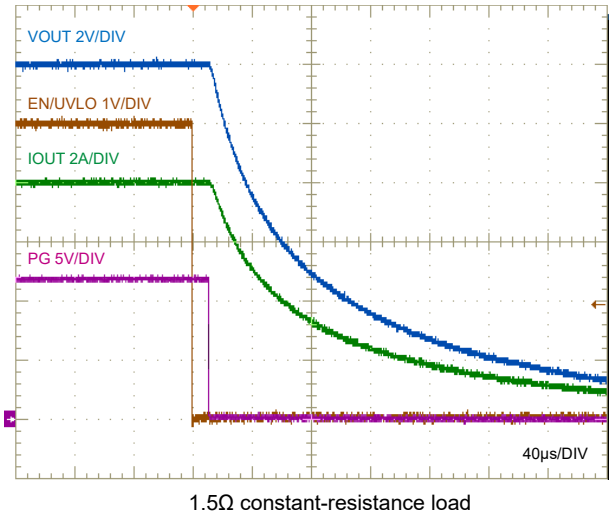
Figure 8-38. V_{IN} Shutdown Characteristic

ADVANCE INFORMATION



1.5Ω constant-resistance load

Figure 8-39. Enable ON Characteristic



1.5Ω constant-resistance load

Figure 8-40. Enable OFF Characteristic

ADVANCE INFORMATION

8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not leave EN/UVLO open circuit.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make the project a success.

8.4 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with the following equation.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (57)$$

where

η is the efficiency.

If the regulator connects to the input supply through long wires or PCB traces, take special care to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output, depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to resolve such issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 22µF to 68µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal body diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the output and the input supply.

ADVANCE INFORMATION

8.5 Layout

8.5.1 Layout Guidelines

Proper PCB design and layout is important in high-current, fast-switching DC/DC regulator circuits (with high current and voltage slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the regulator depends to a large extent on PCB layout.

Figure 8-41 denotes the high-frequency switching power loops of the LM656x0-Q1 power stage. The topological architecture of a buck converter means that particularly high di/dt current flows in the power MOSFETs and input capacitors, and reducing the parasitic inductance by minimizing the effective power loop areas becomes mandatory. Note the dual and symmetrical arrangement of the input capacitors based on the VIN and PGND pins located on each side of the IC package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.

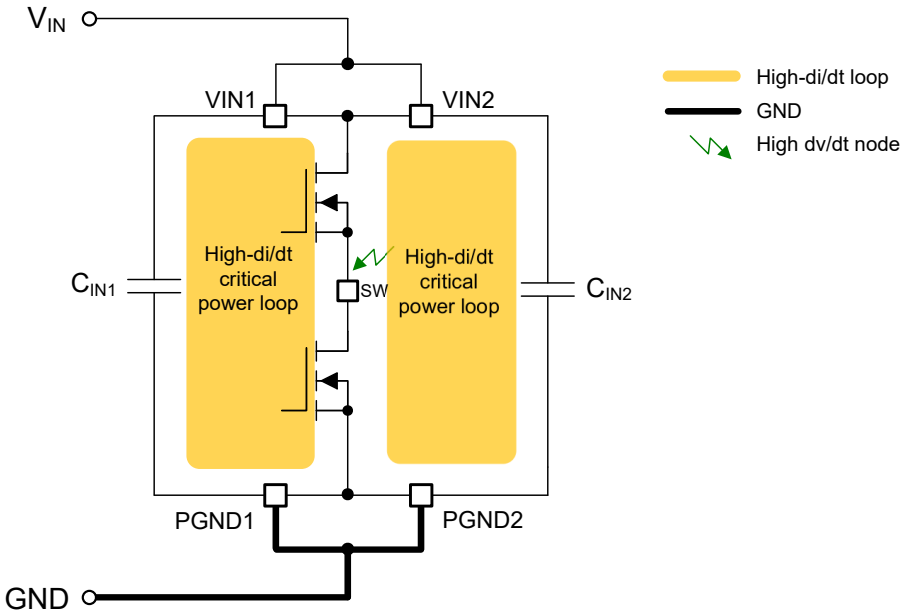


Figure 8-41. Buck Symmetric Power Loops

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC regulator performance, including thermals and EMI signature. Figure 8-42 shows a recommended layout of the LM656x0-Q1 with optimized placement and routing of the power-stage and small-signal components..

- *Place the input capacitors as close as possible to the input pin pairs [VIN1, PGND1] and [VIN2, PGND2]*: The respective VIN and PGND pins pairs are close together (with an NC pin in between to increase clearance), thus simplifying input capacitor placement. The eQFN package provides VIN and PGND pins on either side of the package to provide a symmetrical layout that helps to minimize switching noise and EMI.
  - Use low-ESR ceramic capacitors with X7R or X7S dielectric from VIN1 to PGND1 and VIN2 to PGND2. Place an 0603 capacitor close to each pin pair for high-frequency bypass. Use an adjacent 1210 capacitor on each side for bulk capacitance.
  - Ground return paths for both the input and output capacitors must consist of localized top-side planes that connect to the PGND1 and PGND2 pins.
  - Use a wide polygon plane on a lower PCB layer to connect VIN1 and VIN2 together and to the input supply.
- *Use a solid ground plane on the PCB layer beneath the top layer with the IC*: This plane acts as a noise shield and a heat dissipation path. Using the PCB layer directly below the IC minimizes the magnetic field associated with the currents in the switching loops, thus reducing parasitic inductance and switch voltage overshoot and ringing. Use numerous thermal vias near PGND1 and PGND2 for heatsinking to the inner ground planes.

- *Make the VIN, VOUT, and GND bus connections as wide as possible*: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter, thus maximizing efficiency.
- *Locate the buck inductor close to the SW1, SW2, and SW3 pins*: Use a short, wide connection trace from the converter SW pins to the inductor. At the same time, minimize the length (and area) of this high-dv/dt surface to help reduce capacitive coupling and radiated EMI. Connect the dotted terminal of the inductor to the SW pins.
- *Place the VCC and BOOT capacitors close to the respective pins*: The VCC and boostrap capacitors represent the supplies for the internal low-side and high-side MOSFET gate drivers, respectively, and thus carry high-frequency currents. Locate C_{VCC} close to the VCC and PGND2 pins. Connect C_{BST} close to the BST and SW3 pins.
- *Place the feedback divider as close as possible to the FB pin*: For adjustable output versions of the LM656x0-Q1, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This placement reduces the FB trace length and related noise coupling. The FB pin is the input to the voltage-loop error amplifier and represents a high-impedance node sensitive to noise. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the switch node) that can capacitively couple into the feedback path of the converter. For fixed-output versions, connect FB high or low as needed.
- *Provide enough PCB area for proper heatsinking*: Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the LM656x0-Q1 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad (GND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce).

8.5.1.1 Thermal Design and Layout

For a DC/DC regulator to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM656x0-Q1 converter is available in a small 4.5mm × 4.5mm 26-pin Enhanced HotRod QFN package to cover a range of application requirements. The Section 6.4 table summarizes the thermal metrics of this package, with related detail provided by the *Semiconductor and IC Package Thermal Metrics* application note.

The 26-pin eQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. This exposed pad connects thermally to the substrate of the LM656x0-Q1 (ground). This connection allows a significant improvement in heatsinking, and the PCB must be designed with thermal lands, thermal vias, and one or more ground planes to complete the heat removal subsystem. The exposed pad of the LM656x0-Q1 solders to the ground-connected copper land on the PCB directly underneath the device package, reducing the IC thermal resistance to a very low value.

Preferably, use a four-layer board with 2oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3mm diameter connected from the thermal land (and from the area around the PGND pins) to the internal and solder-side ground planes are vital to promote heat transfer. In a multi-layer PCB design, a solid ground plane locates on the PCB layer below the power-stage components. Not only does this placement provide a plane for the power-stage currents to flow, but this placement also represents a thermally conductive path away from the heat-generating devices.

TI recommends providing adequate device heatsinking by using vias near the PGND and VIN pins to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible for the system ground plane on the top and bottom layers and avoid plane cuts and bottlenecks for the heat flow to optimize heat spreading.

ADVANCE INFORMATION

8.5.2 Layout Example

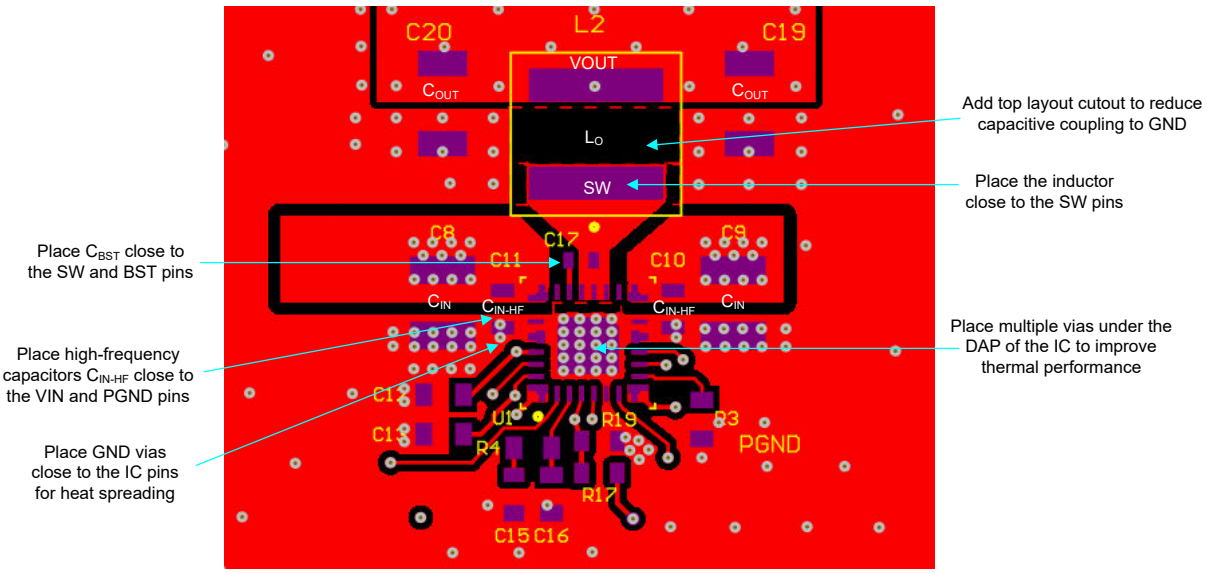


Figure 8-42. PCB Top Layer – High Density, Single-sided Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Development Support

For development support, see the following:

- LM656x0-Q1 Quickstart Calculator
- LM656x0-Q1 Simulation Models
- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- Browse TI's inverting buck-boost solutions
- EVM user's guides:
  - *LM65680-Q1 65V_{IN}, 5V_{OUT}, 8A Synchronous Buck DC/DC Regulator Evaluation Module*
  - *LM67680-Q1 60V_{IN}, –12V_{OUT}, –6A Inverting Buck-Boost DC/DC Regulator Evaluation Module*
- TI Designs:
  - *ADAS 8-Channel Sensor Fusion Hub Reference Design with Two 4-Gbps Quad Deserializers*
  - *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  - *25W Automotive Start-Stop Reference Design Operating at 2.2MHz*
  - *Synchronous Buck Converter for Automotive Cluster Reference Design*
  - *Automotive Synchronous Buck With 3.3V at 12.0A Reference Design*
  - *Automotive Synchronous Buck Reference Design*
  - *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- To view a related device of this product, see the LM65645-Q1 65V, 4.5A synchronous buck converter

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM656x0-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

9.2.1.1 Low-EMI Design Resources

- Texas Instruments, *Low EMI* landing page
- Texas Instruments, *Tackling the EMI challenge* company blog
- Texas Instruments, *An Engineer's Guide to Low EMI in DC/DC Regulators* e-book
- Texas Instruments, *Designing a low-EMI power supply* video series

ADVANCE INFORMATION

- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
- Texas Instruments, *Improve High-Current DC/DC Regulalor EMI for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* analog design journal

9.2.1.2 Thermal Design Resources

- Texas Instruments, *Improving Thermal Performance in High Ambient Temperature Environments With Thermally Enhanced Packaging* white paper
- Applications notes:
  - Texas Instruments, *Thermal Design by Insight, Not Hindsight*
  - Texas Instruments, *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *Using New Thermal Metrics*
- Texas Instruments, *PowerPAD™ Made Easy* application brief

9.2.1.3 Multiphase Design Resources

- Texas Instruments, *Multiphase Buck Design From Start to Finish* application note
- Texas Instruments, *Benefits of a Multiphase Buck Converter* analog design journal

9.2.1.4 PCB Layout Resources

- LM65680-Q1 EVM *Altium layout* source files (buck regulator)
- LM67680-Q1 EVM *Altium layout* source files (IBB regulator)
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note
- Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations* seminar

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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ADVANCE INFORMATION

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2025) to Revision B (May 2026)	Page
• Changed from ZEN to MINT branding and 70V transient support in the document title, *Features*, and *Description* sections	1
• Added SW to PGND transient abs max limits	8
• Added transient VIN recommended operating condition	8
• Added transient EN/UVLO recommended operating condition	8
• Updated the efficiency schematic for design 2	45
• Updated Figure 8-28 (efficiency plot of design 2)	50

Changes from Revision * (October 2024) to Revision A (December 2025)	Page
• Updated the document title, *Features*, and *Description* sections, including the schematic and efficiency plot.	1
• Updated the *Pin Configurations and Functions* to revise pin names: DRSS/MCOMM and CNFG/SYNCOUT	5
• Updated the *Applications and Implementations* section and added the *Design 2 – High Efficiency, 48V to 12V, 8A, 400kHz Synchronous Buck Regulator* section	29

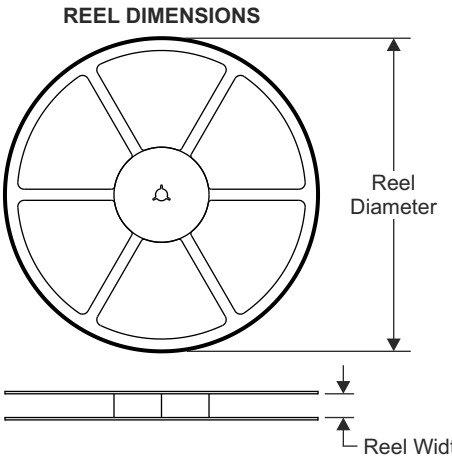
ADVANCE INFORMATION

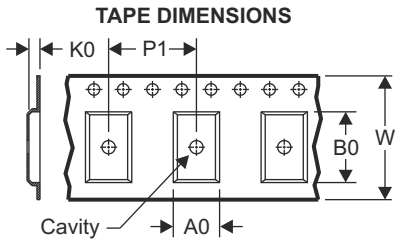
ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

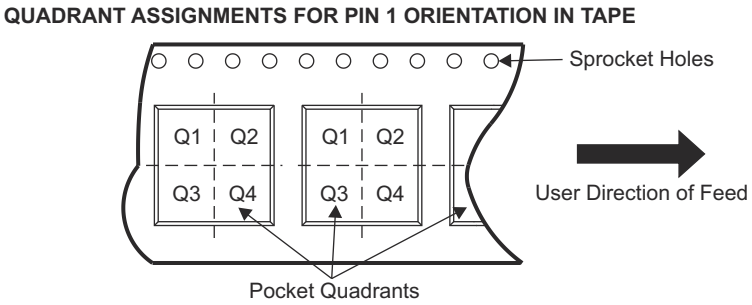
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



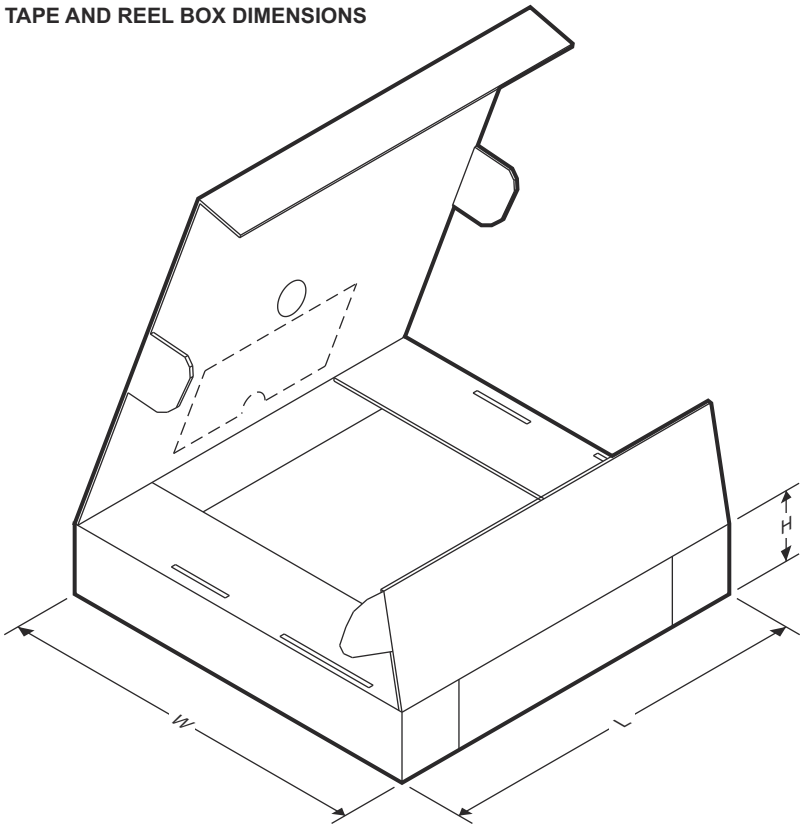


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM65680RZYRQ1	WQFN-FCRLF	RZY	26	2500	330	12.4	3.79	3.79	0.71	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM65680RZYRQ1	WQFN-FCRLF	RZY	26	2500	367	367	35

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PLM65680RZYRQ1	Active	Preproduction	WQFN-FCRLF (RZY) | 26	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PLM65680RZYRQ1.A	Active	Preproduction	WQFN-FCRLF (RZY) | 26	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM65680-Q1 :

- Catalog : LM65680

NOTE: Qualified Version Definitions:

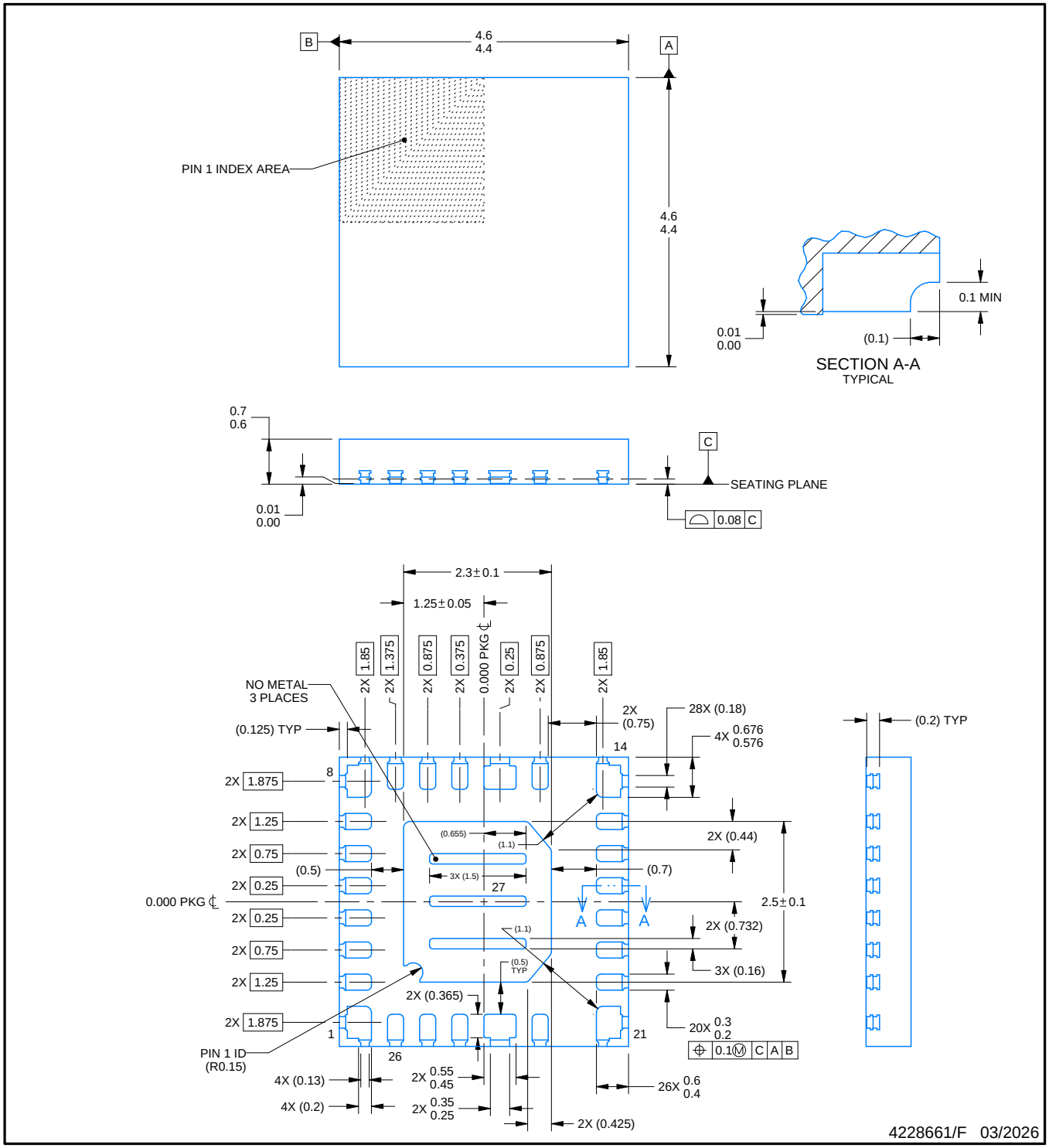
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

RZY0026A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

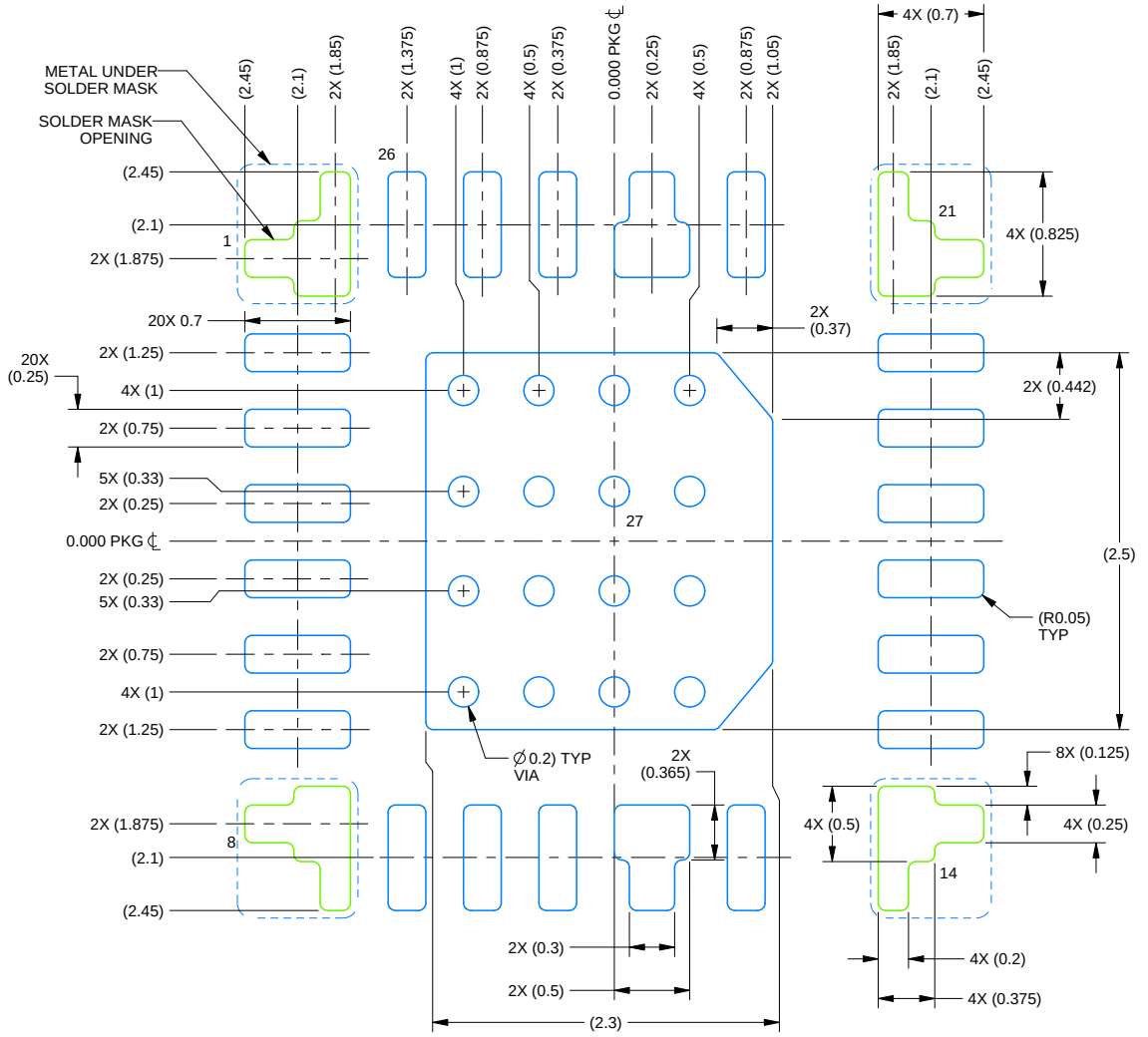
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RZY0026A

WQFN-FCRLF - 0.7 mm max height

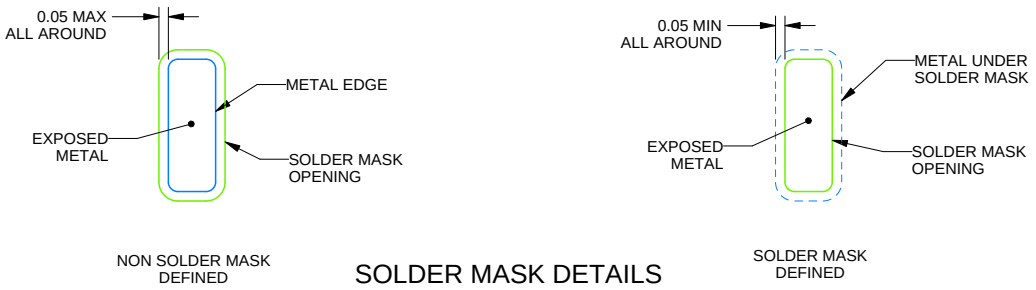
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



NON SOLDER MASK DEFINED

SOLDER MASK DETAILS

SOLDER MASK DEFINED

4228661/F 03/2026

NOTES: (continued)

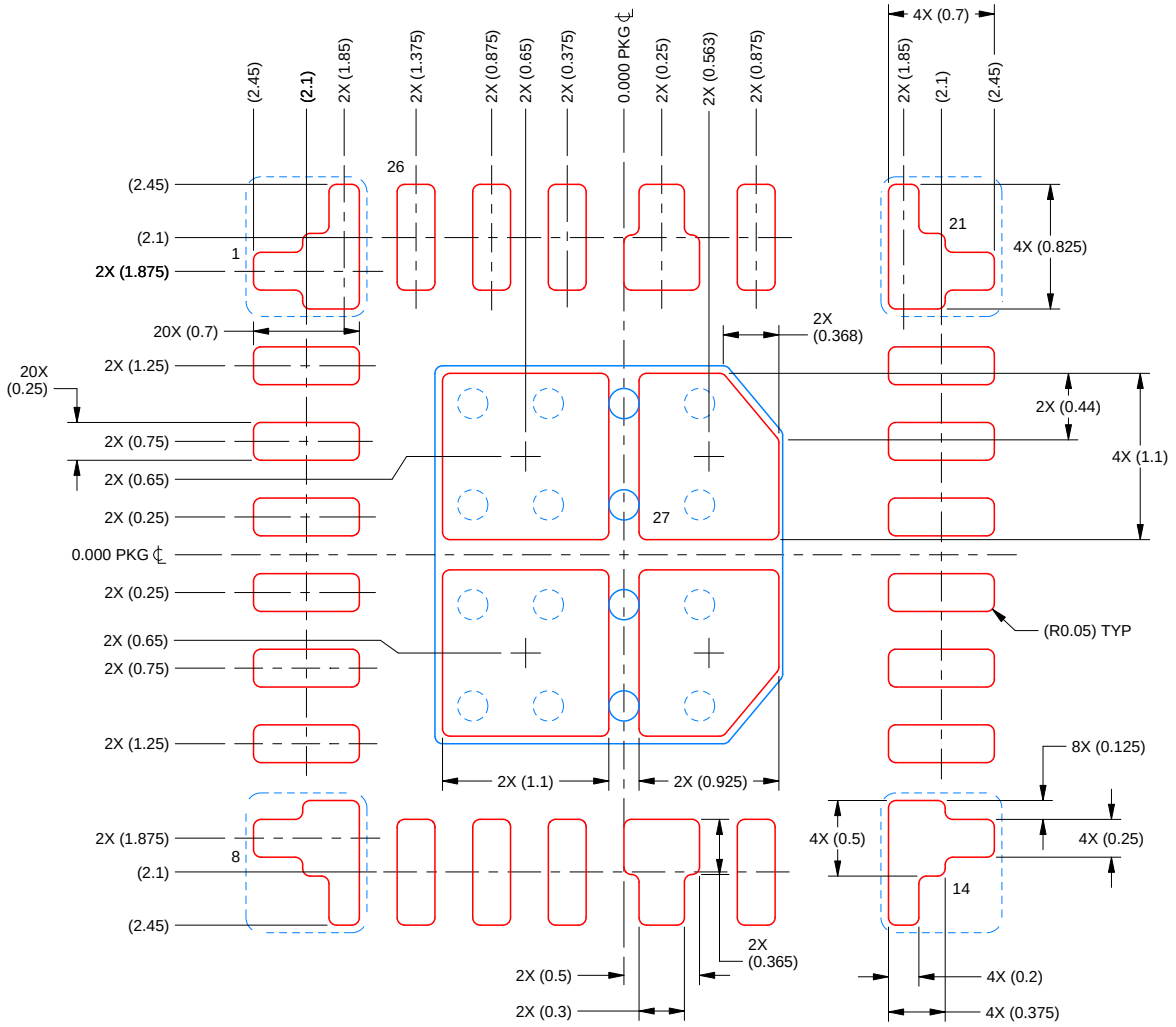
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RZY0026A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL

SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

PAD 27: 84%

4228661/F 03/2026

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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