

TPS37100-Q1, TPS37102-Q1 Automotive 105V, 5µA, Window, Overvoltage, or Undervoltage Supervisor with Integrated Buffer for Supply Voltage Measurements

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature T_A
- [Functional Safety-Compliant \(targeted for TPS37102-Q1\)](#)
 - Documentation to aid ISO 26262 system design
 - Systematic capability up to ASIL D targeted
 - Hardware capability up to ASIL D targeted
- [Functional Safety-Capable \(TPS37100-Q1\)](#)
 - Documentation available to aid functional safety system design
- Wide supply voltage range: 3V to 105V
- Low quiescent current: 5µA
- High threshold accuracy: 1.1% (maximum)
- Reverse polarity protection on SENSE: -95V
- Fast UV/OV monitor for 24V/48V systems: 5µs
- Integrated buffer (AOUT) for supply voltage measurement with enable pin
- Fixed and programmable release time delay
- Fixed and programmable sense time delay
- Open-drain, active-low output: OUT A and OUT B
- BIST and Latch available for TPS37102-Q1

2 Applications

- [Battery management unit](#)
- [DC/DC converter system](#)
- [2-wheeler and 3-wheeler traction drive](#)
- [Low-voltage battery system](#)
- [Traction inverter](#)

3 Description

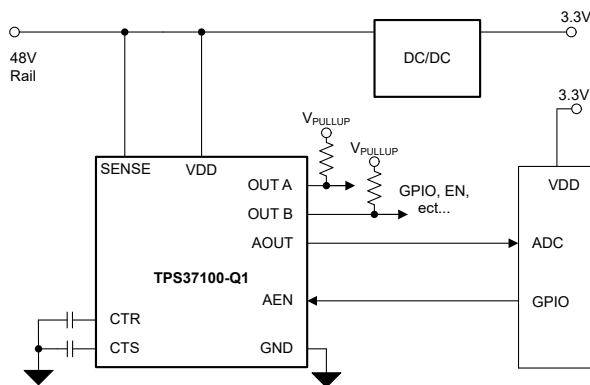
The TPS37100-Q1 and TPS37102-Q1 are 105V input voltage supervisors with low quiescent current (5µA), fast detection time, and an integrated buffer for supply voltage measurements. This family of devices can connect directly to a 24V / 48V / 72V battery or voltage rail for continuous monitoring of over (OV) or under (UV) voltage conditions. Wide hysteresis voltage options are available to ignore false output deassertions that are caused by battery voltage transients.

The TPS37100-Q1 and TPS37102-Q1 include two outputs (OUT A and OUT B) that are used as separate OV and UV fault monitors enabling system to take different action based on the fault that occurs. Additionally, the AOUT pin provides a scaled down SENSE pin voltage output and is intended to be sampled by ADC for supply voltage measurements. The user can select the scaling factor desired based on the orderable part selected. The TPS37102-Q1 comes with BIST which is implemented at start-up to verify device health as well as an optional latching feature on OUT A to help the system bring into a safe state when critical faults occurs.

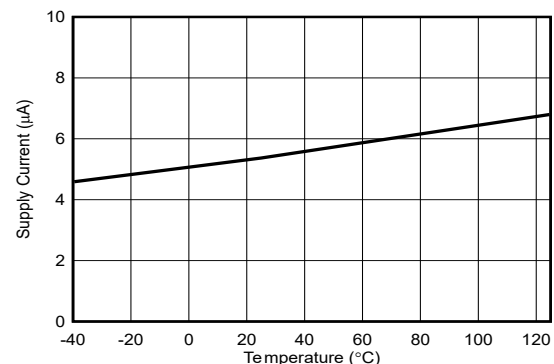
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽³⁾
TPS37100-Q1	SOT-23 (14) (DYY)	4.1mm × 1.9mm
TPS37102-Q1 ⁽²⁾	SOT-23 (14) (DYY)	4.1mm × 1.9mm

- (1) For package details, see the mechanical drawing addendum at the end of the datasheet.
- (2) PRODUCT PREVIEW
- (3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Typical I_{DD} vs Temperature (VDD = 48V)



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4 Device Comparison

Figure 4-1 and Figure 4-2 show the device naming nomenclature of the TPS37100-Q1 and TPS37102-Q1. For a detailed breakdown of device part number by features, thresholds, and analog out scale see Table 4-1 for more details. Contact TI sales representatives or on TI's E2E™ forum for detail and availability of other options.

Table 4-1. Available Devices

ORDERABLE PART NAME	Feature	OV / UV SETTINGS ⁽¹⁾⁽²⁾	OUT A / OUT B SETTINGS	TIME DELAY	ANALOG OUT SCALE
TPS37100Z91DDYYRQ1	Analog Out	V _{ITN} : 800mV (ADJ) HYST: 1%	OUT A: V _{ITN} OUT B: V _{ITN}	CTS: Enabled CTR: Enabled	0.75
TPS37100W41DDYYRQ1	Analog Out	V _{ITP} : 832mV (ADJ) V _{ITN} : 768mV (ADJ) HYST: 1%	OUT A: V _{ITN} & V _{ITP} OUT B: V _{ITN} & V _{ITP}	CTS: Enabled CTR: Enabled	0.75
PPS37100D91KDYYRQ1 ⁽³⁾	Analog Out	V _{ITN} : 24V HYST: 1%	OUT A: V _{ITN} OUT B: V _{ITN}	CTS: Enabled CTR: Enabled	40

- (1) For listed percentage denotes hysteresis tolerance, see Section 6.5 for more information
 (2) V_{ITN} or V_{ITP} threshold with ADJ denotes an adjustable voltage threshold set by an external resistor divider, see Section 7.3.2.1 for more information on how to set the threshold.
 (3) Product preview. Please check with a Texas Instruments representative for availability

TPS3710 X X X X X DYY R Q1

FEATURES

0: AOUT
2: AOUT, BIST

ADJUSTABLE THRESHOLDS

Z9: UV Only
UV: 800mV Adjustable
OV: Not Included

9Z: OV Only
UV: Not Included
OV: 800mV Adjustable

W3: 3% Window
UV: 776mV
OV: 824mV

W4: 4% Window
UV: 768mV
OV: 832mV

W5: 5% Window
UV: 760mV
OV: 840mV

W6: 6% Window
UV: 752mV
OV: 848mV

W7: 7% Window
UV: 744mV
OV: 856mV

W8: 8% Window
UV: 736mV
OV: 864mV

W9: 9% Window
UV: 728mV
OV: 872mV

WA: 10% Window
UV: 720mV
OV: 880mV

WF: 15% Window
UV: 680mV
OV: 920mV

HYSTERESIS

1: 1%
5: 5%
0: 10%

**OUT A / OUT B Settings + TIME DELAY
+ AOUT SCALE ***

A:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Standard
B:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Standard
C:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 40	OUT A/B: Standard
D:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Combined
E:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Combined
F:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Combined
G:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Combined
H:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
I:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Standard
J:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Standard
K:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 40	OUT A/B: Standard
L:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
	Latch: Enabled	
M:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
	Latch: Enabled	

PACKAGE

DYY: SOT23-14

REEL

R: Large reel

Rating

Q1: Automotive

* OV only and UV only variants OUT A and OUT B are combined.

Figure 4-1. Device Naming Convention (Adjustable Threshold Variant)

TPS3710 X X X X X DYY R Q1

FEATURES
0: AOUT
2: AOUT, BIST

UNDERVOLTAGE THRESHOLD

A: 18V
B: 20V
C: 22V
D: 24V
E: 26V
F: 28V
G: 30V
H: 32V
I: 34V
J: 36V
K: 38V
L: 40V
M: 42V
N: 44V
O: 46V
P: 48V
Q: 50V
R: 52V
S: 54V
T: 56V
U: 58V
V: 60V
X: 62V
Y: 64V
0: 66V
1: 68V
2: 70V
3: 72V
4: 74V
5: 76V
6: 78V
7: 80V
8: 82V
9: UV Not Included

OVERVOLTAGE THRESHOLD

A: 40V
B: 42V
C: 44V
D: 46V
E: 48V
F: 50V
G: 52V
H: 54V
I: 56V
J: 58V
K: 60V
L: 62V
M: 64V
N: 66V
O: 68V
P: 70V
Q: 72V
R: 74V
S: 76V
T: 78V
U: 80V
V: 82V
X: 84V
Y: 86V
0: 88V
1: 90V
2: 92V
3: 94V
4: 96V
5: 98V
6: 100V
7: 102V
8: 104V
9: OV Not Included

HYSTERESIS

1: 1%
5: 5%
0: 10%

OUT A / OUT B Settings + TIME DELAY + AOUT SCALE *

A:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Standard
B:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Standard
C:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 40	OUT A/B: Standard
D:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Combined
E:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Combined
F:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Combined
G:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Combined
H:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
I:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 24	OUT A/B: Standard
J:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 30	OUT A/B: Standard
K:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 40	OUT A/B: Standard
L:	CTS: Disabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
	Latch: Enabled	
M:	CTS: Enabled	CTR: Enabled
	AOUT Scale: 0.75	OUT A/B: Standard
	Latch: Enabled	

PACKAGE

DYY: SOT23-14

REEL

R: Large reel

Rating

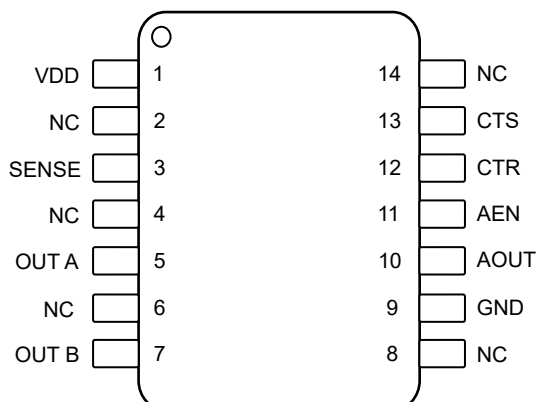
Q1: Automotive

* OV only and UV only variants OUT A and OUT B are combined.

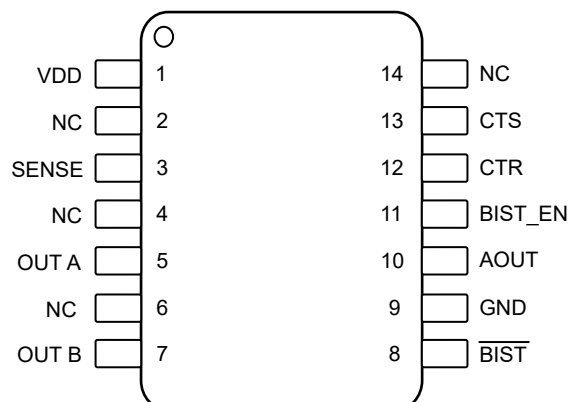
Figure 4-2. Device Naming Convention (Fixed Threshold Variant)

- Adjustable OV or UV only options threshold is 800mV.
- Adjustable Window option thresholds only available with 1% hysteresis.
- For OV only and UV only OUT A/B combined is default. Window can be either OUT A/B combined or standard. Refer to [Section 7.3.3](#).

5 Pin Configuration and Functions



**Figure 5-1. DYY Package,
14-Pin SOT-23, TPS37100-Q1 (Top View)**



**Figure 5-2. DYY Package,
14-Pin SOT-23, TPS37102-Q1 (Top View) PRODUCT
PREVIEW**

Table 5-1. Pin Functions

PIN	TPS37100-Q1	TPS37102-Q1	TYPE	DESCRIPTION
NAME	NO.	NO.	(1)	
VDD	1	1	I	Input Supply Voltage: Supply voltage pin. For noisy systems, bypass with a 0.1µF capacitor to GND.
SENSE	3	3	I	Sense Voltage: Connect this pin to the supply rail that must be monitored. See Section 7.3.2 for more details. Sensing Topology: Overvoltage (OV) or Undervoltage (UV) or Window (OV + UV)
OUT A	5	5	O	Output A: OUT A asserts varies on configuration as denoted by in Section 4 . See Section 7.3.2 for more details on overvoltage and undervoltage behavior. The active low open-drain output requires an external pullup resistor. See Section 7.3.3 for more details on open-drain output. Output topology: Open-Drain Active-Low
OUT B	7	7	O	Output B: OUT B asserts varies on configuration as denoted by in Section 4 . See Section 7.3.2 for more details on overvoltage and undervoltage behavior. The active low open-drain output requires an external pullup resistor. See Section 7.3.3 for more details on open-drain output. Output topology: Open-Drain Active-Low
BIST	-	8	O	Built-In Self-Test: BIST asserts when a logic high input occurs on the BIST_EN pin, this initiates the internal BIST testing. $\overline{\text{BIST}}$ recovers after t_{BIST} to signify BIST completed successfully. $\overline{\text{BIST}}$ remains asserted for a time period longer than t_{BIST} if there is a failure during BIST. BIST active-low open-drain output requires an external pullup resistor. See Section 7.3.7 for more details.
GND	9	9	-	Ground. GND pin must be electrically connected to the board ground.
AOUT	10	10	O	Analog Out: Output of AOUT is a scaled voltage from the SENSE pin. TPS37100-Q1 can enable or disable Analog Out with AEN Pin. TPS37102-Q1 cannot enable or disable Analog Out and it is in default configuration. A 0.1µF is required at AOUT for output stability. See Section 7.3.6 for more details.
AEN	11	-	I	Analog Out Enable: Enables or disables the AOUT pin. A logic high input enables the AOUT. A logic low disables AOUT. AEN pin has an internal 100kΩ pulldown resistor.

Table 5-1. Pin Functions (continued)

PIN	TPS37100-Q1	TPS37102-Q1	TYPE (1)	DESCRIPTION
NAME	NO.	NO.		
BIST_EN	-	11	I	Built-in Self-test Enable: A rising edge input must occur on the BIST_EN to initiate BIST. For variants with latch enabled in the configuration as denoted by in Section 4 , BIST_EN enables or disables a latch on OUT A. See Section 7.3.7 for more details.
CTR	12	12	-	Release Time Delay: User-programmable release time delay for CTR enabled outputs OUT A and OUT B. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 7.3.4 for more details.
CTS	13	13	-	Sense Time Delay: User-programmable sense time delay for CTS enabled outputs OUT A and OUT B. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay when CTS is enabled. See Section 7.3.5 for more details.
NC	2, 4, 6, 8, 14	2, 4, 6, 14	-	NC stands for "No Connect." The pins are to be left floating.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted ⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{DD} , $V_{SENSE(ADJ)}$, $V_{OUT A}$	−0.3	105	V
Voltage	$V_{SENSE(Fixed)}$	−95	105	V
Voltage	V_{AEN} , V_{CTS} , V_{CTR} , $V_{OUT B}$, V_{AOUT} , V_{BIST} , V_{BIST_EN}	−0.3	6	V
Current	$I_{OUT A}$, $I_{OUT B}$, I_{BIST}		10	mA
Output Short-current ⁽²⁾	I_{AOUT}	Continuous		μA
Temperature	Operating junction temperature, T_J	−40	150	°C
Temperature	Operating ambient temperature, T_A	−40	125	°C
Temperature	Storage, T_{stg}	−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	3		105	V
Voltage	V_{SENSE} , $V_{OUT A}$	0		105	V
Voltage	V_{AEN} , $V_{OUT B}$, V_{AOUT} , V_{BIST} , V_{BIST_EN}	0		5.5	V
Current	$I_{OUT A}$, $I_{OUT B}$, I_{BIST}	0		±5	mA
Current	I_{AOUT}	0		±20	μA
T_J	Junction temperature (free air temperature)	−40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3710x-Q1	UNIT
		DYY	
		14-PIN	
R _{θJA}	Junction-to-ambient thermal resistance	120.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	50.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	49.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

6.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output OUT A and OUT B pull-up resistor with $R_{PU} = 10k\Omega$ and $V_{PU} = 5.5V$. The operating free-air temperature range $T_A = -40^\circ C$ to $125^\circ C$, unless otherwise noted. Typical values are at $T_A = 25^\circ C$ and $V_{DD} = 16V$. V_{IT} refers to V_{ITN} or V_{ITP} . AOCT $C_{Load} = 100nF$ and AOCT $V_{OUT} = 2.5V$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V_{DD}	Supply Voltage		3		105	V
UVLO (1)	Undervoltage Lockout	V_{DD} Falling below $V_{DD(MIN)}$			2.6	V
UVLO(HYS) (1)	Undervoltage Lockout Hysteresis	V_{DD} Rising above $V_{DD(MIN)}$		400		mV
V_{POR}	Power on Reset Voltage (2) OUT_A	$V_{OL(MAX)} = 300mV$ $I_{OUT A(Sink)} = 15\mu A$			1.4	V
V_{POR}	Power on Reset Voltage (2) OUT_B	$V_{OL(MAX)} = 300mV$ $I_{OUT B(Sink)} = 15\mu A$			1.4	V
I_{DD}	Supply current into VDD pin	$V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$ Analog out = disabled		5	13	μA
I_{DD}	Supply current into VDD pin	$V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$ Analog out = enabled $I_{AOCT} = 0\mu A$		9	18	μA
SENSE (Input)						
I_{SENSE}	Input current	$V_{IT} = 800mV$			300	nA
I_{SENSE}	Input current	$V_{IT} = 18V$ to $105V$		1.5	8	μA
V_{ITN}	Input Threshold Negative (V_{ITN})	$V_{ITN} = 18V$ to $105V$	-1.1		1.1	%
		$V_{ITN} = 800mV$	-0.8		0.8	%
V_{ITP}	Input Threshold Positive (V_{ITP})	$V_{ITP} = 18V$ to $105V$	-1.1		1.1	%
		$V_{ITP} = 800mV$	-0.8		0.8	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 18V$ to $105V$ V_{HYS} Range = 1%		1	1.5	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 800mV$ V_{HYS} Range = 1%		1	1.8	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 18V$ to $105V$ V_{HYS} Range = 5%	4.5	5	6	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 800mV$ V_{HYS} Range = 5%	4.5	5	6	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 18V$ to $105V$ V_{HYS} Range = 10%	9	10	11	%
V_{HYS}	Hysteresis Accuracy (3)	$V_{IT} = 800mV$ V_{HYS} Range = 10%	9	10	11	%
OUT A and OUT B (Output)						
$I_{lkg(OUT A)}$	Open-Drain leakage	$V_{OUT A} = 5.5V$ $V_{ITN} < V_{SENSE} < V_{ITP}$			900	nA
		$V_{OUT A} = 105V$ $V_{ITN} < V_{SENSE} < V_{ITP}$			900	nA
$V_{OL(OUT A)}$	Low level output voltage	$3V \leq V_{DD} \leq 105V$ $I_{OUT A} = 2.7mA$			350	mV
$I_{lkg(OUT B)}$	Open-Drain leakage	$V_{OUT B} = 5.5V$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$V_{OL(OUT B)}$	Low level output voltage	$3V \leq V_{DD} \leq 105V$ $I_{OUT B} = 5mA$			300	mV
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)		2960	3700	4440	K Ω
R_{CTS}	Internal resistance (CTS)		2960	3700	4440	K Ω

6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output OUT A and OUT B pull-up resistor with $R_{PU} = 10k\Omega$ and $V_{PU} = 5.5V$. The operating free-air temperature range $T_A = -40^\circ C$ to $125^\circ C$, unless otherwise noted. Typical values are at $T_A = 25^\circ C$ and $V_{DD} = 16V$. V_{IT} refers to V_{ITN} or V_{ITP} . AOOUT $C_{Load} = 100nF$ and AOOUT $V_{OUT} = 2.5V$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Out						
I_{OUT}	Output buffer current, sink and source		-20		+20	μA
I_{SC}	Short circuit current.			450		μA
Slew Rate	Slew Rate for current			50		mA/ms
V_{IL_EN}					500	mV
V_{IH_EN}			1300			mV
$V_{AOOUT(Min)}$	AOOUT Range		0.35			V
$V_{AOOUT(Max)}$	AOOUT Range	$V_{DD} - V_{DO} < 5V$		$V_{DD}-V_{DO}$		V
$V_{AOOUT(Max)}$	AOOUT Range	$V_{DD} - V_{DO} \geq 5V$		5		V
V_{DO}	Voltage dropout	$I_{AOOUT} = 0\mu A$			0.41	V
V_{DO}	Voltage dropout	$I_{AOOUT} = 20\mu A$			0.41	V
	Accuracy 25°C	$I_{AOOUT} = 0\mu A$, $T_A = 25^\circ C$ Analog Out Scale = 0.75	-0.3		0.3	%
	Accuracy over Temp	$I_{AOOUT} = 0\mu A$ $3V > V_{AOOUT} \geq 0.5V$	-1		1	%
	Accuracy over Temp	$I_{AOOUT} = 0\mu A$ $0.5V \geq V_{AOOUT}$	-2		2	%
	Line Regulation	$V_{DD} = 3V$ to $105V$	-0.1		0.1	%
	Load Regulation (source)	$I_{AOOUT} = 0\mu A$ to $20\mu A$			0.03	%/ μA
	Load Regulation (sink)	$I_{AOOUT} = 0\mu A$ to $-20\mu A$			0.03	%/ μA
C_{OUT}	Output buffer capacitor for stability	ESR = $5m\Omega$ to $20m\Omega$	0.07	0.1	0.13	μF
	Response time	90% of SENSE input to 0.7% accuracy of V_{AOOUT}		2		ms
	Turn-on (EN) Time	$I_{AOOUT} = 0\mu A$,		1.5		ms
$I_{lkG(BIST_OD)}$	Open-Drain leakage	$V_{BIST} = 5.5V$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{BIST_OL}	Low level output voltage	$3V \leq V_{DD} \leq 105V$ $I_{BIST(Sink)} = 5mA$			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV

- (1) When V_{DD} voltage falls below UVLO, OUT A and OUT B are asserted until V_{POR} . V_{DD} slew rate $\leq 1V/\mu s$
- (2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR} , the output cannot be determined. V_{DD} slew rate $\leq 1V/\mu s$
- (3) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.

6.6 Switching Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output OUT A and OUT B pull-up resistor with $R_{PU} = 10k\Omega$ and $V_{PU} = 5.5V$. The operating free-air temperature range $T_A = -40^\circ C$ to $125^\circ C$, unless otherwise noted. Typical values are at $T_A = 25^\circ C$ and $V_{DD} = 16V$. V_{IT} refers to V_{ITN} or V_{ITP} . AOUT $C_{Load} = 100nF$ and AOUT $V_{OUT} = 2.5V$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common switching parameters						
$t_{CTR(OUT A)}$	Release time delay (CTR) ⁽¹⁾	$V_{IT} = 18V$ to $100V$, $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		500		μs
$t_{CTR(OUT A)}$	Release time delay (CTR) ⁽¹⁾	$V_{IT} = 800mV$, $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		500		μs
$t_{CTR(OUT B)}$	Release time delay (CTR) ⁽¹⁾	$V_{IT} = 18V$ to $100V$, $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		500		μs
$t_{CTR(OUT B)}$	Release time delay (CTR) ⁽¹⁾	$V_{IT} = 800mV$, $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		500		μs
t_{CTS}	Sense time delay ⁽²⁾⁽⁴⁾	$V_{ITP} = 800mV$, CTS = Disabled 20% Overdrive from V_{IT}			3	μs
		$V_{ITN} = 800mV$, CTS = Disabled 20% Overdrive from V_{IT}			5	μs
		$V_{ITP} = 18V$ to $100V$, CTS = Disabled 20% Overdrive from V_{IT}		6	10	μs
		$V_{ITN} = 18V$ to $100V$, CTS = Disabled 20% Overdrive from V_{IT}		6	10	μs
		$V_{IT} = 800mV$, $C_{CTS} = \text{Open}$ ⁽⁵⁾ 20% Overdrive from V_{IT}		75	100	μs
		$V_{IT} = 18V$ to $100V$, $C_{CTS} = \text{Open}$ ⁽⁵⁾ 20% Overdrive from V_{IT}		75	120	μs
t_{SD}	Startup Delay ⁽³⁾	$C_{CTR} = \text{Open}$		1		ms
t_{BIST}	Test time for BIST				2.5	ms

- (1) **CTR Release detect time delay:**
Overvoltage active-LOW output is measure from $V_{ITP-HYS}$ to V_{OH}
Undervoltage active-LOW output is measure from $V_{ITN+HYS}$ to V_{OH}
- (2) **CTS Sense detect time delay:**
Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
- (3) During the power-on sequence, V_{DD} must be at or above $V_{DD(MIN)}$ for at least t_{SD} before the output is in the correct state.
- (4) This parameter is established by design and/or characterization and is not tested in production.
- (5) $C_{CTS} = \text{Open}$ assumes there is less than 20pF of parasitic capacitance on the pin.

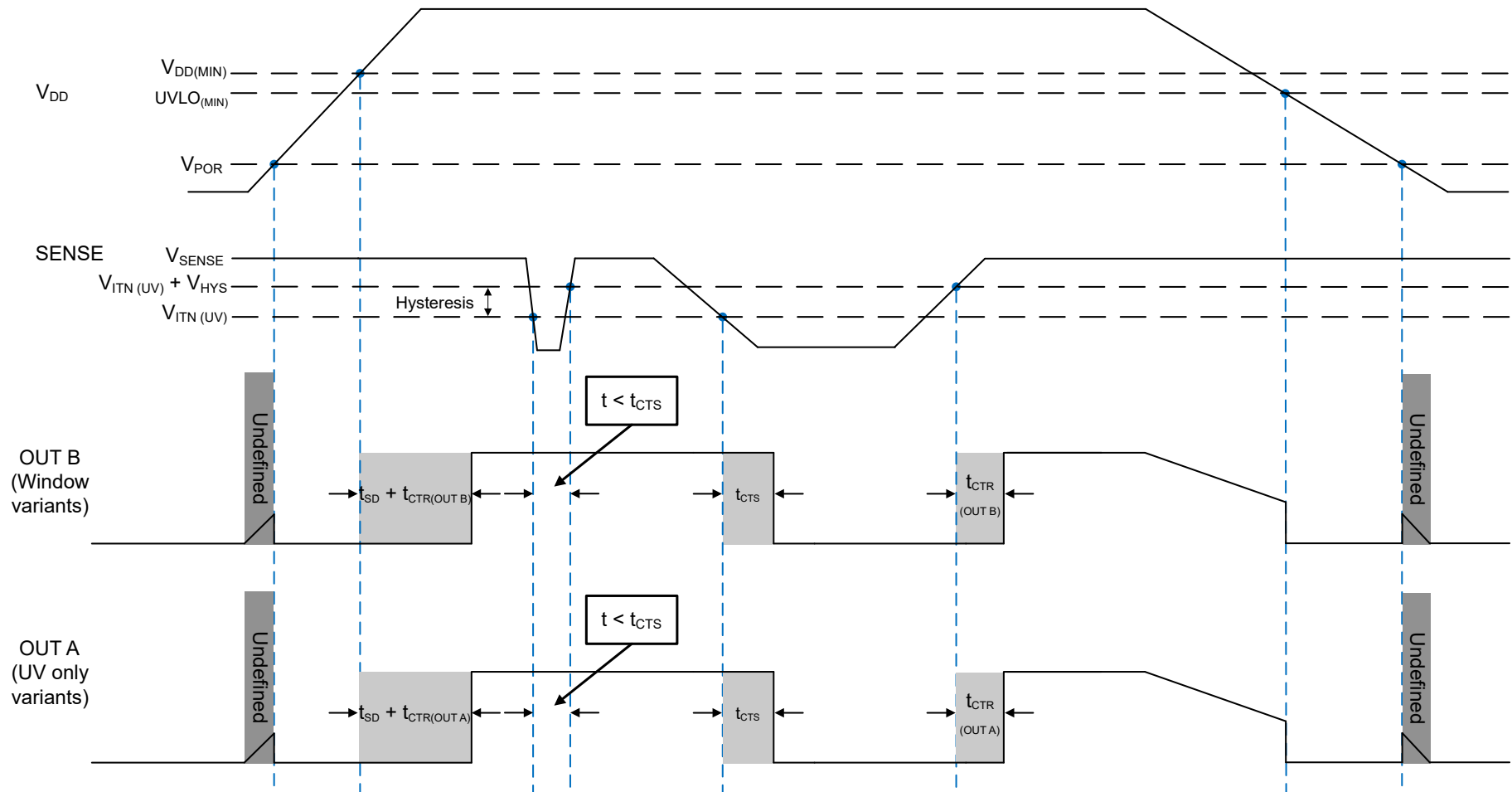
6.7 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, CTR = CTS = open, output OUT A and OUT B pull-up resistor with $R_{PU} = 10k\Omega$ and $V_{PU} = 5.5V$. The operating free-air temperature range $T_A = -40^\circ C$ to $125^\circ C$, unless otherwise noted. Typical values are at $T_A = 25^\circ C$ and $V_{DD} = 16V$. V_{IT} refers to V_{ITN} or V_{ITP} . AOUT $C_{Load} = 100nF$ and AOUT $V_{OUT} = 2.5V$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
t_{GL_SNS}	Sense Glitch ⁽¹⁾	10% overdrive, Fixed threshold, CTS = Disabled		1.2		μs
t_{GL_SNS}	Sense Glitch ⁽¹⁾	10% overdrive, Fixed threshold, CTS = Enabled, CTS = 20pF		65		μs

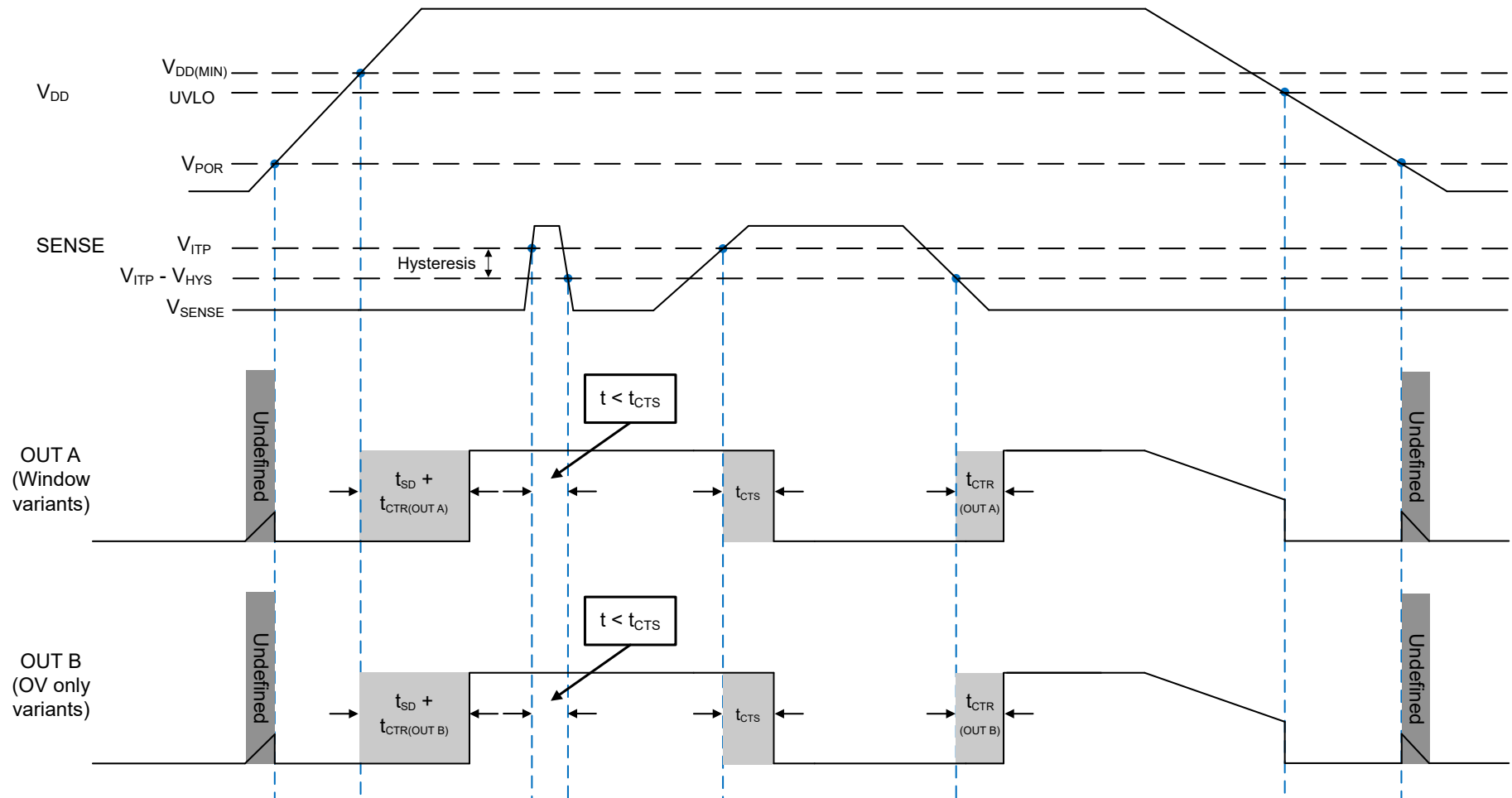
- (1) Overdrive % = $[(V_{SENSE}/V_{IT}) - 1] \times 100\%$ (1)
 V_{IT} refers to either V_{ITN} or V_{ITP}

6.8 Timing Diagrams



- A. OUT A and OUT B pins are connected via external pull-up resistors to pullup voltages.
 B. Be advised that [Figure 6-1](#) shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTR}) time.

Figure 6-1. SENSE Undervoltage (UV) Timing Diagram



- A. OUT A and OUT B pins are connected via external pull-up resistors to pullup voltages.
 B. Be advised that [Figure 6-2](#) shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.

Figure 6-2. SENSE Overvoltage (OV) Timing Diagram

6.9 Typical Characteristics

Typical characteristics show the typical performance of the TPS3710x-Q1 devices. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 10\text{k}\Omega$, $C_{Load} = 10\text{pF}$, AOUT $C_{Load} = 100\text{nF}$ and AOUT $V_{OUT} = 2.5\text{V}$, unless otherwise noted. V_{IT} refers to V_{ITN} or V_{ITP} .

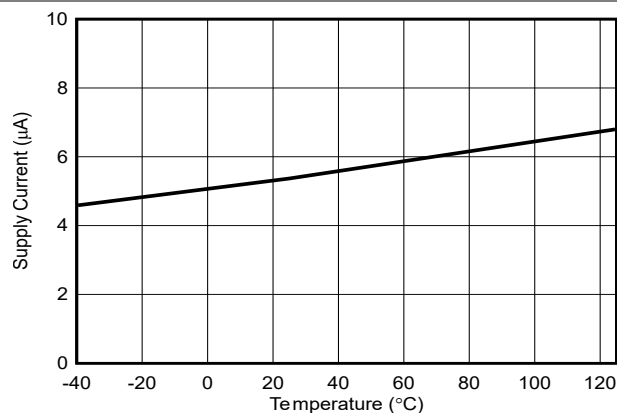


Figure 6-3. Typical I_{DD} vs Temperature ($V_{DD} = 48\text{V}$) with AOUT Disabled

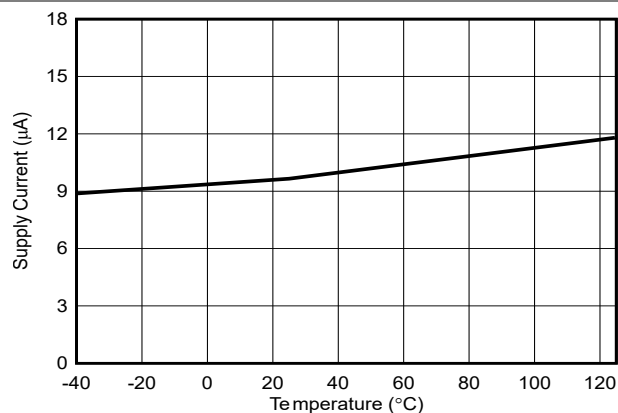


Figure 6-4. Typical I_{DD} vs Temperature ($V_{DD} = 48\text{V}$) with AOUT Enabled

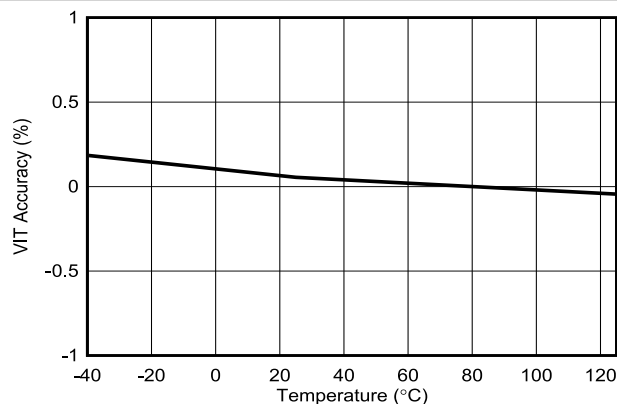


Figure 6-5. Typical Adjustable V_{IT} Accuracy vs Temperature

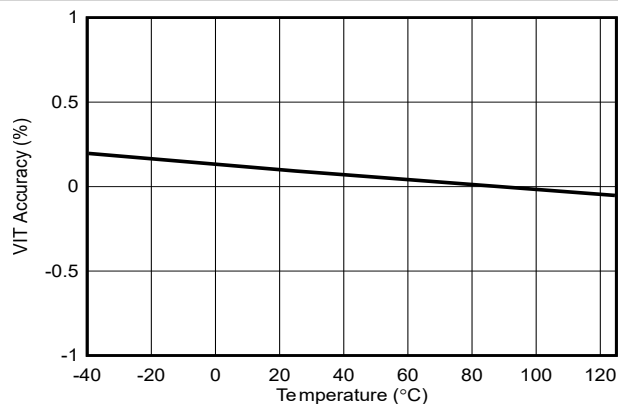


Figure 6-6. Typical Fixed V_{IT} Accuracy vs Temperature

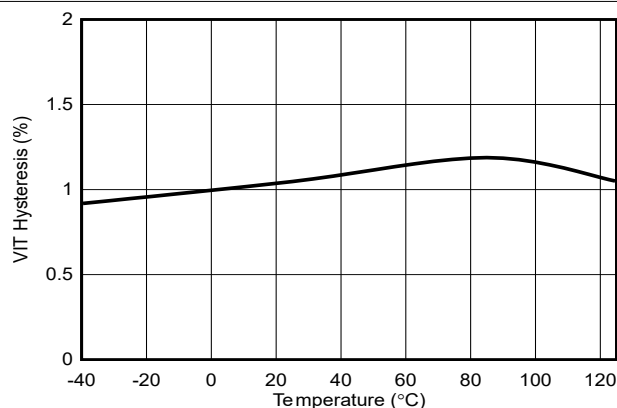


Figure 6-7. Typical V_{IT} 1% Hysteresis vs Temperature

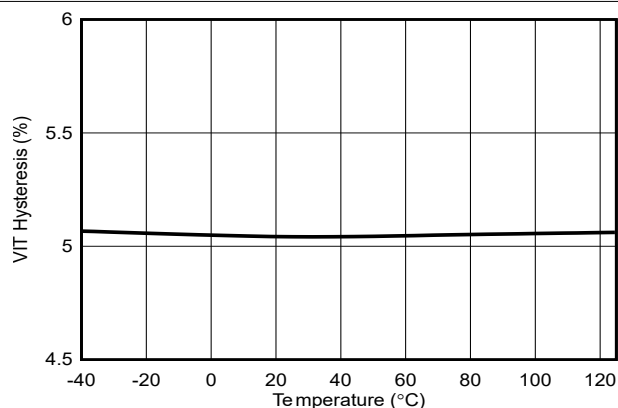


Figure 6-8. Typical V_{IT} 5% Hysteresis vs Temperature

7 Detailed Description

7.1 Overview

The TPS3710x-Q1 is a family of high voltage and low quiescent current voltage supervisors with overvoltage and undervoltage threshold voltage, delay timings, Built-In Self-Test (TPS37102-Q1 only), and AOUT. The TPS3710x-Q1 over and undervoltage thresholds are device specific and are offered in either adjustable thresholds or fixed thresholds. The adjustable threshold option uses an external resistor ladder to make a voltage divider on SENSE pin which uses the internal 800mV threshold to trigger overvoltage or undervoltage faults. The benefit of using an adjustable option with external resistors is the faster reaction speed compared to a fixed internal threshold variant. The TPS3710x-Q1 fixed threshold option utilizes an integrated voltage divider to eliminate the need for external resistors and provides a lower total current consumption.

VDD, SENSE, and OUT A pins can support 105V continuous operation. SENSE has -95V reverse polarity protection for fixed threshold options only. VDD, SENSE, OUT A, and OUT B pins are voltage level independent of each other. Fixed and programmable sense and release time delay options are available to avoid false assertion and false deassertions.

The AOUT pin provides a scaled output voltage from the SENSE for both fixed and adjustable options. The AOUT pin is intended to be sampled with an ADC for supply voltage measurements. The AOUT and supervisor combination simplifies high voltage rail monitoring for low voltage ADCs.

7.2 Functional Block Diagram

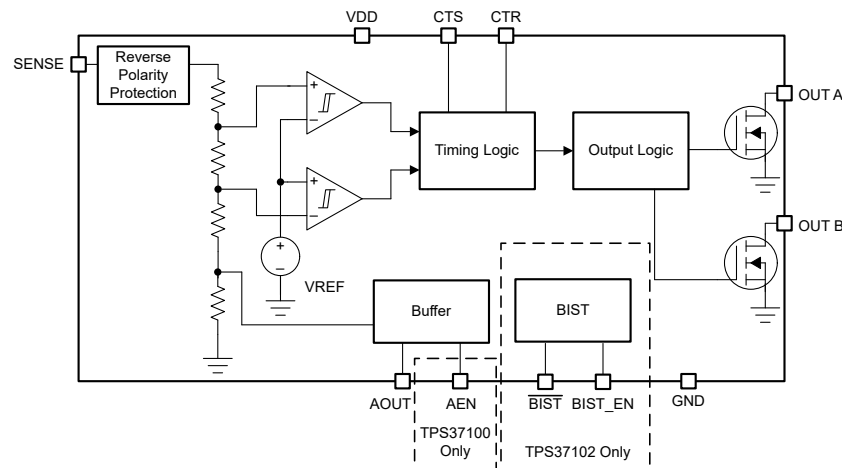


Figure 7-1. Fixed Threshold Functional Block Diagram

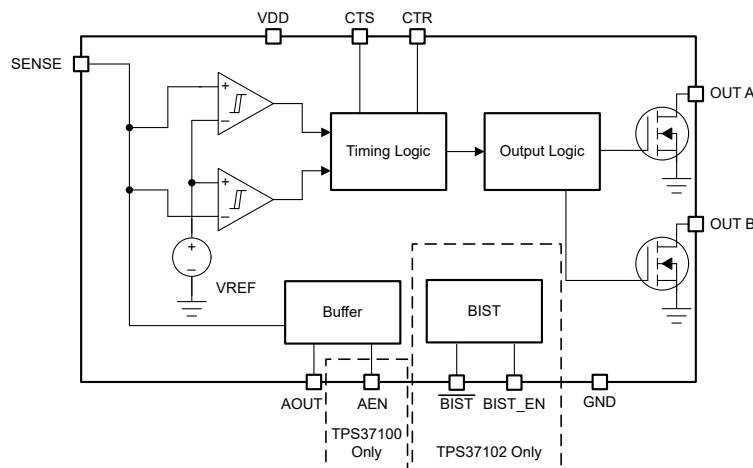


Figure 7-2. Adjustable Threshold Functional Block Diagram

7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 3V to 105V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1μF capacitor between the VDD and GND.

VDD must be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} , $V_{OUT A}$, and $V_{OUT B}$, meaning that VDD can be higher or lower than the other pins.

7.3.1.1 Undervoltage Lockout ($V_{POR} < V_{DD} < UVLO$)

When the voltage on V_{DD} is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the OUT A, OUT B, and BIST pins are asserted, regardless of the voltage at SENSE pin.

7.3.1.2 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than the power-on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

7.3.2 SENSE

The SENSE pin connects to the supply rail that is to be monitored. The sense pin on each device is configured to monitor either overvoltage (OV), undervoltage (UV), or window (OV and UV) conditions. TPS3710x-Q1 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, designers can use either t_{CTS} or place a 10nF to 100nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

7.3.2.1 Adjustable Voltage Thresholds

Section 7.3.2.1 shows an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. Adjustable voltage threshold variants bypass the internal resistor ladder.

For example, consider a 48V rail, V_{MON} , being monitored for undervoltage (UV) only using of the TPS37100Z91DDYYRQ1 variant. The monitored UV threshold, denoted as V_{MON-} , is the desired voltage where the device asserts the reset. For this example $V_{MON-} = 40V$. To assert an undervoltage reset the voltage at the sense pin, V_{SENSE} , must be equal or lower to the input threshold positive, V_{ITN-} . For this example variant $V_{SENSE} = V_{ITN-} = 0.8V$. Using R_1 and R_2 the correlation between V_{MON-} and V_{SENSE} can be seen in Equation 2. Assuming $R_2 = 2k\Omega$, and R_1 can be calculated as $R_1 = 98k\Omega$.

$$V_{SENSE} = V_{MON-} \times [R_2 \div (R_1 + R_2)] \quad (2)$$

The TPS37100Z91DDYYRQ1 comes with variant specific 1% voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} must go above $V_{ITN} + V_{HYS}$. For this example variant a 1% voltage threshold hysteresis is selected. Therefore, V_{MON} equals 40.4V when the reset signal becomes deasserted.

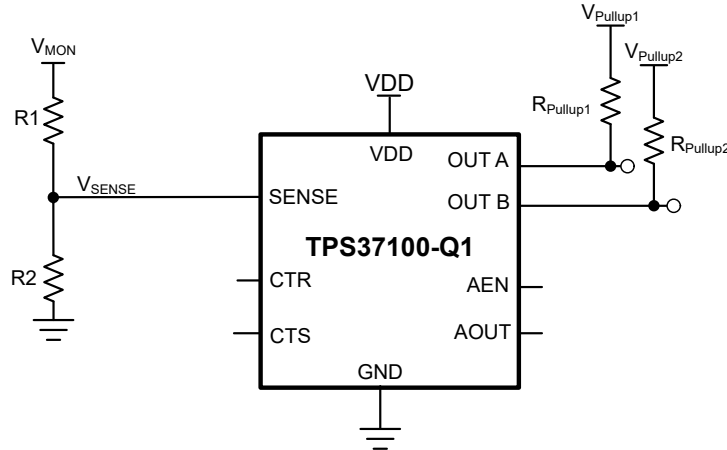


Figure 7-3. Adjustable Voltage Threshold with External Resistor Dividers

7.3.2.2 SENSE Hysteresis

TPS3710x-Q1 device offers built-in hysteresis around the UV and OV thresholds to avoid erroneous OUT A and OUT B deassertions. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}). [Figure 7-4](#) and [Figure 7-5](#) highlight the OUT A and OUT B behavior based on a window variant with standard OUT A/B.

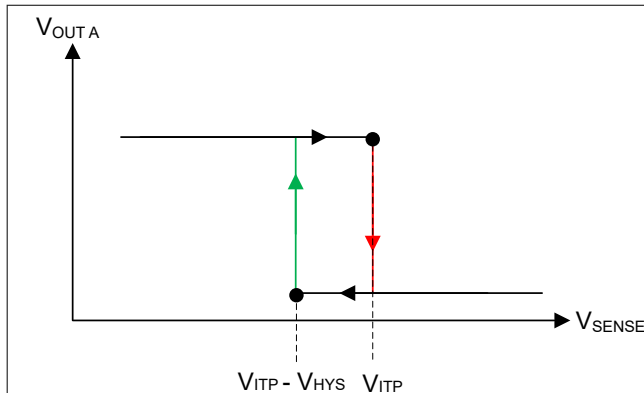


Figure 7-4. Hysteresis (Overvoltage Active-Low)

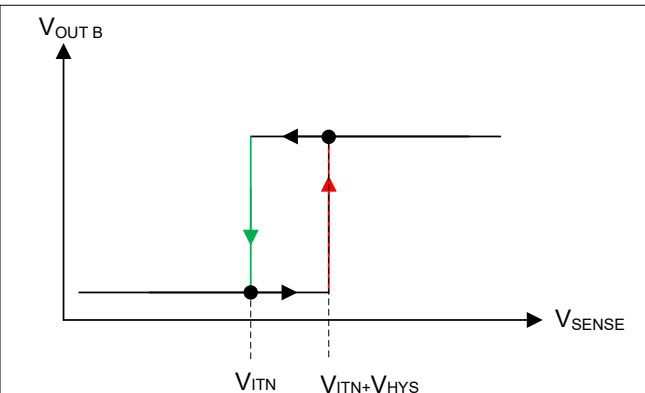


Figure 7-5. Hysteresis (Undervoltage Active-Low)

Table 7-1. Common Adjustable Threshold Hysteresis Lookup Table

ADJUSTABLE THRESHOLD	TARGET		DEVICE HYSTERESIS OPTION
	TOPOLOGY	RELEASE VOLTAGE (V)	
800mV	Overvoltage	792mV	-1%
800mV	Overvoltage	760mV	-5%
800mV	Overvoltage	720mV	-10%
800mV	Undervoltage	808mV	1%
800mV	Undervoltage	840mV	5%
800mV	Undervoltage	880mV	10%

[Table 7-1](#) shows a sample of hysteresis for the 800mV adjustable variant of TPS3710x-Q1.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is ($V_{ITN} + V_{HYS}$) and for the overvoltage (OV) channel is ($V_{ITP} - V_{HYS}$).

Undervoltage (UV)

- $V_{ITN} = 800\text{mV}$
- Voltage Hysteresis (V_{HYS}) = 1% = 8mV
- Release Voltage = $V_{ITN} + V_{HYS} = 808\text{mV}$

Overvoltage (OV)

- $V_{ITP} = 800\text{mV}$
- Voltage Hysteresis (V_{HYS}) = 1% = 8mV
- Release Voltage = $V_{ITP} - V_{HYS} = 792\text{mV}$

7.3.2.3 Reverse Polarity Protection

SENSE has -95V reverse polarity protection for fixed threshold options only. Adjustable threshold option does not have reverse polarity protection.

7.3.3 Output Logic Configurations

TPS3710x-Q1 is a single channel device that has a single input SENSE pin with dual outputs, OUT A and OUT B pins. The OUT A and OUT B pins are available only with open-drain active-low topology.

7.3.3.1 Open-Drain

The open-drain output pins require an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor, consider system V_{OH} and the Open-Drain Leakage Current (I_{lk}) provided in the electrical characteristics, high resistors values have a higher voltage drop affecting the output voltage high. The open-drain outputs can be connected as a wired-AND logic with other open-drain signals such as another TPS3710x-Q1 open-drain output pin.

7.3.3.2 Active-Low (OUT A and OUT B)

OUT A and OUT B (active low) remain high voltage (V_{OH} , deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO.

STANDARD: For **window (Overvoltage + Undervoltage) standard output variants**, to assert the OUT A or OUT B the sense pins must meet one of the conditions below:

- For OUT A, the SENSE voltage must cross the upper boundary (V_{ITP}).
- For OUT B, the SENSE voltage must cross the lower boundary (V_{ITN}).

COMBINED: For **window (Overvoltage + Undervoltage) combined output variants**, to assert the OUT A and OUT B the sense pins must meet one of the conditions below:

- The SENSE voltage must cross the upper boundary (V_{ITP}).
- The SENSE voltage must cross the lower boundary (V_{ITN}).

COMBINED: For **Undervoltage only variants**, to assert the OUT A and OUT B the sense pins must meet the condition below:

- For OUT A and OUT B, the SENSE voltage need to cross the lower boundary (V_{ITN}).

COMBINED: For **Overvoltage only variants**, to assert the OUT A and OUT B the sense pins must meet the condition below:

- For OUT A and OUT B, the SENSE voltage must cross the upper boundary (V_{ITP}).

7.3.4 User-Programmable Release Time Delay

TPS3710x-Q1 has adjustable release time delay with external capacitors.

- A capacitor on CTR programs the deassertion release time of the output.

- No capacitor on this pin gives the fastest release time indicated by t_{CTR} in [Section 6.6](#).
- Certain variants use a fixed internal time delay.

7.3.4.1 Deassertion Time Delay Configuration

Capacitor release time delay (t_{CTR}) occurs when the OUT A and OUT B transitioning from a fault state (V_{OL}) to a non-fault state (V_{OH}). The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND. For situations with a fault on SENSE after OUT A and OUT B recovers, the TPS3710x-Q1 makes sure that the CTR capacitor is fully discharged before starting the recovery sequence. This makes sure that the programmed CTR time is maintained for consecutive faults.

The relationship between external capacitor $C_{CTR_EXT (typ)}$ and the time delay $t_{CTR (typ)}$ is given by [Equation 3](#).

$$t_{CTR(typ)} = R_{CTR(typ)} \times C_{CTR_EXT(typ)} + t_{CTR(CTR=open)} \quad (3)$$

$R_{CTR (typ)}$ = is in kilo ohms (k Ω)

$C_{CTR_EXT (typ)}$ = is in microfarads (μ F)

$t_{CTR (typ)}$ = is in milliseconds (ms)

The release delay time varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in [Section 6.5](#), and the constant ($t_{CTR (CTR = open)}$) provided in [Section 6.7](#). The minimum and maximum variance due to the constant is show in [Equation 4](#) and [Equation 5](#):

$$t_{CTR(min)} R_{CTR(min)} C_{CTR_EXT(min)} + t_{CTR(CTR=open)} \quad (4)$$

$$t_{CTR(max)} R_{CTR(max)} C_{CTR_EXT(max)} + t_{CTR(CTR=open)} \quad (5)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold OUT A or OUT B active.

Leakages on the capacitor can affect accuracy of release time delay.

7.3.5 User-Programmable Sense Delay

TPS3710x-Q1 has adjustable sense release time delay with external capacitors.

- A capacitor on CTS programs the sense time delay of the input.
- When T_{CTS} is enabled, no capacitor on this pin gives the fastest sense delay time indicated by t_{CTS} in [Section 6.7](#).
- Certain TPS3710x-Q1 variants comes with an optional fixed internal time delay that disables the CTS pin and offers the fastest detection time (5 μ s). Check the [Section 4](#) to verify variant specific functionality.

7.3.5.1 Sense Time Delay Configuration

SENSE time delay (t_{CTS}) is the minimum length of time required to count a fault on the SENSE pin as a valid fault and assert OUT A and OUT B. The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS_EXT (typ)}$ and the time delay $t_{CTS (typ)}$ is given by [Equation 6](#).

$$t_{CTS (typ)} = R_{CTS (typ)} \times C_{CTS_EXT (typ)} + t_{CTS (CTS = Open)} \quad (6)$$

$R_{CTS (typ)}$ = is in kilo ohms (k Ω)

$C_{CTS_EXT (typ)}$ = is in microfarads (μ F)

$t_{CTS (typ)}$ = is in milliseconds (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in [Section 6.5](#), and the constant ($t_{CTS (CTS = Open)}$) provided in [Section 6.5](#). The minimum and maximum variance due to the constant is show in [Equation 7](#) and [Equation 8](#):

$$t_{CTS(min)} = R_{CTS(min)} \times C_{CTS_EXT(min)} + t_{CTS(CTS=open)} \quad (7)$$

$$t_{CTS(max)} = R_{CTS(max)} \times C_{CTS_EXT(max)} + t_{CTS(CTS=Open)} \quad (8)$$

The recommended maximum sense delay capacitor for the TPS3710x-Q1 is 10 μ F as this makes sure there is enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip unpredictably. This leads to a variation in time delay where the delay accuracy can be worse in the presence of system noise.

Leakages on the capacitor can affect accuracy of sense time delay.

7.3.6 Analog Out

The TPS3710x-Q1 family contains one buffer for supply voltage measurements. The integrated buffer outputs a voltage on the AOUT pin that is representative on the SENSE pin input voltage. The AOUT pin paired with an ADC can be used to directly measure the voltage on the SENSE pin. The AOUT simplifies the need for an external discrete network of resistors, capacitors, and FETs to measure a high voltage rail with a low voltage ADC.

The AOUT voltage depends on the analog out scale factor. The analog out scale factor can be found in [Section 4](#).

$$AOUT = SENSE / \text{Analog Out Scale} \quad (9)$$

For [Figure 7-6](#) the outputs are calculated in [Equation 10](#).

$$AOUT = SENSE / \text{Analog Out Scale} = 1.6V / 0.75 = 2.133V \quad (10)$$

The AOUT pin requires a 0.1 μ F capacitor for stability. Place the stability capacitor as close as possible to the pin. TI recommends to use a stability capacitor on AOUT even if the feature is not in use.

The AOUT can also be enabled or disabled using AEN on certain variants. When $AEN > 1.3V$ the AOUT is enabled. When the $AEN < 0.5V$ the AOUT is disabled. The AEN has a 100k Ω pull-down resistor which sets the default behavior as disabled. AOUT is always enabled for variants without AEN pin.

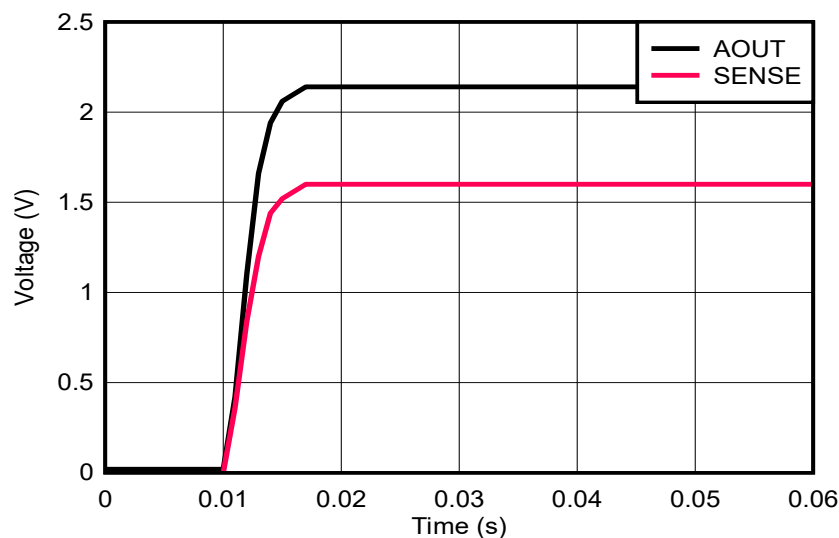


Figure 7-6. AOUT Following SENSE Pin

7.3.7 Built-in Self-Test

The built-in self-test (BIST) feature is only in TPS37102-Q1 option only. TPS37100-Q1 does not have BIST.

The BIST sequence of internal tests verifies the health of the internal signal chain of the device by checking for faults on the internal comparators on the SENSE pin, bandgap voltage, and OUT A and OUT B outputs.

The TPS37102-Q1 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device to monitor the health of the device. During power-up BIST is initiated automatically after crossing $V_{DD(min)}$. During BIST the $\overline{BIST}$ pin and OUT A and OUT B output asserts low and deasserts if the BIST test completes successfully indicating no internal faults in the device. The length of the BIST and $\overline{BIST}$ assertion is specified by t_{BIST} . If BIST is not successful, the $\overline{BIST}$ pin stays asserted low signifying an internal fault. The OUT A and OUT B output asserts on $\overline{BIST}$ failure. During BIST, the device is not monitoring the SENSE pin for faults and the OUT A and OUT B is not dependent on the SENSE pin voltage.

After a successful power-up sequence, BIST can be initiated any time with a rising edge input ($V_{BIST_EN} > 1.3V$) on the BIST_EN pin. BIST initiates and the $\overline{BIST}$ pin asserts only if the SENSE pin is not in a overvoltage or undervoltage fault mode.

7.3.7.1 Latch

The TPS37102-Q1 comes with the optional output reset latching feature for the window (OV and UV) and OV only variants. When using a variant with latch, latch is enabled when enabled $V_{BIST_EN} < 0.5V$ and latch is disabled when $V_{BIST_EN} > 1.3V$. The BIST_EN pin has an internal pull-down resistor to GND which enables latch at startup. When latch is enabled and a OV fault occurs, OUT A asserts and stays asserted regardless of voltage on SENSE pin. When $V_{BIST_EN} > 1.3V$, latch disabled, and $SENSE < V_{ITP} + HYST$ then OUT A deasserts after a delay. This delay depends on BIST and CTR timing. While $V_{BIST_EN} > 1.3V$, the device is in latch disabled mode and OUT A asserts for OV faults but does not latch.

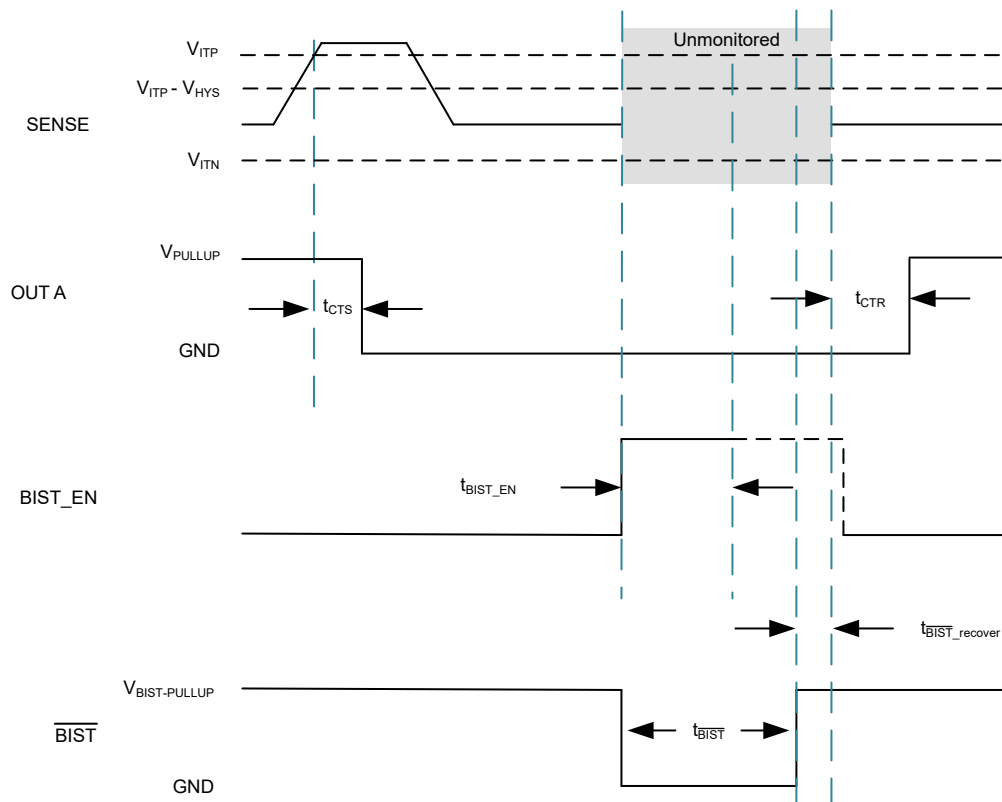


Figure 7-7. TPS37102 Latch Disable

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail how to properly use this device. As this device has many applications and setups, there are many situations that this datasheet cannot characterize in detail and vary from these applications depending on the requirements of the final application

8.2 Typical Application

8.2.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 48V batteries. Variation of the battery voltage is common from 40V to 55V. Furthermore, load transients can cause voltage spikes up to 100V. This design example highlights the ability for low-power, direct off-battery voltage supervision with capabilities to handle 100V transients.

Figure 8-1 shows an example of how the TPS37100-Q1 is monitoring the battery voltage while being powered by the same rail.

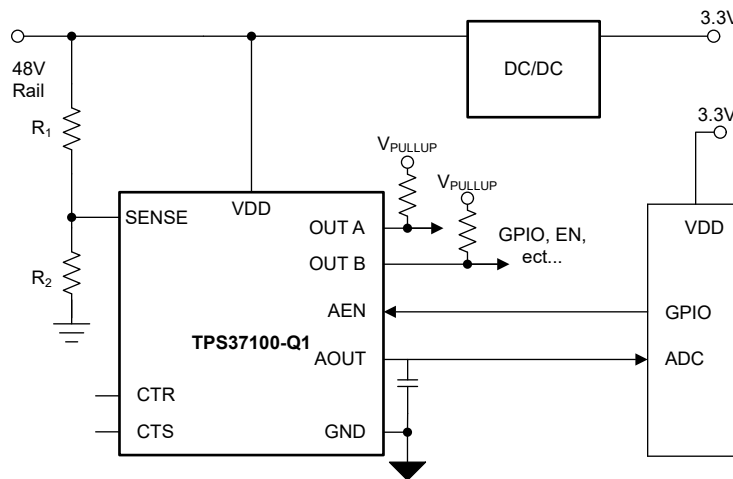


Figure 8-1. TPS37100-Q1 Overvoltage Supervisor with Direct Off-Battery Monitoring

8.2.1.1 Design Requirements

This design requires voltage supervision on a 48V battery voltage rail with possibility of the 48V battery rail rising up as high as 100V. The undervoltage fault occurs when the power supply voltage drops below 40V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 48V power supply for undervoltage condition, trigger a undervoltage fault at 40V.	TPS3710x-Q1 provides undervoltage monitoring up to 100V.
Maximum Input Power	Operate with power supply input up to 100V.	The TPS3710x-Q1 VDD, SENSE, OUT A pin can support a VDD of up to 105V.
Output logic voltage	Open-Drain Output Topology	OUT A and OUT B are both open-drain outputs.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Maximum system current consumption	1mA maximum when power supply is at 48V typical	TPS3710x-Q1 allows for I_Q to remain low with support of up to 100V. The Adjustable variant does require external resistors which increases the power consumption. A fixed threshold variant does not require external resistors which decreases the power consumption.
Always on monitor	Maximum voltage monitor accuracy of 1.5%.	The TPS3710x-Q1 has 0.8% maximum voltage monitor accuracy.
Feature	ADC monitoring for telemetry	The TPS3710x-Q1 has a AOUT pin that can be sampled by an ADC for voltage telemetry.

8.2.1.2 Detailed Design Procedure

The primary advantage of this application is being able to directly monitor a voltage on an automotive battery with the SENSE input.

Voltage rail monitoring is done by connecting the SENSE input to a external resistor ladder then to the battery rail. The TPS3710x-Q1 that is being used in this example is an adjustable voltage variant where the monitored threshold voltage has to be set externally. Word of caution, the TVS protection diodes must be selected such that the transient voltages on the monitored rails do not exceed the absolute maximum limit listed in [Section 6.1](#). Adjustable threshold variants do not offer reverse polarity protection on the SENSE pin.

To use this configuration, the specific voltage threshold variation of the device must be selected according to the application. In this configuration, the TPS37100Z91DDYYRQ1 is used.

The 40V undervoltage threshold is set by R1 and R2. Assuming $R_2 = 2k\Omega$, and R_1 can be calculated as $R_1 = 98k\Omega$.

The AOUT pin requires a 0.1 μ F stability capacitor. When operating at 48V the AOUT = 1.6V which pairs well with a 3 or 3.3V ADC of a MCU.

OUT A and OUT B can connect to different loads. Example, OUT A connects to the enable of a wide VIN DC/DC converter while OUT B can connect to a MCU GPIO.

8.2.1.3 Application Curves

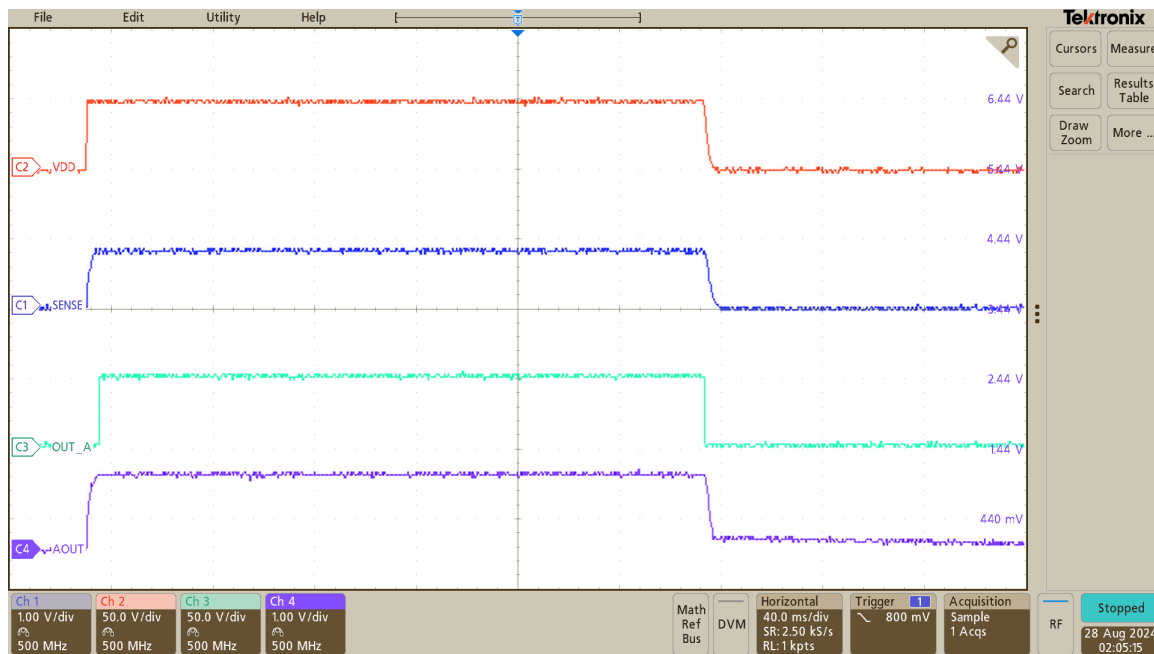


Figure 8-2. TPS3710x-Q1 waveform

8.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 3V (V_{POR}) to 105V (maximum operation). Good analog design practice recommends placing a minimum 0.1 μ F ceramic capacitor as near as possible to the VDD pin.

8.3.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using Equation 11:

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (11)$$

The actual power being dissipated in the device can be represented by Equation 12:

$$P_D = V_{DD} \times I_{DD} + P_{OUTA} + P_{OUTB} \quad (12)$$

P_{OUTA} and P_{OUTB} are calculated by Equation 13 or Equation 14. V_{OUTA} and V_{OUTB} depend on the assertion status of the outputs.

$$P_{OUTA} = V_{OUTA} \times I_{OUTA} \quad (13)$$

$$P_{OUTB} = V_{OUTB} \times I_{OUTB} \quad (14)$$

Equation 11 and Equation 12 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the

device. These two equations must be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) can be increased.

In applications where high power dissipation and poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) have to be de-rated. T_{A-MAX} depends on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 15:

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (15)$$

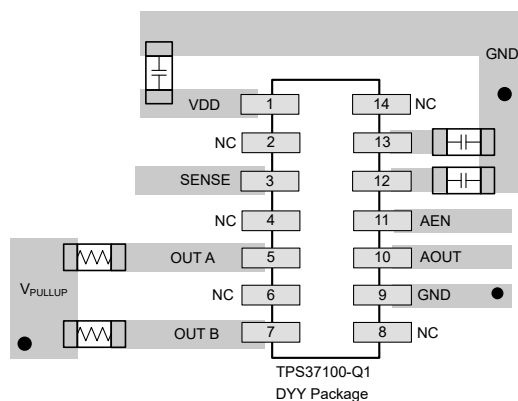
8.4 Layout

8.4.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than $0.1\mu\text{F}$ ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, either use the CTS feature with a 100pF capacitor or place a from 10nF to 100nF capacitor on the SENSE pin.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 20pF as this affects the delay of CTS and CTR.
- To further improve the noise immunity on the SENSE pins, either use the CTS feature with a 100pF capacitor or place a 10nF to 100nF capacitor on the SENSE pin.
- Place the AOUT stability capacitor as close as possible to the pin.
- For the open-drain outputs, place the pull-up resistors on OUT A, OUT B, and $\overline{\text{BIST}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces must be greater than 20mils (0.5mm).
- Do not have high voltage metal pads or traces closer than 20mils (0.5mm) to the low voltage metal pads or traces.

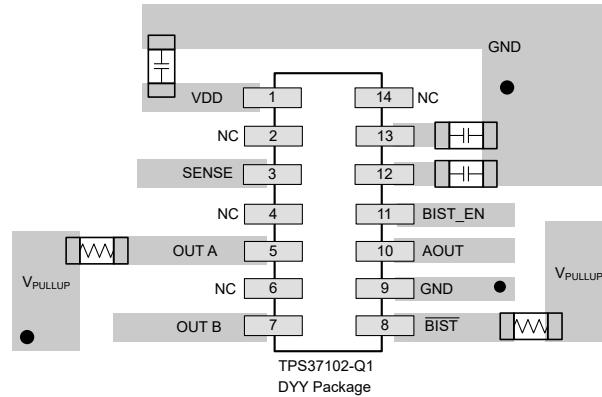
8.4.2 Layout Example

The layout example in Figure 8-3 shows how the TPS37100-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.



● Vias used to connect pins for application-specific connections

Figure 8-3. TPS37100-Q1 Recommended Layout



● Vias used to connect pins for application-specific connections

Figure 8-4. TPS37102-Q1 Recommended Layout

8.4.3 Creepage Distance

Per IEC 60664, Creepage is the shortest distance between two conductive parts or as shown in [Figure 8-5](#) the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

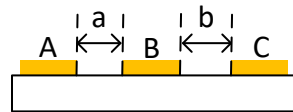


Figure 8-5. Creepage Distance

[Figure 8-5](#) details

- A = Left pins (high voltage)
- B = Central pad (conductive not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltages)
- Creepage distance = $a + b$

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2025) to Revision B (October 2026)	Page
• Updated Functional Safety wording.....	1
• Updated device naming convention by separating adjustable and fixed figures.....	3
• Updated device Threshold Table to reflect released orderables.....	3
• Updated to rename device Threshold Table to Available Devices.....	3
• Updated UV only and OV only variant OUT assertion descriptions.....	18

Changes from Revision * (May 2025) to Revision A (September 2025)	Page
• Changed TPS37100-Q1 device status from Advanced Information to Production Data	1
• Changed data sheet status from Advanced Information to Production Mixed.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS37100W41DDYYRQ1	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	371W41DQ
TPS37100Z91DDYYRQ1	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	371Z91DQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

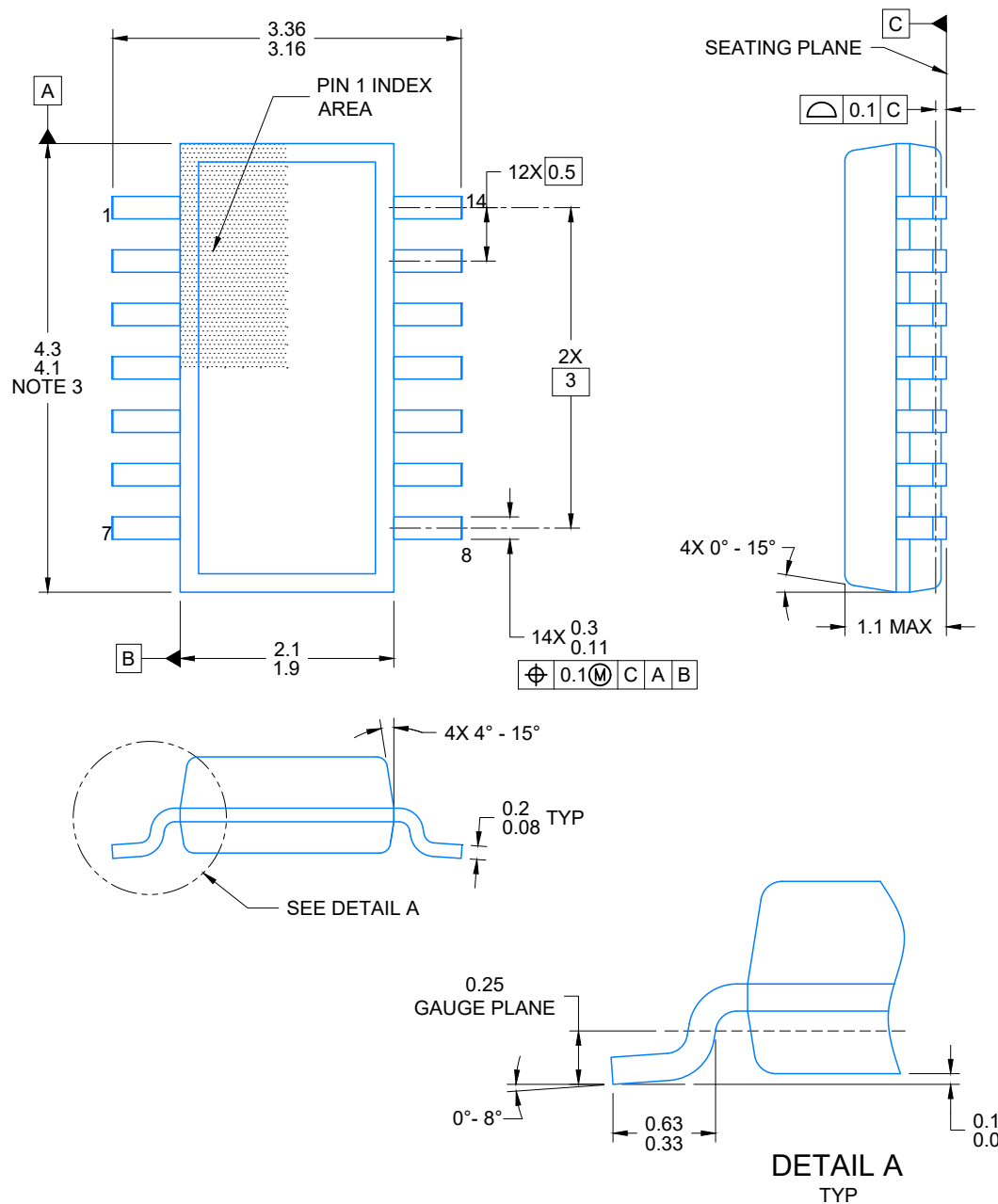
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS37100-Q1 :

- Catalog : [TPS37100](#)

NOTE: Qualified Version Definitions:

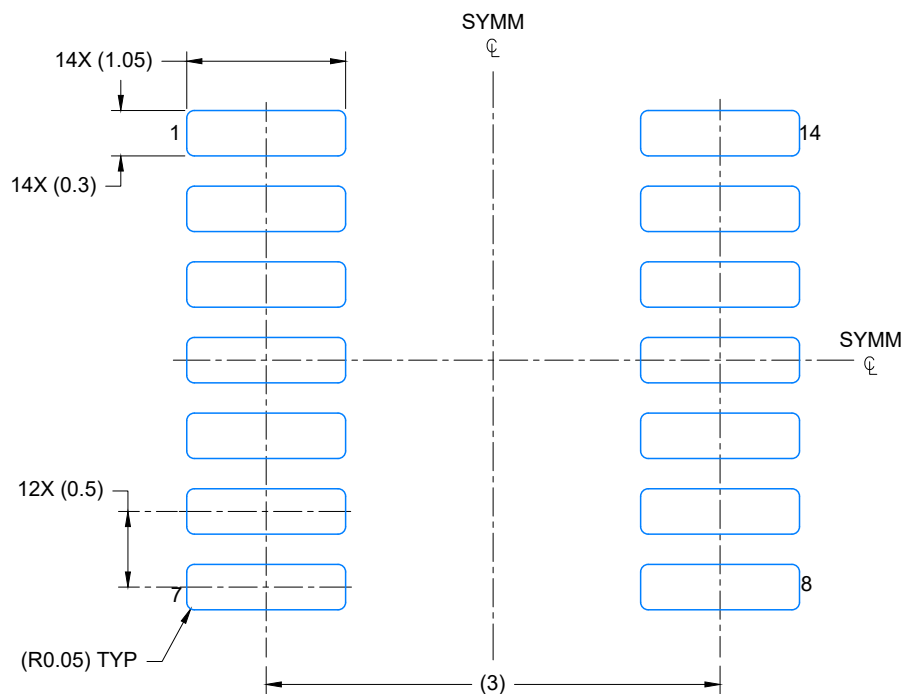
- Catalog - TI's standard catalog product



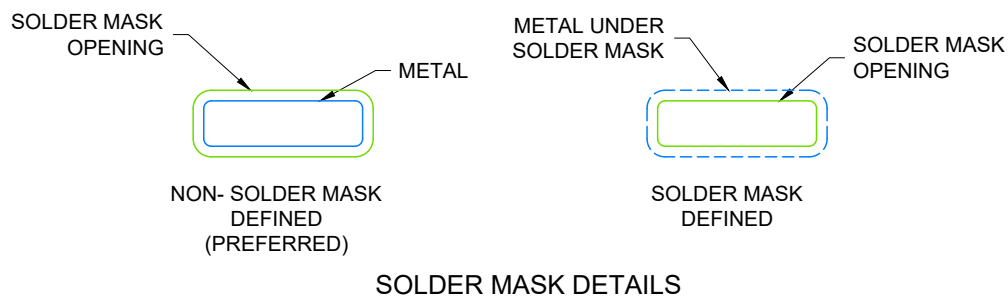
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



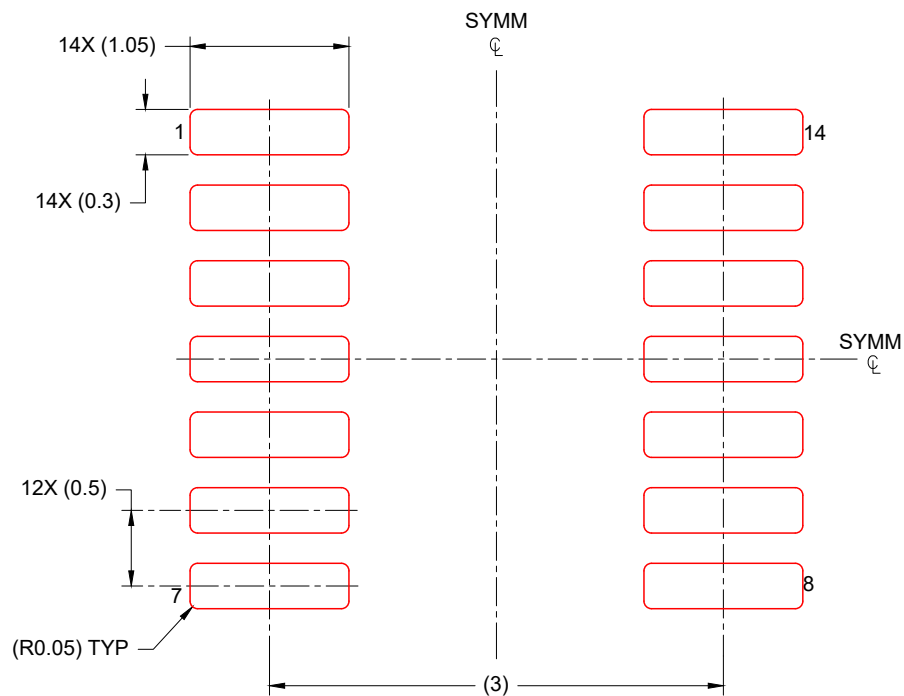
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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