AM13E232x Real-Time Microcontrollers

Technical Reference Manual

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Chapter 1

Read This First

1.1 About This Manual

This Technical Reference Manual (TRM) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device. The TRM should not be considered a substitute for the data sheet, rather a companion guide that can be used alongside the device-specific data sheet to understand the details to program the device. The primary purpose of the TRM is to abstract the programming details of the device from the data sheet. This allows the data sheet to outline the high-level features of the device without unnecessary information about register descriptions or programming models.

Note

Texas Instruments is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers can be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

1.2 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

1.3 Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for these devices, visit the Texas Instruments website at www.ti.com .

1.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 2

Introduction

This chapter introduces the features, subsystems, and architecture of the AM13E232x microcontroller platform.

Note

The AM13E232x microcontroller platform is hereinafter commonly referred to as *AM13E232x, platform, device,* or *chip*.

2.1 Overview.....20
2.2 AM13E232x Architecture.....20

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2.1 Overview

The AM13E232x series of microcontrollers (MCUs) are cost-optimized 32-bit devices built for complex real-time control applications such as motor control. AM13E232x MCUs include a high-performance Arm® Cortex®-M33 core operating at up to 250MHz with a proprietary math accelerator for trigonometric operations (TMU) through a Custom Datapath Extension (CDE) and a TinyEngine™ Neural-network Processing Unit (NPU) Artificial Intelligence (AI) Engine to enable simultaneous motor control and AI model execution. Its rich analog integration offers industry-leading speed, precision, and reduced system cost. The digital peripherals offered on AM13E232x MCUs are specifically designed for motor control applications, and include tailored communications interfaces for appliance and industrial motor drive end equipment.

The AM13E232x MCUs provide up to 512KB of embedded flash program memory (2 banks of 256KB) with built-in error correction code (ECC) and up to 192KB SRAM (6 banks of 32KB) with hardware parity.

AM13E232x MCUs are enabled with robust, high-performance analog peripherals. Three 12-bit ADCs, four high-speed comparators (CMPSS_LITE) with built-in 10-bit reference DACs, and three PGAs (programmable gain amplifiers) provide real-time signal-chain performance. These MCUs also offer intelligent digital peripherals such as two advanced control timers, TIMG4 (16-bit) and TIMG12 (32-bit), one Windowed Watchdog Timer (WWDT), and a 12-channel Direct Memory Access (DMA) controller.

Complex real-time control applications are enabled with the MCUs' five MCPWM modules with 6 channels per module, six EPWM modules with two high-resolution channels per module, three Enhanced Capture (ECAP) modules, and two Enhanced Quadrature Encoder Pulse (EQEP) modules. One Sigma-Delta Filter Module (SDFM) enables direct interface to external sigma-delta modulators for high-resolution current and voltage sensing. The integrated crossbar (XBAR) infrastructure enables flexible configuration and routing of external signals to internal ports and internal signals to external pins.

Data integrity and encryption features (AES, secure boot) provide security across the AM13E232x domains. The Keystore module provides secure management of the AES keys. A Cyclic Redundancy Checker (CRC) module provides internal diagnostics to the AM13E232x MCU.

Enhanced communication interfaces are supported through the two MCAN (CAN-FD) interfaces and two advanced SPG (Serial Peripheral Group) blocks. Each SPG block offers three UNICOMM (Unified Communications Module) blocks, for a total of 6 UNICOMM modules. Within an SPG block, two of the UNICOMM modules can be configured as UART, I2C, or SPI, and one module can be configured as UART/LIN or I2C/SMBUS. Industrial connectivity is enabled through one EtherCAT SubDevice controller interface, and one Fast Serial Interface (FSI) module that provides high-speed, low-latency serial communication for multi-device systems.

The AM13E232x series of microcontrollers (MCUs) offers a range of options in various memory, peripheral, and package configurations, enabling customers to find the most fitting solution that meets their specific project needs. The AM13E232x MCU platform combines the Arm® Cortex®-M33 platform with a holistic low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

2.2 AM13E232x Architecture

The AM13E232x Microcontroller is based on the Arm® Cortex-M33 core running at 250MHz. The device is organized into various functional blocks, each associated with specific clock and power domains. The functional blocks are interfaced through a network of interconnects and buses that connect across the clock and power domains. This section will give a high-level overview of the clock and power domains, interconnects, and peripherals available on this microcontroller.

2.2.1 Bus, Power, Clock Organization

There are two main power domains on AM13E232x devices:

- **PD1** (Power Domain 1): Includes the CPU Subsystem, DMA, SRAM, and PD1 Peripheral Buses
- **PD0** (Power Domain 0): Includes PD0 peripherals and PD0 Bus

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PD1 and PD0 are supplied by the 3.3V VDD input to the MCU, and the on-board STOP (1.0V) and Main (1.35V) LDOs, which supply power to modules with lower voltage requirements. The PD1 domain supports higher clock speeds for performance, and is disabled in certain operating modes to minimize power consumption. The PD0 domain supports low-power performance and is always enabled in operating modes in which the core regulator is operating.

The device clocks are generated from several internal and external oscillators. External oscillators include a crystal oscillator input (20MHz) or a high-frequency clock input (4MHz-48MHz). Internal oscillators include the System Oscillator (SYSOSC, up to 32MHz), and Low-Frequency Oscillator (LFOSC, 32kHz). PLL clocks are generated from the HPLL clock module, programmable up to 250MHz.

The M33 CPU is the fastest operating module in the device, and is clocked at the maximum frequency, 250MHz, referred to as MCLK. Peripheral blocks that do not require MCLK operate at speeds MCLK/2 (maximum frequency divided by 2), or MCLK/4 (maximum frequency divided by 4). Peripheral buses that cross clock domains are connected through SYNC bridges, which ensure that all clock domains are synchronous to the MCLK domain.

There are four main data buses on AM13E232x devices:

- S-AHB (System) bus matrix, interfaces the CPU to all peripheral buses
- C-AHB (CPU) bus matrix, interfaces the CPU to device memory systems (ROM, Flash memory, SRAM3)
- NPU bus, interfaces the Neural-Network Processing Unit to the device SRAM
- DMA bus, interfaces all peripheral buses to the device SRAM and Flash memory

The data buses allow communication between the Peripheral Interconnects on the device. The peripheral interconnects operate in different power and clock domains:

- Fast Peripheral Interconnect (PD1, MCLK)
- Peripheral Interconnect (PD1, MCLK/2)
- CPU Interconnect (PD1, MCLK/4)
- PD0 Interconnect (PD0, MCLK/4)

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2.2.2 Device Block Diagram

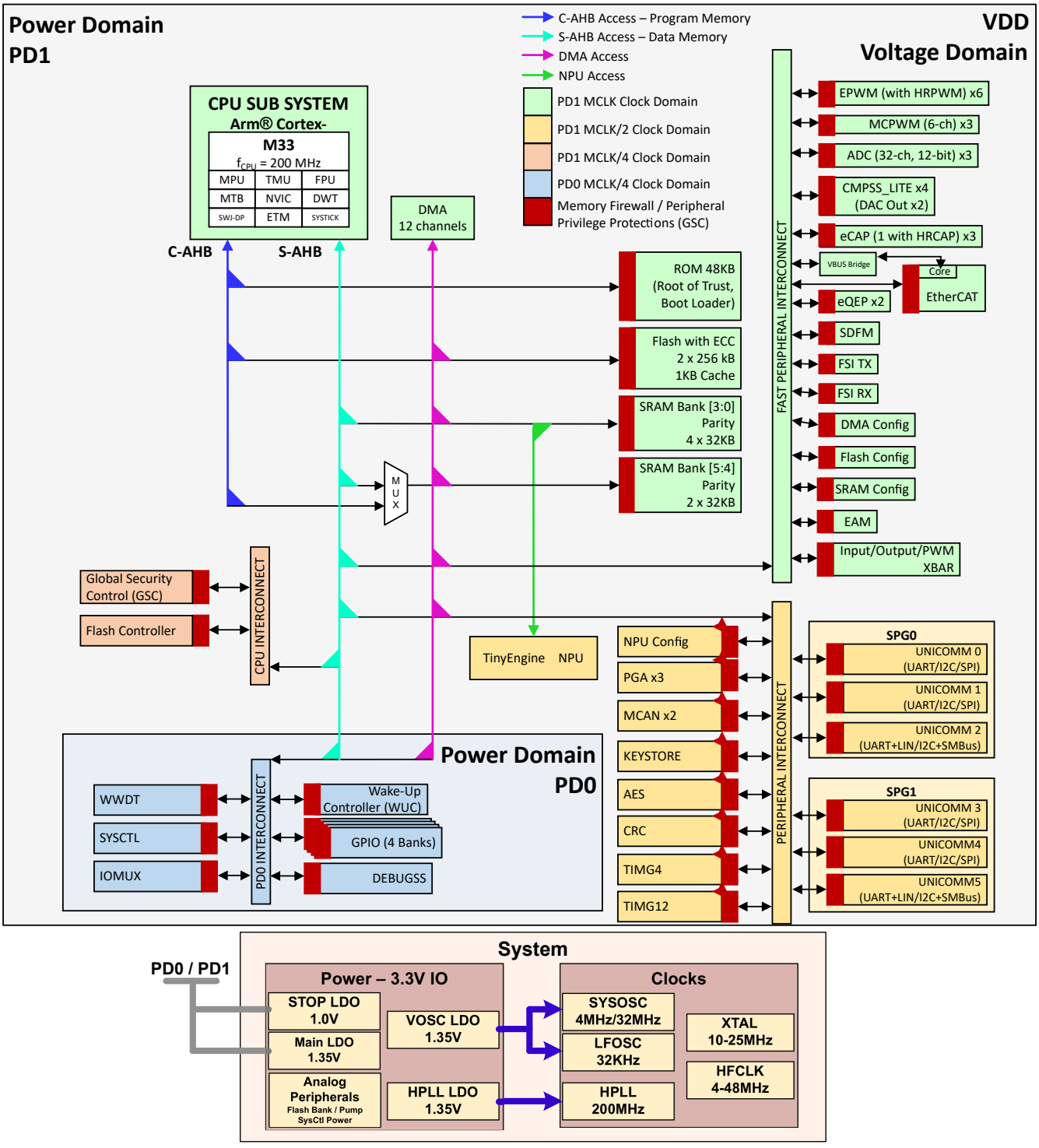


Figure 2-1. AM13E232x Block Diagram

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2.2.3 Module Allocation and Instances

Table 2-1. AM13E232x Module Allocation and Instances

Module Abbreviation	Module Full Name	Size / Device Instances	Power Domain	Notes
CPU & System				
M33 CPU	Arm® Cortex-M33	1	PD1	Includes Custom Datapath Extension (CDE) interface
TMU	Trigonometric Math Unit	1	PD1	
CPUSS Components	Central Processing Unit Subsystem Components	1	PD1	Includes: • Memory Protection Unit (MPU) • Floating-Point Unit (FPU) • Nested Vectored Interrupt Controller (NVIC) • Data Watchpoint and Trace Unit (DWT) • JTAG/Serial Wire Debug ports (SWJ-DP) • Micro Trace Buffer (MTB) • Embedded Trace Macrocell (ETM) • SysTick - 24-bit down counter
TinyEngine™ NPU	Neural-Network Processing Unit	1	PD1	Machine learning accelerator
DMA	Direct Memory Access Controller	1	PD1	12 channels
DEBUGSS	Debug Subsystem	1	PD0	
EAM	Error Aggregator Module	1	PD1	
Memories				
ROM	Read-Only Memory	48KB	PD1	
SRAM	Static Random-Access Memory	192KB	PD1	6 SRAM blocks, each with 32KB. All blocks have hardware parity support.
Flash	Flash Memory	512KB	PD1	Up to 2 banks of 256KB each with Error Correction Code (ECC)
General Connectivity & Communcation Peripherals				
GPIO	General Purpose Input/Output	Up to 107	PD0	
ESC	EtherCAT® SubordinateDevice Controller	1	PD1	
FSI	Fast Serial Interface	1 TX, 1 RX	PD1	
SPG0	Serial Peripheral Group 0	3 UNICOMMs	PD1	UC0: UART / SPI / I2C
				UC1: UART / SPI / I2C
				UC2: UART + LIN / I2C + SMBus
SPG1	Serial Peripheral Group 1	3 UNICOMMs	PD1	UC3: UART / SPI / I2C
				UC4: UART / SPI / I2C
				UC5: UART + LIN / I2C + SMBus
MCAN	Modular Controller Area Network	2	PD1	CAN-FD peripheral with 1KB of RAM
Timer Modules				
TIMG4	32-bit Timer Module	1	PD1	16-bit, general-purpose counter
TIMG12	16-bit Timer Module	1	PD1	32-bit, general-purpose counter
WWDT	Windowed WatchDog Timer	1	PD0	25-bit windowed watchdog timer driven from LFOSC

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Table 2-1. AM13E232x Module Allocation and Instances (continued)

Module Abbreviation	Module Full Name	Size / Device Instances	Power Domain	Notes
Analog Peripherals				
ADC	Analog to Digital Converter	3 32 input channels per ADC	PD1	6.9MSPS at 250MHz CPU speed
PGA	Programmable Gain Amplifier	3	PD1	4:1 input mux for effective 12-ch
CMPSS_LITE	Comparator Subsystem	4	PD1	2 of 4 CMPSS_LITE have DAC Output
VREF	Voltage Reference	1	PD1	ADC voltage reference. Internal reference and brought out to external pin.
Digital Control Peripherals				
EPWM	Enhanced Pulse Width Modulator	6	PD1	2 channels per module. 4 of 6 EPWMs have HRPWM capabilities.
MCPWM	Multi-Channel Pulse Width Modulator	3	PD1	6 channels per module
ECAP	Enhanced Capture Module	3	PD1	32-bit counter for input capture or PWM output. 1 of 3 channels have HRCAP capabilities.
EQEP	Enhanced Quadrature Encoder Pulse Module	2	PD1	32-bit counter for incremental encoders or capture
SDFM	Sigma Delta Filter Module	1	PD1	4 channels per module
System Clock Modules				
SYSOSC	System Oscillator	1	PD0	4MHz / 32MHz
LFOSC	Low-frequency Oscillator	1	PD0	32kHz
XTAL	External high-frequency Crystal Connection	1	PD1	10MHz - 20MHz
HFCLK	External high-frequency clock input	1	PD1	4MHz - 48MHz
PLL	Phase-Locked Loop	1		250MHz
System Power Modules				
REFSYS	Reference System	1	PD0	Supplies required current and voltage references to all analog modules
POR	Power On Reset circuit	1	PD0	
BOR	Brown Out Reset circuit	1	PD0	
TEMPSENSE	Temperature Sensor	1	PD0	
Safety & Security Modules				
AES	Advanced Encryption Standard encryption/decryption	1	PD1	
CRCP	Cyclic Redundancy Checker	1	PD1	32-bit CRC
GSC	Global Security Controller	1	PD1	
Keystore	Keystore Controller	1	PD1	Controller that provides secure management of the AES keys
Crossbar (XBAR) Modules				
INPUTXBAR	Flexible Signal Multiplex Input Crossbar	1	PD1	Routes external input signals to a GPIO pin to internal peripheral blocks
OUTPUTXBAR	Flexible Signal Multiplex Output Crossbar	1	PD1	Routes signals from internal peripheral blocks to an external GPIO pin

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Table 2-1. AM13E232x Module Allocation and Instances (continued)

Module Abbreviation	Module Full Name	Size / Device Instances	Power Domain	Notes
PWMXBAR	PWM Signal Crossbar	1	PD1	Routes input signals from internal peripheral blocks to an MCPWM instance

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Chapter 3

System Controller (SYSCTL)

The system-level configuration of this microcontroller includes the power, clocking, reset, NRST and JTAG/SWD pin mux control, flash bank swap control, and ECC error handling functionality.

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3.12 FACTORY Registers 184

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3.1 System Control Overview

The system control module, called SYSCTL, provides the two power and clocking analog submodules (PMU and CKM), control logic, and interface for these functions. In addition, SYSCTL contains the memory-mapped registers used by software to configure power management and clocks, assess the status of the device, and control resets.

The PMU is an analog submodule that generates the internal regulated supplies for the device and supervises the condition of the external supply. The PMU also contains voltage and current reference circuits used by the on-chip regulators and analog peripherals.

The CKM is an analog submodule that provides clock sources (internal and external oscillators) and presents these clock sources to SYSCTL. SYSCTL distributes these clock sources to the CPU, buses, and peripherals on the device.

The Figure 3-1 shows the interfaces between the system controller and the device supplies, clocks, and signals. Configuration of the SYSCTL by software is always done through the memory-mapped SYSCTL registers.

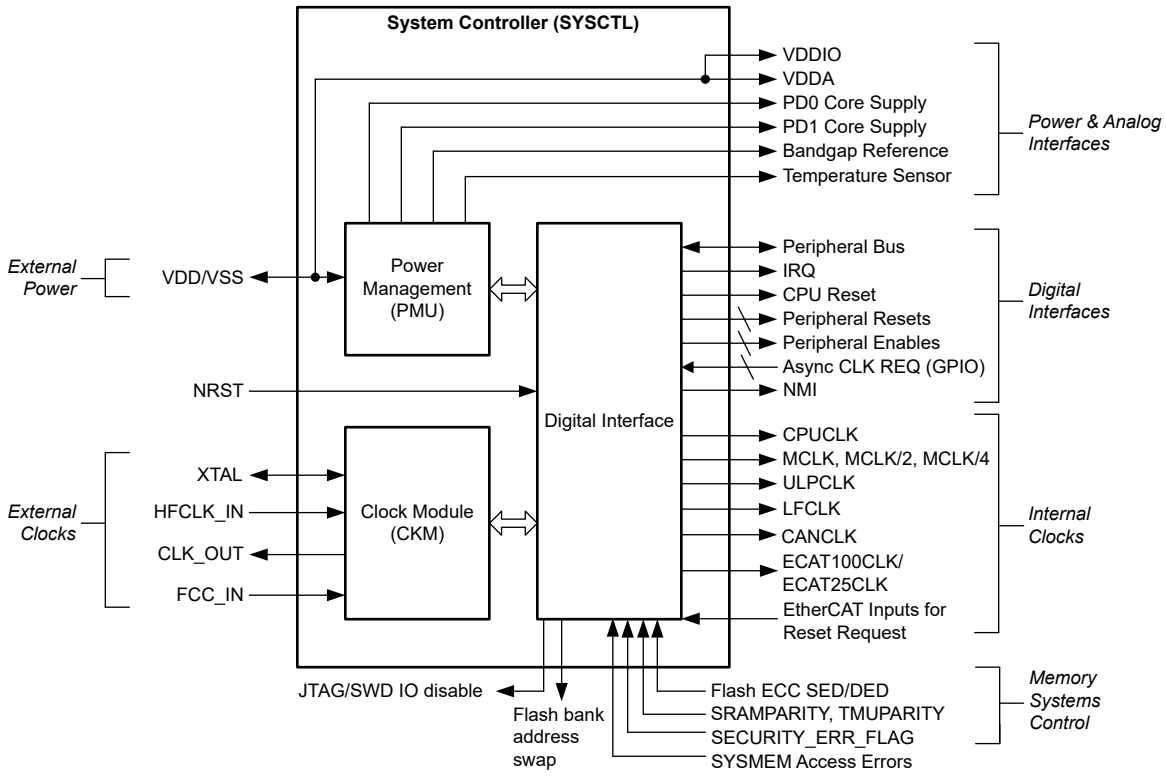


Figure 3-1. Sysctl Top-Level Diagram

Using this Guide

The PMU and CKM sections of this chapter describe the functionality provided by each submodule in detail.

Section 3.2 describes overall system level operation of system controller and how to configure SYSCTL for different application scenarios.

3.1.1 Power Domains

Two core power domains are provided on the device: PD1 and PD0. PD1 is always powered in RUN and SLEEP modes and switched off in STOP and STANDBY modes. PD0 is always powered in RUN, SLEEP, STOP and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

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Table 3-1. Power Domains Summary

Power Mode	PD1	PD1 Supply	PD0	PD0 Supply	LDO Switch
RUN	ON	MAIN LDO	ON	MAIN LDO	CLOSED
SLEEP	ON (CPU clocks gated)	MAIN LDO	ON	MAIN LDO	CLOSED
STOP	OFF	STOP LDO (retention logic/memory)	ON	STOP LDO	OPEN
STANDBY	OFF	STOP LDO (retention logic/memory)	ON	STOP LDO	OPEN
SHUTDOWN	OFF	N/A	OFF	N/A	N/A

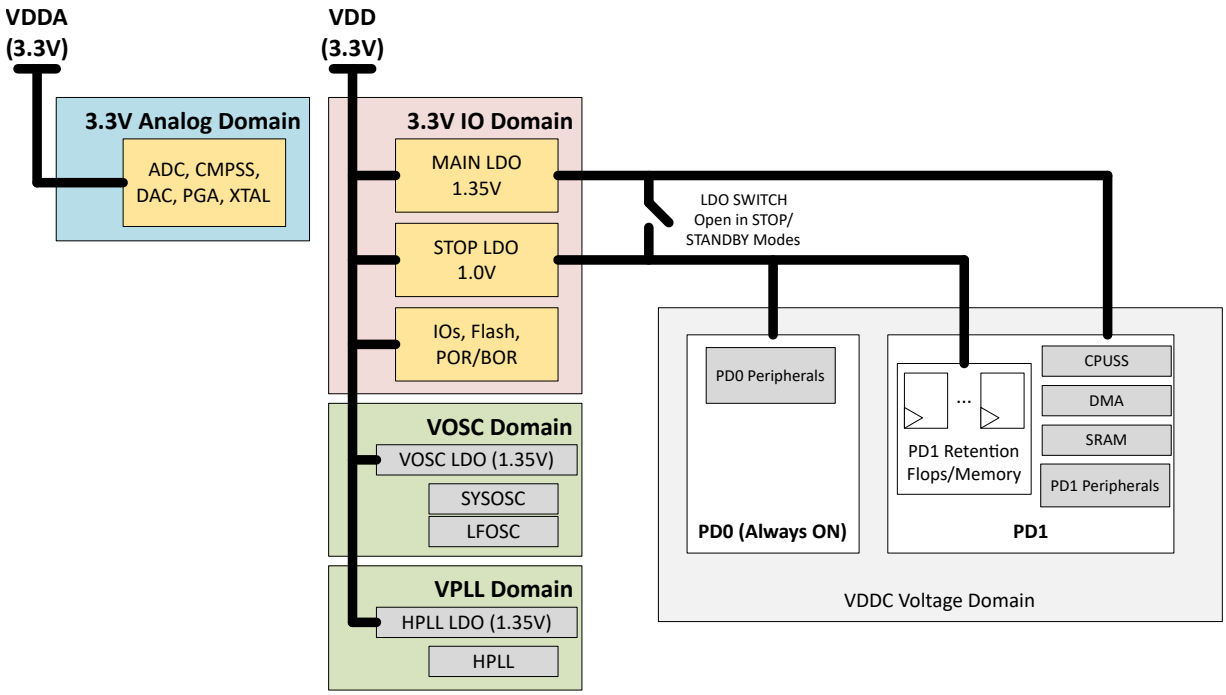


Figure 3-2. Power Hierarchy Block Diagram

- The PD1 domain includes the CPU subsystem, DMA, SRAM, and PD1 peripheral buses: Fast Peripheral Interconnect, Peripheral Interconnect, and CPU Interconnect which run from MCLK, MCLK/2, and MCLK/4, respectively.
- The PD0 domain includes the PD0 peripherals and PD0 bus segment (PD0 Interconnect) which runs at MCLK/4 in RUN and SLEEP mode, 4MHz in STOP mode, and 32kHz in STANDBY mode. This clock source, derived from MCLK/4 is referred to as ULPCLK. The PD0 domain is powered in all modes except SHUTDOWN and can be thought of as an "always-on" domain.
- The VDDC domain includes both PD1 and PD0

Note

For AM13E232x devices, MCLK=250MHz.

- The VDD domain refers to the single external power supply that provides power to the IO and analog peripherals.

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Note

For AM13E232x devices, VDD=3.3V

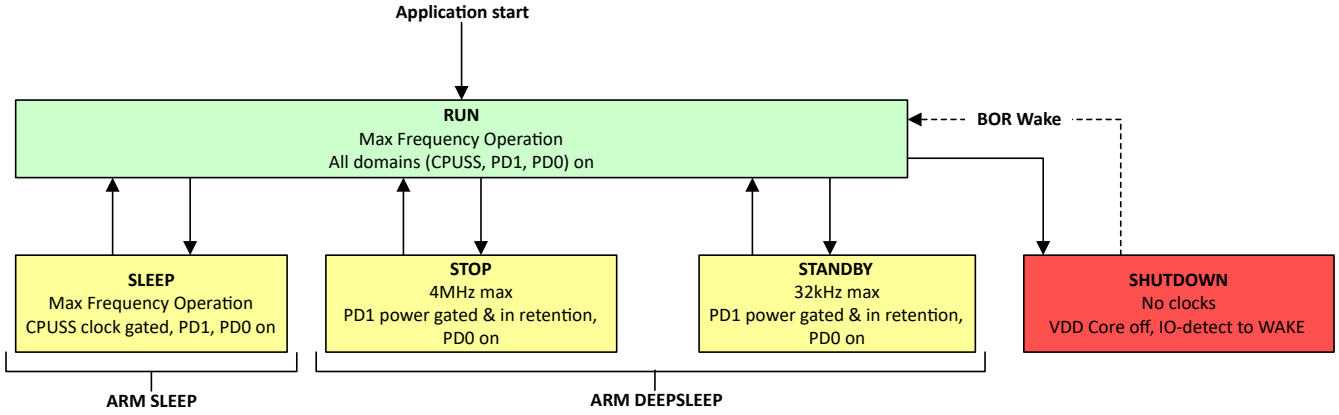
The *Module Allocation and Instances* table describes which peripherals on a device are in PD1 and which are in PD0.

The *Power Supply* section describes the individual power supplies on the device.

3.1.2 Operating Modes

Various operating modes (power modes) are provided to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY and SHUTDOWN. The following figure shows the interaction between the modes.

Figure 3-3. Operating Power Modes



Note

For AM13E232x devices, the Max Frequency Operation is 250MHz (MCLK).

Supported Functionality by Operating Mode details what functions are available in each operating mode of the device. See the Operating Mode Selection section for information on how to configure the device for a particular operating mode.

Operating Mode Concept

The MCU implements a policy-based power and clock management scheme. Policies can be configured through application software to manage the clock in each operating mode to obtain the best balance of power and performance for a given application.

After the operating policy for each mode is configured, application software can enter and exit the various operating modes through simple register commands, and SYSCTL automatically manages all the necessary PMU states, oscillator and clock enable and disables.

A variety of hardware-triggered low-power mode suspension mechanisms also exist to enable on-demand access to a fast clock when requested by supported peripherals in STOP mode. All wakeups bring the device to RUN mode.

The policy-driven operating mode scheme enables application software to select the operating mode and corresponding policy that provide the lowest possible power consumption for background activities, bringing up a fast clock, or bringing the device to RUN (in the case of an IRQ) for burst handling.

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3.1.2.1 RUN Mode

In RUN mode, the CPU is actively executing code and any peripheral can be enabled. In this mode, the MCLK and CPUCLK run from a fast clock source (SYSOSC, HFCLK, or SYSPLL). The VDDC domain is supplied by the on-chip MAIN LDO.

All functions are available at the highest frequency in this mode. If needed, software can be configured to a lower PLL frequency or lower system clock frequency to save dynamic power. For more information on configuring the PLL frequency, refer to the *System Phase-Locked Loop (SYSPLL)* Section.

3.1.2.2 SLEEP Mode

In SLEEP mode, the CPU is disabled (clock gated). Otherwise, the device configuration is the same as RUN.

3.1.2.3 STOP Mode

In STOP mode, the PD1 power domain is switched off and CPU, DMA, SRAM, FLASH, PLL, XTAL, and PD1 peripherals are disabled and kept in retention mode. The VDDC domain voltage is reduced to 10% as the active PD0 peripherals operate at 4MHz, supplied by SYSOSC appropriately divided to get the lower clock output.

During STOP mode operation, the SYSPLL/XTAL/HFCLKIN are switched off.

3.1.2.4 STANDBY Mode

In STANDBY mode, the PD1 power domain is switched off and CPU, DMA, SRAM, FLASH, PLL, XTAL, and PD1 peripherals are disabled and kept in retention mode. VDDC supply voltage is reduced to 10% and active PD0 peripherals operate at a maximum frequency of 32KHz, supplied by LFOSC. High-speed oscillators such as SYSPLL, XTAL, HFCLK_IN and SYSOSC are disabled. A GPIO toggle can wake the device from this mode.

There are 2 policy options for STANDBY mode: STANDBY0 and STANDBY1.

- **STANDBY0**: All PD0 peripherals receive the ULPCLK and LFCLK. A GPIO toggle can synchronously wakeup the device.
- **STANDBY1**: This is the lowest device power mode. PD0 peripherals (such as GPIO) can wake the system upon an external event through an asynchronous fast clock request, but PD0 peripherals are not actively clocked in this policy option.

3.1.2.5 SHUTDOWN Mode

In SHUTDOWN mode, core clocks are not available. The core regulator is completely disabled and all SRAM and register contents are lost, with the exception of the general-purpose memory in SYSCTL that can be used to store state information. The BOR and bandgap circuit are disabled.

Specific IO configuration settings are retained in the SHUTDOWN operating mode.

- Drive strength
- Pullup enable
- Pulldown enable
- Input enable
- Output enable
- Output state

The device can wake through a wake-up capable IO, a debug connection, or NRST.

SHUTDOWN mode has the lowest current consumption of any operating mode. Exiting SHUTDOWN mode triggers a BOR.

3.1.2.5.1 Shutdown Mode Handling

When the device is configured to enter SHUTDOWN mode, the core regulator is powered down and the device register contents and SRAM contents are lost. An exit from SHUTDOWN mode generates a BOR level reset. Two mechanisms are provided to preserve the device state when entering SHUTDOWN mode: IO latching and a small shutdown memory.

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Shutdown IO State

The digital IO pin states (output low/high, pullup/pulldown, Hi-Z, drive configuration) are latched and retained upon entry to SHUTDOWN for pins supporting Wakeup functionality (refer to the device data sheet for the list of WAKEUP pins). After exiting SHUTDOWN mode, the IOs are held in the previous state until released by application software setting the RELEASE bit in the SHDNIOREL register along with the matching KEY value. When exiting SHUTDOWN mode, application software must first re-configure the IO to the proper state, then release the IO. To determine at startup if an exit from SHUTDOWN mode caused the reset, application software must read the RSTCAUSE register in SYSCTL.

Note

When exiting SHUTDOWN, the bootstrap loader (BSL) invoke pin must be held at a logic low level to prevent unintended entry into the BSL during exit from SHUTDOWN. An entry to the BSL during SHUTDOWN exit prevents the application code from starting. The BSL interfaces are not be available, and a SWD connection is possible since the IO states remain latched through SHUTDOWN exit until application software releases the IOs.

Shutdown Memory

To enable saving of application state information before entering SHUTDOWN mode, 4 bytes of shutdown memory are provided in SYSCTL. These memory locations are retained in SHUTDOWN mode and are readable by the application after exiting SHUTDOWN. To save data to the SHUTDOWN memory, write to the SHUTDNSTORE0-SHUTDNSTORE3 registers in SYSCTL.

3.1.2.6 Supported Functionality by Operating Mode

The table below summarizes the behavior of different peripheral instances in each operating mode:

Table Legend

- **EN:** The function is enabled in the specified mode
- **DIS:** The function is disabled (either clock or power gated) in the specified mode
- **RET:** The function's memory and configuration is retained
- **OPT:** The function is optional in the specified mode, and remains enabled if configured to be enabled

Table 3-2. Power Modes Summary

		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
Supply State	**VDD**	*3.3V*	*3.3V*	*3.3V*	*3.3V*	*3.3V*	*3.3V*
	VDDC	*1.35V*	*1.35V*	*1.0V*	*1.0V*	*1.0V*	*0V*
PMU	**POR Monitor**	*EN*	*EN*	*EN*	*EN*	*EN*	*EN*
	BOR Monitor	*EN*	*EN*	*EN*	*EN*	*EN*	*DIS*
	Main LDO	*EN*	*EN*	*DIS*	*DIS*	*DIS*	*DIS*
	STOP LDO	*EN*	*EN*	*EN*	*EN*	*EN*	*DIS*
	VOSC LDO	*EN*	*EN*	*EN*	*EN*	*EN*	*DIS*
Oscillators	**SYSOSC**	*EN*	*EN*	*EN*	*DIS*	*DIS*	*DIS*
	SYSOSC Frequency	*32MHz*	*32MHz*	*4MHz*	*DIS*	*DIS*	*DIS*
	LFOSC	*EN*	*EN*	*EN*	*EN*	*EN*	*DIS*
	XTAL	*OPT*	*OPT*	*DIS*	*DIS*	*DIS*	*DIS*
Clocks	**MCLK**	*250MHz*	*250MHz*	*DIS*	*DIS*	*DIS*	*DIS*
	MCLKDIV2	*125MHz*	*125MHz*	*DIS*	*DIS*	*DIS*	*DIS*
	MCLKDIV4	*62.5MHz*	*62.5MHz*	*DIS*	*DIS*	*DIS*	*DIS*
	CPUCLK	*250MHz*	*DIS*	*DIS*	*DIS*	*DIS*	*DIS*
	LFCLK	*32kHz*	*32kHz*	*32kHz*	*32kHz*	*32kHz*	*DIS*
	ULPCLK	*50MHz*	*50MHz*	*4MHz*	*32kHz*	*DIS*	*DIS*
	CANCLK	*100MHz*	*100MHz*	*DIS*	*DIS*	*DIS*	*DIS*

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Table 3-2. Power Modes Summary (continued)

		RUN	SLEEP	STOP	STANDBY0	STANDBY1	SHUTDOWN
	ECAT25CLK	*25MHz*	*25MHz*	*DIS*	*DIS*	*DIS*	*DIS*
	ECAT100CLK	*100MHz*	*100MHz*	*DIS*	*DIS*	*DIS*	*DIS*
Core Functions	**CPU**	*EN*	*DIS*	*DIS*	*DIS*	*DIS*	*DIS*
	TMU	*EN*	*DIS*	*RET*	*RET*	*RET*	*DIS*
	FPU	*EN*	*DIS*	*RET*	*RET*	*RET*	*DIS*
	TINYENGINE™ NPU	*EN*	*DIS*	*DIS*	*DIS*	*DIS*	*DIS*
	DMA	*EN*	*EN*	*DIS*	*DIS*	*DIS*	*DIS*
	Flash Controller	*EN*	*EN*	*DIS*	*DIS*	*DIS*	*DIS*
	SRAM0	*EN*	*EN*	*RET*	*RET*	*RET*	*DIS*
	SRAM1-*5*	*EN*	*EN*	*DIS*	*DIS*	*DIS*	*DIS*
Peripherals	**PD0 Peripherals**	*OPT*	*OPT*	*DIS*	*DIS*	*DIS*	*DIS*
	PD1 Peripherals	*OPT*	*OPT*	*DIS*	*DIS*	*DIS*	*DIS*
	PD1 Peripheral Retention Logic	*EN*	*EN*	*RET*	*RET*	*RET*	*DIS*
Analog	**ADC**	*OPT*	*OPT*	*DIS*	*DIS*	*DIS*	*DIS*
	CMPSS	*OPT*	*OPT*	*DIS*	*DIS*	*DIS*	*DIS*
	VREF	*EN*	*EN*	*EN (Sampled)*	*EN (Sampled)*	*EN (Sampled)*	*DIS*
IOMUX		*EN*	*EN*	*EN*	*EN*	*EN*	*DIS*
Wake Sources		N/A	• Any IRQ • IO • DMA Request • Debug Req • WWDT	• IO (all) • Debug Request • WWDT	• IO (all) • Debug Request • WWDT	• IO (all) • Debug Request	• IO (subset)(1) • Debug Request

(1) Select WAKEUP GPIOs

3.1.2.7 Operating Mode Selection

The device operating mode is configured through the use of the following:

1. Policy bits in the SYSOSCCFG and MCLKCFG registers in SYSCTL (to control the behavior of SYSOSC in RUN, SLEEP, and STOP modes)
2. Policy bits in the PMODECFG register in SYSCTL (to set the deep sleep level of STOP, STANDBY or SHUTDOWN)
3. SLEEPDEEP policy bit in the SCR local CPU register (to select whether a WFI instruction triggers SLEEP mode or STOP/STANDBY/SHUTDOWN mode)
4. Use of the Arm® WFI (wait for interrupt) CPU instruction (to enter the configured SLEEP/STOP/STANDBY/SHUTDOWN state)

Before entering an operating mode where the CPU is disabled, make sure that the appropriate peripheral that can wake the CPU from sleep has been configured to generate a CPU interrupt on the desired event.

For a detailed description of the behavior of each operating mode, see the associated operating mode section.

Policy Bit Configuration

Table 3-3 defines how to configure the relevant policy bits for each operating mode. All values are indicated in binary format. A dash (-) indicates that the particular policy bit is a don't care for the specified operating mode.

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Table 3-3. Operating Mode Policy Bit Configuration

Operating Mode Policy Control		RUN	SLEEP (1)	STOP	STANDBY		SHUTDOWN
Register	Bit	RUN0	SLEEP0	STOP0	STANDBY0	STANDBY1	
MCLKCFG	STOPCLKSTBY	-	-	-	0	1	1
PMODECFG	DSLEEP	-	-	00	01	01	10
SCR	SLEEPDEEP	0	0	1	1	1	1

(1) SLEEP mode behavior is always identical to RUN mode, except with the CPUCLK disabled. As such, the SLEEP behavior is determined by the configuration of RUN mode.

Entering SLEEP Mode

Entering **SLEEP** mode disables the CPU, but otherwise maintains the same configuration as **RUN**. To enter **SLEEP** mode:

1. Configure the CPU for SLEEP by clearing the SLEEPDEEP bit in the local SCR register.
2. Enter selected mode by executing the WFI (wait for interrupt) CPU instruction.

Entering STOP or STANDBY Modes

To enter **STOP** or **STANDBY** mode:

1. Configure the PMODECFG register in SYSCTL to 0b00 (STOP) or 0b01 (STANDBY).
2. Configure the CPU for DEEP SLEEP by setting the SLEEPDEEP bit in the local SCR register.
3. Enter selected mode by executing a WFI (wait for interrupt) CPU instruction.

Entering SHUTDOWN Mode

To enter **SHUTDOWN** mode:

1. Configure the PMODECFG register in SYSCTL to 0b10 (SHUTDOWN).
2. Configure the CPU for DEEP SLEEP by setting the SLEEPDEEP bit in the local SCR register.
3. Enter selected mode by executing a WFI (wait for interrupt) CPU instruction.

3.1.3 Peripheral Power & Reset

Table 3-4. PWREN, RSTCTL, STAT Functionality Per Peripheral

Peripheral	Register Set Containing PWREN, RSTCTL, and STAT	Peripheral Power Functionality	Peripheral Reset Control Functionality	Peripheral Power & Reset Status Functionality
NPU	SYSCTL_REGS	TINIE field in PWREN_SYSPERIPH register	RESETASSERT_TINIE field in RSTCTL_ASSERT_SYSPERIPH register & RESETSTKYCLR_TINIE field in RSTCTL_CLEAR_SYSPERIPH	TINIE field in STAT_SYSPERIPH register
AES	AES_REGS	PWREN register	RSTCTL register	STAT register

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Table 3-4. PWREN, RSTCTL, STAT Functionality Per Peripheral (continued)

Peripheral	Register Set Containing PWREN, RSTCTL, and STAT	Peripheral Power Functionality	Peripheral Reset Control Functionality	Peripheral Power & Reset Status Functionality
Keystore	N/A	N/A	N/A	N/A
CRC	CRCP_REGS	PWREN register	RSTCTL register	STAT register
DMA	DMA_REGS	PWREN register	RSTCTL register	STAT register
EAM	N/A	N/A	N/A	N/A
GPIO	GPIO_REGS	PWREN register	RSTCTL register	STAT register
GSC	N/A	N/A	N/A	N/A
IOMUX	N/A	N/A	N/A	N/A
TIMx	TIMG4_REGS, TIMG12_REGS	PWREN register	RSTCTL register	STAT register
WWDT	WWDT_REGS	PWREN register	RSTCTL register	STAT register
XBAR	SYSCTL_REGS	XBAR field in PWREN_MCPERIPH register	RESETASSERT_XBAR field in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_XBAR field in RSTCTL_CLEAR_MCPERIPH	XBAR field in STAT_MCPERIPH register
ADC	ADC_LITE_REGS	PWREN register	RSTCTL register	STAT register
CMPSS	SYSCTL_REGS	CMPSSx fields in PWREN_MCPERIPH register	RESETASSERT_CMPSSx field in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_CMPSSx field in RSTCTL_CLEAR_MCPERIPH	CMPSSx fields in STAT_MCPERIPH register
PGA	SYSCTL_REGS	PGAx fields in PWREN_SYSPERIPH register	RESETASSERT_PGAx fields in RSTCTL_ASSERT_SYSPERIPH register & RESETSTKYCLR_PGAx fields in RSTCTL_CLEAR_SYSPERIPH	PGAx fields in STAT_SYSPERIPH register
ECAP	SYSCTL_REGS	ECAPx fields in PWREN_MCPERIPH register	RESETASSERT_ECAPx fields in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_ECAPx fields in RSTCTL_CLEAR_MCPERIPH	ECAPx fields in STAT_MCPERIPH register

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Table 3-4. PWREN, RSTCTL, STAT Functionality Per Peripheral (continued)

Peripheral	Register Set Containing PWREN, RSTCTL, and STAT	Peripheral Power Functionality	Peripheral Reset Control Functionality	Peripheral Power & Reset Status Functionality
EQEP	SYSCTL_REGS	EQEPx fields in PWREN_MCPERIPH register	RESETASSERT_ECAPx fields in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_ECAPx fields in RSTCTL_CLEAR_MCPERIPH	EQEPx fields in STAT_MCPERIPH register
EPWM	SYSCTL_REGS	ETPWMx fields in PWREN_MCPERIPH register	RESETASSERT_ETPWMx fields in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_ETPWMx fields in RSTCTL_CLEAR_MCPERIPH	ETPWMx fields in STAT_MCPERIPH register
MCPWM	SYSCTL_REGS	PWMx fields in PWREN_MCPERIPH register	RESETASSERT_PWMx fields in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_PWMx fields in RSTCTL_CLEAR_MCPERIPH	PWMx fields in STAT_MCPERIPH register
SDFM	SYSCTL_REGS	SDFM0 field in PWREN_MCPERIPH register	RESETASSERT_SDFM0 field in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_SDFM0 field in RSTCTL_CLEAR_MCPERIPH	SDFM0 field in STAT_MCPERIPH register
EtherCAT Core	SYSCTL_REGS	ETHERCAT_CORE0 field in PWREN_MCPERIPH register	RESETASSERT_ETHERCAT_CORE0 field in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_ETHERCAT_CORE0 field in RSTCTL_CLEAR_MCPERIPH	ETHERCAT_CORE0 field in STAT_MCPERIPH register

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Table 3-4. PWREN, RSTCTL, STAT Functionality Per Peripheral (continued)

Peripheral	Register Set Containing PWREN, RSTCTL, and STAT	Peripheral Power Functionality	Peripheral Reset Control Functionality	Peripheral Power & Reset Status Functionality
EtherCAT ESC	SYSCTL_REGS	ETHERCAT_SS0 field in PWREN_SYSPERIPH register	RESETASSERT_ETHERCAT_SS0 field in RSTCTL_ASSERT_SYSPERIPH register & RESETSTKYCLR_ETHERCAT_SS0 field in RSTCTL_CLEAR_SYSPERIPH	ETHERCAT_SS0 field in STAT_SYSPERIPH register
FSI	SYSCTL_REGS	FSI_RX0 and FSI_TX0 fields in PWREN_MCPERIPH register	RESETASSERT_FSI_RX0 and RESETASSERT_FSI_TX0 fields in RSTCTL_ASSERT_MCPERIPH register & RESETSTKYCLR_FSI_RX0 and RESETSTKYCLR_FSI_TX0 fields in RSTCTL_CLEAR_MCPERIPH	FSI_RX0 and FSI_TX0 fields in STAT_MCPERIPH register
MCAN	MCAN_REGS	PWREN register	RSTCTL register	STAT register
UNICOMM	UNICOMM_REGS	PWREN register	RSTCTL register	STAT register
DEBUGSS	N/A	N/A	N/A	N/A

3.2 Quick Start Reference

The AM13E232x System Controller is designed to provide simple, easy-to-use, power management, clocking, and reset management functionality. This section describes the basic operating principles of the SYSCTL as well as tips and tricks for taking the default configuration out of reset and optimizing it for particular applications.

3.2.1 Increasing MCLK Precision

If an application requires high clocking accuracy for high-frequency peripherals, the best accuracy is achieved by using an external high-frequency crystal with the XTAL and sourcing the MCLK tree directly from HFCLK. By sourcing the MCLK directly from HFCLK, the bus clock to all peripherals in PD1 and PD0 will be the HFCLK. Crystal frequencies in the 10-25 MHz range are supported by the XTAL.

If precision clocking is needed for the CAN-FD controller and high CPU performance (high MCLK) is also required, it is also possible to source the CAN-FD controller (CANCLK) from HFCLK directly, asynchronous to MCLK, while running MCLK at maximum frequency using the PLL for the best computing performance.

3.2.2 Configuring MCLK for Maximum Speed

The best CPU compute performance is obtained by using the SYSPLL to generate the maximum clock frequency from either the SYSOSC reference or XTAL.

Running MCLK at the maximum clock frequency also provides the best possible timer resolution for TIMG, MCPWM, ECAP, and EQEP peripherals and the best throughput for ADCs in the PD1 domain.

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3.2.3 High Speed Clock (SYSPLL, HFCLK) Handling in Low-Power Modes

The SYSPLL and HFCLK (XTAL, HFCLK_IN) high speed clock sources are not supported in the STOP and STANDBY operating modes. When a high-speed clock source (SYSPLL, HFCLK) is enabled, entering either the STOP mode or STANDBY mode will cause SYSCTL to automatically disable the SYSPLL and/or HFCLK before entering STOP or STANDBY mode. Upon exit from STOP or STANDBY mode to RUN mode, SYSCTL will automatically re-enable the SYSPLL and/or HFCLK if they were previously enabled before entering the low-power mode.

Before entering STOP or STANDBY for the first time after enabling the SYSPLL or HFCLK, and after waking up from STOP or STANDBY mode, application software must wait to enter STOP or STANDBY mode until any previously enabled high speed clock sources have completed startup. Application software must check the following before entering STOP or STANDBY mode:

- If the **SYSPLL was enabled,** then application software must wait for the SYSPLL to complete startup. When the SYSPLL startup is complete, the SYSPLLGOOD bit will be set in the CLKSTATUS register in SYSCTL. If the SYSPLL fails to start, the SYSPLLOFF bit will be set instead. The SYSPLLOFF bit indicates that the SYSPLL was dead at startup or was not previously enabled. Ensure that either SYSPLLGOOD or SYSPLLOFF is set before attempting to enter STOP or STANDBY.
- If the **HFCLK was enabled,** then application software must wait for the HFCLK to complete startup. When the HFCLK startup is complete, the HFCLKGOOD bit will be set in the CLKSTATUS register in SYSCTL. If the HFCLK fails to start, the HFCLKOFF bit will be set instead. The HFCLKOFF bit indicates that the HFCLK was dead at startup or was not previously enabled. Ensure that either HFCLKGOOD or HFCLKOFF is set before attempting to enter STOP or STANDBY.

In the event that the MCLK was configured to be sourced from HSCLK before entry to STOP or STANDBY, upon exit from STOP or STANDBY the MCLK will be sourced from SYSOSC initially and the CPU will be released to begin executing code at the SYSOSC frequency. SYSCTL will automatically restore the MCLK configuration to the previously selected high-speed clock when the high-speed clock has started and is ready for use. When MCLK switches back to the high-speed clock, SYSCTL will generate an HSCLK GOOD interrupt to alert the application that MCLK is again running from the high-speed clock.

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3.3 Power Management Unit (PMU)

The Power Management Unit (PMU) generates the regulated core supplies for the device and provides supervision of the external supply. It also contains a bandgap voltage reference used by the PMU and other analog peripherals. Refer to the device specific datasheet for the supported PMU features.

Key PMU features include:

- Support for the device across the device operating supply range
- **Main LDO:** Low-dropout linear voltage regulator to generate the internal core logic supply, with multiple operating modes for reducing device current in low-power modes (managed automatically by SYSCTL)
  - Also referred to as the **Core Regulator** or **Core LDO**
- **STOP LDO:** Low-dropout linear voltage regulator to power both PD0 active logic and PD1 retention logic/ memory in STOP/STANDBY modes
- Power-on reset (POR) for VDD supply
- Brownout reset (BOR) for VDD supply
- Bandgap voltage reference supporting the BOR, core regulator, and analog peripherals
- Analog mux VBOOST unit for increasing analog mux performance

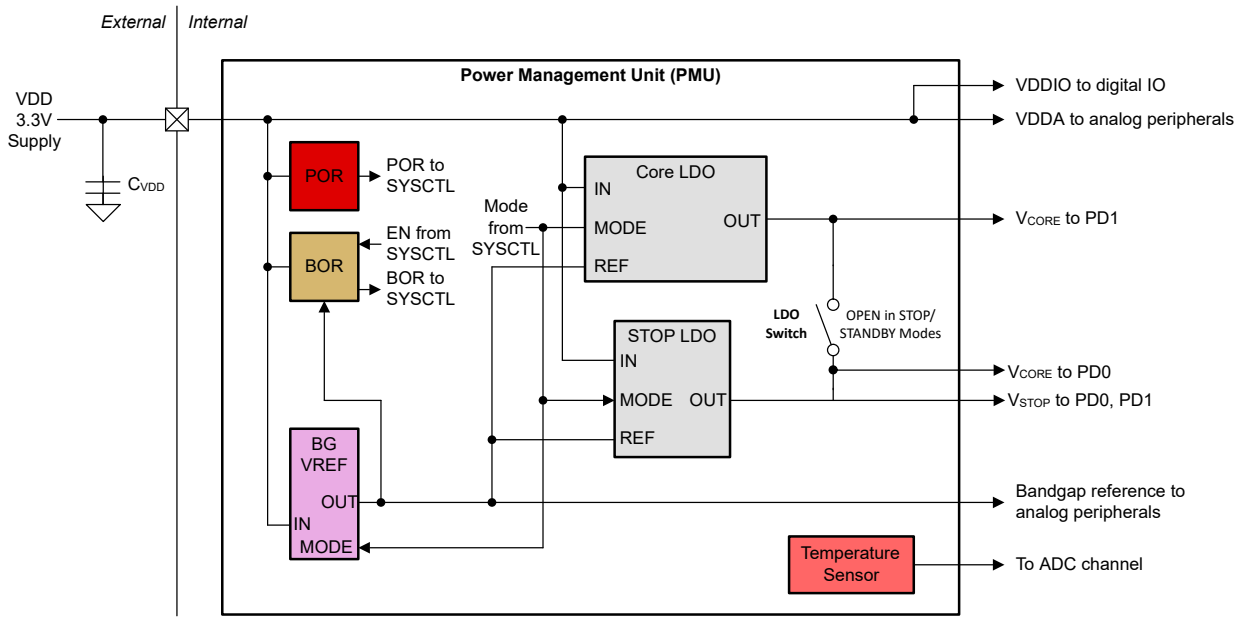


Figure 3-4. PMU Block Diagram

3.3.1 Power Supply

Power is supplied to the device through the VDD/VSS and VDDA/VSSA connections. A decoupling capacitor (C_{VDD}/C_{VDDA}) must be placed across all VDD/VSS and VDDA/VSSA supply pairs. See the device-specific data sheet for the correct value and tolerance of the decoupling capacitors.

Note

VDD and VDDA are to be connected at the board level. There is no separate supply monitor for VDDA, and it is expected that the same power supply being used for VDD is also connected to VDDA.

VDD is used directly to provide the IO supply (VDDIO). VDDA is used directly to provide the analog supply (VDDA).

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3.3.1.1 Main LDO

The PMU uses an on-chip, configurable, low-dropout linear voltage regulator to generate a 1.35V supply rail to power the device core, also referred to as the **core regulator**. The core regulator output (V_{CORE}) supplies power to the core logic, which includes the CPU, digital peripherals and the device memory.

The MAIN LDO is active in RUN and SLEEP modes. In all other power modes (STOP, STANDBY, SHUTDOWN), the regulator is off. SYSCTL automatically configures the regulator for the best power consumption based on the power mode that is currently active.

3.3.1.2 STOP LDO

The PMU uses an on-chip, configurable, low-dropout linear voltage regulator to generate a 1.0V supply rail to power the PD0 active logic and PD1 retention logic domains when the device is in STOP/STANDBY modes.

The STOP LDO is active in all power modes except for SHUTDOWN. In all other power modes (RUN, SLEEP, STOP, and STANDBY) the drive strength of the regulator is configured automatically to support the max load current of each mode. This reduces the quiescent current of the regulator when using low-power modes, improving low power performance. SYSCTL automatically configures the regulator for best power consumption based on the power mode which is currently active.

3.3.1.3 VOSC LDO

The VOSC LDO provides a fixed 1.35V to the SYSOSC, LFOSC and corresponding clock muxes. This LDO is on in all modes except SHUTDOWN.

3.3.2 Supply Supervisors

The PMU provides two supply supervisor circuits:

- A power-on reset (POR) circuit to indicate that the external supply has reached sufficient voltage to start the on-chip bandgap reference and BOR circuit
- A brownout reset (BOR) circuit which verifies that the external supply is maintained at the specified voltage to support correct operation of the device

3.3.2.1 Power-on Reset (POR)

The power-on reset (POR) circuit assures a proper start-up of the device. During cold power-up, the device is held in a POR state until VDD passes the POR+ threshold. When VDD has passed POR+, the POR state is released and the bandgap reference and BOR monitor circuit are started. If VDD drops below the POR- level, then a POR- violation is asserted and the device is again held in a POR reset state.

The POR circuit does not indicate that VDD has reached a level high enough to support correct operation of the device. Rather, it is the first step in the boot process and is used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are then used to determine if the supply has reached a level sufficient to for the device to run correctly.

The POR circuit is active in all power modes including SHUTDOWN and cannot be disabled.

3.3.2.2 Brownout Reset (BOR)

The brownout reset (BOR) supervisor monitors the external supply (VDD) and asserts or deasserts a BOR violation to SYSCTL. The primary responsibility of the BOR circuit is to make sure that the external supply is maintained high enough to enable correct operation of internal circuits, including the core regulator. The BOR threshold reference is derived from the internal bandgap circuit. The threshold is fixed and is always higher than the POR threshold. During cold start, after VDD passes the POR+ threshold, the bandgap reference and BOR circuit are started. The device is then held in a BOR state until VDD passes the BOR+ threshold. When VDD passes BOR+, the BOR supervisor releases the device to continue the boot process, and the PMU is started. A BOR- violation always generates a BOR- violation signal to SYSCTL, generating a BOR level reset. The BOR supervisor is active in RUN, SLEEP, STOP, and STANDBY modes but is disabled automatically in SHUTDOWN mode.

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The BOR threshold level is fixed, and is referred to as BOR2. Refer to the device-specific data sheet for BOR voltage level thresholds.

3.3.2.3 POR and BOR Behavior During Supply Changes

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD that do not pass below the BOR- threshold do not cause a BOR- violation, and the device continues to RUN.

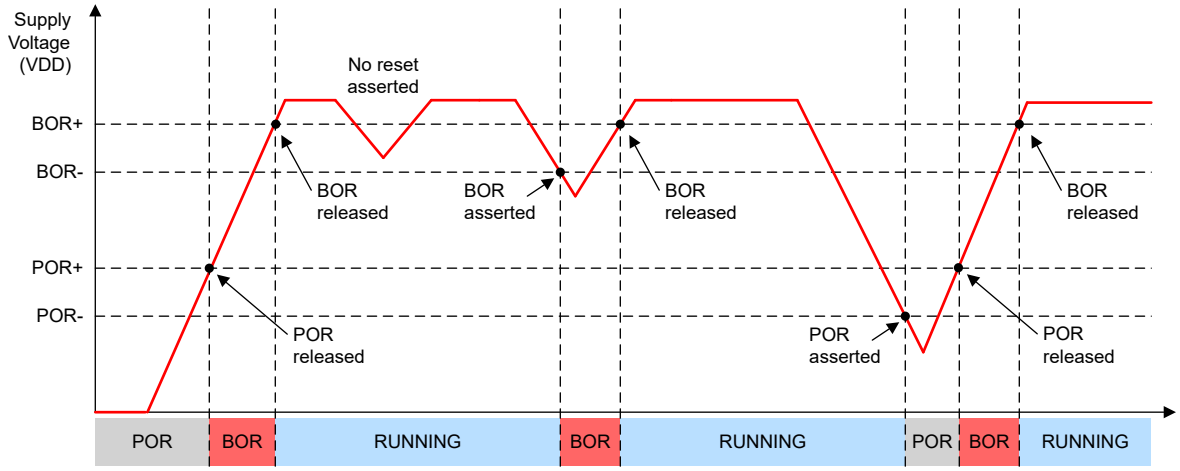


Figure 3-5. POR/BOR vs. Supply Voltage (VDD)

3.3.3 Bandgap Reference

The PMU provides a voltage reference that is stable across temperature and VDD supply voltage and is used by the device for internal functions, including:

- Deriving the brownout reset circuit thresholds
- Setting the output voltage for the core regulator
- Deriving the on-chip VREF levels for on-chip analog peripherals

The bandgap reference is enabled in RUN, SLEEP, STOP modes. This reference operates in a sampled mode in STANDBY to reduce power consumption and is disabled in SHUTDOWN mode. SYSCTL manages the bandgap state automatically; no user configuration is required.

3.3.4 Analog Supplies

The device has the following analog power supply pins for powering analog peripherals and the analog voltage references:

- **VDDA:** 3.3V analog supply used by all modules in ADCCIO (ADC, analog voltage references, CMPSS, internal temperature sensor)
- **VSSA:** Analog ground used by all modules in ADCCIO
- **VREFHI:** ADC0/1/2 reference HIGH input
- **VREFLO:** ADC0/1/2 reference LOW input

On all device packages, physical VREFHI and VREFLO pins are shared by all ADCs. Physical VDDA and VSSA pins supply the ADCs, comparators, PGAs, internal temperature sensor, and analog reference buffer (REFBUF).

3.3.4.1 Analog Reference Circuits

The analog reference circuits are supplied by a single bandgap circuit. The ADC voltage reference input is fixed to the VREFHI pin on the device. There is a single buffer that drives either the internal reference to the VREFHI

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pin or tri-states the reference buffer to high-impedance, which allows an external voltage source to drive the VREFHI pin. For both internal and external reference modes, VREFHI requires a decoupling capacitor, C_{VREF}. The value of C_{VREF} for internal reference mode is defined in the device-specific data sheet. The value of C_{VREF} for external reference mode is dependent on the external reference driver.

In internal reference mode, the ADCREFBUF drives all ADCs. In external reference mode, the VREFHI/VREFLO pads drive the reference. At any given time, **all ADCs** are in internal or external reference mode - i.e. there is no independent configuration of voltage reference for each ADC.

To put the ADCs in internal reference mode, the following condition must be met: {CIO.ANAREFSEL & (ADCEN0 || ADCEN1 || ADCEN2)}. At a register level, the ADC reference mode is selected by setting:

- ANAREFCTL.ANAREFSEL=0 (switch CLOSED) for internal reference mode
- ANAREFCTL.ANAREFSEL=1 (switch OPEN) for external reference mode

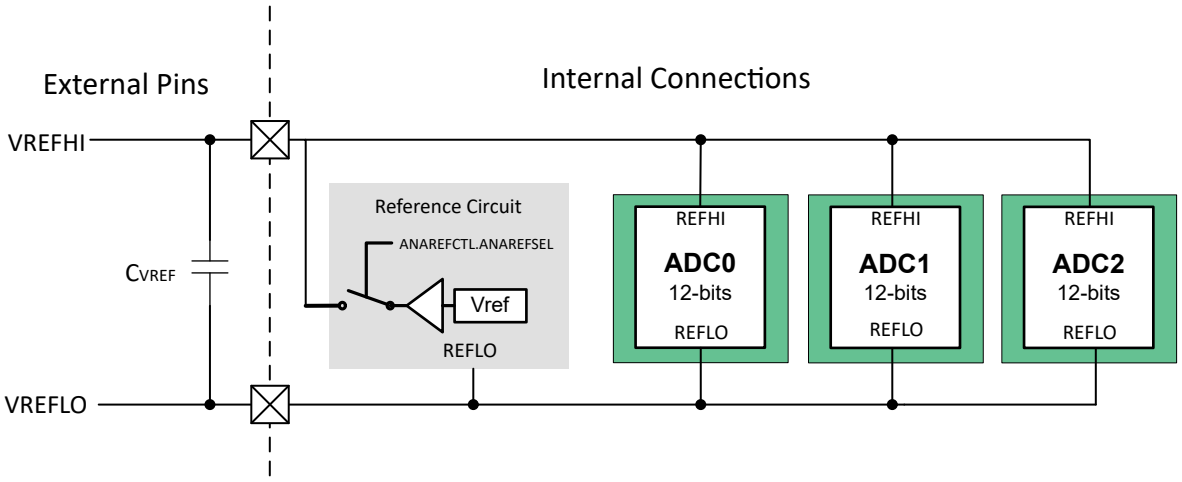


Figure 3-6. VREF to ADC Connections

Note

1. Because VREFHI and VREFLO pins are shared between all ADCs, the control for 2.5V or 3.3V internal reference mode will apply to all ADCs. The same logic applies for external reference mode, i.e. all ADCs will receive the same external voltage reference. For more information on the internal reference modes, refer to *Internal Reference Mode*.
2. The ADCENx corresponds to the ADCCTL1.ADCPWDNZ bit for each ADC
3. When all ADCs are disabled, the ADCREFBUF is disabled and any voltage applied to the VREFHI pin will discharge to VSSA.

For full details on the analog reference configuration, refer to *ADC - Voltage Reference*.

3.3.5 Internal Temperature Sensor

The PMU provides a temperature sensor which can be used to approximate the temperature of the device. The temperature sensor is connected internally to the following ADC mux channels:

Table 3-5. Temperature Sensor Connections

ADC Instance	ADC Mux Channel
ADC0	13

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Table 3-5. Temperature Sensor Connections (continued)

ADC Instance	ADC Mux Channel
ADC2	13

The ADCs listed in the table above are used to perform temperature measurements. The temperature sensor outputs a voltage which has a linear relationship with temperature. The temperature coefficient (TS_C) is the slope of the temperature-voltage relationship (given in mV/C), and is given in the specifications section of the device-specific data sheet.

3.3.6 Peripheral Enable

Most peripherals on the AM13E232x require two user actions to enable the peripheral to be ready for operation.

- Peripheral Write Enable
  - Provided by the peripheral write enable control register (PWREN) with a KEY and ENABLE field.
  - Before any other peripheral registers are configured by software, the peripheral itself must be enabled by writing the ENABLE bit together with the appropriate KEY value to the peripheral's PWREN register.
  - When the PWREN.ENABLE bit is cleared, the peripheral's registers are not accessible for read/write operations.
- Peripheral Function Enable
  - Some peripherals have a functional enable bit specific to the peripheral itself in the corresponding register map to provide access to power or for operation.

Note

Check Section 3.1.3 to see where the PWREN registers for a given peripheral are located on this device.

Note

After setting the ENABLE | KEY bits in the PWREN register to enable a peripheral, wait at least 4 ULPCLK clock cycles before accessing the rest of the peripheral's memory-mapped registers. The 4 cycles allow for the bus isolation signals at the peripheral's bus interface to update.

3.3.6.1 Automatic Peripheral Disable in Low Power Modes

Peripherals in power domain 1 (PD1) will be forced to a disabled state by SYSCTL upon entry into a STOP or STANDBY low-power mode. As such, these peripherals will not be available for use in STOP or STANDBY modes.

Most PD1 peripherals will retain their configuration settings after being automatically disabled, such that re-configuration is not required upon exit from STOP or STANDBY mode.

If a PD1 peripheral was multiplexed to an IO pin (through the IOMUX) in an output configuration, the last valid output state (logic 0 or logic 1) from the peripheral to the IO is latched upon entry to STOP or STANDBY mode. This prevents external circuits from being disturbed by SYSCTL disabling a peripheral during low-power operation. Upon exit from STOP or STANDBY mode, the IO is again connected to the peripheral as the peripheral becomes re-enabled.

3.4 Clock Module (CKM)

The clock module contains the internal and external oscillators, the clock monitors, and the clock selection and control logic. A frequency clock counter is also provided for checking and/or calibrating the frequency of high-speed clocks against either the LFCLK or a reference period/pulse provided on an IO pin (FCC_IN).

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3.4.1 Clock Tree

The following figure shows the top level clocking tree for AM13E232x family devices. This diagram shows the mapping between oscillators (sources) and clocks (destinations), as well as the SYSCTL register bit fields for the selection muxes.

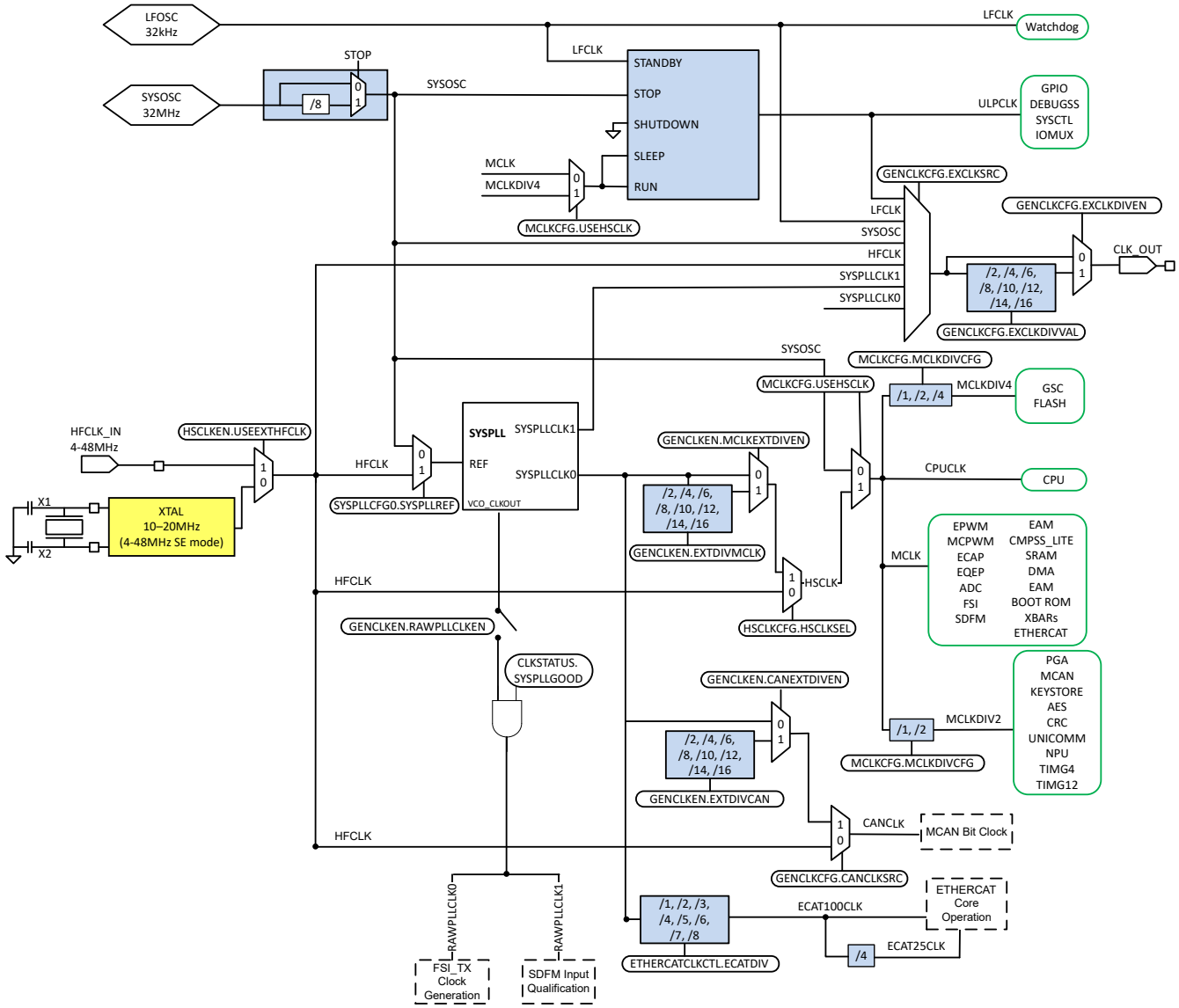


Figure 3-7. AM13E232x Top Level Clocking Diagram

- PD0 Clock Domain
  - RUN/SLEEP - MCLK/4 (62.5MHz)
  - BOOT - SYSOSC (32MHz)
  - STOP - SYSOSC (4MHz)
  - STANDBY - LFCLK (32kHz)
  - SHUTDOWN - DISABLED
- PD1 Clock Domain
  - RUN/SLEEP - MCLK (250MHz)
  - BOOT - SYSOSC (32MHz) for boot, bypass as programmed for other modes

There a few additional items to note about the AM13E232x clocking system:

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1. LFCLK is a fixed-frequency 32kHz clock that can be selected by certain peripherals for ensuring a constant clock rate even when MCLK or ULPCLK changes source or rate. LFCLK is always synchronized to MCLK and ULPCLK.
2. Semi-clock domain peripherals operate on MCLK divided by 2 (MCLKDIV2) clock. The MCLKDIV2 clock domain is synchronous to the MCLK domain and is provided through the semi-divider. This divider allows /2 or bypass with bit 26 of the MCLKCFG register (MCLKDIVCFG).
   a. Programming MCLKCFG[26] = '1' also forces MCLKCFG[24] = '1'. Therefore, writes to MCLKCFG[24] will be ignored if MCLKCFG[26] = '1'.
   b. MCLKDIV2 domain is used and configured when operating from HSCLK and not used when operating from SYSOSC (e.g. out of boot without PLL or out of low power mode).
3. Quarter-clock domain peripherals operate on MCLK divided by 4 (MCLKDIV4) clock. The MCLKDIV2 clock domain is synchronous to the MCLK domain and is provided through the quarter-divider. This divider allows /2, /4, or bypass with bits 24-25 of the MCLKCFG register (MCLKDIVCFG).

Table 3-6. Semi Clock (MCLKDIV2) Divider Select

MCLKCFG[26]	Divider Select
0	/1 (Bypass)
1	/2

Table 3-7. Quarter Clock (MCLKDIV4) Divider Select

MCLKCFG[25]	MCLKCFG[24]	Divider Select
0	0	/1 (Bypass)
0	1	/2
1	0	Reserved
1	1	/4

Valid MCLK Clock Combinations

Each of the MCLKDIV2 and MCLKDIV4 dividers can be configured through MCLKCFG[26:24] with divider selection as shown below. Possible frequency limits corresponding to clock divider values are listed in Table 3-8.

Table 3-8. Valid MCLK Divider Values

Frequency Range	Option	MCLKCFG[26]	MCLKCFG[25]	MCLKCFG[24]	MCLK	MCLK/2	MCLK/4
100MHz - 250MHz	1 (default)	1	1	1	/1	/2	/4
50MHz - 100MHz	1 (default)	0	0	1	/1	/1	/2
	2	0	1	1	/1	/1	/4
	3	1	0	1	/1	/2	/2
	4	1	1	1	/1	/2	/4
< 50MHHz	1 (default)	0	0	0	/1	/1	/1
	2	0	0	1	/1	/1	/2
	3	0	1	1	/1	/1	/4
	4	1	0	1	/1	/2	/2
	5	1	1	1	/1	/2	/4

3.4.2 Oscillators

Several internal and external oscillators are provided for generating low to high frequency clocks for use by the system. The CKM contains all the oscillators in the device and uses them to generate the system clocks. See the device-specific data sheet for whether external oscillators are available.

Internal Oscillators

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- LFOSC: low frequency oscillator (32kHz typical frequency)
- SYSOSC: system oscillator (32MHz frequency)
- SYSPLL: system PLL (phase-locked loop) with programmable frequency (optional)

External Oscillators

- XTAL: crystal oscillator (10MHz - 20MHz frequency range)

In addition to XTAL, a high frequency digital clock input (HFCLK_IN) with a range of 4MHz - 48MHz can be provided to support cases where the XTAL is not used and a direct digital clock is supplied to the device. Note that XTAL also supports a single-ended differential mode.

3.4.2.1 Internal Low-Frequency Oscillator (LFOSC)

The low-frequency oscillator (LFOSC) is an on-chip low power oscillator which is factory trimmed to a frequency of 32.768kHz, providing a stable low frequency clock source.

LFOSC can provide higher accuracy when used over a reduced temperature range. See the device-specific data sheet for details.

The LFOSC is active by default after a BOOTRST, sourcing the LFCLK. The LFOSC startup monitor sets the LFOSCGOOD bit in the CLKSTATUS register when LFOSC is ready.

3.4.2.2 Internal System Oscillator (SYSOSC)

The system oscillator (SYSOSC) is an on-chip, accurate high frequency clock source (32MHz factory-trimmed). The SYSOSC provides a flexible high-speed clock source to the system in cases where the crystal oscillator (XTAL) is either not present or not used, or where fast wake-up from a low-power mode is required.

Key features of the SYSOSC include:

- High accuracy when using optional frequency correction loop (FCL) and reference resistor
  - The frequency correction loop supports correction through an internal resistor
- Fast start-up time from a low power state
- Capable of switching from base frequency to low frequency, or low frequency to base frequency, in one clock cycle with no functional interruption (gear shift)
  - Glitch-less divider and phase-aligned transition to minimize disturbance to peripherals
  - Fast settling to specified accuracy
  - SYSCTL can initiate seamless gear shift frequency switch in STOP mode with user-configurable FCL enablement to reduce SYSOSC current
- Two frequency options: 32MHz supporting RUN/SLEEP power modes and 4MHz in STOP mode
  - While in 32MHz mode, a divider giving a fixed 4MHz output can be multiplexed to when the mode switches

The SYSOSC is active at the device's base frequency (32MHz) by default after a brownout reset, sourcing MCLK.

3.4.2.2.1 SYSOSC Frequency

SYSOSC is factory trimmed for operation at the base frequency of 32MHz, with the option to divide down to 4MHz in STOP mode. The default frequency of operation is the base frequency of 32MHz. In STOP mode, the MCLK (and the ULPCLK) tree run from SYSOSC with a 4MHz rate.

3.4.2.2.2 SYSOSC Frequency Correction Loop

The SYSOSC frequency accuracy can be improved through the use of the Frequency Correction Loop (FCL) feature. The FCL circuit uses an internal resistor to stabilize the SYSOSC frequency by providing a precise reference current for the SYSOSC. The overall frequency accuracy which is achievable depends on the operating temperature range together with the tolerance and temperature drift of the selected reference resistor.

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3.4.2.2.2.1 SYSOSC FCL in Internal Resistor Mode

This section describes the procedure for selecting the internal resistor mode through the device SYSCTL registers. Enabling FCL in internal resistor mode can be beneficial to the user's application which require improved SYSOSC performance while not adding cost to the system for an external resistor.

Enabling FCL with Internal Resistor

To increase the SYSOSC accuracy with FCL, follow this procedure:

1. Enable FCL mode by setting the SETUSEFCL bit in the SYSOSCFCLCTL register.
2. When the FCL mode is enabled, software cannot disable the mode. A BOOTRST is required before a change to the FCL mode.

3.4.2.2.3 Disabling SYSOSC

It is not possible to disable SYSOSC when using a different high frequency clock to source MCLK (such as HFCLK or the PLL). This is due to SYSOSC being used by SYSCTL logic when MCLK is sourced from HFCLK or the PLL.

SYSOSC is always disabled automatically in STANDBY and SHUTDOWN modes. The DISABLE bit in the SYSOSCCFG register displays the status of SYSOSC enable/disable policy.

3.4.2.3 System Phase-Locked Loop (SYSPLL)

The system phase locked loop (SYSPLL) takes an input reference clock SYSPLLREF and scales the input frequency to produce user-specified high frequency clocks (SYSPLLCLK0 and SYSPLLCLK1) for use by the device. Specifically, the SYSPLL clock outputs can be used as sources to MCLK, CANCLK, and ECAT25CLK/ ECAT100CLK. Figure 3-8 shows the block diagram of the SYSPLL. The relation between SYSPLLCLKx and SYSPLLREFx is given by the below formula.

$$f_{SYSPLLCLKx} = \frac{f_{SYSPLLREF} \times (QDIV)}{(PDIV) \times (RDIVCLKx)} \quad (1)$$

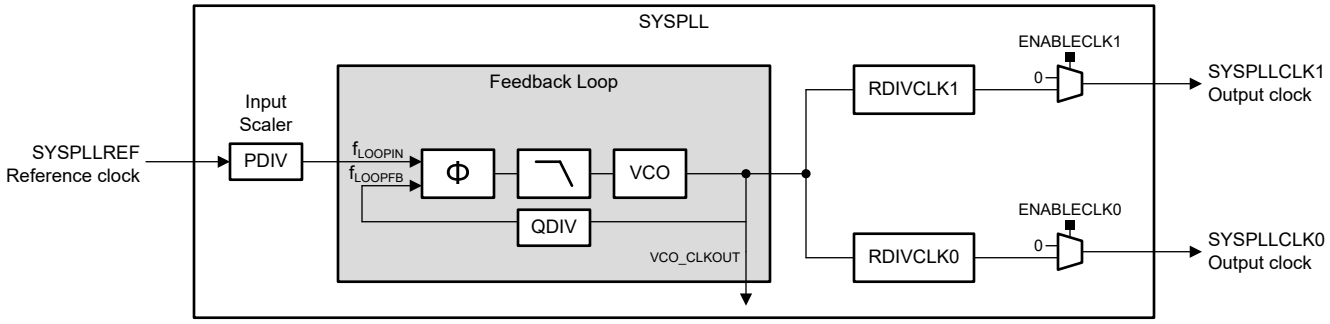


Figure 3-8. SYSPLL Diagram

3.4.2.3.1 Configuring SYSPLL Output Frequencies

The SYSPLL accepts an input reference clock from 4-48MHz. The available reference clocks include SYSOSC and HFCLK. The predivider PDIV scales the selected input reference clock ahead of the PLL feedback loop. PDIV can be selected as /1, /2, /4, or /8 by programming 0x0 to 0x3, respectively, into the PDIV field in the SYSPLLCFG1 register.

The effective divider can be calculated from the PDIV register setting as shown in Equation 2.

$$SYSPLLREF_{DIV} = 2^{PDIV} \quad (2)$$

The PLL feedback loop sets the Voltage Controlled Oscillator (VCO) output equal to the divided input reference clock f_{LOOPIN} multiplied by the QDIV feedback divider. The QDIV divider is an integer divider with a valid range of /2 to /127. The desired QDIV divider is selected by programming 0x01 to 0x7E for /2 to /127, respectively, into

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the QDIV field of the SYSPLLCFG1 register. SYSPLLCFG1.QDIV=0x00 is an invalid configuration. The effective feedback divider can be calculated from the QDIV register setting as shown in Equation 3.

$$SYSPLLFB_{DIV} = QDIV + 1 \quad (3)$$

The output frequency of the VCO f_{VCO} is given in Equation 4.

$$f_{VCO} = f_{SYSPLLREF} \times SYSPLLFB_{DIV} / SYSPLLREF_{DIV} \quad (4)$$

The VCO output sources two separate SYSPLL outputs (SYSPLLCLK0 and SYSPLLCLK1). Each output has its own divider unit to enable generation of up to 2 different output frequencies for use by different modules in the device.

For SYSPLLCLK1 and SYSPLLCLK0, the output dividers can be set from /2 to /32 in steps of 2. To set the SYSPLLCLK0 or SYSPLLCLK1 output divider, program 0x0-0xF for /2 to /32, respectively, into the corresponding RDIVCLKx field in the SYSPLLCFG0 register. Equation 5 shows how to compute the effective SYSPLLCLK0 divider based on a given RDIVCLK0 setting, and Equation 6 shows how to compute the effective SYSPLLCLK1 divider based on a given RDIVCLK1 setting.

$$SYSPLLCLK0_{DIV} = 2 \times (RDIVCLK0 + 1) \quad (5)$$

$$SYSPLLCLK1_{DIV} = 2 \times (RDIVCLK1 + 1) \quad (6)$$

The SYSPLL output clock frequencies are thus set by the combination of f_{VCO} and the respective dividers:

$$f_{SYSPLLCLK0} = f_{VCO} / SYSPLLCLK0_{DIV} \quad (7)$$

$$f_{SYSPLLCLK1} = f_{VCO} / SYSPLLCLK1_{DIV} \quad (8)$$

Enabling and Disabling the SYSPLL

After configuration, enable the SYSPLL by setting the SYSPLLEN bit in the HSCLKEN register. Before enabling the SYSPLL, make sure that the SYSPLL is in a disabled state by verifying that the SYSPLLOFF bit in the CLKSTATUS register is set. After the SYSPLL is enabled, application software must not disable it until the SYSPLLGOOD bit or SYSPLLOFF bit is set in the CLKSTATUS register, indicating that the SYSPLL transitioned to a stable active state or a stable dead state. When the SYSPLL is enabled, the SYSPLL reference clock selection must not be changed.

Please refer to SYSPLL Usage Example (for CAN protocol) for details on how to configure and lock the SYSPLL.

Note

SYSOSC must be enabled and running at base frequency when the SYSPLL is enabled, even if HFCLK is used as the SYSPLL reference clock.

SYSPLL Usage Example (for CAN protocol)

To illustrate the above relationships, take as an example the following requirements:

- The high-frequency external clock (HFCLK) is used as the SYSPLL reference (operating at 20MHz in this example)
- The SYSPLL must be configured with an output frequency of 200MHz to source MCLK and CANCLK at 40MHz.

To achieve this, the VCO can be configured for 400MHz through the use of PDIV and QDIV. Then, SYSPLLCLK0 can feed CANCLK and MCLK with an output divider of /2. Lastly, the external output divider EXTDIVCAN can be used to source CANCLK at 40MHz.

The steps below describe how to configure the CKM to use SYSPLL in this way:

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1. Verify that the SYSPLL is disabled (SYSPLLOFF is set in CLKSTATUS)
2. Make sure that SYSOSC is running at base frequency (32MHz); this is a requirement for SYSPLL operation even though HFCLK is used as the SYSPLL reference clock instead of SYSOSC
3. Set HFCLK as the SYSPLL reference (make sure that the SYSPLLREF bit in the SYSPLLCFG0 register is cleared; this is the default state after reset)
4. Select a predivider PDIV to /2 (set SYSPLLCFG1.PDIV to 0x01), setting f_{LOOPIN} to 10MHz (20 divided by 2)
5. Load the PLL parameters into SYSPLLPARAM0 and SYSPLLPARAM1 to support f_{LOOPIN} of 10MHz
6. Set the feedback divider QDIV to 40 (set SYSPLLCFG1.QDIV to 0x27), giving f_{VCO}=400MHz (10MHz multiplied by 40)
7. Set the SYSPLL output dividers for SYSPLLCLK0 to /2 (set SYSPLLCFG0.RDIVCLK0 to 0x0) to get 200MHz at SYSPLLCLK0
8. Enable SYSPLLCLK0 outputs by setting the ENABLECLK0 bit in the SYSPLLCFG0 register
9. With HFCLK running at 20MHz frequency, enable the SYSPLL by setting SYSPLLEN in the HSCLKEN register
10. Wait for the SYSPLLGOOD indication by testing SYSPLLGOOD in the CLKSTATUS register
11. Select the SYSPLL as the HSCLK source by ensuring that the HSCLKSEL bit is cleared in the HSCLKCFG register (this is the default state)
12. Select the high-speed clock (HSCLK) as the source for MCLK by setting the USEHSCLK bit in the MCLKCFG register. This will switch MCLK from SYSOSC to HSCLK. MCLK is now running from SYSPLLCLK0 at 200MHz.
13. Enable the CANCLK divider (EXTDIVCAN) by setting GENCLKEN.CANEXTDIVEN and configure GENCLKEN.EXTDIVCAN to divide by 5 before sourcing CANCLK
14. Set the CANCLKSRC bit in the GENCLKCFG register to 0x01, applying SYSPLLCLK as CANCLK source

The SYSPLL divider values used in this example are summarized below for reference.

Table 3-9. SYSPLL Divider Example Settings

Parameter	Register	Bit Field	Bit Field Value	Actual Divider
Input reference clock divider	SYSPLLCFG1	PDIV	0x1	/2
VCO feedback loop divider	SYSPLLCFG1	QDIV	0x27	/40
Output clock 0 divider	SYSPLLCFG0	RDIVCLK0	0x0	/2
CAN clock divider	GENCLKEN	EXTDIVCAN	0x4	/5

Tuning Guidelines

In cases where there are multiple combinations of PDIV, QDIV, and RDIVCLKx that provide the desired output frequencies, consider these tuning guidelines to determine the best possible values for an application:

- Lower VCO frequencies (f_{VCO}) result in lower power consumption. Refer to the device data sheet for the allowable range of f_{VCO}.
- Higher feedback loop input frequencies (f_{LOOPIN}) have faster startup. For example, if an 200MHz output frequency is desired with f_{VCO}=200MHz, f_{VCO} = 200MHz can be derived from a SYSPLLREF clock 32MHz by setting PDIV to /8 and QDIV to /50. However, this gives slower startup because f_{LOOPIN} is <8MHz. The same result can be achieved by setting PDIV to /4 and QDIV to /25, but because f_{LOOPIN} is 8MHz in this case (32MHz divided by 4), the Table 3-10 for the higher input range can be used which give faster startup.

3.4.2.3.2 Loading SYSPLL Lookup Parameters

Several tuning parameters must be configured in the SYSPLLPARAM0 and SYSPLLPARAM1 registers before using the SYSPLL. The values are determined by PLL feedback loop input clock frequency (f_{LOOPIN}).

SYSPLL supports four f_{LOOPIN} frequency ranges, given in Table 3-10. Each frequency range has a 64-bit lookup value in the FACTORY flash memory region that must be copied from flash into the SYSPLLPARAM0 and SYSPLLPARAM1 registers in SYSCTL before enabling the SYSPLL.

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Table 3-10. SYSPLL Parameter Lookup

Lookup Address (SYSPLLPARAM0)	Lookup Address (SYSPLLPARAM1)
0x400B0128	0x400B012C

3.4.2.3.3 SYSPLL Startup Time

The PLL startup time depends on the PLL feedback loop input frequency f_{LOOPIN} and if the PLL is starting after previously running (for example, exiting a low-power mode) or starting for the first time after device boot.

Table 3-11 lists an example of how the PLL startup times can be affected by the loop input frequency f_{LOOPIN}. Note that f_{LOOPIN} is determined by the SYSPLLREF and user-configured PDIV and QDIV.

Note

These values are used as a relative example only. For specific device performance, please refer to the device datasheet.

Table 3-11. SYSPLL Startup Times (example)

f_{LOOPIN}	SYSPLL Startup Time (µs)	SYSPLL Startup Time on Exit From Low-Power Mode (µs)
32MHz ≤ FREQ	5	3
16MHz ≤ FREQ < 32MHz	15	12
8MHz ≤ FREQ < 16MHz	25	20
4MHz ≤ FREQ < 8MHz	40	35

3.4.2.4 External Crystal Oscillator (XTAL)

The external crystal oscillator (XTAL) can be used with standard crystals and resonators in the 10-25MHz range to generate a stable reference clock for the system. The XTAL can also operate in single-ended mode, with an external clock in the 4-48MHz range connected to the X1 pin. The XTAL can be used to clock the primary device clock tree (MCLK) directly, or it can be used as a precision reference to the on-chip PLL where higher frequencies can be generated.

To use the XTAL, a crystal or resonator must be populated between the X1 and X2 pins. Loading capacitors must be placed on both pins to circuit ground (VSS). The crystal load capacitors must be sized according to the specifications of the crystal being used. The IOMUX must be configured to enable XTAL functionality on the X1 and X2 pins.

A programmable XTAL startup time is provided with 64µs resolution. Program an appropriate startup time based on the desired crystal or resonator specifications into the XTALTIME field in the HFCLKCLKCFG register in SYSCTL before starting the XTAL.

Once configured properly, the XTAL is started by clearing the OSCOFF bit in the XTALCR register in SYSCTL. When the oscillator has started successfully, the HFCLK startup monitor will assert the HFCLKGOOD bit in the CLKSTATUS register in SYSCTL.

Note

SYSOSC must be enabled at base frequency when the XTAL is enabled.

After clearing XTALCR.OSCOFF to enable the XTAL, application software must verify that either an HFCLKGOOD indication or an HFCLKOFF (off/dead) indication in the CLKSTATUS register was asserted by hardware. When disabling the XTAL, the XTAL must not be re-enabled again until the HFCLKOFF bit in the CLKSTATUS register is set by hardware.

To use XTAL as the PLL reference after receiving an HFCLKGOOD status, set the SYSPLLREF bit in the SYSPLLCFG0 register in SYSCTL. If XTAL is selected as a reference for the SYSPLL and the SYSPLL is enabled, then the SYSPLL must be disabled and the SYSPLLOFF bit in the CLKSTATUS register must be set before the XTAL can be disabled.

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To use the XTAL directly as the MCLK source after receiving an HFCLKGOOD status, first set the HSCLKSEL bit in the HSCLKCFG register to select HFCLK as the high-speed clock source (rather than the system PLL output). Then, set the USEHSCLK bit in the MCLKCFG register to select the high-speed clock source as the MCLK source. Once USEHSCLK is set, HSCLKCFG must not change and the XTAL must not be disabled until the MCLK source is switched back to SYSOSC by clearing USEHSCLK and verifying that the HSCLKMUX bit in CLKSTATUS is cleared by hardware.

Crystal Oscillator Control and Configuration

External clock sources use the X1/X2 pins, which can either be used as an oscillator or as GPIOs. X1 is assigned to GPIO80 and X2 is assigned to GPIO81. These mode settings can be controlled through the XTALCR register. After power-up, the X1 and X2 pin functionality can be enabled by following the procedure in Using an External Crystal or Resonator.

Three types of external clock sources are supported:

- A single-ended 3.3V external clock. The clock signal must be connected to X1, with X2 available as a GPIO.
- An external crystal. The crystal must be connected across X1 and X2 with the load capacitors connected to VSS.
- An external resonator. The resonator must be connected across X1 and X2 with the ground connected to VSS.

Note

To ensure correct switching between single-ended and double-ended modes, the XTAL has to be powered down in between. That is, XTALCR.SE = 0 and XTALCR.OSCOFF = 1 has to be used as a transitory configuration state.

Table 3-12. XTAL Operating Modes

XTALCR.OSCOFF	XTALCR.SE	Operating Mode	X1 using GPIO80?	X2 using GPIO81?
0	0	Crystal Mode: Quartz crystal connected to X1/X2	No	No
0	1	Single-Ended Mode: External clock on X1	No	Yes
1	0	Oscillator off	Yes	Yes
1	1	Single-Ended Mode: External clock on X1	No	Yes

Using an External Crystal or Resonator

The X1 and X2 pins double as GPIO80 and GPIO81 respectively. At power-up, these pins are in GPIO mode and the on-chip crystal oscillator is powered off. The following procedure can be used to switch the pins to X1 and X2 mode and enable the oscillator:

1. Clear the XTALCR.OSCOFF bit
2. Wait for the crystal to power up (5-10ms is the typical wait time but this depends on the crystal that is being used)
3. Clear the X1 counter by writing a 1 to X1CNT.CLR and keep clearing until the X1 counter value in the X1CNT register is no longer saturated 2047 (0x7FF)
4. Wait for the X1 counter value in the X1CNT register to reach 2047 (0x7FF)
5. Repeat steps (3) and (4) three additional times
6. Select XTAL as the HFCLK source by writing a 0 to HSCLKEN.USEEXTHFCLK

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Using an External Oscillator

The X1 and X2 pins double as GPIO80 and GPIO81 respectively. At power-up, these pins are in GPIO mode and the on-chip crystal oscillator is powered off. The following procedure can be used to switch the pins to X1 and X2 mode and enable the oscillator:

1. Clear the XTALCR.OSCOFF bit
2. Set the XTALCR.SE bit to enable single-ended mode
3. Clear the X1 counter by writing a 1 to X1CNT.CLR and keep clearing until the X1 counter value in the X1CNT register is no longer saturated 2047 (0x7FF)
4. Wait for the X1 counter value in the X1CNT register to reach 2047 (0x7FF)
5. Repeat steps (3) and (4) three additional times
6. Select XTAL as the HFCLK source by writing a 0 to HSCLKEN.USEEXTHFCLK

3.4.2.5 HFCLK_IN (Digital clock)

It is possible to bypass the XTAL circuit and bring in an external 4-48MHz digital clock signal into the device to use as the HFCLK source instead of XTAL. To configure HFCLK to use a digital clock input, first configure the IOMUX to enable the HFCLK_IN function on the appropriate pin. When IOMUX is configured correctly and the clock source is outputting a clock to HFCLK_IN, set the USEEXTHFCLK bit in the HSCLKEN register in SYSCTL.

Note

SYSOSC must be enabled at base frequency when the HFCLK_IN is enabled.

The HFCLK_IN can be used as the reference for SYSPLL. The SYSPLL must be off before changing the configuration of the SYSPLL reference clock source. The user can verify that SYSPLL is off by checking the SYSPLLOFF status bit in the CLKSTATUS register. The user must then select HFCLK_IN as the HFCLK source (by setting the USEEXTHFCLK bit in the HSCLKEN register) before setting the SYSPLLREF bit in the SYSPLLCFG0 register in SYSCTL. Finally, the SYSPLL can be enabled by using the SYSPLLEN bit in the HSCLKEN register.

To source MCLK from HFCLK_IN after selecting HFCLK_IN as the HFCLK source, first set the HSCLKSEL bit in the HSCLKCFG register to select HFCLK as the high-speed clock source. Then, set the USEHSCLK bit in the MCLKCFG register to select the high-speed clock source as the MCLK source. Once USEHSCLK is set, HSCLKCFG must not change and the HFCLK_IN must not be disabled until the MCLK source is switched back to SYSOSC by clearing USEHSCLK and verifying that the HSCLKMUX bit in CLKSTATUS was cleared by hardware.

HFCLK_IN is compatible with digital square wave CMOS clock inputs and should have a typical duty cycle of 50%.

Note

HFCLK_IN and XTAL are mutually exclusive and must not be enabled at the same time.

3.4.3 Clocks

The CKM takes oscillator outputs and generates a variety of functional clocks for use by the device. Refer to the device specific datasheet to determine the supported functional clocks.

Clocks

- System Clocks
  - MCLK: Main system clock for PD1 peripherals and PD1 bus
  - CPUCLK: CPU clock, derived from MCLK is available only in RUN mode
  - ULPCLK: Main system clock for PD0 peripherals and PD0 bus, derived from MCLK
  - LFCLK: Fixed 32kHz clock, synchronized to MCLK/ULPCLK
  - HFCLK: High frequency external clock
  - HSCLK: High speed configurable clock for use by MCLK, sourced from SYSPLL or HFCLK

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- Peripheral Specific Clocks
  - CANCLK: CAN-FD module functional clock
  - ECAT25CLK, ECAT100CLK: EtherCAT module functional clocks
  - RAWPLLCLK0: Source for FSI-TX CLK generation
  - RAWPLLCLK1: Source for SDFM module input qualification synchronization
- External Clocks
  - CLK_OUT: External clock output with divider for pushing out a clock to external circuits

All clocks are disabled in SHUTDOWN mode.

3.4.3.1 MCLK (Main Clock) Tree

The MCLK is the main system clock and the root point of synchronization for all synchronized clocks (MCLK, CPUCLK, ULPCLK, and LFCLK). It is typically the highest speed clock in the system and supports operation up to 250MHz across the full temperature range of the device. The MCLK tree is the root source for the CPUCLK (in RUN mode), the PD1 high speed peripheral bus clock (in RUN and SLEEP modes), and the ULPCLK low power bus clock (in RUN, SLEEP, STOP, and STANDBY modes). In addition, the 32kHz LFCLK outputs are synchronized to MCLK.

The MCLK output to PD1 peripherals is enabled in RUN and SLEEP modes, and disabled in all other power modes. While the MCLK output to PD1 is disabled in STOP and STANDBY modes, the MCLK tree is still running to source ULPCLK and to provide synchronization for LFCLK.

The MCLK source is selected with a glitch free clock mux and can be changed dynamically at runtime by user software. It can also be changed automatically by hardware when entering STOP and STANDBY modes or during an asynchronous fast clock request.

The available sources for MCLK include:

- **HSCLK** (high-speed clock) at up to 250MHz which can be sourced by:
  - **SYSPLLCLK0** (used to reach the max MCLK speed of 250MHz)
  - **HFCLK** for applications where the main clock needs to be as accurate as possible
- **SYSOSC** at 32MHz
- **LFCLK** at 32kHz for applications where the entire system, including the CPU, runs at 32kHz with low peak operating current

Note

Set SYSPLLCLK0 as the source of HSCLK before setting HSCLK as the clock source of MCLK, otherwise the device can be in an unpredictable state.

Using MCLK in RUN and SLEEP Mode

After boot, MCLK is sourced from SYSOSC by default. The decision of which oscillator to use to source MCLK is important because MCLK sets both the CPUCLK frequency and the bus clock frequency for PD1 peripherals. As a result, the accuracy and the clock speed of the oscillator selected for MCLK must be appropriate not only for the operation of the CPU but also for the operation of the PD1 peripherals that use the bus clock as their functional clock.

The clock source and frequency selection decisions made for MCLK also affect ULPCLK in RUN and SLEEP modes. See the ULPCLK section for more information on how MCLK and ULPCLK are related in RUN and SLEEP mode.

Using MCLK in STOP and STANDBY Mode

In STOP and STANDBY modes, the MCLK output to PD1 peripherals is disabled, but the ULPCLK, which is the bus clock for PD0 peripherals, is still active in STOP and optionally active in STANDBY. See the ULPCLK section for more information on how the MCLK source and ULPCLK are related in STOP and STANDBY mode.

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MCLK Source Selection

Application software can change the MCLK source from SYSOSC to the SYSPLL outputs or HFCLK (which is either XTAL or HFCLK_IN) by configuring the MCLKCFG.USEHSCLK and HSCLKCFG.HSCLKSEL register bits appropriately in SYSCTL. The following table gives the proper register bit configurations for selecting different clocks for MCLK in RUN and SLEEP modes.

Table 3-13. AM13E232x MCLK Source Selection in RUN and SLEEP Mode

Desired Source	MCLKCFG.USEHSCLK	HSCLKCFG.HSCLKSEL
SYSOSC	0	X
SYSPLLCLK0	1	0
HFCLK	1	1

To switch MCLK from SYSOSC to HSCLK:

1. Verify that MCLK is sourced from SYSOSC (CLKSTATUS.HSCLKMUX is cleared).
2. Enable the desired high speed sources (SYSPLL, XTAL, HFCLK_IN) according to their respective requirements.
3. Select the desired HSCLK source through the HSCLKCFG.HSCLKSEL control
4. Verify that CLKSTATUS.HSCLKGOOD is set, indicating that the selected HSCLK source is valid.
5. Set MCLKCFG.USEHSCLK to switch MCLK to HSCLK.

To switch MCLK from HSCLK to SYSOSC:

1. Verify that MCLK is sourced from HSCLK (CLKSTATUS.HSCLKMUX is set).
2. Clear MCLKCFG.USEHSCLK to switch MCLK to SYSOSC.
3. Wait for CLKSTATUS.HSCLKMUX to clear, indicating that MCLK is now sourced from SYSOSC.
4. If desired, disable any high-speed clock sources (SYSPLL or XTAL)

Note

When MCLK is actively sourced by HSCLK (the HSCLKMUX bit in the CLKSTATUS register is set), the HSCLK source selection must not be changed (the HSCLKSEL bit in the HSCLKCFG register must not be changed). To change the HSCLK source, first switch MCLK to SYSOSC using the procedure given above, re-configure the HSCLK source, and then switch MCLK back to HSCLK.

3.4.3.2 CPUCLK (Processor Clock)

The processor clock (CPU clock) is always derived directly from MCLK and is active in RUN mode at the MCLK frequency. In all other power modes, CPUCLK is disabled.

3.4.3.3 ULPCLK (Low-Power Clock)

The ULPCLK is the bus clock for peripherals in the PD0 power domain. It supports operation up to 50 MHz and is derived directly from the MCLK tree through a clock divider (MCLK/4) which is enabled only when MCLK is sourced from a high-speed clock (SYSPLL, XTAL, or HFCLK_IN). The ULPCLK frequency is dependent on the MCLK dividers configuration and the selected power mode.

ULPCLK Behavior in RUN and SLEEP Modes

The PD0 power domain has a frequency limit of 50MHz in RUN and SLEEP modes. This frequency is derived from the MCLK/4 clock tree. As such, ULPCLK must be maintained to be ≤50MHz at all times. When MCLK is configured to run from SYSOSC, SYSCTL disables the MCLK/4 divider automatically and ULPCLK is sourced from MCLK as these clock sources are always ≤32 MHz.

However, when MCLK is configured to run from a high-speed clock (SYSPLL, XTAL, or HFCLK_IN), hardware shall switch back to MCLK/4 divider. The right configuration of this divider value is the responsibility of

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the application software to ensure that ULPCLK is ≤50 MHz in RUN and SLEEP modes by configuring it appropriately.

Note

MCLK/4 divider for the MCLK/4 domain is by default at /4. When MCLK < 100MHz and > 50MHz, then it can be configured to /2. When MCLK ≤ 50MHz, then it can be configured to /1. Application software shall ensure MCLK/2 and MCLK/4 dividers are configured appropriately using the MCLKDIVCFG field in the MCLKCFG register.

ULPCLK Behavior in STOP, STANDBY, and SHUTDOWN Modes

In STOP mode, the MCLK tree (and by extension, the ULPCLK) run from SYSOSC with a 4MHz rate. In STANDBY mode, the ULPCLK runs from LFCLK to conserve power. In SHUTDOWN mode, the ULPCLK is turned off.

Table 3-14. AM13E232x ULPCLK by Operating Mode

Selected Power Mode	Configuration	Register Settings	ULPCLK Frequency
RUN or SLEEP (250MHz maximum)	MCLK source is SYSOSC	MCLKCFG.USEHSCLK=0x0	ULPCLK is sourced from MCLK according to the MCLK configuration with $f_{ULPCLK} = f_{MCLK}$
	MCLK source is HSCLK (SYSPLL or HFCLK)	MCLKCFG.USEHSCLK=0x1	ULPCLK is sourced from MCLK according to the MCLK configuration with $f_{ULPCLK} = f_{MCLK}$/ Quarter Divider
STOP (4MHz maximum)	STOP with SYSOSC enabled	-	ULPCLK is sourced from SYSOSC with f_{ULPCLK} = 4MHz
STANDBY (32kHz maximum)	STANDBY with ULPCLK and LFCLK enabled	MCLKCFG.STOPCLKSTBY= 0x0	ULPCLK is sourced from LFCLK with $f_{ULPCLK} = f_{LFCLK}$ = 32kHz
SHUTDOWN (Off)	-	-	ULPCLK is off

3.4.3.4 LFCLK (Low-Frequency Clock)

LFCLK provides a continuous 32kHz clock to a variety of peripherals on the device. After a BOOTRST, LFCLK is sourced by the internal 32kHz oscillator (LFOSC).

LFCLK is active in RUN, SLEEP, STOP, and STANDBY power modes. It is possible to disable both ULPCLK and LFCLK together to most peripherals in STANDBY mode to achieve the lowest possible STANDBY mode power consumption (STANDBY1). To do so, set the STOPCLKSTBY bit in the MCLKCFG register in SYSCTL before entering STANDBY. In this state, a few times are the only clocked peripherals.

LFCLK is a synchronized clock. All LFCLK edges are synchronized to the main system clocks (MCLK and ULPCLK), meaning that the registers of peripherals clocked by LFCLK can be read or written to at any time without any special handling.

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Note

When MCLK/ULPCLK are not sourced by LFCLK (for example, when they are sourced by SYSOSC) there is a 5 ULPCLK cycle synchronization delay between the low frequency clock source's clock edge and the corresponding LFCLK edge as seen by peripherals running from LFCLK.

When the MCLK/ULPCLK frequency is constant, this delay is constant and it does not add jitter to LFCLK. If the MCLK/ULPCLK frequency changes, the synchronization delay changes proportionally and this results in a small single-cycle LFCLK jitter at the MCLK/ULPCLK frequency transition point. This jitter changes the duty cycle of one LFCLK period, but there is no accumulation of error (there is never a change in the number of LFCLK periods, ensuring an accurate LFCLK time base for peripherals).

3.4.3.5 HFCLK (High-Frequency External Clock)

The high-frequency external clock (HFCLK) is the output of the high-frequency external clock selection mux, and can be selected as either the high-frequency oscillator (XTAL) output or the high-frequency digital clock input (HFCLK_IN).

The HFCLK can be used as the source for the following clocks:

- HSCLK source (to source MCLK)
- SYSPLL reference clock
- CANCLK source

The HFCLK is only available in RUN and SLEEP modes. HFCLK is automatically disabled by SYSCTL in all other modes, along with the XTAL itself.

3.4.3.6 HSCLK (High Speed Clock)

The high-speed clock (HSCLK) is the output of the high-speed clock selection mux, and can be selected to source MCLK by setting the USEHSCLK bit in the MCLKCFG register. The HSCLK is only a selection option for MCLK; it does not source any other functions. HSCLK can be configured to be sourced from the SYSPLL (SYSPLLCLK0) or the HFCLK (*XTAL* or HFCLK_IN). By default, the HSCLK is sourced from the SYSPLL. To change the HSCLK source to HFCLK, set the HSCLKSEL bit in the HSCLKCFG register.

The HSCLK is only available in RUN and SLEEP modes. It is automatically disabled by SYSCTL in all other modes, along with the SYSPLL and XTAL (if enabled).

SYSCTL will not switch MCLK to HSCLK, even if requested by software, if the HSCLK status check indicates that selected HSCLK source was not started correctly.

3.4.3.7 CANCLK (CAN-FD Functional Clock)

The CANCLK is a functional clock provided directly to the CAN-FD module from either the HFCLK (XTAL or HFCLK_IN) or the SYSPLL (SYSPLLCLK0). This clock is provided as a functional clock to the CAN-FD module asynchronous from the main clock (MCLK) for the highest possible accuracy. The CANCLK source is selected in SYSCTL by configuring the CANCLKSRC bit in the GENCLKCFG register. Additional CAN-FD clock configuration is provided within the CAN-FD peripheral itself (review the *MCAN* chapter for more detail).

3.4.3.8 ECATxCLK (EtherCAT Functional Clock)

ECAT25CLK (PHY clock) and ECAT100CLK (EtherCAT clock) are the functional clocks provided directly to the EtherCAT module from the SYSPLL (SYSPLLCLK0). These clocks are provided as functional clocks to the EtherCAT module asynchronous from the main clock (MCLK) for the highest possible accuracy. The clocks are enabled in SYSCTL by setting the PHYCLKEN and ECAT100CLKEN bits in the ETHERCATCLKCTL register. In addition, the SYSPLL clock sources can be further divided (/1, /2, /3, …, /8) by configuring the ECATDIV bit in the ETHERCATCLKCTL register. Additional EtherCAT clock configuration is provided within the EtherCAT peripheral itself (review the *ESC* chapter for more detail).

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3.4.3.9 External Clock Output (CLK_OUT)

A clock output unit is provided for sending digital clock signals from the device to external circuits or to the frequency clock counter. This feature is useful for clocking external circuitry such as an external ADC that does not have a clock source. The clock output unit has a flexible set of sources to select and includes a programmable divider.

Available clock sources for CLK_OUT:

- SYSPLLCLK0
- SYSPLLCLK1
- HFCLK
- SYSOSC
- ULPCLK
- LFCLK

The selected clock source can be divided by 1 (no divide), 2, 4, 6, 8, 10, 12, 14, or 16 before being output to the pin or to the frequency clock counter.

To use the clock output unit:

1. Configure IOMUX to select the CLK_OUT function on the device pin with CLK_OUT.
2. Select the desired clock source in the EXCLKSRC field of the GENCLKCFG register.
3. Set the desired clock divider, if necessary, in the EXCLKDIVVAL field of the GENCLKCFG register, and enable the divider by setting the EXCLKDIVEN bit. This must be done while EXCLKEN=0 (before CLK_OUT is enabled)
4. Enable the external clock output by setting the EXCLKEN bit in the GENCLKEN register.

Note

When the CLK_OUT source is selected as ULPCLK, the clock divider must be enabled (GENCLKCFG.EXCLKDIVEN must be set).

Note

When clearing the EXCLKEN bit to disable CLK_OUT, allow the clock source to run for 10 clock cycles to stabilize the EXCLKSRC mux.

Note

When disabling a clock source which is selected for CLK_OUT, it is recommended to disable the CLK_OUT function before disabling the clock source if it is important that CLK_OUT be logic low (0) when the clock source is disabled. If CLK_OUT is left enabled and the source for CLK_OUT is disabled, it is possible that CLK_OUT may stop in a logic high (1) state.

Note

When the CLK_OUT source is selected as SYSPLLCLK0 or SYSPLLCLK1, the SYSPLL output must be ≤48MHz. Further speed restrictions can exist depending on the IO capabilities of a specific device and pin; see the Digital IO specifications in the device-specific data sheet for details on supported IO speeds.

3.4.4 Clock Monitors

Several hardware clock monitors are provided to ensure that the CKM is functioning properly. Clock faults are processed through SYSCTL and result in either a brownout reset (in the event of a fatal fault) or a SYSCTL interrupt.

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Table 3-15. AM13E232x CKM Clock Monitors

Clock Monitor	Description
MCLK	Asserts a fault if there is no MCLK activity for a period of 1-12 LFOSC cycles
LFOSC Startup	Indicates when LFOSC startup has completed and is available for use by peripherals
HFCLK Startup	Indicates if XTAL successfuly started within the specified startup time or if HFCLK_IN is stuck, before selecting HFCLK to source system functions
SYSPLL Startup	Indicates if SYSPLL successfully started, at which point the clock outputs from SYSPLL can be selected to source system functions
HSCLK Status	Indicates if the selected HSCLK source successfully started with a GOOD status or failed with a DEAD status

3.4.4.1 MCLK Monitor

A digital clock monitor can be used with MCLK. The MCLK monitor asserts an MCLK fault if there is no MCLK activity for a period of 1-12 LFCLK cycles. An MCLK fault is always considered fatal to the system and generates a BOOTRST.

The MCLK monitor can be enabled after the LFCLK is configured and running. To enable the MCLK monitor, set the MCLKDEADCHK bit in the MCLKCFG register in SYSCTL. When enabled, the MCLK monitor runs in all operating modes except for STANDBY1 and SHUTDOWN.

3.4.4.2 Startup Monitors

Clock startup monitors are provided for application software to check that that the LFOSC, XTAL/HFCLK_IN, SYSPLL, and HSCLK sources are alive before they are selected by software to be used to source a clock in the system. When a clock source has started successfully and is ready, a GOOD indication is given in the CLKSTATUS register in SYSCTL and an interrupt is generated. The startup monitors only provide a status indication when a related clock system configuration change is made. When an initial GOOD indication is given, the clock is not continuously monitored by the startup monitor. Continuous monitoring is provided for *MCLK*.

3.4.4.2.1 LFOSC Startup Monitor

The LFOSC is started automatically after a BOOTRST. Please refer to the device-specific data sheet for the LFOSC startup time. A startup monitor is provided to indicate to the application software when LFOSC startup has completed, at which time the LFCLK is available for use by peripherals. When LFSOSC startup has completed, the LFOSC startup monitor asserts the LFOSCGOOD bit in the CLKSTATUS register in SYSCTL and the LFOSCGOOD interrupt is asserted to alert the application.

3.4.4.2.2 HFCLK Startup Monitor

The XTAL takes time to start after being enabled. A startup monitor is provided to indicate to the application software if the XTAL has successfully started, at which point the HFCLK can be selected to source a variety of system functions. The HFCLK startup monitor also supports checking the HFCLK_IN digital clock input for a clock stuck fault.

To enable the HFCLK startup monitor, clear the HFCLKFLTCHK bit in the HFCLKCLKCFG register in SYSCTL (the default state is disabled).

When XTAL is started or the HFCLK_IN is selected as the HFCLK source, the HFCLKGOOD and HFCLKOFF bits in the CLKSTATUS register in SYSCTL are cleared.

In the case of XTAL being used, after the specified XTAL startup time has expired the XTAL status is tested. If the XTAL started successfully, the XTAL startup monitor asserts the HFCLKGOOD bit in the CLKSTATUS register and the HFCLKGOOD interrupt is also asserted. If the XTAL did not start within the specified startup time, the HFCLKOFF bit is set, indicating that the XTAL was dead at startup.

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In the case of HFCLK_IN being used, after HFCLK_IN is selected a clock stuck check is performed. If the clock is alive, the HFCLKGOOD bit is set in the CLKSTATUS register and the HFCLKGOOD interrupt is also asserted. If the HFCLK_IN signal was stuck, the HFCLKOFF bit in CLKSTATUS register is set, indicating that the HFCLK_IN is dead.

If desired, checking of the HFCLK by the HFCLK startup monitor can be left disabled by keeping the HFCLKFLTCHK bit set in the HFCLKCLKCFG register in SYSCTL.

Note

The HFCLK must be in a stable state before attempting to enter STOP or STANDBY low power modes. Before entering STOP or STANDBY, make sure that either the HFCLKGOOD bit or the HFCLKOFF bit is set.

3.4.4.2.3 SYSPLL Startup Monitor

The SYSPLL takes time to start and settle after being enabled. A startup monitor is provided to indicate to the application software if the SYSPLL has successfully started, at which point the clock outputs from the SYSPLL can be selected to source a variety of system functions.

When the SYSPLL is started, the SYSPLLGOOD and SYSPLLOFF bits in the CLKSTATUS register in SYSCTL are cleared. After the startup/settling time has expired, the SYSPLL status is tested. If the SYSPLL started successfully, the SYSPLL startup monitor will assert the SYSPLLGOOD bit in the CLKSTATUS register and the SYSPLLGOOD interrupt will also be asserted. If the SYSPLL did not start within the specified time, the SYSPLLOFF bit will be set, indicating that the SYSPLL was dead at startup.

Note

The SYSPLL must be in a stable state before attempting to enter STOP or STANDBY low power modes. Before entering STOP or STANDBY, make sure that either the SYSPLLGOOD bit or the SYSPLLOFF bit is set.

3.4.4.2.4 HSCLK Status

The HSCLK is sourced from the HFCLK or the SYSPLL. The CLKSTATUS register in SYSCTL provides HSCLKGOOD and HSCLKDEAD indications, which indicate if the selected HSCLK source started successfully with a GOOD status or failed with a DEAD status, respectively. SYSCTL will not switch MCLK over to HSCLK, even if requested, if HSCLKGOOD is not set.

In addition, the HSCLKSOFF bit is provided in CLKSTATUS to indicate if all HSCLK sources (SYSPLL, HFCLK) are either off (disabled) or started with a DEAD status.

3.4.5 Clock Initialization Procedure

Note

TI recommends using the Clock Tree tool (integrated into Sysconfig) to autogenerate clock initialization code since the tool performs validation checks on all clock register settings and performs the proper clock initialization sequence.

If configuring clocking initializations without the Clock Tree tool from Sysconfig, the below is the recommended clock startup sequence to get the MCLK up to 250MHz.

1. Start the external oscillator (XTAL) as HFCLK source
   a. Power down the XTAL oscillator by writing XTALCR.OSCOFF = 1
   b. Program the crystal startup timeout by writing HFCLKCFG.XTALTIME
   c. Power up and start the XTAL oscillator by writing XTALCR.OSCOFF = 0
   d. Disable the HFCLK startup monitor by writing HFCLKCLKCFG.HFCLKFLTCHK = 0
2. Configure and enable the SYSPLL
   a. Disable the SYSPLL by writing HSCLKEN.SYSPLLEN = 0

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b. Wait until SYSPLL has fully shut down by polling CLKSTATUS.SYSPLLOFF = 1
c. Configure the SYSPLL output dividers for SYSPLLCLK0 and SYSPLLCLK1 by writing the SYSPLLCFG0.RDIV0 and RDIV1 fields respectively
d. Enable the SYSPLL outputs SYSPLLCLK0 and SYSPLLCLK1 by writing the SYSPLLCFG0.ENABLECLK0 and ENABLECLK1 fields respectively
e. Select the SYSPLL reference clock source to HFCLK by setting SYSPLLCFG0.SYSPLLREF = 1
f. Program the SYSPLL feedback loop (QDIV) divider by writing SYSPLLCFG1.QDIV
g. Program the SYSPLL reference clock pre-divider (PDIV) by writing SYSPLLCFG1.PDIV
h. Load PLL analog tuning parameters from the FACTORY flash region.
    i. Write SYSPLLPARAM0.CAPBVAL, CPCURRENT, STARTTIMELP, and STARTTIME fields with the corresponding values from one of the below registers in the FACTORY region (depending on the PDIV set in the previous step).
        1. If PDIV is /1: Write values from PLLSTARTUP0_32_48MHZ fields
        2. If PDIV is /2: Write values from PLLSTARTUP0_16_32MHZ fields
        3. If PDIV is /4: Write values from PLLSTARTUP0_8_16MHZ fields
        4. If PDIV is /8: Write values from PLLSTARTUP0_4_8MHZ fields
    ii. Write SYSPLLPARAM1.LPFRESC, LPFRESA, and LPFCAPA fields with the corresponding values from one of the below registers in the FACTORY region (depending on the PDIV set in the previous step).
        1. If PDIV is /1: Write values from PLLSTARTUP1_32_48MHZ fields
        2. If PDIV is /2: Write values from PLLSTARTUP1_16_32MHZ fields
        3. If PDIV is /4: Write values from PLLSTARTUP1_8_16MHZ fields
        4. If PDIV is /8: Write values from PLLSTARTUP1_4_8MHZ fields
i. Enable the SYSPLL by writing HSCLKEN.SYSPLLEN = 1
j. Wait until the SYSPLL is locked and producing a stable output by polling CLKSTATUS.SYSPLLGOOD = 1

3. Gradually step up the SYSPLL output to full speed
    a. Set the SYSPLL-to-MCLK divider to /4 by setting GENCLKEN.EXTDIVMCLK = 0x1
    b. Enable the SYSPLL-to-MCLK divider by setting GENCLKEN.MCLKEXTDIVEN = 1
4. Switch MCLK source from SYSOSC to HSCLK (SYSPLL)
    a. Select SYSPLLCLK0 as the HSCLK source by setting HSCLKCFG.HSCLKSEL = 0
    b. Wait until HSCLK is running by polling CLKSTATUS.HSCLKGOOD = 1
    c. Switch the MCLK source from SYSOSC to HSCLK by setting MCLKCFG.USEHSCLK = 1
    d. Delay 20 cycles
    e. Wait until MCLK is properly sourced from HSCLK by polling CLKSTATUS.HSCLKMUX = 1
5. Step up to SYSPLL / 2
    a. Set the SYSPLL-to-MCLK divider to /2 by setting GENCLKEN.EXTDIVMCLK = 0x0
    b. Delay 20 cycles
    c. (Recheck) Wait until MCLK is properly sourced from HSCLK by polling CLKSTATUS.HSCLKMUX = 1
6. Ramp up to full SYSPLL speed
    a. Disable the SYSPLL-to-MCLK divider by setting GENCLKEN.MCLKEXTDIVEN = 0
    b. Delay 20 cycles
    c. (Recheck) Wait until MCLK is properly sourced from HSCLK by polling CLKSTATUS.HSCLKMUX = 1
7. Configure MCLKDIV2 and MCLKDIV4 dividers by writing the MCLKCFG.MCLKDIVCFG field
8. Configure additional clock dividers for MCAN
    a. Select SYSPLLCLK0 as the MCAN clock source by setting GENCLKCFG.CANCLKSRC = 1
    b. Set the SYSPLLCLK0-to-MCAN divider by setting the GENCLKEN.EXTDIVCAN field
    c. Enable the SYSPLLCLK0-to-MCAN divider by setting GENCLKEN.CANEXTDIVEN = 1
9. Configure additional clock dividers for and EtherCAT

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a. Set the SYSPLLCLK0-to-EtherCAT divider by setting the ETHERCATCLKCTL.ECATDIV field
b. Enable the EtherCAT clocks by setting ETHERCATCLKCTL.ECAT100CLKEN = 1 and ETHERCATCLKCTL.PHYCLKEN = 1

3.4.6 Frequency Clock Counter (FCC)

The frequency clock counter (FCC) enables flexible in-system testing and calibration of a variety of oscillators and clocks on the device. The FCC counts the number of clock periods seen on the selected source clock within a known fixed trigger period (derived from a secondary reference source) to provide an estimation of the frequency of the source clock.

Application software can use the FCC to measure the frequency of the following source oscillators and clocks (selected through the FCCSELCLK field in the GENCLKCFG register):

- MCLKDIV4
- SYSOSC
- HFCLK
- CLK_OUT
- SYSPLLCLK0 or SYSPLLCLK1
- ECAT25CLK
- The external FCC input (FCC_IN)

The reference clock used to set the trigger time over which pulses of the source clock are counted is configurable (through the FCCTRIGSRC field in the GENCLKCFG register), and can be driven by:

- The external FCC input (FCC_IN)
- LFCLK

The trigger time period can be set in one of two ways (through the FCCLVLTRIG field in the GENCLKCFG register):

- Level triggered (one rising edge to one falling edge of the reference clock input)
- Rising-edge to rising-edge triggered, for a defined number of clock periods of the reference clock (selectable from 1 to 32 through the FCCTRIGCNT field in the GENCLKCFG register)

When the trigger source is selected as the external FCC input in level-triggered mode, a user-specified counting period can be set by applying a logic high pulse on the FCC_IN pin of the desired trigger length.

When the trigger source is selected as the LFCLK, using rising-edge to rising-edge triggering causes the FCC to capture the number of source clock pulses which occurred within 1 to 32 clock periods of the LFCLK (30.5µs).

The FCC counter is 22 bits and supports counting from 0 up to $2^{22} - 1 = 4{,}194{,}303$.

While the external FCC input (FCC_IN function) can be used as either the FCC clock source or the FCC trigger input, the signal cannot be used for both functions during the same FCC capture. FCC_IN must be configured as either the FCC clock source or the FCC trigger.

3.4.6.1 Using the FCC

Rising-Edge to Rising-Edge Triggered Mode with FCC_IN Trigger

The following steps describe how to use the FCC to count the number of source clock pulses within the trigger period set by the reference clock, with the FCC_IN pin being selected as the reference clock and the SYSOSC being selected as the source clock. This example would be useful for calibrating the SYSOSC frequency with respect to an accurate clock source provided to the FCC_IN pin externally.

1. Set the source clock to SYSOSC by configuring the FCCSELCLK field in the GENCLKCFG register.
2. Set the reference clock to FCC_IN by clearing the FCCTRIGSRC bit in the GENCLKCFG register.
3. Select rising-edge to rising-edge triggering by clearing the FCCLVLTRIG bit in the GENCLKCFG register.
4. Select the desired number of reference clock periods to count the source clock over in the FCCTRIGCNT field in the GENCLKCFG register.

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5. Ensure that SYSOSC is enabled at the desired frequency, and that the external clock source connected to FCC_IN is constantly running before continuing.
6. Write the GO bit and KEY field to the FCCCMD register to start the FCC capture on the next trigger clock period.
7. Poll the FCCDONE status bit in the CLKSTATUS register. When the capture completes, FCCDONE will be set by hardware. FCCDONE is read-only and is automatically cleared by hardware when a new capture is started.
8. Extract the resulting count from the 22-bit DATA field in the FCC register.

Note

For an accurate count of FCC cycles, it is best to wait at least 6 pulses of FCC before setting FCCTRIGCNT=0x0

Rising-Edge to Rising-Edge Triggered Mode with LFCLK Trigger

The following steps describe how to use the FCC to count the number of source clock pulses within the reference clock period, with the LFCLK being selected as the reference clock and the SYSOSC being selected as the source clock. This example would be useful for calibrating the SYSOSC frequency with respect to an accurate 32.768kHz watch crystal.

1. Set the source clock to SYSOSC by configuring the FCCSELCLK field in the GENCLKCFG register.
2. Set the reference clock to LFCLK by setting the FCCTRIGSRC bit in the GENCLKCFG register.
3. Select rising-edge to rising-edge triggering by clearing the FCCLVLTRIG bit in the GENCLKCFG register.
4. Select the desired number of reference clock periods to count the source clock over in the FCCTRIGCNT field in the GENCLKCFG register.
5. Ensure that SYSOSC is enabled at the desired frequency, and that the LFCLK is running correctly before continuing.
6. Write the GO bit and KEY field to the FCCCMD register to start the FCC capture on the next trigger clock period.
7. Poll the FCCDONE status bit in the CLKSTATUS register. When the capture completes, FCCDONE will be set by hardware. FCCDONE is read-only and is automatically cleared by hardware when a new capture is started.
8. Extract the resulting count from the 22-bit DATA field in the FCC register. If SYSOSC was running at 32MHz and FCCTRIGCNT was set to '0' (one reference clock period), the result should be approximately 976 cycles counted within the single 32.768kHz period.

In general, increasing the FCCTRIGCNT value increases the accuracy of the measurement, at the expense of longer measurement time.

Level Triggered Mode with FCC_IN Trigger and HFCLK_IN Clock

The following steps describe how to use the FCC to count the number of source clock pulses within one external reference pulse window, with HFCLK_IN being selected as the source clock. This example would be useful for measuring the frequency of an external clock source with respect to a fixed pulse width driven by an external signal.

1. Set the source clock to HFCLK by configuring the FCCSELCLK field in the GENCLKCFG register.
2. Set the trigger clock to the FCC_IN pin function by clearing the FCCTRIGSRC bit in the GENCLKCFG register.
3. Set level triggering by setting the FCCLVLTRIG bit in the GENCLKCFG register.
4. Ensure that IOMUX is configured for FCC_IN, that HFCLK is configured for HFCLK_IN, and that an external clock is sourcing HFCLK_IN.
5. Write the GO bit and KEY field to the FCCCMD register to start the FCC capture when FCC_IN goes logic high. Note that if FCC_IN is already logic high when GO is asserted, counting starts immediately. When using level mode, FCC_IN should be low when GO is set, and the trigger pulse should be sent to FCC_IN after GO is set.

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6. Poll the FCCDONE status bit in the CLKSTATUS register. When the capture completes, FCCDONE will be set by hardware. FCCDONE is read-only and is automatically cleared by hardware when a new capture is started.
7. Extract the resulting count from the 22-bit DATA field in the FCC register.

3.4.6.2 FCC Frequency Computation and Accuracy

The frequency of the source clock can be computed after capture if the trigger time is known. The frequency is computed by dividing the number of source clock cycles captured by the trigger time. For example, if the trigger source was a 32.768kHz clock, the trigger mode was rising-edge to rising-edge, and the period count was 1, then the trigger time is one 32.768kHz clock period (30.5µs). If the captured source count were to come back as 122, the frequency of the source clock is computed as 122 divided by 30.5µs, giving a source clock frequency of approximately 3.99MHz.

$$f_{source} = FCC.DATA / ((GENCLKCFG.FCCTRIGCNT+1) / f_{ref}) \quad (9)$$

The FCC is accuracy is dependent on the trigger clock accuracy as well as the total number of clock cycles captured. The FCC intrinsic error is ≤2 source clock cycles per capture due to synchronization of the trigger to the source clock. Therefore, the impact of these two clock cycles is reduced as more cycles are counted (as the trigger time is increased and/or the source clock frequency is increased). Approximate intrinsic error of the FCC for various source clock frequencies captured against one 32.678kHz period (FCCTRIGCNT=0) and 32 clock periods (FCCTRIGCNT=31) are given in Table 3-16.

Table 3-16. FCC Error

Use Case (Source Clock Frequency)	FCC Trigger Time	FCC Count Result	FCC Count Uncertainty	Approximate FCC Intrinsic Uncertainty Error
4MHz source clock	30.5µs	122	2 cycles	1.6%
	976.6µs	3906		0.05%
32MHz source clock	30.5µs	976		0.20%
	976.6µs	31250		0.01%
200MHz source clock	30.5µs	6100		0.03%
	976.6µs	195200		0.001%

Note

When using the FCC_IN signal, it is recommended to have a fast slew rate of 10ns or less on the FCC_IN pin to minimize measurement uncertainty.

3.4.7 Asynchronous Fast Clock Requests

The GPIO peripheral is configured to asynchronously assert a hardware request to the SYSCTL for a fast clock source, even if the device is operating in STOP or STANDBY mode. This mechanism for applications where the MCLK/ULPCLK tree is normally sourced from either LFCLK (at 32kHz) or SYSOSC, but a faster clock is temporarily needed to quickly handle a GPIO peripheral event.

Asynchronous fast clock requests are also useful for scenarios where the device is running in STANDBY1 mode. In STANDBY1 (when STOPCLKSTBY is set), the ULPCLK and LFCLK are disabled to all peripherals. To wake up the device from this state where the bus clock (ULPCLK) is disabled, a GPIO interrupt request forces an asynchronous fast clock request to wake the device to RUN mode.

Asynchronous fast clock requests temporarily provides the GPIO peripheral with bus clock (MCLK/ULPCLK), sourced from the SYSOSC, for the duration of the request.

Asynchronous Fast Clock Behavior

When configured, SYSCTL responds to a peripheral fast clock request in the following way:

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1. If the device is currently in a STOP or STANDBY mode, the low power state is temporarily suspended to support running the bus clock (ULPCLK) at the SYSOSC base frequency.
2. If disabled, SYSOSC is forced to be enabled; if SYSOSC is already running but at a different frequency than base frequency, SYSOSC is forced to base frequency.
3. The MCLK/ULPCLK tree is forced to be sourced from SYSOSC at the base frequency; if the device is in RUN mode then the CPUCLK is also switches to the SYSOSC rate (the CPUCLK is always derived from MCLK).

After the configuration above is applied, values are held for the duration of time that the asynchronous request remains asserted plus approximately 1µs after the request is removed. The system then returns to the configuration which existed before the fast clock request, provided the CPU did not change the configuration during the request.

Asynchronous fast clock requests are ignored and results in no effect on the device configuration if any of the following are true:

- MCLK is already sourced from SYSOSC at base frequency
- Asynchronous fast clock requests are globally blocked by setting the BLOCKASYNCALL bit in the SYSOSCCFG register in SYSCTL

Peripheral Support

The GPIO peripheral provides support for generating an asynchronous fast clock request. The purpose, request source, and configuration requirements are given in Table 3-17.

Table 3-17. Peripheral Support for Asynchronous Fast Clock Requests

Peripheral	Purpose	Request Source	Configuration
GPIO	Fast CPU wake from GPIO event	GPIO activity	The GPIO generates an asynchronous fast clock request through the GPIO configuration registers. This is for applications where GPIO wake from STANDBY mode is desired, as the fast clock request results in the GPIO digital glitch filters running at SYSOSC base frequency. In addition to configuring the GPIO registers to request the fast clock, the BLOCKASYNCALL bit must be cleared in the SYSOSCCFG register to allow the request to propagate.

Fast CPU Event Handling

In addition to the GPIO fast clock request triggers, SYSCTL can be configured to generate an asynchronous fast clock request upon any IRQ to the CPU. This provides the lowest latency interrupt handling when the system is running at the LFCLK rate (32kHz), as the IRQ request propagates through the wake-up logic at the SYSOSC rate instead of the LFCLK rate (32kHz). When the FASTCPUEVENT bit is set in the SYSOSCCFG register in SYSCTL, any interrupt request to the CPU also generates a fast clock request.

Asynchronous Fast Clock Request Logic

The logic for asserting a fast clock request is given in the following figure.

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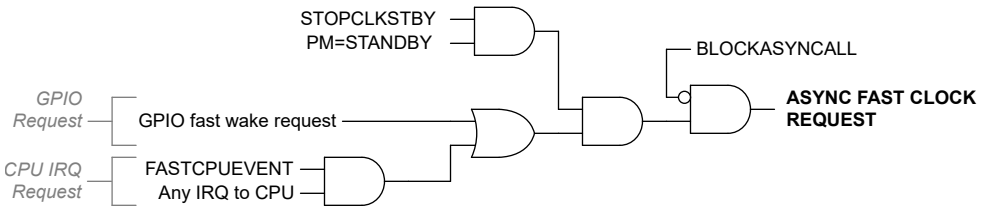


Figure 3-9. Asynchronous Fast Clock Request Logic

3.5 Memory Map

All AM13E232x devices share a common platform memory map. Peripherals are assigned a fixed address space and have the same address space on all devices within the family. The memory map is compliant with the standard ARM® Cortex®-M memory regions.

Note

All regions are non-secure. AM13E232x devices do not have ARM® TrustZone technology enabled.

Table 3-18. Top Level Memory Map Regions

Memory Region	Start Address	End Address	Description
Code	0x0000.0000	0x1FFF.FFFF	Flash memory, ROM, SRAM Bank 4 & 5 (dual mapped in Code Region)
SRAM	0x2000.0000	0x3FFF.FFFF	SRAM Banks 0 to 5
Peripheral	0x4000.0000	0x5FFF.FFFF	Global peripheral memory-mapped registers and global nonexecutable data memory
Subsystem	0x6000.0000	0x7FFF.FFFF	Local CPU subsystem memory-mapped registers. Includes FLASH special regions NONMAIN and FACTORY.
System PPB	0xE000.0000	0xFFFF.FFFF	ARM Private Peripheral Bus

3.5.1 Memory Map Regions

3.5.1.1 Code Region

Table 3-19. Code Region Memory Map

Memory Region	Start Address	End Address	CPU Access	DMA Access	NPU Access
Flash Main Bank 0	0x0000.0000	0x0003.FFFF	Yes	Yes	No
Flash Main Bank 1	0x0004.0000	0x0007.FFFF	Yes	Yes	No
SRAM Bank 4 & 5	0x00C2.0000	0x00C2.FFFF	Yes	No	No
ROM	0x0100.0000	0x0100.BFFF	Yes	No	No

The code region contains the flash memory used to store executable code and data. Accesses to the flash memory from the CPU through the code region are processed through the A-HB bus matrix to the flash read interface directly. See Section 13 for more information on the Flash memories and flash controller module.

The code region also contains the read-only memory (ROM) used for the TI device boot code and the bootstrap loader. The ROM is only available during the initial device boot process.

SRAM Bank 4 & 5 are also dual mapped to this region and the SRAM Region.

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3.5.1.2 SRAM Region

Table 3-20. SRAM Region Memory Map

Memory Region	Start Address	End Address	CPU Access	DMA Access	NPU Access	Access Arbitration
SRAM Bank 0	0x2000.0000	0x2000.7FFF	Yes	Yes	Yes	Dynamic arbitration between the CPU (S-AHB), DMA, and NPU
SRAM Bank 1	0x2000.8000	0x2000.FFFF	Yes	Yes	Yes	Dynamic arbitration between the CPU (S-AHB), DMA and NPU
SRAM Bank 2	0x2001.0000	0x2001.7FFF	Yes	Yes	Yes	Dynamic arbitration between the CPU (S-AHB), DMA and NPU
SRAM Bank 3	0x2001.8000	0x2001.FFFF	Yes	Yes	Yes	Dynamic arbitration between the CPU (S-AHB), DMA and NPU
SRAM Bank 4	0x2002.0000	0x2002.7FFF	Yes	Yes	No	First level static selection between CPU busses S-AHB and C-AHB (selected via the SRAMx_STATIC_MUX_SEL bits in the SYSCTL registers), second level dynamic arbitration with DMA
SRAM Bank 5	0x2002.8000	0x2002.FFFF	Yes	Yes	No	First level static selection between CPU busses S-AHB and C-AHB, second level dynamic arbitration with DMA

The SRAM region contains the dedicated static random access memory (SRAM) banks. The SRAMs supports zero wait state access across all MCLK frequencies.

AM13E232x devices have up to 6 banks of SRAM. Each bank is 32KB and has an 8-bit parity safety checking feature. On a read access, parity is checked and the SRAM parity error triggers an NMI interrupt. The NMIRIS.SRAMPAR bit goes high when a parity error on one of the SRAMs is detected.

Accesses to the SRAM banks from the CPU are processed through the System AHB (S-AHB) bus matrix to the SRAM interface directly. SRAM bank 4-5 can also be accessed from the CPU through the CPU AHB (C-AHB) bus matrix.

See the device-specific data sheet for the amount of SRAM present for a given part number.

3.5.1.2.1 SRAM Write Protection

SRAM Write Protection Control for this device is implemented in the Global Security Controller (GSC). Please refer to the related chapter for more information.

3.5.1.3 Peripheral Region

The peripheral region contains the memory-mapped peripherals on the peripheral buses.

Table 3-21. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address
pd1 by2 clock		
PGA_REGS	PGA0	0x400F_C000
PGA_REGS	PGA1	0x400F_D000
PGA_REGS	PGA2	0x400F_E000
MCAN_REGS	MCAN0	0x4011_0000
MCAN_REGS	MCAN1	0x4011_8000
TIMG4_REGS	TIMG4	0x4018_0000

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Table 3-21. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
TIMG12_REGS	TIMG12	0x4018_8000
AES_REGS	AES	0x401B_0000
CRCP_REGS	CRC	0x401B_2000
KEYSTORE_REGS	KEYSTORE	0x401B_6000
UNICOMMUART_REGS	UC0_UART	0x4060_0000
UNICOMMUART_REGS	UC1_UART	0x4060_1000
UNICOMMUART_REGS	UC2_UART	0x4060_2000
UNICOMMI2CC_REGS	UC0_I2CC	0x4060_8000
UNICOMMI2CC_REGS	UC1_I2CC	0x4060_9000
UNICOMMI2CC_REGS	UC2_I2CC	0x4060_A000
UNICOMMI2CT_REGS	UC0_I2CT	0x4061_0000
UNICOMMI2CT_REGS	UC1_I2CT	0x4061_1000
UNICOMMI2CT_REGS	UC2_I2CT	0x4061_2000
UNICOMMSPI_REGS	UC0_SPI	0x4061_8000
UNICOMMSPI_REGS	UC1_SPI	0x4061_9000
UNICOMM_REGS	UNICOMM0	0x4063_0000
UNICOMM_REGS	UNICOMM1	0x4063_2000
UNICOMM_REGS	UNICOMM2	0x4063_4000
SPG_REGS	SPG0	0x4063_F000
UNICOMMUART_REGS	UC3_UART	0x4064_0000
UNICOMMUART_REGS	UC4_UART	0x4064_1000
UNICOMMUART_REGS	UC5_UART	0x4064_2000
UNICOMMI2CC_REGS	UC3_I2CC	0x4064_8000
UNICOMMI2CC_REGS	UC4_I2CC	0x4064_9000
UNICOMMI2CC_REGS	UC5_I2CC	0x4064_A000
UNICOMMI2CT_REGS	UC3_I2CT	0x4065_0000
UNICOMMI2CT_REGS	UC4_I2CT	0x4065_1000
UNICOMMI2CT_REGS	UC5_I2CT	0x4065_2000
UNICOMMSPI_REGS	UC3_SPI	0x4065_8000
UNICOMMSPI_REGS	UC4_SPI	0x4065_9000
UNICOMM_REGS	UNICOMM3	0x4067_0000
UNICOMM_REGS	UNICOMM4	0x4067_2000
UNICOMM_REGS	UNICOMM5	0x4067_4000
SPG_REGS	SPG1	0x4067_F000
pd1 by1 clock		
ADC_LITE_REGS	ADC0	0x4000_0000
ADC_LITE_REGS	ADC1	0x4000_2000
ADC_LITE_REGS	ADC2	0x4000_4000
ADC_LITE_RESULT_REGS	ADC0RESULT	0x4000_A000
ADC_LITE_RESULT_REGS	ADC1RESULT	0x4000_B000
ADC_LITE_RESULT_REGS	ADC2RESULT	0x4000_C000
MCPWM_6CH_REGS	MCPWM0	0x4001_0000
MCPWM_6CH_REGS	MCPWM1	0x4001_1000
MCPWM_6CH_REGS	MCPWM2	0x4001_2000
DMA_REGS	DMA0	0x4002_0000
FLASH_CTRL_REGS	FLASH	0x4002_8000
MEM_CFG_REGS	MEMCFG	0x4002_A000
EAM_REGS	EAM	0x4002_C000
EPWM_REGS	EPWM0	0x400B_4000

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Table 3-21. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address
EPWM_REGS	EPWM1	0x400B_5000
EPWM_REGS	EPWM2	0x400B_6000
EPWM_REGS	EPWM3	0x400B_7000
EPWM_REGS	EPWM4	0x400B_8000
EPWM_REGS	EPWM5	0x400B_9000
ECAP_REGS	ECAP0	0x4044_0000
ECAP_REGS	ECAP1	0x4044_1000
ECAP_REGS	ECAP2	0x4044_2000
HRCAP_REGS	HRCAP2	0x4044_2040
EQEP_REGS	EQEP0	0x4044_8000
EQEP_REGS	EQEP1	0x4044_9000
CMPSS_LITE_REGS	CMPSS0	0x4046_0000
CMPSS_LITE_REGS	CMPSS1	0x4046_1000
CMPSS_LITE_REGS	CMPSS2	0x4046_2000
CMPSS_LITE_REGS	CMPSS3	0x4046_3000
INPUT_XBAR_REGS	INPUTXBAR	0x4046_8000
PWM_XBAR_REGS	PWMXBAR	0x4046_9000
OUTPUTXBAR_REGS	OUTPUTXBAR	0x4046_A000
SYNC_SOC_REGS	SYNC	0x4046_B000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR0_FLAGS	0x4047_0000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR1_FLAGS	0x4047_1000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR2_FLAGS	0x4047_2000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR3_FLAGS	0x4047_3000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR4_FLAGS	0x4047_4000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR5_FLAGS	0x4047_5000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR6_FLAGS	0x4047_6000
OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR7_FLAGS	0x4047_7000
INPUT_FLAG_XBAR_REGS	INPUTXBAR_FLAGS	0x4049_0000
SDFM_REGS	SDFM	0x4049_1000
ESCSS_REGS	ESCSS	0x404A_8000
ESCSS_CONFIG_REGS	ESCSS_CONFIG	0x404A_8200
FSI_TX_REGS	FSI_TX	0x4050_0000
FSI_RX_REGS	FSI_RX	0x4050_1000
pd1 by4 clock		
NVMNW_REGS	NVMNW	0x4004_2000
GSC_REGS	GSC	0x4004_6000
cbpdd0		
SYSCTL_REGS	SYSCTL	0x400A_F000
DEBUGSS_REGS	DEBUGSS	0x400C_7000
IOMUX_REGS	IOMUX	0x400C_C000
WWDT_REGS	WWDT	0x400D_0000
GPIO_REGS	GPIO0	0x400F_0000
GPIO_REGS	GPIO1	0x400F_2000
GPIO_REGS	GPIO2	0x400F_4000
GPIO_REGS	GPIO3	0x400F_6000

3.5.1.4 Subsystem Region

The Subsystem region contains local CPU subsystem (CPUSS) memory-mapped registers. This region includes flash regions for NONMAIN and FACTORY (read-only) data.

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Table 3-22. Subsystem Region Memory Map

Memory Region	Start Address	End Address	CPU Access	DMA Access	NPU Access
Flash Non-Main Bank 0	0x6010.0000	0x6010.0FFF	Yes	Yes	No
Flash Non-Main Bank 1	0x6010.1000	0x6010.1FFF	Yes	Yes	No
Flash Factory Bank 1	0x6011.1000	0x6011.17FF	Yes	No	No

3.5.1.5 System PPB Region

The system private peripheral bus (PPB) region contains memory-mapped registers on the ARM private peripheral bus. These registers are tightly coupled to the CPU and are the interface for peripherals such as the memory protection unit (MPU), SysTick timer, and CPU power management and reset functions.

3.5.2 Flash Memory

The flash memory is used for storing application code and data, the device boot configuration, and parameters which are preprogrammed by TI from the factory. The flash memory is organized into one or more banks, and the memory in each bank is further mapped into one or more logical memory regions and assigned system address space for use by the application.

3.5.2.1 Banks

The nonvolatile memory system provides support for up to 5 flash memory banks (enumerated as BANK0 through BANK4). The number of flash banks present is device dependent. AM13E232x devices implement 2 flash memory banks (BANK0 and BANK1).

On AM13E232x devices, a program/erase operation on a bank will also stall read requests issued to the bank which is executing the program/erase operation, but it will not stall read requests issued to any other bank. As such, the presence of multiple banks enables application cases such as:

- Dual-image firmware updates (an application can execute code out of one flash bank while a second image is programmed to a second symmetrical flash bank without stalling the application execution)
- EEPROM emulation (an application can execute code out of one flash bank while a second flash bank is used for writing data without stalling the application execution)

3.5.2.2 Flash Memory Regions

The memory within each bank is mapped to one or more logical regions based upon the functions that the memory in each bank supports. There are three regions: FACTORY, NONMAIN (Configuration NVM), and MAIN (Flash Memory).

The NONMAIN and FACTORY regions are assigned to the peripheral address space (0x6000_0000) as the memory does not contain any executable code. The CPU can not fetch executable instructions from this region.

The MAIN region is assigned to both the code address space (0x0000_0000) and the peripheral address space (0x6000_0000). Instruction and data fetches are recommended to always be done through the code address space as this gives the best performance. The CPU can not fetch executable instructions from this region.

Table 3-23. Flash Memory Regions

Flash Memory Region	Region Contents	Executable	Used by	Programmed by
FACTORY	Device ID and other parameters	No	Boot ROM Application	TI Only (Read-Only)
NONMAIN (Configuration NVM)	Device boot configuration (BCR and BSL)	No	Boot ROM	TI, User
MAIN (Flash Memory)	Application code and data	Yes	Application	User

The AM13E232x has two flash banks. Devices with mutliple banks implement FACTORY, NONMAIN, and MAIN regions on BANK0, but include additional banks (BANK1 through BANKx) that can implement MAIN regions.

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All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software.

3.5.2.3 Error Correction Code (ECC)

For error correction code (ECC) support, the ECC codes for all memory regions are also assigned to an address space and software can read the ECC codes as data for diagnostic purposes. It is also possible to read the contents of any of the memory regions without ECC correction applied.

Table 3-24. Flash Region ECC

Region	Read Type	ECC Behavior	Base Address
NONMAIN	Data read	Corrected	0x6010.0000
		ECC code	0x6026.0000
MAIN	Instruction fetch or data read	Corrected	0x0000.0000
	Data read	ECC code	0x6020.0000
FACTORY	Data read	Corrected	0x6011.1000
		ECC code	0x6027.0200

3.5.2.4 Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software.

Key data provided in the FACTORY memory region includes:

- The device unique 96-bit identity
- The default BSL pins
- The total MAIN region flash memory size (in KB)
- The flash bank count
- The total SRAM memory size (in KB)
- The temperature sensor calibration value
- The SYSPLL startup parameters

3.5.2.5 Boot Configuration

After a BOOTRST, the device executes the start-up boot routines to configure the device for operation before starting the main application. Boot routines are executed from read-only memory (ROM) before the main application is started. There are two boot routines: the Boot Configuration Routine (BCR) and Bootstrap Loader (BSL). The boot configuration routine sets up the device security policies, configures the device for operation, and optionally starts the BSL if it presents. The BSL, if started by the BCR, can be used to program or verify the device memory (flash and SRAM) through the use of a standard serial interface (UART, I2C, or MCAN).

After the start-up routines have successfully completed execution, the CPU is reset and the application is started by unconditionally fetching the stack pointer (SP) and reset vector from 0x0000.0000 and 0x0000.0004 of the flash memory for non-secure boot devices. To enable secure boot, a signed application image contains the SP and reset vector in the header which is interpreted by the ROM and updated in the GSC VTOR location.

3.5.2.6 Flash Wait States

Refer to the *Recommended Operation Conditions* section of the device specific data sheet to determine the max clock frequency supported for valid wait state configurations.

Additional details can be found in the FLASH chapter.

3.5.2.7 Flash Bank Address Swap

Devices with multiple flash banks provide a mechanism for swapping the address space of the upper banks with the address space of the lower banks to enable firmware updates, where the firmware image has no knowledge of the containing memory bank, to be able to execute properly on the hardware.

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To swap the addresses of the upper flash banks with the addresses of the lower flash banks, set the USEUPPER bit in the FLBANKSWAP register while also writing the KEY value.

Special care must be taken when swapping the flash bank address space. See the nonvolatile memory system chapter for additional considerations when using flash bank address swapping.

3.5.3 Memory Configuration

On AM13E232x devices, the MEMCFG registers control the configurations of the RAM and ROM. Some of the key features of the MEMCFG registers are:

1. Configuring SRAM for write access based on ECC or data bits
2. Configuring Wait-States on SRAM based on the SRAM bank
3. Configuring Wait-States on ROM

3.6 Resets and Device Initialization

The SYSCTL manages device reset levels and device initialization.

3.6.1 Reset Levels

The device has five reset levels:

1. Power-On Reset (POR)
2. Brownout Reset (BOR)
3. Boot Reset (BOOTRST)
4. System Reset (SYSRST)
5. CPU Reset (CPURST)

The general flow and relationship between reset levels is provided in the diagram below.

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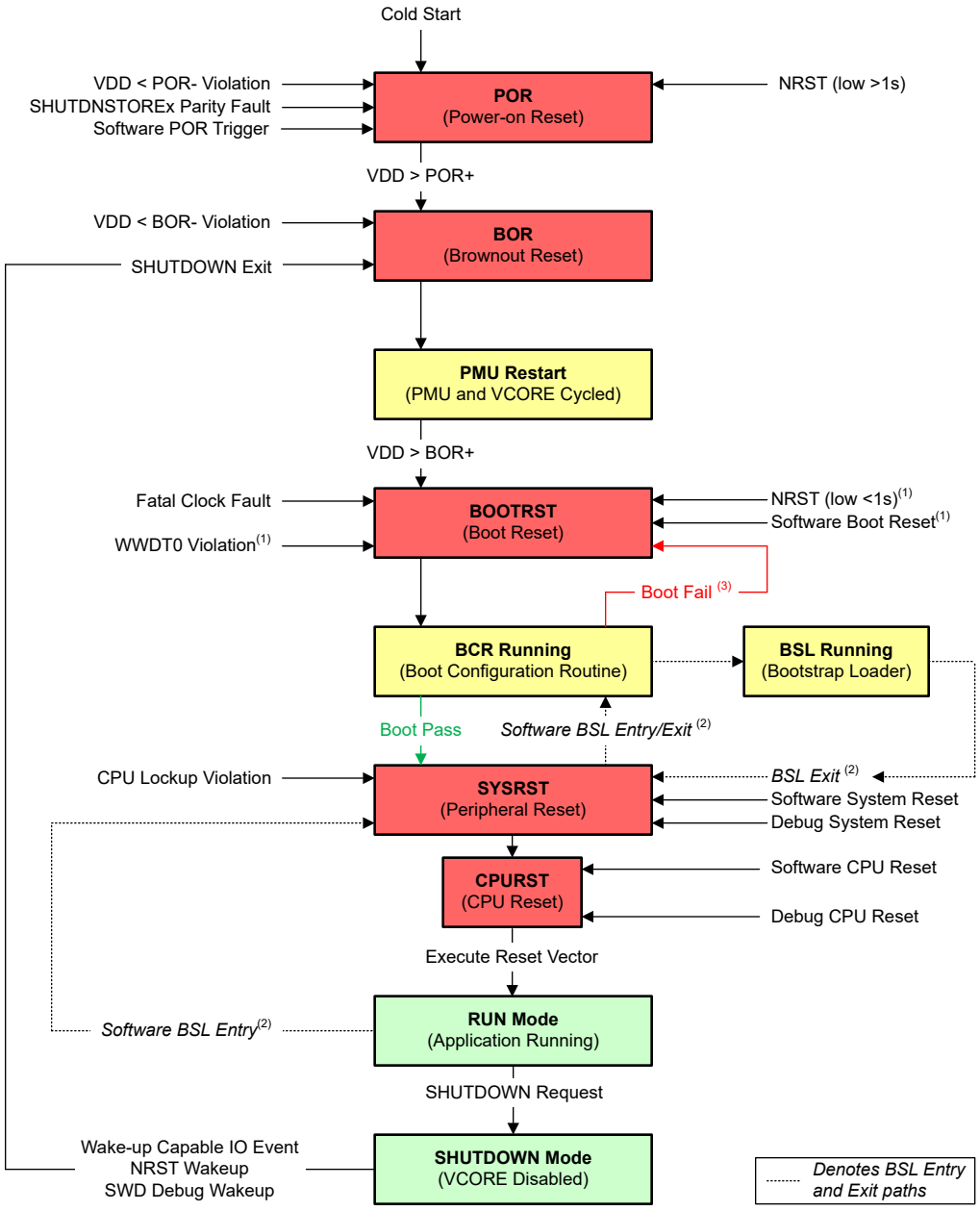


Figure 3-10. Device Reset Levels

(1)An NRST (low <1 s), software boot reset, or WWDT0 violation triggered BOOTRST runs the boot configuration routine.

(2)A software-triggered bootstrap loader (BSL) entry command first triggers a SYSRST, after which the boot configuration routine (BCR) is run to authenticate the BSL entry before starting the BSL. After the BSL execution concludes, a SYSRST is generated and the BCR executes again. When the BCR completes, a final SYSRST is issued and the application is started.

(3)If a boot fail occurs during execution of the boot configuration routine, a BOOTRST can be generated by SYSCTL to attempt the boot process again from the BOOTRST level.

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Note

SLEEP, STOP, and STANDBY operating modes are not shown in this diagram. These modes originate from and return to RUN mode unless an exception occurs which causes a reset level to be asserted or a mode to be suspended.

3.6.1.1 Power-on Reset (POR) Reset Level

A power-on reset (POR) is a complete device reset.

The following conditions generate a POR:

- The device powers up (cold start)
- A POR-supply monitor violation(VDD drops below the POR supply monitor negative-going threshold)
- A parity fault on PMU trim data or the shutdown memory
- Software triggers a POR through SYSCTL *(RESETLEVEL 0x03)*
- The NRST pin is held low for more than one second when in NRST mode

A POR always resets the shutdown memory, re-enables the NRST/JTAG/SWD pin functions (if disabled), and triggers a BOR.

3.6.1.2 Brownout Reset (BOR) Reset Level

A brownout reset (BOR) resets the device power management unit (PMU). All regulated core logic powered from VCORE are power cycled.

The following conditions generate a BOR:

- A POR.
- A BOR- Supply Monitor Violation (VDD drops below the BOR- supply monitor lower threshold voltage level).
- An exit from SHUTDOWN mode (through a wakeup-capable IO, NRST, or SWD) if SHUTDOWN mode is active.

The following are not reset by a BOR:

- The shutdown memory (SHUTDNSTOREx) if SHUTDOWN mode is present in the device
- The NRST state, if disabled by software.
- The JTAG/SWD state, if disabled by software.
- The latched IO pin state, when SHUTDOWN mode is active, and the cause of the BOR is an exit from SHUTDOWN mode (see SHUTDOWN mode handling).

A BOR always asserts a BOOTRST when VDD > BOR+ (brownout supply monitor upper threshold voltage level).

3.6.1.3 Boot Reset (BOOTRST) Reset Level

A boot reset (BOOTRST) triggers execution of the device boot configuration routine and resets the majority of the core logic, system memory (SRAM), and SYSOSC FCL mode (if enabled).

The following conditions generate a BOOTRST:

- A BOR.
- A fatal clock failure (see *LFCLK Monitor* and *MCLK Monitor*).
- A WWDT0 violation.
- Software triggers a BOOTRST through SYSCTL*(RESETLEVEL 0x01)*
- The NRST pin is held low for longer than the minimum reset pulse time but less than one second when in NRST mode. Refer to the device data sheet for reset timing requirements.
- A BOOTRST followed by a boot failure (re-attempt of a failed boot sequence).
- RESET_OUT signal from the EtherCAT module

The following are not reset by a BOOTRST:

- The shutdown memory (SHUTDNSTOREx) if SHUTDOWN mode is present.
- The NRST disable state, if disabled by software.

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- The JTAG/SWD disable state, if disabled by software.

Following a BOOTRST, a SYSRST is always triggered upon successful completion of the boot configuration routine. If the boot configuration routine fails to complete successfully, a BOOTRST is again generated and the boot process is attempted again from the BOOTRST point. The boot process attempts to complete successfully up to 3 times, after which the device state locks until a BOR or POR reset occurs (see Section 3.6.8).

3.6.1.4 System Reset (SYSRST) Reset Level

A system reset clears the state of the CPU and all the peripherals, with the exceptions listed below.

The following conditions generate a SYSRST:

- A BOOTRST followed by a boot pass
- Software triggers a SYSRST with BSL entry through SYSCTL *(RESETLEVEL 0x02)*
- A bootstrap loader (BSL) exit (if present), which is always followed by execution of the boot configuration routine (BCR)
- A CPU lockup violation
- Software triggers a SYSRST through SYSCTL *(RESETLEVEL 0x00)*
- The debug subsystem triggers a system reset

The following are not reset by a SYSRST:

- The shutdown memory (SHUTDNSTOREx) (if present)
- The NRST state, if disabled by software
- The JTAG/SWD state, if disabled by software
- The SYSOSC frequency correction loop (FCL), if enabled by software

In most cases, the device is in RUN mode after a SYSRST, and the CPU executes the reset vector and begins execution of the application software.

There are exceptions to this:

- If the SYSRST was triggered with a BSL entry request, the BCR runs followed by the BSL.
- If the SYSRST was triggered due to a BSL exit request, the BCR runs, followed by an additional SYSRST, after which the application software starts.

3.6.1.5 CPU-only Reset (CPURST) Reset Level

A CPU-only reset clears the state of the CPU logic only. Peripheral states are not affected by a CPU reset. A CPU reset is only generated by software through the CPU AIRCR local register or by the debug subsystem.

3.6.2 Initial Conditions After Power-Up

After a POR, when the boot process completes, the initial device conditions are as follows:

- The NRST pin is always configured in NRST mode.
- JTAG IO are in JTAG mode. (TCK is pulled low, and TMS/TDI/TDO are pulled high.
- All other configurable I/O pins are high impedance (Hi-Z).
- Peripheral modules are disabled and reset as described in the related chapters of this manual.
- The device is in RUN operating mode.
- MCLK is sourced from the internal SYSOSC at base frequency (32MHz).
- LFCLK is sourced from the internal LFOSC
  - Note: LFOSC requires some time to start up before LFCLK can be used. Refer to the device data sheet for LFOSC timing requirements.
- SYSPLL is disabled.
- XTAL (Crystal Oscillator) is disabled.
- Any flash sectors configured to be write protected at boot are write protected.

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3.6.3 NRST Pin

NRST is a dedicated (functional) pin and must be high for the device to boot successfully. This is achieved with an internal pullup resistor on the NRST pin.

After the device is started, a low pulse on NRST <1 second in duration triggers a BOOTRST. If a low pulse on NRST is held for >= 1 second, a POR is triggered.

Note

NRST Low Pulse **< 1 Second** = **BOOTRST** (Boot Reset)

Note

NRST Low Pulse **>= 1 Second** = **POR** (Power-on Reset)

Additionally, the NRST pin has an associated glitch filter circuit which prevents low pulses less than a certain duration from resetting the device. Refer to the device data sheet for the glitch filter and pull-up resistor specifications.

3.6.4 SWD/JTAG Pins

There are four JTAG/SWD (Serial Wire Debug) pins present on all devices: JTDI, JTCK_SWCLK, JTMS_SWDIO, and JTDO_SWO.

After a cold start, the pins are configured in JTAG/SWD mode to allow a debug connection to be established.

- JTDI pin is configured in the IOMUX and the **pull-up** is enabled.
- JTDO_SWD pin is configured in the IOMUX and the pull resistor is **disabled**.
- JTMS_SWDIO pin is configured in the IOMUX and the **pull-up** is enabled.
- JTCK_SWCLK pin is configured in the IOMUX and the **pull-down** is enabled.

The user is able to re-configure the JTAG/SWD pins as general purpose IO (GPIO) or alternative mux mode signal in software to enable use of these pins in an application when debug support is no longer required. To disable SWD functionality, set the DISABLE bit in the SWDJCFG register along with the KEY. Then configure the IOMUX for the desired functionality.

After the JTAG/SWD pin functions are disabled, JTAG/SWD can only be re-enabled after a POR has occurred.

3.6.5 Generating Resets in Software

Software can generate a software POR, a software BOOTRST, a software SYSRST with bootstrap loader (BSL) entry, or a software SYSRST by issuing the appropriate command to SYSCTL. To issue a reset, first select the desired reset level in the RESETLEVEL register in SYSCTL. Then set the GO bit in the RESETCMD register along with the KEY value.

Table 3-25. Software Generated SYSCTL Reset Commands

LEVEL	Action
0x0	Software-triggered SYSRST
0x1	Software-triggerd BOOTRST
0x2	Software-triggered SYSRST with BSL entry
0x3	Software-triggered POR
0x4	Software-triggered CPURST

A CPU-only reset (CPURST) which does not reset the peripherals can also be triggered in software within the device CPU by setting the SYSRESETREQ bit in the AIRCR local CPU register. See the CPU Sub System chapter for more information.

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Starting the BSL From Software

The software-triggered BSL entry *(RESETLEVEL 0x02)* is a special case of the SYSRST which provides a mechanism for the application software to start the ROM bootstrap loader (BSL). Direct access to the bootloader code is disabled during normal software execution in RUN mode. When application software commands a software-triggered BSL entry *(RESETLEVEL 0x02)*, a SYSRST is generated first, followed by execution of the boot configuration routine (for authentication), after which the BSL is started (if the device security policy has enabled the BSL execution).

Once the BSL has completed execution, a second SYSRST is issued and the BCR is executed. When the BCR completes, a final SYSRST is asserted to return control of the system back to the application software.

If the BSL is disabled by the user configuration, and a software-triggered BSL entry is invoked, the device issues a standard SYSRST instead and returns control of the system back to the application software.

Any system configuration which is not reset by a SYSRST is maintained through this entire process.

3.6.6 Reset Cause

After a device reset occurs, the lowest level reset cause which occurred during reset processing is captured in hardware so that application software can interrogate the reason for the reset and take any appropriate action when starting the application. The lowest level reset cause is encoded into a 5-bit field in the reset cause register in SYSCTL. The contents of the reset cause register are always cleared upon a read, and return zero after being read if no reset has occurred after the read. The reset cause encoding is provided in the table below.

Table 3-26. Reset Cause Encoding

Reset				Device Modules Reset									
Reset Level	Cause ID		Reset Cause	NRST/JTAG/SWD Disables	SHUTDN STOREx	Core Regulator	Debug Subsystem	SRAM	BCR/BSL Execution	IOMUX	DMA, FLASHCTL, SYSCTL	Peripherals	CPU
N/A	0x00	0	No reset since last read										
POR	0x01	1	VDD < POR- Violation	R	R	R	R	R	R	R	R	R	R
			PMU Trim Parity Fault										
			SHUTDNSTOREx Parity Fault										
	0x02	2	NRST Pin Reset (=>1sec)	R	R	R	R	R	R	R	R	R	R
	0x03	3	Software-triggered POR	R	R	R	R	R	R	R	R	R	R
BOR	0x04	4	VDD < BOR- Violation			R	R	R	R	R	R	R	R
	0x05	5	Wake from SHUTDOWN			R	R	R	R	R(1)	R	R	R
	0x06-0x8	6-8	Reserved										
BOOTRST	0x09	9	Fatal Clock Fault					R	R	R	R	R	R
	0x0A-0x0B	10-11	Reserved										
	0x0C	12	NRST Pin Reset (< 1sec)					R	R	R(2)	R	R	R
	0x0D	13	Software-triggered BOOTRST					R	R	R(2)	R	R	R
	0x0E	14	WWDT0 Violation					R	R	R(2)	R	R	R
	0x0F	15	RESET_OUT from EtherCAT					R	R	R(2)	R	R	R
SYSRST	0x10	16	BSL Exit						R	R(2)	R(3)	R	R
	0x11	17	BSL Entry						R	R(2)	R(3)	R	R

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Table 3-26. Reset Cause Encoding (continued)

Reset				Device Modules Reset									
Reset Level	Cause ID		Reset Cause	NRST/JTAG/SWD Disables	SHUTDN STOREx	Core Regulator	Debug Subsystem	SRAM	BCR/BSL Execution	IOMUX	DMA, FLASHCTL, SYSCTL	Peripherals	CPU
	0x12-0x13	18-19	Reserved										
	0x14	20	Uncorrectable Flash ECC Error							R(2)	R(3)	R	R
	0x15	21	CPU Lockup Violation							R(2)	R(3)	R	R
	0x16-0x19	22-25	Reserved										
	0x1A	26	Debug-triggered SYSRST							R(2)	R(3)	R	R
	0x1B	27	Software-triggered SYSRST							R(2)	R(3)	R	R
CPURST	0x1C	28	Debug-triggered CPURST										R
	0x1D	29	Software-triggered CPURST										R
	0x1E-0x1F	30-31	Reserved										

(1) In the case of a SHUTDOWN mode exit, the IOMUX registers are always reset but the IOs retain the last state from the point of entry into SHUTDOWN until the user clears the RELEASE bit in the SHDNIOREL register in SYSCTL. This enables application software to be able to reconfigure IOMUX and any corresponding peripherals before releasing the IO after a SHUTDOWN exit. See shutdown mode handling and IOMUX wake.

(2) IOMUX is reset,

(3) The SYSOSC frequency correction loop (FCL) is not reset (if enabled by software)

If two reset causes occur simultaneously, the lowest cause reset ID value is prioritized and reported. For example, if a WWDT0 violation (cause 0x0E) occurs at the same time that a VDD < BOR- violation (cause 0x04) occurs, the reported reset cause is a BOR- violation (cause 0x04), as this is a lower level reset which clears additional aspects of the device state.

The reset cause encoding enables simple software handling during application startup. The reset cause value can be read by application software and tested to be within a certain value range to determine if the following occurred:

- **RESETCAUSE == 0x00:** No reset since last read
- **RESETCAUSE < 0x04:** The NRST/JTAG/SWD disable state is reset and must be reconfigured.
- **RESETCAUSE < 0x04:** The SHUTDNSTOREx memory is reset and must be reconfigured.
- **RESETCAUSE < 0x08:** The regulated VCORE domain and id power cycled. The SRAM is reinitialized and the contents are lost.
- **RESETCAUSE < 0x1C:** The peripherals are reset and must be reconfigured.

3.6.7 Peripheral Reset Control

Most peripherals on the AM13E232x contain a reset control register (RSTCTL) and a status register (STAT). For some peripherals, these registers are contained in SYSCTL, and for others they are in the peripheral-specific register set.

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Note

Check Section 3.1.3 to see where the RSTCTL and STAT registers for a given peripheral are located on this device.

The STAT register is a read-only register which contains a RESETSTKY bit, indicating if the peripheral was reset. This bit can be read by application software to determine if a peripheral was reset and needs to be re-configured. The RESETSTKY bit is cleared by writing the RESETSTKYCLR bit together with the KEY value to the RSTCTL register.

Application software can also force a reset of the peripheral by writing the RESETASSERT bit together with the KEY value to the RSTCTL register. This action resets the peripheral to the default state and sets the RESETSTKY bit in the STAT register.

3.6.8 Boot Fail Handling

If a boot fails during execution of the boot configuration routine (BCR), SYSCTL asserts a BOOTRST to attempt another boot. A boot fail can be caused by the following:

- Boot configuration data integrity error
- Device trim integrity error
- BCR timeout (BCR takes significantly longer than expected to complete for any other reason)

Up to three attempts to successfully boot the device are made by hardware. If the first, second, or third boot attempt is successful, the application starts normally. If the third attempt fails, then the boot process fails, no further boot attempts are made, and the application software is not started.

The purpose of the additional boot attempts is to allow the device to boot correctly if a transient (temporary) error was the cause of the boot fail. If three boot attempts are not successful, a steady-state error condition is likely present and the application is not started to prevent unexpected operation.

Note

If a device is locked due to three failed attempts to boot, and a BOR- violation occurs, a BOR and BOOTRST are still generated (by definition) and a single boot attempt is made. Under the same conditions, if power is completely removed from the device (triggering a POR- violation), then the device again attempts to boot up to three times.

3.7 System Status and Error Handling

3.7.1 System Status

The status of various aspects of the system controller can be polled by software by reading the CLKSTATUS and SYSSTATUS SYSCTL registers.

Checking Clock Status (CLKSTATUS)

The CLKSTATUS register in SYSCTL is a read-only register which indicates the current configuration and status of the clock module. Key status information provided in CLKSTATUS includes:

- The current SYSOSC frequency
- The current HSCLK selection
- The current MCLK selection
- The HFCLK and SYSPLL status
- The LFOSC status
- Indications that the HSCLK, HFCLK, and SYSPLL are disabled
- Error indications if a peripheral requested a clock and the clock cannot be generated

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This status information is useful to validate that a requested clock change has completed successfully, or to check the true SYSOSC frequency in applications where SYSOSC can have asynchronous activation or frequency requests issued by peripherals.

Checking System Status (SYSSTATUS)

The SYSSTATUS register in SYSCTL is a read-only register which indicates flash ECC errors (SED and DED) along with other peripheral-specific status information. ECC error bits in SYSSTATUS are sticky (bits remain set when an ECC error occurs even if future reads do not have errors). These bits can be reset (cleared) by setting the ALLECC bit in the SYSSTATUSCLR register along with the KEY value.

3.7.2 Error Handling

The device includes several diagnostic mechanism to detect errors at runtime. The table below lists the error sources and corresponding handling mechanism.

Note

Not all devices support all diagnostic features. For example, some devices do not have ECC/parity on memories and some devices do not have dual watchdog timers. Always refer to the device-specific data sheet to understand which diagnostic features are available for a given device.

Table 3-27. Error Sources and Handling Mechanisms

Error Source	Error	Handling Mechanism
Flash	Non-correctable ECC Error	• For a CPU or DMA request, a FLASHDED nonmaskable interrupt is generated to the processor or a SYSRST is generated depending on configuration of the FLASHECCRSTDIS bit. • The FLASHDED sticky bit is set in the SYSSTATUS register in SYSCTL.
	Correctable ECC Error	• A FLASHSEC interrupt is also generated in SYSCTL. • The FLASHSEC sticky bit is set in the SYSSTATUS register in SYSCTL.
SRAM	Parity error	• Nonmaskable interrupt is generated to the processor if from CPU request. • DMA data error interrupt is generated if from DMA request.
	Address error on CPU access	• A hard fault is generated in the CPU.
	Address error on DMA access	• A DMA address error interrupt is generated in the DMA controller.
	ECC error on CAN SRAM	• An interrupt is generated in the MCAN peripheral.
SHUTDNSTORExMemory	Parity error	• A POR is generated.
CKM	MCLK failure	• A BOOTRST is generated.
CPUSS	Memory protection unit violation	• A hard fault is generated in the CPU.
WWDT	WWDT0 violation	• A BOOTRST is generated or a nonmaskable interrupt is generated in the SYSCTL NMI registers depending on configuration of the WWDTLP0RSTDIS bit.
PMU	Trim parity error	• A POR is generated.
	POR0- supply error	• A POR is generated.
	BOR- supply error	• A BOR is generated.
CPUSS	Memory protection unit violation (if present)	• A hard fault is generated in the CPU.

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Configurable NMI Triggers

Error sources can be configured to trigger either a nonmaskable interrupt (NMI) or a different handling mechanism. The SYSTEMCFG register in SYSCTL can be used to specify the desired error handling mechanism. For example, the WWDT0 can be configured to generate either a BOOTRST (default) or an NMI. Refer to the relevant SYSTEMCFG register for the available error handling options.

3.8 Configuration Lockout

Configuration registers in SYSCTL can be locked out from writes to add a layer of robustness against unintended changes at runtime. To lock out the configuration registers from writes, set the ACTIVE bit in the WRITELOCK register in SYSCTL.

All SYSCTL registers are protected by the WRITELOCK functionality except for those listed below:

- WRITELOCK
- PMODECFG
- FCC, FCCCMD
- FLBANKSWAP
- RSTCAUSE (read-to-clear), RESETLEVEL, RESETCMD
- SHDNIOREL
- SHUTDNSTOREx

In addition to the overall SYSCTL configuration write lock feature, many SYSCTL registers also require a KEY value to be written in conjunction with the desire configuration data for the write to take effect.

3.9 SYSCTL Interrupts & Triggers

3.9.1 CPU Interrupt (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 3-28. CPU Interrupts Triggered by SYSCTL

NVIC Interrupt Name	Peripheral Instance Name	Register Group	SYSCTL Interrupt Configuration Registers	Description
SYSCTL	SYSCTL	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	SYSCTL interrupt. Multiple OR'd, configurable source condition.

3.9.2 CPU Non-Maskable Interrupts (NMIs)

The SYSCTL module provides nonmaskable interrupt sources which can be configured to source a nonmaskable interrupt event (NMI), see Section 4.3.2 for more information.

Table 3-29. CPU Non-Maskable Interrupts Triggered by SYSCTL

NMI Interrupt Name	Peripheral Instance Name	Register Group	SYSCTL NMI Interrupt Configuration Registers	Description
SYSCTL	SYSCTL	N/A	NMIIIDX, NMIRIS, NMIISET, NMIICLR	SYSCTL NMI interrupt. Multiple source conditions. All conditions are always enabled.

3.10 SYSCTL Registers

This Section describes the SYSCTL Registers.

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3.10.1 SYSCTL Base Address Table

Table 3-30. SYSCTL Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
SysctlRegs	SYSCTL_REGS	SYSCTL	0x400A_F000

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3.10.2 SYSCTL_REGS Registers

Table 3-31 lists the memory-mapped registers for the SYSCTL_REGS registers. All register offset addresses not listed in Table 3-31 should be considered as reserved locations and the register contents should not be modified.

Table 3-31. SYSCTL_REGS Registers

Offset	Acronym	Register Name	Group	Section
1020h	IIDX	SYSCTL interrupt index		Go
1028h	IMASK	SYSCTL interrupt mask		Go
1030h	RIS	SYSCTL raw interrupt status		Go
1038h	MIS	SYSCTL masked interrupt status		Go
1040h	ISET	SYSCTL interrupt set		Go
1048h	ICLR	SYSCTL interrupt clear		Go
1050h	NMIIIDX	NMI interrupt index		Go
1060h	NMIRIS	NMI raw interrupt status		Go
1070h	NMIISET	NMI interrupt set		Go
1078h	NMIICLR	NMI interrupt clear		Go
1100h	SYSOSCCFG	SYSOSC configuration		Go
1104h	MCLKCFG	Main clock (MCLK) configuration		Go
1108h	HSCLKEN	High-speed clock (HSCLK) source enable/disable		Go
110Ch	HSCLKCFG	High-speed clock (HSCLK) source selection		Go
1110h	HFCLKCLKCFG	High-frequency clock (HFCLK) configuration		Go
1120h	SYSPLLCFG0	SYSPLL reference and output configuration		Go
1124h	SYSPLLCFG1	SYSPLL reference and feedback divider		Go
1128h	SYSPLLPARAM0	SYSPLL PARAM0 (load from FACTORY region)		Go
112Ch	SYSPLLPARAM1	SYSPLL PARAM1 (load from FACTORY region)		Go
1130h	SYSPLLPARAM2	SYSPLL PARAM2 (load from FACTORY region)		Go
1134h	SYSPLLLDOCTL	SYSPLL LDO CTL (load from FACTORY region)		Go
1138h	SYSPLLLDOPROG	SYSPLL LDO VOUT PROG (load from FACTORY region)		Go
113Ch	GENCLKEN	General clock enable control		Go
1140h	GENCLKCFG	General clock configuration		Go
1144h	PMODECFG	Power mode configuration		Go
1148h	MLDOLPENCFG	LDO Configuration Control		Go
1150h	FCC	Frequency clock counter (FCC) count		Go
1180h	SYSTEMCFG	System configuration		Go
1184h	SRAMCFG	System SRAM configuration		Go
1200h	WRITELOCK	SYSCTL register write lockout		Go
1204h	CLKSTATUS	Clock module (CKM) status		Go
1208h	SYSSTATUS	System status information		Go
1220h	RSTCAUSE	Reset cause		Go
1300h	RESETLEVEL	Reset level for application-triggered reset command		Go
1304h	RESETCMD	Execute an application-triggered reset command		Go
1310h	SYSOSCFCLCTL	SYSOSC frequency correction loop (FCL) ROSC enable		Go
131Ch	SHDNIOREL	SHUTDOWN IO release control		Go
1320h	EXRSTPIN	Disable the reset function of the NRST pin		Go
1324h	SYSSTATUSCLR	Clear sticky bits of SYSSTATUS		Go

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Table 3-31. SYSCTL_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1328h	SWDJCFG	Disable the SWD/JTAG function on the SWD/JTAG pins		Go
132Ch	FCCCMD	Frequency clock counter start capture		Go
1400h	SHUTDNSTORE0	Shutdown storage memory (byte 0)		Go
1404h	SHUTDNSTORE1	Shutdown storage memory (byte 1)		Go
1408h	SHUTDNSTORE2	Shutdown storage memory (byte 2)		Go
140Ch	SHUTDNSTORE3	Shutdown storage memory (byte 3)		Go
1410h	ADCSEQFRCGB	ADC Global Sequence Force		Go
1414h	ADCSEQFRCGBSEL	ADC Global Sequence Force Select		Go
1418h	M33SPARESOCLOCK1	M33C1 Spare SOC LOCK Reg 1		Go
141Ch	M33SPARESOCLOCK2	M33C1 Spare SOC LOCK Reg 2		Go
1420h	SYSCTL_READ_REG	Sysctl read only Reg		Go
1424h	PWREN_MCPERIPH	Register to control the power state		Go
1428h	RSTCTL_ASSERT_MCPERIPH	rstctl assert register to control reset assertion - Write Only Register, Always Read as 0		Go
142Ch	RSTCTL_CLEAR_MCPERIPH	rstctl clear register to control reset de-assertion - Write Only Register, Always Read as 0		Go
1430h	STAT_MCPERIPH	IP State Register - Read Only		Go
1434h	PWREN_SYSPERIPH	Register to control the power state		Go
1438h	RSTCTL_ASSERT_SYSPERIPH	rstcl assert Register - Write Only Register, Always Read as 0		Go
143Ch	RSTCTL_CLEAR_SYSPERIPH	rstctl clear register to control reset de-assertion - Write Only Register, Always Read as 0		Go
1440h	STAT_SYSPERIPH	IP State Register - Read Only		Go
1444h	CMPHPMXSEL	Bits to select one of the many sources on CompHP inputs. Refer to Pinmux diagram for details.		Go
144Ch	CMPLPMXSEL	Bits to select one of the many sources on CompLP inputs. Refer to Pinmux diagram for details.		Go
1450h	CMPHNMXSEL	Bits to select one of the many sources on CompHN inputs. Refer to Pinmux diagram for details.		Go
1454h	CMPLNMXSEL	Bits to select one of the many sources on CompLN inputs. Refer to Pinmux diagram for details.		Go
1458h	TSNSCFG	Temperature Sensor Config Register		Go
145Ch	TSNSSCTL	Temperature Sensor Control Register		Go
1468h	INTERNALTESTCTL	Internal Test Node Control Register		Go
1474h	XTALCR	XTAL Control Register		Go
1478h	XTALCR2	XTAL Control Register for pad init		Go
147Ch	X1CNT	x1cnt status register		Go
1480h	CMPSSCTL	CMPSS control register		Go
1488h	ANAREFCTL	Analog Reference Select		Go
148Ch	PERCLKCR	PWM Time Base Clock sync		Go
14A0h	AM13SPAREIREFENSOCLOCK	AM13 Spare IREFEN SOC LOCK Reg		Go
14A4h	AM13SPARESOCLOCK2	AM13 Spare SOC LOCK Reg 2		Go
14A8h	AM13SPARESOCLOCK3	AM13 Spare SOC LOCK Reg 3		Go
14ACh	AM13SPARESOCLOCK4	AM13 Spare SOC LOCK Reg 4		Go

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Table 3-31. SYSCTL_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
14B0h	ETHERCATCLKCTL	EtherCAT Clock Control		Go
14B4h	ETHERCATCTL	ETHERCAT control register		Go
14B8h	SDFMTYPE	Configures SDFM type for the device		Go
3038h	FLBANKSWPPOLICY	Flash Bank Swap Policy		Go
303Ch	FLBANKSWP	Flash MAIN bank address swap		Go
3048h	SECSTATUS	Security Configuration status		Go
3060h	INITDONE	INITCODE PASS		Go

Complex bit access types are encoded to fit into small table cells. Table 3-32 shows the codes that are used for access types in this section.

Table 3-32. SYSCTL_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

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1 IIDX Register (Offset = 1020h) [Reset = 00000000h]

IIDX is shown in Figure 3-11 and described in Table 3-33.

Return to the Summary Table.

SYSCTL interrupt index

Figure 3-11. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STAT		
R-0h													R-0h		

Table 3-34. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	STAT	R	0h	The SYSCTL interrupt index (IIDX) register generates a value corresponding to the highest priority pending interrupt source. This value may be used as an address offset for fast, deterministic handling in the interrupt service routine. A read of the IIDX register will clear the corresponding interrupt status in the RIS and MIS registers. 0h = No interrupt pending 1h = LFOSCGOOD interrupt pending 2h = ANACLKERR interrupt pending 3h = FLASHSEC interrupt pending 4h = Reserved 5h = HFCLKGOOD interrupt pending 6h = SYSPLLGOOD interrupt pending 7h = HSCLKGOOD interrupt pending

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2 IMASK Register (Offset = 1028h) [Reset = 00000000h]

IMASK is shown in Figure 3-12 and described in Table 3-34.

Return to the Summary Table.

SYSCTL interrupt mask

Figure 3-12. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	HSCLKGOOD	SYSPLLGOOD	HFCLKGOOD	RESERVED	FLASHSEC	RESERVED	LFOSCGOOD
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-36. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6	HSCLKGOOD	R/W	0h	HSCLK GOOD 0h = 0 1h = 1
5	SYSPLLGOOD	R/W	0h	SYSPLL GOOD 0h = 0 1h = 1
4	HFCLKGOOD	R/W	0h	HFCLK GOOD 0h = 0 1h = 1
3	RESERVED	R/W	0h	Reserved
2	FLASHSEC	R/W	0h	Flash Single Error Correct 0h = 0 1h = 1
1	RESERVED	R/W	0h	Reserved
0	LFOSCGOOD	R/W	0h	Enable or disable the LFOSCGOOD interrupt. LFOSCGOOD indicates that the LFOSC has started successfully. 0h = Interrupt disabled 1h = Interrupt enabled

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3 RIS Register (Offset = 1030h) [Reset = 00000000h]

RIS is shown in Figure 3-13 and described in Table 3-35.

Return to the Summary Table.

SYSCTL raw interrupt status

Figure 3-13. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	HSCLKGOOD	SYSPLLGOOD	HFCLKGOOD	RESERVED	FLASHSEC	RESERVED	LFOSCGOOD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-38. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6	HSCLKGOOD	R	0h	HSCLK GOOD 0h = 0 1h = 1
5	SYSPLLGOOD	R	0h	SYSPLL GOOD 0h = 0 1h = 1
4	HFCLKGOOD	R	0h	HFCLK GOOD 0h = 0 1h = 1
3	RESERVED	R	0h	Reserved
2	FLASHSEC	R	0h	Flash Single Error Correct 0h = 0 1h = 1
1	RESERVED	R	0h	Reserved
0	LFOSCGOOD	R	0h	Raw status of the LFOSCGOOD interrupt. 0h = No interrupt pending 1h = Interrupt pending

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4 MIS Register (Offset = 1038h) [Reset = 00000000h]

MIS is shown in Figure 3-14 and described in Table 3-36.

Return to the Summary Table.

SYSCTL masked interrupt status

Figure 3-14. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	HSCLKGOOD	SYSPLLGOOD	HFCLKGOOD	RESERVED	FLASHSEC	RESERVED	LFOSCGOOD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-40. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6	HSCLKGOOD	R	0h	HSCLK GOOD 0h = 0 1h = 1
5	SYSPLLGOOD	R	0h	SYSPLL GOOD 0h = 0 1h = 1
4	HFCLKGOOD	R	0h	HFCLK GOOD 0h = 0 1h = 1
3	RESERVED	R	0h	Reserved
2	FLASHSEC	R	0h	Flash Single Error Correct 0h = 0 1h = 1
1	RESERVED	R	0h	Reserved
0	LFOSCGOOD	R	0h	Masked status of the LFOSCGOOD interrupt. 0h = No interrupt pending 1h = Interrupt pending

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5 ISET Register (Offset = 1040h) [Reset = 00000000h]

ISET is shown in Figure 3-15 and described in Table 3-37.

Return to the Summary Table.

SYSCTL interrupt set

Figure 3-15. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED	HSCLKGOOD	SYSPLLGOOD	HFCLKGOOD	RESERVED	FLASHSEC	RESERVED	LFOSCGOOD
W-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

Table 3-42. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	W	0h	
6	HSCLKGOOD	W1S	0h	HSCLK GOOD 0h = 0 1h = 1
5	SYSPLLGOOD	W1S	0h	SYSPLL GOOD 0h = 0 1h = 1
4	HFCLKGOOD	W1S	0h	HFCLK GOOD 0h = 0 1h = 1
3	RESERVED	W1S	0h	Reserved
2	FLASHSEC	W1S	0h	Flash Single Error Correct 0h = 0 1h = 1
1	RESERVED	W1S	0h	Reserved
0	LFOSCGOOD	W1S	0h	Set the LFOSCGOOD interrupt. 0h = Writing 0h has no effect 1h = Set interrupt

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6 ICLR Register (Offset = 1048h) [Reset = 00000000h]

ICLR is shown in Figure 3-16 and described in Table 3-38.

Return to the Summary Table.

SYSCTL interrupt clear

Figure 3-16. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED	HSCLKGOOD	SYSPLLGOOD	HFCLKGOOD	RESERVED	FLASHSEC	RESERVED	LFOSCGOOD
W-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

Table 3-44. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	W	0h	
6	HSCLKGOOD	W1C	0h	HSCLK GOOD 0h = 0 1h = 1
5	SYSPLLGOOD	W1C	0h	SYSPLL GOOD 0h = 0 1h = 1
4	HFCLKGOOD	W1C	0h	HFCLK GOOD 0h = 0 1h = 1
3	RESERVED	W1C	0h	Reserved
2	FLASHSEC	W1C	0h	Flash Single Error Correct 0h = 0 1h = 1
1	RESERVED	W1C	0h	Reserved
0	LFOSCGOOD	W1C	0h	Clear the LFOSCGOOD interrupt. 0h = Writing 0h has no effect 1h = Clear interrupt

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7 NMIIIDX Register (Offset = 1050h) [Reset = 00000000h]

NMIIIDX is shown in Figure 3-17 and described in Table 3-39.

Return to the Summary Table.

NMI interrupt index

Figure 3-17. NMIIIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												STAT			
R-0h																												R-0h			

Table 3-46. NMIIIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3-0	STAT	R	0h	The NMI interrupt index (NMIIIDX) register generates a value corresponding to the highest priority pending NMI source. This value may be used as an address offset for fast, deterministic handling in the NMI service routine. A read of the NMIIIDX register will clear the corresponding interrupt status in the NMIRIS register. 0h = No NMI pending 1h = Reserved 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7 8h = 8 9h = 9

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8 NMIRIS Register (Offset = 1060h) [Reset = 00000000h]

NMIRIS is shown in Figure 3-18 and described in Table 3-40.

Return to the Summary Table.

NMI raw interrupt status

Figure 3-18. NMIRIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							ECATRAMPAR
R-0h							R-0h
7	6	5	4	3	2	1	0
ECATRESETOUT	SYSMEMACC	TMUROMPAR	SRAMPAR	FLASHDED	SECURITY	WWDT0	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-48. NMIRIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	ECATRAMPAR	R	0h	ECATSS RAM Parity error 0h = 0 1h = 1
7	ECATRESETOUT	R	0h	ECATSS RESET out 0h = 0 1h = 1
6	SYSMEMACC	R	0h	SYSMEM Access error 0h = 0 1h = 1
5	TMUROMPAR	R	0h	TMU ROM Parity error 0h = 0 1h = 1
4	SRAMPAR	R	0h	SRAM Parity Error Detect 0h = 0 1h = 1
3	FLASHDED	R	0h	Flash Double Error Detect 0h = 0 1h = 1
2	SECURITY	R	0h	Security Fault 0h = 0 1h = 1
1	WWDT0	R	0h	Watch Dog 0 Fault 0h = 0 1h = 1
0	RESERVED	R	0h	Reserved

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9 NMIISET Register (Offset = 1070h) [Reset = 00000000h]

NMIISET is shown in Figure 3-19 and described in Table 3-41.

Return to the Summary Table.

NMI interrupt set

Figure 3-19. NMIISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							ECATRAMPAR
W-0h							W1S-0h
7	6	5	4	3	2	1	0
ECATRESETOUT	SYSMEMACC	TMUROMPAR	SRAMPAR	FLASHDED	SECURITY	WWDT0	RESERVED
W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h	W1S-0h

Table 3-50. NMIISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	W	0h	
8	ECATRAMPAR	W1S	0h	ECATSS RAM Parity error 0h = 0 1h = 1
7	ECATRESETOUT	W1S	0h	ECATSS RESET out 0h = 0 1h = 1
6	SYSMEMACC	W1S	0h	SYSMEM Access error 0h = 0 1h = 1
5	TMUROMPAR	W1S	0h	TMU ROM Parity error 0h = 0 1h = 1
4	SRAMPAR	W1S	0h	SRAM Parity Error Detect 0h = 0 1h = 1
3	FLASHDED	W1S	0h	Flash Double Error Detect 0h = 0 1h = 1
2	SECURITY	W1S	0h	Security Fault 0h = 0 1h = 1
1	WWDT0	W1S	0h	Watch Dog 0 Fault 0h = 0 1h = 1
0	RESERVED	W1S	0h	Reserved

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10 NMIICLR Register (Offset = 1078h) [Reset = 00000000h]

NMIICLR is shown in Figure 3-20 and described in Table 3-42.

Return to the Summary Table.

NMI interrupt clear

Figure 3-20. NMIICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							ECATRAMPAR
W-0h							W1C-0h
7	6	5	4	3	2	1	0
ECATRESETOUT	SYSMEMACC	TMUROMPAR	SRAMPAR	FLASHDED	SECURITY	WWDT0	RESERVED
W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h	W1C-0h

Table 3-52. NMIICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	W	0h	
8	ECATRAMPAR	W1C	0h	ECATSS RAM Parity error 0h = 0 1h = 1
7	ECATRESETOUT	W1C	0h	ECATSS RESET out 0h = 0 1h = 1
6	SYSMEMACC	W1C	0h	SYSMEM Access error 0h = 0 1h = 1
5	TMUROMPAR	W1C	0h	TMU ROM Parity error 0h = 0 1h = 1
4	SRAMPAR	W1C	0h	SRAM Parity Error Detect 0h = 0 1h = 1
3	FLASHDED	W1C	0h	Flash Double Error Detect 0h = 0 1h = 1
2	SECURITY	W1C	0h	Security Fault 0h = 0 1h = 1
1	WWDT0	W1C	0h	Watch Dog 0 Fault 0h = 0 1h = 1
0	RESERVED	W1C	0h	Reserved

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11 SYSOSCCFG Register (Offset = 1100h) [Reset = 0002XXXXh]

SYSOSCCFG is shown in Figure 3-21 and described in Table 3-43.

Return to the Summary Table.

SYSOSC configuration

Figure 3-21. SYSOSCCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						FASTCPUEVENT	BLOCKASYNCALL
R/W-0h						R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED					DISABLE	RESERVED	RESERVED
R/W-Xh					R-0h	R-0h	R-1h
7	6	5	4	3	2	1	0
RESERVED						FREQ	
R/W-Xh						R/W-0h	

Table 3-54. SYSOSCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	0h	
17	FASTCPUEVENT	R/W	1h	if disabled CPU will not wakeup and continue in STANDBY 0h = An interrupt to the CPU will not assert a fast clock request 1h = An interrupt to the CPU will assert a fast clock request
16	BLOCKASYNCALL	R/W	0h	BLOCKASYNCALL may be used to mask block all asynchronous fast clock requests, preventing hardware from dynamically changing the active clock configuration when operating in a given mode. 0h = Asynchronous fast clock requests are controlled by the requesting peripheral 1h = All asynchronous fast clock requests are blocked
15-11	RESERVED	R/W	Xh	
10	DISABLE	R	0h	DISABLE sets the SYSOSC enable/disable policy. SYSOSC may be powered off in RUN, SLEEP, and STOP modes to reduce power consumption. When SYSOSC is disabled, MCLK and ULPCLK are sourced from LFCLK. 0h = Do not disable SYSOSC 1h = Disable SYSOSC immediately and source MCLK and ULPCLK from LFCLK
9	RESERVED	R	0h	Reserved
8	RESERVED	R	1h	Reserved
7-2	RESERVED	R/W	Xh	
1-0	FREQ	R/W	0h	Target operating frequency for the system oscillator (SYSOSC) 0h = Base frequency (32MHz) 1h = Low frequency (4MHz)

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12 MCLKCFG Register (Offset = 1104h) [Reset = 07XXX2X0h]

MCLKCFG is shown in Figure 3-22 and described in Table 3-44.

Return to the Summary Table.

Main clock (MCLK) configuration

Figure 3-22. MCLKCFG Register

31	30	29	28	27	26	25	24
RESERVED					MCLKDIVCFG		
R/W-0h					R/W-7h		
23	22	21	20	19	18	17	16
RESERVED	MCLKDEADCHK	STOPCLKSTBY	USELFCLK	RESERVED			USEHSCLK
R/W-Xh	R/W-0h	R/W-0h	R-0h	R/W-Xh			R/W-0h
15	14	13	12	11	10	9	8
RESERVED			RESERVED	RESERVED			
R/W-Xh			R/W-0h	R/W-2h			
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-Xh				R-0h			

Table 3-56. MCLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	0h	
26-24	MCLKDIVCFG	R/W	7h	MCLK Divider Configuration bits [1:0] are defined as MCLK4 is Bypass, MCLK2 is Bypass 0h = MCLK: No Divide, MCLK2: No Divide, MCLK4: No Divide 1h = MCLK: No Divide, MCLK2: No Divide, MCLK4: Divide MCLK by 2 3h = MCLK: No Divide, MCLK2: No Divide, MCLK4: Divide MCLK by 4 5h = MCLK: No Divide, MCLK2: Divide MCLK by 2, MCLK4: Divide MCLK by 2 7h = MCLK: No Divide, MCLK2: Divide MCLK by 2, MCLK4: MCLK by 4
23	RESERVED	R/W	Xh	
22	MCLKDEADCHK	R/W	0h	MCLKDEADCHK enables or disables the continuous MCLK dead check monitor. LFCLK must be running before MCLKDEADCHK is enabled. 0h = The MCLK dead check monitor is disabled 1h = The MCLK dead check monitor is enabled
21	STOPCLKSTBY	R/W	0h	STOPCLKSTBY sets the STANDBY mode policy (STANDBY0 or STANDBY1). When set, ULPCLK and LFCLK are disabled to all peripherals in STANDBY mode, with the exception of TIMG0 and TIMG1 which continue to run. Wake-up is only possible via an asynchronous fast clock request. 0h = ULPCLK/LFCLK runs to all PD0 peripherals in STANDBY mode 1h = ULPCLK/LFCLK is disabled to all peripherals in STANDBY mode except TIMG0 and TIMG1
20	USELFCLK	R	0h	LFCLK is not an MCLK sourcei in PD1, tied 0. 0h = MCLK will not use the low frequency clock (LFCLK) 1h = MCLK will use the low frequency clock (LFCLK)
19-17	RESERVED	R/W	Xh	

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Table 3-56. MCLKCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	USEHSCLK	R/W	0h	USEHSCLK, together with USELFCLK, sets the MCLK source policy. Set USEHSCLK to use HSCLK (HFCLK or SYSPLL) as the MCLK source in RUN and SLEEP modes. 0h = MCLK will not use the high speed clock (HSCLK) 1h = MCLK will use the high speed clock (HSCLK) in RUN and SLEEP mode
15-13	RESERVED	R/W	Xh	
12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	2h	Reserved
7-4	RESERVED	R/W	Xh	
3-0	RESERVED	R	0h	Reserved

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13 HSCLKEN Register (Offset = 1108h) [Reset = 0000XXXXh]

HSCLKEN is shown in Figure 3-23 and described in Table 3-45.

Return to the Summary Table.

High-speed clock (HSCLK) source enable/disable

Figure 3-23. HSCLKEN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							USEEXTHFCLK
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							SYSPLLEN
R/W-Xh							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-Xh							R/W-0h

Table 3-58. HSCLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	0h	
16	USEEXTHFCLK	R/W	0h	USEEXTHFCLK selects the HFCLK_IN digital clock input to be the source for HFCLK. 0h = Use XTAL as the HFCLK source 1h = Use the HFCLK_IN digital clock input as the HFCLK source
15-9	RESERVED	R/W	Xh	
8	SYSPLLEN	R/W	0h	SYSPLLEN enables or disables the system phase-lock loop (SYSPLL). 0h = Disable the SYSPLL 1h = Enable the SYSPLL
7-1	RESERVED	R/W	Xh	
0	RESERVED	R/W	0h	Reserved

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14 HSCLKCFG Register (Offset = 110Ch) [Reset = 00000000h]

HSCLKCFG is shown in Figure 3-24 and described in Table 3-46.

Return to the Summary Table.

High-speed clock (HSCLK) source selection

Figure 3-24. HSCLKCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							HSCLKSEL
R/W-0h							R/W-0h

Table 3-60. HSCLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	HSCLKSEL	R/W	0h	HSCLKSEL selects the HSCLK source (SYSPLL or HFCLK). 0h = HSCLK is sourced from the SYSPLL 1h = HSCLK is sourced from the HFCLK

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15 HFCLKCLKCFG Register (Offset = 1110h) [Reset = 1XXXXX00h]

HFCLKCLKCFG is shown in Figure 3-25 and described in Table 3-47.

Return to the Summary Table.

High-frequency clock (HFCLK) configuration

Figure 3-25. HFCLKCLKCFG Register

31	30	29	28	27	26	25	24
RESERVED			HFCLKFLTCHK	RESERVED			
R/W-0h			R/W-1h	R/W-XXXh			
23	22	21	20	19	18	17	16
RESERVED							
R/W-XXXh							
15	14	13	12	11	10	9	8
RESERVED		RESERVED		RESERVED			
R/W-XXXh		R/W-0h		R/W-Xh			
7	6	5	4	3	2	1	0
XTALTIME							
R/W-0h							

Table 3-62. HFCLKCLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	HFCLKFLTCHK	R/W	1h	HFCLKFLTCHK enables or disables the HFCLK startup monitor. 0h = HFCLK startup is not checked 1h = HFCLK startup is checked
27-14	RESERVED	R/W	XXXh	
13-12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	Xh	
7-0	XTALTIME	R/W	0h	XTALTIME specifies the XTAL startup time in 64us resolution. If the HFCLK startup monitor is enabled (HFCLKFLTCHK), XTAL will be checked after this time expires. 0h = Minimum startup time (approximatly zero) FFh = Maximum startup time (approximatly 16.32ms)

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16 SYSPLLCFG0 Register (Offset = 1120h) [Reset = 000000XXh]

SYSPLLCFG0 is shown in Figure 3-26 and described in Table 3-48.

Return to the Summary Table.

SYSPLL reference and output configuration

Figure 3-26. SYSPLLCFG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RDIVCLK1				RDIVCLK0			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED	RESERVED	ENABLECLK1	ENABLECLK0	RESERVED		RESERVED	SYSPLLREF
R/W-Xh	R/W-1h	R/W-1h	R/W-1h	R/W-Xh		R/W-0h	R/W-0h

Table 3-64. SYSPLLCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	RESERVED	R/W	0h	Reserved
15-12	RDIVCLK1	R/W	0h	RDIVCLK1 sets the final divider for the SYSPLLCLK1 output. 0h = SYSPLLCLK1 is divided by 2 1h = SYSPLLCLK1 is divided by 4 2h = SYSPLLCLK1 is divided by 6 3h = SYSPLLCLK1 is divided by 8 4h = SYSPLLCLK1 is divided by 10 5h = SYSPLLCLK1 is divided by 12 6h = SYSPLLCLK1 is divided by 14 7h = SYSPLLCLK1 is divided by 16 8h = SYSPLLCLK1 is divided by 18 9h = SYSPLLCLK1 is divided by 20 Ah = SYSPLLCLK1 is divided by 22 Bh = SYSPLLCLK1 is divided by 24 Ch = SYSPLLCLK1 is divided by 26 Dh = SYSPLLCLK1 is divided by 28 Eh = SYSPLLCLK1 is divided by 30 Fh = SYSPLLCLK1 is divided by 32

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Table 3-64. SYSPLLCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	RDIVCLK0	R/W	0h	RDIVCLK0 sets the final divider for the SYSPLLCLK0 output. 0h = SYSPLLCLK0 is divided by 2 1h = SYSPLLCLK0 is divided by 4 2h = SYSPLLCLK0 is divided by 6 3h = SYSPLLCLK0 is divided by 8 4h = SYSPLLCLK0 is divided by 10 5h = SYSPLLCLK0 is divided by 12 6h = SYSPLLCLK0 is divided by 14 7h = SYSPLLCLK0 is divided by 16 8h = SYSPLLCLK0 is divided by 18 9h = SYSPLLCLK0 is divided by 20 Ah = SYSPLLCLK0 is divided by 22 Bh = SYSPLLCLK0 is divided by 24 Ch = SYSPLLCLK0 is divided by 26 Dh = SYSPLLCLK0 is divided by 28 Eh = SYSPLLCLK0 is divided by 30 Fh = SYSPLLCLK0 is divided by 32
7	RESERVED	R/W	Xh	
6	RESERVED	R/W	1h	Reserved
5	ENABLECLK1	R/W	1h	ENABLECLK1 enables or disables the SYSPLLCLK1 output. 0h = SYSPLLCLK1 is disabled 1h = SYSPLLCLK1 is enabled
4	ENABLECLK0	R/W	1h	ENABLECLK0 enables or disables the SYSPLLCLK0 output. 0h = SYSPLLCLK0 is disabled 1h = SYSPLLCLK0 is enabled
3-2	RESERVED	R/W	Xh	
1	RESERVED	R/W	0h	Reserved
0	SYSPLLREF	R/W	0h	SYSPLLREF selects the system PLL (SYSPLL) reference clock source. 0h = SYSPLL reference is SYSOSC 1h = SYSPLL reference is HFCLK

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17 SYSPLLCFG1 Register (Offset = 1124h) [Reset = 000023XXh]

SYSPLLCFG1 is shown in Figure 3-27 and described in Table 3-49.

Return to the Summary Table.

SYSPLL reference and feedback divider

Figure 3-27. SYSPLLCFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	QDIV							RESERVED						PDIV	
R/W-0h	R/W-23h							R/W-Xh						R/W-0h	

Table 3-66. SYSPLLCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	0h	
14-8	QDIV	R/W	23h	QDIV selects the SYSPLL feedback path divider. 0h = Divide-by-one is not a valid QDIV option 1h = Feedback path is divided by 2 7Eh = Feedback path is divided by 127 (0x7E)
7-2	RESERVED	R/W	Xh	
1-0	PDIV	R/W	0h	PDIV selects the SYSPLL reference clock prescale divider. 0h = SYSPLLREF is not divided 1h = SYSPLLREF is divided by 2 2h = SYSPLLREF is divided by 4 3h = SYSPLLREF is divided by 8

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18 SYSPLLPARAM0 Register (Offset = 1128h) [Reset = X1XAX0X0h]

SYSPLLPARAM0 is shown in Figure 3-28 and described in Table 3-50.

Return to the Summary Table.

SYSPLL PARAM0 (load from FACTORY region)

Figure 3-28. SYSPLLPARAM0 Register

31	30	29	28	27	26	25	24
CAPBOVERRIDE	RESERVED			CAPBVAL			
R/W-1h	R/W-Xh			R/W-1h			
23	22	21	20	19	18	17	16
RESERVED		CPCURRENT					
R/W-Xh		R/W-Ah					
15	14	13	12	11	10	9	8
RESERVED	STARTTIMELP						
R/W-Xh	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	STARTTIME						
R/W-Xh	R/W-0h						

Table 3-68. SYSPLLPARAM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAPBOVERRIDE	R/W	1h	CAPBOVERRIDE controls the override for Cap B 0h = Cap B override disabled 1h = Cap B override enabled
30-29	RESERVED	R/W	Xh	
28-24	CAPBVAL	R/W	1h	Override value for Cap B
23-22	RESERVED	R/W	Xh	
21-16	CPCURRENT	R/W	Ah	Charge pump current
15	RESERVED	R/W	Xh	
14-8	STARTTIMELP	R/W	0h	Startup time from low power mode exit to locked clock, in 1us resolution
7	RESERVED	R/W	Xh	
6-0	STARTTIME	R/W	0h	Startup time from enable to locked clock, in 1us resolution

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19 SYSPLLPARAM1 Register (Offset = 112Ch) [Reset = 0FXX01XFh]

SYSPLLPARAM1 is shown in Figure 3-29 and described in Table 3-51.

Return to the Summary Table.

SYSPLL PARAM1 (load from FACTORY region)

Figure 3-29. SYSPLLPARAM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPFRESC								RESERVED						LPFRESA	
R/W-Fh								R/W-Xh						R/W-1h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPFRESA								RESERVED			LPFCAPA				
R/W-1h								R/W-Xh			R/W-Fh				

Table 3-70. SYSPLLPARAM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LPFRESC	R/W	Fh	Loop filter Res C
23-18	RESERVED	R/W	Xh	
17-8	LPFRESA	R/W	1h	Loop filter Res A
7-5	RESERVED	R/W	Xh	
4-0	LPFCAPA	R/W	Fh	Loop filter Cap A

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20 SYSPLLPARAM2 Register (Offset = 1130h) [Reset = 0000000Xh]

SYSPLLPARAM2 is shown in Figure 3-30 and described in Table 3-52.

Return to the Summary Table.

SYSPLL PARAM2 (load from FACTORY region)

Figure 3-30. SYSPLLPARAM2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				RNGFIXVCOIBIASCFG	RESERVED	LPFCAPC	
R/W-0h				R/W-1h	R/W-Xh	R/W-0h	

Table 3-72. SYSPLLPARAM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	RNGFIXVCOIBIASCFG	R/W	1h	0 value for Temperature Compensation R addition
2	RESERVED	R/W	Xh	
1-0	LPFCAPC	R/W	0h	Loop filter Cap C

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21 SYSPLLLDOCTL Register (Offset = 1134h) [Reset = 00000000h]

SYSPLLLDOCTL is shown in Figure 3-31 and described in Table 3-53.

Return to the Summary Table.

SYSPLL LDO CTL (load from FACTORY region)

Figure 3-31. SYSPLLLDOCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LDOCTLLOWV															
R/W-0h																R/W-0h															

Table 3-74. SYSPLLLDOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	LDOCTLLOWV	R/W	0h	LDO Configurability

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22 SYSPLLLDOPROG Register (Offset = 1138h) [Reset = 00000004h]

SYSPLLLDOPROG is shown in Figure 3-32 and described in Table 3-54.

Return to the Summary Table.

SYSPLL LDO VOUT PROG (load from FACTORY region)

Figure 3-32. SYSPLLLDOPROG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					LDOVOUTPROGLOWV		
R/W-0h					R/W-4h		

Table 3-76. SYSPLLLDOPROG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	LDOVOUTPROGLOWV	R/W	4h	HPLL LDO Vout Prog

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23 GENCLKEN Register (Offset = 113Ch) [Reset = 000800XXh]

GENCLKEN is shown in Figure 3-33 and described in Table 3-55.

Return to the Summary Table.

General clock enable control

Figure 3-33. GENCLKEN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				RAWPLLCLKEN	RESERVED	RESERVED	
R/W-0h				R/W-1h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
CANEXTDIVEN	EXTDIVCAN			MCLKEXTDIVEN	EXTDIVMCLK		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED			EXCLKEN
R/W-Xh			R/W-0h	R/W-Xh			R/W-0h

Table 3-78. GENCLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19	RAWPLLCLKEN	R/W	1h	RAWPLLCLKEN enables or disables the 400MHz RAW PLL clock into the system 0h = 400MHz RAW PLL clock is disabled 1h = 400MHz RAW PLL clock is enabled
18	RESERVED	R/W	0h	Reserved
17-16	RESERVED	R/W	0h	Reserved
15	CANEXTDIVEN	R/W	0h	CANEXTDIVEN enables or disables the divider function of the PLL Source to CAN. 0h = CLock divider is disabled (passthrough, EXTDIVCAN is not applied) 1h = Clock divider is enabled (EXTDIVCAN is applied)
14-12	EXTDIVCAN	R/W	0h	EXTDIVCAN selects the divider value for the divider for the PLL Source to CAN. 0h = CLK_OUT source is divided by 2 1h = CLK_OUT source is divided by 4 2h = CLK_OUT source is divided by 6 3h = CLK_OUT source is divided by 8 4h = CLK_OUT source is divided by 10 5h = CLK_OUT source is divided by 12 6h = CLK_OUT source is divided by 14 7h = CLK_OUT source is divided by 16
11	MCLKEXTDIVEN	R/W	0h	MCLKEXTDIVEN enables or disables the divider function of the PLL Source to MCLK. 0h = CLock divider is disabled (passthrough, EXTDIVMCLK is not applied) 1h = Clock divider is enabled (EXTDIVMCLK is applied)

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Table 3-78. GENCLKEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	EXTDIVMCLK	R/W	0h	EXTDIVMCLK selects the divider value for the divider for the PLL Source MCLK. 0h = CLK_OUT source is divided by 2 1h = CLK_OUT source is divided by 4 2h = CLK_OUT source is divided by 6 3h = CLK_OUT source is divided by 8 4h = CLK_OUT source is divided by 10 5h = CLK_OUT source is divided by 12 6h = CLK_OUT source is divided by 14 7h = CLK_OUT source is divided by 16
7-5	RESERVED	R/W	Xh	
4	RESERVED	R/W	0h	Reserved
3-1	RESERVED	R/W	Xh	
0	EXCLKEN	R/W	0h	EXCLKEN enables the CLK_OUT external clock output block. 0h = CLK_OUT block is disabled 1h = CLK_OUT block is enabled

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24 GENCLKCFG Register (Offset = 1140h) [Reset = 00000X0Xh]

GENCLKCFG is shown in Figure 3-34 and described in Table 3-56.

Return to the Summary Table.

General clock configuration

Figure 3-34. GENCLKCFG Register

31	30	29	28	27	26	25	24
RESERVED		RESERVED	FCCTRIGCNT				
R/W-0h		R-0h	R/W-0h				
23	22	21	20	19	18	17	16
RESERVED		FCCLVLTRIG	FCCTRIGSRC	FCCSELCLK			
R-0h		R/W-0h	R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RESERVED		RESERVED	CANCLKSRC
R/W-0h				R/W-Xh		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EXCLKDIVEN	EXCLKDIVVAL			RESERVED	EXCLKSRC		
R/W-0h	R/W-0h			R/W-Xh	R/W-0h		

Table 3-80. GENCLKCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29	RESERVED	R	0h	Reserved
28-24	FCCTRIGCNT	R/W	0h	FCCTRIGCNT specifies the number of trigger clock periods in the trigger window. FCCTRIGCNT=0h (one trigger clock period) up to 1Fh (32 trigger clock periods) may be specified.
23-22	RESERVED	R	0h	Reserved
21	FCCLVLTRIG	R/W	0h	FCCLVLTRIG selects the frequency clock counter (FCC) trigger mode. 0h = Rising edge to rising edge triggered 1h = Level triggered
20	FCCTRIGSRC	R/W	0h	FCCTRIGSRC selects the frequency clock counter (FCC) trigger source. 0h = FCC trigger is the external pin 1h = FCC trigger is the LFCLK
19-16	FCCSELCLK	R/W	0h	FCCSELCLK selectes the frequency clock counter (FCC) clock source. 0h = FCC clock is MCLK/4 1h = FCC clock is SYSOSC 2h = FCC clock is HFCLK 3h = FCC clock is the CLK_OUT selection 4h = FCC clock is SYSPLLCLK0 5h = FCC clock is SYSPLLCLK1 6h = FCC clock is ECAT25CLK 7h = FCC clock is the FCCIN external input
15-12	RESERVED	R/W	0h	Reserved
11-10	RESERVED	R/W	Xh	
9	RESERVED	R/W	0h	Reserved
8	CANCLKSRC	R/W	0h	CANCLKSRC selects the CANCLK source. 0h = CANCLK source is HFCLK 1h = CANCLK source is SYSPLLCLK

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Table 3-80. GENCLKCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	EXCLKDIVEN	R/W	0h	EXCLKDIVEN enables or disables the divider function of the CLK_OUT external clock output block. 0h = CLock divider is disabled (passthrough, EXCLKDIVVAL is not applied) 1h = Clock divider is enabled (EXCLKDIVVAL is applied)
6-4	EXCLKDIVVAL	R/W	0h	EXCLKDIVVAL selects the divider value for the divider in the CLK_OUT external clock output block. 0h = CLK_OUT source is divided by 2 1h = CLK_OUT source is divided by 4 2h = CLK_OUT source is divided by 6 3h = CLK_OUT source is divided by 8 4h = CLK_OUT source is divided by 10 5h = CLK_OUT source is divided by 12 6h = CLK_OUT source is divided by 14 7h = CLK_OUT source is divided by 16
3	RESERVED	R/W	Xh	
2-0	EXCLKSRC	R/W	0h	EXCLKSRC selects the source for the CLK_OUT external clock output block. ULPCLK and MFPCLK require the CLK_OUT divider (EXCLKDIVEN) to be enabled 0h = CLK_OUT is SYSOSC 1h = CLK_OUT is ULPCLK (EXCLKDIVEN must be enabled) 2h = CLK_OUT is LFCLK 3h = CLK_OUT is MFPCLK (EXCLKDIVEN must be enabled) 4h = CLK_OUT is HFCLK 5h = CLK_OUT is SYSPLLCLK1 (SYSPLLCLK1 must be <=48MHz)

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25 PMODECFG Register (Offset = 1144h) [Reset = 00000000h]

PMODECFG is shown in Figure 3-35 and described in Table 3-57.

Return to the Summary Table.

Power mode configuration

Figure 3-35. PMODECFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DSLEEP	
R/W-0h														R/W-0h	

Table 3-82. PMODECFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	DSLEEP	R/W	0h	DSLEEP selects the operating mode to enter upon a DEEPSLEEP request from the CPU. 0h = STOP mode is entered 1h = STANDBY mode is entered 2h = SHUTDOWN mode is entered 3h = Reserved

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26 MLDOLPENCFG Register (Offset = 1148h) [Reset = 000000XXh]

MLDOLPENCFG is shown in Figure 3-36 and described in Table 3-58.

Return to the Summary Table.

LDO Configuration Control

Figure 3-36. MLDOLPENCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CVLODIS
R/W-Xh							R/W-0h

Table 3-84. MLDOLPENCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	Xh	
0	CVLODIS	R/W	0h	Control to disable lowering the core voltage for STOP and STANDBY 0h = Lower Core Voltage for STOP and STANDBY mode 1h = Do Not Lower Core Voltage for STOP and STANDBY mode to provide faster wakeup

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27 FCC Register (Offset = 1150h) [Reset = 00000000h]

FCC is shown in Figure 3-37 and described in Table 3-59.

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Frequency clock counter (FCC) count

Figure 3-37. FCC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										DATA																					
R-0h										R-0h																					

Table 3-86. FCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	
21-0	DATA	R	0h	Frequency clock counter (FCC) count value.

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28 SYSTEMCFG Register (Offset = 1180h) [Reset = 00XXXXXXh]

SYSTEMCFG is shown in Figure 3-38 and described in Table 3-60.

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System configuration

Figure 3-38. SYSTEMCFG Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
R/W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED					FLASHECCRSTDIS	RESERVED	WWDTLP0RSTDIS
R/W-XXXXh					R/W-1h	R/W-Xh	R/W-0h

Table 3-88. SYSTEMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value of 1Bh (27) must be written to KEY together with contents to be updated. Reads as 0 1Bh = Issue write
23-3	RESERVED	R/W	XXXXh	
2	FLASHECCRSTDIS	R/W	1h	FLASHECCRSTDIS specifies whether a flash ECC double error detect (DED) will trigger a SYSRST or an NMI. 0h = Flash ECC DED will trigger a SYSRST 1h = Flash ECC DED will trigger a NMI
1	RESERVED	R/W	Xh	
0	WWDTLP0RSTDIS	R/W	0h	WWDTLP0RSTDIS specifies whether a WWDT Error Event will trigger a BOOTRST or an NMI. 0h = WWDTLP0 Error Event will trigger a BOOTRST 1h = WWDTLP0 Error Event will trigger an NMI

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29 SRAMCFG Register (Offset = 1184h) [Reset = 00X0XXX0h]

SRAMCFG is shown in Figure 3-39 and described in Table 3-61.

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System SRAM configuration

Figure 3-39. SRAMCFG Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED		BANKINITDIS5	BANKINITDIS4	BANKINITDIS3	BANKINITDIS2	BANKINITDIS1	BANKINITDIS0
R/W-Xh		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-XXXh							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	RESERVED	RESERVED
R/W-XXXh				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-90. SRAMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value of B5h (181) must be written to KEY together with contents to be updated. Reads as 0 B5h = Issue write
23-22	RESERVED	R/W	Xh	
21	BANKINITDIS5	R/W	0h	SRAM BANK5 Initialization 0h = SRAM BANK5 will Initialize when transitioning from OFF to ON 1h = SRAM BANK5 will NOT Initialize when transitioning from OFF to ON
20	BANKINITDIS4	R/W	0h	SRAM BANK4 Initialization 0h = SRAM BANK4 will Initialize when transitioning from OFF to ON 1h = SRAM BANK4 will NOT Initialize when transitioning from OFF to ON
19	BANKINITDIS3	R/W	0h	SRAM BANK3 Initialization 0h = SRAM BANK3 will Initialize when transitioning from OFF to ON 1h = SRAM BANK3 will NOT Initialize when transitioning from OFF to ON
18	BANKINITDIS2	R/W	0h	SRAM BANK2 Initialization 0h = SRAM BANK2 will Initialize when transitioning from OFF to ON 1h = SRAM BANK2 will NOT Initialize when transitioning from OFF to ON
17	BANKINITDIS1	R/W	0h	SRAM BANK1 Initialization 0h = SRAM BANK1 will Initialize when transitioning from OFF to ON 1h = SRAM BANK1 will NOT Initialize when transitioning from OFF to ON
16	BANKINITDIS0	R/W	0h	SRAM BANK0 Initialization 0h = SRAM BANK0 will Initialize when transitioning from OFF to ON 1h = SRAM BANK0 will NOT Initialize when transitioning from OFF to ON
15-4	RESERVED	R/W	XXXh	
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved

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Table 3-90. SRAMCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

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30 WRITELOCK Register (Offset = 1200h) [Reset = 00000000h]

WRITELOCK is shown in Figure 3-40 and described in Table 3-62.

Return to the Summary Table.

SYSCTL register write lockout

Figure 3-40. WRITELOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ACTIVE
R/W-0h							R/W-0h

Table 3-92. WRITELOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	ACTIVE	R/W	0h	ACTIVE controls whether critical SYSCTL registers are write protected or not. 0h = Allow writes to lockable registers 1h = Disallow writes to lockable registers

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31 CLKSTATUS Register (Offset = 1204h) [Reset = XXXXXXXXh]

CLKSTATUS is shown in Figure 3-41 and described in Table 3-63.

Return to the Summary Table.

Clock module (CKM) status

Figure 3-41. CLKSTATUS Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	SYSPLLBLKUPD	HFCLKBLKUPD	RESERVED		FCCDONE	FCLMODE
R-0h	R-Xh	R-0h	R-0h	R-Xh		R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED		HSCLKGOOD	HSCLKDEAD	RESERVED		RESERVED	CURHSCLKSEL
R-Xh		R-0h	R-0h	R-Xh		R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	SYSPLLOFF	HFCLKOFF	HSCLKSOFF	LFOSCGOOD	RESERVED	SYSPLLGOOD	HFCLKGOOD
R-Xh	R-1h	R-1h	R-1h	R-0h	R-Xh	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		RESERVED	HSCLKMUX	RESERVED		SYSOSCFREQ	
R-0h		R-Xh	R-0h	R-Xh		R-0h	

Table 3-94. CLKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	Xh	
29	SYSPLLBLKUPD	R	0h	SYSPLLBLKUPD indicates when writes to SYSPLLCFG0/1 and SYSPLLPARAM0/1 are blocked. 0h = writes to SYSPLLCFG0/1 and SYSPLLPARAM0/1 are allowed 1h = writes to SYSPLLCFG0/1 and SYSPLLPARAM0/1 are blocked
28	HFCLKBLKUPD	R	0h	HFCLKBLKUPD indicates when writes to the HFCLKCLKCFG register are blocked. 0h = Writes to HFCLKCLKCFG are allowed 1h = Writes to HFCLKCLKCFG are blocked
27-26	RESERVED	R	Xh	
25	FCCDONE	R	0h	FCCDONE indicates when a frequency clock counter capture is complete. 0h = FCC capture is not done 1h = FCC capture is done
24	FCLMODE	R	0h	FCLMODE indicates if the SYSOSC frequency correction loop (FCL) is enabled. 0h = SYSOSC FCL is disabled 1h = SYSOSC FCL is enabled
23-22	RESERVED	R	Xh	
21	HSCLKGOOD	R	0h	HSCLKGOOD is set by hardware if the selected clock source for HSCLK started successfully. 0h = The HSCLK source did not start correctly 1h = The HSCLK source started correctly
20	HSCLKDEAD	R	0h	HSCLKDEAD is set by hardware if the selected source for HSCLK was started but did not start successfully. 0h = The HSCLK source was not started or started correctly 1h = The HSCLK source did not start correctly
19-18	RESERVED	R	Xh	

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Table 3-94. CLKSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	RESERVED	R	0h	Reserved
16	CURHSCLKSEL	R	0h	CURHSCLKSEL indicates the current clock source for HSCLK. 0h = HSCLK is currently sourced from the SYSPLL 1h = HSCLK is currently sourced from the HFCLK
15	RESERVED	R	Xh	
14	SYSPLLOFF	R	1h	SYSPLLOFF indicates if the SYSPLL is disabled or was dead at startup. When the SYSPLL is started, SYSPLLOFF is cleared by hardware. Following startup of the SYSPLL, if the SYSPLL startup monitor determines that the SYSPLL was not started correctly, SYSPLLOFF is set. 0h = SYSPLL started correctly and is enabled 1h = SYSPLL is disabled or was dead startup
13	HFCLKOFF	R	1h	HFCLKOFF indicates if the HFCLK is disabled or was dead at startup. When the HFCLK is started, HFCLKOFF is cleared by hardware. Following startup of the HFCLK, if the HFCLK startup monitor determines that the HFCLK was not started correctly, HFCLKOFF is set. 0h = HFCLK started correctly and is enabled 1h = HFCLK is disabled or was dead at startup
12	HSCLKSOFF	R	1h	HSCLKSOFF is set when the high speed clock sources (SYSPLL, HFCLK) are disabled or dead. It is the logical AND of HFCLKOFF and SYSPLLOFF. 0h = SYSPLL, HFCLK, or both were started correctly and remain enabled 1h = SYSPLL and HFCLK are both either off or dead
11	LFOSCGOOD	R	0h	LFOSCGOOD indicates when the LFOSC startup has completed and the LFOSC is ready for use. 0h = LFOSC is not ready 1h = LFOSC is ready
10	RESERVED	R	Xh	
9	SYSPLLGOOD	R	0h	SYSPLLGOOD indicates if the SYSPLL started correctly. When the SYSPLL is started, SYSPLLGOOD is cleared by hardware. After the startup settling time has expired, the SYSPLL status is tested. If the SYSPLL started successfully the SYSPLLGOOD bit is set, else it is left cleared. 0h = SYSPLL did not start correctly 1h = SYSPLL started correctly
8	HFCLKGOOD	R	0h	HFCLKGOOD indicates that the HFCLK started correctly. When the XTAL is started or HFCLK_IN is selected as the HFCLK source, this bit will be set by hardware if a valid HFCLK is detected, and cleared if HFCLK is not operating within the expected range. 0h = HFCLK did not start correctly 1h = HFCLK started correctly
7-6	RESERVED	R	0h	Reserved
5	RESERVED	R	Xh	
4	HSCLKMUX	R	0h	HSCLKMUX indicates if MCLK is currently sourced from the high-speed clock (HSCLK). 0h = MCLK is not sourced from HSCLK 1h = MCLK is sourced from HSCLK
3-2	RESERVED	R	Xh	
1-0	SYSOSCFREQ	R	0h	SYSOSCFREQ indicates the current SYSOSC operating frequency. 0h = SYSOSC is at base frequency (32MHz) 1h = SYSOSC is at low frequency (4MHz)

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32 SYSSTATUS Register (Offset = 1208h) [Reset = XXX00XX0h]

SYSSTATUS is shown in Figure 3-42 and described in Table 3-64.

Return to the Summary Table.

System status information

Figure 3-42. SYSSTATUS Register

31	30	29	28	27	26	25	24
REBOOTATTEMPTS		RESERVED					
R-0h		R-XXh					
23	22	21	20	19	18	17	16
RESERVED		SRAMBANK5READY	SRAMBANK4READY	SRAMBANK3READY	SRAMBANK2READY	SRAMBANK1READY	SRAMBANK0READY
R-XXh		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	SHDNIOLOCK	SWDJCFGDIS	EXTRSTPINDIS	RESERVED		MCAN1READY	MCAN0READY
R-0h	R-0h	R-0h	R-0h	R-Xh		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	PMUIREFGOOD	RESERVED	RESERVED	RESERVED		FLASHSEC	FLASHDED
R-Xh	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 3-96. SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	REBOOTATTEMPTS	R	0h	REBOOTATTEMPTS indicates the number of boot attempts taken before the user application starts.
29-22	RESERVED	R	XXh	
21	SRAMBANK5READY	R	0h	SRAM BANK5 READY STATE 0h = SRAM BANK5 is NOT READY for access 1h = SRAM BANK5 is READY for access
20	SRAMBANK4READY	R	0h	SRAM BANK4 READY STATE 0h = SRAM BANK4 is NOT READY for access 1h = SRAM BANK4 is READY for access
19	SRAMBANK3READY	R	0h	SRAM BANK3 READY STATE 0h = SRAM BANK3 is NOT READY for access 1h = SRAM BANK3 is READY for access
18	SRAMBANK2READY	R	0h	SRAM BANK2 READY STATE 0h = SRAM BANK2 is NOT READY for access 1h = SRAM BANK2 is READY for access
17	SRAMBANK1READY	R	0h	SRAM BANK1 READY STATE 0h = SRAM BANK1 is NOT READY for access 1h = SRAM BANK1 is READY for access
16	SRAMBANK0READY	R	0h	SRAM BANK0 READY STATE 0h = SRAM BANK0 is NOT READY for access 1h = SRAM BANK0 is READY for access
15	RESERVED	R	0h	Reserved
14	SHDNIOLOCK	R	0h	SHDNIOLOCK indicates when IO is locked due to SHUTDOWN 0h = IO IS NOT Locked due to SHUTDOWN 1h = IO IS Locked due to SHUTDOWN
13	SWDJCFGDIS	R	0h	SWDJCFGDIS indicates when user has disabled the use of SWD/JTAG Port 0h = SWD/JTAG Port Enabled 1h = SWD/JTAG Port Disabled

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Table 3-96. SYSSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	EXTRSTPINDIS	R	0h	EXTRSTPINDIS indicates when user has disabled the use of external reset pin 0h = External Reset Pin Enabled 1h = External Reset Pin Disabled
11-10	RESERVED	R	Xh	
9	MCAN1READY	R	0h	MCAN1READY indicates when the MCAN1 peripheral is ready. 0h = MCAN1 is not ready 1h = MCAN1 is ready
8	MCAN0READY	R	0h	MCAN0READY indicates when the MCAN0 peripheral is ready. 0h = MCAN0 is not ready 1h = MCAN0 is ready
7	RESERVED	R	Xh	
6	PMUIREFGOOD	R	0h	PMUIREFGOOD is set by hardware when the PMU current reference is ready. 0h = IREF is not ready 1h = IREF is ready
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-2	RESERVED	R	0h	Reserved
1	FLASHSEC	R	0h	FLASHSEC indicates if a flash ECC single bit error was detected and corrected (SEC). 0h = No flash ECC single bit error detected 1h = Flash ECC single bit error was detected and corrected
0	FLASHDED	R	0h	FLASHDED indicates if a flash ECC double bit error was detected (DED). 0h = No flash ECC double bit error detected 1h = Flash ECC double bit error detected

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33 RSTCAUSE Register (Offset = 1220h) [Reset = 00000000h]

RSTCAUSE is shown in Figure 3-43 and described in Table 3-65.

Return to the Summary Table.

Reset cause

Figure 3-43. RSTCAUSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											ID				
R-0h																											RC-0h				

Table 3-98. RSTCAUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	ID	RC	0h	ID is a read-to-clear field which indicates the lowest level reset cause since the last read. 0h = No reset since last read 1h = POR- violation, SHUTDNSTOREx or PMU trim parity fault 2h = NRST triggered POR (>1s hold) 3h = Software triggered POR 4h = BOR0- violation 5h = SHUTDOWN mode exit 8h = Non-PMU trim parity fault 9h = Fatal clock failure Ch = NRST triggered BOOTRST (<1s hold) Dh = Software triggered BOOTRST Eh = WWDT0 violation Fh = Reset out from EthercatSS 10h = BSL exit 11h = BSL entry 14h = Flash uncorrectable ECC error 15h = CPULOCK violation 1Ah = Debug triggered SYSRST 1Bh = Software triggered SYSRST 1Ch = Debug triggered CPURST 1Dh = Software triggered CPURST

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34 RESETLEVEL Register (Offset = 1300h) [Reset = 00000000h]

RESETLEVEL is shown in Figure 3-44 and described in Table 3-66.

Return to the Summary Table.

Reset level for application-triggered reset command

Figure 3-44. RESETLEVEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LEVEL	
R/W-0h														R/W-0h	

Table 3-100. RESETLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	LEVEL	R/W	0h	LEVEL is used to specify the type of reset to be issued when RESETCMD is set to generate a software triggered reset. 0h = Issue a SYSRST (CPU plus peripherals only) 1h = Issue a BOOTRST (CPU, peripherals, and boot configuration routine) 2h = Issue a SYSRST and enter the boot strap loader (BSL) 3h = Issue a power-on reset (POR) 4h = Issue a SYSRST and exit the boot strap loader (BSL)

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35 RESETCMD Register (Offset = 1304h) [Reset = 00XXXXXXh]

RESETCMD is shown in Figure 3-45 and described in Table 3-67.

Return to the Summary Table.

Execute an application-triggered reset command

Figure 3-45. RESETCMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY								RESERVED							
W-0h								W-XXXXh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GO
W-XXXXh															W-0h

Table 3-102. RESETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value of E4h (228) must be written to KEY together with GO to trigger the reset. E4h = Issue reset
23-1	RESERVED	W	XXXXh	
0	GO	W	0h	Execute the reset specified in RESETLEVEL.LEVEL. Must be written together with the KEY. 1h = Issue reset

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36 SYSOSCFCLCTL Register (Offset = 1310h) [Reset = 00XXXXXXh]

SYSOSCFCLCTL is shown in Figure 3-46 and described in Table 3-68.

Return to the Summary Table.

SYSOSC frequency correction loop (FCL) ROSC enable

Figure 3-46. SYSOSCFCLCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED						RESERVED	SETUSEFCL
W-XXXXh						W-0h	W-0h

Table 3-104. SYSOSCFCLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value of 2Ah (42) must be written to KEY together with SETUSEFCL to enable the FCL. 2Ah = Issue Command
23-2	RESERVED	W	XXXXh	
1	RESERVED	W	0h	Reserved
0	SETUSEFCL	W	0h	Set SETUSEFCL to enable the frequency correction loop in SYSOSC. Once enabled, this state is locked until the next BOOTRST. 1h = Enable the SYSOSC FCL

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37 SHDNIOREL Register (Offset = 131Ch) [Reset = 00XXXXXXh]

SHDNIOREL is shown in Figure 3-47 and described in Table 3-69.

Return to the Summary Table.

SHUTDOWN IO release control

Figure 3-47. SHDNIOREL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							RELEASE
W-XXXXh							W-0h

Table 3-106. SHDNIOREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value 91h must be written to KEY together with RELEASE to set RELEASE. 91h = Issue command
23-1	RESERVED	W	XXXXh	
0	RELEASE	W	0h	Set RELEASE to release the IO after a SHUTDOWN mode exit. 1h = Release IO

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38 EXRSTPIN Register (Offset = 1320h) [Reset = 00XXXXXXh]

EXRSTPIN is shown in Figure 3-48 and described in Table 3-70.

Return to the Summary Table.

Disable the reset function of the NRST pin

Figure 3-48. EXRSTPIN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							DISABLE
W-XXXXh							W-0h

Table 3-108. EXRSTPIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value 1Eh must be written together with DISABLE to disable the reset function. 1Eh = Issue command
23-1	RESERVED	W	XXXXh	
0	DISABLE	W	0h	Set DISABLE to disable the reset function of the NRST pin. Once set, this configuration is locked until the next POR. 0h = Reset function of NRST pin is enabled 1h = Reset function of NRST pin is disabled

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39 SYSSTATUSCLR Register (Offset = 1324h) [Reset = 00XXXXXXh]

SYSSTATUSCLR is shown in Figure 3-49 and described in Table 3-71.

Return to the Summary Table.

Clear sticky bits of SYSSTATUS

Figure 3-49. SYSSTATUSCLR Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							ALLECC
W-XXXXh							W-0h

Table 3-110. SYSSTATUSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value CEh (206) must be written to KEY together with ALLECC to clear the ECC state. CEh = Issue command
23-1	RESERVED	W	XXXXh	
0	ALLECC	W	0h	Set ALLECC to clear all ECC related SYSSTATUS indicators. 1h = Clear ECC error state

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40 SWDJCFG Register (Offset = 1328h) [Reset = 00XXXXXXh]

SWDJCFG is shown in Figure 3-50 and described in Table 3-72.

Return to the Summary Table.

Disable the SWD/JTAG function on the SWD/JTAG pins

Figure 3-50. SWDJCFG Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							DISABLE
W-XXXXh							W-0h

Table 3-112. SWDJCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value 62h (98) must be written to KEY together with DISBALE to disable the SWD/JTAG functions. 62h = Issue command
23-1	RESERVED	W	XXXXh	
0	DISABLE	W	0h	Set DISABLE to disable the SWD/JTAG function on SWD/JTAG pins, allowing the SWD/JTAG pins to be used as GPIO. 1h = Disable SWD/JTAG function on SWD/JTAG pins

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41 FCCCMD Register (Offset = 132Ch) [Reset = 00XXXXXXh]

FCCCMD is shown in Figure 3-51 and described in Table 3-73.

Return to the Summary Table.

Frequency clock counter start capture

Figure 3-51. FCCCMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY								RESERVED							
W-0h								W-XXXXh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															GO
W-XXXXh															W-0h

Table 3-114. FCCCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value 0Eh (14) must be written with GO to start a capture. 0Eh = Issue command
23-1	RESERVED	W	XXXXh	
0	GO	W	0h	Set GO to start a capture with the frequency clock counter (FCC). 1h = 1

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42 SHUTDNSTORE0 Register (Offset = 1400h) [Reset = 00000000h]

SHUTDNSTORE0 is shown in Figure 3-52 and described in Table 3-74.

Return to the Summary Table.

Shutdown storage memory (byte 0)

Figure 3-52. SHUTDNSTORE0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R/W-0h						R-0h	R/W-0h
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

Table 3-116. SHUTDNSTORE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-0	DATA	R/W	0h	Shutdown storage byte 0

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43 SHUTDNSTORE1 Register (Offset = 1404h) [Reset = 00000000h]

SHUTDNSTORE1 is shown in Figure 3-53 and described in Table 3-75.

Return to the Summary Table.

Shutdown storage memory (byte 1)

Figure 3-53. SHUTDNSTORE1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R/W-0h						R-0h	R/W-0h
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

Table 3-118. SHUTDNSTORE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-0	DATA	R/W	0h	Shutdown storage byte 1

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44 SHUTDNSTORE2 Register (Offset = 1408h) [Reset = 00000000h]

SHUTDNSTORE2 is shown in Figure 3-54 and described in Table 3-76.

Return to the Summary Table.

Shutdown storage memory (byte 2)

Figure 3-54. SHUTDNSTORE2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R/W-0h						R-0h	R/W-0h
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

Table 3-120. SHUTDNSTORE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-0	DATA	R/W	0h	Shutdown storage byte 2

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45 SHUTDNSTORE3 Register (Offset = 140Ch) [Reset = 00000000h]

SHUTDNSTORE3 is shown in Figure 3-55 and described in Table 3-77.

Return to the Summary Table.

Shutdown storage memory (byte 3)

Figure 3-55. SHUTDNSTORE3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						RESERVED	RESERVED
R/W-0h						R-0h	R/W-0h
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

Table 3-122. SHUTDNSTORE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-0	DATA	R/W	0h	Shutdown storage byte 3

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46 ADCSEQFRCGB Register (Offset = 1410h) [Reset = 00000000h]

ADCSEQFRCGB is shown in Figure 3-56 and described in Table 3-78.

Return to the Summary Table.

ADC Global Sequence Force

Figure 3-56. ADCSEQFRCGB Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				SEQ3	SEQ2	SEQ1	SEQ0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-124. ADCSEQFRCGB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	SEQ3	R/W	0h	Generate synchronous SW trigger for SEQ3
2	SEQ2	R/W	0h	Generate synchronous SW trigger for SEQ2
1	SEQ1	R/W	0h	Generate synchronous SW trigger for SEQ1
0	SEQ0	R/W	0h	Generate synchronous SW trigger for SEQ0

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47 ADCSEQFRCGBSEL Register (Offset = 1414h) [Reset = 00000000h]

ADCSEQFRCGBSEL is shown in Figure 3-57 and described in Table 3-79.

Return to the Summary Table.

ADC Global Sequence Force Select

Figure 3-57. ADCSEQFRCGBSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					ADCC	ADCB	ADCA
R/W-0h					R/W-0h	R/W-0h	R/W-0h

Table 3-126. ADCSEQFRCGBSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2	ADCC	R/W	0h	Generate synchronous SW trigger for ADCC
1	ADCB	R/W	0h	Generate synchronous SW trigger for ADCB
0	ADCA	R/W	0h	Generate synchronous SW trigger for ADCA

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48 M33SPARESOCLOCK1 Register (Offset = 1418h) [Reset = 00000000h]

M33SPARESOCLOCK1 is shown in Figure 3-58 and described in Table 3-80.

Return to the Summary Table.

M33C1 Spare SOC LOCK Reg 1

Figure 3-58. M33SPARESOCLOCK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE																															
R/W-0h																															

Table 3-128. M33SPARESOCLOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE	R/W	0h	Spare SOC LOCK Register 1

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49 M33SPARESOCLOCK2 Register (Offset = 141Ch) [Reset = 00000000h]

M33SPARESOCLOCK2 is shown in Figure 3-59 and described in Table 3-81.

Return to the Summary Table.

M33C1 Spare SOC LOCK Reg 2

Figure 3-59. M33SPARESOCLOCK2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE																															
R/W-0h																															

Table 3-130. M33SPARESOCLOCK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE	R/W	0h	Spare SOC LOCK Register 2

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50 SYSCTL_READ_REG Register (Offset = 1420h) [Reset = 00000000h]

SYSCTL_READ_REG is shown in Figure 3-60 and described in Table 3-82.

Return to the Summary Table.

Sysctl read only Reg

Figure 3-60. SYSCTL_READ_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ecoreg																															
R/W-0h																															

Table 3-132. SYSCTL_READ_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ecoreg	R/W	0h	Read only register

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51 PWREN_MCPERIPH Register (Offset = 1424h) [Reset = 00000000h]

PWREN_MCPERIPH is shown in Figure 3-61 and described in Table 3-83.

Return to the Summary Table.

Register to control the power state

Figure 3-61. PWREN_MCPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
HRPWM0	SDFM0	FSI_RX0	FSI_TX0	ETHERCAT_CORE0	ETPWM5	ETPWM4	ETPWM3
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ETPWM2	ETPWM1	ETPWM0	XBAR	CMPSS3	CMPSS2	CMPSS1	CMPSS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PWM2	PWM1	PWM0	ECAP2	ECAP1	ECAP0	EQEP1	EQEP0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-134. PWREN_MCPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0x26 26h = 0x26
23	HRPWM0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
22	SDFM0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
21	FSI_RX0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
20	FSI_TX0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
19	ETHERCAT_CORE0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
18	ETPWM5	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
17	ETPWM4	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
16	ETPWM3	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
15	ETPWM2	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power

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Table 3-134. PWREN_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ETPWM1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
13	ETPWM0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
12	XBAR	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
11	CMPSS3	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
10	CMPSS2	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
9	CMPSS1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
8	CMPSS0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
7	PWM2	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
6	PWM1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
5	PWM0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
4	ECAP2	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
3	ECAP1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
2	ECAP0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
1	EQEP1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
0	EQEP0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power

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52 RSTCTL_ASSERT_MCPERIPH Register (Offset = 1428h) [Reset = 00000000h]

RSTCTL_ASSERT_MCPERIPH is shown in Figure 3-62 and described in Table 3-84.

Return to the Summary Table.

rstctl assert register to control reset assertion - Write Only Register, Always Read as 0

Figure 3-62. RSTCTL_ASSERT_MCPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESETASSERT_HRPWM0	RESETASSERT_SDFM0	RESETASSERT_FSI_RX0	RESETASSERT_FSI_TX0	RESETASSERT_ETHERCAT_CORE0	RESETASSERT_ETPWM5	RESETASSERT_ETPWM4	RESETASSERT_ETPWM3
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
RESETASSERT_ETPWM2	RESETASSERT_ETPWM1	RESETASSERT_ETPWM0	RESETASSERT_XBAR	RESETASSERT_CMPSS3	RESETASSERT_CMPSS2	RESETASSERT_CMPSS1	RESETASSERT_CMPSS0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RESETASSERT_PWM2	RESETASSERT_PWM1	RESETASSERT_PWM0	RESETASSERT_ECAP2	RESETASSERT_ECAP1	RESETASSERT_ECAP0	RESETASSERT_EQEP1	RESETASSERT_EQEP0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-136. RSTCTL_ASSERT_MCPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0xb1 B1h = 0xb1
23	RESETASSERT_HRPWM0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
22	RESETASSERT_SDFM0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
21	RESETASSERT_FSI_RX0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
20	RESETASSERT_FSI_TX0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
19	RESETASSERT_ETHERCAT_CORE0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
18	RESETASSERT_ETPWM5	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset

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Table 3-136. RSTCTL_ASSERT_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	RESETASSERT_ETPWM4	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
16	RESETASSERT_ETPWM3	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
15	RESETASSERT_ETPWM2	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
14	RESETASSERT_ETPWM1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
13	RESETASSERT_ETPWM0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
12	RESETASSERT_XBAR	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
11	RESETASSERT_CMPSS3	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
10	RESETASSERT_CMPSS2	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
9	RESETASSERT_CMPSS1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
8	RESETASSERT_CMPSS0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
7	RESETASSERT_PWM2	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
6	RESETASSERT_PWM1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
5	RESETASSERT_PWM0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
4	RESETASSERT_ECAP2	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset

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Table 3-136. RSTCTL_ASSERT_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESETASSERT_ECAP1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
2	RESETASSERT_ECAP0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
1	RESETASSERT_EQEP1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
0	RESETASSERT_EQEP0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset

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53 RSTCTL_CLEAR_MCPERIPH Register (Offset = 142Ch) [Reset = 00000000h]

RSTCTL_CLEAR_MCPERIPH is shown in Figure 3-63 and described in Table 3-85.

Return to the Summary Table.

rstctl clear register to control reset de-assertion - Write Only Register, Always Read as 0

Figure 3-63. RSTCTL_CLEAR_MCPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESETSTKYCLR_HRPWM0	RESETSTKYCLR_SDFM0	RESETSTKYCLR_FSI_RX0	RESETSTKYCLR_FSI_TX0	RESETSTKYCLR_ETHERCAT_CORE0	RESETSTKYCLR_ETPWM5	RESETSTKYCLR_ETPWM4	RESETSTKYCLR_ETPWM3
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
RESETSTKYCLR_ETPWM2	RESETSTKYCLR_ETPWM1	RESETSTKYCLR_ETPWM0	RESETSTKYCLR_XBAR	RESETSTKYCLR_CMPSS3	RESETSTKYCLR_CMPSS2	RESETSTKYCLR_CMPSS1	RESETSTKYCLR_CMPSS0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RESETSTKYCLR_PWM2	RESETSTKYCLR_PWM1	RESETSTKYCLR_PWM0	RESETSTKYCLR_ECAP2	RESETSTKYCLR_ECAP1	RESETSTKYCLR_ECAP0	RESETSTKYCLR_EQEP1	RESETSTKYCLR_EQEP0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-138. RSTCTL_CLEAR_MCPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0xb1 B1h = 0xb1
23	RESETSTKYCLR_HRPWM0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
22	RESETSTKYCLR_SDFM0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
21	RESETSTKYCLR_FSI_RX0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
20	RESETSTKYCLR_FSI_TX0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
19	RESETSTKYCLR_ETHERCAT_CORE0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
18	RESETSTKYCLR_ETPWM5	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
17	RESETSTKYCLR_ETPWM4	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
16	RESETSTKYCLR_ETPWM3	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect

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Table 3-138. RSTCTL_CLEAR_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESETSTKYCLR_ETPWM2	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
14	RESETSTKYCLR_ETPWM1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
13	RESETSTKYCLR_ETPWM0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
12	RESETSTKYCLR_XBAR	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
11	RESETSTKYCLR_CMPSS3	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
10	RESETSTKYCLR_CMPSS2	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
9	RESETSTKYCLR_CMPSS1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
8	RESETSTKYCLR_CMPSS0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
7	RESETSTKYCLR_PWM2	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
6	RESETSTKYCLR_PWM1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
5	RESETSTKYCLR_PWM0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
4	RESETSTKYCLR_ECAP2	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
3	RESETSTKYCLR_ECAP1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
2	RESETSTKYCLR_ECAP0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
1	RESETSTKYCLR_EQEP1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
0	RESETSTKYCLR_EQEP0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect

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54 STAT_MCPERIPH Register (Offset = 1430h) [Reset = 00000000h]

STAT_MCPERIPH is shown in Figure 3-64 and described in Table 3-86.

Return to the Summary Table.

IP State Register - Read Only

Figure 3-64. STAT_MCPERIPH Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
HRPWM0	SDFM0	FSI_RX0	FSI_TX0	ETHERCAT_CORE0	ETPWM5	ETPWM4	ETPWM3
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
ETPWM2	ETPWM1	ETPWM0	XBAR	CMPSS3	CMPSS2	CMPSS1	CMPSS0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PWM2	PWM1	PWM0	ECAP2	ECAP1	ECAP0	EQEP1	EQEP0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-140. STAT_MCPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23	HRPWM0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
22	SDFM0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
21	FSI_RX0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
20	FSI_TX0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
19	ETHERCAT_CORE0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
18	ETPWM5	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear

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Table 3-140. STAT_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	ETPWM4	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
16	ETPWM3	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15	ETPWM2	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
14	ETPWM1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
13	ETPWM0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
12	XBAR	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
11	CMPSS3	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
10	CMPSS2	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
9	CMPSS1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
8	CMPSS0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
7	PWM2	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
6	PWM1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear

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Table 3-140. STAT_MCPERIPH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PWM0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
4	ECAP2	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
3	ECAP1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
2	ECAP0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
1	EQEP1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
0	EQEP0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear

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55 PWREN_SYSPERIPH Register (Offset = 1434h) [Reset = 00XXXXX0h]

PWREN_SYSPERIPH is shown in Figure 3-65 and described in Table 3-87.

Return to the Summary Table.

Register to control the power state

Figure 3-65. PWREN_SYSPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
R/W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED		ETHERCAT_SS0	EPI	PGA2	PGA1	PGA0	TINIE
R/W-XXXXh		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-142. PWREN_SYSPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0x26 26h = 0x26
23-6	RESERVED	R/W	XXXXh	
5	ETHERCAT_SS0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
4	EPI	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
3	PGA2	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
2	PGA1	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
1	PGA0	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power
0	TINIE	R/W	0h	Enable the power to IP, KEY must be set to 26h to write to this bit 0h = Disable Power 1h = Enable Power

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56 RSTCTL_ASSERT_SYSPERIPH Register (Offset = 1438h) [Reset = 00XXXXX0h]

RSTCTL_ASSERT_SYSPERIPH is shown in Figure 3-66 and described in Table 3-88.

Return to the Summary Table.

rstcl assert Register - Write Only Register, Always Read as 0

Figure 3-66. RSTCTL_ASSERT_SYSPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESETASSERT_EPI	RESETASSERT_PGA2	RESETASSERT_PGA1	RESETASSERT_PGA0	RESETASSERT_TINIE
W-XXXXh		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-144. RSTCTL_ASSERT_SYSPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0xb1 B1h = 0xb1
23-6	RESERVED	W	XXXXh	
5	RESERVED	W	0h	Reserved
4	RESETASSERT_EPI	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
3	RESETASSERT_PGA2	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
2	RESETASSERT_PGA1	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
1	RESETASSERT_PGA0	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset
0	RESETASSERT_TINIE	W	0h	assert reset to the peripheral, KEY must be set to B1h to write to this bit 0h = Writing 0 has no effect 1h = Assert reset

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57 RSTCTL_CLEAR_SYSPERIPH Register (Offset = 143Ch) [Reset = 00XXXXX0h]

RSTCTL_CLEAR_SYSPERIPH is shown in Figure 3-67 and described in Table 3-89.

Return to the Summary Table.

rstctl clear register to control reset de-assertion - Write Only Register, Always Read as 0

Figure 3-67. RSTCTL_CLEAR_SYSPERIPH Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESETSTKYCLR_EPI	RESETSTKYCLR_PGA2	RESETSTKYCLR_PGA1	RESETSTKYCLR_PGA0	RESETSTKYCLR_TINIE
W-XXXXh		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-146. RSTCTL_CLEAR_SYSPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to Allow Enable State Change -- 0xb1 B1h = 0xb1
23-6	RESERVED	W	XXXXh	
5	RESERVED	W	0h	Reserved
4	RESETSTKYCLR_EPI	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
3	RESETSTKYCLR_PGA2	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
2	RESETSTKYCLR_PGA1	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
1	RESETSTKYCLR_PGA0	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect
0	RESETSTKYCLR_TINIE	W	0h	Clear the RESETSTKY bit in the STAT register, KEY must be set to B1h to write to this bit 1h = Writing 0 has no effect

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58 STAT_SYSPERIPH Register (Offset = 1440h) [Reset = 00000000h]

STAT_SYSPERIPH is shown in Figure 3-68 and described in Table 3-90.

Return to the Summary Table.

IP State Register - Read Only

Figure 3-68. STAT_SYSPERIPH Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	EPI	PGA2	PGA1	PGA0	TINIE
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-148. STAT_SYSPERIPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	
5	RESERVED	R	0h	Reserved
4	EPI	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
3	PGA2	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
2	PGA1	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
1	PGA0	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
0	TINIE	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear

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59 CMPHPMXSEL Register (Offset = 1444h) [Reset = 00000000h]

CMPHPMXSEL is shown in Figure 3-69 and described in Table 3-91.

Return to the Summary Table.

Bits to select one of the many sources on CompHP inputs. Refer to Pinmux diagram for details.

Figure 3-69. CMPHPMXSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				CMP3HPMXSEL			CMP2HPMXSEL
R/W-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
CMP2HPMXSEL		CMP1HPMXSEL			CMP0HPMXSEL		
R/W-0h		R/W-0h			R/W-0h		

Table 3-150. CMPHPMXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	0h	
11-9	CMP3HPMXSEL	R/W	0h	CMP3HPMXSEL bits
8-6	CMP2HPMXSEL	R/W	0h	CMP2HPMXSEL bits
5-3	CMP1HPMXSEL	R/W	0h	CMP1HPMXSEL bits
2-0	CMP0HPMXSEL	R/W	0h	CMP0HPMXSEL bits

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60 CMPLPMXSEL Register (Offset = 144Ch) [Reset = 00000000h]

CMPLPMXSEL is shown in Figure 3-70 and described in Table 3-92.

Return to the Summary Table.

Bits to select one of the many sources on CompLP inputs. Refer to Pinmux diagram for details.

Figure 3-70. CMPLPMXSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				CMP3LPMXSEL			CMP2LPMXSEL
R/W-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
CMP2LPMXSEL			CMP1LPMXSEL			CMP0LPMXSEL	
R/W-0h			R/W-0h			R/W-0h	

Table 3-152. CMPLPMXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	0h	
11-9	CMP3LPMXSEL	R/W	0h	CMP3LPMXSEL bits
8-6	CMP2LPMXSEL	R/W	0h	CMP2LPMXSEL bits
5-3	CMP1LPMXSEL	R/W	0h	CMP1LPMXSEL bits
2-0	CMP0LPMXSEL	R/W	0h	CMP0LPMXSEL bits

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61 CMPHNMXSEL Register (Offset = 1450h) [Reset = 00000000h]

CMPHNMXSEL is shown in Figure 3-71 and described in Table 3-93.

Return to the Summary Table.

Bits to select one of the many sources on CompHN inputs. Refer to Pinmux diagram for details.

Figure 3-71. CMPHNMXSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				CMP3HNMXSEL	CMP2HNMXSEL	CMP1HNMXSEL	CMP0HNMXSEL
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-154. CMPHNMXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	CMP3HNMXSEL	R/W	0h	CMP3HNMXSEL bits
2	CMP2HNMXSEL	R/W	0h	CMP2HNMXSEL bits
1	CMP1HNMXSEL	R/W	0h	CMP1HNMXSEL bits
0	CMP0HNMXSEL	R/W	0h	CMP0HNMXSEL bits

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62 CMPLNMXSEL Register (Offset = 1454h) [Reset = 00000000h]

CMPLNMXSEL is shown in Figure 3-72 and described in Table 3-94.

Return to the Summary Table.

Bits to select one of the many sources on CompLN inputs. Refer to Pinmux diagram for details.

Figure 3-72. CMPLNMXSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				CMP3LNMXSEL	CMP2LNMXSEL	CMP1LNMXSEL	CMP0LNMXSEL
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-156. CMPLNMXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	CMP3LNMXSEL	R/W	0h	CMP3LNMXSEL bits
2	CMP2LNMXSEL	R/W	0h	CMP2LNMXSEL bits
1	CMP1LNMXSEL	R/W	0h	CMP1LNMXSEL bits
0	CMP0LNMXSEL	R/W	0h	CMP0LNMXSEL bits

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63 TSNSCFG Register (Offset = 1458h) [Reset = 00000000h]

TSNSCFG is shown in Figure 3-73 and described in Table 3-95.

Return to the Summary Table.

Temperature Sensor Config Register

Figure 3-73. TSNSCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-158. TSNSCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

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64 TSNSSCTL Register (Offset = 145Ch) [Reset = 00000000h]

TSNSSCTL is shown in Figure 3-74 and described in Table 3-96.

Return to the Summary Table.

Temperature Sensor Control Register

Figure 3-74. TSNSSCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/W-0h

Table 3-160. TSNSSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	ENABLE	R/W	0h	Temperature Sensor Enable

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65 INTERNALTESTCTL Register (Offset = 1468h) [Reset = 00000000h]

INTERNALTESTCTL is shown in Figure 3-75 and described in Table 3-97.

Return to the Summary Table.

Internal Test Node Control Register

Figure 3-75. INTERNALTESTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		TESTSEL					
R/W-0h		R/W-0h					

Table 3-162. INTERNALTESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8-6	RESERVED	R/W	0h	Reserved

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Table 3-162. INTERNALTESTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	TESTSEL	R/W	0h	Test Select 1h = VDDCORE 2h = VDDA 3h = VSSA 4h = VREFLOAC 5h = CDAC1H 6h = CDAC1L 7h = CDAC2H 8h = CDAC2H 9h = CDAC2H Ah = CDAC2H Bh = CDAC2H Ch = CDAC2H 1Dh = ENZ_CALIB_GAIN_3P3V will be made low. ADCA and ADCC will be in gain calibration mode, and 0.9xVREFHIAB pin voltage will be sampled by both ADCs through internal test-mux output 1Eh = CMPSS1 VDDA sense on TESTANA0,VSSA sense on TESTANA1 1Fh = ADCA VDDA sense on TESTANA0,VSSA sense on TESTANA1 20h = COMP DAC BUFFER VDDA sense on TESTANA0,VSSA sense on TESTANA1 21h = PGA1 VDDA sense on TESTANA0,VSSA sense on TESTANA1 22h = ADCCIO_TESTANA0_INT 23h = PMM/HPLL/INTOSC TESTANA0_INT 24h = ADCCIO_TESTANA1_INT 25h = PMM/HPLL/INTOSC TESTANA1_INT 26h = Enable resistor for I2V conversion. The same control enables the sampling of voltage across a resistor by ADC. R=2.5k, 38: R=10k, 39: R=35k 29h = USB_TESTANA0_INT 2Ah = USB_TESTANA1_INT 2Bh = USB_TESTANA0_INT & USB_TESTANA1_INT 2Ch = VSS 2Dh = Bring FLT3 & TESTPAD3 of flash on TESTANA1 2Eh = Enable resistor for I2V conversion. The same control enables the sampling of voltage across a resistor by ADC. R=2.5k, 47: R=10k, 48: R=35k 31h = VREFLOAC

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66 XTALCR Register (Offset = 1474h) [Reset = 00000001h]

XTALCR is shown in Figure 3-76 and described in Table 3-98.

Return to the Summary Table.

XTAL Control Register

Figure 3-76. XTALCR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SE	OSCOFF
R/W-0h						R/W-0h	R/W-1h

Table 3-164. XTALCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SE	R/W	0h	XTAL Oscilator in Single-Ended 0h = XTAL oscillator in Crystal mode 1h = XTAL oscilator in single-ended mode (through X1)
0	OSCOFF	R/W	1h	This bit if 1, powers-down the XTAL oscillator macro and hence doesnt let X2 to be driven by the XTAL oscillator. If a crystal is connected to X1/X2, user needs to first clear this bit, wait for the oscillator to power up (using X1CNT) and then only switch the clock source to X1/X2 0h = XTAL Oscillator powered-up using X1/X2 1h = XTAL Oscillator powered-down

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67 XTALCR2 Register (Offset = 1478h) [Reset = 0000XXXXh]

XTALCR2 is shown in Figure 3-77 and described in Table 3-99.

Return to the Summary Table.

XTAL Control Register for pad init

Figure 3-77. XTALCR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FKEEPXI															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													FEN	XOF	XIF
R/W-XXXh													R/W-0h	R/W-1h	R/W-1h

Table 3-166. XTALCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FKEEPXI	R/W	0h	This field when written 0xface allows to hold the force value on XI as programmed on XIF. 0xface: Force on XI is continued as per XIF value regardless of XOSC ON/OFF state only in XTAL mode. In Single ended mode this field has no impact. Any other value: Force on XI is removed with enabling of XOSC as per FEN function.
15-3	RESERVED	R/W	XXXh	
2	FEN	R/W	0h	XOSC pads initialisation enable. Configures XTAL oscillator pad initilisation. This register has effect only when XOSC is OFF (no SE , no XTAL mode). If this register is set during XOSC off state (XOSCOFF=1 & SE=0) then upon change of these controls this bit gets reset and rearmed 0h = XOSC pads are not driven through GPIO connection. 1h = XOSC pads are driven through connected GPIO as per XIF & XOF values.
1	XOF	R/W	1h	XO Initial value deposited before XOSC start. Polarity selection to initialise XO/X2 pad of the XOSC before start-up. This value shall be deposited on the pad before XOSC started (XOSCOFF=1). If FEN=0 or XOSC is in XTAL or SE mode then this value will not be applied to the pad.
0	XIF	R/W	1h	XI Initial value deposited before XOSC start. Polarity selection to initialise XI/X1 pad of the XOSC before start-up. This value shall be deposited on the pad before XOSC started (XOSCOFF=1). If FEN=0 or XOSC is in XTAL or SE mode then this value will not be applied to the pad.

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68 X1CNT Register (Offset = 147Ch) [Reset = 0000XX00h]

X1CNT is shown in Figure 3-78 and described in Table 3-100.

Return to the Summary Table.

x1cnt status register

Figure 3-78. X1CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															CLR
R/W-0h															W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					X1CNT										
R/W-Xh					R-0h										

Table 3-168. X1CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	0h	
16	CLR	W	0h	X1 Counter clear: A write of 1 to this bit field clears the X1CNT and makes it count from 0x0 again (provided X1 clock is ticking). Writes of 0 are ignore to this bit field
15-11	RESERVED	R/W	Xh	
10-0	X1CNT	R	0h	This counter increments on every X1 CLOCKs positive-edge. Once it reaches the values of 0x7ff, it freezes. Before switching from SYSOSC/PLL clock to X1, application must check this counter and make sure that it has saturated. This will ensure that the Crystal connected to X1/X2 is oscillating

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69 CMPSSCTL Register (Offset = 1480h) [Reset = XXXXXXXXh]

CMPSSCTL is shown in Figure 3-79 and described in Table 3-101.

Return to the Summary Table.

CMPSS control register

Figure 3-79. CMPSSCTL Register

31	30	29	28	27	26	25	24
CMPSSCTLEN	RESERVED						
R/W-0h	R/W-000XXXXXh						
23	22	21	20	19	18	17	16
RESERVED							
R/W-000XXXXXh							
15	14	13	12	11	10	9	8
RESERVED							
R/W-000XXXXXh							
7	6	5	4	3	2	1	0
RESERVED						CMP3LDACOUTEN	CMP2LDACOUTEN
R/W-000XXXXXh						R/W-0h	R/W-0h

Table 3-170. CMPSSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMPSSCTLEN	R/W	0h	Enable the CMPSSCTL Register
30-2	RESERVED	R/W	XXXXh	
1	CMP3LDACOUTEN	R/W	0h	Enable general purpose DAC functionality for CMPSS3 COMPDACL
0	CMP2LDACOUTEN	R/W	0h	Enable general purpose DAC functionality for CMPSS2 COMPDACL

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70 ANAREFCTL Register (Offset = 1488h) [Reset = 000000XXh]

ANAREFCTL is shown in Figure 3-80 and described in Table 3-102.

Return to the Summary Table.

Analog Reference Select

Figure 3-80. ANAREFCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							ANAREF2P5SEL
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					RESERVED	RESERVED	ANAREFSEL
R/W-Xh					R/W-0h	R/W-0h	R/W-1h

Table 3-172. ANAREFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	ANAREF2P5SEL	R/W	0h	Analog reference 2.5V source select. In internal reference mode, this bit selects which voltage the internal reference buffer drives onto the VREFHI pin. The buffer can drive either 1.65V onto the pin, resulting in a reference range of 0 to 3.3V, or the buffer can drive 2.5V onto the pin, resulting in a reference range of 0 to 2.5V. If switching between these two modes, the user must allow adequate time for the external capacitor to charge to the new voltage before using the ADC or buffered DAC. 0 - Internal 1.65V reference mode (3.3V reference range) 1 - Internal 2.5V reference mode (2.5V reference range)
7-3	RESERVED	R/W	Xh	
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	ANAREFSEL	R/W	1h	Analog reference mode select. This bit selects whether the VREFHI pin uses internal reference mode (the device drives a voltage onto the VREFHI pin) or external reference mode (the system is expected to drive a voltage into the VREFHI pin). 0 - Internal reference mode 1 - External reference mode

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71 PERCLKCR Register (Offset = 148Ch) [Reset = 00000000h]

PERCLKCR is shown in Figure 3-81 and described in Table 3-103.

Return to the Summary Table.

PWM Time Base Clock sync

Figure 3-81. PERCLKCR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							TBCLKSYNC
R/W-0h							R/W-0h

Table 3-174. PERCLKCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	TBCLKSYNC	R/W	0h	PWM Time Base Clock sync: When set PWM time bases of all the PWM modules belonging to the same CPU-Subsystem (as partitioned using their CPUSEL bits) start counting

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72 AM13SPAREIREFENSOCLOCK Register (Offset = 14A0h) [Reset = 00000000h]

AM13SPAREIREFENSOCLOCK is shown in Figure 3-82 and described in Table 3-104.

Return to the Summary Table.

AM13 Spare IREFEN SOC LOCK Reg

Figure 3-82. AM13SPAREIREFENSOCLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SPARE					
R/W-0h																										R/W-0h					

Table 3-176. AM13SPAREIREFENSOCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-0	SPARE	R/W	0h	Spare IREFEN SOC LOCK Register

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73 AM13SPARESOCLOCK2 Register (Offset = 14A4h) [Reset = 0000003Eh]

AM13SPARESOCLOCK2 is shown in Figure 3-83 and described in Table 3-105.

Return to the Summary Table.

AM13 Spare SOC LOCK Reg 2

Figure 3-83. AM13SPARESOCLOCK2 Register

31	30	29	28	27	26	25	24
SPARE							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE		SRAM5_STATIC_MUX_SEL	SRAM4_STATIC_MUX_SEL	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h		R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

Table 3-178. AM13SPARESOCLOCK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	SPARE	R/W	0h	Spare SOC LOCK Register 2
5	SRAM5_STATIC_MUX_SEL	R/W	1h	SRAM5 static mux select between CBUS and SBUS 0h = SBUS path is selected 1h = CBUS path is selected
4	SRAM4_STATIC_MUX_SEL	R/W	1h	SRAM4 static mux select between CBUS and SBUS 0h = SBUS path is selected 1h = CBUS path is selected
3	RESERVED	R/W	1h	Reserved
2	RESERVED	R/W	1h	Reserved
1	RESERVED	R/W	1h	Reserved
0	RESERVED	R/W	0h	Reserved

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74 AM13SPARESOCLOCK3 Register (Offset = 14A8h) [Reset = 00000000h]

AM13SPARESOCLOCK3 is shown in Figure 3-84 and described in Table 3-106.

Return to the Summary Table.

AM13 Spare SOC LOCK Reg 3

Figure 3-84. AM13SPARESOCLOCK3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE																															
R/W-0h																															

Table 3-180. AM13SPARESOCLOCK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE	R/W	0h	Spare SOC LOCK Register 3

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75 AM13SPARESOCLOCK4 Register (Offset = 14ACh) [Reset = 00000000h]

AM13SPARESOCLOCK4 is shown in Figure 3-85 and described in Table 3-107.

Return to the Summary Table.

AM13 Spare SOC LOCK Reg 4

Figure 3-85. AM13SPARESOCLOCK4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE																															
R/W-0h																															

Table 3-182. AM13SPARESOCLOCK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE	R/W	0h	Spare SOC LOCK Register 4

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76 ETHERCATCLKCTL Register (Offset = 14B0h) [Reset = 000000XXh]

ETHERCATCLKCTL is shown in Figure 3-86 and described in Table 3-108.

Return to the Summary Table.

EtherCAT Clock Control

Figure 3-86. ETHERCATCLKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHYCLKEN
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
ECAT100CLKEN	RESERVED			ECATDIV			RESERVED
R/W-1h	R/W-Xh			R/W-7h			R/W-Xh

Table 3-184. ETHERCATCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	PHYCLKEN	R/W	0h	etherCAT PHY clock enable 0h = etherCAT phy clock disabled 1h = etherCAT phy clock enabled
7	ECAT100CLKEN	R/W	1h	etherCAT 100 clock enable 0h = etherCAT 100 clock disabled 1h = etherCAT 100 clock enabled
6-4	RESERVED	R/W	Xh	
3-1	ECATDIV	R/W	7h	etherCAT clock divider configuration
0	RESERVED	R/W	Xh	

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77 ETHERCATCTL Register (Offset = 14B4h) [Reset = 000000XXh]

ETHERCATCTL is shown in Figure 3-87 and described in Table 3-109.

Return to the Summary Table.

ETHERCAT control register

Figure 3-87. ETHERCATCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							I2CLOOPBACK
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-XXh							

Table 3-186. ETHERCATCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	I2CLOOPBACK	R/W	0h	Loopback I2C port of etherCAT IP to I2C_A 0h = I2C port of etherCAT is not looped back to I2C_A 1h = I2C port of etherCAT is looped back to I2C_A
7-0	RESERVED	R/W	XXh	

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78 SDFMTYPE Register (Offset = 14B8h) [Reset = 00000000h]

SDFMTYPE is shown in Figure 3-88 and described in Table 3-110.

Return to the Summary Table.

Configures SDFM type for the device

Figure 3-88. SDFMTYPE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SDFMTYPE	
R/W-0h						R/W-0h	

Table 3-188. SDFMTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	SDFMTYPE	R/W	0h	Based on the configuration enables or disables features associated with the SDFM type. 0h = 1. Data Ready conditions combined with the fault conditions on the SDFM interrupt line. 2. Data ready interrupts from individual filters are not generated. 1h = 1. Data Ready conditions do not generate the SDFMINT. 2. Each filter generates a separate data ready interrupts. Ah = 1. Data Ready conditions combined with the fault conditions on the SDFM interrupt line. 2. Data ready interrupts from individual filters are not generated. Bh = 1. Data Ready conditions combined with the fault conditions on the SDFM interrupt line. 2. Data ready interrupts from individual filters are not generated.

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79 FLBANKSWPPOLICY Register (Offset = 3038h) [Reset = 00XXXXXXh]

FLBANKSWPPOLICY is shown in Figure 3-89 and described in Table 3-111.

Return to the Summary Table.

Flash Bank Swap Policy

Figure 3-89. FLBANKSWPPOLICY Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							DISABLE
W-XXXXh							W-0h

Table 3-190. FLBANKSWPPOLICY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Must have KEY==0xCA(202) for write CAh = Write Key
23-1	RESERVED	W	XXXXh	
0	DISABLE	W	0h	1: Disables Policy To Allow Flash Bank Swapping 1h = Disallow Bank Swap

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80 FLBANKSWP Register (Offset = 303Ch) [Reset = 00XXXXXXh]

FLBANKSWP is shown in Figure 3-90 and described in Table 3-112.

Return to the Summary Table.

Flash MAIN bank address swap

Figure 3-90. FLBANKSWP Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							USEUPPER
W-XXXXh							W-0h

Table 3-192. FLBANKSWP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	The key value of 58h (88) must be written with USEUPPER to change the bank swap configuration. 58h = Issue write
23-1	RESERVED	W	XXXXh	
0	USEUPPER	W	0h	1: Use Upper Bank as Logical 0 0h = Normal (default) memory map addressing scheme 1h = Flash upper region address space swapped with lower region

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81 SECSTATUS Register (Offset = 3048h) [Reset = 00000XXXh]

SECSTATUS is shown in Figure 3-91 and described in Table 3-113.

Return to the Summary Table.

Security Configuration status

Figure 3-91. SECSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			FLBANKSWP	RESERVED	FLBANKSWPPOLICY	RESERVED	
R-0h			R-0h	R-Xh	R-0h	R-Xh	
7	6	5	4	3	2	1	0
RESERVED					CSCEXISTS	RESERVED	INITDONE
R-Xh					R-1h	R-Xh	R-0h

Table 3-194. SECSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	
12	FLBANKSWP	R	0h	1: Upper and Lower Banks have been swapped
11	RESERVED	R	Xh	
10	FLBANKSWPPOLICY	R	0h	1: Upper and Lower Banks allowed to be swapped 0h = 0 1h = 1
9-3	RESERVED	R	Xh	
2	CSCEXISTS	R	1h	1: CSC Exists in the system 0h = System does not have a CSC 1h = System does have a CSC
1	RESERVED	R	Xh	
0	INITDONE	R	0h	1: CSC has been completed 0h = INIT is not yet done 1h = INIT is done

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82 INITDONE Register (Offset = 3060h) [Reset = 00XXXXXXh]

INITDONE is shown in Figure 3-92 and described in Table 3-114.

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INITCODE PASS

Figure 3-92. INITDONE Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-XXXXh							
15	14	13	12	11	10	9	8
RESERVED							
W-XXXXh							
7	6	5	4	3	2	1	0
RESERVED							PASS
W-XXXXh							W-0h

Table 3-196. INITDONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Must have KEY==0x9D(157) for write 9Dh = Issue Reset
23-1	RESERVED	W	XXXXh	
0	PASS	W	0h	INITCODE writes 1 for PASS, left unwritten a timeout will occur if not blocked 1h = INITCODE PASS

3.11 MEMCFG Registers

This Section describes the MEMCFG Registers.

3.11.1 MEMCFG Base Address Table

Table 3-197. MEMCFG Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
MemcfgRegs	MEM_CFG_REGS	MEMCFG	0x4002_A000

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3.11.2 MEM_CFG_REGS Registers

Table 3-116 lists the memory-mapped registers for the MEM_CFG_REGS registers. All register offset addresses not listed in Table 3-116 should be considered as reserved locations and the register contents should not be modified.

Table 3-198. MEM_CFG_REGS Registers

Offset	Acronym	Register Name	Group	Section
1000h	TEST	RAM TEST Register		Go
1014h	TMUROM_TEST	TMUROM TEST Register		Go
1018h	ECATRAM_TEST	ETHERCAT RAM TEST Register		Go

Complex bit access types are encoded to fit into small table cells. Table 3-117 shows the codes that are used for access types in this section.

Table 3-199. MEM_CFG_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 TEST Register (Offset = 1000h) [Reset = 00000000h]

TEST is shown in Figure 3-93 and described in Table 3-118.

Return to the Summary Table.

RAM TEST Register

Figure 3-93. TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED				TEST_SRAM5		TEST_SRAM4	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
TEST_SRAM3		TEST_SRAM2		TEST_SRAM1		TEST_SRAM0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 3-201. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	TEST_SRAM5	R/W	0h	Selects the defferent modes for SRAM5: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST
9-8	TEST_SRAM4	R/W	0h	Selects the defferent modes for SRAM4: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST
7-6	TEST_SRAM3	R/W	0h	Selects the defferent modes for SRAM3: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST
5-4	TEST_SRAM2	R/W	0h	Selects the defferent modes for SRAM2: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST

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Table 3-201. TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	TEST_SRAM1	R/W	0h	Selects the defferent modes for SRAM1: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST
1-0	TEST_SRAM0	R/W	0h	Selects the defferent modes for SRAM0: 00: Functional Mode. 01: Writes are allowed to data bits only. No write to parity bits. 10: Writes are allowed to parity bits only. No write to data bits. 11: Same as functional mode Reset type: SYSRST

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2 TMUROM_TEST Register (Offset = 1014h) [Reset = 00000005h]

TMUROM_TEST is shown in Figure 3-94 and described in Table 3-119.

Return to the Summary Table.

TMUROM TEST Register

Figure 3-94. TMUROM_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				TMUROM_PAR_FORCE			
R-0-0h				R/W-5h			

Table 3-203. TMUROM_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3-0	TMUROM_PAR_FORCE	R/W	5h	TMUROM Parity Error Force: 0xA: Error forced Others: No error forced Reset type: SYSRST

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3 ECATRAM_TEST Register (Offset = 1018h) [Reset = 00000005h]

ECATRAM_TEST is shown in Figure 3-95 and described in Table 3-120.

Return to the Summary Table.

ETHERCAT RAM TEST Register

Figure 3-95. ECATRAM_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				ECATRAM_PAR_FORCE			
R-0-0h				R/W-5h			

Table 3-205. ECATRAM_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3-0	ECATRAM_PAR_FORCE	R/W	5h	ETHERCAT RAM Parity Error Force: 0xA: Error forced Others: No error forced Reset type: SYSRST

3.12 FACTORY Registers

This Section describes the FACTORY Registers.

3.12.1 FACTORY Base Address Table

Table 3-206. FACTORY Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
FactoryRegs	FACTORY_REGION_REGS	FACTORY	0x6011_1000

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3.12.2 FACTORY_REGION_REGS Registers

Table 3-122 lists the memory-mapped registers for the FACTORY_REGION_REGS registers. All register offset addresses not listed in Table 3-122 should be considered as reserved locations and the register contents should not be modified.

Table 3-207. FACTORY_REGION_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	TRACEID	Defined by TI, during ATE, based on wafer		Go
4h	DEVICEID	This is the JTAGIDCODE that comes from the Ramp system		Go
8h	USERID	Defined by TI, depending on device spin		Go
Ch	BSLPIN_UART	BSL UART Pin Configuration		Go
10h	BSLPIN_I2C	BSL I2C Pin Configuration		Go
14h	BSLPIN_CAN	BSL UART Pin Configuration		Go
18h	BSLPIN_INVOKE	BSL Pin Invocation Configuration		Go
1Ch	ROM_SRAMFLASH	Number of banks , sram size and flash size		Go
20h	PLLSTARTUP0_4_8MHZ			Go
24h	PLLSTARTUP1_4_8MHZ	System PLL Paramater 1 MMR --- Data from Flash Table Lookup		Go
28h	PLLSTARTUP0_8_16MHZ			Go
2Ch	PLLSTARTUP1_8_16MHZ	System PLL Paramater 1 MMR --- Data from Flash Table Lookup		Go
30h	PLLSTARTUP0_16_32MHZ			Go
34h	PLLSTARTUP1_16_32MHZ	System PLL Paramater 1 MMR --- Data from Flash Table Lookup		Go
38h	PLLSTARTUP0_32_48MHZ			Go
3Ch	PLLSTARTUP1_32_48MHZ	System PLL Paramater 1 MMR --- Data from Flash Table Lookup		Go
40h	TEMP_SENSE0	Temperature sensor room temperature calibration code. This is ADC conversion results of temperature sensor output voltage. Included in BOOTCRC calculation.		Go
4Ch	ROM_VERSION			Go
50h	ROM_INM_VERSION			Go
54h	SYSPLLPARAM2			Go
58h	SYSPLLLDOCTL			Go
5Ch	SYSPLLLDOPROG			Go
60h	EXTREF_MP3	External Reference MP3 Temp Sense		Go
64h	INTREF_MP3	Internal Refernce Temp Sene		Go
68h	TSCODE_MP1	Tempsense Code MP1		Go
6Ch	TSCODE_MP3	Tempsense code MP3		Go
70h	TSTEMP	Temperature sense TEMP		Go
74h	SRAMFLASH	Number of banks , sram size and flash size		Go

Complex bit access types are encoded to fit into small table cells. Table 3-123 shows the codes that are used for access types in this section.

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Table 3-208. FACTORY_REGION_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

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1 TRACEID Register (Offset = 0h) [Reset = 00000000h]

TRACEID is shown in Figure 3-96 and described in Table 3-124.

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unique per part shipped, done per established TI process

Figure 3-96. TRACEID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 3-210. TRACEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	

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2 DEVICEID Register (Offset = 4h) [Reset = 1BBB702Fh]

DEVICEID is shown in Figure 3-97 and described in Table 3-125.

Return to the Summary Table.

per Connectivity format, provisioned from RAMP and is die rev specific

Figure 3-97. DEVICEID Register

31	30	29	28	27	26	25	24
VERSION				PARTNUM			
R-1h				R-BBB7h			
23	22	21	20	19	18	17	16
PARTNUM							
R-BBB7h							
15	14	13	12	11	10	9	8
PARTNUM				MANUFACTURER			
R-BBB7h				R-17h			
7	6	5	4	3	2	1	0
MANUFACTURER							ALWAYS_1
R-17h							R-1h

Table 3-212. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	VERSION	R	1h	Revision of the device. This field should change each time that the logic or mask set of the device is revised.
27-12	PARTNUM	R	BBB7h	Part number of the device.
11-1	MANUFACTURER	R	17h	TI's JEDEC bank and company code, which is: 00000010111b
0	ALWAYS_1	R	1h	This is always 1

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3 USERID Register (Offset = 8h) [Reset = 00000000h]

USERID is shown in Figure 3-98 and described in Table 3-126.

Return to the Summary Table.

per Connectivity format, defines the variant feature set

Figure 3-98. USERID Register

31	30	29	28	27	26	25	24
START	MAJORREV			MINORREV			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
VARIANT							
R-0h							
15	14	13	12	11	10	9	8
PART							
R-0h							
7	6	5	4	3	2	1	0
PART							
R-0h							

Table 3-214. USERID Register Field Descriptions

Bit	Field	Type	Reset	Description
31	START	R	1h	
30-28	MAJORREV	R	0h	Monotonic increasing value indicating a new revision of the SKU significant enough that users of the device may have to revise PCB or or software design
27-24	MINORREV	R	0h	Monotonic increasing value indicating a new revision of the SKU that preserves compatibility with lesser minorrev values. New capability may be introduced such that lesser minorrev numbers may not be compatible with greater if the new capability is used.
23-16	VARIANT	R	0h	Bit pattern uniquely identifying a variant of a part. This is used to indicate memory or package variations of the same part number. This number shall be selected at random among the remaining numbers for the relevant combination of IDCODE.device and USERCODE.part such that the order of creation cannot be inferred by the number. The variant number does not encode specifics of the variant directly.
15-0	PART	R	0h	Bit pattern that uniquely identifying a part. This is used to identify the specific part based on the die identified in DEVICEID.device. This number shall be selected at random among the remaining numbers for DEVICEID.device such that the order of creation cannot be inferred by the number. This value does not encode the part number directly.

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4 BSLPIN_UART Register (Offset = Ch) [Reset = 00000000h]

BSLPIN_UART is shown in Figure 3-99 and described in Table 3-127.

Return to the Summary Table.

BSL UART Pin Configuration

Figure 3-99. BSLPIN_UART Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UART_TXD_PF								UART_TXD_PAD							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART_RXD_PF								UART_RXD_PAD							
R-0h								R-0h							

Table 3-216. BSLPIN_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	UART_TXD_PF	R	07h	UART TXD Pin Function Selection Value
23-16	UART_TXD_PAD	R	00h	UART TXD Pin used by BSL
15-8	UART_RXD_PF	R	07h	UART RXD Pin Function Selection Value
7-0	UART_RXD_PAD	R	01h	UART RXD Pad used by BSL

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5 BSLPIN_I2C Register (Offset = 10h) [Reset = 00000000h]

BSLPIN_I2C is shown in Figure 3-100 and described in Table 3-128.

Return to the Summary Table.

BSL I2C Pin Configuration

Figure 3-100. BSLPIN_I2C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I2C_SCL_PF								I2C_SCL_PAD							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_SDA_PF								I2C_SDA_PAD							
R-0h								R-0h							

Table 3-218. BSLPIN_I2C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	I2C_SCL_PF	R	04h	I2C SCL Pin Function Selection Value
23-16	I2C_SCL_PAD	R	17h	I2C SCL Pin used by BSL
15-8	I2C_SDA_PF	R	4h	I2C SDA Pin Function Selection Value
7-0	I2C_SDA_PAD	R	16h	I2C SDA Pin used by BSL

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6 BSLPIN_CAN Register (Offset = 14h) [Reset = 00000000h]

BSLPIN_CAN is shown in Figure 3-101 and described in Table 3-129.

Return to the Summary Table.

BSL UART Pin Configuration

Figure 3-101. BSLPIN_CAN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CAN_TX_PF								CAN_TX_PAD							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAN_RX_PF								CAN_RX_PAD							
R-0h								R-0h							

Table 3-220. BSLPIN_CAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CAN_TX_PF	R	0Ah	MCAN TX Pin Function Selection Value
23-16	CAN_TX_PAD	R	0Ch	MCAN TX Pin used by BSL
15-8	CAN_RX_PF	R	0Ah	MCAN RX Pin Function Selection Value
7-0	CAN_RX_PAD	R	0Bh	MCAN RX Pin used by BSL

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7 BSLPIN_INVOKE Register (Offset = 18h) [Reset = 00000000h]

BSLPIN_INVOKE is shown in Figure 3-102 and described in Table 3-130.

Return to the Summary Table.

BSL Pin Invocation Configuration

Figure 3-102. BSLPIN_INVOKE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	GPIO_REG_SEL		GPIO_PIN_SEL				
R-0h	R-0h		R-0h				
7	6	5	4	3	2	1	0
GPIO_LEVEL	BSL_PAD						
R-0h	R-0h						

Table 3-222. BSLPIN_INVOKE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	
14-13	GPIO_REG_SEL	R	AAh	GPIO Module Selection
12-8	GPIO_PIN_SEL	R	BBh	GPIO Pin Number in GPIO Module
7	GPIO_LEVEL	R	06h	GPIO Level Configuration for BSL Invocation
6-0	BSL_PAD	R	86h	BSL Invocation Pin Number

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8 ROM_SRAMFLASH Register (Offset = 1Ch) [Reset = 00000000h]

ROM_SRAMFLASH is shown in Figure 3-103 and described in Table 3-131.

Return to the Summary Table.

Number of banks , sram size and flash size

Figure 3-103. ROM_SRAMFLASH Register

31	30	29	28	27	26	25	24
DATAFLASH_SZ						SRAM_SZ	
R-0h						R-0h	
23	22	21	20	19	18	17	16
SRAM_SZ							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		MAINNUMBANKS		MAINFLASH_SZ			
R-0h		R-0h		R-0h			
7	6	5	4	3	2	1	0
MAINFLASH_SZ							
R-0h							

Table 3-224. ROM_SRAMFLASH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	DATAFLASH_SZ	R	00h	The encoding of the field is that the value of the field is an integer to be interpreted as number of KBs. For eg: if the value of the field id 4, then it is 4KB, if the value is 32, then 32KB, and so on.
25-16	SRAM_SZ	R	020h	The encoding of the field is that the value of the field is an integer to be interpreted as number of KBs. For eg: if the value of the field id 4, then it is 4KB, if the value is 32, then 32KB, and so on.
15-14	RESERVED	R	0h	
13-12	MAINNUMBANKS	R	2h	Defines the number of main flash banks
11-0	MAINFLASH_SZ	R	200h	The encoding of the field is that the value of the field is an integer to be interpreted as number of KBs. For eg: if the value of the field id 4, then it is 4KB, if the value is 32, then 32KB, and so on.

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9 PLLSTARTUP0_4_8MHZ Register (Offset = 20h) [Reset = 00000000h]

PLLSTARTUP0_4_8MHZ is shown in Figure 3-104 and described in Table 3-132.

Return to the Summary Table.

Figure 3-104. PLLSTARTUP0_4_8MHZ Register

31	30	29	28	27	26	25	24
CAPBOVERRIDE	RESERVED			CAPBVAL			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
RESERVED		CPCURRENT					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESERVED		STARTTIMELP					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RESERVED		STARTTIME					
R-0h		R-0h					

Table 3-226. PLLSTARTUP0_4_8MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAPBOVERRIDE	R	1h	Override Enable For Cap B 0h = 0 1h = 1
30-29	RESERVED	R	0h	
28-24	CAPBVAL	R	1h	Override Value for Cap B
23-22	RESERVED	R	0h	
21-16	CPCURRENT	R	Ah	Charge Pump Current
15-14	RESERVED	R	0h	
13-8	STARTTIMELP	R	16h	Startup time from Low Power Exit to Locked Clock in resolution of 1usec
7-6	RESERVED	R	0h	
5-0	STARTTIME	R	16h	Startup time from Enable to Locked Clock in resolution of 1usec

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10 PLLSTARTUP1_4_8MHZ Register (Offset = 24h) [Reset = 00000000h]

PLLSTARTUP1_4_8MHZ is shown in Figure 3-105 and described in Table 3-133.

Return to the Summary Table.

Figure 3-105. PLLSTARTUP1_4_8MHZ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPFRESC								RESERVED						LPFRESA	
R-0h								R-0h						R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPFRESA								RESERVED			LPFCAPA				
R-0h								R-0h			R-0h				

Table 3-228. PLLSTARTUP1_4_8MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LPFRESC	R	FFh	Loop Filter Res C
23-18	RESERVED	R	0h	
17-8	LPFRESA	R	4h	Loop Filter Res A
7-5	RESERVED	R	0h	
4-0	LPFCAPA	R	1Fh	Loop Filter Cap A

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11 PLLSTARTUP0_8_16MHZ Register (Offset = 28h) [Reset = 00000000h]

PLLSTARTUP0_8_16MHZ is shown in Figure 3-106 and described in Table 3-134.

Return to the Summary Table.

Figure 3-106. PLLSTARTUP0_8_16MHZ Register

31	30	29	28	27	26	25	24
CAPBOVERRIDE	RESERVED			CAPBVAL			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
RESERVED			CPCURRENT				
R-0h			R-0h				
15	14	13	12	11	10	9	8
RESERVED			STARTTIMELP				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED			STARTTIME				
R-0h			R-0h				

Table 3-230. PLLSTARTUP0_8_16MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAPBOVERRIDE	R	1h	Override Enable For Cap B 0h = 0 1h = 1
30-29	RESERVED	R	0h	
28-24	CAPBVAL	R	1h	Override Value for Cap B
23-22	RESERVED	R	0h	
21-16	CPCURRENT	R	Ah	Charge Pump Current
15-14	RESERVED	R	0h	
13-8	STARTTIMELP	R	16h	Startup time from Low Power Exit to Locked Clock in resolution of 1usec
7-6	RESERVED	R	0h	
5-0	STARTTIME	R	16h	Startup time from Enable to Locked Clock in resolution of 1usec

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12 PLLSTARTUP1_8_16MHZ Register (Offset = 2Ch) [Reset = 00000000h]

PLLSTARTUP1_8_16MHZ is shown in Figure 3-107 and described in Table 3-135.

Return to the Summary Table.

Figure 3-107. PLLSTARTUP1_8_16MHZ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPFRESC								RESERVED						LPFRESA	
R-0h								R-0h						R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPFRESA								RESERVED			LPFCAPA				
R-0h								R-0h			R-0h				

Table 3-232. PLLSTARTUP1_8_16MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LPFRESC	R	FFh	Loop Filter Res C
23-18	RESERVED	R	0h	
17-8	LPFRESA	R	4h	Loop Filter Res A
7-5	RESERVED	R	0h	
4-0	LPFCAPA	R	Fh	Loop Filter Cap A

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13 PLLSTARTUP0_16_32MHZ Register (Offset = 30h) [Reset = 00000000h]

PLLSTARTUP0_16_32MHZ is shown in Figure 3-108 and described in Table 3-136.

Return to the Summary Table.

Figure 3-108. PLLSTARTUP0_16_32MHZ Register

31	30	29	28	27	26	25	24
CAPBOVERRIDE	RESERVED			CAPBVAL			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
RESERVED		CPCURRENT					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESERVED		STARTTIMELP					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RESERVED		STARTTIME					
R-0h		R-0h					

Table 3-234. PLLSTARTUP0_16_32MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAPBOVERRIDE	R	1h	Override Enable For Cap B 0h = 0 1h = 1
30-29	RESERVED	R	0h	
28-24	CAPBVAL	R	1h	Override Value for Cap B
23-22	RESERVED	R	0h	
21-16	CPCURRENT	R	Ah	Charge Pump Current
15-14	RESERVED	R	0h	
13-8	STARTTIMELP	R	16h	Startup time from Low Power Exit to Locked Clock in resolution of 1usec
7-6	RESERVED	R	0h	
5-0	STARTTIME	R	16h	Startup time from Enable to Locked Clock in resolution of 1usec

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14 PLLSTARTUP1_16_32MHZ Register (Offset = 34h) [Reset = 00000000h]

PLLSTARTUP1_16_32MHZ is shown in Figure 3-109 and described in Table 3-137.

Return to the Summary Table.

Figure 3-109. PLLSTARTUP1_16_32MHZ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPFRESC								RESERVED						LPFRESA	
R-0h								R-0h						R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPFRESA								RESERVED			LPFCAPA				
R-0h								R-0h			R-0h				

Table 3-236. PLLSTARTUP1_16_32MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LPFRESC	R	FFh	Loop Filter Res C
23-18	RESERVED	R	0h	
17-8	LPFRESA	R	4h	Loop Filter Res A
7-5	RESERVED	R	0h	
4-0	LPFCAPA	R	Fh	Loop Filter Cap A

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15 PLLSTARTUP0_32_48MHZ Register (Offset = 38h) [Reset = 00000000h]

PLLSTARTUP0_32_48MHZ is shown in Figure 3-110 and described in Table 3-138.

Return to the Summary Table.

Figure 3-110. PLLSTARTUP0_32_48MHZ Register

31	30	29	28	27	26	25	24
CAPBOVERRIDE	RESERVED		CAPBVAL				
R-0h	R-0h		R-0h				
23	22	21	20	19	18	17	16
RESERVED		CPCURRENT					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESERVED		STARTTIMELP					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RESERVED		STARTTIME					
R-0h		R-0h					

Table 3-238. PLLSTARTUP0_32_48MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAPBOVERRIDE	R	1h	Override Enable For Cap B 0h = 0 1h = 1
30-29	RESERVED	R	0h	
28-24	CAPBVAL	R	1h	Override Value for Cap B
23-22	RESERVED	R	0h	
21-16	CPCURRENT	R	Ah	Charge Pump Current
15-14	RESERVED	R	0h	
13-8	STARTTIMELP	R	16h	Startup time from Low Power Exit to Locked Clock in resolution of 1usec
7-6	RESERVED	R	0h	
5-0	STARTTIME	R	16h	Startup time from Enable to Locked Clock in resolution of 1usec

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16 PLLSTARTUP1_32_48MHZ Register (Offset = 3Ch) [Reset = 00000000h]

PLLSTARTUP1_32_48MHZ is shown in Figure 3-111 and described in Table 3-139.

Return to the Summary Table.

Figure 3-111. PLLSTARTUP1_32_48MHZ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPFRESC								RESERVED						LPFRESA	
R-0h								R-0h						R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPFRESA								RESERVED			LPFCAPA				
R-0h								R-0h			R-0h				

Table 3-240. PLLSTARTUP1_32_48MHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LPFRESC	R	FFh	Loop Filter Res C
23-18	RESERVED	R	0h	
17-8	LPFRESA	R	4h	Loop Filter Res A
7-5	RESERVED	R	0h	
4-0	LPFCAPA	R	Fh	Loop Filter Cap A

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17 TEMP_SENSE0 Register (Offset = 40h) [Reset = 00000000h]

TEMP_SENSE0 is shown in Figure 3-112 and described in Table 3-140.

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Temperature sensor room temperature calibration code. This is ADC conversion results of temperature sensor output voltage. Included in BOOTCRC calculation.

Figure 3-112. TEMP_SENSE0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 3-242. TEMP_SENSE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	

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18 ROM_VERSION Register (Offset = 4Ch) [Reset = 01010000h]

ROM_VERSION is shown in Figure 3-113 and described in Table 3-141.

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Figure 3-113. ROM_VERSION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM_PG_VER								ROM_MAJOR_VER							
R-1h								R-1h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM_MINOR_VER								ROM_PATCH_VER							
R-0h								R-0h							

Table 3-244. ROM_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ROM_PG_VER	R	01h	
23-16	ROM_MAJOR_VER	R	01h	
15-8	ROM_MINOR_VER	R	00h	
7-0	ROM_PATCH_VER	R	00h	

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19 ROM_INM_VERSION Register (Offset = 50h) [Reset = 01010000h]

ROM_INM_VERSION is shown in Figure 3-114 and described in Table 3-142.

Return to the Summary Table.

Figure 3-114. ROM_INM_VERSION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM_INM_PG_VER								ROM_INM_MAJOR_VER							
R-1h								R-1h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROM_INM_MINOR_VER								ROM_INM_PATCH_VER							
R-0h								R-0h							

Table 3-246. ROM_INM_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ROM_INM_PG_VER	R	01h	
23-16	ROM_INM_MAJOR_VER	R	01h	
15-8	ROM_INM_MINOR_VER	R	00h	
7-0	ROM_INM_PATCH_VER	R	00h	

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20 SYSPLLPARAM2 Register (Offset = 54h) [Reset = 00000000h]

SYSPLLPARAM2 is shown in Figure 3-115 and described in Table 3-143.

Return to the Summary Table.

Figure 3-115. SYSPLLPARAM2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RNGIXVCOIBIASCFG	RESERVED	LPFCAPC	
R-0h				R-0h	R-0h	R-0h	

Table 3-248. SYSPLLPARAM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	RNGIXVCOIBIASCFG	R	1h	
2	RESERVED	R	0h	
1-0	LPFCAPC	R	00h	

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21 SYSPLLLDOCTL Register (Offset = 58h) [Reset = 00000000h]

SYSPLLLDOCTL is shown in Figure 3-116 and described in Table 3-144.

Return to the Summary Table.

Figure 3-116. SYSPLLLDOCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LDOCTLLOWV															
R-0h																R-0h															

Table 3-250. SYSPLLLDOCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	LDOCTLLOWV	R	00h	

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22 SYSPLLLDOPROG Register (Offset = 5Ch) [Reset = 00000000h]

SYSPLLLDOPROG is shown in Figure 3-117 and described in Table 3-145.

Return to the Summary Table.

Figure 3-117. SYSPLLLDOPROG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					LDOVOUTPROGLOWV		
R-0h					R-0h		

Table 3-252. SYSPLLLDOPROG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2-0	LDOVOUTPROGLOWV	R	4h	

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23 EXTREF_MP3 Register (Offset = 60h) [Reset = 00000000h]

EXTREF_MP3 is shown in Figure 3-118 and described in Table 3-146.

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External Reference MP3 Temp Sense

Figure 3-118. EXTREF_MP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSOFFSET_EXTREF_MP3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSGAIN_EXTREF_MP3															
R-0h															

Table 3-254. EXTREF_MP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TSOFFSET_EXTREF_MP3	R	0h	Temperature sensor offset is recorded here
15-0	TSGAIN_EXTREF_MP3	R	0h	Temperature sensor gain is recorded here

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24 INTREF_MP3 Register (Offset = 64h) [Reset = 00000000h]

INTREF_MP3 is shown in Figure 3-119 and described in Table 3-147.

Return to the Summary Table.

Internal Refernce Temp Sene

Figure 3-119. INTREF_MP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSOFFSET_INTREF_MP3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSGAIN_INTREF_MP3															
R-0h															

Table 3-256. INTREF_MP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TSOFFSET_INTREF_MP3	R	0h	Temperature sensor offset is recorded here
15-0	TSGAIN_INTREF_MP3	R	0h	Temperature sensor gain is recorded here

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25 TSCODE_MP1 Register (Offset = 68h) [Reset = 00000000h]

TSCODE_MP1 is shown in Figure 3-120 and described in Table 3-148.

Return to the Summary Table.

Tempsense Code MP1

Figure 3-120. TSCODE_MP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSCODE_INTREF_MP1															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCODE_EXTREF_MP1															
R-0h															

Table 3-258. TSCODE_MP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TSCODE_INTREF_MP1	R	0h	Temperature sensor value at 30C stored at this location
15-0	TSCODE_EXTREF_MP1	R	0h	Temperature sensor value at 30C stored at this location

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26 TSCODE_MP3 Register (Offset = 6Ch) [Reset = 00000000h]

TSCODE_MP3 is shown in Figure 3-121 and described in Table 3-149.

Return to the Summary Table.

Tempsense code MP3

Figure 3-121. TSCODE_MP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSCODE_INTREF_MP3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCODE_EXTREF_MP3															
R-0h															

Table 3-260. TSCODE_MP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TSCODE_INTREF_MP3	R	0h	Temperature sensor value at 125C stored at this location
15-0	TSCODE_EXTREF_MP3	R	0h	Temperature sensor value at 125C stored at this location

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27 TSTEMP Register (Offset = 70h) [Reset = 00000000h]

TSTEMP is shown in Figure 3-122 and described in Table 3-150.

Return to the Summary Table.

Temperature sense TEMP

Figure 3-122. TSTEMP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTEMP_MP3																TSTEMP_MP1															
R-0h																R-0h															

Table 3-262. TSTEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TSTEMP_MP3	R	0h	Test temperature (125C) is recorded here
15-0	TSTEMP_MP1	R	0h	Test temperature (30C) is recorded here

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28 SRAMFLASH Register (Offset = 74h) [Reset = 00000000h]

SRAMFLASH is shown in Figure 3-123 and described in Table 3-151.

Return to the Summary Table.

Number of banks , sram size and flash size

Figure 3-123. SRAMFLASH Register

31	30	29	28	27	26	25	24
DATAFLASH_SZ						SRAM_SZ	
R-0h						R-0h	
23	22	21	20	19	18	17	16
SRAM_SZ							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		MAINNUMBANKS		MAINFLASH_SZ			
R-0h		R-0h		R-0h			
7	6	5	4	3	2	1	0
MAINFLASH_SZ							
R-0h							

Table 3-264. SRAMFLASH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	DATAFLASH_SZ	R	00h	The encoding of the field is that the value of the field is an integer to be interpreted as number of KBs. For eg: if the value of the field id 4, then it is 4KB, if the value is 32, then 32KB, and so on.
25-16	SRAM_SZ	R	80h	The encoding of the field is that the value of the field is an integer to be interpreted as number of KBs.
15-14	RESERVED	R	0h	
13-12	MAINNUMBANKS	R	2h	Defines the number of main flash banks
11-0	MAINFLASH_SZ	R	200h	For eg: if the value of the field id 4, then it is 4KB, if the value is 32, then 32KB, and so on.

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Chapter 4

Central Processing Unit (CPU)

The CPU subsystem (CPUSS) includes the Arm Cortex-M33 processor and the interrupt logic.

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4.4 CPU Peripherals 229
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4.1 Overview

The AM13E232x CPU subsystem (CPUSS) contains the central processing unit (CPU) along with associated supporting logic and read-only memory (ROM). The functional blocks that comprise the CPUSS include:

- The Arm Cortex-M33 32-bit CPU and internal peripherals
- The CPU bus splitter and router
- The interrupt management logic and DEEPSLEEP entry and exit logic
- The CPU debug interface to the Debug Subsystem (DEBUGSS)
- The Read-Only Memory (ROM) used for the BCR and BSL

The top level architecture of the CPUSS is shown in Figure 4-1.

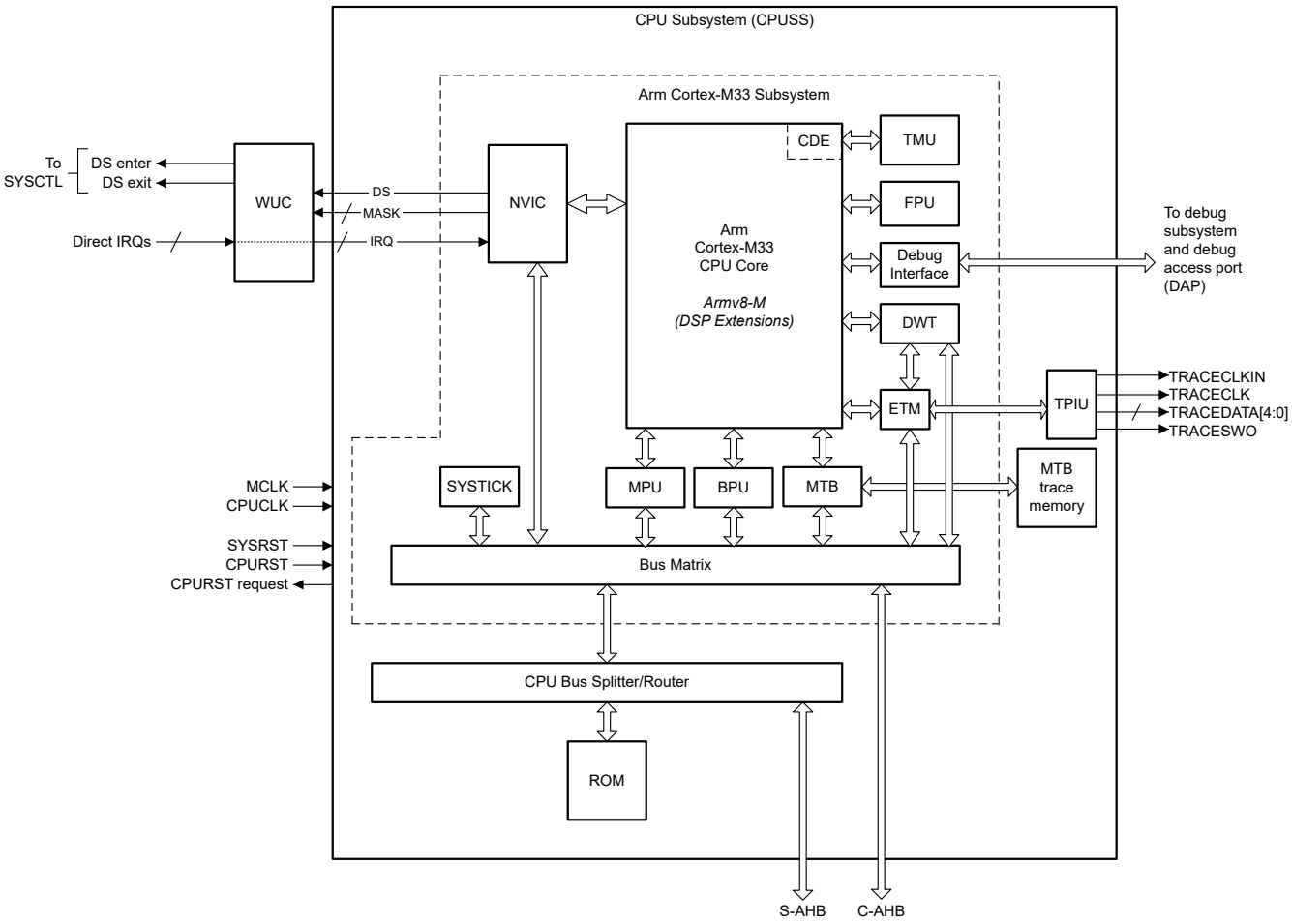


Figure 4-1. AM13E232x CPUSS Top Level Diagram

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4.2 CPU

The CPU subsystem (CPUSS) includes the Arm Cortex-M33 processor and the interrupt logic.

4.2.1 Arm Cortex-M33 CPU

The CPUSS contains an energy-efficient Arm Cortex-M33 CPU implementing the Armv8-M instruction set architecture with support for CPU clock speeds up to 250MHz. The Cortex-M33 is a Harvard architecture style 32-bit processor with a 3-stage ultra-low power pipeline.

The Cortex-M33 implementation on AM13E232x devices has the following features:

- Up to 250MHz execution frequency
- Little-endian (least significant byte at lowest byte address location)
- Support for 32-bit word instruction fetches
- Single cycle 32×32 multiply instruction
- Integrated Memory Protection Unit (MPU)
- Integrated Floating Point Unit (FPU)
- Custom Datapath Extension Trigonometric Math Unit (CDE TMU)
- DSP extensions
- User and privileged execution modes
- Integrated 24-bit system tick timer (SYSTICK)
- Eight hardware breakpoints and four hardware watchpoints for debug
- Micro Trace Buffer (MTB)
- Embedded Trace Macrocell (ETM) with timestamp counter
- Reset-all-registers support
- Vector table offset support

The Cortex-M33 architecture enables excellent code density, deterministic interrupt handling, and upwards compatibility with other processor architectures in the Arm Cortex-M family.

A general overview of the Arm Cortex-M33 is given in this section to provide a basic understanding of the features of the processor. For detailed information on developing with the Arm Cortex-M33 processor, refer to the *Arm Cortex-M33 Devices Generic User's Guide*.

4.2.2 CPU Register File

The Arm Cortex-M33 processor instructions operate on registers in the CPU register file. The processor contains a register file consisting of 16 32-bit wide standard registers and 5 special registers as shown in Figure 4-2.

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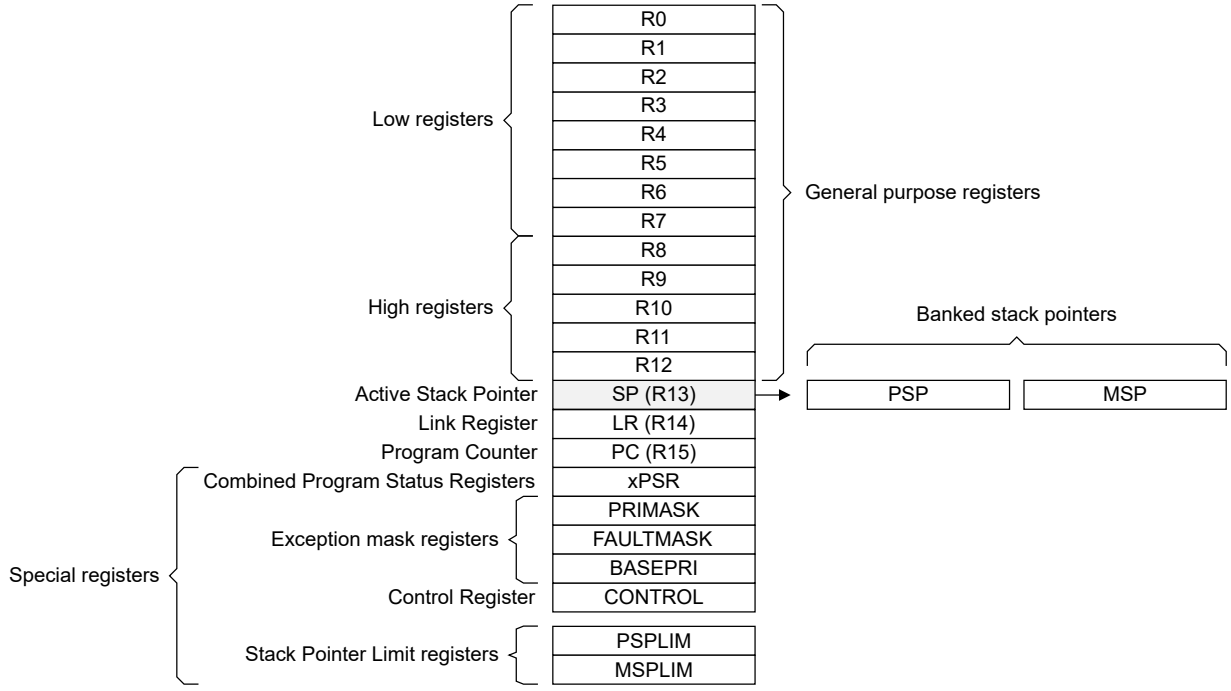


Figure 4-2. CPU Core Registers

General Purpose Registers (R0-R12)

The processor provides 13 general purpose registers, R0-R12, for operating on data. Registers R0 to R7 (low registers) are accessible by all instructions which specify a general purpose register. Registers R8 to R12 (high registers) are not accessible by 16-bit instructions but are accessible by any 32-bit instructions which specify a general purpose register.

Stack Pointer Register (R13)

The stack pointer is contained in R13, and can contain the Main Stack Pointer (MSP) or the Process Stack Pointer (PSP). When the processor is running in handler mode, the MSP is always used. When the processor is running in thread mode, the MSP or PSP can be used depending on the configuration of the SPSEL bit in the CONTROL register.

After a CPURST, the processor automatically and unconditionally fetches the default stack pointer from the first address of main flash (0x0000.0000) as the main stack pointer (MSP).

The MSPLIM and PSPLIM are registers that define the lower limit for the corresponding stack. The processor raises an exception on most instructions that attempt to update the stack pointer below the defined limit.

Link Register (R14)

The Link Register (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions. On reset, the processor sets the LR value to 0xFFFFFFFF. It is accessible in privileged and unprivileged mode.

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Program Counter Register (R15)

The program counter register (R15) contains the address of the next instruction to be executed. The PC is accessible in privileged and unprivileged mode.

After a CPURST, the processor automatically and unconditionally fetches the default PC from the second word of main flash (0x0000.0004).

Special Registers

Special registers include the program status register (xPSR), the interrupt mask register (PRIMASK), fault mask register (FAULTMASK), base priority mask register (BASEPRI), and the control register (CONTROL). Special registers are typically accessed by using the CPS, MRS, and MSR system instructions.

- **Program Status Register (xPSR):** The xPSR is a combination of the application status (APSR), interrupt status (IPSR), and execution status (EPSR) registers. Application software can access the PSR with MRS and MSR instructions, accessing either the complete PSR or a combination of one or more registers, with some restrictions. The PSR registers can be accessed with MRS and MSR instructions using the mnemonics given in *Program Status Register (PSR) Access Mnemonics*.
  - The **Application Program Status Register (APSR)** contains the N, Z, C, V, Q, and GE flags which are used by the processor to evaluate conditional branch instructions. These bits are located in BIT31, BIT30, BIT29, BIT28, BIT27, and BIT16 to BIT19 of the PSR, respectively.
  - The **Interrupt Program Status Register (IPSR)** reports the exception number of the current interrupt service routine when in handler mode. In thread mode, this register reads as all zero. Attempts to write to the IPSR are ignored. The exception number field is presented in from BIT0 to BIT5 of the PSR.
  - The **Execution Program Status Register (EPSR)** contains the Thumb state bit and the execution state bits for the If-Then (IT) instruction, and Interruptible-Continuable Instruction (ICI) field for an interrupted load multiple or store multiple instruction. Attempts to read the EPSR directly through application software using the `MRS` instruction always return zero. Attempts to write the EPSR using the `MSR` instruction in application software are ignored.
- **Interrupt Mask Register (PRIMASK):** BIT0 of the PRIMASK register (PM) can be used to mask all interrupts to the processor which have configurable priority (see Section 4.3). This can be thought of as a global peripheral interrupt mask control. The processor ignores unprivileged writes to PRIMASK. Clearing PM to 0 enables interrupts. Setting PM to 1 disables interrupts. The CPS instruction can be used to change the PM bit value in the PRIMASK register.
- **Fault Mask Register (FAULTMASK):** The Fault mask register prevents activation of all exceptions with configurable priority and some exceptions with fixed priority. The priority it is boosted to changes based on the value of BIT14 (PRIS) and BIT13 (BFHFNMINS) bit of the AIRCR register in the SCB.
- **Base Priority Mask Register (BASEPRI)** The base priority mask register can be used to change the priority level that is required for exception preemption. BIT0 to BIT7 of BASEPRI are used for configure what the boosted priority will be. When the current execution priority is boosted to a particular value, all exceptions with a lower priority are masked. Writing 0 to BASEPRI disables base priority boosting.
- **Control Register (CONTROL):** The CONTROL register can be used to define whether the code executing in thread mode is privileged or unprivileged by clearing or setting the nPRIV bit (BIT0), respectively. It can also be used to select the active stack pointer used in R13 as either the Main Stack Pointer (MSP) or Process Stack Pointer (PSP) by clearing or setting the SPSEL bit (BIT1), respectively. The FPCA bit (BIT2) of the CONTROL register also indicates whether the FPU state is active. A CPURST clears the CONTROL register to zero. The processor ignores unprivileged writes to the CONTROL register. The SPSEL stack pointer selection bit is updated by the processor automatically when entering and returning from exceptions.

Note

For more information on the core registers, please refer to the Arm Cortex-M33 Devices Generic User Guide.

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Note

Software must implement an ISB barrier instruction after writing to CONTROL to ensure that any changes take effect before the next application instruction is executed by the processor.

Table 4-1. Program Status Register (xPSR) Access Mnemonics

Mnemonic	Subregisters Included
xPSR	APSR, IPSR, EPSR
APSR	APSR
IPSR	IPSR
EPSR	EPSR
IAPSR	IPSR and APSR
EAPSR	EPSR and APSR
IEPSR	IPSR and EPSR

4.2.3 Stack Behavior

The Arm Cortex-M33 processor implements a full descending stack protocol. The stack pointer register (SP) always indicates the location of the last stacked data. When new data is added to the call stack, the SP value is decremented and the data is written to the location indicated by the SP after being decremented.

The Arm Cortex-M33 supports managing two independent stacks with two pointers: the main stack (MSP) and the process stack (PSP).

4.2.4 Execution Modes and Privilege Levels

The processor supports two primary modes of execution:

- **Thread mode** (for executing application software)
- **Handler mode** (for handling processor exceptions and peripheral interrupts)

By default, the processor is in thread mode out of reset. If an exception is issued to the processor, the processor handles the exception in handler mode and return to thread mode after handler execution is complete. Code running in thread mode can be configured as being privileged or unprivileged, based on the configuration of the CONTROL register. Code running in handler mode always executes as privileged.

Note

Handler mode always uses the MSP, so the processor ignores explicit writes to the active stack pointer bit of the CONTROL register when in Handler mode. The exception entry and return mechanisms automatically update the CONTROL register based on the EXC_RETURN value.

By default, thread mode uses the MSP. To switch the stack pointer that is used in thread mode to the PSP, either:

1. Use the `MSR` instruction to set the CONTROL.SPSEL bit to 1.
2. Perform an exception return to thread mode with the appropriate EXC_RETURN value.

In general, code which executes as privileged has complete control of the processor configuration, including control of the MPU, Systick, NVIC, and SCB. Only privileged code can change the privilege level for code running in thread mode.

Code that is executing in thread mode in an unprivileged state cannot access the previously mentioned resources (MPU, Systick, NVIC, and SCB).

4.2.5 Address Space and Supported Data Sizes

AM13E232x devices implement a flat memory map with a 32-bit byte-addressable address space. Byte addresses are unsigned numbers ranging from zero to 2^{32}-1.

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Address Space

The processor sees the address space as containing 2^{30} 32-bit words, with each word being word-aligned (4-byte aligned). Pointers are always 32-bits, and stack operations (for example, push, pop) increment the stack pointer by 4 addresses (4 bytes). Address calculations by the processor wrap around if they overflow or underflow the 32-bit memory space.

Instruction fetches by the processor are always 16-bit half-word aligned.

Data reads by the processor must be naturally aligned (for example, words must be word aligned, half words must be half-word aligned, etc.).

Supported Data Sizes

The processor supports the following data types:

- 32-bit words
- 16-bit halfwords
- 8-bit bytes
- 32-bit single-precision floating point numbers
- 64-bit double-precision floating point numbers

Signed and unsigned data is supported, and signed data is stored in CPU registers in 32-bit two's complement format. The Armv8-M instruction set does not provide native instructions supporting operations on 64-bit double-word data.

Load operations from memory to a CPU register can be signed or unsigned when the data size is less than 32 bits. When loading unsigned half-word or byte data to a CPU register, the value is zero-extended to 32 bits automatically. When loading signed half-word or byte data to a CPU register, the value is sign-extended to 32 bits automatically.

Stores from CPU registers to memory are sign agnostic.

All instruction and data accesses use little endian byte order.

4.3 Interrupts and Exceptions

Peripheral interrupt exceptions and system exceptions temporarily pause the processor's normal execution flow so that the processor can be used to handle an event.

The following can cause interruption of normal execution flow:

- **Reset**: The exception model treats reset as a special form of exception. When either power-on or warm reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When reset is deasserted, execution restarts from the address provided by the reset entry in the vector table. Execution restarts as privileged execution in Thread mode.
- **Non-Maskable Interrupt (NMI)**: A Non-Maskable Interrupt (NMI) can be signaled by a peripheral or triggered by software. This is the highest priority exception other than reset. It is permanently enabled and has a fixed priority of -2. NMIs cannot be masked or preempted by any exception other than Reset.
- **HardFault**: A HardFault is an exception that occurs because of an error during exception processing, or because an exception cannot be managed by any other exception mechanism. HardFaults have a fixed priority of -1, meaning they have higher priority than any exception with configurable priority.
- **MemManage**: A MemManage fault is an exception that occurs because of a memory protection violation, compared to the MPU or the fixed memory protection constraints, for both instruction and data memory transactions. This fault is always used to abort instruction accesses to "Execute Never" (XN) memory regions.
- **BusFault**: A BusFault is an exception that occurs because of a memory-related fault for an instruction or data memory transaction. This might be from an error that is detected on a bus in the memory system.
- **UsageFault**: A UsageFault is an exception that occurs because of a fault related to instruction execution. This includes: an undefined instruction, an illegal unaligned access, invalid state on instruction execution,

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or an error on exception return. Software can configure the core to report a UsageFault when: there is an unaligned address on word and halfword memory access or division by zero.
- **SVCall**: A Supervisor Call (SVC) is an exception that is triggered by the SVC instruction.
- **DebugMonitor**: A DebugMonitor exception. If halting debug is disabled and the debug monitor is enabled, a debug event causes a DebugMonitor exception when the group priority of the DebugMonitor exception is greater than the current execution priority.
- **PendSV**: PendSV is an asynchronous request for system-level service.
- **SysTick**: A SysTick exception is an exception the system timer generates when it reaches zero. Software can also be configured to generate a SysTick exception.
- **Interrupt (IRQ)**: An interrupt, or IRQ, is an exception signaled by a peripheral, or generated by a software request. All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor.

Properties of the different exception types are detailed in Table 4-4.

Exception States

Each exception source to the processor will be in one of the below states at any given point in time:
- **Inactive** (not active, not pending)
- **Pending** (waiting to be serviced by the processor)
- **Active** (actively being serviced by the processor but has not completed)
- **Active and pending** (actively being serviced by the processor and there is a pending exception from the same source)

Exception Prioritization, Entry, and Exit

Exceptions are prioritized by the processor together with the Nested Vectored Interrupt Controller (NVIC). Each exception has either a fixed priority (Reset, NMI, HardFault) or a configurable priority (MemManage, BusFault, UsageFault, DebugMonitor, SVCall, PendSV, SysTick, peripheral IRQs). Exceptions with configurable priority can be disabled by application software running in privileged mode. Exceptions with fixed priority cannot be disabled.

The processor exception model supports preemption, tail-chaining, and late-arrival features to boost exception handling performance:

- In the **preemption** case, if an exception of higher priority is pending when an exception of lower priority is executing, the higher priority exception will preempt the ongoing handler servicing the lower priority exception.
- In the **tail-chaining** case, if a valid-for-entry exception is pending at the time of completion of an exception handler, then the application context is not restored from the stack and control is given immediately to the pending exception.
- In the **late-arriving** case, if a higher priority exception occurs during entry to a lower priority exception, the higher priority exception will be serviced first after the processor state is saved to the stack. Once the higher priority exception handling is complete, the lower priority exception (which is still pending) is serviced based on the tail-chaining procedure.

An exception entry is issued if and when all of the following are true:

- An exception is in a **pending** state
- The priority of the pending exception is higher than the limit set by the exception mask register (PRIMASK)
- The processor is currently in either thread mode (not servicing an exception) or the newly pending exception is higher priority than the exception which is currently being serviced (resulting in a preemption)

Processor exceptions are vectored. When an exception occurs, the current processor state is pushed onto the stack which was active at the time of the event, and execution is vectored to the entry point address in the vector table corresponding to the exception which is to be processed.

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If the exception is tail-chained to a previous handler which has completed, then there is no need to push any state to the stack and the interrupt service routine can be vectored to immediately. Likewise, if the exception is higher priority than a previous exception which started entry but did not complete entry, then there is no need to save the context again (late arrival).

Upon completion of an exception handler, if there is no exception pending which needs to be handled then the processor will pop the state from the stack and restore the processor to the previous state which it was in when the exception occurred.

4.3.1 Peripheral Interrupts (IRQs)

Peripheral interrupt functionality is managed by several components on the device:

- The Nested Vectored Interrupt Controller (NVIC)
- The Wake-Up Controller (WUC)

AM13E232x devices include an Arm Nested Vectored Interrupt Controller (NVIC) with the Cortex-M33 CPU for managing peripheral interrupts. The NVIC operation is tightly integrated with the processor and supports 48 native peripheral interrupt sources.

The Wake-Up Controller (WUC) determines if the PD1 power domain (containing the processor) needs to be powered up to service a peripheral interrupt if the PD1 domain is powered down in STOP or STANDBY mode.

4.3.1.1 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an industry-standard Arm component which interfaces peripheral interrupts (which are external to the processor) into the CPU. The NVIC supports connection of up to 48 native peripheral interrupt sources. For information on which peripheral is being mapped, please refer to Table 4-2.

Table 4-2. NVIC IRQ Mapping

NVIC IRQ mapping	Interrupt Source
0	SYSCTL.CPU_INT
1	DEBUGSS.CPU_INT
2	Reserved
3	WWDT.CPU_INT
4	GPIO0.CPU_INT
5	GPIO1.CPU_INT
6	GPIO2.CPU_INT
7	GPIO3.CPU_INT
8	ADC0_INT1
9	ADC0_INT2
10	ADC0_INT3
11	ADC0_INT4
12	ADC0_EVT
13	ADC1_INT1
14	ADC1_INT2
15	ADC1_INT3
16	ADC1_INT4
17	ADC1_EVT
18	ADC2_INT1

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Table 4-2. NVIC IRQ Mapping (continued)

NVIC IRQ mapping	Interrupt Source
19	ADC2_INT2
20	ADC2_INT3
21	ADC2_INT4
22	ADC2_EVT
23	MCAN0.CPU_INT
24	MCPWM0_INT
25	MCPWM1_INT
26	MCPWM2_INT
27	Reserved
28	Reserved
29	ECAP0
30	ECAP1
31	EQEP0
32	EQEP1
33	Reserved
34	UNICOMM0.CPU_INT
35	UNICOMM1.CPU_INT
36	UNICOMM2.CPU_INT
37	UNICOMM3.CPU_INT
38	UNICOMM4.CPU_INT
39	UNICOMM5.CPU_INT
40	DMA.CPU_INT
41	NPU
42	Reserved
43	AES.INT_EVENT0
44	TIMG4.CPU_INT
45	TIMG12.CPU_INT
46	TMU_LUF_INT
47	TMU_LVF_INT
48	MCAN1.CPU_INT
49	ECAP2
50	EPWM0_INT
51	EPWM0_TZ_INT
52	EPWM1_INT
53	EPWM1_TZ_INT
54	EPWM2_INT
55	EPWM2_TZ_INT

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Table 4-2. NVIC IRQ Mapping (continued)

NVIC IRQ mapping	Interrupt Source
56	EPWM3_INT
57	EPWM3_TZ_INT
58	EPWM4_INT
59	EPWM4_TZ_INT
60	EPWM5_INT
61	EPWM5_TZ_INT
62	SDFM
63	SDFMDR1
64	SDFMDR2
65	SDFMDR3
66	SDFMDR4
67	FSITX_INT1
68	FSITX_INT2
69	FSIRX_INT1
70	FSIRX_INT2
71	ECAT_INTn
72	ECAT_SYNC0
73	ECAT_SYNC1
74	ECAT_RST
75	HRCAP2

The NVIC is configured through memory-mapped registers in the system private peripheral bus (PPB) region. See *Arm Cortex-M33 NVIC Registers* for the list of NVIC registers. The software development kit (SDK) provided with the devices supports the standard Arm Cortex Microcontroller Software Interface Standard (CMSIS) register access definitions for the NVIC. Application software must use 32-bit aligned, word-size transactions when accessing any NVIC register.

In addition to interfacing peripheral interrupts to the processor, the NVIC also supports programmable priority for each interrupt.

Enabling and Disabling Interrupts

Peripheral interrupt enables can be read, set, and cleared through the interrupt set-enable (ISER) and interrupt clear-enable (ICER) registers in the NVIC. Each ICER and ISER register supports 32 different interrupts. The interrupts are mapped to the ISER and ICER registers with interrupt zero in the BIT0 position (LSB) and interrupt 31 in the BIT31 position (MSB) of each register. For example, SETENA[m] in NVIC_ISERn, allows interrupt 32n + m to be accessed.

To enable an interrupt, set the corresponding enable bit in the ISER register. Writing a '0' to ISER has no effect. It is possible to read the ISER or ICER registers to determine which interrupts are enabled. Upon a read, a '1' indicates that an interrupt is enabled; a '0' indicates disabled. To disable an interrupt, set the corresponding clear enable bit in the ICER register. Writing a '0' to ICER has no effect.

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Note

In addition to enabling a peripheral interrupt at the NVIC, it is generally necessary to also configure the interrupt configuration of the corresponding peripheral as well. Most peripherals have multiple interrupt sources, which are merged together in the peripheral to source a single NVIC interrupt. Masking of individual peripheral interrupts is done within the peripheral's interrupt management registers.

In the event that an interrupt is disabled in the NVIC, if the interrupt is asserted by the corresponding peripheral then the NVIC interrupt will go to a pending state but the processor is not interrupted. If an interrupt is disabled when in an active state (when a handler is running) it will remain active until the exception handler returns or a reset occurs, but no further activations will happen.

Note

If a peripheral asserts an interrupt to the NVIC, but that peripheral's interrupt in the NVIC is disabled, the device may remain in a higher power mode than expected as the wake-up controller (WUC) is holding an event for the processor. To prevent this situation, ensure peripheral interrupts are masked at the peripheral directly, versus only masking interrupts at the NVIC.

Setting and Clearing Pending Interrupt Status

Pending interrupt status can be read, set, and cleared through the interrupt set-pending (ISPR) and interrupt clear-pending (ICPR) registers in the NVIC. Each ISPR and ICPR register supports 32 interrupts, with interrupt zero in the BIT0 position (LSB) and interrupt 31 in the BIT31 position (MSB) of each register. For example, SETPEND[m] in NVIC_ISPRn, allows interrupt 32n + m to be accessed.

To read if an interrupt is pending, read either the ISPR or the ICPR. Upon a read, a '1' indicates that an interrupt is pending; a '0' indicates not pending. To set an interrupt to a pending state through software, set the corresponding bit in the ISPR register. Writing a '0' to ISPR has no effect. To clear an interrupt pending state, set the corresponding bit in the ICPR register. Writing a '0' to ICPR has no effect. Note that if a peripheral interrupt condition is still present, the pending state will be set again by hardware even if it is cleared.

Active State of Interrupts

The IABR registers in the NVIC indicate the active state of each interrupt. Each IABR register supports 32 interrupts, with interrupt 0 in the BIT0 position (LSB) and interrupt 31 in the BIT31 position (MSB) of each register. For example, ACTIVE[m] in NVIC_IABRn, indicates the active state for interrupt 32n+m.

To read if an interrupt is active, read the IABR register. Upon a read, a '1' indicates that an interrupt is active; a '0' indicates not active.

Software Triggered Interrupts

The STIR register in the NVIC is used to generate an interrupt from software. The INTID field of the STIR register designates the interrupt ID of the interrupt to trigger, in the range of 0-48. For example, a INTID value of 0x03 specified IRQ3. When the USERSETMPEND bit in the CCR register is set to '1', unpriveileged software can access the STIR register. Only privileged software can enable unprivileged access.

Setting Interrupt Priority

Interrupts on the NVIC have programmable priority. There are 16 priority levels possible. Priority is set by programming the IPR registers in the NVIC. Each priority field is 8 bits in length, and the priority for 4 interrupts is configured per 32-bit IPR register. AM13E232x only implements the most significant 4 bits of each 8-bit priority field (giving the 16 priority levels). Lower priority values have higher priority. System exceptions (Reset, NMI, and HardFault) have fixed priorities of -4, -2, and -1, respectively. As such, these exceptions always have higher priority than peripheral interrupts. Peripheral interrupt priorities are programmable as 0, 16, 32, 48, 64, …, 240 with 0 being highest priority and 240 being lowest priority.

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If the processor is currently handling an exception, it can only be preempted by a higher priority exception. In the event that there are multiple exceptions in a pending state which all have the same priority level assigned, the exception with the lowest exception number is taken first.

Note

Application software must not change the priority of an interrupt while the corresponding interrupt is either active (being handled) or enabled. Doing so can result in unpredictable behavior.

Table 4-3. Arm Cortex-M33 NVIC Registers

Address	Register	CMSIS	Description
0xE000.E100 - 0xE000.E13C	NVIC_ISER0 - NVIC_ISER15	NVIC->ISER[0] - NVIC->ISER[15]	Interrupt set-enable register
0xE000.E180 - 0xE000.E1BC	NVIC_ICER0 - NVIC_ICER15	NVIC->ICER[0] - NVIC->ICER[15]	Interrupt clear-enable register
0xE000.E200 - 0xE000.E23C	NVIC_ISPR0 - NVIC_ISPR15	NVIC->ISPR[0] - NVIC->ISPR[15]	Interrupt set-pending register
0xE000.E280 - 0xE000.E2BC	NVIC_ICPR0 - NVIC_ICPR15	NVIC->ICPR[0] - NVIC->ICPR[15]	Interrupt clear-pending register
0xE000.E300 - 0xE000.E33C	NVIC_IABR0 - NVIC_IABR15	NVIC->IABR[0] - NVIC->IABR[15]	Interrupt active bit register
0xE000.E400 - 0xE000.E5DC	NVIC_IPR0 - NVIC_IPR119	NVIC->IPR[0] - NVIC->IPR[119]	Interrupt priority register (0 - 3) - Interrupt priority register (115 - 119)
0xE000EF00	STIR	NVIC->STIR	Software trigger interrupt register

4.3.1.2 Wake Up Controller (WUC)

The Wake Up Controller (WUC) is responsible for monitoring for assertion of interrupts when the processor is powered down in the STOP or STANDBY operating mode. In these modes, the entire PD1 power domain is power gated, and as such, the processor and NVIC are not available to check for interrupts. The WUC retains a copy of which peripheral interrupt sources to the NVIC were enabled when the processor entered STOP or STANDBY mode. In the event that an enabled interrupt is issued, the WUC will handshake with the System Controller to bring the device out of STOP or STANDBY mode so that the CPU can service the interrupt. The WUC will capture the interrupt state and present it to the NVIC and processor when the processor is brought up, such that the processor will see the interrupt even if the raw interrupt status of the peripheral is removed before the processor finishes powering up to service the interrupt.

The WUC requires no configuration by application software upon entry to or exit from low-power modes, and operation is transparent to application software.

4.3.2 Interrupt and Exception Table

The Arm Cortex-M33 interrupt vector table is 500 words long (2000 bytes). The complete platform interrupt and exception table with vector table addresses is given in Table 4-4.

See Table 4-2 for a complete list of which interrupts a particular device supports along with a more detail interrupt vector table describing which NVIC number is used for what peripheral.

Table 4-4. AM13E232x Platform Processor Interrupt and Exception Table

Exception Number	NVIC Number(1)	Priority Group	Secure Vector	Vector Table Address	Vector Description(2)
-	-	-	-	0x0000.0000	Stack pointer
1	-	-4	Reset	0x0000.0004	Reset vector
2	-14	-2	NMI	0x0000.0008	NMI handler
3	-13	-1	HardFault	0x0000.000C	Hard fault handler
4	-12	Configurable	MemManage	0x0000.0010	Memory Protection Violation
5	-11	Configurable	BusFault	0x0000.0014	Memory-related fault

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Table 4-4. AM13E232x Platform Processor Interrupt and Exception Table (continued)

Exception Number	NVIC Number(1)	Priority Group	Secure Vector	Vector Table Address	Vector Description(2)
6	-10	Configurable	UsageFault	0x0000.0018	UsageFault
7	-	-	Reserved	0x0000.001C	-
8	-	-	Reserved	0x0000.0020	-
9	-	-	Reserved	0x0000.0024	-
10	-	-	Reserved	0x0000.0028	-
11	-5	Configurable	SVCall	0x0000.002C	Supervisor call handler
12	-4	Configurable	DebugMonitor	0x0000.0030	DebugMonitor exception
13	-	-	Reserved	0x0000.0034	-
14	-2	Configurable	PendSV	0x0000.0038	Pended supervisor handler
15	-1	Configurable	SysTick	0x0000.003C	SysTick handler
16	0	Configurable	Device Interrupt 0	0x0000.0040	Handler for Device Interrupt 0
17	1	Configurable	Device Interrupt 1	0x0000.0044	Handler for Device Interrupt 1
18	2	Configurable	Device Interrupt 2	0x0000.0048	Handler for Device Interrupt 2
...	...	...	...	...	...
63	47	Configurable	Device Interrupt 47	0x0000.00FC	Handler for Device Interrupt 47

(1) The NVIC number also indicates the relative interrupt priority if multiple NVIC interrupts have the same group priority. However, an interrupt does not preempt an active handler for another interrupt with the same group priority, even if the interrupt has a higher (numerically lower) NVIC position. For preemption to occur, the new interrupt must be configured to a higher priority group (numerically lower).

(2) For more information on the exceptions, please see Arm Cortex-M33 Generic User Guide

Non-Maskable Interrupt (NMI)

The CPU implements a nonmaskable interrupt, which handles critical interrupts which must be serviced immediately by the processor. The NMI interrupt sources are managed by SYSCTL. See the corresponding NMI information in the SYSCTL chapter of this document.

4.3.3 Processor Lockup Scenario

There are several exception conditions which can cause the processor to enter a lockup state. On AM13E232x devices, a processor lockup is considered a fatal fault which always triggers a SYSRST to clear the lockup condition and restart the system.

A lockup state is entered by the processor if an SVC (supervisor call) or fault condition occurs while the processor is handling an exception with priority of -1 or higher (numerically lower). Such a fault is considered by the processor to be unexpected under normal operating conditions.

The following examples are conditions that can trigger a lockup state in the processor:

- The processor cannot fetch the stack pointer or reset vector at reset
- The processor cannot fetch the NMI vector
- The processor cannot fetch the hard fault vector
- A memory fault occurs when the processor is already handling an exception with priority of -1 or -2 (hard fault or NMI)
- A supervisor call (SVC) occurs when the processor is already handling an exception with priority of -1 or -2 (hard fault or NMI)
- A usage fault or undefined instruction is fetched when the processor is already handling an exception with priority of -1 or -2 (hard fault or NMI)
- A BKPT instruction is executed when the processor is already handling an exception with priority of -1 or -2 (hard fault or NMI)

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- The NMI Handler function is empty

4.4 CPU Peripherals

The Arm Cortex-M33 includes tightly coupled peripherals for system timing, memory protection, floating point computation, and security

4.4.1 System Control Block (SCB)

The System Control Block (SCB) provides system implementation information and system control functionality, as well as configuration, control, and reporting of processor exceptions.

The SCB is configured through memory-mapped registers in the system private peripheral bus (PPB) region. See Table 4-5 for the list of SCB registers. The software development kit (SDK) provided with the devices supports the standard Arm Cortex Microcontroller Software Interface Standard (CMSIS) register access definitions for the SCB. Application software must use 32-bit aligned, word-size transactions when accessing any SCB register.

Table 4-5. Arm Cortex-M33 System Control Block Registers

Address	Register	CMSIS	Description
0xE000.ED00	CPUID	SCB->CPUID	Read-only register indicating the processor part number, version, and implementation information
0xE000.ED04	ICSR	SCB->ICSR	Provides a set-pending bit for the non-maskable interrupt exception, and set-pending and clear-pending bits for the PendSV and SysTick exceptions
0xE000.ED08	VTOR	SCB->VTOR	Used to specify the vector table offset from 0x0000.0000
0xE000.ED0C	AIRCR	SCB->AIRCR	Used to issue a CPU reset request (SYSRESETREQ)
0xE000.ED10	SCR	SCB->SCR	System control register, used to control low-power mode behavior
0xE000.ED14	CCR	SCB->CCR	Read-only register indicating behavior of the processor
0xE000.ED18	SHPR1	SCB->SHP[1]	Used to configure priority level of Usagefault, BusFault, and MemManage system handlers
0xE000.ED1C	SHPR2	SCB->SHP[2]	Used to configure the priority level of the SVCall system handler
0xE000.ED20	SHPR3	SCB->SHP[3]	Used to configure the priority level of the SysTick and PendSV system handlers
0xE000.ED24	SHCSR	SCB->SHCSR	Enables the system handlers. Indicates the pending status of the BusFault, MemManage fault, and SVC exceptions, and indicates the active status of the system handlers.
0xE000.ED28	CFSR	SCB->CFSR	Used to indicate cause of MemManage fault, BusFault, and Usage Fault
0xE000.ED2C	HFSR	SCB->HFSR	Provides information about events that active the HardFault handler
0xE000.ED34	MMFAR	SCB->MMFAR	Contains the address of the MemManage fault location
0xE000.ED38	BFAR	SCB->BFAR	Contains the address of the BusFault location

For detailed information on the SCB register configuration, see the SCB section of the Arm Cortex-M33 Devices Generic User Guide.

4.4.2 System Tick Timer (SysTick)

The system tick timer (SysTick) is a tightly-coupled timer clocked by MCLK, which can be used for system time keeping. The SysTick is available in RUN and SLEEP modes but is not available for use in STOP, STANDBY, or SHUTDOWN modes.

The SysTick is configured through memory-mapped registers in the system private peripheral bus (PPB) region. See *SysTick Registers* for the list of SysTick configuration registers. The software development kit (SDK) provided with the devices supports the standard Arm Cortex Microcontroller Software Interface Standard (CMSIS) register access definitions for the SysTick.

The SysTick timer can be used in several different ways, including:

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- As an RTOS timer which fires at a programmable rate (for example, 100Hz) and invokes a SysTick routine
- A high-speed alarm timer
- A simple counter used to measure time to completion and time used in an application
- A timeout counter to check that a routine has not timed out within a specified period

The SysTick timer is a simple 24-bit down counter, which counts down from its reload value to zero. Upon reaching zero, SysTick will reload the value programmed into the reload value register (SYST_RVR) on the next clock cycle, and then again begin counting down to zero. Writing a value of zero to the SYST_RVR disables the counter on the next wrap.

A SysTick event is generated when the SysTick counter reaches zero, and which point the COUNTFLAG status flag will be set. Reading the SYST_CSR register will clear the COUNTFLAG status bit. Writing to the current value register (SYST_CVR) clears the register and the COUNTFLAG status but does not generate an interrupt to the CPU. Reading SYST_CVR returns the counter value at time of access.

Application software must only use 32-bit word-aligned word accesses to the SysTick registers. To initialize the SysTick, follow the steps below:

1. Program the desired reload value (example: to generate a flag every 1000 MCLK cycles, program 999) to SYST_RVR
2. Clear the current value by writing to the SYST_CVR register
3. Program the SYST_CSR register to enable SysTick

Note

The SysTick counter does not decrement when the CPU is halted for debug.

Table 4-6. SysTick Registers

Address	Register	CMSIS	Description
0xE002.E014	SYST_CSR	SysTick->CTRL	Control and status register used to enable/disable SysTick and the SysTick exception, and to check the COUNTFLAG status
0xE002.E014	SYST_RVR	SysTick->LOAD	Reload register used to program the counter reload value to set the SysTick interval in MCLK cycles
0xE002.E018	SYST_CVR	SysTick->VAL	Returns the current value of the SysTick counter; a write clears the counter to zero and clears COUNTFLAG in SYST_CSR
0xE002.E01C	SYST_CALIB	SysTick->CALIB	Indicates the SysTick calibration value

4.4.3 Memory Protection Unit (MPU)

The Memory Protection Unit (MPU) can be used to check all memory accesses made by the processor against a set of access permission policies which can be defined by the programmer. When used together with the privileged/unprivileged execution modes of the Arm Cortex-M33, the MPU supports limiting access to certain memory locations to privileged code only. If unprivileged code accesses a nonrestricted region, execution continues as if the MPU was not present. However, if unprivileged code issues an access to a restricted region, a HardFault is generated if MemMange fault is not enabled in the processor. It is also possible to restrict access to both privileged and unprivileged code (no access possible through the processor).

The MPU is configured through memory-mapped registers in the system private peripheral bus (PPB) region. See *MPU Registers* for the list of MPU configuration registers. The software development kit (SDK) provided with the devices supports the standard Arm Cortex Microcontroller Software Interface Standard (CMSIS) register access definitions for the MPU.

Since the MPU checks all memory accesses from the processor (including accesses to flash, SRAM, and peripherals), it is well suited for improving reliability and robustness in threaded applications involving an RTOS. The MPU can be used to restrict the memory access of individual threads, including establishing stack boundaries and limiting access to specific peripherals. Key state data used by the RTOS can be protected from modification by unprivileged threads.

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Note

The MPU only monitors access to the memory map which originate from the processor. The MPU does not restrict the access of the DMA controller.

Note

Protecting flash memory regions with the MPU does not protect the flash memory from being read or modified by the flash controller. This is because the flash controller can take control of the flash memory banks directly for read verify, program, and erase operations. Dedicated write protection functions are provided within the flash controller, and these mechanisms are for use when write protecting the flash memory. Software can configure the MPU to restrict access to the flash controller registers, thus preventing the CPU from configuring or initiating a flash command directly.

The MPU provides a mechanism to partition the device memory map into 8 regions (numbered 0-7) plus a default background region. Each region can be configured with access permissions and memory attributes, and regions can be configured to overlap if desired. In the case of overlapping regions, a memory access to a location existing in multiple regions is subjected to the attributes of the region with the highest number.

When the MPU is not enabled (ENABLE bit is cleared in the MPU_CTRL register), the device uses the default memory map and the CPU has access to the memory map as if the MPU was not present.

When the MPU is enabled for use, access to the vector table and the system control space are always permitted, but access to any other location depends on the following:

- The region configurations
- Whether the access was privileged or unprivileged
- The privileged software default memory map access control configuration (PRIVDEFENA)

Because the Arm Cortex-M33 is a single-bus CPU architecture, there is no delineation between an instruction fetch and a data access by the MPU. Instructions and data are treated the same.

Note

If the MPU is enabled (ENABLE bit is set), then PRIVDEFENA must be set to give privileged software access to the memory map, or at least one memory region must be configured and enabled for the CPU to proceed without a hard fault. If PRIVDEFENA is cleared, no regions are defined and enabled, and the MPU is enabled, then the entire memory map is restricted, and any access generates a fault.

Table 4-7. MPU Registers

Address	Register	CMSIS	Description
0xE002.ED90	MPU_TYPE	MPU->TYPE	Type register indicating that if the MPU is present, and if so, how many regions supported
0xE002.ED94	MPU_CTRL	MPU->CTRL	MPU control register for enabling and configuring the MPU
0xE002.ED98	MPU_RNR	MPU->RNR	Region select register for using MPU_RBAR and MPU_RLAR
0xE002.ED9C	MPU_RBAR	MPU->RBAR	Defines the base address of the MPU region selected by the MPU_RNR
0xE002.EDA0	MPU_RLAR	MPU->RLAR	The MPU_RLAR defines the limit address of the MPU region selected by the MPU_RNR

For detailed information on the MPU register configuration, see the MPU section of the Arm Cortex-M33 Devices Generic User Guide.

4.4.4 Floating Point Unit (FPU)

The Cortex®-M33 Floating-Point Unit (FPU) implements the FPv5 floating-point extensions.The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

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The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

The FPU contains 32 single-precision extension registers, which users can also access as 16 doubleword registers for load, store, and move operations.

Note

The FPU is not connected to the NVIC. This requires the programmer to check the FPSCR register to see the status of the FPU, which is accessible by instruction.

Table 4-8. FPU Registers

Address	Register	CMSIS	Description
0xE002.EF34	FPCCR	FPU->FPCCR	Used to control different attributes of the FPU
0xE002.EF38	FPCAR	FPU->FPCAR	Holds the location of upopulated floating-point register space
0xE002.EF3C	FPDSCR	FPU->FPDSCR	Holds the default values for the floating-point status control data

For detailed information on the FPU, see the FPU section of the Arm Cortex-M33 Devices Generic User Guide.

4.4.5 Digital Signal Processing Extension

The Arm Cortex-M33 allows specific instructions to be used for digital signal processing (DSP). This gives programmers the ability to use the DSP instructions given in the Armv8-m instruction set. For more information on these instructions please see Armv8-M Architecture Reference Manual.

4.4.6 Custom Datapath Extension TMU

The Trigonometric Math Unit (TMU) is a floating-point hardware accelerator that uses the Custom Datapath Extension (CDE) interface of the Arm® Cortex-M33 to enable faster trigonometric math function functions. The trigonometric math functions are supported as an enhanced instruction set on the M33 core that utilizes the Floating Point Unit (FPU) registers for the operands and the data path implemented on the CDE interface. For more information on these instructions, please refer to Section 6 .

4.5 Read-Only Memory (ROM)

The CPUSS contains 48KB of read-only memory which contains the executable code for the boot configuration routine (BCR) and bootstrap loader (BSL). The ROM is active after a BOOTRST, or after a SYSRST with BSL entry/exit. The ROM is disabled automatically when the application is started and is not accessible by application software.

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Chapter 5

Secure Read-Only Memory (ROM)

The read-only memory (ROM) is used to configure the device before starting the user application.

5.1 ROM Overview

The ROM contains the executable code for the boot configuration routine (BCR) and bootstrap loader (BSL). The ROM includes:

- Lifecycle Detection of the device
- Configuring the SoC Security as per the NON-Main flash data
- Loads TI trim data
- Authentication of the Application in Flash
- Logs boot errors in all life-cycle states
- ROM Services
  - Authentication of service requests through DSSM
  - Debug Services
  - Key Services
  - RMA Services
  - BCR Existing Services

The ROM is active after a BOOTRST, or after a SYSRST with BSL entry/exit. The ROM is disabled automatically when the application is started and is not accessible by application software.

AM13E232x devices provide a 48KB ROM that includes the implementation for BCR and BSL.

The DSSM Commands for the AM13E232x device are detailed in Section 35.2.4.1 .

5.2 Memory Map

Table 5-1 details the high-level overview of different Flash, Data, Engineering, and TRIM Sectors and their associated protections.

Table 5-1. ROM Memory Map

Memory Usage	Memory Size	Start Address	Permission	Purpose
ROM	48KB	TI reserved	Immutable	BCR & BSL code
BANK0 NM0	2KB	0x6010_0000	Immutable and BCR has Write/Erase/Read permission	User keys
BANK0 NM1	2KB	0x6010_0800	Reprogrammable	BCR & BSL configuration
BANK1 NM0	2KB	0x6010_1000	BCR has Write/Erase/Read permission	Unused by ROM
BANK1 NM1	2KB	0x6010_1800	Reprogrammable	Additional user application storage

Note

The ROM does not utilize the BANK1 NM0/NM1 regions. BANK1 NM1 can be used by the user application as additional storage.

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5.3 Configuration Memory

The configuration memory is a dedicated region of flash memory (not the same as the code region) which stores the configuration data used by the BCR and BSL to boot the device. This memory region is called the NONMAIN Flash region. This region is not used for any other purpose. The BCR and BSL both have configuration policies which can be left at their default values (as is typical during development and evaluation), or modified for specific purposes (as is typical during production programming) by altering the values programmed into the configuration flash region.

The BCR and BSL configuration data structures are both contained within a single flash sector in the configuration memory region. To change any parameter in the boot configuration, it is necessary to erase the entire configuration memory and re-program both the BCR and BSL configuration structures with the desired settings.

The configuration data in this region is not affected by a mass erase command, but it is erased and re-programmed to factory defaults by a factory reset command sent to the BCR via the debug sub system mailbox (DSSM) over SWD/JTAG.

The configuration memory is also erased by a factory reset command sent to the BSL using the UART, I2C, or MCAN BSL interface. However, unlike the DSSM factory reset, the BSL factory reset does not program TI factory defaults to the configuration memory following the erase. As such, it is the responsibility of the host which is connected to the microcontroller target (via the BSL interface) to re-program the configuration memory with a valid configuration before terminating the BSL session.

Note

If a factory reset command is executed through the BSL, and a valid configuration is not programmed back into the device before the BSL session is terminated, the device will assume a maximally restrictive state upon the next reset cycle, and it will not be possible to access the device via SWD/JTAG or the BSL. Always ensure that a valid configuration is programmed back when using the BSL factory reset command.

A detailed breakdown of the NONMAIN region registers is provided at the end of this section.

5.3.1 Boot Configuration Routine (BCR)

The boot configuration routine is the first firmware to run on the device after a BOOTRST. The BCR manages the following at boot time:

- Configuring the debug interface security policy
- Optionally executing a mass erase
- Optionally executing a factory reset
- Configuring the flash memory static write protection policy
- Optionally verifying the integrity of some or all of the application firmware (with a 32-bit CRC)
- Optionally starting the bootstrap loader (BSL)

5.3.1.1 SWD Mass Erase and Factory Reset Commands

The BCR provides mass erase and factory reset functionality through commands sent to the device over SWD from a debug probe using the debug subsystem mailbox (DSSM). When the device is not configured for SWD disabled, the mass erase and factory reset commands can be individually configured to be enabled with a unique 128-bit password, or disabled. By default, both commands are enabled.

The SWD mass erase and factory reset DSSM commands supersede any static write protection policies. For example, if SWD factory reset is configured to be enabled or enabled with password, the BCR configuration data can be reset even if it is statically write protected.

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SWD Mass Erase

A SWD mass erase is an erase of the MAIN flash regions only, which typically includes the user application. The BCR and BSL policies stored in the NONMAIN flash region are not affected by a mass erase. A mass erase is useful for erasing all application code and data while leaving the device configuration itself intact.

To set the mass erase command mode and password, configure the BOOTCFG3.MASSERASECMDACCESS field and the PWDMASSERASE password fields in the NONMAIN memory.

SWD Factory Reset

A SWD factory reset is an erase of the MAIN flash regions followed by a reset of the NONMAIN flash region to default values. Such an erase is useful for completely resetting the BCR and BSL device boot policies while also erasing the application code and data.

To set the factory reset command mode and password, configure the BOOTCFG3.FACTORYRESETCMDACCESS field and the PWDFACTORYRESET password fields in the NONMAIN memory.

5.3.1.2 Fast Boot

The execution time of the BCR can be reduced by enabling fast boot mode. Fast boot mode, when enabled, speeds up the boot process using the following methods:

- Limiting the BSL entry methods. When fast boot mode is enabled, only the SYSCTL register invoke method and the DSSM invoke method can be used to enter the bootloader. The other BSL invoke conditions are not tested (for example, pin based invoke).
- Bypassing the application CRC check (even if the application CRC check is enabled).

To enable fast boot mode, set the fast boot mode to enabled in the BOOTCFG2.FASTBOOTMODE field in the configuration memory.

5.3.2 Bootstrap Loader (BSL)

The bootstrap loader (BSL) provides a method to program and/or verify the device memory through a standard UART, I2C, or MCAN interface. Key features of the BSL which are accessible through the serial interface include:

- Programming and erase of flash memory
- Ability to return a firmware version number through a pointer to the main flash
- Ability to specify a hardware invoke GPIO
- Ability to enable code/data read-out (disabled by default)
- Ability to return a 32-bit CRC of a code/data region (2KB minimum region size) to verify programming
- Access is always protected with a 256-bit password
- Configurable security alert handling for resisting brute force attacks
- Configurable UART, I2C and MCAN pins

For a complete description of the BSL features, see the *AM13E23x Bootstrap Loader User's Guide*.

The BSL can be enabled or disabled by setting the bootloader mode to enabled or disabled in the BOOTCFG2.BSLMODE field in the NONMAIN flash memory. When the BSL is disabled, the bootloader cannot be entered through any invocation mechanism and the device will boot from the application code in the flash.

5.3.2.1 Application Version

The BSL supports returning an application version number through the BSL serial interface. This allows the BSL host to interrogate the firmware version without being able to read the firmware. The version field is 32 bits in length. To link the application version command to a version number programmed in the main flash, program the address of the version number in the APP_REV_POINTER field in configuration memory. The version data is only returned if the address specified in APP_REV_POINTER corresponds to a valid flash memory address.

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5.3.2.2 GPIO Invoke

The bootloader supports hardware invoking after a BOOTRST through the use of a GPIO. The BSL configuration in the configuration memory contains the pad, pin, and polarity definition for the GPIO invocation. Devices come configured from TI for a specific GPIO and polarity, but software can change this default by modifying the GPIO pin configuration in the BSL configuration in configuration memory.

To specify the polarity of the BSL_invoke pin, configure the BSLCONFIG0.BSLIVK_LVL field in the configuration memory.

To specify the device pin to be used for BSL_invoke, configure the following fields in the configuration memory:

- Store the IOMUX PINCMx index into the BSLCONFIG0.BSLIVK_PAD_NUM field
- Store the GPIO port (A/B/C/D) into the BSLCONFIG0.BSLIVK_GPIOPORT field
- Store the GPIO pin (0-31) into the BSLCONFIG0.BSLIVK_GPIOPIN field

See the device specific data sheet to determine the default BSL invoke GPIO.

5.3.2.3 BSL Triggered Mass Erase and Factory Reset

It is possible to send a mass erase or factory reset command to the BSL. The commands work in a similar way as the SWD mass erase and factory reset commands, with several key exceptions.

BSL Mass Erase

A mass erase command sent to the BSL will erase the MAIN flash memory.
Any MAIN flash memory sectors which are configured to be statically write protected (via the BANK0_WRITE_ERASE_PROTECTION_A, BANK0_WRITE_ERASE_PROTECTION_B, BANK1_WRITE_ERASE_PROTECTION_A and BANK1_WRITE_ERASE_PROTECTION_B fields in the configuration memory) will not be erased. The device configuration memory is never erased by a mass erase.

BSL Factory Reset

A factory reset command sent to the BSL will first perform a BSL mass erase to erase the main flash memory (excluding any sectors which are statically write protected). Then, it will additionally erase the device configuration memory.

A BSL factory reset command is only accepted if the following are true:

1. The configuration memory itself is not currently configured to be statically write protected (BANK0_NM_USER_CONFIG field in the configuration memory is set to not protected)
2. The factory reset command is not configured to be disabled (BOOTCFG4.FACTORY_RESET_MODE field in the configuration memory is not set to disabled)

The BSL host must program valid configuration data back into the configuration memory (via BSL commands) before terminating the BSL session, or the device may enter an unrecoverable state.

Note

If the configuration memory is left unprogrammed after a BSL factory reset, the device will assume a maximally restrictive state on the next reset cycle, any application code in MAIN flash will not be started, and it will not be possible to access the device via any means. To prevent lockout, always ensure that valid configuration data is programmed into configuration memory following a BSL factory reset.

5.4 Lifecycle Management

AM13E232x devices support lifecycle management to manage the device process from the TI factory to customer development, to production, to end-of-life. The Lifecycle Management controls which features of the device are enabled at each stage of the product's life.

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Lifecycle management allows customers to increase the level of security from open to completely closed in a controlled manner, and prevent on-device information from getting leaked by converting the device to a specific state when the device is at its end-of-life or in failure analysis.

The device ROM code supports the AM13E232x lifecycle with two states that represent the operation state of the device:

- HS (High Security) - fully operational unit
  - The HS lifecycle state is broken down into multiple **Device Sub-Type** states that represent the specific configuration of the operational device.
- BAD/DCOM - decomissioned or faulty unit

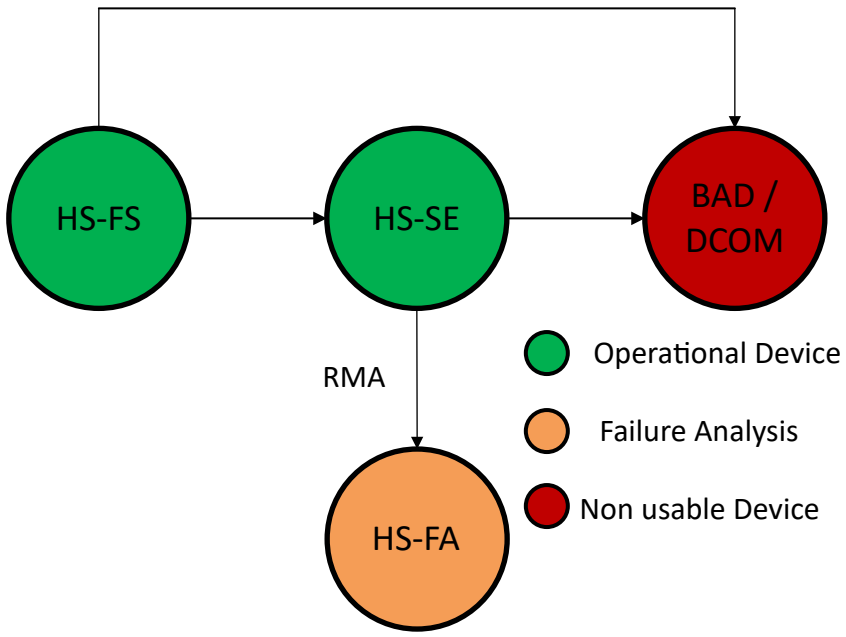


Figure 5-1. AM13E232x Lifecycle Transitions

5.4.1 Device Sub-Type

HS (High Security) lifecycle state is divided into the following **Device Sub-Type** states. The bootcode will read the corresponding security sector to determine the device sub-types for High Security.

- HS-FS (High Security-Field Securable): The devices are shipped from TI in this state. In the HS-FS state, the device can be used with or without security features. If security features are not required, then the device will remain in this state for the rest of the device's lifecycle (**unless the device enters a BAD state or a failure analysis is performed)**.
- HS-SE (High Security-Security Enforced): This is the state the device moves to once the signed CSC (Customer Secure Code) or application has been programmed and verified by Secure Boot.

In addition to the two above Operational Device states, the device enters HS-FA (High Security-Failure Analysis) state when failure analysis is enabled on the device.

5.4.2 Lifecycle Transitions

During the life of the device, the state is changed depending on the current state of the device and the security settings applied.

The following sequence transitions a device from HS-FS to HS-SE:

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1. If debug port is not locked, application/CSC can be programmed via debug port
2. Alternatively, invoke the BSL to program the application over supported BSL interfaces (UART/I2C/MCAN)
3. Program the signed CSC or application over BSL
4. Once ROM validates the CSC or application, the device is marked as HS-SE

The following sequence transitions a device from HS-SE to HS-FA:

1. DSSM command (DSSM_COMMAND_RMA) shall be given to the device by the user
2. If Combined Certificate is received and validated, then ROM marks the device as HS-FA
3. Device will go into HS-FA Authenticated flow

To convert a device to DCOM/BAD, the user can send the DSSM command DSSM_COMMAND_CONVERT_BAD_DEVICE.

Note

Customer Return Flow

Customers need to transition the device to HS-FA state from HS-SE before sending the device back to TI for failure analysis. Customer has the option to secure the different assets (e.g. code, keys, etc.) by programming / erasing them. Customer should be aware that erasing the content will restrict / limit the debug of some of the failures (e.g. flash data retention failure cannot be debugged once the content is erased).

5.5 Boot and Startup Sequence

Figure 5-2 illustrates the boot and startup sequence in security enabled applications. At BOOTRST, TI Bootcode starts executing. According to the device's lifecycle status, the device will execute the corresponding process as regular boot, secure boot, or retest flow.

The Bootloader (BSL) can be invoked by Bootcode when a valid bootloader invocation condition is detected. The Bootloader provides a method to program and verify the device Flash memory through a standard serial interface (see Section 5.3.2).

During the Bootcode execution, the Debug Subsystem Mailbox (DSSM) enables a debug probe to pass messages to the target device through the Serial Wire Debug (SWD) interface, and for the target device to return data to the debug probe. In Bootcode, the DSSM helps with the transmission of commands to the device during boot, including lifecycle state change requests, authenticating the debug probe for password-protected debug, mass erase, and factory reset operations.

After a successful boot, the Bootcode issues BOOTDONE. At this point in the sequence, SYSCTL issues a SYSRST to the device to trigger execution from flash memory. Depending on the boot configuration record, this leads to either the start of the main application (if CSC does **not** exist in this configuration) or to the start of the CSC (if CSC is configured).

CSC (Customer Secure Code) executes from flash memory to further configure security elements. Note that CSC is **customer-owned** secure software. This two-step secure boot concept enables application-specific policies to be implemented and managed by CSC while the standard security enablers are implemented by Bootcode. When CSC has completed execution, the system undergoes a second SYSRST followed by the start of the main aplication.

In this security model, both TI Bootcode and CSC are considered *trusted*. The main application is considered *untrusted*. When execution jumps to the main application, all security elements are expected to have been configured, including restrictions on the debug port, memory accesses, and key management.

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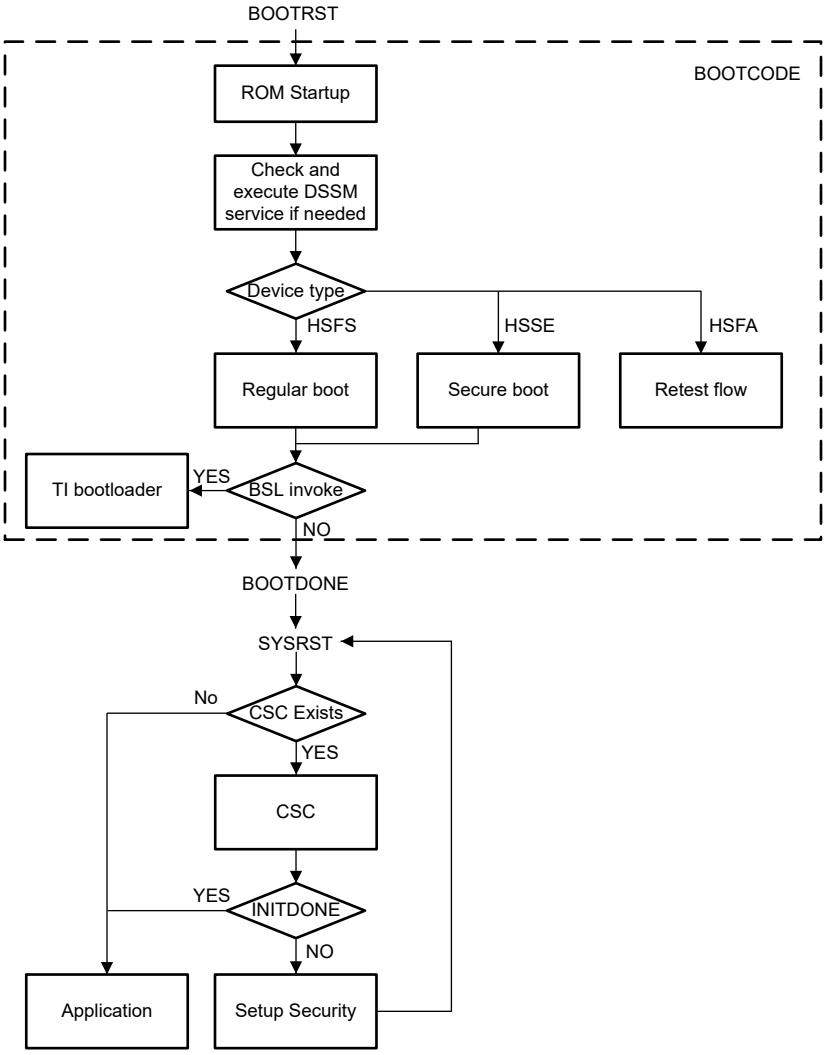


Figure 5-2. AM13E232x Secure Boot and Startup Sequence

Note

The AM13E232x security architecture provides a clean separation between policies and mechanisms. It is possible to build applications where no CSC is implemented and the main application begins immediately following BOOTRST.

The secure exection flow is the path where CSC_EXISTS = YES. In this case, it may be observed that after BOOTRST, two SYSRSTs will be issues before the main application is launched.

After the first SYSRST, the CSC executes. It configures security and issues INITDONE = NO. At this point, the security configuration is locked and enforced. A second SYSRST is issued, and restarts CSC execution. At the second SYSRST, INITDONE = YES and the main application is launched.

If CSC is not enabled, then only one SYSRST is issued and the application launches following the reset.

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5.5.1 Secure Boot

AM13E232x devices support an immutable secure boot in ROM leveraging the device's lifecycle management. The immutable secure boot establishes a chain of trust that allows the execution of authenticated and authorized firmware on the device, utilizing the device's lifecycle management transitions: from a provisioning state (HS-FS) to a permanently secured operational state (HS-SE).

Secure boot provides mechanisms to validate image integrity through 128-bit CMAC, and verify key integrity via BCH encoding. ROM secure boot supports the following features:

- Verification of the integrity of the firmware through 128-bit CMAC
- Anti-rollback to prevent downgrade to older firmware that can be a potentail security vulberibility
- Key revocation to decomission compromised keys - support for up to 4 keys
- TI proprietary MCUBoot trailer processing for security metadata

AM13E232x devices support up to 4 keys. Secure boot uses the first key for verification. The rest of the keys are utilized if the first key is revoked.

Secure boot is performed only when the device is in HS-SE state. In HS-SE state, secure boot is performed during one of the following conditions:

- BOOTRST
- Power-on reset
- Wake up from Shutdown

5.5.2 Customer Secure Code (CSC)

If the user wants to add additional features or functionality to the immutable secure boot on AM13E232x devices, then a Customer Secure Code (CSC) (also referred to as the secondary bootloader) can be implemented in the MAIN flash of the device. The ROM provides the following features to support the CSC:

- Bank swap decision
- Initialization of the secure key store

When the CSC issues INITDONE (by writing to SYSCTL.SECCFG.INITDONE MMR) then SYSCTL issues the second SYSRST (as outlined in Section 5.5). The device again starts execution from 0x0 mapped to flash, and the CSC executes a second time. After the second CSC execution, the CSC will find that INITDONE has already been issued previously (from after the first CSC execution), determined by reading the SYSCTL.SECCFG.SECSTATUS.INITDONE bit. The main application is then called.

The customer owned secure code can leverage the Global Security Controller (GSC) to implement additional security capabilities such as:

- Flash read-execute protection
- Flash IP protection
- SRAM write-execute mutual exclusion

The CSC specifies which bank holds the more recent authenticated application image. If that bank is physical bank 0 (same bank as where CSC is executing from), then bank 1 is read-write only and does not have execute privilege. If the correct application image is determined to be on physical bank 1, then the CSC must issue a bank-swap request.

The CSC indicates the end of CSC execution by writing to the SYSCTL.SECCFG.INITDONE register with a PASS value (0x1) along with a KEY value of 0x9d. Successfully writing to the INITDONE register results in a second SYSRST operation during which the bank-swap takes effect.

5.6 NONMAIN Registers

This Section describes the NONMAIN Registers.

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5.6.1 NONMAIN Base Address Table

Table 5-2. NONMAIN Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
NonMainRegs	NONMAIN_REGION_REGS	NONMAIN	0x6010_0000
NonMainRegs	NONMAIN_REGION_REGS	NONMAIN	0x6010_1000

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5.6.2 NONMAIN_REGION_REGS Registers

Table 5-3 lists the memory-mapped registers for the NONMAIN_REGION_REGS registers. All register offset addresses not listed in Table 5-3 should be considered as reserved locations and the register contents should not be modified.

Table 5-3. NONMAIN_REGION_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	BCR_CONFIG_ID	Predetermined Bootcode config signature ID		Go
4h	BOOTCFG0	Controls enable/disable of AHB-AP, ET-AP, PWR-AP. Values: DEBUG_EN, DEBUG_EN_PW, DEBUG_NS_EN, DEBUG_NS_EN_PW, DEBUG_DIS; Serial Wire Debug Port mode. Disabling this will disable all Debug ports including CFG_AP, SEC_AP. When disabled no DSSM commands are serviced		Go
8h	BOOTCFG1	Controls BSL pin invocation capability. Values: BSL_PIN_INVOKE_EN, BSL_PIN_INVOKE_DIS; Controls debug access release until INITDONE is issued		Go
Ch	BOOTCFG2	Controls CSC policy in SYSCTL. YES enables CSC policy checking; Controls flash bank swap policy in SYSCTL		Go
10h	BOOTCFG3	Fast boot mode configuration - Skips certain boot time checks when enabled; Bootloader mode enable/disable control. Must be enabled for BSL functionality		Go
14h	BOOTCFG4	Mass erase mode configuration. Values: BC_CFG_MASS_ERASE_EN(0xAABB), BC_CFG_MASS_ERASE_EN_PW(0xCCDD), BC_CFG_MASS_ERASE_DIS(0x5522); Factory reset mode configuration. Values: BC_CFG_FACTORY_RESET_EN(0xAABB), BC_CFG_FACTORY_RESET_EN_PW(0xCCDD), BC_CFG_FACTORY_RESET_DIS(0x5522)		Go
18h	MASS_ERASE_0	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 0		Go
1Ch	MASS_ERASE_1	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 1		Go
20h	MASS_ERASE_2	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 2		Go
24h	MASS_ERASE_3	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 3		Go
28h	MASS_ERASE_4	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 4		Go
2Ch	MASS_ERASE_5	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 5		Go
30h	MASS_ERASE_6	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 6		Go
34h	MASS_ERASE_7	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 7		Go

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Table 5-3. NONMAIN_REGION_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
38h	FACTORY_RESET_0	Password for factory reset command - Word 0		Go
3Ch	FACTORY_RESET_1	Password for factory reset command - Word 1		Go
40h	FACTORY_RESET_2	Password for factory reset command - Word 2		Go
44h	FACTORY_RESET_3	Password for factory reset command - Word 3		Go
48h	FACTORY_RESET_4	Password for factory reset command - Word 4		Go
4Ch	FACTORY_RESET_5	Password for factory reset command - Word 5		Go
50h	FACTORY_RESET_6	Password for factory reset command - Word 6		Go
54h	FACTORY_RESET_7	Password for factory reset command - Word 7		Go
58h	DEBUG_LOCK_0	Password for debug access authentication - Word 0		Go
5Ch	DEBUG_LOCK_1	Password for debug access authentication - Word 1		Go
60h	DEBUG_LOCK_2	Password for debug access authentication - Word 2		Go
64h	DEBUG_LOCK_3	Password for debug access authentication - Word 3		Go
68h	DEBUG_LOCK_4	Password for debug access authentication - Word 4		Go
6Ch	DEBUG_LOCK_5	Password for debug access authentication - Word 5		Go
70h	DEBUG_LOCK_6	Password for debug access authentication - Word 6		Go
74h	DEBUG_LOCK_7	Password for debug access authentication - Word 7		Go
78h	DEBUG_NS_LOCK_0	Password for non-secure debug access - Word 0		Go
7Ch	DEBUG_NS_LOCK_1	Password for non-secure debug access - Word 1		Go
80h	DEBUG_NS_LOCK_2	Password for non-secure debug access - Word 2		Go
84h	DEBUG_NS_LOCK_3	Password for non-secure debug access - Word 3		Go
88h	DEBUG_NS_LOCK_4	Password for non-secure debug access - Word 4		Go
8Ch	DEBUG_NS_LOCK_5	Password for non-secure debug access - Word 5		Go
90h	DEBUG_NS_LOCK_6	Password for non-secure debug access - Word 6		Go
94h	DEBUG_NS_LOCK_7	Password for non-secure debug access - Word 7		Go
98h	RESERVED_REG0			
9Ch	RESERVED_REG1			
A0h	RESERVED_REG2			
A4h	RESERVED_REG3			
A8h	RESERVED_REG4			
ACh	RESERVED_REG5	Reserved - Word 5		
B0h	RESERVED_REG6	Reserved - Word 6		
B4h	RESERVED_REG7	Reserved - Word 7		
B8h	SECURE_BOOT_MODE	Controls application authentication; Reserved field		
BCh	USER_SECURE_APP_START_ADDR	Starting address for secure application		Go
C0h	USER_SECURE_APP_LENGTH	Length of secure application		Go
C4h	USER_SECURE_APP_CRC_0	Secure application CRC - Word 0		Go
C8h	RESERVED_REG8	Reserved field - Word 1		
CCh	RESERVED_REG9	Reserved field - Word 2		

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Table 5-3. NONMAIN_REGION_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
D0h	RESERVED_REG10	Reserved field - Word 3		
D4h	RESERVED_REG11	Reserved field - Word 4		
D8h	RESERVED_REG12	Reserved field - Word 5		
DCh	RESERVED_REG13	Reserved field - Word 6		
E0h	RESERVED_REG14	Reserved field - Word 7		
E4h	BANK0_NM_USER_CONFIG	User Config Non Main Flash Static Write Protection. WEP_DISABLE=0xAABB; Reserved field		
E8h	BANK0_WRITE_ERASE_PROTECTION_A	Write protection for first 32 sectors		Go
ECh	BANK0_WRITE_ERASE_PROTECTION_B	Write Protection for 512KB-64KB		Go
F0h	BANK0_SECURITY_PROTECTION_A	Security protection for first 32 sectors		Go
F4h	BANK0_SECURITY_PROTECTION_B	Security protection for 512KB-64KB		Go
F8h	BANK0_PRIVILEGE_PROTECTION_A	Privilege protection for first 32 sectors		Go
FCh	BANK0_PRIVILEGE_PROTECTION_B	Privilege protection for 512KB-64KB		Go
100h	BANK0_RESERVED	Reserved field for BANK0 alignment		
104h	BANK1_WRITE_ERASE_PROTECTION_A	Write protection for first 32 sectors		Go
108h	BANK1_WRITE_ERASE_PROTECTION_B	Write Protection for 512KB-64KB		Go
10Ch	BANK1_SECURITY_PROTECTION_A	Security protection for first 32 sectors		Go
110h	BANK1_SECURITY_PROTECTION_B	Security protection for 512KB-64KB		Go
114h	BANK1_PRIVILEGE_PROTECTION_A	Privilege protection for first 32 sectors		Go
118h	BANK1_PRIVILEGE_PROTECTION_B	Privilege protection for 512KB-64KB		Go
11Ch	BANK1_RESERVED	Reserved field for BANK1		
120h	RESERVED_REG15	Reserved field		
124h	RESERVED_REG16	Reserved field		
128h	RESERVED_REG17	Reserved field		
12Ch	RESERVED_REG18	Reserved field		
130h	BOOTCLK0	Clock configuration; PLL multiplier value; PLL divider value; PLL clock source configuration		Go
134h	BOOTCLK1	CPU delay cycles for PLL settling time; CPU delay cycles for XTAL monitoring; Reserved configuration field 0		
138h	RESERVED_REG_0	Reserved configuration field 0; Reserved configuration field 1		
13Ch	RESERVED_REG_1	Reserved configuration field 2; Reserved configuration field 3		
140h	RESERVED_REG_2	Reserved configuration field 4; Reserved configuration field 5		
144h	RESERVED_REG_3	Reserved configuration field 6; Reserved configuration field 7		

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Table 5-3. NONMAIN_REGION_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
148h	RESERVED_REG_4	Reserved configuration field 8; Reserved configuration field 9		
14Ch	CRC	JAMCRC of BCR config structure		Go
0h	BSL_CONFIG_ID	Predetermined Bootloader config signature ID		Go
4h	BSLPINCFG0	UART receive pin number configuration; UART receive pin multiplexer selection; UART transmit pin number configuration; UART transmit pin multiplexer selection		Go
8h	BSLPINCFG1	I2C data pin number configuration; I2C data pin multiplexer selection; I2C clock pin number configuration; I2C clock pin multiplexer selection		Go
Ch	BSLPINCFG2	MCAN receive pin number configuration; MCAN receive pin multiplexer selection; MCAN transmit pin number configuration; MCAN transmit pin multiplexer selection		Go
10h	BSLCONFIG0	BSL invoke pin configuration data 0; BSL invoke pin configuration data 1; Memory readout control. ENABLE allows memory read operations		Go
14h	PASSWORD_0	BSL access password - Word 0		Go
18h	PASSWORD_1	BSL access password - Word 1		Go
1Ch	PASSWORD_2	BSL access password - Word 2		Go
20h	PASSWORD_3	BSL access password - Word 3		Go
24h	PASSWORD_4	BSL access password - Word 4		Go
28h	PASSWORD_5	BSL access password - Word 5		Go
2Ch	PASSWORD_6	BSL access password - Word 6		Go
30h	PASSWORD_7	BSL access password - Word 7		Go
34h	APP_REV_POINTER	Pointer to application version information in MAIN flash		Go
38h	BSLCONFIG1	Security alert response: Factory Reset/Disable BSL/Ignore; UART communication speed selection for ROM BSL		Go
3Ch	I2C_SLAVE_ADDR	I2C slave address for ROM BSL I2C interface; Reserved field; Reserved field		
40h	RESERVED_REG_0	Reserved field; Reserved field; Reserved field; Reserved field		
44h	RESERVED_REG_1	Reserved field; Reserved field; Reserved field; Reserved field		
48h	RESERVED_REG_2	Reserved field; Reserved field; Reserved field; Reserved field		
4Ch	CRC	JAMCRC of BSL configuration structure		Go

Complex bit access types are encoded to fit into small table cells. Table 5-4 shows the codes that are used for access types in this section.

Table 5-4. NONMAIN_REGION_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

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Table 5-4. NONMAIN_REGION_REGS Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

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1 BCR_CONFIG_ID Register (Offset = 0h) [Reset = 00000000h]

BCR_CONFIG_ID is shown in Figure 5-3 and described in Table 5-5.

Return to the Summary Table.

Predetermined Bootcode config signature ID

Figure 5-3. BCR_CONFIG_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCR_CONFIG_ID																															
R/W-0h																															

Table 5-6. BCR_CONFIG_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCR_CONFIG_ID	R/W	0h	Predetermined Bootcode config signature ID

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2 BOOTCFG0 Register (Offset = 4h) [Reset = 00000000h]

BOOTCFG0 is shown in Figure 5-4 and described in Table 5-6.

Return to the Summary Table.

Controls enable/disable of AHB-AP, ET-AP, PWR-AP. Values: DEBUG_EN, DEBUG_EN_PW, DEBUG_NS_EN, DEBUG_NS_EN_PW, DEBUG_DIS
Serial Wire Debug Port mode. Disabling this will disable all Debug ports including CFG_AP, SEC_AP. When disabled no DSSM commands are serviced

Figure 5-4. BOOTCFG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWDP_MODE																DEBUG_ACCESS															
R/W-0h																R/W-0h															

Table 5-8. BOOTCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SWDP_MODE	R/W	0h	Serial Wire Debug Port mode. Disabling this will disable all Debug ports including CFG_AP, SEC_AP. When disabled no DSSM commands are serviced 5522h = DISABLED configuration AABBh = ENABLED configuration
15-0	DEBUG_ACCESS	R/W	0h	Controls enable/disable of AHB-AP, ET-AP, PWR-AP. Values: DEBUG_EN, DEBUG_EN_PW, DEBUG_NS_EN, DEBUG_NS_EN_PW, DEBUG_DIS 5522h = DISABLED configuration AABBh = ENABLED configuration

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3 BOOTCFG1 Register (Offset = 8h) [Reset = 00000000h]

BOOTCFG1 is shown in Figure 5-5 and described in Table 5-7.

Return to the Summary Table.

Controls BSL pin invocation capability. Values: BSL_PIN_INVOKE_EN, BSL_PIN_INVOKE_DIS
Controls debug access release until INITDONE is issued

Figure 5-5. BOOTCFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_HOLD																BSL_PIN_INVOKE															
R/W-0h																R/W-0h															

Table 5-10. BOOTCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DEBUG_HOLD	R/W	0h	Controls debug access release until INITDONE is issued
15-0	BSL_PIN_INVOKE	R/W	0h	Controls BSL pin invocation capability. Values: BSL_PIN_INVOKE_EN, BSL_PIN_INVOKE_DIS 5522h = DISABLED configuration AABBh = ENABLED configuration

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4 BOOTCFG2 Register (Offset = Ch) [Reset = 00000000h]

BOOTCFG2 is shown in Figure 5-6 and described in Table 5-8.

Return to the Summary Table.

Controls CSC policy in SYSCTL. YES enables CSC policy checking
Controls flash bank swap policy in SYSCTL

Figure 5-6. BOOTCFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FLASH_BANK_SWAP_POLICY															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_EXISTS															
R/W-0h															

Table 5-12. BOOTCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FLASH_BANK_SWAP_POLICY	R/W	0h	Controls flash bank swap policy in SYSCTL
15-0	CSC_EXISTS	R/W	0h	Controls CSC policy in SYSCTL. YES enables CSC policy checking 5522h = DISABLED configuration AABBh = ENABLED configuration

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5 BOOTCFG3 Register (Offset = 10h) [Reset = 00000000h]

BOOTCFG3 is shown in Figure 5-7 and described in Table 5-9.

Return to the Summary Table.

Fast boot mode configuration - Skips certain boot time checks when enabled
Bootloader mode enable/disable control. Must be enabled for BSL functionality

Figure 5-7. BOOTCFG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOTLOADER_MODE																FAST_BOOT_MODE															
R/W-0h																R/W-0h															

Table 5-14. BOOTCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	BOOTLOADER_MODE	R/W	0h	Bootloader mode enable/disable control. Must be enabled for BSL functionality
15-0	FAST_BOOT_MODE	R/W	0h	Fast boot mode configuration - Skips certain boot time checks when enabled

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6 BOOTCFG4 Register (Offset = 14h) [Reset = 00000000h]

BOOTCFG4 is shown in Figure 5-8 and described in Table 5-10.

Return to the Summary Table.

Mass erase mode configuration. Values: BC_CFG_MASS_ERASE_EN(0xAABB), BC_CFG_MASS_ERASE_EN_PW(0xCCDD), BC_CFG_MASS_ERASE_DIS(0x5522)
Factory reset mode configuration. Values: BC_CFG_FACTORY_RESET_EN(0xAABB), BC_CFG_FACTORY_RESET_EN_PW(0xCCDD), BC_CFG_FACTORY_RESET_DIS(0x5522)

Figure 5-8. BOOTCFG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FACTORY_RESET_MODE															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_MODE															
R/W-0h															

Table 5-16. BOOTCFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FACTORY_RESET_MODE	R/W	0h	Factory reset mode configuration. Values: BC_CFG_FACTORY_RESET_EN(0xAABB), BC_CFG_FACTORY_RESET_EN_PW(0xCCDD), BC_CFG_FACTORY_RESET_DIS(0x5522) 5522h = DISABLE configuration AABBh = ENABLE configuration CCDDh = ENABLE_WITH_PASSWORD configuration
15-0	MASS_ERASE_MODE	R/W	0h	Mass erase mode configuration. Values: BC_CFG_MASS_ERASE_EN(0xAABB), BC_CFG_MASS_ERASE_EN_PW(0xCCDD), BC_CFG_MASS_ERASE_DIS(0x5522) 5522h = DISABLE configuration AABBh = ENABLE configuration CCDDh = ENABLE_WITH_PASSWORD configuration

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7 MASS_ERASE_0 Register (Offset = 18h) [Reset = 00000000h]

MASS_ERASE_0 is shown in Figure 5-9 and described in Table 5-11.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 0

Figure 5-9. MASS_ERASE_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_0																															
R/W-0h																															

Table 5-18. MASS_ERASE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_0	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 0

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8 MASS_ERASE_1 Register (Offset = 1Ch) [Reset = 00000000h]

MASS_ERASE_1 is shown in Figure 5-10 and described in Table 5-12.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 1

Figure 5-10. MASS_ERASE_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_1																															
R/W-0h																															

Table 5-20. MASS_ERASE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_1	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 1

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9 MASS_ERASE_2 Register (Offset = 20h) [Reset = 00000000h]

MASS_ERASE_2 is shown in Figure 5-11 and described in Table 5-13.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 2

Figure 5-11. MASS_ERASE_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_2																															
R/W-0h																															

Table 5-22. MASS_ERASE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_2	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 2

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10 MASS_ERASE_3 Register (Offset = 24h) [Reset = 00000000h]

MASS_ERASE_3 is shown in Figure 5-12 and described in Table 5-14.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 3

Figure 5-12. MASS_ERASE_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_3																															
R/W-0h																															

Table 5-24. MASS_ERASE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_3	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 3

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11 MASS_ERASE_4 Register (Offset = 28h) [Reset = 00000000h]

MASS_ERASE_4 is shown in Figure 5-13 and described in Table 5-15.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 4

Figure 5-13. MASS_ERASE_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_4																															
R/W-0h																															

Table 5-26. MASS_ERASE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_4	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 4

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12 MASS_ERASE_5 Register (Offset = 2Ch) [Reset = 00000000h]

MASS_ERASE_5 is shown in Figure 5-14 and described in Table 5-16.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 5

Figure 5-14. MASS_ERASE_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_5																															
R/W-0h																															

Table 5-28. MASS_ERASE_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_5	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 5

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13 MASS_ERASE_6 Register (Offset = 30h) [Reset = 00000000h]

MASS_ERASE_6 is shown in Figure 5-15 and described in Table 5-17.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 6

Figure 5-15. MASS_ERASE_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_6																															
R/W-0h																															

Table 5-30. MASS_ERASE_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_6	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 6

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14 MASS_ERASE_7 Register (Offset = 34h) [Reset = 00000000h]

MASS_ERASE_7 is shown in Figure 5-16 and described in Table 5-18.

Return to the Summary Table.

Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 7

Figure 5-16. MASS_ERASE_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASS_ERASE_7																															
R/W-0h																															

Table 5-32. MASS_ERASE_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MASS_ERASE_7	R/W	0h	Password for DSSM_BC_MASS_ERASE_REQUEST command - Word 7

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15 FACTORY_RESET_0 Register (Offset = 38h) [Reset = 00000000h]

FACTORY_RESET_0 is shown in Figure 5-17 and described in Table 5-19.

Return to the Summary Table.

Password for factory reset command - Word 0

Figure 5-17. FACTORY_RESET_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_0																															
R/W-0h																															

Table 5-34. FACTORY_RESET_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_0	R/W	0h	Password for factory reset command - Word 0

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16 FACTORY_RESET_1 Register (Offset = 3Ch) [Reset = 00000000h]

FACTORY_RESET_1 is shown in Figure 5-18 and described in Table 5-20.

Return to the Summary Table.

Password for factory reset command - Word 1

Figure 5-18. FACTORY_RESET_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_1																															
R/W-0h																															

Table 5-36. FACTORY_RESET_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_1	R/W	0h	Password for factory reset command - Word 1

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17 FACTORY_RESET_2 Register (Offset = 40h) [Reset = 00000000h]

FACTORY_RESET_2 is shown in Figure 5-19 and described in Table 5-21.

Return to the Summary Table.

Password for factory reset command - Word 2

Figure 5-19. FACTORY_RESET_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_2																															
R/W-0h																															

Table 5-38. FACTORY_RESET_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_2	R/W	0h	Password for factory reset command - Word 2

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18 FACTORY_RESET_3 Register (Offset = 44h) [Reset = 00000000h]

FACTORY_RESET_3 is shown in Figure 5-20 and described in Table 5-22.

Return to the Summary Table.

Password for factory reset command - Word 3

Figure 5-20. FACTORY_RESET_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_3																															
R/W-0h																															

Table 5-40. FACTORY_RESET_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_3	R/W	0h	Password for factory reset command - Word 3

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19 FACTORY_RESET_4 Register (Offset = 48h) [Reset = 00000000h]

FACTORY_RESET_4 is shown in Figure 5-21 and described in Table 5-23.

Return to the Summary Table.

Password for factory reset command - Word 4

Figure 5-21. FACTORY_RESET_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_4																															
R/W-0h																															

Table 5-42. FACTORY_RESET_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_4	R/W	0h	Password for factory reset command - Word 4

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20 FACTORY_RESET_5 Register (Offset = 4Ch) [Reset = 00000000h]

FACTORY_RESET_5 is shown in Figure 5-22 and described in Table 5-24.

Return to the Summary Table.

Password for factory reset command - Word 5

Figure 5-22. FACTORY_RESET_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_5																															
R/W-0h																															

Table 5-44. FACTORY_RESET_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_5	R/W	0h	Password for factory reset command - Word 5

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21 FACTORY_RESET_6 Register (Offset = 50h) [Reset = 00000000h]

FACTORY_RESET_6 is shown in Figure 5-23 and described in Table 5-25.

Return to the Summary Table.

Password for factory reset command - Word 6

Figure 5-23. FACTORY_RESET_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_6																															
R/W-0h																															

Table 5-46. FACTORY_RESET_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_6	R/W	0h	Password for factory reset command - Word 6

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22 FACTORY_RESET_7 Register (Offset = 54h) [Reset = 00000000h]

FACTORY_RESET_7 is shown in Figure 5-24 and described in Table 5-26.

Return to the Summary Table.

Password for factory reset command - Word 7

Figure 5-24. FACTORY_RESET_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FACTORY_RESET_7																															
R/W-0h																															

Table 5-48. FACTORY_RESET_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FACTORY_RESET_7	R/W	0h	Password for factory reset command - Word 7

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23 DEBUG_LOCK_0 Register (Offset = 58h) [Reset = 00000000h]

DEBUG_LOCK_0 is shown in Figure 5-25 and described in Table 5-27.

Return to the Summary Table.

Password for debug access authentication - Word 0

Figure 5-25. DEBUG_LOCK_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_0																															
R/W-0h																															

Table 5-50. DEBUG_LOCK_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_0	R/W	0h	Password for debug access authentication - Word 0

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24 DEBUG_LOCK_1 Register (Offset = 5Ch) [Reset = 00000000h]

DEBUG_LOCK_1 is shown in Figure 5-26 and described in Table 5-28.

Return to the Summary Table.

Password for debug access authentication - Word 1

Figure 5-26. DEBUG_LOCK_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_1																															
R/W-0h																															

Table 5-52. DEBUG_LOCK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_1	R/W	0h	Password for debug access authentication - Word 1

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25 DEBUG_LOCK_2 Register (Offset = 60h) [Reset = 00000000h]

DEBUG_LOCK_2 is shown in Figure 5-27 and described in Table 5-29.

Return to the Summary Table.

Password for debug access authentication - Word 2

Figure 5-27. DEBUG_LOCK_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_2																															
R/W-0h																															

Table 5-54. DEBUG_LOCK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_2	R/W	0h	Password for debug access authentication - Word 2

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26 DEBUG_LOCK_3 Register (Offset = 64h) [Reset = 00000000h]

DEBUG_LOCK_3 is shown in Figure 5-28 and described in Table 5-30.

Return to the Summary Table.

Password for debug access authentication - Word 3

Figure 5-28. DEBUG_LOCK_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_3																															
R/W-0h																															

Table 5-56. DEBUG_LOCK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_3	R/W	0h	Password for debug access authentication - Word 3

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27 DEBUG_LOCK_4 Register (Offset = 68h) [Reset = 00000000h]

DEBUG_LOCK_4 is shown in Figure 5-29 and described in Table 5-31.

Return to the Summary Table.

Password for debug access authentication - Word 4

Figure 5-29. DEBUG_LOCK_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_4																															
R/W-0h																															

Table 5-58. DEBUG_LOCK_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_4	R/W	0h	Password for debug access authentication - Word 4

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28 DEBUG_LOCK_5 Register (Offset = 6Ch) [Reset = 00000000h]

DEBUG_LOCK_5 is shown in Figure 5-30 and described in Table 5-32.

Return to the Summary Table.

Password for debug access authentication - Word 5

Figure 5-30. DEBUG_LOCK_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_5																															
R/W-0h																															

Table 5-60. DEBUG_LOCK_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_5	R/W	0h	Password for debug access authentication - Word 5

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29 DEBUG_LOCK_6 Register (Offset = 70h) [Reset = 00000000h]

DEBUG_LOCK_6 is shown in Figure 5-31 and described in Table 5-33.

Return to the Summary Table.

Password for debug access authentication - Word 6

Figure 5-31. DEBUG_LOCK_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_6																															
R/W-0h																															

Table 5-62. DEBUG_LOCK_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_6	R/W	0h	Password for debug access authentication - Word 6

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30 DEBUG_LOCK_7 Register (Offset = 74h) [Reset = 00000000h]

DEBUG_LOCK_7 is shown in Figure 5-32 and described in Table 5-34.

Return to the Summary Table.

Password for debug access authentication - Word 7

Figure 5-32. DEBUG_LOCK_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_LOCK_7																															
R/W-0h																															

Table 5-64. DEBUG_LOCK_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_LOCK_7	R/W	0h	Password for debug access authentication - Word 7

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31 DEBUG_NS_LOCK_0 Register (Offset = 78h) [Reset = 00000000h]

DEBUG_NS_LOCK_0 is shown in Figure 5-33 and described in Table 5-35.

Return to the Summary Table.

Password for non-secure debug access - Word 0

Figure 5-33. DEBUG_NS_LOCK_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_0																															
R/W-0h																															

Table 5-66. DEBUG_NS_LOCK_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_0	R/W	0h	Password for non-secure debug access - Word 0

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32 DEBUG_NS_LOCK_1 Register (Offset = 7Ch) [Reset = 00000000h]

DEBUG_NS_LOCK_1 is shown in Figure 5-34 and described in Table 5-36.

Return to the Summary Table.

Password for non-secure debug access - Word 1

Figure 5-34. DEBUG_NS_LOCK_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_1																															
R/W-0h																															

Table 5-68. DEBUG_NS_LOCK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_1	R/W	0h	Password for non-secure debug access - Word 1

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33 DEBUG_NS_LOCK_2 Register (Offset = 80h) [Reset = 00000000h]

DEBUG_NS_LOCK_2 is shown in Figure 5-35 and described in Table 5-37.

Return to the Summary Table.

Password for non-secure debug access - Word 2

Figure 5-35. DEBUG_NS_LOCK_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_2																															
R/W-0h																															

Table 5-70. DEBUG_NS_LOCK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_2	R/W	0h	Password for non-secure debug access - Word 2

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34 DEBUG_NS_LOCK_3 Register (Offset = 84h) [Reset = 00000000h]

DEBUG_NS_LOCK_3 is shown in Figure 5-36 and described in Table 5-38.

Return to the Summary Table.

Password for non-secure debug access - Word 3

Figure 5-36. DEBUG_NS_LOCK_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_3																															
R/W-0h																															

Table 5-72. DEBUG_NS_LOCK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_3	R/W	0h	Password for non-secure debug access - Word 3

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35 DEBUG_NS_LOCK_4 Register (Offset = 88h) [Reset = 00000000h]

DEBUG_NS_LOCK_4 is shown in Figure 5-37 and described in Table 5-39.

Return to the Summary Table.

Password for non-secure debug access - Word 4

Figure 5-37. DEBUG_NS_LOCK_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_4																															
R/W-0h																															

Table 5-74. DEBUG_NS_LOCK_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_4	R/W	0h	Password for non-secure debug access - Word 4

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36 DEBUG_NS_LOCK_5 Register (Offset = 8Ch) [Reset = 00000000h]

DEBUG_NS_LOCK_5 is shown in Figure 5-38 and described in Table 5-40.

Return to the Summary Table.

Password for non-secure debug access - Word 5

Figure 5-38. DEBUG_NS_LOCK_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_5																															
R/W-0h																															

Table 5-76. DEBUG_NS_LOCK_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_5	R/W	0h	Password for non-secure debug access - Word 5

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37 DEBUG_NS_LOCK_6 Register (Offset = 90h) [Reset = 00000000h]

DEBUG_NS_LOCK_6 is shown in Figure 5-39 and described in Table 5-41.

Return to the Summary Table.

Password for non-secure debug access - Word 6

Figure 5-39. DEBUG_NS_LOCK_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_6																															
R/W-0h																															

Table 5-78. DEBUG_NS_LOCK_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_6	R/W	0h	Password for non-secure debug access - Word 6

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38 DEBUG_NS_LOCK_7 Register (Offset = 94h) [Reset = 00000000h]

DEBUG_NS_LOCK_7 is shown in Figure 5-40 and described in Table 5-42.

Return to the Summary Table.

Password for non-secure debug access - Word 7

Figure 5-40. DEBUG_NS_LOCK_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_NS_LOCK_7																															
R/W-0h																															

Table 5-80. DEBUG_NS_LOCK_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_NS_LOCK_7	R/W	0h	Password for non-secure debug access - Word 7

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39 SECURE_BOOT_MODE Register (Offset = B8h) [Reset = 00000000h]

SECURE_BOOT_MODE is shown in Figure 5-41 and described in Table 5-43.

Return to the Summary Table.

Controls application authentication
Reserved field

Figure 5-41. SECURE_BOOT_MODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SECURE_BOOT_MODE															
R/W-0h																R/W-0h															

Table 5-82. SECURE_BOOT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	Reserved field
15-0	SECURE_BOOT_MODE	R/W	0h	Controls application authentication AABBh = BC_CFG_SECURE_BOOT_CRC_EN configuration FFFFh = DISABLED configuration

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40 USER_SECURE_APP_START_ADDR Register (Offset = BCh) [Reset = 00000000h]

USER_SECURE_APP_START_ADDR is shown in Figure 5-42 and described in Table 5-44.

Return to the Summary Table.

Starting address for secure application

Figure 5-42. USER_SECURE_APP_START_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_SECURE_APP_START_ADDR																															
R/W-0h																															

Table 5-84. USER_SECURE_APP_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	USER_SECURE_APP_START_ADDR	R/W	0h	Starting address for secure application

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41 USER_SECURE_APP_LENGTH Register (Offset = C0h) [Reset = 00000000h]

USER_SECURE_APP_LENGTH is shown in Figure 5-43 and described in Table 5-45.

Return to the Summary Table.

Length of secure application

Figure 5-43. USER_SECURE_APP_LENGTH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_SECURE_APP_LENGTH																															
R/W-0h																															

Table 5-86. USER_SECURE_APP_LENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	USER_SECURE_APP_LENGTH	R/W	0h	Length of secure application

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42 USER_SECURE_APP_CRC_0 Register (Offset = C4h) [Reset = 00000000h]

USER_SECURE_APP_CRC_0 is shown in Figure 5-44 and described in Table 5-46.

Return to the Summary Table.

Secure application CRC - Word 0

Figure 5-44. USER_SECURE_APP_CRC_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_SECURE_APP_CRC_0																															
R/W-0h																															

Table 5-88. USER_SECURE_APP_CRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	USER_SECURE_APP_CRC_0	R/W	0h	Secure application CRC - Word 0

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43 BANK0_NM_USER_CONFIG Register (Offset = E4h) [Reset = 00000000h]

BANK0_NM_USER_CONFIG is shown in Figure 5-45 and described in Table 5-47.

Return to the Summary Table.

User Config Non Main Flash Static Write Protection. WEP_DISABLE=0xAABB
Reserved field

Figure 5-45. BANK0_NM_USER_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_NM_USER_CONFIG															
R/W-0h															

Table 5-90. BANK0_NM_USER_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	Reserved field
15-0	BANK0_NM_USER_CONFIG	R/W	0h	User Config Non Main Flash Static Write Protection. WEP_DISABLE=0xAABB

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44 BANK0_WRITE_ERASE_PROTECTION_A Register (Offset = E8h) [Reset = 00000000h]

BANK0_WRITE_ERASE_PROTECTION_A is shown in Figure 5-46 and described in Table 5-48.

Return to the Summary Table.

Write protection for first 32 sectors

Figure 5-46. BANK0_WRITE_ERASE_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_WRITE_ERASE_PROTECTION_A																															
R/W-0h																															

Table 5-92. BANK0_WRITE_ERASE_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_WRITE_ERASE_PROTECTION_A	R/W	0h	Write protection for first 32 sectors

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45 BANK0_WRITE_ERASE_PROTECTION_B Register (Offset = ECh) [Reset = 00000000h]

BANK0_WRITE_ERASE_PROTECTION_B is shown in Figure 5-47 and described in Table 5-49.

Return to the Summary Table.

Write Protection for 512KB-64KB

Figure 5-47. BANK0_WRITE_ERASE_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_WRITE_ERASE_PROTECTION_B																															
R/W-0h																															

Table 5-94. BANK0_WRITE_ERASE_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_WRITE_ERASE_PROTECTION_B	R/W	0h	Write Protection for 512KB-64KB

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46 BANK0_SECURITY_PROTECTION_A Register (Offset = F0h) [Reset = 00000000h]

BANK0_SECURITY_PROTECTION_A is shown in Figure 5-48 and described in Table 5-50.

Return to the Summary Table.

Security protection for first 32 sectors

Figure 5-48. BANK0_SECURITY_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_SECURITY_PROTECTION_A																															
R/W-0h																															

Table 5-96. BANK0_SECURITY_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_SECURITY_PROTECTION_A	R/W	0h	Security protection for first 32 sectors

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47 BANK0_SECURITY_PROTECTION_B Register (Offset = F4h) [Reset = 00000000h]

BANK0_SECURITY_PROTECTION_B is shown in Figure 5-49 and described in Table 5-51.

Return to the Summary Table.

Security protection for 512KB-64KB

Figure 5-49. BANK0_SECURITY_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_SECURITY_PROTECTION_B																															
R/W-0h																															

Table 5-98. BANK0_SECURITY_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_SECURITY_PROTECTION_B	R/W	0h	Security protection for 512KB-64KB

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48 BANK0_PRIVILEGE_PROTECTION_A Register (Offset = F8h) [Reset = 00000000h]

BANK0_PRIVILEGE_PROTECTION_A is shown in Figure 5-50 and described in Table 5-52.

Return to the Summary Table.

Privilege protection for first 32 sectors

Figure 5-50. BANK0_PRIVILEGE_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_PRIVILEGE_PROTECTION_A																															
R/W-0h																															

Table 5-100. BANK0_PRIVILEGE_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_PRIVILEGE_PROTECTION_A	R/W	0h	Privilege protection for first 32 sectors

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49 BANK0_PRIVILEGE_PROTECTION_B Register (Offset = FCh) [Reset = 00000000h]

BANK0_PRIVILEGE_PROTECTION_B is shown in Figure 5-51 and described in Table 5-53.

Return to the Summary Table.

Privilege protection for 512KB-64KB

Figure 5-51. BANK0_PRIVILEGE_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK0_PRIVILEGE_PROTECTION_B																															
R/W-0h																															

Table 5-102. BANK0_PRIVILEGE_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK0_PRIVILEGE_PROTECTION_B	R/W	0h	Privilege protection for 512KB-64KB

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50 BANK1_WRITE_ERASE_PROTECTION_A Register (Offset = 104h) [Reset = 00000000h]

BANK1_WRITE_ERASE_PROTECTION_A is shown in Figure 5-52 and described in Table 5-54.

Return to the Summary Table.

Write protection for first 32 sectors

Figure 5-52. BANK1_WRITE_ERASE_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_WRITE_ERASE_PROTECTION_A																															
R/W-0h																															

Table 5-104. BANK1_WRITE_ERASE_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_WRITE_ERASE_PROTECTION_A	R/W	0h	Write protection for first 32 sectors

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51 BANK1_WRITE_ERASE_PROTECTION_B Register (Offset = 108h) [Reset = 00000000h]

BANK1_WRITE_ERASE_PROTECTION_B is shown in Figure 5-53 and described in Table 5-55.

Return to the Summary Table.

Write Protection for 512KB-64KB

Figure 5-53. BANK1_WRITE_ERASE_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_WRITE_ERASE_PROTECTION_B																															
R/W-0h																															

Table 5-106. BANK1_WRITE_ERASE_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_WRITE_ERASE_PROTECTION_B	R/W	0h	Write Protection for 512KB-64KB

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52 BANK1_SECURITY_PROTECTION_A Register (Offset = 10Ch) [Reset = 00000000h]

BANK1_SECURITY_PROTECTION_A is shown in Figure 5-54 and described in Table 5-56.

Return to the Summary Table.

Security protection for first 32 sectors

Figure 5-54. BANK1_SECURITY_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_SECURITY_PROTECTION_A																															
R/W-0h																															

Table 5-108. BANK1_SECURITY_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_SECURITY_PROTECTION_A	R/W	0h	Security protection for first 32 sectors

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53 BANK1_SECURITY_PROTECTION_B Register (Offset = 110h) [Reset = 00000000h]

BANK1_SECURITY_PROTECTION_B is shown in Figure 5-55 and described in Table 5-57.

Return to the Summary Table.

Security protection for 512KB-64KB

Figure 5-55. BANK1_SECURITY_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_SECURITY_PROTECTION_B																															
R/W-0h																															

Table 5-110. BANK1_SECURITY_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_SECURITY_PROTECTION_B	R/W	0h	Security protection for 512KB-64KB

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54 BANK1_PRIVILEGE_PROTECTION_A Register (Offset = 114h) [Reset = 00000000h]

BANK1_PRIVILEGE_PROTECTION_A is shown in Figure 5-56 and described in Table 5-58.

Return to the Summary Table.

Privilege protection for first 32 sectors

Figure 5-56. BANK1_PRIVILEGE_PROTECTION_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_PRIVILEGE_PROTECTION_A																															
R/W-0h																															

Table 5-112. BANK1_PRIVILEGE_PROTECTION_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_PRIVILEGE_PROTECTION_A	R/W	0h	Privilege protection for first 32 sectors

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55 BANK1_PRIVILEGE_PROTECTION_B Register (Offset = 118h) [Reset = 00000000h]

BANK1_PRIVILEGE_PROTECTION_B is shown in Figure 5-57 and described in Table 5-59.

Return to the Summary Table.

Privilege protection for 512KB-64KB

Figure 5-57. BANK1_PRIVILEGE_PROTECTION_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BANK1_PRIVILEGE_PROTECTION_B																															
R/W-0h																															

Table 5-114. BANK1_PRIVILEGE_PROTECTION_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BANK1_PRIVILEGE_PROTECTION_B	R/W	0h	Privilege protection for 512KB-64KB

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56 BOOTCLK0 Register (Offset = 130h) [Reset = 00000000h]

BOOTCLK0 is shown in Figure 5-58 and described in Table 5-60.

Return to the Summary Table.

Clock configuration
PLL multiplier value
PLL divider value
PLL clock source configuration

Figure 5-58. BOOTCLK0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYSPLL_SOURCE								SYSPLL_CONFIG_RDIV							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYSPLL_CONFIG_QDIV								SYSPLL_CONFIG							
R/W-0h								R/W-0h							

Table 5-116. BOOTCLK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SYSPLL_SOURCE	R/W	0h	PLL clock source configuration AAh = BC_CFG_PLL_SOURCE_XTAL_20MHZ configuration FFh = DEFAULT configuration
23-16	SYSPLL_CONFIG_RDIV	R/W	0h	PLL divider value
15-8	SYSPLL_CONFIG_QDIV	R/W	0h	PLL multiplier value
7-0	SYSPLL_CONFIG	R/W	0h	Clock configuration AAh = PLL_80 configuration BBh = PLL_CUSTOM configuration FFh = NOPLL configuration

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57 BOOTCLK1 Register (Offset = 134h) [Reset = 00000000h]

BOOTCLK1 is shown in Figure 5-59 and described in Table 5-61.

Return to the Summary Table.

CPU delay cycles for PLL settling time
CPU delay cycles for XTAL monitoring
Reserved configuration field 0

Figure 5-59. BOOTCLK1 Register

31	30	29	28	27	26	25	24
RESVD_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESVD_0							
R/W-0h							
15	14	13	12	11	10	9	8
XTAL_STARTUP_MONITOR_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
SYSPLL_SETTLING_TIME							
R/W-0h							

Table 5-118. BOOTCLK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESVD_0	R/W	0h	Reserved configuration field 0
15-8	XTAL_STARTUP_MONITOR_TIME	R/W	0h	CPU delay cycles for XTAL monitoring
7-0	SYSPLL_SETTLING_TIME	R/W	0h	CPU delay cycles for PLL settling time

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58 CRC Register (Offset = 14Ch) [Reset = 00000000h]

CRC is shown in Figure 5-60 and described in Table 5-62.

Return to the Summary Table.

JAMCRC of BCR config structure

Figure 5-60. CRC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC																															
R/W-0h																															

Table 5-120. CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRC	R/W	0h	CRC-32 of BCR config structure

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59 BSL_CONFIG_ID Register (Offset = 0h) [Reset = 00000000h]

BSL_CONFIG_ID is shown in Figure 5-61 and described in Table 5-63.

Return to the Summary Table.

Predetermined Bootloader config signature ID

Figure 5-61. BSL_CONFIG_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSL_CONFIG_ID																															
R/W-0h																															

Table 5-122. BSL_CONFIG_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BSL_CONFIG_ID	R/W	0h	Predetermined Bootloader config signature ID

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60 BSLPINCFG0 Register (Offset = 4h) [Reset = 00000000h]

BSLPINCFG0 is shown in Figure 5-62 and described in Table 5-64.

Return to the Summary Table.

UART receive pin number configuration
UART receive pin multiplexer selection
UART transmit pin number configuration
UART transmit pin multiplexer selection

Figure 5-62. BSLPINCFG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UART_TXD_PF_MUX_SEL								UART_TXD_PAD_NUM							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART_RXD_PF_MUX_SEL								UART_RXD_PAD_NUM							
R/W-0h								R/W-0h							

Table 5-124. BSLPINCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	UART_TXD_PF_MUX_SEL	R/W	0h	UART transmit pin multiplexer selection
23-16	UART_TXD_PAD_NUM	R/W	0h	UART transmit pin number configuration
15-8	UART_RXD_PF_MUX_SEL	R/W	0h	UART receive pin multiplexer selection
7-0	UART_RXD_PAD_NUM	R/W	0h	UART receive pin number configuration

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61 BSLPINCFG1 Register (Offset = 8h) [Reset = 00000000h]

BSLPINCFG1 is shown in Figure 5-63 and described in Table 5-65.

Return to the Summary Table.

I2C data pin number configuration
I2C data pin multiplexer selection
I2C clock pin number configuration
I2C clock pin multiplexer selection

Figure 5-63. BSLPINCFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I2C_SCL_PF_MUX_SEL								I2C_SCL_PAD_NUM							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_SDA_PF_MUX_SEL								I2C_SDA_PAD_NUM							
R/W-0h								R/W-0h							

Table 5-126. BSLPINCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	I2C_SCL_PF_MUX_SEL	R/W	0h	I2C clock pin multiplexer selection
23-16	I2C_SCL_PAD_NUM	R/W	0h	I2C clock pin number configuration
15-8	I2C_SDA_PF_MUX_SEL	R/W	0h	I2C data pin multiplexer selection
7-0	I2C_SDA_PAD_NUM	R/W	0h	I2C data pin number configuration

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62 BSLPINCFG2 Register (Offset = Ch) [Reset = 00000000h]

BSLPINCFG2 is shown in Figure 5-64 and described in Table 5-66.

Return to the Summary Table.

MCAN receive pin number configuration
MCAN receive pin multiplexer selection
MCAN transmit pin number configuration
MCAN transmit pin multiplexer selection

Figure 5-64. BSLPINCFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCAN_TX_PF_MUX_SEL								MCAN_TX_PAD_NUM							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCAN_RX_PF_MUX_SEL								MCAN_RX_PAD_NUM							
R/W-0h								R/W-0h							

Table 5-128. BSLPINCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MCAN_TX_PF_MUX_SEL	R/W	0h	MCAN transmit pin multiplexer selection
23-16	MCAN_TX_PAD_NUM	R/W	0h	MCAN transmit pin number configuration
15-8	MCAN_RX_PF_MUX_SEL	R/W	0h	MCAN receive pin multiplexer selection
7-0	MCAN_RX_PAD_NUM	R/W	0h	MCAN receive pin number configuration

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63 BSLCONFIG0 Register (Offset = 10h) [Reset = 00000000h]

BSLCONFIG0 is shown in Figure 5-65 and described in Table 5-67.

Return to the Summary Table.

BSL invoke pin configuration data 0
BSL invoke pin configuration data 1
Memory readout control. ENABLE allows memory read operations

Figure 5-65. BSLCONFIG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
READOUT															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN_DATA_1								PIN_DATA_0							
R/W-0h								R/W-0h							

Table 5-130. BSLCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	READOUT	R/W	0h	Memory readout control. ENABLE allows memory read operations
15-8	PIN_DATA_1	R/W	0h	BSL invoke pin configuration data 1
7-0	PIN_DATA_0	R/W	0h	BSL invoke pin configuration data 0

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64 PASSWORD_0 Register (Offset = 14h) [Reset = 00000000h]

PASSWORD_0 is shown in Figure 5-66 and described in Table 5-68.

Return to the Summary Table.

BSL access password - Word 0

Figure 5-66. PASSWORD_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_0																															
R/W-0h																															

Table 5-132. PASSWORD_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_0	R/W	0h	BSL access password - Word 0

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65 PASSWORD_1 Register (Offset = 18h) [Reset = 00000000h]

PASSWORD_1 is shown in Figure 5-67 and described in Table 5-69.

Return to the Summary Table.

BSL access password - Word 1

Figure 5-67. PASSWORD_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_1																															
R/W-0h																															

Table 5-134. PASSWORD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_1	R/W	0h	BSL access password - Word 1

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66 PASSWORD_2 Register (Offset = 1Ch) [Reset = 00000000h]

PASSWORD_2 is shown in Figure 5-68 and described in Table 5-70.

Return to the Summary Table.

BSL access password - Word 2

Figure 5-68. PASSWORD_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_2																															
R/W-0h																															

Table 5-136. PASSWORD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_2	R/W	0h	BSL access password - Word 2

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67 PASSWORD_3 Register (Offset = 20h) [Reset = 00000000h]

PASSWORD_3 is shown in Figure 5-69 and described in Table 5-71.

Return to the Summary Table.

BSL access password - Word 3

Figure 5-69. PASSWORD_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_3																															
R/W-0h																															

Table 5-138. PASSWORD_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_3	R/W	0h	BSL access password - Word 3

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68 PASSWORD_4 Register (Offset = 24h) [Reset = 00000000h]

PASSWORD_4 is shown in Figure 5-70 and described in Table 5-72.

Return to the Summary Table.

BSL access password - Word 4

Figure 5-70. PASSWORD_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_4																															
R/W-0h																															

Table 5-140. PASSWORD_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_4	R/W	0h	BSL access password - Word 4

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69 PASSWORD_5 Register (Offset = 28h) [Reset = 00000000h]

PASSWORD_5 is shown in Figure 5-71 and described in Table 5-73.

Return to the Summary Table.

BSL access password - Word 5

Figure 5-71. PASSWORD_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_5																															
R/W-0h																															

Table 5-142. PASSWORD_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_5	R/W	0h	BSL access password - Word 5

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70 PASSWORD_6 Register (Offset = 2Ch) [Reset = 00000000h]

PASSWORD_6 is shown in Figure 5-72 and described in Table 5-74.

Return to the Summary Table.

BSL access password - Word 6

Figure 5-72. PASSWORD_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_6																															
R/W-0h																															

Table 5-144. PASSWORD_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_6	R/W	0h	BSL access password - Word 6

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71 PASSWORD_7 Register (Offset = 30h) [Reset = 00000000h]

PASSWORD_7 is shown in Figure 5-73 and described in Table 5-75.

Return to the Summary Table.

BSL access password - Word 7

Figure 5-73. PASSWORD_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PASSWORD_7																															
R/W-0h																															

Table 5-146. PASSWORD_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PASSWORD_7	R/W	0h	BSL access password - Word 7

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72 APP_REV_POINTER Register (Offset = 34h) [Reset = 00000000h]

APP_REV_POINTER is shown in Figure 5-74 and described in Table 5-76.

Return to the Summary Table.

Pointer to application version information in MAIN flash

Figure 5-74. APP_REV_POINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APP_REV_POINTER																															
R/W-0h																															

Table 5-148. APP_REV_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	APP_REV_POINTER	R/W	0h	Pointer to application version information in MAIN flash

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73 BSLCONFIG1 Register (Offset = 38h) [Reset = 00000000h]

BSLCONFIG1 is shown in Figure 5-75 and described in Table 5-77.

Return to the Summary Table.

Security alert response: Factory Reset/Disable BSL/Ignore
UART communication speed selection for ROM BSL

Figure 5-75. BSLCONFIG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UART_BAUD_RATE															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECURITY_ALERT_LEVEL															
R/W-0h															

Table 5-150. BSLCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UART_BAUD_RATE	R/W	0h	UART communication speed selection for ROM BSL 1h = BAUDRATE_4800 configuration 2h = BAUDRATE_9600 configuration 3h = BAUDRATE_19200 configuration 4h = BAUDRATE_38400 configuration 5h = BAUDRATE_57600 configuration 6h = BAUDRATE_115200 configuration 7h = BAUDRATE_1000000 configuration 8h = BAUDRATE_2000000 configuration 9h = BAUDRATE_3000000 configuration
15-0	SECURITY_ALERT_LEVEL	R/W	0h	Security alert response: Factory Reset/Disable BSL/Ignore AABBh = FACTORY_RESET configuration CCDDh = DISABLE_BSL configuration FFFFh = DO_NOTHING configuration

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74 I2C_SLAVE_ADDR Register (Offset = 3Ch) [Reset = 00000000h]

I2C_SLAVE_ADDR is shown in Figure 5-76 and described in Table 5-78.

Return to the Summary Table.

I2C slave address for ROM BSL I2C interface
Reserved field
Reserved field

Figure 5-76. I2C_SLAVE_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED								I2C_SLAVE_ADDR															
R/W-0h								R/W-0h								R/W-0h															

Table 5-152. I2C_SLAVE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	Reserved field
23-16	RESERVED	R/W	0h	Reserved field
15-0	I2C_SLAVE_ADDR	R/W	0h	I2C slave address for ROM BSL I2C interface

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Chapter 6

Trigonometric Math Unit (TMU)

This chapter describes the trigonometric math unit (TMU) .

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6.3 Functional Operation.....322
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6.1 Introduction

The Trigonometric Math Unit (TMU) is a floating-point hardware accelerator that uses the Custom Datapath Extension (CDE) interface of the Arm® Cortex-M33 core to reduce the effective MIPS of the M33 core by enabling faster trigonometric math function calculations. The trigonometric math functions are supported as an enhanced instruction set on the M33 core that utilizes the M33 core's Floating Point Unit (FPU) registers for the operands and the data path implemented on the CDE interface.

In many sensing and control algorithms, common math operations such as Sine, Cosine, Arctangent, Division, and Square Root take many cyces to complete in a software-only implementation. The TMU hardware accelerator significantly reduces cycle times, and thus increases the achievable control frequencies of a system by adding custom instructions specifcally for these operations to the M33 CPU.

6.2 Features

- TMU functions implemented as native Cortex-M33 instructions
- Utilizes Custom Datapath Extension (CDE) interface of the M33 CPU
- M33 FPU registers used to store operands, data path is implemented outside of FPU
- M33 TMU32 operations supported:
  - SINPUF32
  - COSPUF32
  - ATANPUF32
  - DIVF32
  - QUADF32
  - SQRTF32
  - IEXP2F32
  - LOG2F32
  - ISQRTF32
- RSCTFLT instruction to read/write Latched Underflow (LUF) and Latched Overflow (LVF) flags
- External interface for LUF/LVF interrupts and ROM parity error
- Safety enabled through parity protection for ROM
- No pipelining of back to back instructions inside the CDE TMU - M33 CPU expected to issue new instruction after the result is given for the previous instruction
- Interruptible multicycle instructions
- Kill signal terminates current instruction in the M33 CDE module. The kill signal is generated when the M33 CPU encounters an interrupt while executing a CDE or FPCDE instruction.

Note

Multiple LUF/LCF interrupts could be generated due to a kill signal being asserted.

The AM13E232x SDK enables TMU usage in software. Refer to the SDK for examples using the TMU.

6.3 Functional Operation

6.3.1 Supported TMU Instructions

The following mathematical operations are supported on the M33 CDE TMU accelerator:

Table 6-1. M33 CDE TMU Instructions

Instruction	Description	# of Inputs	# of Outputs	Equivalent Operation	# of M33 Cycles
SINPUF32	Returns the SINE of input value	1 : Sm	1: Sd	sin(Sm * 2pi rad) Sm = -1.0 to 1.0	5
COSPUF32	Returns the COSINE of input value	1 : Sm	1 : Sd	cos(Sm * 2pi rad) Sm = -1.0 to 1.0	5

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Table 6-1. M33 CDE TMU Instructions (continued)

Instruction	Description	# of Inputs	# of Outputs	Equivalent Operation	# of M33 Cycles
ATANPUF32	Returns the ARCTAN of input value	1 : Sm	1: Sd	arctan(Sm) rad/2pi Sm = -1.0 to 1.0 Sd = -0.125 to 0.125	5
DIVF32	Returns the DIV value of two input values	2 : Sn = X, Sm = Y	1: Sd = (X / Y)	Sn / Sm	6
QUADF32	Returns the quadrant value of the (X,Y) input values	2 : Sn = X, Sm = Y	1 : Sd	Quadrant(X,Y)	1
SQRTF32	Returns the Square Root of input value	1 : Sm	1 : Sd	sqrt(Sm)	6
IEXP2F32	Returns the Inverse Exponent of input value. **Note** There is loss of accuracy with increased values of the exponent. Refer to the software example test cases in the SDK for more details.	1 : Sm	1 : Sd	$1 / (2^{Sm})$	5
LOG2F32	Returns the Base-2 Logarithm of input value	1 : Sm	1 : Sd	$Log_2(Sm)$	6
ISQRTF32	Returns the Inverse Square Root of input value	1 : Sm	1 : Sd	1 / sqrt(Sm)	6
RSCTFLG	Read/Set/Clear the LUF and/or LVF flags that are maintained inside the TMU CDE **Note** For a **flag read only** instruction, keep Rm[1:0]=00 **Note** The default value of the LUV and LVF flags at reset are 0.	2: Rn : 2-bit write value (Rn[0] - LUF, Rn[1]-LVF) Rm : 2-bit mask (Rm[0] - LUF, Rm[1] - LVF)	1 : Rd 2-bit read value (Rd[0] - LUF, Rd[1] - LVF)	**Operation** • LUF = (LUF & ~Rm[0]) | (Rn[0] & Rm[0]) • LVF = (LVF & ~RM[1]) | (Rn[1] & Rm[1]) • Rd[0] = LUF • Rd[1] = LVF **Examples** • Read both flags • Set both flags • Clear both flags • Set LUF only • Set LVF only • Clear LUF only • Clear LVF only	1

- Sd: Destination Register (floating-point)
- Sn: Source Register (floating-point)
- Sm: Source Register (floating-point)
- Rd: Destination Register (general-purpose)
- Rn: Source register (general-purpose)
- Rm: Source register (general-purpose)

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6.4 TMU Interrupts & Triggers

6.4.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 6-2. CPU Interrupts Triggered by TMU

NVIC Interrupt Name	Peripheral Instance Name	Register Group	TMU Interrupt Configuration Registers	Description
TMU_LUF_INT	N/A - not a peripheral	N/A	N/A	TMU latched underflow CPU interrupt. Single source condition.
TMU_LVF_INT	N/A - not a peripheral	N/A	N/A	TMU latched overflow CPU interrupt. Single source condition.

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Chapter 7

TinyEngine™ Neural Processing Unit (NPU)

This chapter describes the features and operation of the TinyEngine™ Neural Processing Unit (NPU), used to improve the efficiency of machine learning inferencing.

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7.2 NPU Interrupts & Triggers.....326

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7.1 Introduction

The TinyEngine™ NPU can support intelligent inferencing running pre-trained models. Capable of 800–1600MOPS(Mega Operations Per Second) with example model support for ARC fault detection or Motor Fault detection, the TinyEngine™ NPUprovides up to 10x Neural Network (NN) inferencing cycle improvement versus a software only based implementation. Load and train models with tools from TI: Model Composer GUI or TI's command-line Modelmaker tool for an advanced set of capabilities. Both of these options automatically generate source code for the ARM® Cortex® -M33 , eliminating the need to manually write code.

Figure 7-1 shows the toolchain and steps to add TinyEngine™ NPU support to a project, starting with importing or using existing models from TI, training the models, generating the associated software libraries, and integrating into an existing Code Composer Studio™ IDE project.

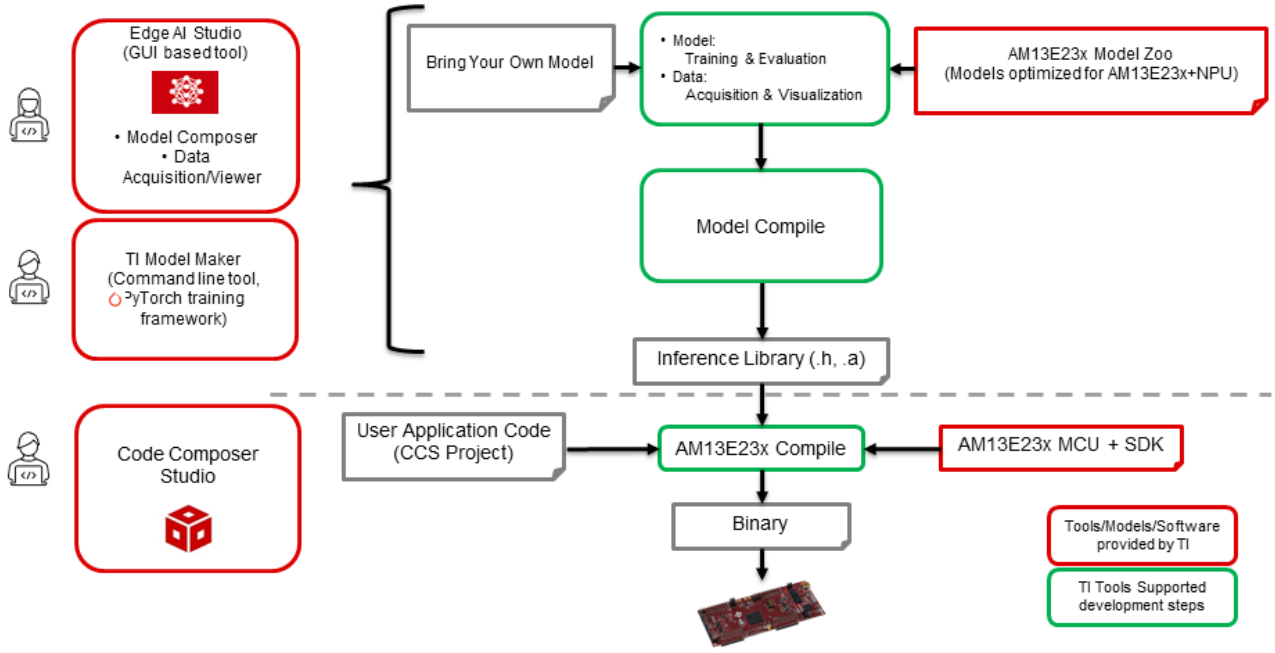


Figure 7-1. TinyEngine™ NPUDevelopment Flow

7.2 NPU Interrupts & Triggers

7.2.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 7-1. CPU Interrupts Triggered by NPU

NVIC Interrupt Name	Peripheral Instance Name	Register Group	NPU Interrupt Configuration Registers	Description
NPU	N/A	N/A	N/A - NPU-level registers are not intended for user configuration. Configurations are generated by Edge AI application.	NPU interrupt: TinyEngine NPU has completed running a model. Single, non-configurable source condition.

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7.2.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 7-2. DMA Triggers from the NPU

Trigger Name	Peripheral Instance Name	Register Group	NPU DMA Configuration Registers	Description
NPU	N/A	N/A	N/A - NPU-level registers are not intended for user configuration. Configurations are generated by Edge AI application.	NPU interrupt: TinyEngine NPU has completed running a model. Single, non-configurable source condition.

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Chapter 8

Advanced Encryption Standard (AES) Accelerator

The AESA accelerator module accelerates encryption and decryption operations in hardware based on the FIPS PUB 197 advanced encryption standard (AES).

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8.2 AESADV Operation 330
8.3 AES Interrupts & Triggers 349
8.4 AES Registers 349

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8.1 AES Overview

The AES accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware. AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AES accelerator features include:

- AES 128-bit block encryption and decryption
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- AES-CCM
- AES-GCM
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AES ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the *Operating Modes* section of the device technical reference manual)

A high level block diagram of the AES engine is shown in Figure 8-1. The AES engine consists of a processing core that performs both encryption/decryption as well as Galois field multiplication. The core is driven with configuration and data inputs that software will configure via memory mapped registers.

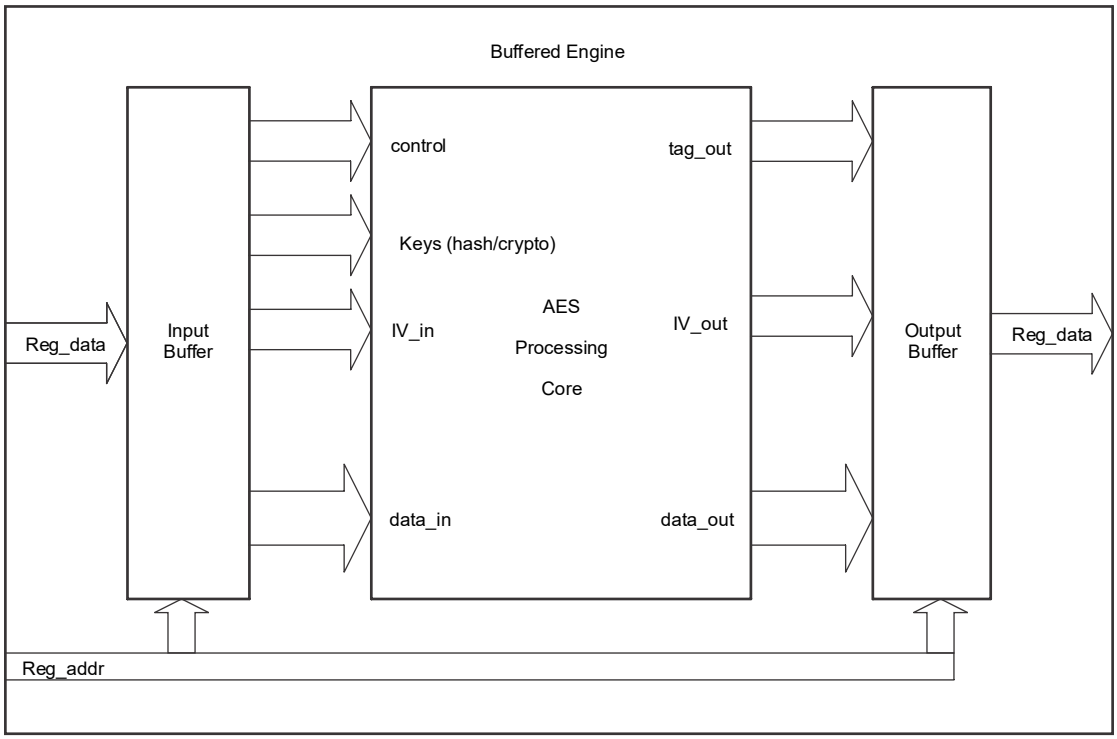


Figure 8-1. AES Block Diagram

8.1.1 AESADV Performance

The AESADV accelerator provides fast encryption and decryption of 128-bit blocks. AESADV accelerator performance in both cycles and execution time for block encryption and block decryption (with pregenerated decryption key) is given in Section 8.1 . This table assumes that there are no system overheads (delays in supplying next input or reading out available output) that stall the engine.

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Table 8-1. AESADV Hardware Accelerator Key Performance Metrics

AESADV Key Length	Encryption			Decryption		
	Cycles	Time (32MHz)	Time (100MHz)	Cycles	Time (32MHz)	Time (100MHz)
128-bit	76	2.38us	0.76us	76	2.38us	0.76us
256-bit	81	2.53us	0.81us	81	2.53us	0.81us

8.2 AESADV Operation

The AESADV engine provides an efficient implementation of the Rijndael cipher (the AES algorithm) and a 128-bit polynomial multiplication (referred here to as 'GHASH', as per the AES-GCM specification). Rijndael is a block cipher with each data block consisting of 128-bits.

AES encryption requires a specific number of rounds depending on the key length. Supported key lengths are 128-bit, and 256 bit, requiring 10, and 14 rounds respectively.

The AESADV engine contains the AES ECB core and a dedicated 32-cycle polynomial multiplication module for performing GHASH operations (when GCM is configured). The polynomial multiplication operates in parallel with the AES core, if there is data available for both modules. This is the case after encryption of the first data block.

8.2.1 Loading the Key

Keys can be configured into the engine in one of two ways.

1. Secure key initialization via keystore controller: In this method, the intended AES key is securely transferred from the keystore controller into the engine via a secure private bus connecting the keystore controller and the AES engine. The keystore controller initiates the key transfer and waits for the AES engine to acknowledge transfer completion.
2. Software explicitly configures keys: In this method, software configures the key data into the engine by writing to the KEY0--KEY7 registers, writing 32-bits at a time starting with KEY0. For 128-bit keys, KEY0--KEY3 register will need to be written. For 256-bit keys, KEY0--KEY7 will need to be written.

In order to prevent key stealing attacks by partial modification method, the engine ensures that once a secure key transfer has completed via the keystore, software can no longer explicitly configure/modify the key. This status is provided by the STATUS.KEYWR field. If this field is 0, then software is allowed to write key data. If this field is 1, then software is not allowed to write key data. In order to allow software to write key data, the module has to be reset. The reset operation clears existing key data before new key data can be written by software.

8.2.2 Writing Input Data

Input data is written into the engine either through the DATA0, DATA1, DATA2, and DATA3 registers or through the DATA_IN register. If DMA is not being used to automate the input/output transfers (DMA_HS is 0), then CPU software can perform the 128-bit data input by writing 32-bit data to each of the registers DATA0, DATA1, DATA2 and DATA3 in sequence.

If DMA is being used to automate the input/output transfers (DMA_HS is 1), then the DMA channel that is associated with DMA Trigger 0 event must be configured to perform four 32-bit writes to the DATA_IN register.

8.2.3 Reading Output Data

Output data is read from the engine either via the DATA0/1/2/3 registers or via the DATA_OUT register. If DMA is not being used to automate the input/output transfers (DMA_HS is 0), then CPU software can read out the 128-bit data output by reading 32-bit data from each of DATA0, DATA1, DATA2 and DATA3 registers in sequence.

If DMA is being used to automate the input/output transfers (DMA_HS is 1), then the DMA channel that is associated with DMA Trigger 1 event will need to be configured to perform 4 32-bit reads from the DATA_OUT register.

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8.2.4 Operation Descriptions

Both single block and block cipher mode operations are configured by writing the appropriate context to the AESADV registers. Independently, the input and output data can be transferred via CPU software or via DMA.

Block cipher modes are used to implement the ECB, CBC, OFB, and CFB block cipher modes using AES as the underlying block cipher. These modes work together with the DMA using the DMA triggers to support easy and fast encryption or decryption of more than 128 bits.

8.2.4.1 Single Block Operation

A single 128-bit block of data can be encrypted or decrypted by first configuring the context registers and then initiating input data transfer. The following pseudo code describes the actions that are typically executed by CPU software for a basic encryption operation with 128-bit key.

```
wait AES_CTRL.CNTXT_RDY == '1' // wait for CNTXT_RDY to become 1
wait AES_CTRL.INPUT_RDY == '10' // wait for INPUT_RDY to become 1
write AES_KEY0 // first 32 bits of key
write AES_KEY1 // next 32 bits of key
write AES_KEY2 // next 32 bits of key
write AES_KEY3 // final 32 bits of key
write AES_CTRL.SAVE_CNTXT == '0' // clear AES save context
write AES_CTRL.KEYSIZE == '01' // Write AES 128 bit mode
write AES_CTRL.DIR == '1'      //Write AES encrypt mode
write AES_DATA0 // write 32-bit data LSW to supply 128-bit block
write AES_DATA1 // write 32-bit data (LSW + 1) to supply 128-bit block
write AES_DATA2 // write 32-bit data (LSW + 2) to supply 128-bit block
write AES_DATA3 // write 32-bit data MSW to supply 128-bit block
wait AES_CTRL.OUTPUT_RDY == '1' // wait for OUTPUT_RDY to become 1
read AES_DATA0 // read 32-bit data LSW to read out 128-bit encrypted data
read AES_DATA1 // read 32-bit data (LSW + 1) to read out 128-bit encrypted data
read AES_DATA2 // read 32-bit data (LSW + 2) to read out 128-bit encrypted data
read AES_DATA3 // read 32-bit data MSW to read out 128-bit encrypted data
```

8.2.4.2 Electronic Codebook (ECB) Mode

The electronic codebook (ECB) cipher is the simplest block cipher mode. The plaintext data is divided into 128-bit blocks, and each block is encrypted and decrypted independently from any other block. The ECB cipher is shown in Figure 8-2. Note that each 128-bit data block can be encrypted or decrypted individually without any knowledge of the other blocks of plaintext or ciphertext.

While ECB is simple to understand and implement, it has a key disadvantage: the same 128-bit plaintext block is always encrypted into the same ciphertext block, allowing patterns in the ciphertext to be detected.

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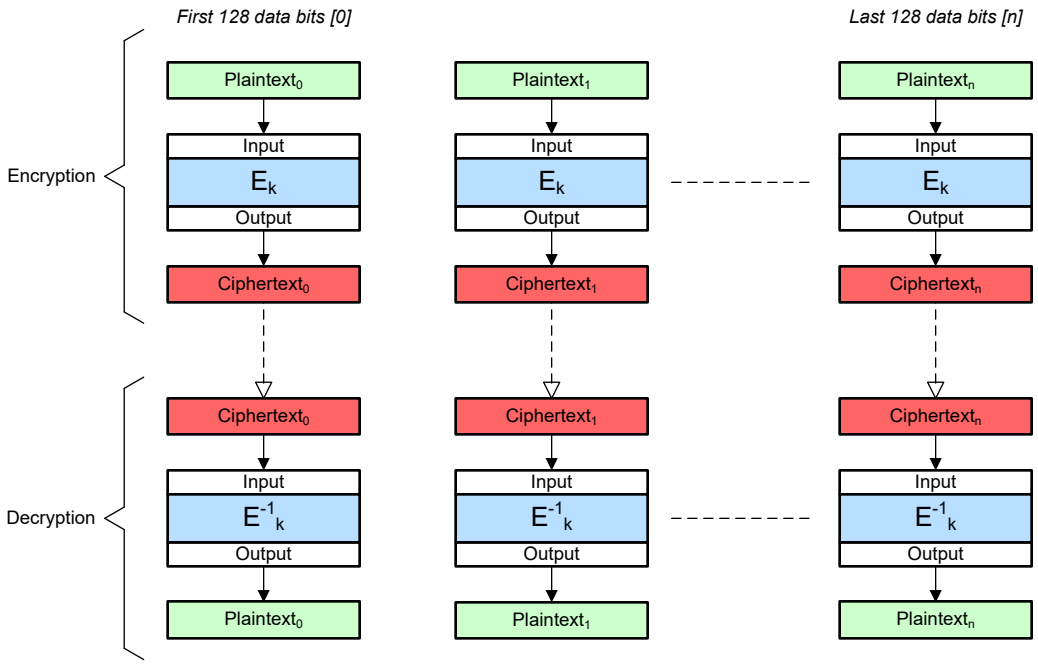


Figure 8-2. ECB Cipher

The AESADV accelerator supports automated encryption and decryption of more than 128 bits of data in ECB block cipher mode either through interrupts or through the use of DMA. Software interrupt-based multi-block handling uses the AESADV interrupt condition reported in the CPU_INT.IIDX.STAT field. If this field reads 0x2 (INPUTRDY), then the next block of input can be written (as 4 32-bit writes to DATA0/1/2/3). If this field reads 0x1 (OUTPUTRDY), then the output block can be read (as 4 32-bit reads from DATA0/1/2/3).

In DMA mode, ECB uses two DMA channels. Channel bound to DMA_TRIG0 is the input channel. Channel bound to DMA_TRIG1 is the output channel. The channels need to be configured to perform one 32-bit read/write per trigger.

8.2.4.2.1 ECB Encryption

ECB mode encryption of *N* blocks of plaintext into *N* blocks of ciphertext without CPU interaction is achieved through the use of 2 DMA channels (referred to as DMA_A and DMA_B). To implement ECB encryption follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AESADV event registers, unmask Trig1 in the IMASK register of DMA_TRIG1
2. Configure Input DMA channel for loading plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1

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5. Configure the CTRL register for block cipher encryption mode for ECB:
   a. Set key size in CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select ECB mode by setting rest of the bits in CTRL to 0
6. Load key as described in Section 8.2.1 .
7. Start encryption by writing the number of bytes *N×4* to AES C_LENGTH_0 and C_LENGTH_1 registers
8. Wait for the DMA channel interrupt which indicates completion of the entire operation. The ciphertext output will be stored in the location configured in step 1c.

8.2.4.2.2 ECB Decryption

ECB Mode Decryption configuration is nearly identical to ECB Mode Encryption. The only difference is that the direction bit (CTRL.DIR) has to be set to 0.

8.2.4.3 Cipher Block Chaining (CBC) Mode

The cipher block chaining (CBC) cipher mode builds upon the ECB cipher mode to make the ciphertext output for each block dependent not only on the plaintext and the cipher key *k*, but also upon the ciphertext of the previous block. The CBC cipher is shown in Figure 8-3. Like ECB mode, the plaintext data is divided into 128-bit blocks. Unlike ECB mode, in CBC mode each new plaintext block is bit-wise XORed with the previous ciphertext block to create the input to the AES block cipher.

In CBC mode, an unpredictable initialization vector (IV) must be provided. The initialization vector is XORed with the first plaintext block, as there is no "previous" ciphertext block to XOR the first plaintext block with.

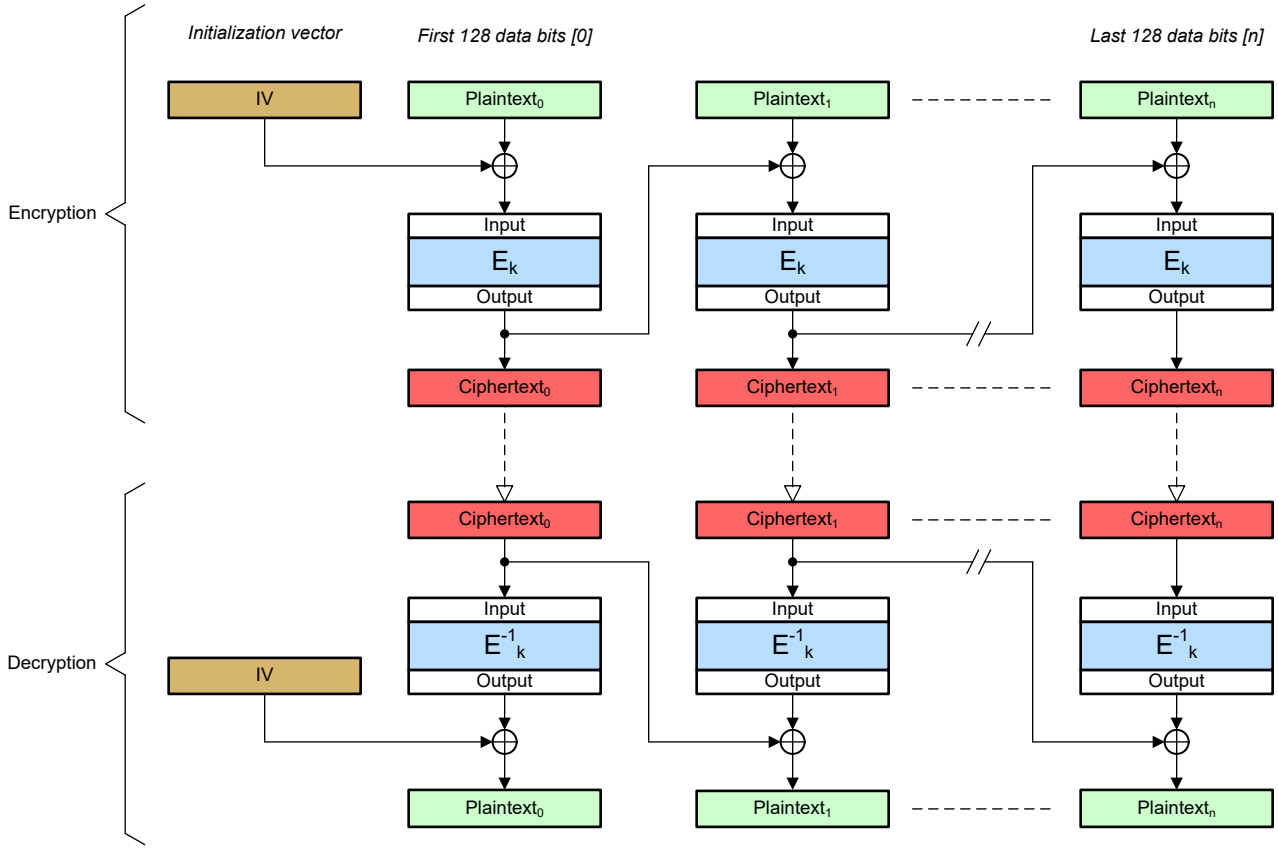


Figure 8-3. CBC Cipher

The AESADV accelerator supports automated CBC mode operation of more than 128 bits of data either through interrupts or through the use of DMA. Software interrupt-based multi-block handling uses the AES interrupt

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condition reported in the CPU_INT.IIDX.STAT field. If this field reads 0x2 (INPUTRDY), then the next block of input can be written (as 4 32-bit writes). If this field reads 0x1 (OUTPUTRDY), then the output block can be read (as 4 32-bit reads).

In DMA mode, CBC utilizes two DMA channels. Channel bound to DMA_TRIG0 is the input channel. Channel bound to DMA_TRIG1 is the output channel. The channels need to be configured to perform one 32-bit read/write per trigger.

8.2.4.3.1 CBC Encryption

CBC mode encryption of *N* blocks of plaintext into *N* blocks of ciphertext without CPU interaction is achieved through the use of 2 DMA channels. To implement CBC encryption follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG1
2. Configure Input DMA channel for loading plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load key as described in Section 8.2.1
6. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers
7. Configure the CTRL register for block cipher encryption mode for CBC
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select CBC mode by setting CTRL[CBC]=1
8. Start encryption by writing the number of bytes N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
9. Wait for the DMA channel interrupt that indicates completion of the entire operation. The ciphertext output is stored in the location configured in step 1c.

8.2.4.3.2 CBC Decryption

CBC-mode decryption is nearly identical to CBC-mode encryption setup, with the exception of configuring CTRL[DIR] = 0 for decryption.

8.2.4.4 Output Feedback (OFB) Mode

The output feedback mode leverages an initialization vector (IV) to generate a keystream by repeatedly encrypting the IV with the cipher key. The output ciphertext is obtained by XORing plaintext with the encrypted and re-encrypted versions of the initialization vector. The OFB cipher is shown in Figure 8-4.

In OFB mode, the initialization vector must be a nonce (number used once). To prevent loss of confidentiality, each IV must only be used one time with a given key, and any value passed into the cipher E_k for a given key k must not be used as an initialization vector with the same key k.

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Note

As OFB is a stream cipher, the AES block function is used in the forward (encryption) mode when performing OFB encryption or OFB decryption. When decrypting, the keystream is simply regenerated again to be XORed with the ciphertext, giving back the plaintext.

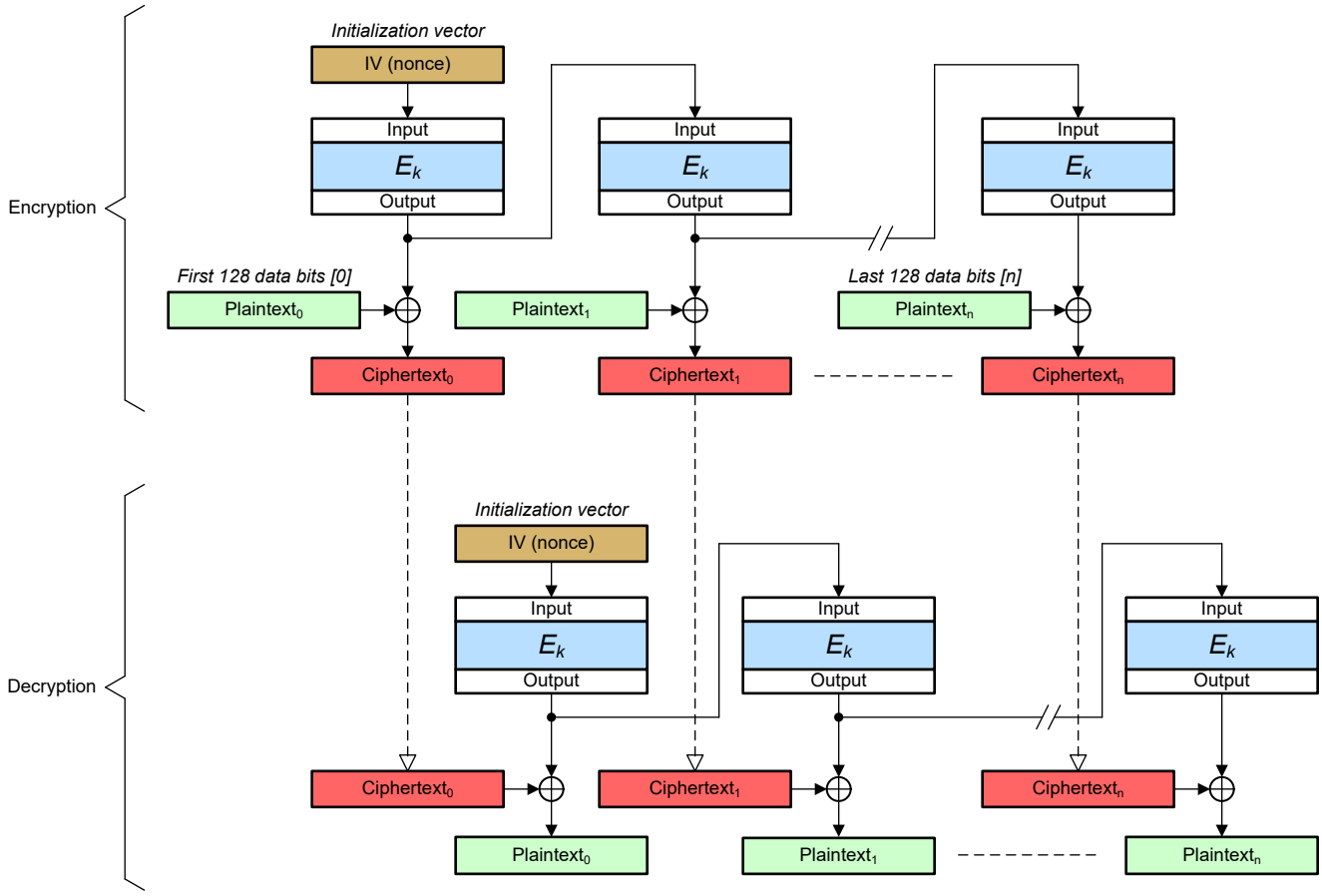


Figure 8-4. OFB Cipher

The AES accelerator supports automated OFB mode operation of more than 128 bits of data either through interrupts or through the use of DMA. Software interrupt-based multi-block handling uses the AES interrupt condition reported in the CPU_INT.IIDX.STAT field. If this field reads 0x2 (INPUTRDY), then the next block of input can be written (as 4 32-bit writes). If this field reads 0x1 (OUTPUTRDY), then the output block can be read (as 4 32-bit reads).

In DMA mode, OFB utilizes two DMA channels. Channel bound to DMA_TRIG0 is the input channel. Channel bound to DMA_TRIG1 is the output channel. The channels need to be configured to perform one 32-bit read/write per trigger.

8.2.4.4.1 OFB Encryption

OFB mode encryption of *N* blocks of plaintext into *N* blocks of ciphertext without CPU interaction is achieved through the use of 2 DMA channels. To implement OFB encryption follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N*∗4

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e. Set DMA channel mode to single transfer mode
f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG_DATAOUT

2. Configure Input DMA channel for loading plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *N**4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load key as described in Section 8.2.1
6. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers
7. Configure the CTRL register for block cipher encryption mode for OFB
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select OFB mode by setting CTRL[OFB_GCM_CCM_CONT]=1
8. Start encryption by writing number of bytes N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
9. Wait for the DMA channel interrupt which indicates completion of the entire operation. The ciphertext output will be stored in the location configured in step 1c.

Note

OFB_GCM_CCM_CONT bit has dual use. When CCM/GCM modes are not selected, then this bit serves to select OFB mode.

8.2.4.4.2 OFB Decryption

OFB-mode decryption is nearly identical to OFB-mode encryption setup, with the exception of configuring CTRL[DIR] = 0 for decryption.

8.2.4.5 Cipher Feedback (CFB) Mode

The cipher feedback (CFB) mode is similar to the output feedback (OFB) mode, with the key difference being that the input block to the block cipher *E* used to generate the key stream is taken from the previous ciphertext block (after being XORed with the plaintext), vs. taken before being XORed with the plaintext (as in the case of OFB). As a result, the keystream is dependent upon the plaintext, which is not true of OFB. The CFB cipher is shown in Figure 8-5.

Like OFB, CFB requires an initialization vector (IV). In CFB mode, the initialization vector (IV) must be unpredictable.

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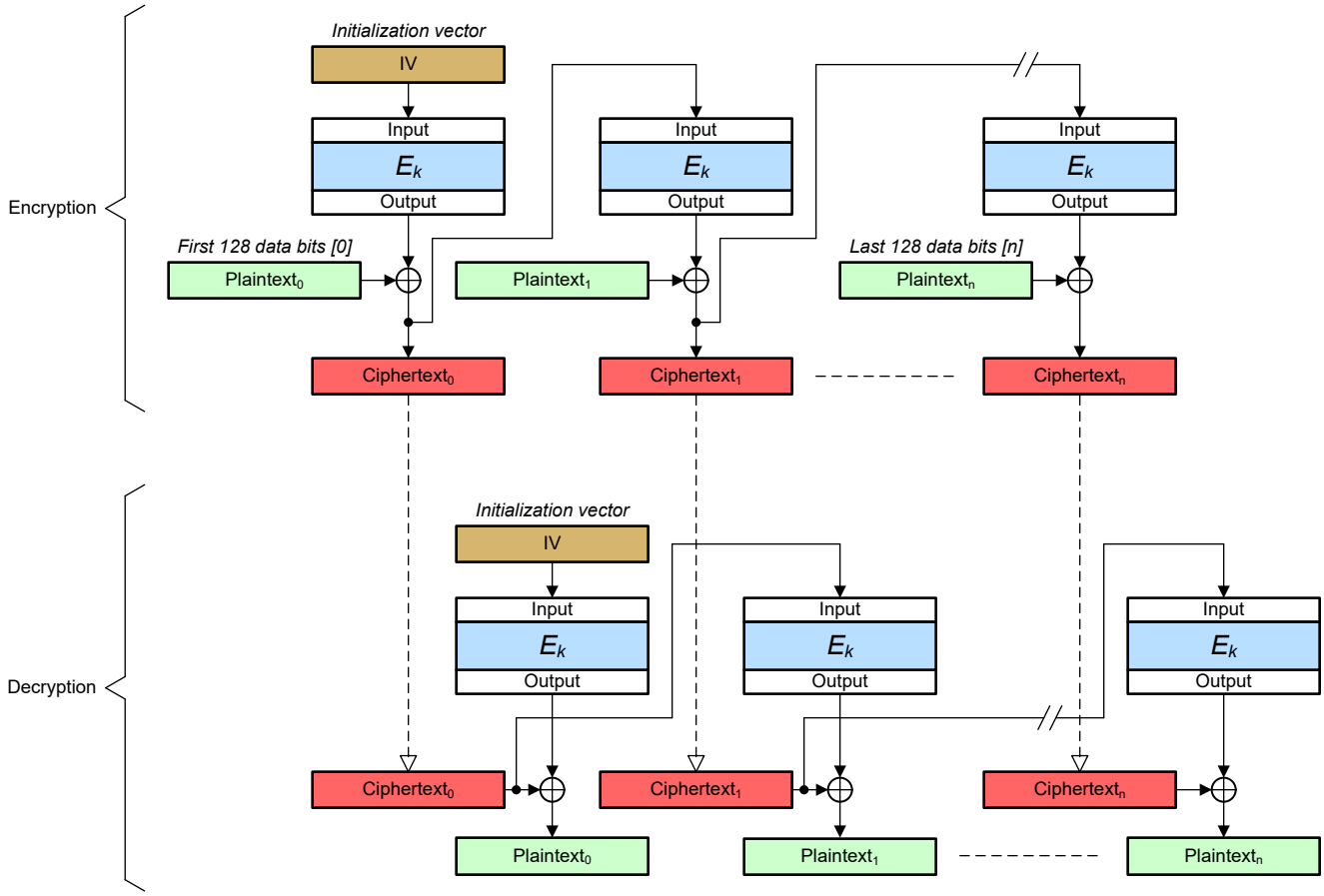


Figure 8-5. CFB Cipher

The AESADV accelerator supports automated CFB mode operation of more than 128 bits of data either through interrupts or through the use of DMA. Software interrupt-based multi-block handling uses the AES interrupt condition reported in the CPU_INT.IIDX.STAT field. If this field reads 0x2 (INPUTRDY), then the next block of input can be written (as 4 32-bit writes). If this field reads 0x1 (OUTPUTRDY), then the output block can be read (as 4 32-bit reads).

In DMA mode, CFB utilizes two DMA channels. Channel bound to DMA_TRIG_DATAIN is the input channel. Channel bound to DMA_TRIG_DATAOUT is the output channel. The channels need to be configured to perform one 32-bit read/write per trigger.

8.2.4.5.1 CFB Encryption

CFB mode encryption of *N* blocks of plaintext into *N* blocks of ciphertext without CPU interaction is achieved through the use of 2 DMA channels. To implement CFB encryption follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG_DATAOUT
2. Configure Input DMA channel for loading plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN

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d. Set DMA channel transfer size to *N**4
e. Set DMA channel mode to single transfer mode
f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0

3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load key as described in Section 8.2.1
6. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers
7. Configure the CTRL register for block cipher encryption mode for CFB
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select CFB mode by setting CTRL[CFB]=1
   d. Select feedback width by setting CTRL[CTR_WIDTH]
      i. 00b - CFB-128
      ii. 01b - CFB-1
      iii. 10b - CFB-8
8. Start encryption by writing number of bytes N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
9. Wait for the DMA channel interrupt that indicates completion of the entire operation. The ciphertext output is stored in the location configured in step 1c.

8.2.4.5.2 CFB Decryption

CFB-mode decryption is nearly identical to CFB-mode encryption setup, with the exception of configuring CTRL[DIR] = 0 for decryption.

8.2.4.6 Counter (CTR) Mode

The counter mode leverages a nonce (number used once) and a counting integer to generate a keystream by appending the counter to the nonce and encrypting the combined nonce || counter value with the cipher key.

The nonce must only be used once with a given key *k*. The counter value can start from any value and is incremented for each 128-bit block of data.

The keystream is derived be encrypting the nonce || counter value for each 128-bit data block with the cipher key *k*. The output ciphertext is then obtained by XORing the plaintext with the encrypted nonce || counter value for each data block. The CTR cipher is shown in Figure 8-6.

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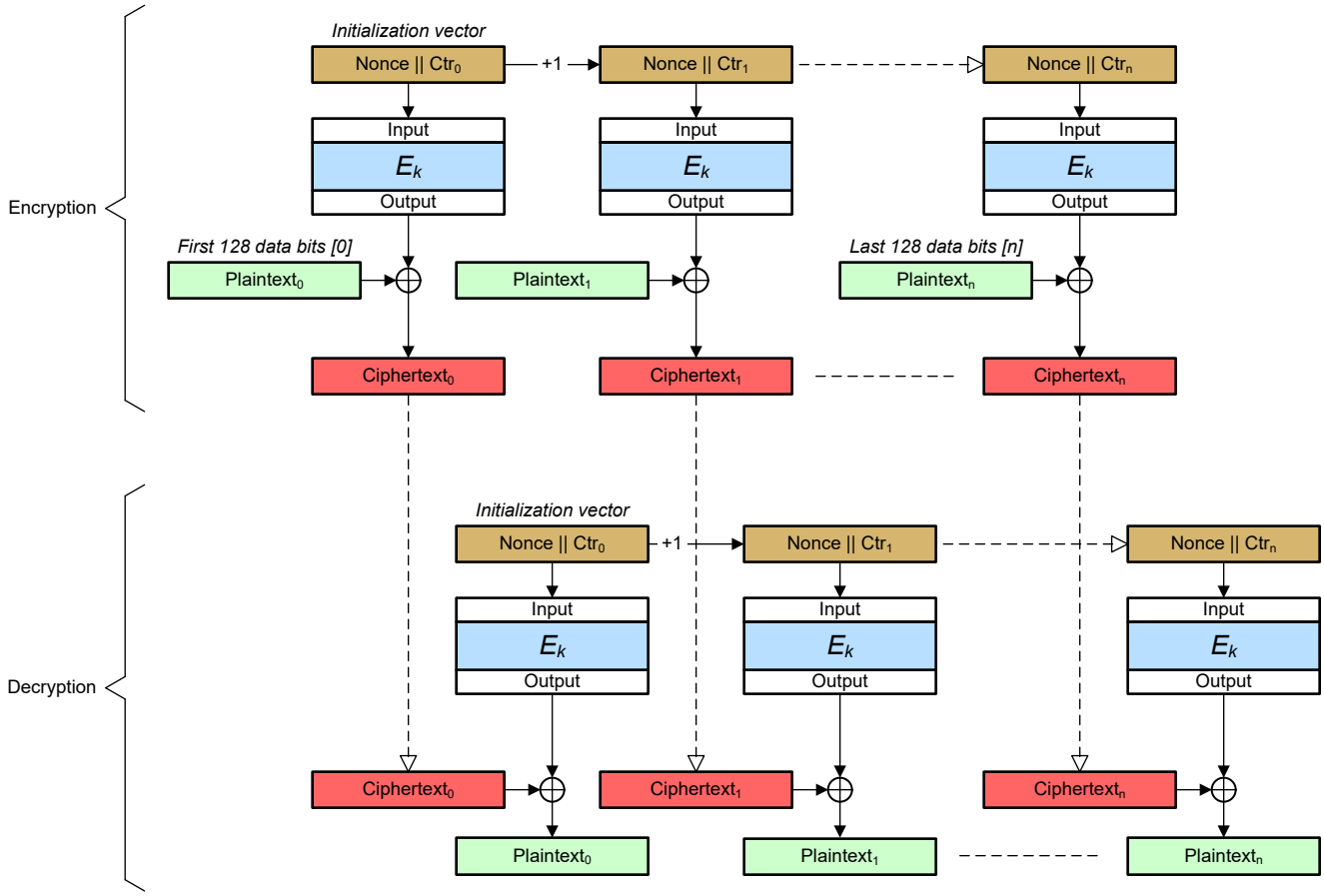


Figure 8-6. CTR Cipher

The AES accelerator implements logic and storage for incrementing and storing nonce || counter from one block to the next.

8.2.4.6.1 CTR Encryption

CTR mode encryption of *N* blocks of plaintext into *N* blocks of ciphertext without CPU interaction is achieved through the use of 2 DMA channels. To implement CTR encryption follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG_DATAOUT
2. Configure Input DMA channel for loading plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *N*∗4
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load key as described in Section 8.2.1

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6. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers
7. Configure the CTRL register for block cipher encryption mode for CTR
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select CTR mode by setting CTRL[CTR]=1
   d. Select CTR width by setting CTRL[CTR_WIDTH]
      i. 00b -CTR32
      ii. 01b -CTR64
      iii. 10b -CTR96
      iv. 11b -CTR128
8. Start encryption by writing number of bytes N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
9. Wait for the DMA channel interrupt which indicates completion of the entire operation. The ciphertext output will be stored in the location configured in step 1c.

8.2.4.6.2 CTR Decryption

CTR-mode decryption is nearly identical to CTR-mode encryption setup, with the exception of configuring CTRL[DIR] = 0 for decryption.

8.2.4.7 Galois Counter (GCM) Mode

A GCM protocol operation is a combined operation, consisting of encryption/decryption and authentication. Figure 8-7 illustrates an overview of the GCM operation.

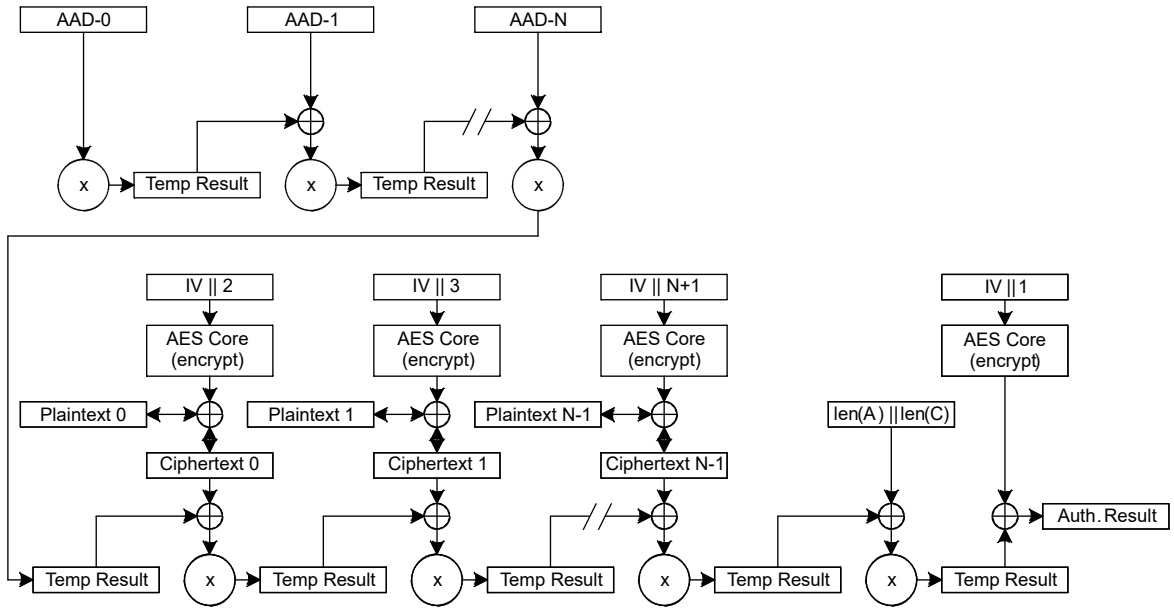


Figure 8-7. GCM Protocol Operation

A part of the input data stream can be authenticated only, while normally most of the input data is encrypted/decrypted and authenticated. The authentication only data always needs to be in front of the data that requires encryption. Within GCM, the authentication only data is called the AAD (Additional Authentication Data). The AAD is fetched independently of the other data.

The intermediate (temp) result data is used as input for the remaining authentication operation. Since the authentication operation does not require the encryption core but only the polynomial multiplication, both encryption/decryption and authentication are performed in parallel. After encryption of the last data block, an additional polynomial multiplication and encryption are required to respectively authenticate a 128-bit length vector and finally encrypt the authentication result.

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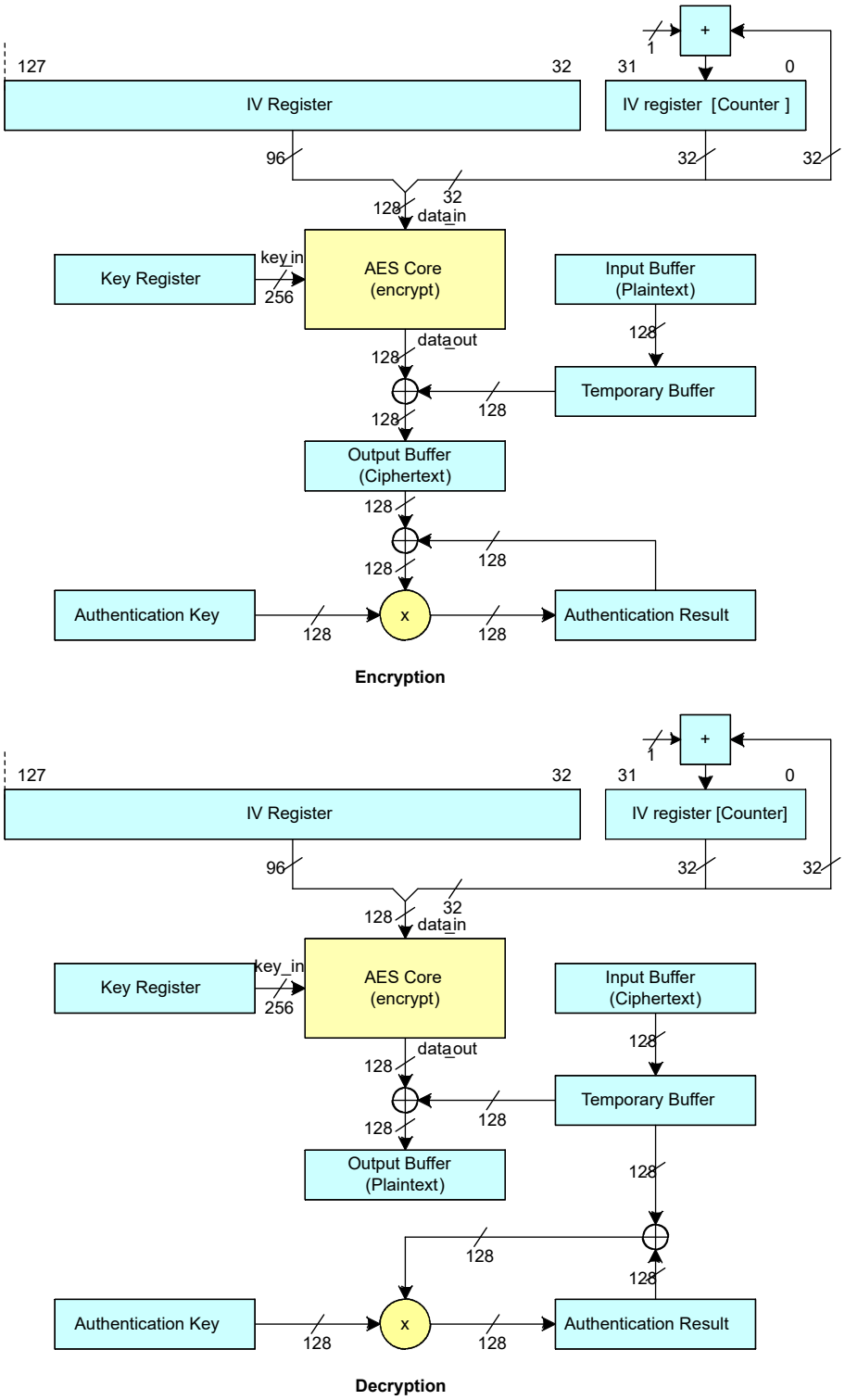


Figure 8-8. GCM Operation on a Block

GMAC operations, as specified in [NIST-SP800-38D], are also supported via the GCM operation. GMAC is a special use of GCM where no crypto data is processed and only AAD data is provided to produce a MAC of the input data. The crypto data length is set to zero for this case.

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Figure 8-8 illustrates the operations performed in one round. In one round of a GCM operation for both encryption and decryption, a 32-bit counter is used as IV (as it is for CTR mode). The data is encrypted the same way as CTR mode, by XOR-ing the crypto output with the input. After the encryption/decryption, the ciphertext is XOR-ed with the intermediate authentication result. The XOR-ed result is used as input for the polynomial multiplication to create the next (intermediate) authentication result.

8.2.4.7.1 GHASH Operation

For GHASH operations, the engine performs a modular polynomial multiplication in the GF(2128) field. The result is XOR-ed with the encrypted GCM initialization vector (referred to as 'Y0-encrypted'). Y0-encrypted is only relevant when the engine is performing a complete GCM operation, therefore in other modes the value of Y0-encrypted is forced to zero.

Also, for GCM mode only, the GCM 'Hash key' or 'H' input can be pre-calculated and supplied to the engine directly, or it can be calculated by the engine internally, by encrypting the value '0', using the encryption key.

8.2.4.7.2 GCM Operating Modes

For GCM three cases need to be distinguished.

- The first one is Autonomous GCM Mode where both H and Y0-encrypted are calculated internally. This mode requires that a 128-bit Y0 be provided to the core via the IV together with the mode.

  Note

  GCM mode bits must be set to 2'b11.

- The second case is the scenario where H is pre-calculated and Y0 still needs to be encrypted by the engine on a per packet basis. This can be useful when multiple packets use the same AES-key. Since H is constant for all packets using the same key, a pre-calculation saves cycles for each packet using that key. H can simply be calculated by performing a basic AES-ECB encryption with the AES-key and a data block containing all zeros or more formally: H=E(K, {}). Once H is calculated, it can be loaded with the control data every time a packet is processed that requires the same AES-key.

  Note

  GCM mode bits must be set to 2'b10.

- In the last case, neither H nor Y0-encrypted are calculated by the core. In this case, Y0-encrypted is forced to zeros, such that the hash result is not encrypted but provided plain via the TAG output registers. This scenario can be selected if a hash (GHASH) only operation needs to be performed. A scenario where this setting can be used is GCM IV-truncation. The GCM specification [GCM] allows an IV that has a length other than 96-bits. In this case, a basic GHASH operation needs to be performed to calculate a 128-bit Y0. For a basic GHASH operation, H needs to be pre-calculated (as explained in the previous paragraph). If H is available, the GHASH operation is similar to that of a general GCM operation with H pre-calculated, only the crypto input data will not be encrypted or decrypted.

  Note

  In the default case a 96-bit IV is combined with a 32-bit counter to create a 128-bit Y0 (meaning: Y0 = {IV||031||1}).

  Note

  GCM mode bits must be set to 2'b01.

8.2.4.7.2.1 Autonomous GCM Operation

In this mode, the engine calculates H and Y0-encrypted internally. At the high-level, the programming involves these steps:

- Provide GCM context (key, IV, lengths and mode).
- Provide AAD data (and wait for calculation of H and encryption of Y0).

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- Provide next AAD data.
- Provide last AAD data.
- Provide first crypto data.
- Provide next crypto data.
- Read result data and provide next crypto data.
- ...
- Read result data and provide last crypto data.
- Read result data.
- Read result data.
- Read authentication result (TAG).

To implement GCM encryption over N blocks of plaintext and M blocks of AAD, follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N×4*
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG_DATAOUT
2. Configure Input DMA channel for loading AAD and plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *(N+M)*4*
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load Encryption/Decryption key as described in Section 8.2.1
6. Load GCMCCM_TAGn (0,1,2,3) registers with 0s.
7. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers
8. Configure the CTRL register for block cipher encryption mode for GCM
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select GCM mode by setting CTRL[GCM] = 3
   d. Select CTR mode by setting CTRL[CTR] = 1
   e. Enable saving of TAG by setting CTRL[SAVE_CNTXT] = 1
9. Write encryption/decryption byte count N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
10. Write authentication data (AAD) byte count M*4 to AES AAD_LENGTH register
11. Wait for the DMA output channel interrupt to indicate completion of the entire operation. The output is stored started at the location configured in step 1c.
12. Read out the final TAG from the TAG0, TAG1, TAG2, TAG3 registers
13. GCM Continued Operation:
    a. SW guidelines for suspend resume operation of GCM through DMA:
       i. Before suspending the GCM operation (before writing to the GET_DIGEST bit in CTRL register) stop the DMA transfer
       ii. After stopping the DMA transfer, request for the GET_DIGEST
       iii. Read all required fields - note where the DMA transfer is halted
       iv. Use the above information as input to the engine before the resume operation starts
    b. SW guidelines for saved context ready interrupt:

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i. Poll the RIS register continuously for SAVEDCNTXTRDY status instead of waiting for interrupt

Note

The AAD and cryptographic data can end misaligned. The CPU must pad both to a 128-bit boundary with zeroes. More formally, the AAD and crypto data padding must satisfy the bit string: 0n, with 0 <= n <= 127. This means that the AAD must be provided as separate blocks to the engine, such that the cryptographic data starts 128-bit aligned. If the AAD/cryptographic data stream is 128-bit aligned no padding is required. Because the engine only supports bytes, n must be such that (n MOD 8) = 0. Further, because a single DMA channel supplies both AAD and plaintext, the entire data must be organized contiguously in memory with the first M blocks of AAD followed by N blocks of plaintext. This memory contiguity restriction is not applicable when CPU software directly provides inputs via interrupt handling.

Do not load both length values with zeroes. If a data stream is done and the next data stream uses the same key and control, only the IV and length values need be re-loaded.

8.2.4.7.2.1.1 GMAC

GMAC is a special case of GCM wherein there is no payload (N=0). AES C_LENGTH_0 and C_LENGTH_1 registers are set to 0 in this case.

8.2.4.7.2.2 GCM With Pre-Calculations

Pre-calculation of H:

1. Provide AES-ECB context (key and mode)
2. Provide zeros as data
3. Read result data (H)

IV truncation/pre-calculation (GHASH only operation):

- Provide GHASH context (H, lengths and mode)

Note

GHASH only: Y0-encrypted forced to zero, H loaded, and no crypto mode selected

1. Provide IV-data-block
2. Provide next IV-data-block
3. Read dummy result and provide next IV-data-block
4. ...
5. Read dummy result data and provide last IV-data-block
6. Read dummy result data
7. Read dummy result data
8. Read authentication result (TAG... this data is Y0)

GCM operation with pre-calculated H:

1. Provide GCM context (key, Y0 as IV, H, lengths and mode)
2. Provide AAD data (and wait for encryption of Y0)
3. Provide next AAD data
4. Provide last AAD data
5. Provide first crypto data
6. Provide next crypto data
7. Read result data and provide next crypto data
8. ...
9. Read result data and provide last crypto data
10. Read result data

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11. Read result data
12. Read authentication result (TAG)

For GCM with pre-calculated H, select GCM mode by setting CTRL[GCM] = 2

8.2.4.7.2.3 GCM Operation With Precalculated H- and Y0-Encrypted Forced to Zero

The outline of operations is listed below:

1. Provide GCM context (key, H, lengths and mode)
2. Provide AAD data
3. Provide next AAD data
4. Provide last AAD data
5. Provide first crypto data
6. Provide next crypto data
7. Read result data and provide next crypto data
8. ...
9. Read result data and provide last crypto data
10. Read result data
11. Read result data
12. Read plaintext authentication result

8.2.4.8 Counter With Cipher Block Chaining Message Authentication Code (CCM)

The CCM (Counter with CBC-MAC) protocol operation is a combined operation, consisting of encryption/decryption and authentication. Both the authentication and encryption/decryption operations use the crypto core; these are executed sequentially on the AES core. A part of the data stream can require authentication only. The authentication only data always needs to be in front of the data that requires encryption.

Figure 8-9 illustrates the CCM protocol. The authentication starts with the encryption of a pre-defined block B0. This block consists of flags, nonce and message length. The next blocks contain the authentication data length concatenated with the authentication only data. After processing the authentication only data, the encryption/decryption operations are performed, each followed by the related authentication of the plaintext data block (which equals the input in the case of encryption and the output in the case of decryption). The final authentication result needs to be encrypted using the output of the encryption of the IV block A0. This block contains the IV (consisting of flags and nonce) concatenated with the counter, which is zero for A0.

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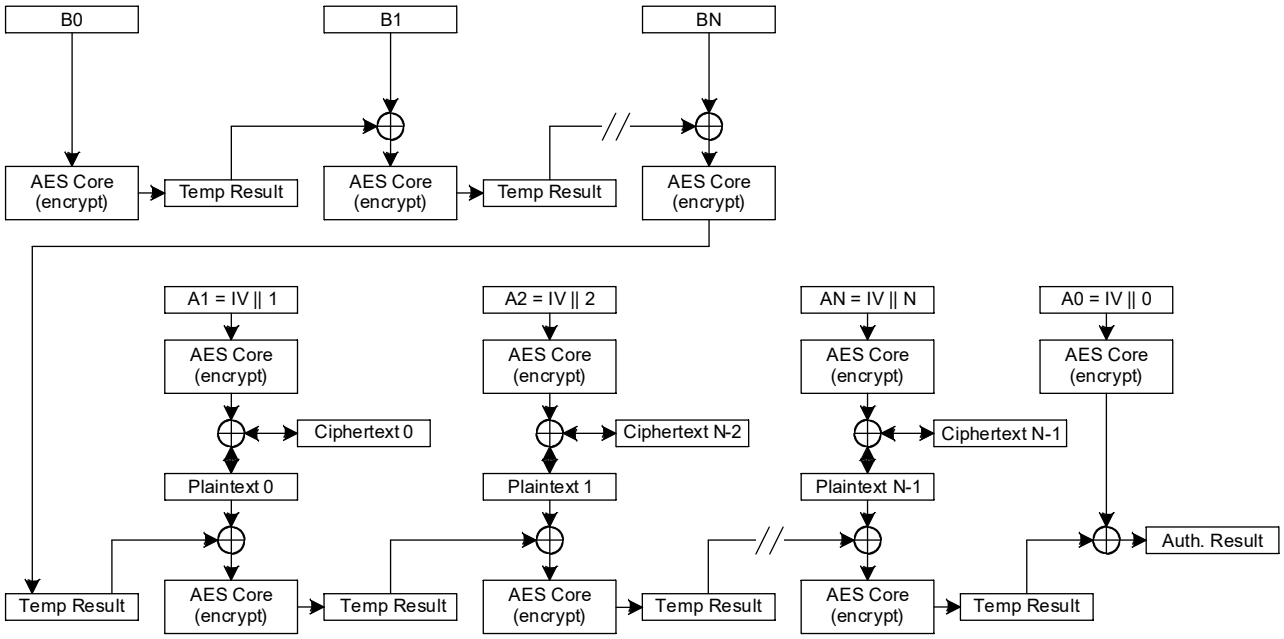


Figure 8-9. CCM Protocol Operation

Figure 8-10 shows one round of a CCM operation for both encryption and decryption. A 32-bit counter is used as IV (as it is for CTR mode). The data is encrypted in the same way as CTR mode, by XOR-ing the crypto core output with the input. Directly after the encrypt-operation, the plaintext is XOR-ed with the intermediate authentication result. The XOR result is used as input for a second encrypt-operation to calculate the next (intermediate) authentication result.

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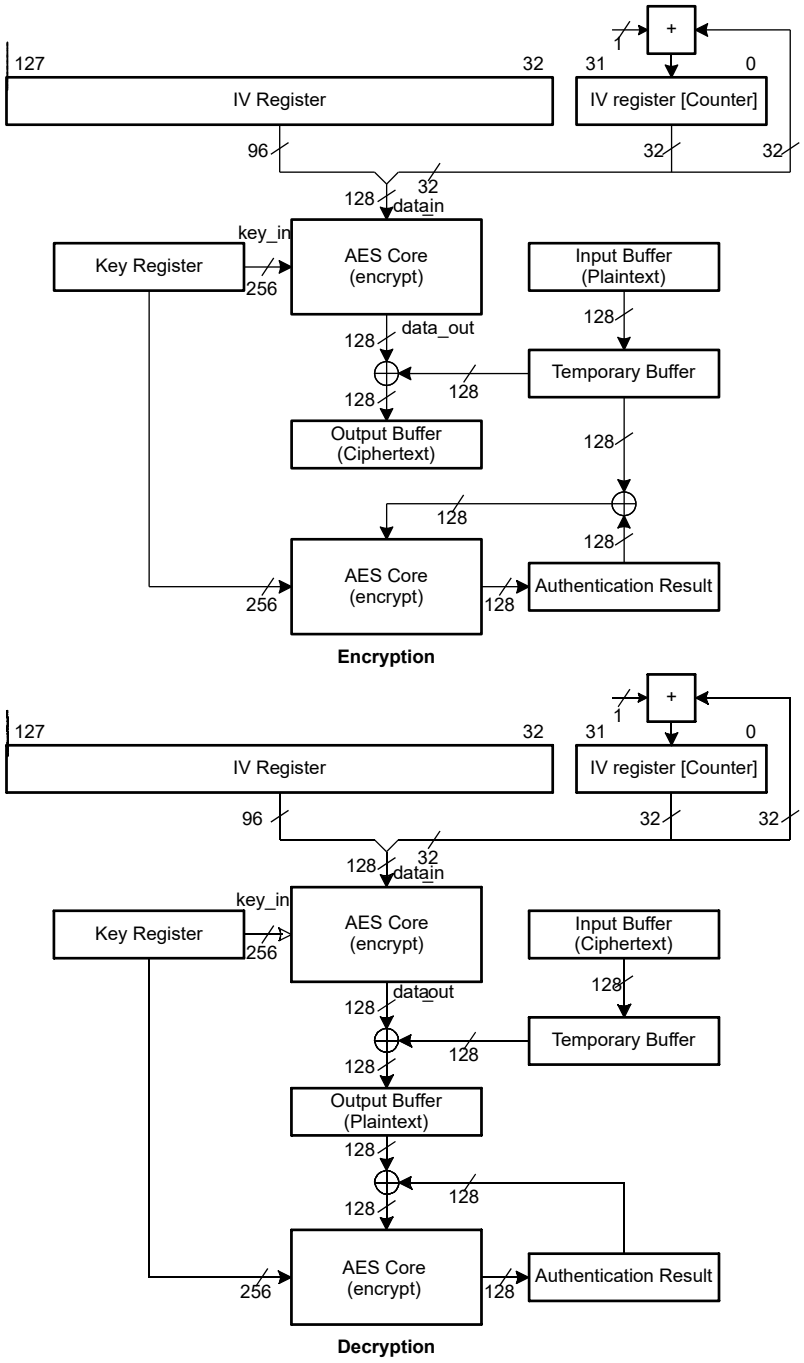


Figure 8-10. CCM Operation

8.2.4.8.1 CCM Operation

At the high-level, CCM operation is performed in the following sequence:

- Provide CCM context (key, IV including flags, lengths and mode)
- Provide hash only data
- Provide next hash only data
- Provide last hash only data
- Provide first crypto data
- Provide next crypto data

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- Read result data and provide next crypto data
- ...
- Read result data and provide last crypto data
- Read result data
- Read result data
- Read authentication result (TAG)

The read/write of data can be managed via DMA or by CPU software.

To implement CCM encryption over N blocks of plaintext and M blocks of AAD, follow these steps:

1. Configure Output DMA channel for saving ciphertext:
   a. Set DMA channel trigger selection to AES Trig1
   b. Set DMA channel source address to DATA_OUT
   c. Set DMA channel destination address to location where ciphertext is to be stored (for example, SRAM)
   d. Set DMA channel transfer size to *N×4*
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig1 in the IMASK register of DMA_TRIG_DATAOUT
2. Configure Input DMA channel for loading AAD and plaintext:
   a. Set DMA channel trigger selection to AES Trig0
   b. Set DMA channel source address to location where plaintext is stored (for example, SRAM)
   c. Set DMA channel destination address to DATA_IN
   d. Set DMA channel transfer size to *(N+M)*4*
   e. Set DMA channel mode to single transfer mode
   f. In the AES event registers, unmask Trig0 in the IMASK register of DMA_TRIG0
3. Configure and enable the DMA interrupt for the Output DMA channel in the DMA controller
4. Configure DMA_HS for DMA based handshake: set DMA_HS[DMA_DATA_ACK] = 1
5. Load Encryption/Decryption key as described in Section 8.2.1
6. Load Initialization vector (IV) by writing to IV0, IV1, IV2 and IV3 registers (must contain the flags for the cryptographic operation and the NONCE bytes, for both authentication and encryption)
7. Configure the CTRL register for block cipher encryption mode for CCM
   a. Select key size via CTRL[KEY_SIZ]
   b. Select Direction for Encryption by CTRL[DIR] = 1
   c. Select CCM mode by setting CTRL[CCM] = 1
   d. Select CTR mode by setting CTRL[CTR] =

      1
   e. Enabke saving of TAG by setting CTRL[SAVE_CNTXT] = 1
   f. Configure CTRL[CCML] -- CCM-L can be set to any value, representing a crypto data length field of CCML plus one Bytes.
   g. Configure CTRL[CTR_WIDTH] -- Note: CCM-L sets the actual counter field width in the IV register for CCM operations, in the range from 2 (CCM-L = 1) up to and including 8 (CCM-L = 7) Bytes. The actual counter width chosen with the CTR_WIDTH must be long enough to cover this field. The counter field width must be chosen so that the counter cannot overflow.
   h. Configure CTRL[CCMM] -- CCM-M can be set to any value and has no effect on the actual processing (other than being present in the special ‘B0’ block that is encrypted at the start of the operation). The CPU must select the valid TAG bytes from the 128-bit TAG (which are in the least significant 2 * (CCMM + 1) Bytes).
8. Write encryption/decryption byte count N×4 to AES C_LENGTH_0 and C_LENGTH_1 registers
9. Write authentication data (AAD) byte count M*4 to AES AAD_LENGTH register
10. Wait for the DMA output channel interrupt that indicates completion of the entire operation. The output is stored started at the location configured in step 1c.
11. Read out the final TAG from the TAG0/1/2/3 registers

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Note

The AAD and cryptographic data can end misaligned. The CPU must pad both to a 128-bit boundary with zeroes. More formally, the AAD and crypto data padding must satisfy the bit string: 0n, with 0<= n <= 127. This means that the AAD must be provided as separate blocks to the engine, such that the cryptographic data starts 128-bit aligned. If the AAD/cryptographic data stream is 128-bit aligned, no padding is required. Because the engine only supports bytes, n must be such that (n MOD 8) = 0. Further, since a single DMA channel is used to supply both AAD and plaintext, the entire data must be organized contiguously in memory with the first M blocks of AAD followed by N blocks of plaintext. This memory contiguity restriction is not applicable when CPU software directly provides inputs via interrupt handling.

Do not write both length values with zeroes. If a data stream is done and the next data stream uses the same key and control, only the IV and length values need be re-loaded.

8.3 AES Interrupts & Triggers

8.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 8-2. CPU Interrupts Triggered by AES

NVIC Interrupt Name	Peripheral Instance Name	Register Group	AES Interrupt Configuration Registers	Description
AES.INT_EVENT0	AES	INT_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	AES RTC interrupt. Multiple OR'd, configurable source condition.

8.3.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 8-3. DMA Triggers from the AES

Trigger Name	Peripheral Instance Name	Register Group	AES DMA Configuration Registers	Description
AES.INT_EVENT1	AES	INT_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	AES Data input to engine DMA trigger. Single, configurable source condition.
AES.INT_EVENT2	AES	INT_EVENT2	IIDX, IMASK, RIS, MIS, ISET, ICLR	AES Data output from engine DMA trigger. Single, configurable source condition.

8.4 AES Registers

This Section describes the AES Registers.

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8.4.1 AES Base Address Table

Table 8-4. AES Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
AesRegs	AES_REGS	AES	0x401B_0000

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8.4.2 AES_REGS Registers

Table 8-5 lists the memory-mapped registers for the AES_REGS registers. All register offset addresses not listed in Table 8-5 should be considered as reserved locations and the register contents should not be modified.

Table 8-5. AES_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt Index Register	INT_EVENT0	Go
1028h	IMASK	Interrupt mask	INT_EVENT0	Go
1030h	RIS	Raw interrupt status	INT_EVENT0	Go
1038h	MIS	Masked interrupt status	INT_EVENT0	Go
1040h	ISET	Interrupt set	INT_EVENT0	Go
1048h	ICLR	Interrupt clear	INT_EVENT0	Go
1050h	IIDX	Interrupt Index Register	INT_EVENT1	Go
1058h	IMASK	Interrupt mask	INT_EVENT1	Go
1060h	RIS	Raw interrupt status	INT_EVENT1	Go
1068h	MIS	Masked interrupt status	INT_EVENT1	Go
1070h	ISET	Interrupt set	INT_EVENT1	Go
1078h	ICLR	Interrupt clear	INT_EVENT1	Go
1080h	IIDX	Interrupt Index Register	INT_EVENT2	Go
1088h	IMASK	Interrupt mask	INT_EVENT2	Go
1090h	RIS	Raw interrupt status	INT_EVENT2	Go
1098h	MIS	Masked interrupt status	INT_EVENT2	Go
10A0h	ISET	Interrupt set	INT_EVENT2	Go
10A8h	ICLR	Interrupt clear	INT_EVENT2	Go
10E0h	EVT_MODE	Event Mode		Go
1100h	GCMCCM_TAG0	CBC-MAC third key (LSW) / GCM & CCM Intermediate TAG (LSW)		Go
1104h	GCMCCM_TAG1	CBC-MAC third key / GCM & CCM Intermediate TAG		Go
1108h	GCMCCM_TAG2	CBC-MAC third key / GCM & CCM Intermediate TAG		Go
110Ch	GCMCCM_TAG3	CBC-MAC third key (MSW) / GCM & CCM Intermediate TAG (MSW)		Go
1110h	GHASH_H0	CCM & CBC-MAC second key (LSW) / GCM Hash Key input (LSW)		Go
1114h	GHASH_H1	CCM & CBC-MAC second key / GCM Hash Key input		Go
1118h	GHASH_H2	CCM & CBC-MAC second key / GCM Hash Key input		Go
111Ch	GHASH_H3	CCM & CBC-MAC second key (MSW) / GCM Hash Key input (MSW)		Go
1120h	KEY0	KEY (LSW)		Go
1124h	KEY1	KEY		Go
1128h	KEY2	KEY		Go
112Ch	KEY3	KEY		Go
1130h	KEY4	KEY		Go

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Table 8-5. AES_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1134h	KEY5	KEY		Go
1138h	KEY6	KEY		Go
113Ch	KEY7	KEY (MSW)		Go
1140h	IV0	IV (LSW)		Go
1144h	IV1	IV		Go
1148h	IV2	IV		Go
114Ch	IV3	IV		Go
1150h	CTRL	Input/Output Buffer Control and Mode selection		Go
1154h	C_LENGTH_0	Crypto data length (LSW)		Go
1158h	C_LENGTH_1	Crypto data length (MSW)		Go
115Ch	AAD_LENGTH	AAD Data Length		Go
1160h	DATA0	Data input (LSW) / Data output (LSW)		Go
1164h	DATA1	Data input / Data output		Go
1168h	DATA2	Data input / Data output		Go
116Ch	DATA3	Data input (LSW) / Data output (MSW)		Go
1170h	TAG0	Hash result (LSW)		Go
1174h	TAG1	Hash result		Go
1178h	TAG2	Hash result		Go
117Ch	TAG3	Hash result (MSW)		Go
1180h	STATUS	Status		Go
1184h	DATA_IN	Data in alias register		Go
1188h	DATA_OUT	Data out alias register		Go
11D0h	FORCE_IN_AV	Data control register for input data		Go
11D4h	CCM_ALN_WRD	AES-CCM AAD alignment data word		Go
11D8h	BLK_CNT0	Internal block counter (LSW)		Go
11DCh	BLK_CNT1	Internal block counter (MSW)		Go
11F4h	DMA_HS	Control register for DMA handshaking		Go

Complex bit access types are encoded to fit into small table cells. Table 8-6 shows the codes that are used for access types in this section.

Table 8-6. AES_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 8-11 and described in Table 8-7.

Return to the Summary Table.

Register to control the power state

Figure 8-11. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 8-8. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 8-12 and described in Table 8-8.

Return to the Summary Table.

Register to control reset assertion and de-assertion

Figure 8-12. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 8-10. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 8-13 and described in Table 8-9.

Return to the Summary Table.

peripheral enable and reset status

Figure 8-13. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 8-12. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 PDBGCTL Register (Offset = 1018h) [Reset = 00000000h]

PDBGCTL is shown in Figure 8-14 and described in Table 8-10.

Return to the Summary Table.

AES can not be halted when the core is halted. In order to halt the AES, the DMA shall be halted.
This achieves the same effect as a halt feature in the AES: when the AES submits the next DMA trigger, if the DMA is halted, then the AES will automatically halt.

Figure 8-14. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							FREE
R-0h							R-0h

Table 8-14. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	FREE	R	1h	Free run control 1h = The peripheral ignores the state of the Core Halted input

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5 IIDX Register (Offset = 1020h) [Reset = 00000000h] (INT_EVENT0)

IIDX is shown in Figure 8-15 and described in Table 8-11.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 8-15. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 8-16. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 1h = This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 2h = This indicates that the engine can take new input. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 3h = This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 4h = This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write new context.

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6 IMASK Register (Offset = 1028h) [Reset = 00000000h] (INT_EVENT0)

IMASK is shown in Figure 8-16 and described in Table 8-12.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 8-16. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				CNTXTRDY	SAVEDCNTXTRDY	INPUTRDY	OUTPUTRDY
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-18. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	CNTXTRDY	R/W	0h	This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write next context. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SAVEDCNTXTRDY	R/W	0h	This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INPUTRDY	R/W	0h	This indicates that the engine can take new input. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	OUTPUTRDY	R/W	0h	This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

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7 RIS Register (Offset = 1030h) [Reset = 00000000h] (INT_EVENT0)

RIS is shown in Figure 8-17 and described in Table 8-13.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 8-17. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CNTXTRDY	SAVEDCNTXTRDY	INPUTRDY	OUTPUTRDY
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-20. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CNTXTRDY	R	0h	This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write next context. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SAVEDCNTXTRDY	R	0h	This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INPUTRDY	R	0h	This indicates that the engine can take new input. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	OUTPUTRDY	R	0h	This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Interrupt did not occur 1h = Interrupt occured

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8 MIS Register (Offset = 1038h) [Reset = 00000000h] (INT_EVENT0)

MIS is shown in Figure 8-18 and described in Table 8-14.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 8-18. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CNTXTRDY	SAVEDCNTXTRDY	INPUTRDY	OUTPUTRDY
R-0h				R-0h	R-0h	R-0h	R-0h

Table 8-22. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	CNTXTRDY	R	0h	This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write next context. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SAVEDCNTXTRDY	R	0h	This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INPUTRDY	R	0h	This indicates that the engine can take new input. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	OUTPUTRDY	R	0h	This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Interrupt did not occur 1h = Interrupt occured

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9 ISET Register (Offset = 1040h) [Reset = 00000000h] (INT_EVENT0)

ISET is shown in Figure 8-19 and described in Table 8-15.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 8-19. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				CNTXTRDY	SAVEDCNTXTRDY	INPUTRDY	OUTPUTRDY
W-0h				W-0h	W-0h	W-0h	W-0h

Table 8-24. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	CNTXTRDY	W	0h	This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write next context. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SAVEDCNTXTRDY	W	0h	This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INPUTRDY	W	0h	This indicates that the engine can take new input.This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	OUTPUTRDY	W	0h	This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Writing 0 has no effect 1h = Set Interrupt

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10 ICLR Register (Offset = 1048h) [Reset = 00000000h] (INT_EVENT0)

ICLR is shown in Figure 8-20 and described in Table 8-16.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 8-20. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				CNTXTRDY	SAVEDCNTXTRDY	INPUTRDY	OUTPUTRDY
W-0h				W-0h	W-0h	W-0h	W-0h

Table 8-26. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	CNTXTRDY	W	0h	This bit indicates that the context data registers can be overwritten, and the CPU is permitted to write next context. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SAVEDCNTXTRDY	W	0h	This bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the CPU to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INPUTRDY	W	0h	This indicates that the engine can take new input. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	OUTPUTRDY	W	0h	This indicates that the core has an output available to be read out. This should not be used if DMA handshake is used (AES_DMA_HS.DMA_DATA_ACK set to 1) 0h = Writing 0 has no effect 1h = Clear Interrupt

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11 IIDX Register (Offset = 1050h) [Reset = 00000000h] (INT_EVENT1)

IIDX is shown in Figure 8-21 and described in Table 8-17.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 8-21. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 8-28. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 1h = AES trigger 0 DMA (Data Input trigger)

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12 IMASK Register (Offset = 1058h) [Reset = 00000000h] (INT_EVENT1)

IMASK is shown in Figure 8-22 and described in Table 8-18.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 8-22. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG0
R/W-0h							R/W-0h

Table 8-30. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	TRIG0	R/W	0h	TRIG0 event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

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13 RIS Register (Offset = 1060h) [Reset = 00000000h] (INT_EVENT1)

RIS is shown in Figure 8-23 and described in Table 8-19.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 8-23. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG0
R-0h							R-0h

Table 8-32. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	TRIG0	R	0h	TRIG0 event 0h = Interrupt did not occur 1h = Interrupt occured

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14 MIS Register (Offset = 1068h) [Reset = 00000000h] (INT_EVENT1)

MIS is shown in Figure 8-24 and described in Table 8-20.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 8-24. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG0
R-0h							R-0h

Table 8-34. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	TRIG0	R	0h	TRIG0 event 0h = Interrupt did not occur 1h = Interrupt occured

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15 ISET Register (Offset = 1070h) [Reset = 00000000h] (INT_EVENT1)

ISET is shown in Figure 8-25 and described in Table 8-21.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 8-25. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG0
W-0h							W-0h

Table 8-36. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG0	W	0h	TRIG0 0h = Writing 0 has no effect 1h = Set Interrupt

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16 ICLR Register (Offset = 1078h) [Reset = 00000000h] (INT_EVENT1)

ICLR is shown in Figure 8-26 and described in Table 8-22.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 8-26. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG0
W-0h							W-0h

Table 8-38. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG0	W	0h	TRIG0 event 0h = Writing 0 has no effect 1h = Clear Interrupt

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17 IIDX Register (Offset = 1080h) [Reset = 00000000h] (INT_EVENT2)

IIDX is shown in Figure 8-27 and described in Table 8-23.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 8-27. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 8-40. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 1h = AES DMA Trigger 1 (Data Output trigger)

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18 IMASK Register (Offset = 1088h) [Reset = 00000000h] (INT_EVENT2)

IMASK is shown in Figure 8-28 and described in Table 8-24.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 8-28. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG1
R/W-0h							R/W-0h

Table 8-42. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	TRIG1	R/W	0h	TRIG1 event mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

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19 RIS Register (Offset = 1090h) [Reset = 00000000h] (INT_EVENT2)

RIS is shown in Figure 8-29 and described in Table 8-25.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 8-29. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG1
R-0h							R-0h

Table 8-44. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	TRIG1	R	0h	TRIG1 event 0h = Interrupt did not occur 1h = Interrupt occured

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20 MIS Register (Offset = 1098h) [Reset = 00000000h] (INT_EVENT2)

MIS is shown in Figure 8-30 and described in Table 8-26.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 8-30. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG1
R-0h							R-0h

Table 8-46. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	TRIG1	R	0h	TRIG1 event 0h = Interrupt did not occur 1h = Interrupt occured

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21 ISET Register (Offset = 10A0h) [Reset = 00000000h] (INT_EVENT2)

ISET is shown in Figure 8-31 and described in Table 8-27.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 8-31. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG1
W-0h							W-0h

Table 8-48. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG1	W	0h	TRIG1 event 0h = Writing 0 has no effect 1h = Set Interrupt

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22 ICLR Register (Offset = 10A8h) [Reset = 00000000h] (INT_EVENT2)

ICLR is shown in Figure 8-32 and described in Table 8-28.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 8-32. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG1
W-0h							W-0h

Table 8-50. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG1	W	0h	TRIG1 event 0h = Writing 0 has no effect 1h = Clear Interrupt

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23 EVT_MODE Register (Offset = 10E0h) [Reset = 00000000h]

EVT_MODE is shown in Figure 8-33 and described in Table 8-29.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 8-33. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		EVT2_CFG		EVT1_CFG		INT0_CFG	
R/W-0h		R-0h		R-0h		R-0h	

Table 8-52. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-4	EVT2_CFG	R	2h	Event line mode select for event corresponding to [IPSTANDARD.INT_EVENT2] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
3-2	EVT1_CFG	R	2h	Event line mode select for event corresponding to [IPSTANDARD.INT_EVENT1] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
1-0	INT0_CFG	R	1h	Event line mode select for event corresponding to [IPSTANDARD.INT_EVENT0] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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24 GCMCCM_TAG0 Register (Offset = 1100h) [Reset = 00000000h]

GCMCCM_TAG0 is shown in Figure 8-34 and described in Table 8-30.

Return to the Summary Table.

CBC-MAC third key (LSW) / GCM & CCM Intermediate TAG (LSW)
For CBC-MAC: Pre-calculated CBC-MAC third key used to perform a final XOR operation on the last input data block.
For CCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new CCM context. To restore an interrupted CCM operation, this register needs to be loaded with the intermediate TAG.
For GCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new GCM context. To restore an interrupted GCM operation, this register needs to be loaded with the intermediate TAG.

Figure 8-34. GCMCCM_TAG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-54. GCMCCM_TAG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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25 GCMCCM_TAG1 Register (Offset = 1104h) [Reset = 00000000h]

GCMCCM_TAG1 is shown in Figure 8-35 and described in Table 8-31.

Return to the Summary Table.

CBC-MAC third key / GCM & CCM Intermediate TAG
For CBC-MAC: Pre-calculated CBC-MAC third key used to perform a final XOR operation on the last input data block.
For CCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new CCM context. To restore an interrupted CCM operation, this register needs to be loaded with the intermediate TAG.
For GCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new GCM context. To restore an interrupted GCM operation, this register needs to be loaded with the intermediate TAG.

Figure 8-35. GCMCCM_TAG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-56. GCMCCM_TAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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26 GCMCCM_TAG2 Register (Offset = 1108h) [Reset = 00000000h]

GCMCCM_TAG2 is shown in Figure 8-36 and described in Table 8-32.

Return to the Summary Table.

CBC-MAC third key / GCM & CCM Intermediate TAG
For CBC-MAC: Pre-calculated CBC-MAC third key used to perform a final XOR operation on the last input data block.
For CCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new CCM context. To restore an interrupted CCM operation, this register needs to be loaded with the intermediate TAG.
For GCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new GCM context. To restore an interrupted GCM operation, this register needs to be loaded with the intermediate TAG.

Figure 8-36. GCMCCM_TAG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-58. GCMCCM_TAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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27 GCMCCM_TAG3 Register (Offset = 110Ch) [Reset = 00000000h]

GCMCCM_TAG3 is shown in Figure 8-37 and described in Table 8-33.

Return to the Summary Table.

CBC-MAC third key (MSW) / GCM & CCM Intermediate TAG (MSW)
For CBC-MAC: Pre-calculated CBC-MAC third key used to perform a final XOR operation on the last input data block.
For CCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new CCM context. To restore an interrupted CCM operation, this register needs to be loaded with the intermediate TAG.
For GCM: This register is internally used to store intermediate values. This register must be initialized with zeroes when writing a new GCM context. To restore an interrupted GCM operation, this register needs to be loaded with the intermediate TAG.

Figure 8-37. GCMCCM_TAG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-60. GCMCCM_TAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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28 GHASH_H0 Register (Offset = 1110h) [Reset = 00000000h]

GHASH_H0 is shown in Figure 8-38 and described in Table 8-34.

Return to the Summary Table.

CCM & CBC-MAC second key (LSW) / GCM Hash Key input (LSW)
For CBC-MAC: Pre-calculated CBC-MAC second key used to perform a final XOR operation on the last input data block.
For GCM: Hash key
can be calculated internal or written via these registers. Only used for GHASH (GCM) modes.
For a CPU write operation, these registers must be written with the new values to be subsequently transferred to the engine.

Figure 8-38. GHASH_H0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-62. GHASH_H0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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29 GHASH_H1 Register (Offset = 1114h) [Reset = 00000000h]

GHASH_H1 is shown in Figure 8-39 and described in Table 8-35.

Return to the Summary Table.

CCM & CBC-MAC second key / GCM Hash Key input
For CBC-MAC: Pre-calculated CBC-MAC second key used to perform a final XOR operation on the last input data block.
For GCM: Hash key
can be calculated internal or written via these registers. Only used for GHASH (GCM) modes.
For a CPU write operation, these registers must be written with the new values to be subsequently transferred to the engine.

Figure 8-39. GHASH_H1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-64. GHASH_H1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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30 GHASH_H2 Register (Offset = 1118h) [Reset = 00000000h]

GHASH_H2 is shown in Figure 8-40 and described in Table 8-36.

Return to the Summary Table.

CCM & CBC-MAC second key / GCM Hash Key input
For CBC-MAC: Pre-calculated CBC-MAC second key used to perform a final XOR operation on the last input data block.
For GCM: Hash key
can be calculated internal or written via these registers. Only used for GHASH (GCM) modes.
For a CPU write operation, these registers must be written with the new values to be subsequently transferred to the engine.

Figure 8-40. GHASH_H2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-66. GHASH_H2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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31 GHASH_H3 Register (Offset = 111Ch) [Reset = 00000000h]

GHASH_H3 is shown in Figure 8-41 and described in Table 8-37.

Return to the Summary Table.

CCM & CBC-MAC second key (MSW) / GCM Hash Key input (MSW)
For CBC-MAC: Pre-calculated CBC-MAC second key used to perform a final XOR operation on the last input data block.
For GCM: Hash key
can be calculated internal or written via these registers. Only used for GHASH (GCM) modes.
For a CPU write operation, these registers must be written with the new values to be subsequently transferred to the engine.

Figure 8-41. GHASH_H3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-68. GHASH_H3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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32 KEY0 Register (Offset = 1120h) [Reset = 00000000h]

KEY0 is shown in Figure 8-42 and described in Table 8-38.

Return to the Summary Table.

KEY (LSW)

Figure 8-42. KEY0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-70. KEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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33 KEY1 Register (Offset = 1124h) [Reset = 00000000h]

KEY1 is shown in Figure 8-43 and described in Table 8-39.

Return to the Summary Table.

KEY

Figure 8-43. KEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-72. KEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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34 KEY2 Register (Offset = 1128h) [Reset = 00000000h]

KEY2 is shown in Figure 8-44 and described in Table 8-40.

Return to the Summary Table.

KEY

Figure 8-44. KEY2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-74. KEY2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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35 KEY3 Register (Offset = 112Ch) [Reset = 00000000h]

KEY3 is shown in Figure 8-45 and described in Table 8-41.

Return to the Summary Table.

KEY

Figure 8-45. KEY3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-76. KEY3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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36 KEY4 Register (Offset = 1130h) [Reset = 00000000h]

KEY4 is shown in Figure 8-46 and described in Table 8-42.

Return to the Summary Table.

KEY

Figure 8-46. KEY4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-78. KEY4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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37 KEY5 Register (Offset = 1134h) [Reset = 00000000h]

KEY5 is shown in Figure 8-47 and described in Table 8-43.

Return to the Summary Table.

KEY

Figure 8-47. KEY5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-80. KEY5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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38 KEY6 Register (Offset = 1138h) [Reset = 00000000h]

KEY6 is shown in Figure 8-48 and described in Table 8-44.

Return to the Summary Table.

KEY

Figure 8-48. KEY6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-82. KEY6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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39 KEY7 Register (Offset = 113Ch) [Reset = 00000000h]

KEY7 is shown in Figure 8-49 and described in Table 8-45.

Return to the Summary Table.

KEY (MSW)

Figure 8-49. KEY7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-84. KEY7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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40 IV0 Register (Offset = 1140h) [Reset = 00000000h]

IV0 is shown in Figure 8-50 and described in Table 8-46.

Return to the Summary Table.

IV (LSW)

Figure 8-50. IV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-86. IV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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41 IV1 Register (Offset = 1144h) [Reset = 00000000h]

IV1 is shown in Figure 8-51 and described in Table 8-47.

Return to the Summary Table.

IV

Figure 8-51. IV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-88. IV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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42 IV2 Register (Offset = 1148h) [Reset = 00000000h]

IV2 is shown in Figure 8-52 and described in Table 8-48.

Return to the Summary Table.

IV

Figure 8-52. IV2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-90. IV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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43 IV3 Register (Offset = 114Ch) [Reset = 00000000h]

IV3 is shown in Figure 8-53 and described in Table 8-49.

Return to the Summary Table.

IV

Figure 8-53. IV3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-92. IV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Key data

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44 CTRL Register (Offset = 1150h) [Reset = 80000000h]

CTRL is shown in Figure 8-54 and described in Table 8-50.

Return to the Summary Table.

Input/Output Buffer Control and Mode selection. The content of this register determines the mode of operation of the EIP-39.

Figure 8-54. CTRL Register

31	30	29	28	27	26	25	24
CNTXT_RDY	SAVED_CNTXT_RDY	SAVE_CNTXT	GCM_CONT	GET_DIGEST	OFB_GCM_CCM_CONT	RESERVED	CCMM
R-1h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CCMM		CCML			CCM	GCM	
R/W-0h		R/W-0h			R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
CBCMAC	RESERVED				CFB	ICM	CTR_WIDTH
R/W-0h	R/W-0h				R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CTR_WIDTH	CTR	CBC	KEYSIZE		DIR	INPUT_RDY	OUTPUT_RDY
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R-0h	R-0h

Table 8-94. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CNTXT_RDY	R	1h	If '1b', this read-only status bit indicates that the context data registers can be overwritten, and the CPU is permitted to write the next context. 0h = Not ready 1h = Ready
30	SAVED_CNTXT_RDY	R	0h	If '1b', this read-only status bit indicates that an AES authentication TAG and/or IV block(s) is/are available for the Host to retrieve. This bit is only asserted if the 'save_context' bit is set to '1b'. The bit is mutually exclusive with the 'context_ready' bit. 0h = Not ready 1h = Ready
29	SAVE_CNTXT	R/W	0h	This bit is used to indicate that an authentication TAG or result IV needs to be stored as a result context. If this bit is set, context output DMA and/or interrupt will be asserted if the operation is finished, and related signals are enabled. Typically, this value must be set for authentication modes returning a TAG (CBC-MAC, GCM and CCM), or for basic encryption modes that require future continuation with the current result IV. If this bit is set, the engine will hold its full context until the TAG and/or IV registers are read. Only after reading the TAG or IV, a new DMA request for a new (input) context will be asserted. If this bit is not set, the engine will assert the context input DMA request signal directly after starting to process the last block with the current context. 0h = No effect 1h = Enable

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Table 8-94. CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	GCM_CONT	R/W	0h	Continue processing of an interrupted AES-GCM or AES-CCM operation in the crypto/payload phase. Set this write-only signal to '1b' together with the regular mode bit settings for a GCM or CCM operation, to continue processing from the next full block (128 bits) boundary. Before setting this bit all applicable context to resume processing must have been loaded into the engine: Keys, IV, intermediate digest/TAG and block counter. The mode can be written together with this bit, as it is part of the same register. 0h = No effect 1h = Enable
27	GET_DIGEST	R/W	0h	Interrupt processing and generate an intermediate digest during an AES-GCM or AES-CCM operation. Set this write-only signal to '1b' to interrupt GCM or CCM processing at the next full block (128 bits) boundary. An intermediate digest may be requested during the encryption/decryption data phase or in the AAD phase. Note: Interruption can only be done on full block (128 bits) boundaries. The minimum number of remaining bytes to resume and finalize the operation, must be greater than or equal to 1. 0h = No effect 1h = Enable
26	OFB_GCM_CCM_CONT	R/W	0h	This bit has a dual use, depending on the selection of CCM/GCM, see bits [18:16]. If CCM/GCM is not selected: If this bit is set to '1b', full block AES output feedback mode (OFB-128) is selected. If CCM/GCM is selected: Continue processing of an interrupted AES-GCM or AES-CCM operation in the AAD phase. Set this write-only signal to '1b' together with the regular mode bit settings for a GCM or CCM operation, to continue processing from the next full AAD block (128 bits) boundary. Before setting this bit all applicable context to resume processing must have been loaded into the engine: Keys, IV, intermediate digest/TAG, block counter and the CCM align data word (the latter is for CCM mode only). The mode can be written together with this bit, as it is part of the same register. 1h = Continue GCM/CCM processing in AAD phase
25	RESERVED	R/W	0h	
24-22	CCMM	R/W	0h	Defines "M" that indicates the length of the authentication field for CCM operations the authentication field length equals two times (the value of CCM-M plus one). Note: The EIP-39 always returns a 128-bit authentication field, of which the M least significant bytes are valid. All values are supported. 0h = Length is 1 7h = Length is 8
21-19	CCML	R/W	0h	Defines "L" that indicates the width of the length field for CCM operations the length field in bytes equals the value of CMM-L plus one. All values are supported. 0h = Length is 1 7h = Length is 8
18	CCM	R/W	0h	If set to '1b', AES-CCM is selected, this is a combined mode, using AES for both authentication and encryption. In addition to the CCM bit, the CTR mode bit must be set such that AES-CTR is enabled. Other combinations with CCM are invalid. 0h = Disable CBC mode 1h = Select CBC mode

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Table 8-94. CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	GCM	R/W	0h	If not set to '00b', AES-GCM mode is selected, this is a combined mode, using the Galois field multiplier GF(2128) for authentication and AES-CTR mode for encryption, the bits specify the GCM mode: 01b = GHASH with H loaded and Y0-encrypted forced to zero 10b = GHASH with H loaded and Y0-encrypted calculated internally 11b = Autonomous GHASH (both H and Y0-encrypted calculated internally) Note: Besides GCM, the CTR mode bits must also be set to '1b' to enable GCM with AES-CTR if the CTR bit is not set a GHASH (authentication) only operation is performed. A GHASH only operation is only allowed if the GCM mode is set to '01b' and the direction bit is set to '0b'. Other modes may not be selected in combination with GCM. Table 14 below shows the valid combinations for the GCM and CTR mode bits, all other options are invalid and must not be selected. 1h = GHASH with H loaded and Y0-encrypted forced to 0. 2h = GHASH with H loaded and Y0-encrypted calculated internally 3h = Autonomous GHASH (both H and Y0-encrypted calculated internally)
15	CBCMAC	R/W	0h	If set to '1b', AES-CBC MAC is selected, the Direction bit must be set to '1' for this mode. 0h = Disable CBC mode 1h = Select CBC mode
14-11	RESERVED	R/W	0h	
10	CFB	R/W	0h	If set to '1b', AES cipher feedback mode CFB is selected. Use the ctr_width field to specify the feedback width. 0h = Disable CBC mode 1h = Select CBC mode
9	ICM	R/W	0h	When the CFB bit is set, specifies the CFB mode feedback width: 0h = Disable CBC mode 1h = Select CBC mode
8-7	CTR_WIDTH	R/W	0h	When the CTR bit is set, specifies the counter width for AES-CTR mode. When the CFB bit is set, specifies the CFB mode feedback width: 0h = CFB-128 mode 1h = 64-bit counter 2h = 96-bit counter 3h = 128-bit counter
6	CTR	R/W	0h	If set to '1b', AES counter mode (CTR) is selected. Note: This bit must also be set for GCM and CCM, when encryption/decryption is required. 0h = Disable CBC mode 1h = Select CBC mode
5	CBC	R/W	0h	If set to '1b', cipher-block-chaining (CBC) mode is selected. 0h = Disable CBC mode 1h = Select CBC mode
4-3	KEYSIZE	R/W	0h	Specifies the encryption strength / key width 1h = 128-bit key 3h = 256-bit key
2	DIR	R/W	0h	Direction. If set to '1b' an encrypt operation is performed. If set to '0b' a decrypt operation is performed. Note: This bit must be written with a '1b' when CBC-MAC is selected. 0h = Decryption 1h = Encryption
1	INPUT_RDY	R	0h	Ready for input. If '1b', this read-only status bit indicates that the 16-byte input buffer is empty, and the CPU is permitted to write the next block of data. After reset, this bit is '0'. After writing a context, this bit will become '1b'. 0h = Not Ready 1h = Ready

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Table 8-94. CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OUTPUT_RDY	R	0h	Output Ready. If '1b', this read-only status bit indicates that an AES output block is available for the CPU to retrieve. 0h = Not Ready 1h = Ready

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45 C_LENGTH_0 Register (Offset = 1154h) [Reset = 00000000h]

C_LENGTH_0 is shown in Figure 8-55 and described in Table 8-51.

Return to the Summary Table.

Crypto data length (LSW). These registers buffer the Length values to the EIP-39. While processing, the length values decrement to zero. If both lengths are zero, the data stream is finished, and a new context is requested. For basic AES modes (ECB/CBC/CTR/ICM/CFB/OFB), a crypto length of '0' can be written if the context DMA is disabled. Writing a zero length results in continued data requests until a new context is written. For the other modes (GCM and CCM) no (new) data requests are done if the length decrements to or equals zero.
It is advised to write a new length per packet. If the length registers decrement to zero, no new data is processed until a new context or length value is written.
When writing a new context without writing the length registers, the length register values from the previous context are reused.

Figure 8-55. C_LENGTH_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-96. C_LENGTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Bits [60:0] of the crypto length registers (LSW and MSW) store the cryptographic data length in bytes for all modes. Once processing with this context is started, this length decrements to zero. Data lengths up to (261-1) bytes are allowed. For GCM, any value up to 236-32 bytes can be used. This is because a 32-bit counter mode is used the maximum number of 128-bit blocks is 232-2, resulting in a maximum number of bytes of 236-32. A write to this register triggers the engine to start using this context. This is valid for all modes except GCM and CCM. Note that for the combined modes, this length does not include the authentication only data the authentication length is specified in the AES_AAD_LENGTH register below. All modes must have a length > 0. For the combined modes, it is allowed to have one of the lengths equal to zero. For the basic encryption modes (ECB/CBC/CTR/ICM/CFB/OFB) it is allowed to program zero to the length field in that case the length is assumed infinite. All data must be byte (8-bit) aligned for stream cipher modes bit aligned data streams are not supported. For block cipher modes, the data length must be programmed in multiples of the block cipher size, 16 bytes.

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46 C_LENGTH_1 Register (Offset = 1158h) [Reset = 00000000h]

C_LENGTH_1 is shown in Figure 8-56 and described in Table 8-52.

Return to the Summary Table.

Crypto data length (MSW). These registers buffer the Length values to the EIP-39. While processing, the length values decrement to zero. If both lengths are zero, the data stream is finished, and a new context is requested. For basic AES modes (ECB/CBC/CTR/ICM/CFB/OFB), a crypto length of '0' can be written if the context DMA is disabled. Writing a zero length results in continued data requests until a new context is written. For the other modes (GCM and CCM) no (new) data requests are done if the length decrements to or equals zero.
It is advised to write a new length per packet. If the length registers decrement to zero, no new data is processed until a new context or length value is written.
When writing a new context without writing the length registers, the length register values from the previous context are reused.

Figure 8-56. C_LENGTH_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			DATA																												
W-0h			W-0h																												

Table 8-98. C_LENGTH_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28-0	DATA	W	0h	Bits [60:0] of the crypto length registers (LSW and MSW) store the cryptographic data length in bytes for all modes. Once processing with this context is started, this length decrements to zero. Data lengths up to (261-1) bytes are allowed. For GCM, any value up to 236-32 bytes can be used. This is because a 32-bit counter mode is used the maximum number of 128-bit blocks is 232-2, resulting in a maximum number of bytes of 236-32. A write to this register triggers the engine to start using this context. This is valid for all modes except GCM and CCM. Note that for the combined modes, this length does not include the authentication only data the authentication length is specified in the AES_AAD_LENGTH register below. All modes must have a length > 0. For the combined modes, it is allowed to have one of the lengths equal to zero. For the basic encryption modes (ECB/CBC/CTR/ICM/CFB/OFB) it is allowed to program zero to the length field in that case the length is assumed infinite. All data must be byte (8-bit) aligned for stream cipher modes bit aligned data streams are not supported. For block cipher modes, the data length must be programmed in multiples of the block cipher size, 16 bytes.

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47 AAD_LENGTH Register (Offset = 115Ch) [Reset = 00000000h]

AAD_LENGTH is shown in Figure 8-57 and described in Table 8-53.

Return to the Summary Table.

AAD Data Length

Figure 8-57. AAD_LENGTH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-100. AAD_LENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Bits [31:0] of the authentication length register store the authentication data length in bytes for combined modes only (GCM or CCM) Supported AAD-lengths for CCM are from 0 to (216-28) bytes. For GCM any value up to (232-1) bytes can be used. Once processing with this context is started, this length decrements to zero. A write to this register triggers the engine to start using this context for GCM and CCM.

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48 DATA0 Register (Offset = 1160h) [Reset = 00000000h]

DATA0 is shown in Figure 8-58 and described in Table 8-54.

Return to the Summary Table.

Data input (LSW) / Data output (LSW)\. The Data Input/Output Registers buffer the input/output data blocks to/from the EIP-39. Notice that the data input buffer (AES_DATA_IN_n) and data output buffer (AES_DATA_OUT_n) are mapped to the same address locations. Writes to these addresses load the Input Buffer while reads pull from the Output Buffer. Therefore, for write access, the data input buffer is written for read access, the data output buffer is read. The data input buffer must be written prior to starting an operation. The data output buffer contains valid data on completion of an operation. All writes from, and reads to, these registers are tracked independently per direction. Therefore, any 128-bit data block can be split over multiple 32-bit word transfers, which can be mixed with other transfers over the external interface.

Figure 8-58. DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

Table 8-102. DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Data

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49 DATA1 Register (Offset = 1164h) [Reset = 00000000h]

DATA1 is shown in Figure 8-59 and described in Table 8-55.

Return to the Summary Table.

Data input / Data output. The Data Input/Output Registers buffer the input/output data blocks to/from the EIP-39. Notice that the data input buffer (AES_DATA_IN_n) and data output buffer (AES_DATA_OUT_n) are mapped to the same address locations. Writes to these addresses load the Input Buffer while reads pull from the Output Buffer. Therefore, for write access, the data input buffer is written
for read access, the data output buffer is read. The data input buffer must be written prior to starting an operation. The data output buffer contains valid data on completion of an operation. All writes from, and reads to, these registers are tracked independently per direction. Therefore, any 128-bit data block can be split over multiple 32-bit word transfers, which can be mixed with other transfers over the external interface.

Figure 8-59. DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

Table 8-104. DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Data

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50 DATA2 Register (Offset = 1168h) [Reset = 00000000h]

DATA2 is shown in Figure 8-60 and described in Table 8-56.

Return to the Summary Table.

Data input / Data output. The Data Input/Output Registers buffer the input/output data blocks to/from the EIP-39. Notice that the data input buffer (AES_DATA_IN_n) and data output buffer (AES_DATA_OUT_n) are mapped to the same address locations. Writes to these addresses load the Input Buffer while reads pull from the Output Buffer. Therefore, for write access, the data input buffer is written
for read access, the data output buffer is read. The data input buffer must be written prior to starting an operation. The data output buffer contains valid data on completion of an operation. All writes from, and reads to, these registers are tracked independently per direction. Therefore, any 128-bit data block can be split over multiple 32-bit word transfers, which can be mixed with other transfers over the external interface.

Figure 8-60. DATA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

Table 8-106. DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Data

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51 DATA3 Register (Offset = 116Ch) [Reset = 00000000h]

DATA3 is shown in Figure 8-61 and described in Table 8-57.

Return to the Summary Table.

Data input (MSW) / Data output (MSW). The Data Input/Output Registers buffer the input/output data blocks to/from the EIP-39. Notice that the data input buffer (AES_DATA_IN_n) and data output buffer (AES_DATA_OUT_n) are mapped to the same address locations. Writes to these addresses load the Input Buffer while reads pull from the Output Buffer. Therefore, for write access, the data input buffer is written for read access, the data output buffer is read. The data input buffer must be written prior to starting an operation. The data output buffer contains valid data on completion of an operation. All writes from, and reads to, these registers are tracked independently per direction. Therefore, any 128-bit data block can be split over multiple 32-bit word transfers, which can be mixed with other transfers over the external interface.

Figure 8-61. DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

Table 8-108. DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Data

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52 TAG0 Register (Offset = 1170h) [Reset = 00000000h]

TAG0 is shown in Figure 8-62 and described in Table 8-58.

Return to the Summary Table.

Hash result (LSW). These registers buffer the TAG from the EIP-39. The registers are shared with the intermediate authentication result registers but cannot be read until the processing is finished.

Figure 8-62. TAG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 8-110. TAG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	For a CPU read operation, these registers contain the last 128-bit TAG output of the EIP-39 the TAG is available until the next context is written. This register will only contain valid data if the TAG is available, when the 'saved_context_ready' or 'get_digest' bit from AES_CTRL register is set. In case of get_digest, the output will be an intermediate TAG for CCM or GCM operation continuation. During processing or for operations/modes that do not return a TAG, reads from this register returns data from the IV register. For operations that do return a TAG in the IV register, the IV register must be accessed directly.

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53 TAG1 Register (Offset = 1174h) [Reset = 00000000h]

TAG1 is shown in Figure 8-63 and described in Table 8-59.

Return to the Summary Table.

Hash result. These registers buffer the TAG from the EIP-39. The registers are shared with the intermediate authentication result registers but cannot be read until the processing is finished.

Figure 8-63. TAG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 8-112. TAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	For a CPU read operation, these registers contain the last 128-bit TAG output of the EIP-39 the TAG is available until the next context is written. This register will only contain valid data if the TAG is available, when the 'saved_context_ready' or 'get_digest' bit from AES_CTRL register is set. In case of get_digest, the output will be an intermediate TAG for CCM or GCM operation continuation. During processing or for operations/modes that do not return a TAG, reads from this register returns data from the IV register. For operations that do return a TAG in the IV register, the IV register must be accessed directly.

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54 TAG2 Register (Offset = 1178h) [Reset = 00000000h]

TAG2 is shown in Figure 8-64 and described in Table 8-60.

Return to the Summary Table.

Hash result. These registers buffer the TAG from the EIP-39. The registers are shared with the intermediate authentication result registers but cannot be read until the processing is finished.

Figure 8-64. TAG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 8-114. TAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	For a CPU read operation, these registers contain the last 128-bit TAG output of the EIP-39 the TAG is available until the next context is written. This register will only contain valid data if the TAG is available, when the 'saved_context_ready' or 'get_digest' bit from AES_CTRL register is set. In case of get_digest, the output will be an intermediate TAG for CCM or GCM operation continuation. During processing or for operations/modes that do not return a TAG, reads from this register returns data from the IV register. For operations that do return a TAG in the IV register, the IV register must be accessed directly.

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55 TAG3 Register (Offset = 117Ch) [Reset = 00000000h]

TAG3 is shown in Figure 8-65 and described in Table 8-61.

Return to the Summary Table.

Hash result (MSW). These registers buffer the TAG from the EIP-39. The registers are shared with the intermediate authentication result registers but cannot be read until the processing is finished.

Figure 8-65. TAG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 8-116. TAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	For a CPU read operation, these registers contain the last 128-bit TAG output of the EIP-39 the TAG is available until the next context is written. This register will only contain valid data if the TAG is available, when the 'saved_context_ready' or 'get_digest' bit from AES_CTRL register is set. In case of get_digest, the output will be an intermediate TAG for CCM or GCM operation continuation. During processing or for operations/modes that do not return a TAG, reads from this register returns data from the IV register. For operations that do return a TAG in the IV register, the IV register must be accessed directly.

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56 STATUS Register (Offset = 1180h) [Reset = 00000000h]

STATUS is shown in Figure 8-66 and described in Table 8-62.

Return to the Summary Table.

Status register

Figure 8-66. STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							KEYWR
R-0h							R-0h

Table 8-118. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	KEYWR	R	0h	Key write status. 0 - user write to KEY register is allowed. 1 - user write to KEY register is ignored. In order to allow user write, perform a module reset. 0h = User write to KEY MMR is allowed 1h = User write to KEY MMR is disabled. Writing has no effect.

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57 DATA_IN Register (Offset = 1184h) [Reset = 00000000h]

DATA_IN is shown in Figure 8-67 and described in Table 8-63.

Return to the Summary Table.

Data-in register: alias for DATA0/1/2/3 at a single address for DMA addressing

Figure 8-67. DATA_IN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-120. DATA_IN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Data input word

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58 DATA_OUT Register (Offset = 1188h) [Reset = 00000000h]

DATA_OUT is shown in Figure 8-68 and described in Table 8-64.

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Data-out register: alias for DATA0/1/2/3 at a single address for DMA addressing

Figure 8-68. DATA_OUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

Table 8-122. DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	Data output word

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59 FORCE_IN_AV Register (Offset = 11D0h) [Reset = 00000000h]

FORCE_IN_AV is shown in Figure 8-69 and described in Table 8-65.

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Data control register for input data. This write-only register provides a means to force the availability of the input data buffer of the EIP-39.

Figure 8-69. FORCE_IN_AV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-124. FORCE_IN_AV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Any write to this register forces the input data buffer to valid and will force the engine to start processing this data. The data written here is not used. The core must be configured to have input and output data acknowledge be I/O register based

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60 CCM_ALN_WRD Register (Offset = 11D4h) [Reset = 00000000h]

CCM_ALN_WRD is shown in Figure 8-70 and described in Table 8-66.

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AES-CCM AAD alignment data word. This register provides a means to access an internal EIP-39 register that stores alignment data bytes during the AAD phase of AES-CCM processing. This register needs to be read and stored when an AES-CCM operation is interrupted during the AAD phase. This value needs to be restored by writing this register, when resuming that AES-CCM operation in a later session.

Figure 8-70. CCM_ALN_WRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 8-126. CCM_ALN_WRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	This register provides a means to access an internal EIP-39 register that stores alignment data bytes during the AAD phase of AES-CCM processing. This register needs to be read and stored when an AES-CCM operation is interrupted during the AAD phase. This value needs to be restored by writing this register, when resuming that AES-CCM operation in a later session.

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61 BLK_CNT0 Register (Offset = 11D8h) [Reset = 00000000h]

BLK_CNT0 is shown in Figure 8-71 and described in Table 8-67.

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Internal block counter (LSW). This register along with BLK_CNT1 register provides access to the internal data block counter of the EIP-39. This counter keeps track of the number of data blocks during AES-CCM and AES-GCM operations. Reading and writing this counter allows interruption and resuming of long CCM or GCM operations. Note that internally, the block counter is used for AAD data as well as encryption/decryption data. Interruption and resuming is only supported in the encryption/decryption data phase and not during AAD.

Figure 8-71. BLK_CNT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

Table 8-128. BLK_CNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Internal block counter for AES GCM and CCM operations. These bits read the block count value that represents the number of blocks to go. This value is valid with saved_context_ready after a request for an intermediate GCM/CCM digest. Writing these registers will restore the internal block counter to the programmed value. This only needs to be done to prepare the engine to continue processing of an interrupted GCM or CCM operation. Also refer to the get_digest and gcm_ccm_continue bits in AES_CTRL register.

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62 BLK_CNT1 Register (Offset = 11DCh) [Reset = 00000000h]

BLK_CNT1 is shown in Figure 8-72 and described in Table 8-68.

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Internal block counter (MSW). This register along with BLK_CNT0 register provides access to the internal data block counter of the EIP-39. This counter keeps track of the number of data blocks during AES-CCM and AES-GCM operations. Reading and writing this counter allows interruption and resuming of long CCM or GCM operations. Note that internally, the block counter is used for AAD data as well as encryption/decryption data. Interruption and resuming is only supported in the encryption/decryption data phase and not during AAD.

Figure 8-72. BLK_CNT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DATA																							
R/W-0h								R/W-0h																							

Table 8-130. BLK_CNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23-0	DATA	R/W	0h	Internal block counter for AES GCM and CCM operations. These bits read the block count value that represents the number of blocks to go. This value is valid with saved_context_ready after a request for an intermediate GCM/CCM digest. Writing these registers will restore the internal block counter to the programmed value. This only needs to be done to prepare the engine to continue processing of an interrupted GCM or CCM operation. Also refer to the get_digest and gcm_ccm_continue bits in AES_CTRL register.

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63 DMA_HS Register (Offset = 11F4h) [Reset = 00000000h]

DMA_HS is shown in Figure 8-73 and described in Table 8-69.

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Control register for DMA handshaking

Figure 8-73. DMA_HS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							DMA_DATA_ACK
R/W-0h							R/W-0h

Table 8-132. DMA_HS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	DMA_DATA_ACK	R/W	0h	When this bit is 0b, input and output data acknowledge is I/O register based, as specified in the description of the AES_DATA_IN_n / AES_DATA_OUT_n registers. When this bit is 1b, input and ouput data acknowledge is based on DMA handshake signals. 0h = Disable DMA based data handshake 1h = Enables DMA based handshake

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Chapter 9

Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys.

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9.1 Detailed Description

The keystore supports storage of AES keys. Up to four 128-bit key slots are provisioned and can be used in different software-managed configurations, such as:

- Four 128-bit keys
- Two 256-bit keys
- One 256-bit key and two 128-bit keys

Note

Refer to the device-specific data sheet to determine the number of AES keys supported.

This configuration selection is the first to be performed by customer secure code before depositing keys into slots. Configuration is done by writing the number of 256-bit keys into the NK256 field of the CFG register.

After configuration, the key bytes can be written to selected slots in the keystore controller register. This is done by programming the KEYSZSEL (key size selection) and KEYSLOTSEL (key slot selection) fields of the KEYWR register. Note that the hardware expects any 256-bit keys to be store in lower-numbered slots. For example, if the store is configured for one 256-bit key and two 128-bit keys, the 256-bit key must be stored in slots 0 and 1. The IP reports an error (invalid configuration) if any other slot is used for the 256-bit key. If the store is configured for two 256-bit keys, then key 0 occupies slots 0 and 1 and key 1 occupies slots 2 and 3.

Depositing the key bytes into slots is done by writing them to the KEYIN register. Once a key write transaction is initiated, until and unless all the key bytes are written (4 words for a 128-bit key and 8 words for a 256-bit key), the key is not considered valid. Validity of slots is presented via a status register for the application. When customer secure code has deposited the required number of bytes, the key becomes valid and can be used by the application. The STATUS register provides status and validity fields to indicate status of the keystore controller as well as the validity of key slots.

Note that key configuration operations are permitted only while customer secure code is executing. Subsequently, the keystore configuration is locked and can not be modified. The signaling of the end of customer secure code is discussed in the Security Architecture chapter.

At run-time (after the end of customer secure code execution), the application is able to use one of the valid keys for an AES encryption/decryption operation. To configure the AES engine to use a specific key, the application references a key slot and initiates a transfer of the key data into the AES engine via a secure internal bus. This is performed by writing to the KEYSZSEL (key size selection), and KEYSLOTSEL (Key slot selection) fields of the KEYRD register. The selected key data is securely transferred to the AES engine over a private bus that is not accessible by software or the debugger.

The keystore holds the state and key data until a subsequent boot reset. At boot reset, customer startup code configures the keystore. If one or more slots are not used at the end of customer startup code execution, those slots remain unusable for the rest of the application execution.

9.2 KEYSTORE Registers

This Section describes the KEYSTORE Registers.

9.2.1 KEYSTORE Base Address Table

Table 9-1. KEYSTORE Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
KeystoreRegs	KEYSTORE_REGS	KEYSTORE	0x401B_6000

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9.2.2 KEYSTORE_REGS Registers

Table 9-2 lists the memory-mapped registers for the KEYSTORE_REGS registers. All register offset addresses not listed in Table 9-2 should be considered as reserved locations and the register contents should not be modified.

Table 9-2. KEYSTORE_REGS Registers

Offset	Acronym	Register Name	Group	Section
1100h	CFG	Keystore configuration		Go
1104h	KEYWR	Key write configuration		Go
1108h	KEYRD	Key read configuration		Go
110Ch	STATUS	Status		Go
1110h	KEYIN	Input key		Go
1114h	KEYLOCK	Keylock		Go

Complex bit access types are encoded to fit into small table cells. Table 9-3 shows the codes that are used for access types in this section.

Table 9-3. KEYSTORE_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 CFG Register (Offset = 1100h) [Reset = 00000001h]

CFG is shown in Figure 9-1 and described in Table 9-4.

Return to the Summary Table.

Key-store configuration register.

Figure 9-1. CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NK256			
R/W-0h												R/W-1h			

Table 9-5. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3-0	NK256	R/W	1h	Number of 256 bit keys to be held in the key-store. Can not exceed the total number of slots present in the hardware / 2. For eg: if SYS_N_SLOTS = 4, then atmost 2 256-bit keys can be held in the key-store. Incorrect setting of this field will be reported via STATUS register 0h = No 256-bit keys 1h = One 256-bit key 2h = Two 256-bit keys 3h = Three 256-bit keys 4h = Four 256-bit keys

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2 KEYWR Register (Offset = 1104h) [Reset = 00000000h]

KEYWR is shown in Figure 9-2 and described in Table 9-5.

Return to the Summary Table.

Register to configure a key write operation

Figure 9-2. KEYWR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
KEYSLOTSEL				RESERVED	KEYSZSEL		
R/W-0h				R/W-0h	R/W-0h		

Table 9-7. KEYWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-4	KEYSLOTSEL	R/W	0h	Select the key slot to write the key into. NOTE: SW needs to ensure that it is writing to the correct slots. The slot numbering is from 0 through SYS_N_SLOTS-1. Each slot is a 128-bit slot. Therefore, when writing a 256-bit key, two slots will need to budgeted. The selected slot for the 256-bit key needs to be an even numbered slot (eg: 0 or 2). Also all the 256-bit keys need to be stored in lower numbered slots and 128-bit keys stored in higher numbered slots. 0h = Slot 0 1h = Slot 1 2h = Slot 2 3h = Slot 3 4h = Slot 4 5h = Slot 5 6h = Slot 6 7h = Slot 7
3	RESERVED	R/W	0h	
2-0	KEYSZSEL	R/W	0h	Key size selection. Selection of 128 or 256 bit keys 0h = 256 bit key 1h = 128 bit key

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3 KEYRD Register (Offset = 1108h) [Reset = 00000000h]

KEYRD is shown in Figure 9-3 and described in Table 9-6.

Return to the Summary Table.

Register to configure a key transfer operation - transfer from keystore into a crypto engine

Figure 9-3. KEYRD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						CRYPTOSEL	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
KEYSLOTSEL				RESERVED		KEYSZSEL	
R/W-0h				R/W-0h		R/W-0h	

Table 9-9. KEYRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9-8	CRYPTOSEL	R/W	0h	Crypto engine selector
7-4	KEYSLOTSEL	R/W	0h	Select the key slot to read the key from. NOTE: SW needs to ensure that it is reading from the correct slots. The slot numbering is from 0 through SYS_N_SLOTS-1. Each slot is a 128-bit slot. Therefore, when reading a 256-bit key, two adjacent slots will be read. For a 256-bit key, an even numbered slot index must be specified.
3	RESERVED	R/W	0h	
2-0	KEYSZSEL	R/W	0h	Key size selection. Selection of 128 or 256 bit keys 0h = 256 bit key 1h = 128 bit key

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4 STATUS Register (Offset = 110Ch) [Reset = 00020001h]

STATUS is shown in Figure 9-4 and described in Table 9-7.

Return to the Summary Table.

Status register

Figure 9-4. STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						NKEYSLOTS	
R-0h						R-2h	
15	14	13	12	11	10	9	8
RESERVED				VALID			
R-0h				R-0h			
7	6	5	4	3	2	1	0
VALID				STAT			
R-0h				R-1h			

Table 9-11. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17-16	NKEYSLOTS	R	2h	Size of keystorage: Number of 128-bit key slots 0h = Two slots 1h = Three slots 2h = Four slots
15-12	RESERVED	R	0h	
11-4	VALID	R	0h	Bitvector of valid bits to indicate which slots have been configured
3-0	STAT	R	1h	Status information 0h = Valid configuration 1h = Key-store has not been configured. NK256 has not been set. 2h = Invalid value for NK256 field in CFG. 3h = Busy receiving a key deposit 4h = Busy transmitting a key to a crypto engine 5h = Invalid keyslot selection for writing 6h = Invalid keyslot selection for reading

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5 KEYIN Register (Offset = 1110h) [Reset = 00000000h]

KEYIN is shown in Figure 9-5 and described in Table 9-8.

Return to the Summary Table.

Write 32-bit key value by writing to this register. This is not readable.

Figure 9-5. KEYIN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 9-13. KEYIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	32-bit key data

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6 KEYLOCK Register (Offset = 1114h) [Reset = 00000000h]

KEYLOCK is shown in Figure 9-6 and described in Table 9-9.

Return to the Summary Table.

Writing 1 to this will lock the key access to the particular one hot encoded slot

Figure 9-6. KEYLOCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LOCKBIT							
R/W-0h																								R/W-0h							

Table 9-15. KEYLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	LOCKBIT	R/W	0h	Bitvector of lock bits to lock certain slots from being used by application.

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Chapter 10

Cyclic Redundancy Check (CRC)

The cyclic redundancy check (CRC) accelerator generates signatures for a given data sequence based on the CRC16-CCITT polynomial and CRC32-ISO3309 polynomial.

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10.1 CRC Overview

The CRC-P accelerator produces CRC signatures for given sequences of data. The CRC16-CCITT and CRC32-ISO3309 polynomial functions are supported. Identical input data sequences result in identical CRC signatures when the CRC is initialized with a fixed seed value. Different sequences of input data, in general, result in different signatures for a given CRC function.

Table 10-1. CRC-P Key Features

Feature	CRC-P
Support for CRC16-CCITT	✓
Support for CRC32-ISO3309 Polynomial	✓
Fast single cycle computation of new CRC output for each data input (no wait states)	X
Support for input / output bit reversal	✓
Support for big endian and little endian operation	✓
Byte, Half-word, or word input to CRCIN	✓
512-word CRCIN_IDX input field in which all addresses are mapped to CRCIN, supporting use of a standard C-style memcpy() routine to load data into the CRC module for data lengths up to 2KB	✓
User-selectable CRC32 polynomial	✓

10.1.1 CRC16-CCITT

For CRC16-CCITT, the CRC signature is generated based on the polynomial given in the 16-bit CCITT standard, as shown in the equation below.

$$f(x)=x^{16}+x^{12}+x^{5}+1 \quad (10)$$

The CRC16-CCITT digest size is 16 bits (half-word).

10.1.2 CRC32-ISO3309

For CRC32-ISO3309, the CRC signature is generated based on the polynomial given in the ISO3309 Ethernet standard, as shown in the equation below.

$$f(x)=x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1 \quad (11)$$

The digest size for CRC32-ISO3309 is 32 bits.

10.2 CRC Operation

The CRC generator is initialized by configuring the desired mode of operation in the CRCCTRL register, followed by writing the seed value to the CRCSEED register. After the seed is loaded to the CRCSEED register, the CRCOUT register will reflect the SEED value loaded to CRCSEED.

Note

If the endianness mode is configured to big endian before the seed value is written to CRCSEED, then the byte order of the seed value written to CRCSEED is swapped when the seed value is loaded into the CRC module.

Once initialized, data can be input into the CRC generator by writing to the CRCIN register using byte (8-bit), half-word (16-bit), or word (32-bit) writes. The CPU or the DMA can be used to move input data into the CRC accelerator.

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Note

Byte writes need not be word aligned; a byte write to any byte location in CRCIN will be interpreted the same way (adding the 8 written bits to the computed CRC). Half-word writes also need not be word aligned, but they must be half-word aligned. For example, a half-word can be written to BIT0-BIT15 or BIT16-BIT32 of CRCIN, but not to BIT8-BIT23.

When using the CRC generator to verify a data set, all data to be included in the CRC calculation must be written to the CRCIN register in the same order as was used to calculate the original CRC signature. When using the CRC generator to create a new signature to be used in the future for verification, be sure to load the data the same way and with the same settings when performing verification.

The current CRC output can be read at any time by reading the CRCOUT register.

10.2.1 CRC Generator Implementation

The CRC generator is implemented with a set of XOR trees. After a set of 8, 16, or 32 bits is provided to the CRC accelerator by writing to the CRCIN register, a calculation for the whole set of input bits is performed. When new data is written to CRCIN, the CRC generator updates the CRC output in a single cycle when using the CRC peripheral. CRC-P versions require additional cycles. Bus wait states are not required to load data back-to-back into the CRC generator.

10.2.2 Configuration

The CRC accelerator supports polynomial selection, bit reversal selection, and byte order (endianness) selection. This section describes these configuration aspects.

The CRC accelerator must be enabled before being used through the PWREN register (see peripheral power enable).

The CRC accelerator is in power domain 1 (PD1), and as such can only be active in RUN or SLEEP mode. If the CRC accelerator is configured to be enabled by application software, and the device enters STOP or STANDBY mode, SYSCTL forces the CRC into a disabled state until the device exists STOP or STANDBY mode. All CRC register contents are retained when the CRC is forced to a disabled state in STOP or STANDBY mode.

The CRC module only runs from the PD1 bus clock (MCLK).

10.2.2.1 Polynomial Selection

The desired polynomial (CRC16-CCITT or CRC32-ISO3309) is selected with the POLYSIZE bit in the CRCCTRL register. The polynomial to be used must be selected before loading the seed value and any data values.

When the CRC generator is configured for a 16-bit digest (CRC16-CCITT), the following conditions apply:

- The upper half-word (16 bits) of the CRCSEED register are ignored and only the lower half-word is used
- The upper half-word (16 bits) of the CRCOUT register read back as zero and only the lower half-word is valid

When the CRC generator is configured for CRC32-ISO3309, all 32 bits of CRCSEED and CRCOUT are valid.

10.2.2.2 Bit Order

The various CRC standards were defined in the era of main frame computers. At that time, BIT0 was treated as the MSB. In modern computing, BIT0 is typically the LSB.

The Arm Cortex-M33 CPU treats BIT0 as the LSB, as is typical in modern CPUs and MCUs. This sometimes causes confusion, because BIT0 has been treated as the LSB in some cases and as the MSB in other cases. Therefore, the CRC accelerator provides a bit order reversal capability to support both conventions.

Bit order reversal can be enabled by setting the BITREVERSE bit in the CRCCTRL register, giving the following behavior for input and output data:

- **Input data:** The bit order of each input byte written to the CRCIN register is reversed before it is passed to the CRC generator to be used for CRC calculation

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- **Output data:** The bit order of the 16-bit or 32-bit CRC result is reversed when read from the CRCOUT register

Note

If input data must be provided bit-reversed, but the output is to be read not reversed, the BITREVERSE bit can be set before loading data to CRCIN and then cleared after all data is written to CRCIN but before the resulting signature is read from CRCOUT. Likewise, it is possible to load input data to CRCIN with BITREVERSE cleared (not reversed), and flip the output before reading it (by setting BITREVERSE before reading CRCOUT).

10.2.2.3 Byte Swap

The bit OUTPUT_BYTESWAP in the register CRCCTRL can be used to enable or disable CRC output byte swap. This bit controls whether the output is byte-swapped upon a read of the CRCOUT register. If CRCOUT is accessed as a half-word, and the OUTPUT_BYTESWAP is set to 1, then the two bytes in the 16-bit access are swapped and returned. Using B0, B1, B2 and B3 to identify Byte 0, Byte 1, Byte 2, Byte 3. B1 is returned as B0 and B0 is returned as B1. If CRCOUT is accessed as a word, and the OUTPUT_BYTESWAP is set to 1, then the four bytes in the 32-bit read are swapped. B3 is returned as B0, B2 is returned as B1, B1 is returned as B2 and B0 is returned as B3.

Note that if the CRC POLYSIZE is 16-bit and a 32-bit read of CRCOUT is performed with OUTPUT_BYTESWAP enabled, then the output is: MSB LSB 0x0 0x0 B0 B1. If the CRC POLYSIZE is 16-bit and a 32-bit read of CRCOUT is performed with OUTPUT_BYTESWAP disabled, then the output is: MSB LSB 0x0 0x0 B1 B0.

10.2.2.4 Byte Order

When working with half-word or word input data, the input byte order can be configured as either little endian or big endian. The default configuration is little endian. To reverse the byte order when using half-word or word inputs, set the INPUT_ENDIANNESS bit in the CRCCTRL register.

Reversing the endianness will cause the following translation for half-word and word writes:

Table 10-2. CRCIN Byte Order Translation

Endianness	Data Written to CRCIN	Data Applied to CRC Logic
0 (little)	0x1234	0x1234
1 (big)	0x1234	0x3412
0 (little)	0x12345678	0x12345678
1 (big)	0x12345678	0x78563412

Note

If the ENDIANNESS bit is set before the seed value is written to CRCSEED, then the byte order of the seed value written to CRCSEED is also reversed when it is loaded into the CRC, and the seed value will read back reversed when reading the CRCOUT register after writing to the CRCSEED register.

10.2.2.5 CRC C Library Compatibility

To simplify loading of data by software into the CRC, the CRC accelerator provides a 512-word (2KB) CRCIN_IDX region. Within the CRCIN_IDX region, a write to any word is re-mapped as, and functionally equivalent to, a write to the CRCIN register. This mechanism enables the use of the standard C library *memcpy()* routine to copy data from SRAM or flash into the CRC, provided that the source data is less than 2KB (2,048 bytes).

10.3 CRC Registers

This Section describes the CRC Registers.

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10.3.1 CRC Base Address Table

Table 10-3. CRC Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
CrcRegs	CRCP_REGS	CRC	0x401B_2000

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10.3.2 CRCP_REGS Registers

Table 10-4 lists the memory-mapped registers for the CRCP_REGS registers. All register offset addresses not listed in Table 10-4 should be considered as reserved locations and the register contents should not be modified.

Table 10-4. CRCP_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1004h	CLKSEL	Clock Select		Go
10FCh	DESC	Module Description		Go
1100h	CRCCTRL	CRC Control Register		Go
1104h	CRCSEED	CRC Seed Register		Go
1108h	CRCIN	CRC Input Data Register		Go
110Ch	CRCOUT	CRC Output Result Register		Go
1110h	CRCPOLY	CRC Polynomial configuration register		Go
1800h + formula	CRCIN_IDX_y	CRC Input Data Array Register		Go

Complex bit access types are encoded to fit into small table cells. Table 10-5 shows the codes that are used for access types in this section.

Table 10-5. CRCP_REGS Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 10-1 and described in Table 10-6.

Return to the Summary Table.

Register to control the power state

Figure 10-1. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 10-7. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 10-2 and described in Table 10-7.

Return to the Summary Table.

Register to control reset assertion and de-assertion

Figure 10-2. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 10-9. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 10-3 and described in Table 10-8.

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peripheral enable and reset status

Figure 10-3. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 10-11. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 CLKSEL Register (Offset = 1004h) [Reset = 00000001h]

CLKSEL is shown in Figure 10-4 and described in Table 10-9.

Return to the Summary Table.

Clock source selection

Figure 10-4. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MCLK_SEL
R-0h							R-1h

Table 10-13. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	MCLK_SEL	R	1h	Selects main clock (MCLK) if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source

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5 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 10-5 and described in Table 10-10.

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This register identifies the peripheral and its exact version.

Figure 10-5. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				INSTNUM				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 10-15. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	2011h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	8h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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6 CRCCTRL Register (Offset = 1100h) [Reset = 00000000h]

CRCCTRL is shown in Figure 10-6 and described in Table 10-11.

Return to the Summary Table.

CRC Control Register. Configuration control of the CRC.

Figure 10-6. CRCCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			OUTPUT_BYTESWAP	RESERVED	INPUT_ENDIANNESS	BITREVERSE	POLYSIZE
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 10-17. CRCCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	OUTPUT_BYTESWAP	R/W	0h	CRC Output Byteswap Enable. This bit controls whether the output is byte-swapped upon a read of the CRCOUT register. If CRCOUT is accessed as a half-word, and the OUTPUT_BYTESWAP is set to to 1, then the two bytes in the 16-bit access are swapped and returned. B1 is returned as B0 B0 is returned as B1 If CRCOUT is accessed as a word, and the OUTPUT_BYTESWAP is set to 1, then the four bytes in the 32-bit read are swapped. B3 is returned as B0 B2 is returned as B1 B1 is returned as B2 B0 is returned as B3 Note that if the CRC POLYSIZE is 16-bit and a 32-bit read of CRCOUT is performed with OUTPUT_BYTESWAP enabled, then the output is: MSB LSB 0x0 0x0 B0 B1 If the CRC POLYSIZE is 16-bit and a 32-bit read of CRCOUT is performed with OUTPUT_BYTESWAP disabled, then the output is: MSB LSB 0x0 0x0 B1 B0 0h = Output byteswapping is disabled 1h = Output byteswapping is enabled.
3	RESERVED	R/W	0h	
2	INPUT_ENDIANNESS	R/W	0h	CRC Endian. This bit indicates the byte order within a word or half word of input data. 0h = LSB is lowest memory address and first to be processed. 1h = LSB is highest memory address and last to be processed.

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Table 10-17. CRCCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BITREVERSE	R/W	0h	CRC Bit Input and output Reverse. This bit indictes that the bit order of each input byte used for the CRC calculation is reversed before it is passed to the generator, and that the bit order of the calculated CRC is be reversed when read from CRC_RESULT. 0h = Bit order is not reversed. 1h = Bit order is reversed.
0	POLYSIZE	R/W	0h	This bit indicates which CRC calculation is performed by the generator. 0h = CRC-32 ISO-3309 calulation is performed 1h = CRC-16 CCITT is performed

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7 CRCSEED Register (Offset = 1104h) [Reset = 00000000h]

CRCSEED is shown in Figure 10-7 and described in Table 10-12.

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CRC Seed Register. The Data written to this register is used to initialize the CRC result with this SEED value. Note that in 16-bit mode only the lower 16-bits of this value are used. After writing this register the CRC Output Result Register will reflect this value.

Figure 10-7. CRCSEED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEED																															
W-0h																															

Table 10-19. CRCSEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEED	W	0h	Seed Data 00000000h = Mnimum value FFFFFFFFh = Maximum value

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8 CRCIN Register (Offset = 1108h) [Reset = 00000000h]

CRCIN is shown in Figure 10-8 and described in Table 10-13.

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CRC Input Data Register. The Data writen to this register is used along with the current CRC result to calculate the next CRC result. This is done in a single clock cycle and requires no wait states. This register can by written as a byte, half word or word transfer and the correct number of bits will be used for the next CRC result.
This register is also mapped to a range of registers starting at 0xTDB_X000 and ending at 0xTDB_XFFF to allow memcpy to be used instead of DMA for CRC calculations that do not exceed the bounds of the memory range of this register.

Figure 10-8. CRCIN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

Table 10-21. CRCIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Input Data 00000000h = Mnimum value FFFFFFFFh = Maximum value

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9 CRCOUT Register (Offset = 110Ch) [Reset = 00000000h]

CRCOUT is shown in Figure 10-9 and described in Table 10-14.

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CRC Output Result Register. This register stores the result of the currect CRC calculation. Note when configured for 16-bit mode the upper bits will read back 0. Note that if output inversion is set in the CRC Control register it will be applied.

Figure 10-9. CRCOUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULT																															
R-0h																															

Table 10-23. CRCOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESULT	R	0h	Result 00000000h = Mnimum value FFFFFFFFh = Maximum value

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10 CRCPOLY Register (Offset = 1110h) [Reset = 00000000h]

CRCPOLY is shown in Figure 10-10 and described in Table 10-15.

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CRC Polynomial configuration register

Figure 10-10. CRCPOLY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
-0																															

Table 10-25. CRCPOLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	04C11DB7h	Polynomial definition	

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11 CRCIN_IDX_y Register (Offset = 1800h + formula) [Reset = 00000000h]

CRCIN_IDX_y is shown in Figure 10-11 and described in Table 10-16.

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This register is dual mapped to CRCIN and is intended to allow operation with C memcpy routine.

Offset = 1800h + (y * 4h); where y = 0h to 1FFh

Figure 10-11. CRCIN_IDX_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
HW-0h																															

Table 10-27. CRCIN_IDX_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	HW	0h	Input Data 00000000h = Minimum value FFFFFFFFh = Maximum value

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Chapter 11

Direct Memory Access (DMA)

The direct memory access (DMA) module transfers data from one address to another, without CPU intervention. This chapter describes the operation of the DMA module.

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11.1 DMA Overview

The DMA transfers data from a source address to a destination address without CPU intervention across a set of independently configurable channels. It does so by receiving an interrupt, or trigger through hardware or software to initiate a data transfer. The DMA can be used to transfer data to or from memory blocks, and transfer data to or from various peripherals.

AM13E232x devices support 12 DMA channels separated into 6 BASIC and 6 FULL_FEATURE channels. Each channel can be configured for various data sizes, transfer modes, addressing modes, and triggers.

Using the DMA controller can increase the throughput of peripheral modules. It can also reduce system power consumption by allowing the CPU to remain in a low-power mode, without having to awaken to move data to or from a peripheral.

DMA controller features include:

- Up to 12 independent transfer channels
- Byte (8-bit), half-word (16-bit), word (32-bit), long-word (64-bit), and long-long-word (128-bit) or mixed byte and word transfer capability
- Single or block transfer modes
- Seven flexible addressing modes
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Configurable DMA channel priorities
- DMA trigger support in various operating modes

The DMA controller block diagram is shown in Figure 11-1.

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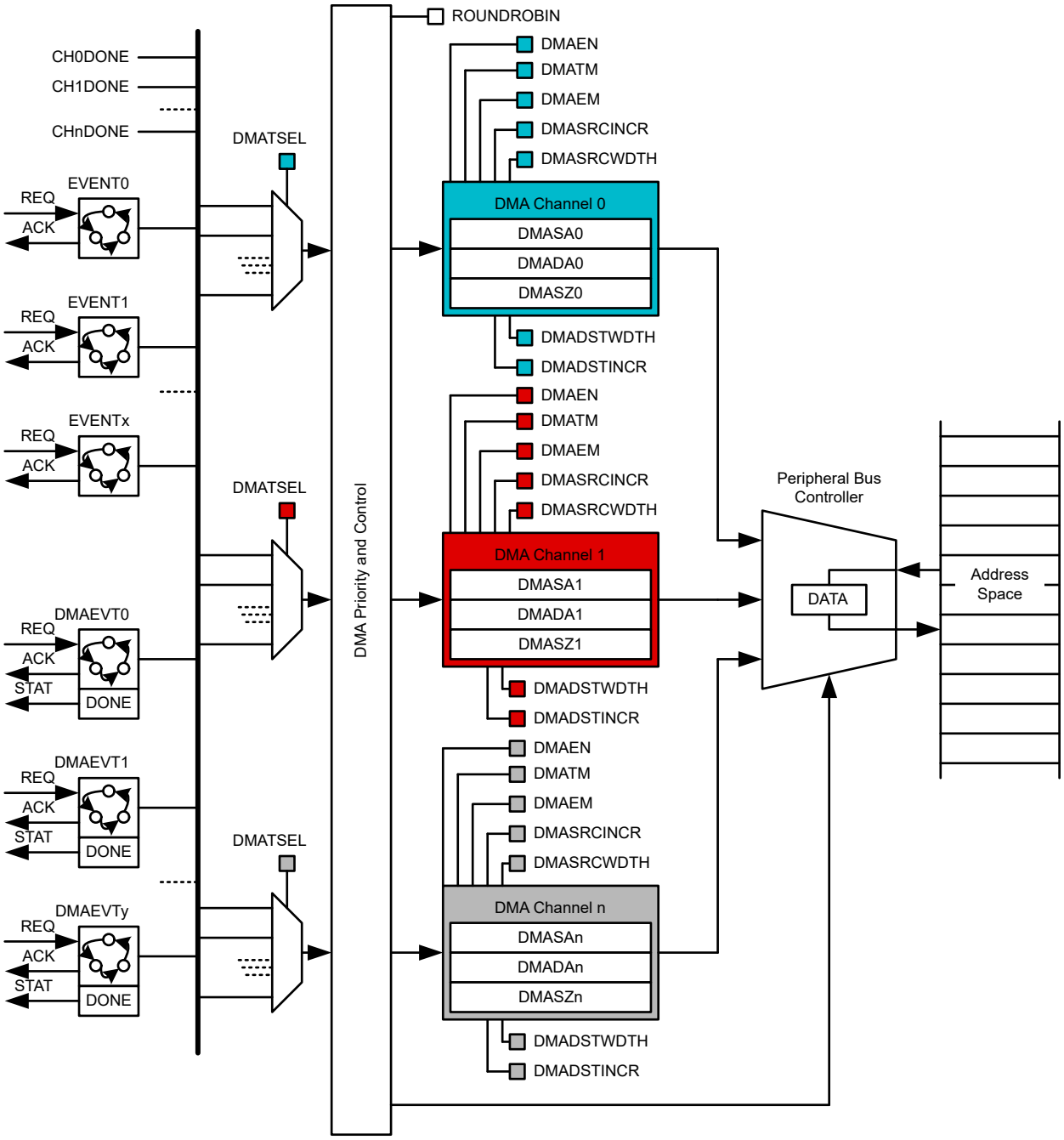


Figure 11-1. DMA Block Diagram

Note

The left portion of the above diagram may vary for different peripherals. The ACK and STATUS signals are only returned to peripherals that have a DMA_DONE interrupt inside their registers (for example UNICOMM peripherals).

11.2 DMA Operation

For each DMA channel, the DMA controller utilizes a source address pointer (DMASA), a destination address pointer (DMADA), and a transfer counter (DMASZ). After the DMA channel is configured, the channel must be enabled by setting the DMA_CTL.DMAEN bit to begin transfers. With each transfer, the DMA reads a data

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element from the source and writes the element at the destination. After the transfer, the source and the destination addresses are updated based on the source increment (DMASRCINCR) and destination increment (DMADSTINCR) registers, and the DMASZ is decremented. The DMA loops through this cycle until the DMASZ reaches zero, at which point the DMA channel generates a raw interrupt status (RIS) flag.

The full setup and operation of the DMA is discussed in the following sections.

11.2.1 Channel Types

The DMA module has **six** channels supporting basic (BASIC) features and **six** channels with full-featured (FULL) support. BASIC channels support only single or block transfers, and FULL channels additionally support repeated single transfers, repeated block transfers, and features such as early interrupt request generation and extended table, fill, and gather modes.

The highest priority DMA channels, (DMA0 - DMA5) are FULL channels, and the remaining lower priority channels are BASIC channels (DMA6 - DMA11).

Table 11-1 shows the features supported in the available basic and full-feature DMA channel types.

Table 11-1. Feature Comparison of BASIC and FULL Channels

DMA Feature	Full-Feature	Basic Channel
Single/Block transfer mode	✓	✓
Repeated transfer mode	✓	–
Block burst mode	✓	✓
4 Addressing modes	✓	✓
Stride mode	✓	✓
Extended modes	✓	–
Early IRQ notification	✓	–
Auto enable	✓	✓
Configurable Trigger Selection	✓	✓
Cascading channel support	✓	✓

11.2.2 Channel Priorities

The default DMA channel priorities are that DMA0 is highest priority, DMA1 has the second highest priority, etc., down to DMA11 which has the lowest default priority. If two or three triggers happen simultaneously or are pending, the channel with the highest priority completing the transfer (single or block transfer) first, then the second highest priority channel, then the third priority channel and so on. Transfers in progress are not halted if a higher-priority channel is triggered. The higher-priority channel waits until the transfer in progress completes before starting.

The DMA channel priorities are configurable with the ROUNDROBIN bit of the DMAPRIO register. When the ROUNDROBIN bit is set, the channel that completes a transfer becomes the lowest priority. The order of the priority of the channels always stays the same, DMA0-DMA1-DMA2, for example, for three channels. When the ROUNDROBIN bit is cleared, the channel priority returns to the default priority.

Table 11-2. Round-Robin DMA Priority Example Using 3 DMA Channels

Current DMA Priority	Transfer Occurs	New DMA Priority
DMA0 - DMA1 - DMA2	DMA1	DMA2 - DMA0 - DMA1
DMA2 - DMA0 - DMA1	DMA2	DMA0 - DMA1 - DMA2
DMA2 - DMA0 - DMA1	DMA0	DMA1 - DMA2 - DMA0

11.2.3 Initiating DMA Transfers

To begin a transfer, the DMA controller requires a trigger. Each DMA channel is independently configured for a specific trigger source within the correlating DMA trigger control registers.

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Note

The trigger control registers must be modified only when the DMA channel is disabled, otherwise unpredictable DMA triggers can occur.

The DMA can be configured for either an external trigger or an internal channel trigger via the DMATINT bits of the DMA Trigger Select register (DMATCTL). The DMATSEL bits then configure the exact trigger. See Section 11.2.3.1 for the list of external triggers available, along with the respective DMATSEL values. When configuring for an internal channel trigger, the DMATSEL bits must be set to the desired DMA channel index.

Note

The recommended software initialization sequence is to configure the DMA channel trigger source before the triggering peripheral is enabled to avoid triggering the DMA before the channel is fully configured. For DMA channels configured with DMA_TRIG_RX trigger sources, clear the RX FIFO of the UNICOMM before enabling or re-enabling the DMA channel.

When an enabled DMA channel receives a trigger from it's trigger source, the DMA controller begins execution of the data transfer. For both trigger types, completion of activity occurs when a DMA channel's size (DMASZ) counter reaches zero.

11.2.3.1 DMA Trigger Source Options

The below are the trigger options available for the DMATCTL.DMATSEL field on the AM13E232x.

Table 11-3. DMA Trigger Source Options

Select Index	Trigger Source
0	DMA_SOFTWARE_TRIGGER
1	ADC0_DMA_TRIG1
2	ADC0_DMA_TRIG2
3	ADC0_DMA_TRIG3
4	ADC0_DMA_TRIG4
5	ADC1_DMA_TRIG1
6	ADC1_DMA_TRIG2
7	ADC1_DMA_TRIG3
8	ADC1_DMA_TRIG4
9	ADC2_DMA_TRIG1
10	ADC2_DMA_TRIG2
11	ADC2_DMA_TRIG3
12	ADC2_DMA_TRIG4
13	MCPWM0_SOCA
14	MCPWM0_SOCB
15	MCPWM0_SOCC
16	MCPWM0_SOCD
17	MCPWM1_SOCA
18	MCPWM1_SOCB
19	MCPWM1_SOCC
20	MCPWM1_SOCD
21	MCPWM2_SOCA

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Table 11-3. DMA Trigger Source Options (continued)

Select Index	Trigger Source
22	MCPWM2_SOCB
23	MCPWM2_SOCC
24	MCPWM2_SOCD
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Reserved
33	Reserved
34	TIMG4.GEN_EVENT1
35	Reserved
36	TIMG12.GEN_EVENT1
37	AES.INT_EVENT1
38	AES.INT_EVENT2
39	ECAP0DMA
40	ECAP1DMA
41	GPIO0.GEN_EVENT0
42	GPIO0.GEN_EVENT1
43	GPIO1.GEN_EVENT0
44	GPIO1.GEN_EVENT1
45	GPIO2.GEN_EVENT0
46	GPIO2.GEN_EVENT1
47	GPIO3.GEN_EVENT0
48	GPIO3.GEN_EVENT1
49	ECAP2DMA
50	FSITXA_DMA_ALT
51	FSIRXA_DMA_ALT
52	NPU
53	EPWM0_SOCA
54	EPWM0_SOCB
55	EPWM1_SOCA
56	EPWM1_SOCB
57	EPWM2_SOCA
58	EPWM2_SOCB

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Table 11-3. DMA Trigger Source Options (continued)

Select Index	Trigger Source
59	EPWM3_SOCA
60	EPWM3_SOCB
61	EPWM4_SOCA
62	EPWM4_SOCB
63	EPWM5_SOCA
64	EPWM5_SOCB
65	SDDRINT1
66	SDDRINT2
67	SDDRINT3
68	SDDRINT4
69	FSITX_DMA
70	FSIRX_DMA
71	FSIRX_DATA_TAG_MATCH
72	FSIRX_PING_TAG_MATCH
73	ECAT_SYNC_DMA_TRIG
74	UNICOMM0.DMA_TRIG_TX
75	UNICOMM0.DMA_TRIG_RX
76	UNICOMM1.DMA_TRIG_TX
77	UNICOMM1.DMA_TRIG_RX
78	UNICOMM2.DMA_TRIG_TX
79	UNICOMM2.DMA_TRIG_RX
80	UNICOMM3.DMA_TRIG_TX
81	UNICOMM3.DMA_TRIG_RX
82	UNICOMM4.DMA_TRIG_TX
83	UNICOMM4.DMA_TRIG_RX
84	UNICOMM5.DMA_TRIG_TX
85	UNICOMM5.DMA_TRIG_RX

11.2.3.2 Cascading DMA Channels

DMA channels can be internally triggered upon the completion of activity on another DMA channel to support cascading. This is beneficial for applications where data can be retrieved, transferred, and/or error-checked without an interrupt or event configuration.

For example, if UART data is received and transmitted to SRAM through DMA channel 0 and DMATSEL is set to UART RX, then DMA channel 1 can be internally triggered when the UART is finished receiving data. If DMA channel 1 is configured to transmit the data from SRAM to CRC, then the DMA transfer will trigger once the UART data is received. In this case, the DMA channels are cascaded from Channel 0 to Channel 1.

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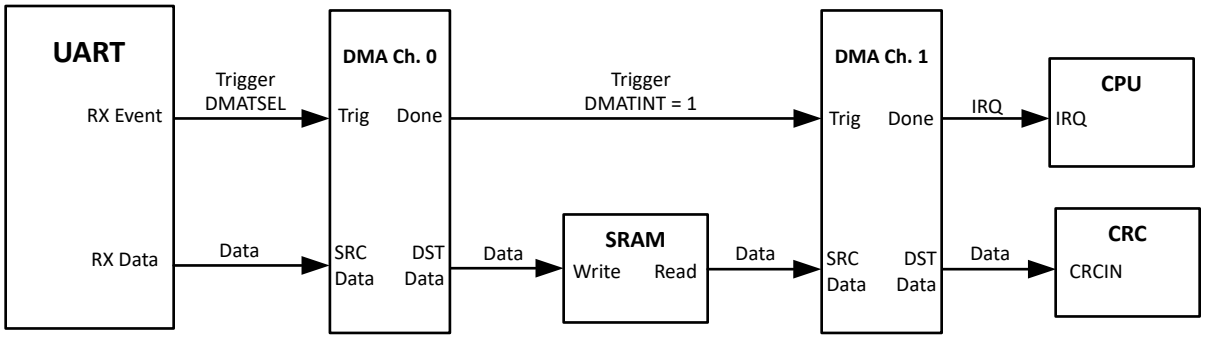


Figure 11-2. DMA Cascading Channels

11.2.4 Transfer Modes

The DMA has four transfer modes that are selected by the transfer mode (DMATM) bits in the DMA channel control registers. These transfer modes are listed in Table 11-4. The transfer mode of each channel is individually configurable. For example, channel 0 can be configured in repeated block transfer mode, while channel 1 is configured for block transfer mode, and channel 2 operates in single transfer mode. The transfer mode (single, block, repeat) is configured independently from the addressing mode (decrement, fixed, increment, stride). Any addressing mode can be used with any transfer mode.

The five types of data that can be transferred are selectable by the destination width (DMADSTWDTH) and source width (DMASRCWDTH) control bits. The source and destination locations can be either byte (8-bit), half-word (16-bit), word (32-bit), long-word (64-bit), or long-long-word (128-bit) data. Transfers can be byte to byte, half-word to half-word, word to word, long-word to long-word, long-long-word to long-long-word or any combination of the five. When transferring a wider bit width source to a shorter bit width destination, only the lower bits of the destination data transfers. When transferring a shorter bit width source to a wider bit width destination, the upper bytes of the destination data is cleared when the transfer occurs. There is no packing or unpacking support by combining several source byte transfers to one single destination word or the reverse.

Note

When doing long-word (64-bit) or long-long-word (128-bit) data transfers, software must ensure proper alignment of source and destination addresses.

Table 11-4. DMA Transfer Modes

DMATM	Transfer Mode	Description	Channel Type
0	Single transfer	Each transfer requires a trigger. DMAEN is automatically cleared when DMASZ transfers have been made.	Basic or Full-Feature
1	Block transfer	A complete block of individual single transfers is transferred with one trigger. DMASZ is equal to the block size (in amount of single transfers) and decrements after each single transfer of data. DMAEN is automatically cleared at the end of the block transfer (when DMASZ = 0).	Basic or Full-Feature
2	Repeated single transfer	Each transfer requires a trigger. The DAMSA, DMADA and DMASZ registers are reloaded to the original value when the DMASZ counted down to zero. DMAEN remains enabled.	Full-feature
3	Repeated block transfer	A complete block is transferred with one trigger and continuous transferring. The DAMSA, DMADA and DMASZ registers are reloaded to the original value when the DMASZ counted down to zero. DMAEN remains enabled.	Full-feature

11.2.4.1 Single Transfer

In single transfer mode (DMATM = 0), each byte, half-word, word, long-word, or long-long-word transfer requires a separate trigger.

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The DMASZ register defines the number of transfers to be made. The DMADSTINCR and DMASRCINCR bits select if the destination address and the source address's are incremented or decremented after each transfer. If DMASZ = 0, no transfers occur. The DMASA and DMADA registers are incremented or decremented after each transfer. DMASZ is decremented after each transfer. The DMADSTWDTH indicates whether the destination address increments or decrements by 1, 2, 4, 8, or 16 with each transfer cycle. The same is true for the DMASRCWDTH and the source address respectively. When the DMASZ register decrements to zero, the RIS.DMACHx flag is set.

The DMAEN bit is cleared automatically when DMASZ decrements to zero and must be set again for another transfer to occur.

11.2.4.2 Block Transfer

In block transfer mode (DMATM = 1), a transfer of a complete block of data occurs after one trigger.

The DMASZ register defines the size of the block in the number of single transfers of the specified data type, and the DMADSTINCR and DMASRCINCR bits select if the destination address and the source address are incremented or decremented after each transfer of the block. The DMA is done transferring the block once DMASZ = 0, which sets the corresponding RIS.DMACHx flag. The DMADSTWDTH indicates whether the destination address increments or decrements by 1, 2, 4, 8 or 16 with each transfer cycle. The same is true for the DMASRCWDTH and the source address respectively. The DMASZ register is decremented after each transfer of one data type and shows the number of single transfers remaining.

The DMAEN bit is cleared after the completion of the block transfer and must be set again before another block transfer can be triggered. After a block transfer has started, any other trigger signal that occurs during the block transfer is ignored until the block transfer is complete.

11.2.4.3 Repeated Single Transfer

Repeated single transfer mode is only available in FULL feature DMA channels.

In repeated single transfer mode (DMATM = 2), the DMA controller remains enabled with DMAEN = 1, and a transfer occurs every time a trigger occurs.

The DMASA, DMADA, and DMASZ registers are copied into internal hidden registers. The values of DMASA and DMADA are incremented or decremented after each transfer. The DMASZ register is decremented after each transfer. The DMADSTWDTH indicates whether the destination address increments or decrements by 1, 2, 4, 8 or 16 with each transfer cycle. The same is true for the DMASRCWDTH and the source address respectively. When the DMASZ register decrements to zero, the intialized value is reloaded from an internal register and the corresponding RIS.DMACHx flag is set. The DMA channel remains enabled and waits for another trigger before starting the next transfer.

Note

When using repeated single transfer mode, the DMA does not support pausing and continuing a transfer by disabling a channel (to pause) and then re-enabling the channel (to continue).

11.2.4.4 Repeated Block Transfer

Repeated block transfer mode is only available in FULL feature DMA channels.

In repeated block transfer mode (DMATM = 3), the DMAEN bit remains set after completion of the block transfer. The next trigger after the completion of a repeated block transfer starts another block transfer.

The DMASA, DMADA, and DMASZ registers are copied into internal hidden registers. The temporary values of DMASA and DMADA are incremented or decremented after each transfer in the block. The DMADSTWDTH indicates whether the destination address increments or decrements by 1, 2, 4, 8 or 16 with each transfer cycle. The same is true for the DMASRCWDTH and the source address respectively. The DMASZ register is decremented after each transfer of the block and shows the number of transfers remaining in the block. When the DMASZ register decrements to zero, the initialized value is reloaded from an internal register and the

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corresponding RIS.DMACHx flag is set. The DMA channel remains enabled and waits for another trigger before starting the next transfer.

11.2.4.5 Burst Block Mode

By default, once a block transfer begins, the DMA does not service any other incoming triggers until the transfer-in-progress is complete. In the case of larger block transfers, this can cause a delay in servicing higher priority channels. As such, the DMA module supports a burst block mode for suspending an active channel after a configurable number of transfers to service other pending channels. The burst block size is configurable by setting DMAPRIO.BURSTSZ to 8, 16, 32, or an infinite number of transfers (essentially the full block size). When using Burst Block mode, the DMA will pause an in-progress block transfer after the configured burst block size and check for pending triggers. If a higher priority channel is pending after the burst block, the DMA will execute the higher priority channel and resume on the suspended channel once the higher priority channel is complete. If no other channel is pending, the priority logic assigns the control back to the original block transfer for the next burst.

11.2.5 Pausing DMA Transfers

A DMA block transfer in progress can be paused by clearing the DMAEN bit. The DMA stops after the completion of the ongoing transfer cycle and all the channel registers stay in the current state during a channel pause. The block transfer can be continued as originally configured after setting the DMAEN bit again and resending the trigger. Please note that an additional trigger is necessary for halted transfer to resume.

Note

A single transfer in progress cannot be interrupted.

11.2.6 DMA Transfer Status

For certain peripherals on the AM13E232x, the DMA can inform the triggering peripheral about the status of the assigned DMA channel. This will allow the triggering peripheral to issue an interrupt itself after the completion of a repeated transfer, instead of the DMA issuing an interrupt event. The advantage is that the DMA interrupt service routine does not need to keep track of the assigned function of the channel and instead leaves that to the triggering peripheral's own interrupt service routine. The below are the peripherals that support DMA end-of-transfer interrupts within the triggering peripheral itself.

- UNICOMM-UART
- UNICOMM-SPI
- UNICOMM-I2CC / UNICOMM-I2CT

The DMA status sent to the triggering peripheral will reflect the value of the DMASZ register. If the last DMA transfer resulted in a size decrement to zero, the DMA will return the status of 1, indicating the end of the transfer. Otherwise the status will be 0.

Additionally, for FULL channels, the DMA module can generate an early interrupt request (pre-IRQ) to the CPU to indicate that a transfer will complete within a configurable number of transfers (1, 2, 4, 8, 32, 64, half-DMASZ). An early IRQ event is enabled by setting the DMAPREIRQ bits of the channel control register to the desired number of transfers. When the DMA has reached the number of transfers, the corresponding DMA channel’s PREIRQ interrupt is set.

Early DMA interrupt generation is useful to:

- Reduce the interrupt latency in timing-critical applications where it would be beneficial to let the DMA preemptively generate the IRQ before the DMA transfer is complete
- Serve as a “progress notification” when scheduling other tasks for the CPU to complete
- Transfer weights of a neural network layer and notify the CPU to complete software configuration writes to the IP
- Implement a ping-pong buffer (by setting DMAPREIRQ to half)

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11.2.7 DMA Auto-enable

All DMA channels can be set to automatically enable based on a register write to DMASA, DMADA, or DMASZ. The automatic DMA channel enable source is configured by the DMAAUTOEN bits of the DMA channel control register.

This allows application software to only have to modify one register when updating a DMA channel configuration as opposed to modifying DMASA, DMADA, or DMASZ and then also re-enabling the DMA channel by setting DMACTL.DMAEN

11.2.8 Addressing Modes

The DMA module has seven addressing modes: 4 basic addressing modes available to all channels and 3 extended modes available on full-feature channels. The addressing mode for each DMA channel is independently configurable. For example, channel 0 can transfer between two fixed addresses, while channel 1 transfers between two blocks of addresses.

The 4 basic addressing modes are:

1. Fixed address to fixed address
2. Fixed address to block of addresses
3. Block of addresses to fixed address
4. Block of addresses to block of addresses

The 3 extended modes are:

1. Fill data to block of addresses
2. Data table to specific address
3. Gather data from address table to fixed address or block of addresses

The configuration and operation of the addressing modes are detailed in the following sections.

11.2.8.1 Basic Addressing Modes

The basic addressing modes available on channel types are configured with the source increment (DMASRCINCR) and destination increment (DMADSTINCR) control bits within the respective channel control registers. The DMASRCINCR bits select if the source address is incremented, decremented, or unchanged after each transfer. The DMADSTINCR bits select if the destination address is incremented, decremented, or unchanged after each transfer. The basic addressing modes are showcased in DMA Basic Addressing Modes. The configuration settings for the basic addressing modes are in DMA Basic Addressing Mode Configuration.

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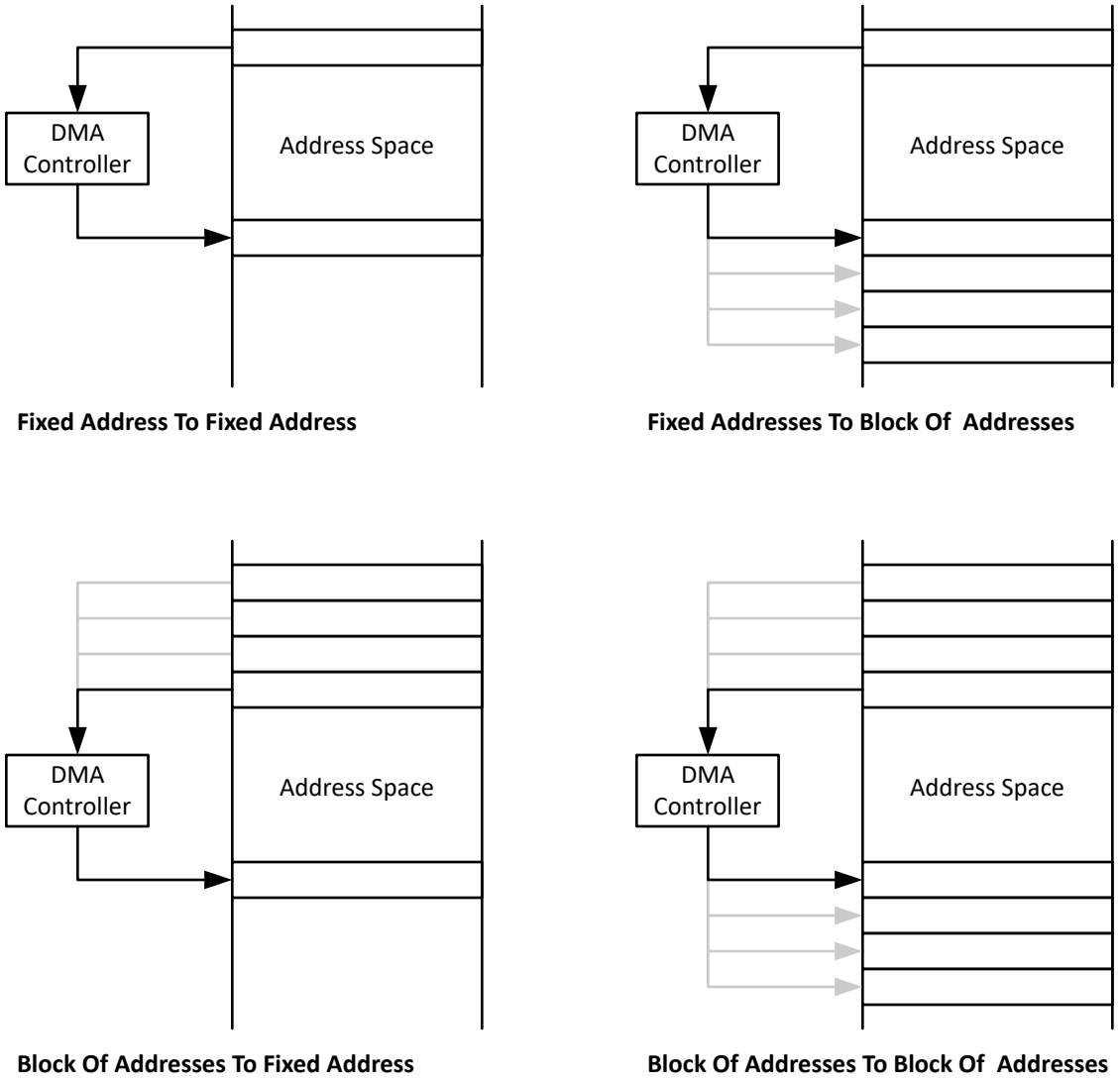


Figure 11-3. DMA Basic Addressing Modes

Table 11-5. DMA Basic Addressing Mode Configuration

Addressing Mode	DMASRCINCR	DMADSTINCR	Recommended Usage	Example
Fixed address to fixed address	Unchanged	Unchanged	Peripheral to peripheral	Transfer ADCRESULT0 register value to UNICOMM-UART TXDATA register
Fixed address to block of addresses	Unchanged	Increment/Decrement	Peripheral to memory	UNICOMM Receive operation - Transfer RXDATA register value to a buffer in memory
Block of addresses to fixed address	Increment/Decrement	Unchanged	Memory to peripheral	UNICOMM Transmit operation - Transfer buffer in memory to TXDATA register

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Table 11-5. DMA Basic Addressing Mode Configuration (continued)

Addressing Mode	DMASRCINCR	DMADSTINCR	Recommended Usage	Example
Block of addresses to block of addresses	Increment/Decrement	Increment/Decrement	Memory to memory	Transfer memory buffer contents to another memory buffer

11.2.8.2 Stride Mode

To make data organization easier, all channels support a “stride” mode where the DMA source and destination addresses can be incremented to a higher value (rather than +1) after a transfer. This is helpful for re-organizing the order of data between the source and destination.

To support incremental strides, set the DMADSTINCR and/or DMASRCINCR to STRIDE_n, where n is the number of destination and/or source increments. The real address increment values for the source and destination addresses are based on the definitions of DMASRCWDTH and DMADSTWDTH respectively. The formulas for calculating the incremental strides are:

- DMASRCINCR = (STRIDE_n * DMASRCWDTH)
- DMADSTINCR = (STRIDE_n * DMADSTWDTH)

Note

Stride mode is increment only.

11.2.8.3 Extended Modes

FULL channels have 3 extended modes selected by the DMAEM bits as listed in Table 11-6. A graphical overview of the extended modes can be seen in Figure 11-4. Each channel is individually configurable for a specific extended mode. For example, channel 0 can be configured in table mode while channel 1 is configured in fill mode. These extended modes are each designed with a specific use case in mind, the recommendation is to configure the DMASA, DMADA, DMASRCINCR, DMADSTINCR, DMASRCWDTH, and DMADSTWDTH registers/fields as described in the below sections for each mode so the intended operation to occurs.

Table 11-6. DMA Extended Modes

DMAEM	Extended Mode	Description
0	Normal mode	Operation is defined by the transfer mode (DMATM) and basic addressing mode configurations.
1	Gather mode	Used to read data from an address table and copy to configurable address
2	Fill mode	Used to fill predefined data patterns into memory
3	Table mode	Used to help configure a table of peripheral control registers

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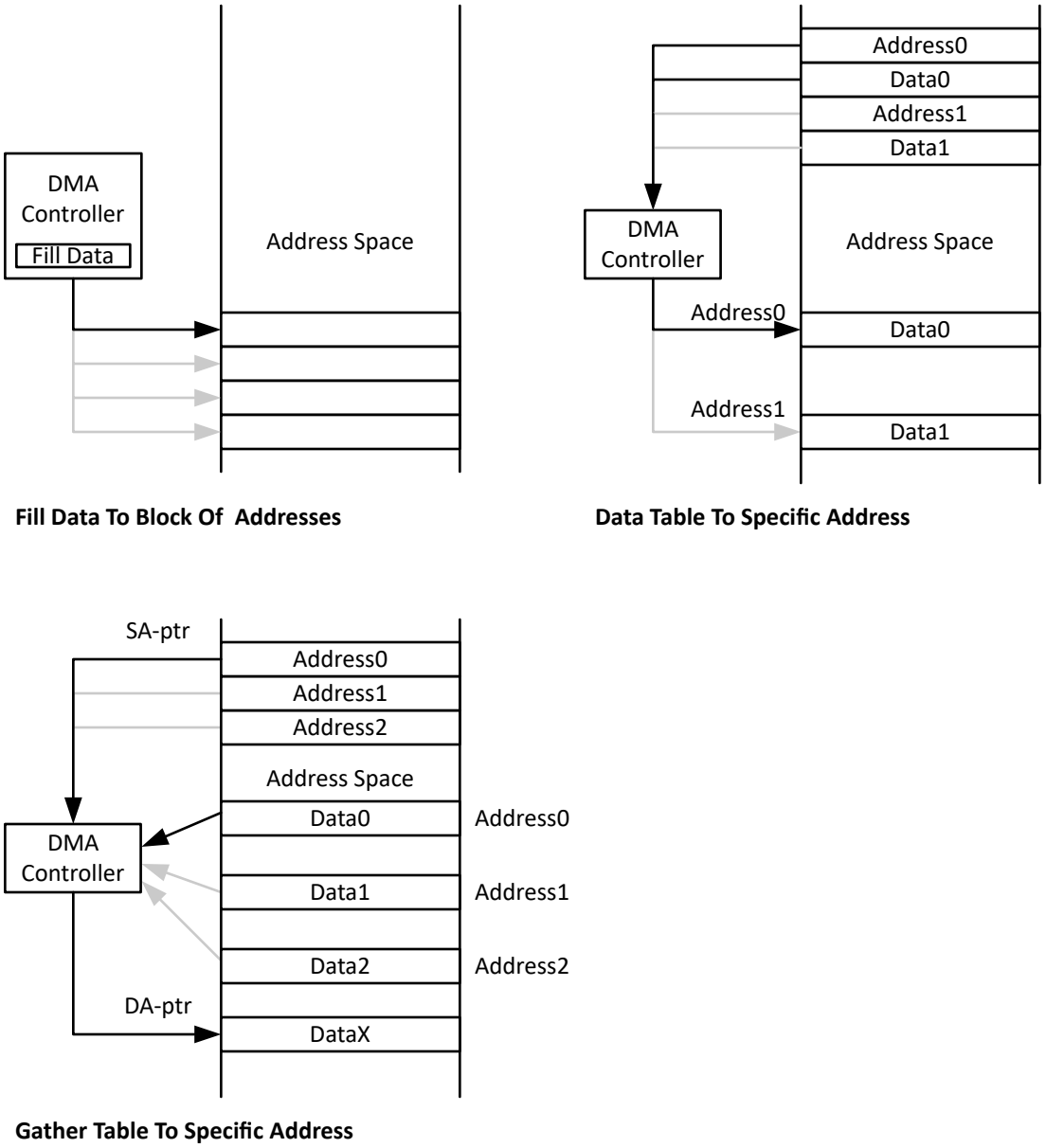


Figure 11-4. DMA Extended Modes Diagram

11.2.8.3.1 Fill Mode

In fill mode (DMAEM = 2h), the DMA module takes a predefined FILL value/pattern and writes this to a user defined segment of memory. The DMATM register setting is ignored and the "block transfer" mode is used automatically. The intended use case for this mode is to initialize or re-initialize a memory buffer with values (for example all zeros or incrementing data) using the DMA, without the need for a software loop doing each write individually via the CPU.

In other modes, the 32-bit value programmed to the DMASA register is used as a pointer to a memory location, whereas in FILL mode, the value programmed to the DMASA register is used directly as the FILL data. The DMASRCINCR bit field is used to indicate whether the FILL data remains constant or is incremented/decremented with every write cycle. This feature allows for filling a memory block with a sequential pattern. The DMASRCWDTH bit field indicates the magnitude to increment of the FILL mode data. Refer to Table 11-7 for how to use DMASRCWDTH in fill mode.

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The benefit of doing this operation using FILL mode (DMAEN=2) rather than normal mode with block transfer configured (DMAEN=2, DMATM=1), is that FILL mode has an improved performance due to the fact that the transfer of each individual element in normal mode requires the DMA to read and write, whereas in FILL mode, the fill data is stored inside the DMASA register, so each element only requires a write operation.

Table 11-7. DMASRCWDTH in Fill Mode

DMASRCWDTH	FILL Mode Data Increment Value
0	±1
1	±2
2	±4
3	±8

The channel destination registers and bit fields DMADA, DMADSTINCR, and DMADSTWDTH all behave as expected and influence where and how in memory the FILL pattern is written.

11.2.8.3.2 Table Mode

In table mode (DMAEM = 3h), the DMA controller executes two 32-bit reads from the source and one 32-bit write to a determined destination. Table mode allows the DMA to parse through a table of addresses and data to configure peripheral memory mapped registers in a single block transfer. This feature can be leveraged to interpret a table of addresses and data and use the DMA to efficiently program that data to the associated addresses without CPU intervention. For example, to configure a peripheral to a default setting after an interrupt or initialize/re-initialize a peripheral's settings after entering a low power mode.

The DMASRCWDTH bit field must be set to "3" (64-bit mode) and the DMADSTWDTH bit field must be set to "2" (32-bit mode). This is to make sure that the DMA controller reads the table correctly (two 32-bit reads) and writes the table data correctly (one 32-bit write). The DMASRCINCR bit field can be set to either increment or decrement the source address after transfers. DMASZ is set to represent the number of entries in the table and DMATM must be set for block transfer mode. The DMADA and DMADSTINCR are ignored in table mode and can be treated as "don’t care" values as the destination write is based on the information in the table.

For table mode to work properly, the DMASA register must be programmed with the start address of the table, which must be aligned to 64-bit data (DMASA[2:0] = "000b"). The address stored in the table needs to be on the lower word of a 64-bit data (ADDR[2:0] = "000b") while the data needs to be on the upper word of a 64-bit data (ADDR[2:0] = "100b"). Table 11-8 is an example of a table in memory compatible with the DMA table mode.

Table 11-8. Example of an Incremental Table Compatible with DMA Table Mode

Table Address	Table Data
0x0000	Address 0
0x0004	Data 0
0x0008	Address 1
0x000C	Data 1

The DMA programs the addresses in the order laid out by the table. User must be sure the order of the addresses/data pairs in the table complies with the requirements of the peripheral. For example, if the peripheral requires the register containing an enable bit be written after all other register configurations, make sure this is the last address and data pair in the table.

11.2.8.3.3 Gather Mode

In gather mode (DMAEM = 1h), the DMA controller executes two 32-bit reads and one 32-bit write based on an address table located at the source. Different from table mode, where the table consists of an Address followed by the Data to be written in a 64-bit block, in gather mode the initial table contains a list of source addresses to be read from. The DMA controller reads an address, then reads the data stored at the read address, and then writes the data read to a memory block at a specified destination. The intended use case for this feature is to read all the registers of a specific peripheral and save the state to a buffer in memory. This feature is especially

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useful for CRC calculations, memory mapped register validation checks, or to save the register context before entering low power mode.

DMASA points to the beginning of a table containing addresses of data to gather. DMADA points to the memory location used to write (or "gather") the gathered data to. The DMASRCWDTH bit field and the DMADSTWDTH bit fields must be set to "2" (32-bit mode). This is to make sure that the DMA controller reads the gather table correctly (one 32-bit read) and writes the gathered data correctly (one 32-bit write). The DMASRCINCR bit field and DMADSTINCR bit fieldcan be set to either increment or decrement the source address after transfers. DMASZ is set to represent the number of entries in the table and DMATM must be set for block transfer mode.

The basic steps that the DMA controller takes in gather mode are as follows:

1. The DMA controller reads the data stored at the source address (DMASA).
2. The data read at the source address is copied into a temporary address register.
3. The DMA controller reads the gather data from the address stored in the temporary address register.
4. The DMA controller then writes the gathered data to the destination address (DMADA).
5. The DMASA, DMADA, and DMASZ registers are incremented or decremented as configured.

11.2.9 DMA Operating Mode Support

The DMA supports triggered transfers in RUN mode and in the SLEEP low-power mode. Refer to the following sections for more details.

11.2.9.1 Transfer in RUN Mode

In RUN mode the system is fully operational. The CPU and all other peripherals and resources are available, therefore there is no restriction on the DMA functionality in RUN mode.

11.2.9.2 Transfer in SLEEP Mode

In SLEEP mode only the CPU is halted. All other peripherals and resources are available as when in RUN mode, therefore there is no restriction on the DMA functionality in SLEEP mode. All peripherals that can trigger a DMA transfer in RUN mode will also be able to trigger a DMA transfer in SLEEP mode.

11.2.9.3 Transfer in STOP Mode

In STOP mode the CPU is halted and the ULPCLK is limited to 4MHz operation. PD1 peripherals are disabled and in retention mode when applicable. Only PD0 peripherals are functional and therefore only PD0 peripherals are able to trigger a DMA transfer in STOP mode. The DMA is located in PD1, so although the register settings are retained, the DMA is not functional during STOP mode. If a DMA channel is triggered during this mode, the transfer does not take place until the device leaves STOP mode.

11.2.9.4 Transfers in STANDBY Mode

In STANDBY mode the CPU is halted and the ULPCLK is limited to 32kHz operation. PD1 peripherals are disabled and in retention mode when applicable. Only PD0 peripherals are functional and therefore only PD0 peripherals are able to trigger a DMA transfer in STANDBY mode. The DMA is located in PD1, so although the register settings are retained, the DMA is not functional during STOP mode. If a DMA channel is triggered during this mode, the transfer does not take place until the device leaves STOP mode.

11.2.9.5 Transfers in SHUTDOWN Mode

In SHUTDOWN mode the core regulator is completely disabled and all SRAM and register contents are lost, except general purpose memory in SYSCTL storing state information. This means the DMA register settings are lost and the DMA is not functional during SHUTDOWN mode. After exiting SHUTDOWN mode (which triggers a BOR), the DMA module must be reconfigured to perform any transfers.

11.3 DMA Interrupts & Triggers

11.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

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Table 11-9. CPU Interrupts Triggered by the DMA

NVIC Interrupt Name	Peripheral Instance Name	Register Group	DMA Interrupt Configuration Registers	Description
DMA.CPU_INT	DMA	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	DMA interrupt. Multiple OR'd, configurable source conditions.

11.3.1.1 DMA Controller Interrupts

Each DMA channel has its own raw interrupt status (RIS) flag. Each RIS flag is set in any mode when the corresponding DMASZ register counts to zero. If the corresponding interrupt mask (MASK) and RIS bits are set, an interrupt request is generated.

All RIS flags are prioritized, with DMA0 being the highest, and combined to source a single interrupt vector. The highest-priority enabled interrupt generates a number in the interrupt index (IIDX) register. This number can be evaluated or added to the program counter (PC) to automatically enter the appropriate software routine.

Any access, read or write, of the IIDX register automatically resets the highest pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt. For example, assume that DMA0 has the highest priority. If the DMA0-RIS and DMA2-RIS flags are set when the interrupt service routine accesses the IIDX register, DMA0-RIS is reset automatically. After the interrupt service routine is executed, the DMA2-RIS generates another interrupt which can then be serviced.

11.3.1.2 DMA Address Errors

The DMA has the ability to flag address errors. Source or destination address errors can come from accessing a protected or nonexisting memory range. If an address error occurs, the interrupt index IIDX.STAT field flags a DMA address error. Address error interrupts can be masked, set, and cleared using the ADDERR bit.

Note

The DMA does not perform range checking. If the DMA transfer occurs over a protected memory range, the destination data reports zeros (0h) for each byte of the DMA transaction that overlaps the protected or nonexisting memory range.

11.4 DMA Registers

This Section describes the DMA Registers.

11.4.1 DMA Base Address Table

Table 11-10. DMA Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Dma0Regs	DMA_REGS	DMA0	0x4002_0000

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11.4.2 DMA_REGS Registers

Table 11-11 lists the memory-mapped registers for the DMA_REGS registers. All register offset addresses not listed in Table 11-11 should be considered as reserved locations and the register contents should not be modified.

Table 11-11. DMA_REGS Registers

Offset	Acronym	Register Name	Group	Section
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
10FCh	DESC	Module Description		Go
1100h	DMAPRIO	DMA Channel Priority Control		Go
1110h + formula	DMATCTL_j	DMA Trigger Select		Go
1200h + formula	DMACTL_j	DMA Channel Control		Go
1204h + formula	DMASA_j	DMA Channel Source Address		Go
1208h + formula	DMADA_j	DMA Channel Destination Address		Go
120Ch + formula	DMASZ_j	DMA Channel Size		Go

Complex bit access types are encoded to fit into small table cells. Table 11-12 shows the codes that are used for access types in this section.

Table 11-12. DMA_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PDBGCTL Register (Offset = 1018h) [Reset = 00000000h]

PDBGCTL is shown in Figure 11-5 and described in Table 11-13.

Return to the Summary Table.

This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 11-5. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 11-14. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft halt boundary control. This function is only available, if [FREE] is set to 'STOP' 0h = The peripheral will halt immediately, even if the resultant state will result in corruption if the system is restarted 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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2 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 11-6 and described in Table 11-14.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, . . . IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred.
On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in RIS [RIS] and MIS [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-6. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 11-16. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No bit is set means there is no pending interrupt request 01h = DMA Channel 0 size counter reached zero (DMASZ=0). 02h = DMA Channel 1 size counter reached zero (DMASZ=0). 03h = DMA Channel 2 size counter reached zero (DMASZ=0). 04h = DMA Channel 3 size counter reached zero (DMASZ=0). 05h = DMA Channel 4 size counter reached zero (DMASZ=0). 06h = DMA Channel 5 size counter reached zero (DMASZ=0). 07h = DMA Channel 6 size counter reached zero (DMASZ=0). 08h = DMA Channel 7 size counter reached zero (DMASZ=0). 09h = DMA Channel 8 size counter reached zero (DMASZ=0). 0Ah = DMA Channel 9 size counter reached zero (DMASZ=0). 0Bh = DMA Channel 10 size counter reached zero (DMASZ=0). 0Ch = DMA Channel 11 size counter reached zero (DMASZ=0). 0Dh = DMA Channel 12 size counter reached zero (DMASZ=0). 0Eh = DMA Channel 13 size counter reached zero (DMASZ=0). 0Fh = DMA Channel 14 size counter reached zero (DMASZ=0). 10h = DMA Channel 15 size counter reached zero (DMASZ=0). 11h = PRE-IRQ event for DMA Channel 0. 12h = PRE-IRQ event for DMA Channel 1. 13h = PRE-IRQ event for DMA Channel 2. 14h = PRE-IRQ event for DMA Channel 3. 15h = PRE-IRQ event for DMA Channel 4. 16h = PRE-IRQ event for DMA Channel 5. 17h = PRE-IRQ event for DMA Channel 6. 18h = PRE-IRQ event for DMA Channel 7. 19h = DMA address error, SRC address not reachable.

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3 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 11-7 and described in Table 11-15.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then the corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX [IIDX], as well as MIS [MIS].
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-7. IMASK Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	ADDRERR
R/W-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	PREIRQCH5	PREIRQCH4	PREIRQCH3	PREIRQCH2	PREIRQCH1	PREIRQCH0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 11-18. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	0h	
25	RESERVED	R/W	0h	Reserved
24	ADDRERR	R/W	0h	DMA address error, SRC address not reachable. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	PREIRQCH5	R/W	0h	Pre-IRQ for Channel 5. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
20	PREIRQCH4	R/W	0h	Pre-IRQ for Channel 4. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
19	PREIRQCH3	R/W	0h	Pre-IRQ for Channel 3. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
18	PREIRQCH2	R/W	0h	Pre-IRQ for Channel 2. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
17	PREIRQCH1	R/W	0h	Pre-IRQ for Channel 1. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
16	PREIRQCH0	R/W	0h	Pre-IRQ for Channel 0. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit

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Table 11-18. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMACH15	R/W	0h	DMA Channel 15 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
14	DMACH14	R/W	0h	DMA Channel 14 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
13	DMACH13	R/W	0h	DMA Channel 13 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
12	DMACH12	R/W	0h	DMA Channel 12 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
11	DMACH11	R/W	0h	DMA Channel 11 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
10	DMACH10	R/W	0h	DMA Channel 10 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
9	DMACH9	R/W	0h	DMA Channel 9 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
8	DMACH8	R/W	0h	DMA Channel 8 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
7	DMACH7	R/W	0h	DMA Channel 7 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
6	DMACH6	R/W	0h	DMA Channel 6 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
5	DMACH5	R/W	0h	DMA Channel 5 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
4	DMACH4	R/W	0h	DMA Channel 4 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
3	DMACH3	R/W	0h	DMA Channel 3 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
2	DMACH2	R/W	0h	DMA Channel 2 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit

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Table 11-18. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DMACH1	R/W	0h	DMA Channel 1 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
0	DMACH0	R/W	0h	DMA Channel 0 interrupt signal. Size counter reached zero (DMASZ=0). 0h = Clear interrupt mask bit 1h = Set interrupt mask bit

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4 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 11-8 and described in Table 11-16.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR [ICLR] register bit even if the corresponding IMASK [IMASK] bit is not enabled.
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-8. RIS Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	ADDRERR
R-0h						R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	PREIRQCH5	PREIRQCH4	PREIRQCH3	PREIRQCH2	PREIRQCH1	PREIRQCH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 11-20. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25	RESERVED	R	0h	Reserved
24	ADDRERR	R	0h	DMA address error, SRC address not reachable. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	PREIRQCH5	R	0h	Pre-IRQ for Channel 5. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
20	PREIRQCH4	R	0h	Pre-IRQ for Channel 4. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
19	PREIRQCH3	R	0h	Pre-IRQ for Channel 3. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
18	PREIRQCH2	R	0h	Pre-IRQ for Channel 2. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
17	PREIRQCH1	R	0h	Pre-IRQ for Channel 1. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
16	PREIRQCH0	R	0h	Pre-IRQ for Channel 0. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit

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Table 11-20. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMACH15	R	0h	DMA Channel 15 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
14	DMACH14	R	0h	DMA Channel 14 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
13	DMACH13	R	0h	DMA Channel 13 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
12	DMACH12	R	0h	DMA Channel 12 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
11	DMACH11	R	0h	DMA Channel 11 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
10	DMACH10	R	0h	DMA Channel 10 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
9	DMACH9	R	0h	DMA Channel 9 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
8	DMACH8	R	0h	DMA Channel 8 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
7	DMACH7	R	0h	DMA Channel 7 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
6	DMACH6	R	0h	DMA Channel 6 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
5	DMACH5	R	0h	DMA Channel 5 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
4	DMACH4	R	0h	DMA Channel 4 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
3	DMACH3	R	0h	DMA Channel 3 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
2	DMACH2	R	0h	DMA Channel 2 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred

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Table 11-20. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DMACH1	R	0h	DMA Channel 1 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred
0	DMACH0	R	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur 1h = Interrupt occurred

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5 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 11-9 and described in Table 11-17.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK [IMASK] and RIS [RIS] registers.
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-9. MIS Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	ADDRERR
R-0h						R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	PREIRQCH5	PREIRQCH4	PREIRQCH3	PREIRQCH2	PREIRQCH1	PREIRQCH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 11-22. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25	RESERVED	R	0h	Reserved
24	ADDRERR	R	0h	DMA address error, SRC address not reachable. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	PREIRQCH5	R	0h	Pre-IRQ for Channel 5. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
20	PREIRQCH4	R	0h	Pre-IRQ for Channel 4. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
19	PREIRQCH3	R	0h	Pre-IRQ for Channel 3. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
18	PREIRQCH2	R	0h	Pre-IRQ for Channel 2. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
17	PREIRQCH1	R	0h	Pre-IRQ for Channel 1. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
16	PREIRQCH0	R	0h	Pre-IRQ for Channel 0. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
15	DMACH15	R	0h	DMA Channel 15 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred

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Table 11-22. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMACH14	R	0h	DMA Channel 14 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
13	DMACH13	R	0h	DMA Channel 13 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
12	DMACH12	R	0h	DMA Channel 12 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
11	DMACH11	R	0h	DMA Channel 11 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
10	DMACH10	R	0h	DMA Channel 10 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
9	DMACH9	R	0h	DMA Channel 9 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
8	DMACH8	R	0h	DMA Channel 8 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
7	DMACH7	R	0h	DMA Channel 7 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
6	DMACH6	R	0h	DMA Channel 6 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
5	DMACH5	R	0h	DMA Channel 5 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
4	DMACH4	R	0h	DMA Channel 4 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
3	DMACH3	R	0h	DMA Channel 3 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
2	DMACH2	R	0h	DMA Channel 2 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred
1	DMACH1	R	0h	DMA Channel 1 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred

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Table 11-22. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMACH0	R	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Interrupt did not occur or is masked out 1h = Interrupt occurred

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6 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 11-10 and described in Table 11-18.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS [RIS] bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS [MIS] bit is also set.
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-10. ISET Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	ADDRERR
W-0h						W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	PREIRQCH5	PREIRQCH4	PREIRQCH3	PREIRQCH2	PREIRQCH1	PREIRQCH0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 11-24. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	W	0h	
25	RESERVED	W	0h	Reserved
24	ADDRERR	W	0h	DMA address error, SRC address not reachable. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
23	RESERVED	W	0h	Reserved
22	RESERVED	W	0h	Reserved
21	PREIRQCH5	W	0h	Pre-IRQ for Channel 5. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
20	PREIRQCH4	W	0h	Pre-IRQ for Channel 4. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
19	PREIRQCH3	W	0h	Pre-IRQ for Channel 3. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
18	PREIRQCH2	W	0h	Pre-IRQ for Channel 2. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
17	PREIRQCH1	W	0h	Pre-IRQ for Channel 1. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
16	PREIRQCH0	W	0h	Pre-IRQ for Channel 0. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit

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Table 11-24. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMACH15	W	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
14	DMACH14	W	0h	DMA Channel 14 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
13	DMACH13	W	0h	DMA Channel 13 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
12	DMACH12	W	0h	DMA Channel 12 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
11	DMACH11	W	0h	DMA Channel 11 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
10	DMACH10	W	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
9	DMACH9	W	0h	DMA Channel 9 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
8	DMACH8	W	0h	DMA Channel 8 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
7	DMACH7	W	0h	DMA Channel 7 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
6	DMACH6	W	0h	DMA Channel 6 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
5	DMACH5	W	0h	DMA Channel 5 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
4	DMACH4	W	0h	DMA Channel 4 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
3	DMACH3	W	0h	DMA Channel 3 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
2	DMACH2	W	0h	DMA Channel 2 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt

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Table 11-24. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DMACH1	W	0h	DMA Channel 1 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt
0	DMACH0	W	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Set interrupt

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7 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 11-11 and described in Table 11-19.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.
Note: The number of DMACH is device dependent. Please consult the datasheet of the specific device to map which channel number is implemented.

Figure 11-11. ICLR Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	ADDRERR
W-0h						W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	PREIRQCH5	PREIRQCH4	PREIRQCH3	PREIRQCH2	PREIRQCH1	PREIRQCH0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 11-26. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	W	0h	
25	RESERVED	W	0h	Reserved
24	ADDRERR	W	0h	DMA address error, SRC address not reachable. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
23	RESERVED	W	0h	Reserved
22	RESERVED	W	0h	Reserved
21	PREIRQCH5	W	0h	Pre-IRQ for Channel 5. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
20	PREIRQCH4	W	0h	Pre-IRQ for Channel 4. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
19	PREIRQCH3	W	0h	Pre-IRQ for Channel 3. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
18	PREIRQCH2	W	0h	Pre-IRQ for Channel 2. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
17	PREIRQCH1	W	0h	Pre-IRQ for Channel 1. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
16	PREIRQCH0	W	0h	Pre-IRQ for Channel 0. Size counter reached Pre-IRQ threshold. 0h = Clear interrupt mask bit 1h = Set interrupt mask bit
15	DMACH15	W	0h	DMA Channel 15 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt

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Table 11-26. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMACH14	W	0h	DMA Channel 14 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
13	DMACH13	W	0h	DMA Channel 13 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
12	DMACH12	W	0h	DMA Channel 12 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
11	DMACH11	W	0h	DMA Channel 11 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
10	DMACH10	W	0h	DMA Channel 10 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
9	DMACH9	W	0h	DMA Channel 9 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
8	DMACH8	W	0h	DMA Channel 8 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
7	DMACH7	W	0h	DMA Channel 7 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
6	DMACH6	W	0h	DMA Channel 6 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
5	DMACH5	W	0h	DMA Channel 5 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
4	DMACH4	W	0h	DMA Channel 4 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
3	DMACH3	W	0h	DMA Channel 3 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
2	DMACH2	W	0h	DMA Channel 2 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt
1	DMACH1	W	0h	DMA Channel 1 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt

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Table 11-26. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMACH0	W	0h	DMA Channel 0 interrupt signals that size counter reached zero (DMASZ=0). 0h = Writing 0 has no effect 1h = Clear interrupt

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8 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 11-12 and described in Table 11-20.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 11-12. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				RESERVED				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 11-28. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	2511h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	Fh	Feature Set for the DMA: number of DMA channel minus one (e.g. 0->1ch, 2->3ch, 15->16ch). 0h = Smallest value (1 channel) Fh = Highest value (16 channel)
11-8	RESERVED	R	0h	
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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9 DMAPRIO Register (Offset = 1100h) [Reset = 00000000h]

DMAPRIO is shown in Figure 11-13 and described in Table 11-21.

Return to the Summary Table.

DMA Channel Priority Control

Figure 11-13. DMAPRIO Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						BURSTSZ	
R/W-0h						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ROUNDROBIN
R/W-0h							R/W-0h

Table 11-30. DMAPRIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	0h	
17-16	BURSTSZ	R/W	0h	Define the burst size of a block transfer, before the priority is re-evaluated 0h = There is no burst size, the whole block transfer is completed on one transfer without interruption 1h = The burst size is 8, after 9 transfers the block transfer is interrupted and the priority is reevaluated 2h = The burst size is 16, after 17 transfers the block transfer is interrupted and the priority is reevaluated 3h = The burst size is 32, after 33 transfers the block transfer is interrupted and the priority is reevaluated
15-1	RESERVED	R/W	0h	
0	ROUNDROBIN	R/W	0h	Round robin. This bit enables the round-robin DMA channel priorities. 0h = Roundrobin priority disabled, DMA channel priority is fixed: DMA0-DMA1-DMA2-...-DMA16 1h = Roundrobin priority enabled, DMA channel priority changes with each transfer

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10 DMATCTL_j Register (Offset = 1110h + formula) [Reset = 00000000h]

DMATCTL_j is shown in Figure 11-14 and described in Table 11-22.

Return to the Summary Table.

DMA Trigger Control

Offset = 1110h + (j * 4h); where j = 0h to Fh

Figure 11-14. DMATCTL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
DMATINT	DMATSEL						
R/W-0h	R/W-0h						

Table 11-32. DMATCTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	DMATINT	R/W	0h	DMA Trigger by Internal Channel 0h = DMATSEL will define external trigger select as transfer trigger. 1h = DMATSEL will define internal channel as transfer trigger select. 0-> Channel0-done, 1-> Channel1-done, ...
6-0	DMATSEL	R/W	0h	DMA Trigger Select Note: Reference the datasheet of the device to see the specific trigger mapping. 00h = Software trigger request 7Fh = Highest possible value

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11 DMACTL_j Register (Offset = 1200h + formula) [Reset = 00000000h]

DMACTL_j is shown in Figure 11-15 and described in Table 11-23.

Return to the Summary Table.

DMA Channel Control

Offset = 1200h + (j * 10h); where j = 0h to Fh

Figure 11-15. DMACTL_j Register

31	30	29	28	27	26	25	24
RESERVED		DMATM		RESERVED		DMAEM	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
DMADSTINCR				DMASRCINCR			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	DMADSTWDTH			RESERVED	DMASRCWDTH		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	DMAPREIRQ			DMAAUTOEN		DMAEN	DMAREQ
R/W-0h	R/W-0h			R/W-0h		R/W-0h	R/W-0h

Table 11-34. DMACTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29-28	DMATM	R/W	0h	DMA transfer mode register Note: The repeat-single (2h) and repeat-block (3h) transfer are only available in a FULL-channel configuration. Please consult the datasheet of the specific device to map which channel number has FULL or BASIC capability. In a BASIC channel configuration only the values for single (0h) and block (1h) transfer can be set. 0h = Single transfer. Each transfers requires a new trigger. When the DMASZ counts down to zero an event can be generated and the DMAEN is cleared. 1h = Block transfer. Each trigger transfers the complete block defined in DMASZ. After the transfer is complete an event can be generated and the DMAEN is cleared. 2h = Repeated single transfer. Each transfers requires a new trigger. When the DMASZ counts down to zero an event can be generated. After the last transfer the DMASA, DMADA, DAMSZ registers are restored to its initial value and the DMAEN stays enabled. 3h = Repeated block transfer. Each trigger transfers the complete block defined in DMASZ. After the last transfer the DMASA, DMADA, DAMSZ registers are restored to its initial value and the DMAEN stays enabled.
27-26	RESERVED	R/W	0h	

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Table 11-34. DMACTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-24	DMAEM	R/W	0h	DMA extended mode Note: The extended transfer modes are only available in a FULL-channel configuration. Please consult the datasheet of the specific device to map which channel number has FULL or BASIC capability. In a BASIC channel configuration this register is a read-only register and reads 0x0. 0h = Normal mode is related to transfers from SRC to DST 1h = Gather mode will read a data from an address table located at SA, and the data is transfered to the DA 2h = Fill mode will copy the SA register content as data to DA 3h = Table mode will read an address and data value from SA and write the data to address
23-20	DMADSTINCR	R/W	0h	DMA destination increment. This bit selects automatic incrementing or decrementing of the destination address DMADA for each transfer. The amount of change to the DMADA is based on the definitin in the DMADSTWDTH. For example an increment of 1 (+1) on a WORD transfer will increment the DMADA by 4. 0h = Address is unchanged (+0) 2h = Decremented by 1 (-1 * DMADSTWDTH) 3h = Incremented by 1 (+1 * DMADSTWDTH) 8h = Stride size 2 (+2 * DMADSTWDTH) 9h = Stride size 3 (+3 * DMADSTWDTH) Ah = Stride size 4 (+4 * DMADSTWDTH) Bh = Stride size 5 (+5 * DMADSTWDTH) Ch = Stride size 6 (+6 * DMADSTWDTH) Dh = Stride size 7 (+7 * DMADSTWDTH) Eh = Stride size 8 (+8 * DMADSTWDTH) Fh = Stride size 9 (+9 * DMADSTWDTH)
19-16	DMASRCINCR	R/W	0h	DMA source increment. This bit selects automatic incrementing or decrementing of the source address DMASA for each transfer. The amount of change to the DMASA is based on the definitin in the DMASRCWDTH. For example an increment of 1 (+1) on a WORD transfer will increment the DMASA by 4. 0h = Address is unchanged (+0) 2h = Decremented by 1 (-1 * DMASRCWDTH) 3h = Incremented by 1 (+1 * DMASRCWDTH) 8h = Stride size 2 (+2 * DMASRCWDTH) 9h = Stride size 3 (+3 * DMASRCWDTH) Ah = Stride size 4 (+4 * DMASRCWDTH) Bh = Stride size 5 (+5 * DMASRCWDTH) Ch = Stride size 6 (+6 * DMASRCWDTH) Dh = Stride size 7 (+7 * DMASRCWDTH) Eh = Stride size 8 (+8 * DMASRCWDTH) Fh = Stride size 9 (+9 * DMASRCWDTH)
15	RESERVED	R/W	0h	
14-12	DMADSTWDTH	R/W	0h	DMA destination width. This bit selects the destination as a byte, half word, word, long word or long-long word. 0h = Destination data width is BYTE (8-bit) 1h = Destination data width is HALF-WORD (16-bit) 2h = Destination data width is WORD (32-bit) 3h = Destination data width is LONG-WORD (64-bit) 4h = Source data width is LONG-LONG-WORD (128-bit)
11	RESERVED	R/W	0h	
10-8	DMASRCWDTH	R/W	0h	DMA source width. This bit selects the source data width as a byte, half word, word, long word or long-long word. 0h = Source data width is BYTE (8-bit) 1h = Source data width is HALF-WORD (16-bit) 2h = Source data width is WORD (32-bit) 3h = Source data width is LONG-WORD (64-bit) 4h = Source data width is LONG-LONG-WORD (128-bit)
7	RESERVED	R/W	0h	

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Table 11-34. DMACTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	DMAPREIRQ	R/W	0h	Enable an early IRQ event. This can help software to react quicker to and DMA done event or allows some additional configuration before the channel is complete. Note: This register is only available in a FULL-channel configuration. Please consult the datasheet of the specific device to map which channel number has FULL or BASIC capability. In a BASIC configuration this register is a read only value and always reads as 0x0. 0h = Pre-IRQ event disabled. 1h = Issure Pre-IRQ event when DMASZ=1 2h = Issure Pre-IRQ event when DMASZ=2 3h = Issure Pre-IRQ event when DMASZ=4 4h = Issure Pre-IRQ event when DMASZ=8 5h = Issure Pre-IRQ event when DMASZ=32 6h = Issure Pre-IRQ event when DMASZ=64 7h = Issure Pre-IRQ event when DMASZ reached the half size point of the original transfer size
3-2	DMAAUTOEN	R/W	0h	Automatic DMA channel enable on DMASA, DMADA, DMASZ register write. If channel is configured as SW trigger (DMATCTL=0), the AUTOEN will set the DMAEN and DMAREQ. If channel is configured as HW trigger (DMACTL!=0), the AUTOEN will only set the DMAEN. 0h = No automatic DMA enable 1h = Automatic DMA enable on DMASA register write. 2h = Automatic DMA enable on DMADA register write. 3h = Automatic DMA enable on DMASZ register write.
1	DMAEN	R/W	0h	DMA enable 0h = DMA channel disabled 1h = DMA channel enabled
0	DMAREQ	R/W	0h	DMA request. Software-controlled DMA start. DMAREQ is reset automatically. 0h = Default read value 1h = DMA transfer request (start DMA)

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12 DMASA_j Register (Offset = 1204h + formula) [Reset = 00000000h]

DMASA_j is shown in Figure 11-16 and described in Table 11-24.

Return to the Summary Table.

DMA Channel Source Address

Offset = 1204h + (j * 10h); where j = 0h to Fh

Figure 11-16. DMASA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R/W-0h																															

Table 11-36. DMASA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	DMA Channel Source Address 0h = Smallest value FFFFFFFFh = Highest possible value

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13 DMADA_j Register (Offset = 1208h + formula) [Reset = 00000000h]

DMADA_j is shown in Figure 11-17 and described in Table 11-25.

Return to the Summary Table.

DMA Channel Destination Address

Offset = 1208h + (j * 10h); where j = 0h to Fh

Figure 11-17. DMADA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R/W-0h																															

Table 11-38. DMADA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR	R/W	0h	DMA Channel Destination Address 0h = Smallest value FFFFFFFFh = Highest possible value

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14 DMASZ_j Register (Offset = 120Ch + formula) [Reset = 00000000h]

DMASZ_j is shown in Figure 11-18 and described in Table 11-26.

Return to the Summary Table.

DMA Channel Size

Offset = 120Ch + (j * 10h); where j = 0h to Fh

Figure 11-18. DMASZ_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SIZE															
R/W-0h																R/W-0h															

Table 11-40. DMASZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	SIZE	R/W	0h	DMA Channel Size in number of transfers 0h = Smallest value FFFFh = Highest possible value

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Chapter 12

Error Aggregator Module (EAM)

The Error Aggregator Module (EAM) provides a log of errors related to memory access and Error Correction Code (ECC) failures in the device.

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12.1 EAM Introduction

The EAM module's purpose is to aggregate safety and security errors from multiple sources. The EAM then stores these errors in the Memory Mapped Registers (MMR's). The types of errors are split into three groups: safety errors, security errors, and access errors. Each group has their own set of fixed priority which is defined in the Section 12.2 .

The top-level block diagram for the EAM is shown in Figure 12-1.

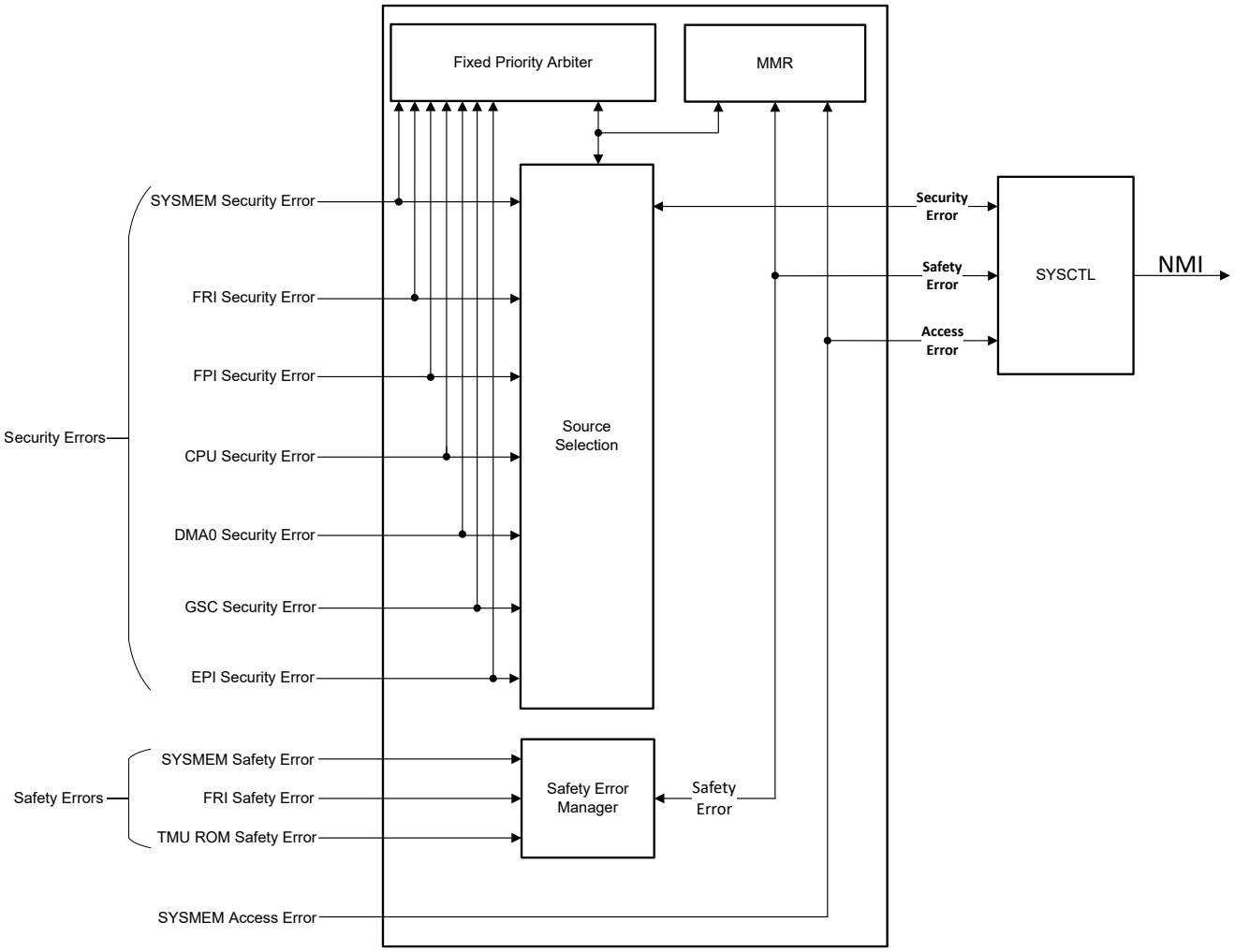


Figure 12-1. Top-Level EAM Block Diagram

12.2 EAM Operation

Each aggregator stores the errors from various sources with their own fixed priority. The fixed priority is determined by the fixed priority arbiter. The fixed priority table uses 1 as the highest priority and the largest number being the lowest priority. See the corresponding error aggregator on details on the corresponding fixed priority arbiter. Information on which address the error occurred, corresponding error type and error flag are stored in the respective register.

When an error occurs the following steps are taken:

1. Error source is selected based on the fixed priority arbiter
2. Error flag bit, address, and id are latched into respective registers corresponding to the selected error
3. Selected error will be forwarded to SYSCTL generating an NMI or interrupt
4. Wait for software to write to the clear register

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During step 4 the corresponding clear register must be written to by software for the next error to properly propagate. To see the corresponding register to clear please see *EAM Registers*.

12.2.1 Security Error Aggregator

The security error aggregator is used to handle the security errors generated from SRAM (SYSMEM), Flash Read Interface (FRI), Flash Program Interface (FPI), CPU, DMA0, and the Global Security Controller (GSC). These modules all generate different types of security errors that are propagated to the security error aggregator. After receiving these errors, the security error aggregator generates an security error non-maskable interrupt (NMI). Detailed information about the NMI can be seen in the Section 3.9.2 section.

Note

AM13E232x devices do not have ARM TrustZone technology enabled. All security errors are due to privilege policy violations.

When one of the security errors occur, the security fixed priority arbiter selects the error source based on the Table 12-1. After the security fixed priority arbiter selects an error, the corresponding error is stored in the SECURITY_ERR_FLAG register. Then the error is forwarded to SYSCTL and causes a security error NMI. This transaction can be seen in the Figure 12-2.

Table 12-1. Security Error Aggregator's Fixed Priority

Priority	Source
1 (Highest Priority)	MEM0
2	MEM1
3	MEM2
4	MEM3
5	FRI
6	FPI
7	CPU
8	DMA0
9	Reserved
10	GSC
11	EPI

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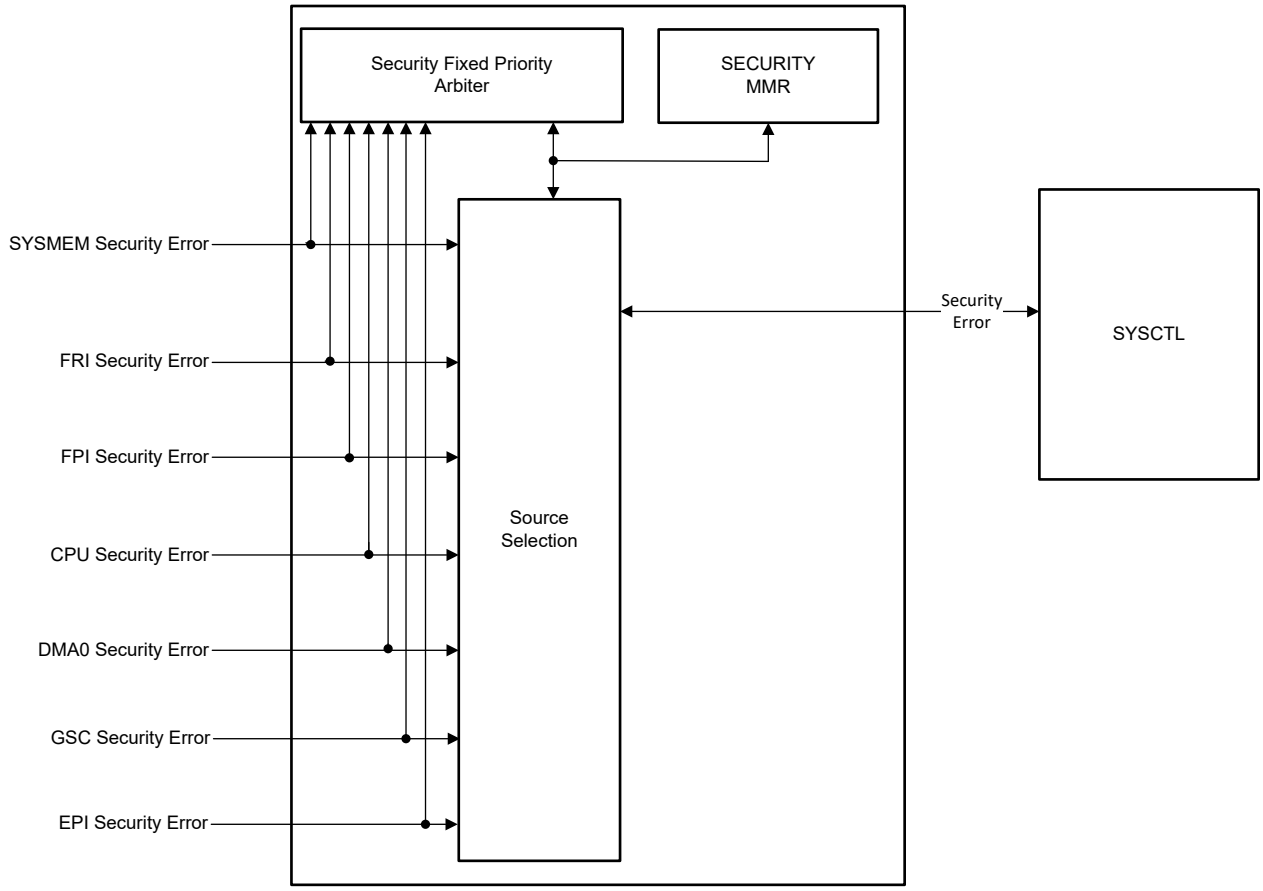


Figure 12-2. Security Error Aggregator Block Diagram

To properly understand the error that has occurred, information about the error can be found in the SECURITY_ERR_MSTID and SECURITY_ERR_ADDR registers. To clear the error and propagate the next error, the SECURITY_ERR_CLR register must be written to. Please see the *EAM Registers* section for a more detailed description on these registers.

12.2.2 Safety Error Aggregator

The safety error aggregator is the other error aggregator in the EAM. This error aggregator handles multiple safety errors caused by ECC or parity failures.When the safety error aggregator receives an ECC or parity error the module causes a NMI or an interrupt depending on the error. Information on the different types of errors can be seen in Section 3.9.2 . These ECC or parity errors can occur from the Flash Read Interface (FRI) or the SRAM memory (SYSMEM). Information on the ECC or parity error can be seen in the ECC Error Handling section of the Flash chapter. Information on the SRAM errors can be seen in the SRAM region section of the SYSCTL chapter. The key difference is that the safety error aggregator can generate NMIs as well as interrupts to handle the different types of ECC errors. See Table 12-2 for details on which interrupts are generated from the corresponding error.

Table 12-2. Safety Error Aggregator NMI and Interrupt

Error	Resulting Interrupt
Flash Read ECC SEC	FLASHSEC Interrupt
Flash Read ECC DED	FLASHDED NMI
SRAM MEM0 - SRAM MEM3 Parity error	SRAMPARITY NMI

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Due to the single bit errors (SEC) and dual bit errors (DED) generating different types of interrupts there are 4 sets of MMR's for this error aggregator: FRI_SEC, FRI_DED, SYSMEM_PARITY, and TMU_PARITY. Each one of these groups of MMR's has an individual set of MSTID, ADDR, FLAG, and CLR registers. To see detailed descriptions on these registers please see *EAM Registers*.

Note

For the FRI_SEC and FRI_DED registers, the address and master ID may hold arbitrary values if an error has not occurred. Only read this for debugging once the corresponding flag is set.

For a visual representation of the safety error aggregator module, please see Figure 12-3 to find the configuration of the source selectors, fixed priority arbiters, and segregation module. The fixed priority arbiter is only used for SYSMEM errors and as such the SYSMEM_PARITY uses the same priority level. The fixed priority arbiter is not needed for the flash read interface as there is only one type of flash error from the SEC and DED interfaces. To see the different priority levels please see table Table 12-3.

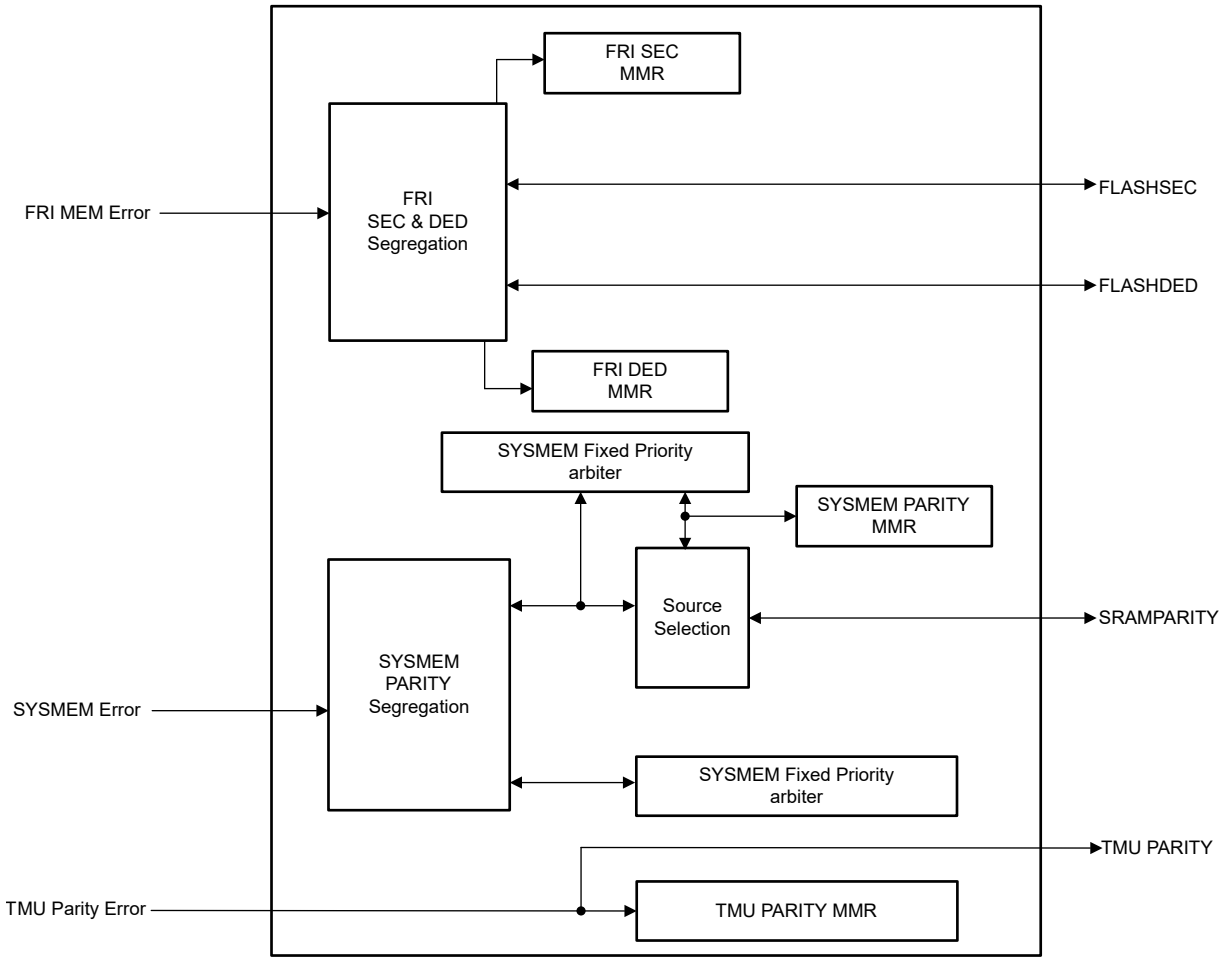


Figure 12-3. Safety Error Aggregator Block Diagram

Table 12-3. Safety Error Aggregator's Fixed Priority

Priority	Source
1 (Highest Priority)	MEM0
2	MEM1
3	MEM2
4	MEM3

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12.2.3 SYSMEM Access Error

The third type of error handled by the EAM is a SYSMEM Access Error. This error exists due to the AM13E232x device design which dual maps SRAM4 and SRAM5 to both the C-AHB (CPU bus) and S-AHB (System bus). Refer to the Architecture chapter for more information on the AM13E232x data buses.

There are four situations in which an access error is triggered:

1. The SRAM4_STATIC_MUX is configured for C-AHB access (default, SRAM4_STATIC_MUX_SEL = 1h) and S-AHB access is attempted.
2. The SRAM4_STATIC_MUX mux is configured for S-AHB access (SRAM4_STATIC_MUX_SEL = 0h) and C-AHB access is attempted.
3. The SRAM5_STATIC_MUX is configured for C-AHB access (default, SRAM5_STATIC_MUX_SEL = 1h) and S-AHB access is attempted.
4. The SRAM5_STATIC_MUX mux is configured for S-AHB access (SRAM5_STATIC_MUX_SEL = 0h) and C-AHB access is attempted.



Figure 12-4. SYSMEM Access Error

12.3 EAM Registers

This Section describes the EAM Registers.

12.3.1 EAM Base Address Table

Table 12-4. EAM Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
EamRegs	EAM_REGS	EAM	0x4002_C000

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12.3.2 EAM_REGS Registers

Table 12-5 lists the memory-mapped registers for the EAM_REGS registers. All register offset addresses not listed in Table 12-5 should be considered as reserved locations and the register contents should not be modified.

Table 12-5. EAM_REGS Registers

Offset	Acronym	Register Name	Group	Section
1000h	REVISION	IP revision id register		Go
1010h	SECURITY_ERR_FLAG	Security error flag		Go
1014h	SECURITY_ERR_CLR	Security error clear		Go
1018h	SECURITY_ERR_MSTID	Security error master id		Go
101Ch	SECURITY_ERR_ADDR	Security error address		Go
1030h	FRI_SEC_FLAG	FRI SEC flag		Go
1034h	FRI_SEC_CLR	FRI SEC clear		Go
1038h	FRI_SEC_ADDR	FRI SEC address		Go
103Ch	FRI_SEC_MSTID	FRI SEC master id		Go
1050h	FRI_DED_FLAG	FRI DED flag		Go
1054h	FRI_DED_CLR	FRI DED clear		Go
1058h	FRI_DED_ADDR	FRI DED address		Go
105Ch	FRI_DED_MSTID	FRI DED master id		Go
10B0h	SYSMEM_PAR_FLAG	SYSMEM parity error flag		Go
10B4h	SYSMEM_PAR_CLR	SYSMEM parity error clear		Go
10B8h	SYSMEM_PAR_ADDR	SYSMEM parity error address		Go
10BCh	SYSMEM_PAR_MSTID	SYSMEM parity error master id		Go
10D0h	TMUROM_PAR_FLAG	TMUROM parity error flag		Go
10D4h	TMUROM_PAR_CLR	TMUROM parity error clear		Go
10D8h	TMUROM_PAR_ADDR	TMUROM parity error address		Go
10DCh	TMUROM_PAR_TYPE	TMUROM parity error type		Go
10F0h	SYSMEM_ACC_FLAG	SYSMEM access error flag		Go
10F4h	SYSMEM_ACC_CLR	SYSMEM access error clear		Go
10F8h	SYSMEM_ACC_ADDR	SYSMEM access error address		Go
10FCh	SYSMEM_ACC_TYPE	SYSMEM access error type		Go
1110h	ECATRAM_PAR_FLAG	EtherCAT RAM parity error flag		Go
1114h	ECATRAM_PAR_CLR	EtherCAT RAM parity error clear		Go
1118h	ECATRAM_PAR_ADDR	EtherCAT RAM parity error address		Go

Complex bit access types are encoded to fit into small table cells. Table 12-6 shows the codes that are used for access types in this section.

Table 12-6. EAM_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

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Table 12-6. EAM_REGS Access Type Codes (continued)

Access Type	Code	Description
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 REVISION Register (Offset = 1000h) [Reset = 00000000h]

REVISION is shown in Figure 12-5 and described in Table 12-7.

Return to the Summary Table.

IP revision id register

Figure 12-5. REVISION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED							REVISION
R-0-0h							R-0h

Table 12-8. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	REVISION	R	0h	Revision register Reset type: SYSRST

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2 SECURITY_ERR_FLAG Register (Offset = 1010h) [Reset = 00000000h]

SECURITY_ERR_FLAG is shown in Figure 12-6 and described in Table 12-8.

Return to the Summary Table.

Security error flag

Figure 12-6. SECURITY_ERR_FLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED				FLSEM_ACCESS_ERROR	FLC_MMR_ACCESS_ERROR	FPI_ILLSIZE	FPI_ILLCMD
R-0-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
FPI_ILLMODECH	FPI_ILLRDVER	FPI_ILLERASE	FPI_ILLPROG	FPI_ILLADDR	HDP	PRIV	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 12-10. SECURITY_ERR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11	FLSEM_ACCESS_ERROR	R	0h	FLSEM ACCESS ERROR flag Reset type: SYSRST
10	FLC_MMR_ACCESS_ERROR	R	0h	FLC MMR ACCESS ERROR flag Reset type: SYSRST
9	FPI_ILLSIZE	R	0h	FPI ILLSIZE flag Reset type: SYSRST
8	FPI_ILLCMD	R	0h	FPI ILLCMD flag Reset type: SYSRST
7	FPI_ILLMODECH	R	0h	FPI ILLMODECH flag Reset type: SYSRST
6	FPI_ILLRDVER	R	0h	FPI ILLRDVER flag Reset type: SYSRST
5	FPI_ILLERASE	R	0h	FPI ILLERASE flag Reset type: SYSRST
4	FPI_ILLPROG	R	0h	FPI ILLPROG flag Reset type: SYSRST
3	FPI_ILLADDR	R	0h	FPI ILLADDR flag Reset type: SYSRST

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Table 12-10. SECURITY_ERR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HDP	R	0h	Hide protection error flag Reset type: SYSRST
1	PRIV	R	0h	Privilege error flag Reset type: SYSRST
0	RESERVED	R	0h	Reserved

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3 SECURITY_ERR_CLR Register (Offset = 1014h) [Reset = 00000000h]

SECURITY_ERR_CLR is shown in Figure 12-7 and described in Table 12-9.

Return to the Summary Table.

Security error clear

Figure 12-7. SECURITY_ERR_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED				FLSEM_ACCESS_ERROR	FLC_MMR_ACCESS_ERROR	FPI_ILLSIZE	FPI_ILLCMD
R-0-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
FPI_ILLMODECH	FPI_ILLRDVER	FPI_ILLERASE	FPI_ILLPROG	FPI_ILLADDR	HDP	PRIV	RESERVED
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 12-12. SECURITY_ERR_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11	FLSEM_ACCESS_ERROR	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FLSEM_ACCESS_ERROR] register. Reset type: SYSRST
10	FLC_MMR_ACCESS_ERROR	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FLC_MMR_ACCESS_ERROR] register. Reset type: SYSRST
9	FPI_ILLSIZE	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLSIZE] register. Reset type: SYSRST
8	FPI_ILLCMD	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLCMD] register. Reset type: SYSRST
7	FPI_ILLMODECH	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLMODECH] register. Reset type: SYSRST
6	FPI_ILLRDVER	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLRDVER] register. Reset type: SYSRST
5	FPI_ILLERASE	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLERASE] register. Reset type: SYSRST
4	FPI_ILLPROG	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLPROG] register. Reset type: SYSRST

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Table 12-12. SECURITY_ERR_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FPI_ILLADDR	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[FPI_ILLADDR] register. Reset type: SYSRST
2	HDP	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[HDP] register. Reset type: SYSRST
1	PRIV	R-0/W1C	0h	writing '1' will clear SECURITY_ERR_FLAG[PRIV] register. Reset type: SYSRST
0	RESERVED	R-0/W1C	0h	Reserved

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4 SECURITY_ERR_MSTID Register (Offset = 1018h) [Reset = 00000000h]

SECURITY_ERR_MSTID is shown in Figure 12-8 and described in Table 12-10.

Return to the Summary Table.

Security error master id

Figure 12-8. SECURITY_ERR_MSTID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTID							
R-0-0h																								R-0h							

Table 12-14. SECURITY_ERR_MSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R-0	0h	Reserved
7-0	MSTID	R	0h	Security error master ID. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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5 SECURITY_ERR_ADDR Register (Offset = 101Ch) [Reset = 00000000h]

SECURITY_ERR_ADDR is shown in Figure 12-9 and described in Table 12-11.

Return to the Summary Table.

Security error address

Figure 12-9. SECURITY_ERR_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-16. SECURITY_ERR_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Security error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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6 FRI_SEC_FLAG Register (Offset = 1030h) [Reset = 00000000h]

FRI_SEC_FLAG is shown in Figure 12-10 and described in Table 12-12.

Return to the Summary Table.

FRI single error correction flag

Figure 12-10. FRI_SEC_FLAG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SEC
R-0-0h															R-0h

Table 12-18. FRI_SEC_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	SEC	R	0h	Single error correction error Reset type: SYSRST

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7 FRI_SEC_CLR Register (Offset = 1034h) [Reset = 00000000h]

FRI_SEC_CLR is shown in Figure 12-11 and described in Table 12-13.

Return to the Summary Table.

FRI single error correction clear

Figure 12-11. FRI_SEC_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SEC
R-0-0h															R-0/W1C-0h

Table 12-20. FRI_SEC_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	SEC	R-0/W1C	0h	writing '1' will clear FRI_SEC_FLAG[SEC] register. Reset type: SYSRST

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8 FRI_SEC_ADDR Register (Offset = 1038h) [Reset = 00000000h]

FRI_SEC_ADDR is shown in Figure 12-12 and described in Table 12-14.

Return to the Summary Table.

FRI single error correction address

Figure 12-12. FRI_SEC_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-22. FRI_SEC_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Single error correction error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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9 FRI_SEC_MSTID Register (Offset = 103Ch) [Reset = 00000000h]

FRI_SEC_MSTID is shown in Figure 12-13 and described in Table 12-15.

Return to the Summary Table.

FRI single error correction master id

Figure 12-13. FRI_SEC_MSTID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTID							
R-0-0h																								R-0h							

Table 12-24. FRI_SEC_MSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R-0	0h	Reserved
7-0	MSTID	R	0h	Single error correction error master ID. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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10 FRI_DED_FLAG Register (Offset = 1050h) [Reset = 00000000h]

FRI_DED_FLAG is shown in Figure 12-14 and described in Table 12-16.

Return to the Summary Table.

FRI double error detection flag

Figure 12-14. FRI_DED_FLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						DIAG_DED	DED
R-0-0h						R-0h	R-0h

Table 12-26. FRI_DED_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	DIAG_DED	R	0h	diagnostic Double error detect error Reset type: SYSRST
0	DED	R	0h	Double error detect error Reset type: SYSRST

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11 FRI_DED_CLR Register (Offset = 1054h) [Reset = 00000000h]

FRI_DED_CLR is shown in Figure 12-15 and described in Table 12-17.

Return to the Summary Table.

FRI double error detection clear

Figure 12-15. FRI_DED_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						DIAG_DED	SEC
R-0-0h						R-0/W1C-0h	R-0/W1C-0h

Table 12-28. FRI_DED_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	DIAG_DED	R-0/W1C	0h	writing '1' will clear FRI_DED_FLAG[DIAG_DED] register. Reset type: SYSRST
0	SEC	R-0/W1C	0h	writing '1' will clear FRI_DED_FLAG[DED] register. Reset type: SYSRST

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12 FRI_DED_ADDR Register (Offset = 1058h) [Reset = 00000000h]

FRI_DED_ADDR is shown in Figure 12-16 and described in Table 12-18.

Return to the Summary Table.

FRI double error detection address

Figure 12-16. FRI_DED_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-30. FRI_DED_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Single error correction error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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13 FRI_DED_MSTID Register (Offset = 105Ch) [Reset = 00000000h]

FRI_DED_MSTID is shown in Figure 12-17 and described in Table 12-19.

Return to the Summary Table.

FRI double error detection master id

Figure 12-17. FRI_DED_MSTID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTID							
R-0-0h																								R-0h							

Table 12-32. FRI_DED_MSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R-0	0h	Reserved
7-0	MSTID	R	0h	Single error correction error master ID. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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14 SYSMEM_PAR_FLAG Register (Offset = 10B0h) [Reset = 00000000h]

SYSMEM_PAR_FLAG is shown in Figure 12-18 and described in Table 12-20.

Return to the Summary Table.

SYSMEM parity error flag

Figure 12-18. SYSMEM_PAR_FLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						WR_PAR	RD_PAR
R-0h						R-0h	R-0h

Table 12-34. SYSMEM_PAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved Reset type: HASH(0x4113de0)
1	WR_PAR	R	0h	Parity error during write Reset type: SYSRST
0	RD_PAR	R	0h	Parity error during read Reset type: SYSRST

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15 SYSMEM_PAR_CLR Register (Offset = 10B4h) [Reset = 00000000h]

SYSMEM_PAR_CLR is shown in Figure 12-19 and described in Table 12-21.

Return to the Summary Table.

SYSMEM parity error clear

Figure 12-19. SYSMEM_PAR_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						WR_PAR	RD_PAR
R-0h						R/W1C-0h	R/W1C-0h

Table 12-36. SYSMEM_PAR_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved Reset type: HASH(0x3fc32e8)
1	WR_PAR	R/W1C	0h	writing '1' will clear SYSMEM_PAR_FLAG[WR_PAR] register. Reset type: SYSRST
0	RD_PAR	R/W1C	0h	writing '1' will clear SYSMEM_PAR_FLAG[RD_PAR] register. Reset type: SYSRST

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16 SYSMEM_PAR_ADDR Register (Offset = 10B8h) [Reset = 00000000h]

SYSMEM_PAR_ADDR is shown in Figure 12-20 and described in Table 12-22.

Return to the Summary Table.

SYSMEM parity error address

Figure 12-20. SYSMEM_PAR_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-38. SYSMEM_PAR_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Parity error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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17 SYSMEM_PAR_MSTID Register (Offset = 10BCh) [Reset = 00000000h]

SYSMEM_PAR_MSTID is shown in Figure 12-21 and described in Table 12-23.

Return to the Summary Table.

SYSMEM parity error master id

Figure 12-21. SYSMEM_PAR_MSTID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTID							
R-0h																								R-0h							

Table 12-40. SYSMEM_PAR_MSTID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved Reset type: HASH(0x3ef1670)
7-0	MSTID	R	0h	Parity error master ID. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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18 TMUROM_PAR_FLAG Register (Offset = 10D0h) [Reset = 00000000h]

TMUROM_PAR_FLAG is shown in Figure 12-22 and described in Table 12-24.

Return to the Summary Table.

TMUROM parity error flag

Figure 12-22. TMUROM_PAR_FLAG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PAR
R-0h															R-0h

Table 12-42. TMUROM_PAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x40c4ec0)
0	PAR	R	0h	Parity error Reset type: SYSRST

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19 TMUROM_PAR_CLR Register (Offset = 10D4h) [Reset = 00000000h]

TMUROM_PAR_CLR is shown in Figure 12-23 and described in Table 12-25.

Return to the Summary Table.

TMUROM parity error clear

Figure 12-23. TMUROM_PAR_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PAR
R-0h															R/W1C-0h

Table 12-44. TMUROM_PAR_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x4014860)
0	PAR	R/W1C	0h	writing '1' will clear TMUROM_PAR_FLAG[PAR] register. Reset type: SYSRST

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20 TMUROM_PAR_ADDR Register (Offset = 10D8h) [Reset = 00000000h]

TMUROM_PAR_ADDR is shown in Figure 12-24 and described in Table 12-26.

Return to the Summary Table.

TMUROM parity error address

Figure 12-24. TMUROM_PAR_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	ADDRESS														
R-0h																	R-0h														

Table 12-46. TMUROM_PAR_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved Reset type: HASH(0x401b2f0)
14-0	ADDRESS	R	0h	Parity error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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21 TMUROM_PAR_TYPE Register (Offset = 10DCh) [Reset = 00000000h]

TMUROM_PAR_TYPE is shown in Figure 12-25 and described in Table 12-27.

Return to the Summary Table.

TMUROM parity error type

Figure 12-25. TMUROM_PAR_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TYPE		
R-0h													R-0h		

Table 12-48. TMUROM_PAR_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved Reset type: HASH(0x3eee288)
2-0	TYPE	R	0h	Parity error type. This field will be cleared along with the corresponding flag clear. [0] - Y0i ROM table read has parity error [1] - S1i ROM table read has parity error [2] - S2i ROM table read has parity error Reset type: SYSRST

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22 SYSMEM_ACC_FLAG Register (Offset = 10F0h) [Reset = 00000000h]

SYSMEM_ACC_FLAG is shown in Figure 12-26 and described in Table 12-28.

Return to the Summary Table.

SYSMEM access error flag

Figure 12-26. SYSMEM_ACC_FLAG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ERR
R-0h															R-0h

Table 12-50. SYSMEM_ACC_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x40ff918)
0	ERR	R	0h	SYSMEM access error Reset type: SYSRST

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23 SYSMEM_ACC_CLR Register (Offset = 10F4h) [Reset = 00000000h]

SYSMEM_ACC_CLR is shown in Figure 12-27 and described in Table 12-29.

Return to the Summary Table.

SYSMEM access error clear

Figure 12-27. SYSMEM_ACC_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ERR
R-0h															R/W1C-0h

Table 12-52. SYSMEM_ACC_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x409a9f8)
0	ERR	R/W1C	0h	writing '1' will clear SYSMEM_ACC_FLAG[ERR] register. Reset type: SYSRST

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24 SYSMEM_ACC_ADDR Register (Offset = 10F8h) [Reset = 00000000h]

SYSMEM_ACC_ADDR is shown in Figure 12-28 and described in Table 12-30.

Return to the Summary Table.

SYSMEM access error address

Figure 12-28. SYSMEM_ACC_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-54. SYSMEM_ACC_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	SRAM access error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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25 SYSMEM_ACC_TYPE Register (Offset = 10FCh) [Reset = 00000000h]

SYSMEM_ACC_TYPE is shown in Figure 12-29 and described in Table 12-31.

Return to the Summary Table.

SYSMEM access error type

Figure 12-29. SYSMEM_ACC_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											TYPE			
R-0h																											R-0h			

Table 12-56. SYSMEM_ACC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved Reset type: HASH(0x3d414c8)
4-0	TYPE	R	0h	SRAM access error type. This field will be cleared along with the corresponding flag clear. [4] - CBUS Access Error [3] - SBUS Access Error [2] - Write Error [1] - Read Error [0] - Fetch Error Note: Under the rare condition of both CBUS and SBUS access errors occurring at the same time, bit[4] and bit[3] will be set together to indicate the same, but bits[2:0] (as well as SYSMEM_ACC_ADDR) will convey information only realted to the CBUS access error. Under this condition, the CBUS access error has to be debugged, fixed and rerun before proceeding to debug the SBUS access error. Reset type: SYSRST

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26 ECATRAM_PAR_FLAG Register (Offset = 1110h) [Reset = 00000000h]

ECATRAM_PAR_FLAG is shown in Figure 12-30 and described in Table 12-32.

Return to the Summary Table.

EtherCAT RAM parity error flag

Figure 12-30. ECATRAM_PAR_FLAG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PAR
R-0h															R-0h

Table 12-58. ECATRAM_PAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x3dd2b88)
0	PAR	R	0h	Parity error Reset type: SYSRST

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27 ECATRAM_PAR_CLR Register (Offset = 1114h) [Reset = 00000000h]

ECATRAM_PAR_CLR is shown in Figure 12-31 and described in Table 12-33.

Return to the Summary Table.

EtherCAT RAM parity error clear

Figure 12-31. ECATRAM_PAR_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															PAR
R-0h															R/W1C-0h

Table 12-60. ECATRAM_PAR_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved Reset type: HASH(0x40c5958)
0	PAR	R/W1C	0h	writing '1' will clear ECATRAM_PAR_FLAG[PAR] register. Reset type: SYSRST

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28 ECATRAM_PAR_ADDR Register (Offset = 1118h) [Reset = 00000000h]

ECATRAM_PAR_ADDR is shown in Figure 12-32 and described in Table 12-34.

Return to the Summary Table.

EtherCAT RAM parity error address

Figure 12-32. ECATRAM_PAR_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

Table 12-62. ECATRAM_PAR_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Parity error address. This field will be cleared along with the corresponding flag clear. Reset type: SYSRST

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Chapter 13

Flash (NVM)

The Flash module provides nonvolatile memory (NVM) for storing executable code and data.

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13.1 Introduction to Flash

Flash is an electrically erasable/programmable nonvolatile memory that can be programmed and erased many times to ease code development. Flash memory can be used primarily as a program memory for the core, and secondarily as static data memory. This section describes the proper sequence to configure the wait states and operating mode of Flash. This section also includes information on how to improve Flash performance by enabling the Flash cache mode, and the SECDED safety feature. The nonvolatile memory system provides in-system programmable flash memory for storing executable code and data. This chapter describes the functionality provided by the nonvolatile memory system.

13.1.1 Flash Features

Key features of the Flash nonvolatile memory system include:

- Two Flash Banks up to 256KB each (refer to the device data sheet for flash sizes)
- In-circuit program and erase supported across the entire supply voltage range
- Flash commands for Program, Erase, Mode Change, and Read-verify functions
- Internal programming voltage generation
- 128-bit flash word size (144-bit when ECC is present)
- Static write protection (latched at boot and held until Power on Reset)
- Dynamic write protection (configurable at runtime)
- Sector (2KB) and Bank (up to 256KB) Erase
- Automatic hardware pre-verification to extend flash bank longevity
- Automatic hardware post-verification of program/erase
- ECC Single Error Correction Dual Error Detection (SECDED) protection
- Bank address swap mode (for OTA dual-image firmware updates)

13.1.2 System Components

The nonvolatile memory system consists of three components (listed below):

- One or more flash memory banks (for storing code and data)
- The flash controller (for managing all program/erase operations on the flash banks)
- The read interface (for interfacing the flash banks to the CPU and peripheral bus)

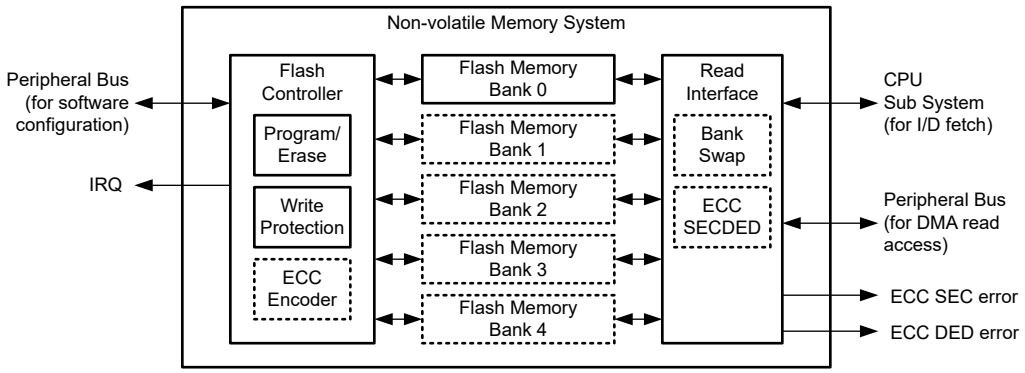


Figure 13-1. Non-volatile Memory System Components

Note

AM13E232x devices have 2 flash memory banks.

13.1.3 Terminology

Key flash bank terms are defined in this section to be used as a reference for the rest of this chapter.

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Table 13-1. NVM System Terminology

Term	Definition	Size
Flash word	Basic data size for program and read operations on the flash memory (also the read bus width to the system)	128 data bits (144 bits with ECC)
Word line	Group of flash words within a sector, with maximum program operation limit before sector erase	16 flash words (256 data bytes, optionally 16 ECC bytes)
Sector	Group of word lines that are erased together (minimum erase resolution of the flash memory)	8 word lines (2048 data bytes, optionally 128 ECC bytes)
Bank	Group of sectors that can be mass erased in one operation. Only one read, program, erase, or verify operation can run concurrently on a given bank.	Variable
Region	Logical assignment of a region of flash memory from a bank.	Variable

13.2 Flash Controller

The flash controller manages all program, erase, and verification operations performed on the nonvolatile memory system. Memory-mapped registers exist in the peripheral region of the device memory map which must be configured by software to perform operations on the flash memory.

TI provides software abstraction for the flash controller as a part of the DriverLib layer of the software development kit (SDK). TI recommends using the DriverLib abstraction layer when operating on the flash memory with software, but this is not a mandatory requirement. To use the DriverLib software abstraction layer to perform operations on the flash memory, review the software development kit (SDK) documentation provided separately from this document. To directly operate on the flash memory with using low level register accesses to the flash controller, review the remainder of this section in detail.

Note

The flash control registers (FLASH_CTRL_REGS and NVMNW_REGS) will not always be configured to default values after a reset. This can occur if the boot configuration routine (BCR) or boot strap loader (BSL) performs an operation on the flash memory during boot. When configuring the flash control registers for an operation, verify that all registers that are relevant for the operation are correctly configured.

13.2.1 Overview of Flash Controller Commands

All writes to the NVMNW_REGS registers are protected by a semaphore in the GSC module. To write to the NVMNW_REGS, software must:

1. Grab the flash semaphore by writing a '1' to the flash semaphore request register FPC_FLSEMREQ.REQ bit from GSC_REGS.
2. Verify that the semaphore is sucessfully held by the CPU by checking that the FPC_FLSEMSTAT.ASSIGNED and FPC_FLSEMSTAT.MATCH bits are set. If these bits are '0', go back to step 1 and re-request the semaphore until the bits are set to '1'.
3. Perform necessary writes to NVMNW_REGS registers.
4. Release the semaphore by writing a '1' to the FPC_FLSEMCLR.CLR bit

Operations on the flash memory are executed by configuring the command type (CMDTYPE) and command control (CMDCTL) registers for the desired command, along with any other registers which must be configured for a particular command, and writing 0x01 to the command execute (CMDEXEC) register to initiate the command.

When 0x01 is set in CMDEXEC, the commanded operation begins executing. While an operation is executing, most configuration registers are blocked for writes until the operation completes. Some registers (for example, mask registers) can change state under hardware control while the operation runs to completion. The flash controller indicates completion of the commanded operation by setting the CMDDONE bit in the command status (STATCMD) register. The flash controller also sources an interrupt vector to the CPU subsystem to indicate a “DONE” status when an operation has completed.

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The software sequence of setting the CMDEXEC bit and waiting for the CMDDONE response must be executed from either the device SRAM or from a different flash bank from the bank that is being operated on, as the flash controller takes control of the flash bank undergoing the operation. Reads to the flash bank that is being operated on while the flash controller is executing the command are not predictable.

The flash controller provides five basic commands for operating on the flash memory, specified in the COMMAND field of the CMDTYPE register. These commands are described in Table 13-2.

Table 13-2. Flash Controller Commands

Command	Description
NOOP	No operation (default setting).
PROGRAM	Selects a program operation on the flash memory.
ERASE	Selects an erase operation on the flash memory.
READVERIFY	Selects a standalone read verify operation.

There are two additional commands: Mode Change for only changing the bank and pump modes (which are otherwise set automatically by hardware) and no other operation; and Clear Status.

Note

TI recommends calling the clear status command (CMDTYPE = 0x5) before calling any flash operation.

13.2.2 Command Diagnostics

The flash controller updates several software-readable registers to communicate information about an initiated operation.

13.2.2.1 Command Status

The STATCMD register is a read-only register which provides diagnostic information about an operation which is been initiated or completed. The CMDINPROGRESS bit indicates that an operation is currently ongoing. The CMDDONE bit indicates that an operation has completed. These bits can be polled by software to determine the state of the flash controller during operations.

In addition, the STATCMD register has the following bitfields for additional diagnostic information:

- CMDPASS: Command pass bit to indicate if a command passed (valid when CMDDONE is 1).
- FAILWEPROT: Indicates the command failed due to Write/Erase protect sector violation.
- FAILVERIFY: Indicates the command failed due to verify error.
- FAILILLADDR: Indicates the command failed due to the use of an illegal address.
- FAILMODE: Indicates the command failed because a bank is set to a mode other than READ. Program and Erase commands cannot be initiated unless all banks are in READ mode.
- FAILINVDATA: Indicates that the PROGRAM command failed because a program attempted to store a 0 value as a 1.
- FAILMISC: This is an extra bit that indicates the command failed due to error outside of what is currently defined.

13.2.2.2 Address Translation

The address status (STATADDR) register is a read-only register which can be read to determine the current bank ID, region ID, and bank address which the flash controller is pointing to. These values can increment during execution of certain commands, in which case the value present after the completion of a command indicates the last address touched by the flash controller.

13.2.3 NOOP Command

When not using the flash controller, it is best to set the CMDTYPE.COMMAND field to NOOP to prevent any unintentional operations on the flash memory in the event that the CMDEXEC bit is unintentionally set. Executing a NOOP command has no effect on the flash memory.

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13.2.4 PROGRAM Command

The PROGRAM command is used to write (program) the flash memory. Specifically, the purpose of a PROGRAM operation is to configure the flash bits in one or more flash words from the nondeterministic erased state to the deterministic programmed state. Once a byte is programmed using the PROGRAM command, the byte can not be re-programmed unless the sector is erased using the ERASE command.

All devices support single flash word programming of 128 data bits (plus 16 ECC bits) at a time, with control to limit the scope of a program operation to specific bytes within a 128-bit flash word.

AM13E232x devices additionally have support for a multi-word programming mode where 2 or 4 flash words can be written with a single commanded operation. Multi-word programming, when available, significantly speeds up programming when multiple words need to be programmed (for example, during production programming or firmware updates).

13.2.4.1 Program Bit Masking Behavior

The flash controller provides a program verification mechanism to extend the lifetime of the flash bank. During program operations, the command data (CMDDATAx) registers are used by the flash controller as a programming bit mask to indicate which specific bits in the flash word require program pulses. As a result, data which is loaded into the CMDDATAx registers before starting the program operation will be lost from the CMDDATAx registers during and/or upon completion of the program operation. If the same data is to be programmed again, the CMDDATAx registers must be re-loaded by software with the correct data values to be programmed.

13.2.4.2 Target Data Alignment

There are two options for loading data to be programmed: direct mode or indexed mode. The programmer must select the mode that is most suitable to the application requirements.

Additional alignment rules apply when loading data into the CMDDATAx and CMDECCx registers on devices that support multiword programming, even if the multiword programming feature is not used and only single word programming is not used.

- 1-word program operations must have CMDADDR (the target system address) aligned to a 0b000 boundary (for example, the 3 LSBs in CMDADDR must be zero).
- 2-word program operations must have CMDADDR (the target system address) aligned to a 0b0000 boundary (for example, the 4 LSBs in CMDADDR must be zero).
- 4-word program operations must have CMDADDR (the target system address) aligned to a 0b0.0000 boundary (for example, the 5 LSBs in CMDADDR must be zero).

Direct Data Load

To configure a program operation with direct data loading, the target data is loaded into the appropriate CMDDATAx registers based on the number of flash words supported by the device, the target address alignment, and the target data size. For example, if a 4-word program operation is to be initiated on a device supporting 4-word programming, the CMDDATA0-CMDDATA7 registers are populated with the target data. If ECC is being specified directly (rather than automatically calculated by the flash controller) then the appropriate CMDECCx registers also needs to be populated with the ECC values for each data word being programmed.

Indexed Data Load

Rather than buffering data into all the CMDDATAx registers individually, it is possible to use only the CMDDATA0-CMDDATA1 registers in combination with an index register (CMDDATAINDEX) to indicate the flash word offset of the data being loaded. In this way, the index can be adjusted for each word loaded, and each target data word can be written to the same 128-bit space (CMDDATA0-CMDDATA1). When an index is applied, the loaded data is mapped by the hardware into the appropriate CMDDATAx register. For example, if a 4-word program operation is to be initiated on a device supporting 4-word programming, the CMDDATA1:0 registers are loaded 4 times with the target data, with CMDDATAINDEX being incremented by one before each new word is loaded into CMDDATA1:0.

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Alignment Rules

The alignment rules for each device configuration (2 or 4 words) is given in the tables below with guidance on how target data must be placed with the CMDDATAx, CMDECCx, and CMDDATAINDEX registers for 1, 2, or 4 word programming operations.

Table 13-3. Data Load Alignment for Programming of 2 Flash Words

Direct Load Registers	Indexed Load Index	1 Word Aligned to 0b000	2 Words Aligned to 0b0000	4 Words Aligned to 0b0.0000
CMDDATA1:0 / CMDECC0	CMDINDEX = 0	Target data word 0 if the target address ends in 0b0000	Target data word 0	Not supported
CMDDATA3:2 / CMDECC1	CMDINDEX = 1	Target data word 0 if the target address ends in 0b1000	Target data word 1	

Table 13-4. Data Load Alignment for Programming of 4 Flash Words

Direct Load Registers	Indexed Load Index	1 Word Aligned to 0b000	2 Words Aligned to 0b0000	4 Words Aligned to 0b0.0000
CMDDATA1:0 / CMDECC0	CMDINDEX= 0	Target data word 0 if the target address ends in 0b0.0000	Target data word 0 if the target address ends in 0b0.0000	Target data word 0
CMDDATA3:2 / CMDECC1	CMDINDEX= 1	Target data word 0 if the target address ends in 0b0.1000	Target data word 1 if the target address ends in 0b0.0000	Target data word 1
CMDDATA5:4 / CMDECC2	CMDINDEX= 2	Target data word 0 if the target address ends in 0b1.0000	Target data word 0 if the target address ends in 0b1.0000	Target data word 2
CMDDATA7:6 / CMDECC3	CMDINDEX= 3	Target data word 0 if the target address ends in 0b1.1000	Target data word 1 if the target address ends in 0b1.0000	Target data word 3

13.2.4.3 Executing a PROGRAM Operation

To program the flash memory:

1. Select the command in the CMDTYPE register:
   a. Set the COMMAND field in the CMDTYPE register to PROGRAM.
   b. Set the SIZE field in the CMDTYPE register to the desired size (1, 2, or 4 flash words). The hardware does not check for invalid configuration of the SIZE field; software must verify that the selection option is supported by the device. Note that SECTOR and BANK sizes are not valid sizes for PROGRAM operations. These sizes only apply to erase operations.
2. Configure the program command in the CMDCTL register:
   a. On devices with ECC, the flash controller by default generates the needed ECC bits from the data during the PROGRAM operation. Optionally, software can override the hardware ECC code generation and manually provide the ECC code to be programmed by setting the ECCGENOVR bit in CMDCTL register.
3. Select the target programming address in the CMDADDR and CMDBYTEN register:
   a. Load the target system address into the CMDADDR register to indicate the base address from which programming starts. The target address must be a flash word address (128-bit aligned). The flash controller translates the system address into the applicable flash region, bank ID, and bank address. If desired, after the operation completes the flash region, bank ID, and bank address can be read from the STATADDR register. In a multi-word program, STATADDR indicates the bank ID and the final address programmed.
   b. If subword programming (programming of less than the full 128 or 144 bit flash word) is desired, configure the CMDBYTEN register to set the bytes within the addressed flash word which are to be programmed. Each bit in CMDBYTEN corresponds to a byte in the addressed flash word to be programmed, including the ECC byte. For example, programming of the ECC code can be masked by clearing bit 8 in CMDBYTEN while programming the data bytes of the flash word. Note that there is a

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maximum number of program operations allowed per word line before a sector erase must be applied (see the device specific data sheet for the maximum).

4. Load the data to program into the CMDDATAx registers:
   a. For a single flash word programming operation (128 or 144 bits depending on the presence of ECC), load the data into the CMDDATAx registers consistent with the alignment requirements (for devices which only support single-word programming, CMDDATA0 and CMDDATA1 are always used regardless of the target address).
   b. For multi-word programming (if available and selected), load data into the CMDDATAx registers consistent with the alignment rules and the size of the multi-word program operation specified in step 1.
   c. If ECCGENOVR in the CMDCTL register is set above (disabling hardware ECC code generation), then write the ECC data in the CMDDATAECC0 register (for single word programming) and optionally additional CMDDATAECCx registers as applicable for multi-word programming.
   d. Note that the CMDDATA registers are used as bit masking registers by the flash controller during the program operation; after the operation completes, the values written to these registers are overwritten by the flash controller.
5. Validate the write protection scheme is configured to allow writes to the target addresses (see the write protection section of this guide for additional information on configuring write protection).
6. Execute the program operation by writing 0x1 to the CMDEXEC register.
7. Monitor for completion of the program operation:
   a. The STATCMD register can be polled to determine the status of the program operation. The CMDINPROGRESS bit is set by hardware as soon as the command is initiated. The CMDDONE bit is set when the operation terminates.
   b. When CMDDONE is set, the CMDPASS bit is reset or set at the same time to indicate whether the operation completed successfully or failed. If a program attempted to load on a protected region, the FAILWEPROT or FAILILLADDR bit is asserted depending on dynamic or static write protection. If the program operation cannot be completed successfully within the maximum program pulse count limit FAILVERIFY is asserted. See the device-specific data sheet for maximum program times.
8. After completion of a program operation, the flash controller configures several settings:
   a. All dynamic write protection registers are set to a protected state (to protect against inadvertent programming)
   b. All data registers are set to 1.
   c. All program byte enables are cleared to 0.
9. Following programming of the flash memory, there can be stale data in the processor's cache logic. Before reading programmed locations, TI recommends to first flush the cache in the CPU subsystem.

Note

Direct user configuration is not required. The TI Flash API takes care of these steps for the user. This information is provided for debug/reference.

13.2.5 ERASE Command

The erase command is used to erase individual sectors of flash memory (for MAIN, NONMAIN, or DATA regions) or a complete bank of flash memory (for MAIN regions only). Flash memory region types are described in Section 3.5.2.2 . From this erased state, bits can later be programmed to a ‘0’ state or a '1' state as desired using the PROGRAM command. It is not possible to erase with a resolution lower than one sector (1KB) with sector alignment. For devices with multiple banks, a bank erase must be executed on all banks to erase the entire MAIN region on the device.

13.2.5.1 Erase Sector Masking Behavior

The flash controller provides an erase verification mechanism to extend the lifetime of the flash bank. The CMDWEPROTx registers are used as an erase mask and are manipulated by the flash controller during the execution of the erase operation. At the end of all erase operations, the CMDWEPROTx registers are set to a

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fully protected state to prevent against inadvertent programming and must be re-configured before attempting another program or erase operation.

13.2.5.2 Executing an ERASE Operation

To erase a sector or bank of the flash memory, follow these steps:

1. Select the command in the CMDTYPE register:
   a. Set the COMMAND field in the CMDTYPE register to ERASE.
   b. Set the SIZE field in the CMDTYPE register to SECTOR or BANK. Sizes other than SECTOR or BANK (for example, ONEWORD) are not supported by the ERASE command. It is the responsibility of software to check the configuration before issuing an ERASE command.
2. Select the target erase address in the CMDADDR register:
   a. Store the target system address into the CMDADDR register to indicate the base address of the sector or bank to be erased. When performing a bank erase with write protection enabled (such that only unprotected sectors are erased), ensure that the address written to CMDADDR is in an unprotected sector. The flash controller will translate the system address into the applicable flash region, bank ID, and bank address. If desired, after the operation completes the flash region, bank ID, and bank address can be read from the STATADDR register.
3. Ensure the write protection scheme is configured to allow writes to the target sectors (see the write protection section of this guide for additional information on configuring write protection).
4. Execute the erase operation by writing 0x1 to the CMDEXEC register.
5. Monitor for completion of the erase operation:
   a. The STATCMD register can be polled to determine the status of the erase operation. The CMDINPROGRESS bit will be set by hardware as soon as the command is initiated. The CMDDONE bit will be set when the operation terminates. When CMDDONE is set, the CMDPASS bit will be reset or set at the same time to indicate whether the operation completed successfully or failed.
   b. If an erase was attempted on a protected region, the FAILWEPROT bit is asserted.
   c. If the erase operation cannot be completed successfully within the maximum erase pulse count limit, FAILVERIFY will be asserted.
6. After completion of the erase operation, the flash controller will configure several settings to protect against inadvertent programming:
   a. All dynamic write protection registers are set to a protected state.

13.2.6 READVERIFY Command

The read verify command can be used to read a flash location and compare the data to data which is preloaded into the CMDDATA registers of the flash controller. The command can be applied to a single flash word, multiple flash words (if the device supports multi-word programming), an entire sector, or an entire bank. When performing a read verify on an entire sector or bank, the data in CMDDATAx will be re-used.

13.2.6.1 Executing a READVERIFY Operation

To execute a read verify command, follow these steps:

1. Select the command in the CMDTYPE register:
   a. Set the COMMAND field in the CMDTYPE register to READVERIFY.
   b. Set the SIZE field in the CMDTYPE register to the desired size.
2. Configure the read verify command in the CMDCTL register:
   a. If the desire is to manually provide ECC bits along with the data, set the ECCGENOVR bit in the CMDCTL register. If ECCGENOVR is cleared, the flash controller will generate ECC bits for comparison based on the provided compare data.
3. Select the target address to verify on the CMDADDR register:

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a. Load the target system address into the CMDADDR register to indicate the base address to be verified. The flash controller will translate the system address into the applicable flash region, bank ID, and bank address. If desired, after the operation completes the flash region, bank ID, and bank address can be read from the STATADDR register.

4. Load the data to verify into the CMDDATAx registers:
   a. For single word verification, write the data to be verified to the CMDDATA0 and CMDDATA1 registers. For multi-word verification, if available on the target device, write the data to be verified to the appropriate CMDDATAx registers beyond CMDDATA0 and CMDDATA1.
5. Configure the byte enable settings in the CMDBYTEN register:
   a. Any CMDBYTEN bit set to logic “0” will mask the associated data byte from being compared during the execution of the READVERIFY command. This can be used to verify data less than one flash word (less than 64 bits).
6. Execute the read verify operation by writing 0x1 to the CMDEXEC register.
7. Monitor for completion of the read verify operation:
   a. The STATCMD register can be polled to determine the status of the erase operation. The CMDINPROGRESS bit will be set by hardware as soon as the command is initiated. The CMDDONE bit will be set when the operation terminates. When CMDDONE is set, the CMDPASS bit will be reset or set at the same time to indicate whether the read verification passed or failed.
   b. The FAILVERIFY bit in STATCMD will be set if any data read from the flash did not match the expected data loaded in CMDDATAx.
8. After completion of the read verify operation, the flash controller will configure several settings:
   a. All dynamic write protection registers are set to a protected state (to protect against inadvertent programming).
   b. All data registers are set to ‘1’s.
   c. All program byte enables are cleared to ‘0’s.

13.2.7 Overriding the System Address With a Bank ID, Region ID, and Bank Address

Normally, flash controller commands are targeted to a specific flash location by loading a system memory map address into the CMDADDR register. This is the recommended way to specify the target address for a PROGRAM, ERASE, or READVERIFY command. In this mode of operation, the flash controller automatically translates the system address into the corresponding bank ID, region ID, and bank address which are used to execute the command on the flash memory. Application software does not need to specify these items individually; only the system address is needed.

However, in some circumstances direct specification of the target flash bank, region, and address in the specified bank/region is needed. For example, if the desire is to erase a complete bank when doing a mass erase operation on the device, application software actually does not need to have any knowledge of the system address of the bank to be erased- the software only needs to specify the bank ID and region ID to the flash controller to erase the bank.

To use the flash controller to execute a command in address override mode, set the ADDRXLATEOVR bit in the CMDCTL register, and specify the bank ID, region, and bank address before executing the command. To return to system addressed mode, clear ADDRXLATEOVR. ADDRXLATEOVR is cleared by default (supporting system address operation).

Example Case - Bank Erase with ADDRXLATEOVR

To erase the MAIN region of BANK0 by specifying the bank ID and region instead of the system address, follow the steps in Section 13.2.5.2 , but replace step 2 with the alternate steps given below:

1. Set the ADDRXLATEOVR bit in CMDCTL to enable address translation override mode
2. Specify BANK0 by setting the BANKSEL field to 0x1 in the CMDCTL register

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3. Specify the MAIN region by setting the REGIONSEL field to 0x1 in the CMDCTL register
4. Set the CMDADDR register to 0x0000.0000

13.3 Write Protection

The flash controller provides two write protection mechanisms (one static, one dynamic) which are applied in parallel (logical OR) to protect user-specified sectors during any attempted program or erase operation. If a program or erase operation is issued to a write protected flash sector, the operation terminates with a FAILWEPROT error reported in the STATCMD register.

Note

This is the lowest priority of Write Protection, after Global Security Controller configurations of 2 layers (Life-cycle HW Blocking + WDPROC Blocking). Refer to the GSC Chapter for additional details.

13.3.1 Write Protection Resolution

The write protection resolution for both the static and dynamic write protection mechanisms is dependent on the flash bank and memory region which is being protected.

Flash Bank	Memory Region	Write Protection Resolution
0	NONMAIN	512B (Entire Region)
	MAIN	1KB (1 sector) for first 32KB (32 sectors) 8KB (8 sectors) for remaining sectors
1	NONMAIN	512B (Entire Region)
	MAIN	8KB (8 sectors)
	DATA	1KB (1 sector)

13.3.2 Static Write Protection

The static write protection scheme is configured and latched during device boot by the immutable ROM boot code before the main application in flash can execute. After a flash sector is configured to be write protected through the static write protection mechanism, software cannot remove the protection at runtime without a reboot. Thus, sectors protected by static write protection can be thought of as immutable after boot. This type of protection is useful for protecting a custom bootloader in a dual-image application, or for extending the secure root of trust from the ROM boot code into a portion of the main flash region to enable a secure boot manager with locked public keys.

The static write protection scheme is configured by programming the appropriate bits in the NONMAIN flash region, which is read by the boot code before the main application starts. The NONMAIN flash sector can be statically write protected, resulting in a system in which the static write protection scheme is fully permanent and cannot be modified. If the NONMAIN sector is configured to be statically protected, along with any other flash sectors, all statically protected flash sectors can be functionally viewed as read only memory which cannot be updated by any means.

Static write protection can be configured for all sectors of flash memory across all banks present on a device. Program or erase static write protected area will cause illegal address failure, and the FAILILLADDR bit in STATCMD will be set. Instructions for configuring the static write protection, along with the rest of the NONMAIN region, are given in *Boot Configuration*.

13.3.3 Dynamic Write Protection

The dynamic write protection scheme is intended to be configured at runtime by software. This scheme provides a simple way for application software to specify sectors to protect from modification by any program or erase operations that are issued with the flash controller. Unlike the static write protection mechanism, the dynamic mechanism is not lockable and thus does not provide any level of data security.

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There are two primary uses for dynamic write protection. First, it provides an extra level of robustness against unintentional program or erase of specified sectors in applications that involve in-system programming for either firmware updates or EEPROM emulation. Second, it provides a way to simplify a situation where a bank erase is desired but a small number of sectors should not be erased when a bank erase command is issued. One example would be an application running on a single-bank device in which most of the MAIN region sectors are used to store the executable image, but a few sectors are used to store device-specific data that should not be erased during a firmware update. In that case, the sectors containing the device-specific data can be protected with dynamic write protection, and a bank erase command can be issued to erase all other sectors. This has the benefit that the majority of the MAIN region can be erased with a single command (a bank erase) rather than individual sector-by-sector commands, which would have a longer overall erase time and use more energy.

The dynamic write protection scheme is configured by setting up the CMDWEPROTx registers in the flash controller. The CMDWEPROTx registers cover one flash bank at a time. This means that these registers must be configured with knowledge of which flash bank an attempted program or erase operation will be applied to. Note that the CMDWEPROTx registers are reset to a protected state at the end of all program and erase operations. These registers must be re-configured by software before a new operation is initiated. Program or erase dynamic write protected area will cause write/erase protction failure, and the FAILWEPROT bit in STATCMD will be set.

13.3.3.1 Configuring Protection for the MAIN Region

The CMDWEPROTA register is used to configure the dynamic write protection for the first 32 sectors (32KB) of the MAIN region in BANK0. Each bit corresponds to one sector of the MAIN region, starting from the beginning of the MAIN region. CMDWEPROTA is only applicable to operations on the lower 32 sectors of the MAIN region of BANK0 (sectors 0-31). It is not used during program/erase operations applied to other sectors.

The CMDWEPROTB register is also used to configure the dynamic write protection for the MAIN region. There are two modes in which CMDWEPROTB is applied, depending on whether the program/erase operation is being applied to BANK0 or BANK1. In the case of a program/erase operation on BANK0, CMDWEPROTB protects sectors 32-255 in 8-sector increments (1 bit per 8KB), starting from BIT4. BIT0-BIT3 in CMDWEPROTB are ignored. The lower 32 sectors (sectors 0-31 of BANK0) are protected by CMDWEPROTA. In the case of a program/erase operation on BANK1, CMDWEPROTB protects sectors 0-255 in 8-sector increments (1 bit per 8 sectors), starting from BIT0 in CMDWEPROTB.

13.3.3.2 Configuring Protection for the NONMAIN Region

The CMDWEPROTNM register protects the NONMAIN region from program and erase. One protection bit is provided per sector.

13.4 Flash Read Interface

The Flash subsystem includes one Flash Read Interface modules (FRI-1). The Flash read interface modules provide a means for the various initiators on the system to perform read operations on Flash memory. These initiators include:

- **M33 CPU**: The CPU has one 128-bit instruction fetch bus, and two 64-bit data buses.
- **DMA**: The DMA module can perform 64-bit data reads of Flash memory.
- **Debug Interface**: A debugger connected to M33 CPU can perform data read accesses to Flash memory locations.

The Flash read interface is addressable through one or more Flash read ports. Because of bank interleaving and support for bank swapping during firmware updates, Flash code banks do not have a fixed mapping to CPU address space. Rather, each read port has a fixed address range, but can map to a different Flash region depending on the current system configuration. The Flash bank access router performs the background translation, routing read access requests to the intended bank or banks as directed by the Global Security Controller (GSC). The are two types of Flash read operations that can be performed: program instruction fetches for CPU execution, and data accesses.

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FRI-1: CPU1 Program

FRI-1 interfaces with the instruction fetch bus of the M33 CPU, and is primarily used for executing program code on the CPU. Additionally, FRI-1 is connected to all data read initiators in the system. This read interface has four read ports, numbered RP0 to RP3. These read ports are mapped to code banks depending on the configuration of BANKMODE and BANKMAP.CPU1SWAP registers in the SSU. These settings are described in subsequent sections.

FRI-3: Firmware Update Region

FRI-3 provides an address range to be used for programming and verifying an updated firmware image into the second half of Flash memory, while the current application continues to execute from the first half through FRI-1 and FRI-2 (if present). When the firmware update is complete, the Flash memory ranges can then be swapped using BANKMAP.CPUxSWAP, and the newly programmed firmware now executes from FRI-1 and FRI-2 (if present). This supports Firmware-Over-The-Air (FOTA) and Live Firmware Update (LFU) firmware upgrade mechanisms. FRI-3 does not have an instruction fetch interface—only data reads are possible from all system initiators. FRI-3 has two read ports, numbered RP0 to RP1, which are mapped to available Flash code memory.

FRI-4: Data Bank

FRI-4 is exclusively used for the data bank (FLC1.B4), and does not have an instruction fetch interface. Thus, application code cannot be executed from the data bank; only read accesses are possible from all system initiators. FRI-4 has one read port (RP0) which has a fixed mapping to the data Flash bank, and does not change based on the BANKMODE or BANKMAP.CPUxSWAP settings.

13.4.1 Bank Modes and Swapping

The BANKMODE register in the SSU_GEN_REGS register range configures the system Flash bank mode setting. These modes determine the allocation of Flash memory to primary CPUs in the system, and whether the swapping feature is enabled for firmware updates. The BANKMODE register is loaded from the BANKMGMT sector of the active code bank pair in FLC1 during device boot. The active BANKMGMT sector is determined based on the values of the BANK_STATUS and BANK_UPDATE fields; afterward, the winning BANKMGMT sector is used to configure the system BANKMODE.

The available bank mode options are described in Table 13-5.

Table 13-5. CPU Bank Modes

BANKMODE	Flash Mapping	Swap Enabled	1-CPU Devices
0	All program Flash mapped to CPU1	No	Available
1		Yes	Available
2	Reserved	N/A	N/A
3		N/A	N/A

The FLBANKSWAP.USEUPPER register bitfield in SYSCTL is used to determine the current active A/B swap setting for firmware updates using FOTA or LFU.

For specific mappings of Flash address ranges to read port addresses refer to the device data sheet.

13.4.2 Flash Wait States

When a CPU performs a read access to a Flash memory address, data is returned after (RWAIT + 1) MCLK cycles.

For an access to the SECCFG or BANKMGMT Flash regions, data is returned after 10 MCLK cycles.

RWAIT defines the number of random access wait states, and is configured using the RWAIT field in the FRDCNTL register. At reset, RWAIT defaults to a value of 2. RWAIT can be reconfigured to a lower value when

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the CPU clock frequency is low enough to accommodate the Flash access time. For a table of supported RWAIT values versus CPU clock frequency ranges, refer to the device data sheet.

For a given system clock frequency, configure RWAIT using the following formula:

$$\text{RWAIT} = \text{ceiling}\left(\frac{\text{MCLK}}{\text{FCLK}} - 1\right) \quad (12)$$

where MCLK is the system operating frequency, and FCLK is the Flash clock frequency.

FCLK must be ≤ FCLK_{max}, the allowed maximum Flash clock frequency defined in the device data sheet.

If RWAIT results in a fractional value when calculated using the above formula, round up RWAIT to the nearest integer.

Note

Zero wait state reads are only supported when MCLK <= 50MHz.

13.4.3 Buffer and Cache Mechanisms

Each Flash read interface includes mechanisms designed to maximize performance for read operations. These mechanisms include:

- A program code block cache (MAIN Region Block Cache for both Data and Code Access)
- A line buffer for data read operations (Only for NONMAIN/ENGR Regions, not MAIN region)

These mechanisms are disabled by default at device boot, and must be configured to enable them before application execution commences.

13.4.4 Flash Read Arbitration

Each Flash read interface contains multiple levels of arbitration to determine in which order concurrent read requests from multiple initiators are serviced.

1. The first level of arbitration is a fixed priority arbiter between CPU read buses. Data Read Bus 1 (DRB1) always gets a higher priority than Data Read Bus 2 (DRB2). This arbitration level enables zero-wait-state switching between the two data buses belonging to the same CPU. The actual data read bus used for a specific read request is automatically generated by the compiler.
2. The second level of arbitration is the L1 data read pipeline. This level arbitrates between data read requests generated by multiple initiators in the system. The initiators are selected using a round-robin pointer. The round-robin selection order for FRI-1, FRI-3, and FRI-4 is as follows:
   a. CPU1
   b. DMA
   c. Data Pre-read
   d. DEBUGSS

   Switching between initiators incurs a one-cycle pipeline delay, to allow for the round-robin pointer change.
3. For FRI-1, there is a third level of arbitration between fetch and data requests (L2). This arbiter is also a round-robin arbiter like the second level, with selection using the following order:
   a. Instruction fetch (CPU1 for FRI-1)
   b. L1 data read pipeline output

   Changes to the L2 round-robin pointer incur a one-cycle pipeline delay, similar to the L1 arbiter.

13.4.5 Error Correction Code (ECC) Protection

The device features an end-to-end safety architecture, with ECC logic. When a Flash data read or instruction fetch operation is performed, ECC check bits are sent along with the data bits onto the CPU program or data buses. The CPU automatically checks incoming instructions and data using the ECC bits, correcting single-bit

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data errors, and generating a fault for double-bit (uncorrectable) errors. These errors generate a regular interrupt for a single-bit error, or a non-masking interrupt (NMI) for a double-bit error.

Each 8-bit ECC code is computed based on the requested data address and 64 bits of data. For each 128-bit Flash word, there are two ECC codes (8 for the upper 64 bits and 8 for the lower 64 bits), for a total of 16 ECC bits. ECC bits can be independently read through separate FRI read port memory regions as described in the device data sheet.

For more information on ECC protections, see the Section 3 chapter.

Note

Read accesses from other initiators such as the debugger or DMA do not have ECC protection. This means flash memory reads from these initiators do not have error detection and correction enabled.

13.4.6 Procedure to Change Flash Read Interface Registers

While configuring a Flash Read Interface (FRI), no accesses to any Flash memory that is covered by the Flash Read Interface can be in progress. This includes instructions still in the CPU pipeline, data reads, and instruction prefetch operations. To be sure that no access takes place during the configuration change, follow the procedure shown below for any code that modifies the Flash Read Interface registers.

1. Start executing the application code from RAM or Flash.
2. Branch to or call the Flash configuration code (that writes the FRI registers) in RAM. This is required to properly flush the CPU pipeline before the configuration change. Any function that changes the FRI configuration must reside in RAM, and cannot execute from Flash memory using the same FRI.
3. Execute the Flash configuration code to configure the FRI registers (FRDCNTL, FRIx_INTF_CTRL, and so on).
4. At the end of the Flash configuration code execution, wait nine cycles to allow the write instructions to propagate through the CPU pipeline. This must be done before the return-from-function call is made.
5. Return to the calling function residing in Flash or RAM, and continue execution.

Note

Flash read interfaces that do not include instruction fetch capability, such as FRI-3 and FRI-4, can be configured by code executing directly from Flash, provided that no data access to the covered Flash banks is being made. In such cases, verify that no current data access to the target Flash banks is being performed by placing the FRI configuration code in a separate function. Be sure to wait nine cycles to flush the CPU pipeline before branching back to regular application execution.

13.5 Read Interface

The read interface provides the read path to the CPU subsystem (for instruction/data fetch), the read path to the peripheral bus (for use by the DMA controller or CPU), main bank address swapping, and detection and reporting of ECC SEC or DED errors.

13.5.1 Bank Address Swapping

Devices that contain more than one bank support swapping of the MAIN regions of the banks within the address space. This mechanism enables two versions of application firmware to be programmed into the device without the firmware needing to know which physical bank it exists in.

Table 13-6 gives an example of the mapping before and after a bank swap is requested for a device with a 512KB main flash split across 2 banks (256KB each).

Table 13-6. Bank Address Swap Translation

Bank and Region	Address Space Before Swap	Address Space After Swap
BANK0 MAIN	0x0000.0000 – 0x0003.FFFF	0x0004.0000 – 0x0007.FFFF
BANK1 MAIN	0x0004.0000 – 0x0007.FFFF	0x0000.0000 – 0x0003.FFFF

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After a device reset, the MAIN region of the lower bank is always mapped to the lowest address space. The application software is responsible for determining if a bank address swap is to be applied. The bank address swap control is contained within the SYSCTL module; see the SYSCTL chapter for register and bit definitions. During an address swap, the application software must meet the following constraints:

1. The software must disable interrupts before issuing the bank swap command.
2. The software must poll the bank swap status after issuing the bank swap command before proceeding with execution.
3. If the swap command and poll status routines are executing from flash, they must exist at the exact same location in both banks such that execution resumes from where it left off after the bank swap. This restriction does not apply if the bank swap and status polling is done from SRAM and not from flash memory.

13.5.2 ECC Error Handling

The read interface detects and corrects single bit errors in a 64-bit flash word (SEC) and detects dual-bit errors in a 64-bit flash word (DED). ECC checks are ignored for an “all-1’s” or “all-0’s” scenario.

13.5.2.1 Single bit (correctable) errors

Single bit errors are corrected automatically before the requested data is returned to either the CPU subsystem or the peripheral bus (DMA). Errors occurring as a result of a debug access are not reported.

13.5.2.2 Dual bit (uncorrectable) errors

Dual bit errors are detectable but not correctable and are indicated to SYSCTL. SYSCTL can be configured to generate either a nonmaskable interrupt (NMI) or a reset, as uncorrectable errors can be fatal. Errors occurring as a result of a debug access are not reported.

13.6 FLASH Registers

This Section describes the FLASH Registers.

13.6.1 FLASH Base Address Table

Table 13-7. FLASH Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
FlashRegs	FLASH_CTRL_REGS	FLASH	0x4002_8000
NvmnwRegs	NVMNW_REGS	NVMNW	0x4004_2000

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13.6.2 FLASH_CTRL_REGS Registers

Table 13-8 lists the memory-mapped registers for the FLASH_CTRL_REGS registers. All register offset addresses not listed in Table 13-8 should be considered as reserved locations and the register contents should not be modified.

Table 13-8. FLASH_CTRL_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	FRDCNTL	Flash Read Control Register		Go
Ch	FRD_INTF_CTRL	Flash Read Interface Control Register		Go

Complex bit access types are encoded to fit into small table cells. Table 13-9 shows the codes that are used for access types in this section.

Table 13-9. FLASH_CTRL_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 FRDCNTL Register (Offset = 0h) [Reset = 02000201h]

FRDCNTL is shown in Figure 13-2 and described in Table 13-10.

Return to the Summary Table.

Flash Read Control Register

Figure 13-2. FRDCNTL Register

31	30	29	28	27	26	25	24
RESERVED				RESERVED			
R-0h				R/W-2h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				RWAIT			
R-0h				R/W-2h			
7	6	5	4	3	2	1	0
RESERVED							WS0_MODE
R-0h							R/W-1h

Table 13-11. FRDCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	RESERVED	R/W	2h	Reserved
23-12	RESERVED	R	0h	Reserved
11-8	RWAIT	R/W	2h	Random read waitstate These bits indicate how many waitstates are added to a flash read/fetch access. The RWAIT value can be set anywhere from 0x1 to 0xF. For a flash access, data is returned in RWAIT+1 SYSCLK cycles. Note: The required wait states for each SYSCLK frequency can be found in the device data manual. Reset type: SYSRSn
7-1	RESERVED	R	0h	Reserved
0	WS0_MODE	R/W	1h	When set, waitstate of the flash will be forced to 0 Waitstate. When this bit is set, RWAIT and TRIMENGRRWAIT values will be ignored. Reset type: SYSRSn

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2 FRD_INTF_CTRL Register (Offset = Ch) [Reset = 00000000h]

FRD_INTF_CTRL is shown in Figure 13-3 and described in Table 13-11.

Return to the Summary Table.

Flash Read Interface Control Register

Figure 13-3. FRD_INTF_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CACHE_EN	DLB_EN	RESERVED
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 13-13. FRD_INTF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-3	RESERVED	R	0h	Reserved
2	CACHE_EN	R/W	0h	Cache enable. Affects CPU code execution and data reads from flash. 0 A value of 0 disables the cache. 1 A value of 1 enables the cache. Reset type: SYSRSn
1	DLB_EN	R/W	0h	Data Line Buffer enable. Affects DMA reads from flash. 0 A value of 0 disables the data line buffer. 1 A value of 1 enables the data line buffer. Reset type: SYSRSn
0	RESERVED	R/W	0h	Reserved

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13.6.3 NVMNW_REGS Registers

Table 13-12 lists the memory-mapped registers for the NVMNW_REGS registers. All register offset addresses not listed in Table 13-12 should be considered as reserved locations and the register contents should not be modified.

Table 13-14. NVMNW_REGS Registers

Offset	Acronym	Register Name	Group	Section
1100h	CMDEXEC	Command Execute Register		Go
1104h	CMDTYPE	Command Type Register		Go
1108h	CMDCTL	Command Control Register		Go
1120h	CMDADDR	Command Address Register		Go
1124h	CMDBYTEN	Command Program Byte Enable Register		Go
112Ch	CMDDATAINDEX	Command Data Index Register		Go
1130h	CMDDATA0	Command Data Register 0		Go
1134h	CMDDATA1	Command Data Register 1		Go
1138h	CMDDATA2	Command Data Register 2		Go
113Ch	CMDDATA3	Command Data Register Bits 3		Go
1140h	CMDDATA4	Command Data Register 4		Go
1144h	CMDDATA5	Command Data Register 5		Go
1148h	CMDDATA6	Command Data Register 6		Go
114Ch	CMDDATA7	Command Data Register 7		Go
1150h	CMDDATA8	Command Data Register 8		Go
1154h	CMDDATA9	Command Data Register 9		Go
1158h	CMDDATA10	Command Data Register 10		Go
115Ch	CMDDATA11	Command Data Register 11		Go
1160h	CMDDATA12	Command Data Register 12		Go
1164h	CMDDATA13	Command Data Register 13		Go
1168h	CMDDATA14	Command Data Register 14		Go
116Ch	CMDDATA15	Command Data Register 15		Go
11B0h	CMDDATAECC0	Command Data Register ECC 0		Go
11B4h	CMDDATAECC1	Command Data Register ECC 1		Go
11B8h	CMDDATAECC2	Command Data Register ECC 2		Go
11BCh	CMDDATAECC3	Command Data Register ECC 3		Go
11D0h	CMDWEPROTA	Command Write Erase Protect A Register		Go
11D4h	CMDWEPROTB	Command Write Erase Protect B Register		Go
1210h	CMDWEPROTNM	Command Write Erase Protect Non-Main Register		Go
13D0h	STATCMD	Command Status Register		Go
13D8h	STATPCNT	Pulse Count Status Register		Go

Complex bit access types are encoded to fit into small table cells. Table 13-13 shows the codes that are used for access types in this section.

Table 13-15. NVMNW_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

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Table 13-15. NVMNW_REGS Access Type Codes (continued)

Access Type	Code	Description
Reset or Default Value		
-n		Value after reset or the default value

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1 CMDEXEC Register (Offset = 1100h) [Reset = 00000000h]

CMDEXEC is shown in Figure 13-4 and described in Table 13-14.

Return to the Summary Table.

Command Execute Register:
Initiates execution of the command specified in the CMDTYPE register.
This register is blocked for writes after being written to 1 and prior to
STATCMD.DONE being set by the flash wrapper hardware.
flash wrapper hardware clears this register after the processing of the command
has completed.

Figure 13-4. CMDEXEC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															VAL
R-0h															R/W-0h

Table 13-17. CMDEXEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	VAL	R/W	0h	Command Execute value Initiates execution of the command specified in the CMDTYPE register. 0h (R/W) = Command will not execute or is not executing in flash wrapper 1h (R/W) = Command will execute or is executing in flash wrapper

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2 CMDTYPE Register (Offset = 1104h) [Reset = 00000000h]

CMDTYPE is shown in Figure 13-5 and described in Table 13-15.

Return to the Summary Table.

Command Type Register
This register specifies the type of command to be executed by the flash wrapper hardware.
This register is blocked for writes after CMDEXEC is written to a 1 and prior to STATCMD.DONE being set by the hardware to indicate that command execution has completed.

Figure 13-5. CMDTYPE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	SIZE			RESERVED	COMMAND		
R-0h	R/W-0h			R-0h	R/W-0h		

Table 13-19. CMDTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6-4	SIZE	R/W	0h	Command size 0h (R/W) = Operate on 1 flash word 1h (R/W) = Operate on 2 flash words 2h (R/W) = Operate on 4 flash words 3h (R/W) = Operate on 8 flash words 4h (R/W) = Operate on a flash sector 5h (R/W) = Operate on an entire flash bank
3	RESERVED	R	0h	Reserved
2-0	COMMAND	R/W	0h	Command type 0h (R/W) = No Operation 1h (R/W) = Program 2h (R/W) = Erase 3h (R/W) = ReadVerify - Perform a standalone ReadVerify operation. 4h (R/W) = Mode Change - Perform a mode change only, no other operation. 5h (R/W) = Clear Status - Clear status bits in FW_SMSTAT only. 6h (R/W) = Blank Verify - Check whether a flash word is in the erased state. This command may only be used with CMDTYPE.SIZE = ONEWORD

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3 CMDCTL Register (Offset = 1108h) [Reset = 00000000h]

CMDCTL is shown in Figure 13-6 and described in Table 13-16.

Return to the Summary Table.

Command Control Register This register configures specific capabilities of the state machine for related to the execution of a command. This register is blocked for writes after CMDEXEC is written to a 1 and prior to STATCMD.DONE being set by the hardware to indicate that command execution has completed.

Figure 13-6. CMDCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED		DATAVEREN	SSERASEDIS	ERASEMASKDIS	PROGMASKDIS	ECCGENOVR	ADDRXLATEOVR
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
POSTVEREN	PREVEREN	RESERVED	REGIONSEL				RESERVED
R/W-0h	R/W-0h	R-0h	R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
RESERVED			BANKSEL	MODESEL			
R/W-0h			R/W-0h	R/W-0h			

Table 13-21. CMDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21	DATAVEREN	R/W	0h	Enable invalid data verify. This checks for 0->1 transitions in the memory when a program operation is initiated. If such a transition is found, the program will fail with an error without executing the program. 0h (R/W) = Disable 1h (R/W) = Enable
20	SSERASEDIS	R/W	0h	Disable Stair-Step Erase. If set, the default VHV trim voltage setting will be used for all erase pulses. By default, this bit is reset, meaning that the VHV voltage will be stepped during successive erase pulses. The step count, step voltage, begin and end voltages are all hard-wired. 0h (R/W) = Enable 1h (R/W) = Disable
19	ERASEMASKDIS	R/W	0h	Disable use of erase mask for erase Bit masking will not be used during erase verify. If one or more sectors fail the verify either before (prever) or after (postver) the operation, then all specified flash sectors will receive subsequent erase pulse. 0h (R/W) = Enable 1h (R/W) = Disable
18	PROGMASKDIS	R/W	0h	Disable use of program mask for programming. Bit masking will not be used during program verify. If one or more bits fail the verify either before (prever) or after (postver) the operation, then all specified flash entries will receive subsequent program pulse. 0h (R/W) = Enable 1h (R/W) = Disable

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Table 13-21. CMDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	ECCGENOVR	R/W	0h	Override hardware generation of ECC data for program. Use data written to CMDDATAECC*. 0h (R/W) = Do not override 1h (R/W) = Override
16	ADDRXLATEOVR	R/W	0h	Override hardware address translation of address in CMDADDR from a system address to a bank address and bank ID. Use data written to CMDADDR directly as the bank address. Use the value written to CMDCTL.BANKSEL directly as the bank ID. Use the value written to CMDCTL.REGIONSEL directly as the region ID. 0h (R/W) = Do not override 1h (R/W) = Override
15	POSTVEREN	R/W	1h	Enable verify after program or erase 0h (R/W) = Disable 1h (R/W) = Enable
14	PREVEREN	R/W	1h	Enable verify before program or erase. For program, bits already programmed to the requested value will be masked. For erase, sectors already erased will be masked. 0h (R/W) = Disable 1h (R/W) = Enable
13	RESERVED	R	0h	Reserved
12-9	REGIONSEL	R/W	0h	Bank Region A specific region ID can be written to this field to indicate to which region an operation is to be applied if CMDCTL.ADDRXLATEOVR is set. 1h (R/W) = Main Region 2h (R/W) = Non-Main Region 4h (R/W) = Trim Region 8h (R/W) = Engr Region
8-5	RESERVED	R/W	0h	
4	BANKSEL	R/W	0h	Bank Select A specific Bank ID can be written to this field to indicate to which bank an operation is to be applied if CMDCTL.ADDRXLATEOVR is set. 1h (R/W) = Bank 0 2h (R/W) = Bank 1 4h (R/W) = Bank 2 8h (R/W) = Bank 3 10h (R/W) = Bank 4
3-0	MODESEL	R/W	0h	Mode This field is only used for the Mode Change command type. Otherwise, bank and pump modes are set automaticlly through the NW hardware. 0h = Read Mode 2h = Read Margin 0 Mode 4h = Read Margin 1 Mode 6h = Read Margin 0B Mode 7h = Read Margin 1B Mode 9h = Program Verify Mode Ah = Program Single Word Bh = Erase Verify Mode Ch = Erase Sector Eh = Program Multiple Word Fh = Erase Bank

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4 CMDADDR Register (Offset = 1120h) [Reset = 00000000h]

CMDADDR is shown in Figure 13-7 and described in Table 13-17.

Return to the Summary Table.

Command Address Register:
This register forms the target address of a command. The use cases are as follows:
1) For single-word program, this address indicates the flash bank word to be programmed.
2) For multi-word program, this address indicates the first flash bank address for the program. The address will be incremented for further words.
3) For sector erase, this address indicates the sector to be erased.
4) For bank erase, the address indicates the bank to be erased.
Note the address written to this register will be submitted for translation to the flash wrapper address translation interface, and the translated address will be used to access the bank. However, if the CMDCTL.ADDRXLATEOVR bit is set, then the address written to this register will be used directly as the bank address.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.

Figure 13-7. CMDADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-23. CMDADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Address value 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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5 CMDBYTEN Register (Offset = 1124h) [Reset = 00000000h]

CMDBYTEN is shown in Figure 13-8 and described in Table 13-18.

Return to the Summary Table.

Command Program Byte Enable Register:
This register forms a per-byte enable for programming data. For data bytes to be programmed, a 1 must be written to the corresponding bit in this register. Normally, all bits are written to 1, allowing program of full flash words. However, leaving some bits 0 allows programming of 8-bit, 16-bit, 32-bit or 64-bit portions of a flash word.
During verify, data bytes read from the flash will not be checked if the corresponding CMDBYTEN bit is 0.
ECC data bytes are protected by the 1-2 MSB bits in this register, depending on the presence of ECC and the flash word data width.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
This register is written to all 0 after the completion of all flash wrapper commands.

Figure 13-8. CMDBYTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														RESERVED										VAL							
R-0h														R/W-0h										R/W-0h							

Table 13-25. CMDBYTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-8	RESERVED	R/W	0h	
7-0	VAL	R/W	0h	Command Byte Enable value. A 1-bit per flash word byte value is placed in this register. 0h = Minimum value of [VAL] 0003FFFFh = Maximum value of [VAL]

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6 CMDDATAINDEX Register (Offset = 112Ch) [Reset = 00000000h]

CMDDATAINDEX is shown in Figure 13-9 and described in Table 13-19.

Return to the Summary Table.

Command Program Data Index Register:
When multiple data registers are available for multi-word program, this register can be written with an index which points to one of the data registers. When a write to CMDDATA* is done, the data will be written to the physical data register indexed by the value in this register.
Up to 8 data registers can be present, so this register can be written with 0x0 to 0x7. If less than 8 data registers are present, successive MSB bits of this register are ignored when indexing the CMDDATA* registers.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.

Figure 13-9. CMDDATAINDEX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													VAL		
R-0h																													R/W-0h		

Table 13-27. CMDDATAINDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	VAL	R/W	0h	Data register index 0h = Minimum value of [VAL] 7h = Maximum value of [VAL]

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7 CMDDATA0 Register (Offset = 1130h) [Reset = 00000000h]

CMDDATA0 is shown in Figure 13-10 and described in Table 13-20.

Return to the Summary Table.

Command Data Register 0
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 31:0 of flash word data register 0.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 0.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-10. CMDDATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-29. CMDDATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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8 CMDDATA1 Register (Offset = 1134h) [Reset = 00000000h]

CMDDATA1 is shown in Figure 13-11 and described in Table 13-21.

Return to the Summary Table.

Command Data Register 1
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 63:32 of flash word data register 0.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 0.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to CMDSTAT.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-11. CMDDATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-31. CMDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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9 CMDDATA2 Register (Offset = 1138h) [Reset = 00000000h]

CMDDATA2 is shown in Figure 13-12 and described in Table 13-22.

Return to the Summary Table.

Command Data Register 2
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 95:64 of flash word data register 0.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 1.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-12. CMDDATA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-33. CMDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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10 CMDDATA3 Register (Offset = 113Ch) [Reset = 00000000h]

CMDDATA3 is shown in Figure 13-13 and described in Table 13-23.

Return to the Summary Table.

Command Data Register 3
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 127:96 of flash word data register 0.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 1.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-13. CMDDATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-35. CMDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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11 CMDDATA4 Register (Offset = 1140h) [Reset = 00000000h]

CMDDATA4 is shown in Figure 13-14 and described in Table 13-24.

Return to the Summary Table.

Command Data Register 4
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 31:0 of flash word data register 1.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 2.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-14. CMDDATA4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-37. CMDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. T 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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12 CMDDATA5 Register (Offset = 1144h) [Reset = 00000000h]

CMDDATA5 is shown in Figure 13-15 and described in Table 13-25.

Return to the Summary Table.

Command Data Register 5
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 63:32 of flash word data register 1.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 2.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-15. CMDDATA5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-39. CMDDATA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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13 CMDDATA6 Register (Offset = 1148h) [Reset = 00000000h]

CMDDATA6 is shown in Figure 13-16 and described in Table 13-26.

Return to the Summary Table.

Command Data Register 6
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 95:64 of flash word data register 1.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 3.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-16. CMDDATA6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-41. CMDDATA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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14 CMDDATA7 Register (Offset = 114Ch) [Reset = 00000000h]

CMDDATA7 is shown in Figure 13-17 and described in Table 13-27.

Return to the Summary Table.

Command Data Register 7
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 127:96 of flash word data register 1.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 3.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-17. CMDDATA7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-43. CMDDATA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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15 CMDDATA8 Register (Offset = 1150h) [Reset = 00000000h]

CMDDATA8 is shown in Figure 13-18 and described in Table 13-28.

Return to the Summary Table.

Command Data Register 8
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 31:0 of flash word data register 2.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 4.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-18. CMDDATA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-45. CMDDATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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16 CMDDATA9 Register (Offset = 1154h) [Reset = 00000000h]

CMDDATA9 is shown in Figure 13-19 and described in Table 13-29.

Return to the Summary Table.

Command Data Register 9
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 63:32 of flash word data register 2.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 4.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-19. CMDDATA9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-47. CMDDATA9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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17 CMDDATA10 Register (Offset = 1158h) [Reset = 00000000h]

CMDDATA10 is shown in Figure 13-20 and described in Table 13-30.

Return to the Summary Table.

Command Data Register 10
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 95:64 of flash word data register 2.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 5.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-20. CMDDATA10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-49. CMDDATA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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18 CMDDATA11 Register (Offset = 115Ch) [Reset = 00000000h]

CMDDATA11 is shown in Figure 13-21 and described in Table 13-31.

Return to the Summary Table.

Command Data Register 11
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 127:96 of flash word data register 2.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 5.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-21. CMDDATA11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-51. CMDDATA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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19 CMDDATA12 Register (Offset = 1160h) [Reset = 00000000h]

CMDDATA12 is shown in Figure 13-22 and described in Table 13-32.

Return to the Summary Table.

Command Data Register 12
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 31:0 of flash word data register 3.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 6.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-22. CMDDATA12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-53. CMDDATA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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20 CMDDATA13 Register (Offset = 1164h) [Reset = 00000000h]

CMDDATA13 is shown in Figure 13-23 and described in Table 13-33.

Return to the Summary Table.

Command Data Register 13
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 63:32 of flash word data register 3.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 6.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-23. CMDDATA13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-55. CMDDATA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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21 CMDDATA14 Register (Offset = 1168h) [Reset = 00000000h]

CMDDATA14 is shown in Figure 13-24 and described in Table 13-34.

Return to the Summary Table.

Command Data Register 14
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 95:64 of flash word data register 3.
For DATAWIDTH == 64: This register represents bits 31:0 of flash word data register 7.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-24. CMDDATA14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-57. CMDDATA14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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22 CMDDATA15 Register (Offset = 116Ch) [Reset = 00000000h]

CMDDATA15 is shown in Figure 13-25 and described in Table 13-35.

Return to the Summary Table.

Command Data Register 15
This register forms the data for a command.
For DATAWIDTH == 128: This register represents bits 127:96 of flash word data register 3.
For DATAWIDTH == 64: This register represents bits 63:32 of flash word data register 7.
This register is blocked for writes after a 1 is written to the CMDEXEC
register and prior to STATCMD.DONE being set by the flash wrapper
hardware.
This register is used to aggregate masking for bits that do not
require additional program pulses during program operations, and will be
written to all 1 after the completion of all flash wrapper commands.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.

Figure 13-25. CMDDATA15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-59. CMDDATA15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	A 32-bit data value is placed in this field. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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23 CMDDATAECC0 Register (Offset = 11B0h) [Reset = 00000000h]

CMDDATAECC0 is shown in Figure 13-26 and described in Table 13-36.

Return to the Summary Table.

Command Data Register 0
This register forms the ECC portion of the data for a command. This ECC data in this register covers flash data register 0.
The hardware ECC generation in flash wrapper can be overridden and ECC data developed elsewhere can be used. ECC data is placed in this register.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.
This register is used to aggregate masking for bits that do not require additional program pulses during program operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-26. CMDDATAECC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL1								VAL0							
R-0h																R/W-0h								R/W-0h							

Table 13-61. CMDDATAECC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	VAL1	R/W	FFh	ECC data for bits 127:64 of the data is placed here. 0h = Minimum value FFh = Maximum value
7-0	VAL0	R/W	FFh	ECC data for bits 63:0 of the data is placed here. 0h = Minimum value FFh = Maximum value

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24 CMDDATAECC1 Register (Offset = 11B4h) [Reset = 00000000h]

CMDDATAECC1 is shown in Figure 13-27 and described in Table 13-37.

Return to the Summary Table.

Command Data Register 1
This register forms the ECC portion of the data for a command. This ECC data in this register covers flash data register 0.
The hardware ECC generation in flash wrapper can be overridden and ECC data developed elsewhere can be used. ECC data is placed in this register.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.
This register is used to aggregate masking for bits that do not require additional program pulses during program operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-27. CMDDATAECC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL1								VAL0							
R-0h																R/W-0h								R/W-0h							

Table 13-63. CMDDATAECC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	VAL1	R/W	FFh	ECC data for bits 127:64 of the data is placed here. 0h = Minimum value FFh = Maximum value
7-0	VAL0	R/W	FFh	ECC data for bits 63:0 of the data is placed here. 0h = Minimum value FFh = Maximum value

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25 CMDDATAECC2 Register (Offset = 11B8h) [Reset = 00000000h]

CMDDATAECC2 is shown in Figure 13-28 and described in Table 13-38.

Return to the Summary Table.

Command Data Register 2
This register forms the ECC portion of the data for a command. This ECC data in this register covers flash data register 2.
The hardware ECC generation in flash wrapper can be overridden and ECC data developed elsewhere can be used. ECC data is placed in this register.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.
This register is used to aggregate masking for bits that do not require additional program pulses during program operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-28. CMDDATAECC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL1								VAL0							
R-0h																R/W-0h								R/W-0h							

Table 13-65. CMDDATAECC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	VAL1	R/W	FFh	ECC data for bits 127:64 of the data is placed here. 0h = Minimum value FFh = Maximum value
7-0	VAL0	R/W	FFh	ECC data for bits 63:0 of the data is placed here. 0h = Minimum value FFh = Maximum value

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26 CMDDATAECC3 Register (Offset = 11BCh) [Reset = 00000000h]

CMDDATAECC3 is shown in Figure 13-29 and described in Table 13-39.

Return to the Summary Table.

Command Data Register 3
This register forms the ECC portion of the data for a command. This ECC data in this register covers flash data register 3.
The hardware ECC generation in flash wrapper can be overridden and ECC data developed elsewhere can be used. ECC data is placed in this register.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
Use cases for the CMDDATA* registers are as follows:
1) Program - These registers contain the data to be programmed.
2) Erase - These registers are not used.
This register is used to aggregate masking for bits that do not require additional program pulses during program operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-29. CMDDATAECC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL1								VAL0							
R-0h																R/W-0h								R/W-0h							

Table 13-67. CMDDATAECC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	VAL1	R/W	FFh	ECC data for bits 127:64 of the data is placed here. 0h = Minimum value FFh = Maximum value
7-0	VAL0	R/W	FFh	ECC data for bits 63:0 of the data is placed here. 0h = Minimum value FFh = Maximum value

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27 CMDWEPROTA Register (Offset = 11D0h) [Reset = 00000000h]

CMDWEPROTA is shown in Figure 13-30 and described in Table 13-40.

Return to the Summary Table.

Command WriteErase Protect A Register
This register allows the first 32 sectors of the main region to be protected from program or erase, with 1 bit protecting each sector. If the main region size is smaller than 32 sectors, then this register provides protection for the whole region.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
In addition, this register is used to aggregate masking for sectors that do not require additional erase pulses during bank erase operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-30. CMDWEPROTA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-69. CMDWEPROTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Each bit protects 1 sector. bit [0]: When 1, sector 0 of the flash memory will be protected from program and erase. bit [1]: When 1, sector 1 of the flash memory will be protected from program and erase. : : bit [31]: When 1, sector 31 of the flash memory will be protected from program and erase. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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28 CMDWEPROTB Register (Offset = 11D4h) [Reset = 00000000h]

CMDWEPROTB is shown in Figure 13-31 and described in Table 13-41.

Return to the Summary Table.

Command WriteErase Protect B Register
This register allows main region sectors to be protected from program and erase. Each bit corresponds to a group of 8 sectors.
There are multiple cases for how these protect bits are applied:
1. Single-bank system, CMDWEPROTA register present:
The first 32 sectors are protected via the CMDWEPROTA register. Thus, the protection given by the bits in CMDWEPROTB begin with sector 32.
2. Single-bank system, CMDWEPROTA register not present:
The protection given by the bits in CMDWEPROTB begin with sector 0.
3. Multi-bank system, CMDWEPROTA register present - Bank 0:
The first 32 sectors of bank 0 are protected via the CMDWEPROTA register. Thus, only bits 4 and above of CMDWEPROTB would be applicable to bank 0. The protection of bit 4 and above would begin at sector 32. Bits 3:0 of WEPROTB are ignored for bank 0.
4. Multi-bank system, CMDWEPROTA register present, Banks 1-N:
For banks other than bank 0 in a multi-bank system, CMDWEPROTA has no effect, so the bits in CMDWEPROTB will protect these banks starting from sector 0.
5. Multi-bank system, CMDWEPROTA register not present:
The bits in CMDWEPROTB will protect any of the banks starting from sector 0.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
In addition, this register is used to aggregate masking for sectors that do not require additional erase pulses during bank erase operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-31. CMDWEPROTB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-71. CMDWEPROTB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Each bit protects a group of 8 sectors. When a bit is 1, the associated 8 sectors in the flash will be protected from program and erase. A maximum of 256 sectors can be protected with this register. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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29 CMDWEPROTNM Register (Offset = 1210h) [Reset = 00000000h]

CMDWEPROTNM is shown in Figure 13-32 and described in Table 13-42.

Return to the Summary Table.

Command WriteErase Protect Non-Main
Register
This register allows non-main region region sectors to be protected from program and erase. Each bit corresponds to 1 sector.
This register is blocked for writes after a 1 is written to the CMDEXEC register and prior to STATCMD.DONE being set by the flash wrapper hardware.
In addition, this register is used to aggregate masking for sectors that do not require additional erase pulses during bank erase operations, and will be written to all 1 after the completion of all flash wrapper commands.

Figure 13-32. CMDWEPROTNM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

Table 13-73. CMDWEPROTNM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	FFFFFFFFh	Each bit protects 1 sector. bit [0]: When 1, sector 0 of the non-main region will be protected from program and erase. bit [1]: When 1, sector 1 of the non-main region will be protected from program and erase. : : bit [31]: When 1, sector 31 of the non-main will be protected from program and erase. 0h = Minimum value of [VAL] FFFFFFFFh = Maximum value of [VAL]

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30 STATCMD Register (Offset = 13D0h) [Reset = 00000000h]

STATCMD is shown in Figure 13-33 and described in Table 13-43.

Return to the Summary Table.

Command Status Register This register contains status regarding completion and errors of command execution.

Figure 13-33. STATCMD Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			FAILMISC	RESERVED			FAILINVDATA
R-0h			R-0h	R-0h			R-0h
7	6	5	4	3	2	1	0
FAILMODE	FAILILLADDR	FAILVERIFY	FAILWEPROT	RESERVED	CMDINPROGRESS	CMDPASS	CMDDONE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 13-75. STATCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	FAILMISC	R	0h	Command failed due to error other than write/erase protect violation or verify error. This is an extra bit in case a new failure mechanism is added which requires a status bit. 0h = No Fail 1h = Fail
11-9	RESERVED	R	0h	Reserved
8	FAILINVDATA	R	0h	Program command failed because an attempt was made to program a stored 0 value to a 1. 0h = No Fail 1h = Fail
7	FAILMODE	R	0h	Command failed because a bank has been set to a mode other than READ. Program and Erase commands cannot be initiated unless all banks are in READ mode. 0h = No Fail 1h = Fail
6	FAILILLADDR	R	0h	Command failed due to the use of an illegal address 0h = No Fail 1h = Fail
5	FAILVERIFY	R	0h	Command failed due to verify error 0h = No Fail 1h = Fail
4	FAILWEPROT	R	0h	Command failed due to Write/Erase Protect Sector Violation 0h = No Fail 1h = Fail
3	RESERVED	R	0h	Reserved
2	CMDINPROGRESS	R	0h	Command In Progress 0h = Complete 1h = In Progress

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Table 13-75. STATCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CMDPASS	R	0h	Command Pass - valid when CMD_DONE field is 1 0h = Fail 1h = Pass
0	CMDDONE	R	0h	Command Done 0h = Not Done 1h = Done

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31 STATPCNT Register (Offset = 13D8h) [Reset = 00000000h]

STATPCNT is shown in Figure 13-34 and described in Table 13-44.

Return to the Summary Table.

Current Pulse Count Register: Read only register giving read access to the state machine current pulse count value for program/erase operations.

Figure 13-34. STATPCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				PULSECNT											
R-0h																				R-0h											

Table 13-77. STATPCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-0	PULSECNT	R	0h	Current Pulse Counter Value 0h = Minimum value FFFh = Maximum value

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Chapter 14

General-Purpose Input/Output (GPIO)

The GPIO peripheral provides the user with a means to write data out and read data in to and from the device pins. The GPIO also provides a way to detect wakeup events while the device is in a low power state. This chapter describes the operation of the GPIO peripheral.

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14.2 GPIO Operation 582
14.3 GPIO Interrupts & Triggers 585
14.4 GPIO Registers 587

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14.1 GPIO Overview

The GPIO is used to read in digital data from the device pins and to send digital data out to the device pins.

The GPIO module features include:

- Single CLK cycle access to registers (zero wait state MMR access from CPU)
- Set/clear/toggle multiple bits without the need of a read-modify-write construct in software
- Direct writes to individual GPIO output bits (DOUT) without the need of a read-modify-write construct in software
- Direct read comparisons of individual GPIO input bits (DIN) without the need to use masking in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes based on input edge detection
- User controlled input filtering (configurable per IO)

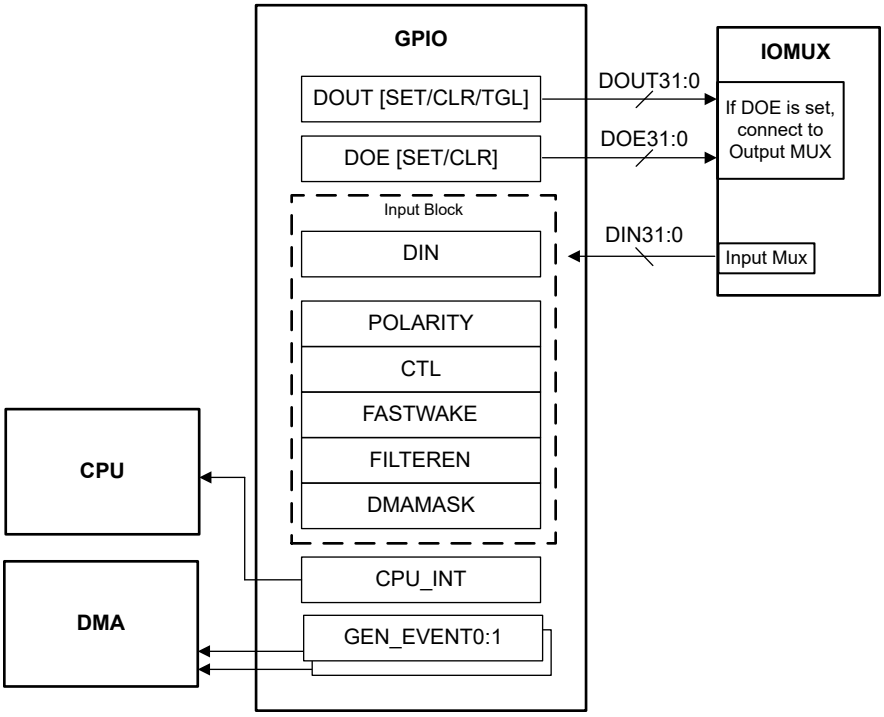


Figure 14-1. GPIO Block Diagram

Note

The GPIO module for the AM13E232x platform does not manage the complete digital IO functionality (for example, pullup, pulldown, or other functional muxing). For complete digital IO control details, refer to IOMUX chapter. Similar to any other peripheral, the GPIO has inputs and outputs (with output enable) that interface with the IOMUX to make connections to the physical device pins.

14.2 GPIO Operation

The GPIO peripheral is configured with user software. The GPIO peripheral mainly controls output functionality, but is able to read and filter input signals as long as the digital input on a pin is enabled by the IOMUX. The value of an input or an output on a specified pin is stored within the DIOx bits of the Data Output registers (DOUT31_0) and Data Input registers (DIN31_0) for a given GPIO instance.

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GPIO Outputs

To output a signal on a pin, the output enable bit (DIOx) within the output enable register (DOE31_0) must be set for the specified pin. The output enable bits can be set and cleared directly within the DOE31_0 register, but can also be set and cleared by writing to the data output enable set (DOESET31_0) and data output enable clear (DOECLR 31_0) registers.

Once an output is enabled, the output value can be updated within the DOUT31_0 register. For full explanation of output value manipulation, please see GPIO Read/Write Interface.

GPIO Inputs

To read an input value on a specified pin, the IOMUX must enable the digital input on the pin, allowing the signal to propagate internally to the device. From there, the GPIO can read the value of a specified pin by reading the respective bit within the DIN31_0 register.

As long as the GPIO peripheral is enabled, the GPIO peripheral can read the input of an associated pin as long as the input is enabled by the IOMUX. This means that as long as a pin is enabled for digital input by the IOMUX, regardless of what the peripheral function of the pin is, the GPIO peripheral can read the state of the pin.

In addition to reading the input value of a signal, the GPIO can also filter the input signal to detect pulses greater than a specified amount of ULPCLK cycles. See GPIO Input Glitch Filtering and Synchronization for more details. The GPIO peripheral can also generate interrupts to the CPU and the DMA based on input edge detection by configuring the polarity registers.

Table 14-1. GPIO Interrupts & DMA Triggers Available

GPIO Instance	Interrupt Lines	DMA Trigger Lines
GPIO[0:2]	1x	2x
GPIO3	1x	1x

14.2.1 GPIO Ports

Each instance of the GPIO peripheral supports up to 32 data input/output (DIO) bits. For devices with greater than 32 GPIOs, multiple instances of the GPIO peripheral are used to address all of the device pins. Each GPIO instance is associated with a port name to differentiate pins by name. Please see the *Pin Configuration and Functions* section of the device data sheet to determine which GPIO signal is associated with which pin.

Table 14-2. GPIO Instances

GPIO Instance	GPIO Port Name
GPIO0	PA
GPIO1	PB
GPIO2	PC
GPIO3	PD

14.2.2 GPIO Read/Write Interface

The GPIO peripheral has features and dedicated registers to allow for advanced bit manipulations without the need to execute a read-modify-write construct in software.

For both input and output data registers, there exists a set of alias registers to allow read/write byte access of a single GPIO pin instead of bit-wise access.

In addition, for output data, there are specific write to set (DOUTSET31_0), clear (DOUTCLR31_0), and toggle (DOUTTGL31_0) registers to set, clear, and toggle the outputs of a pin without the need to read-modify-write, preventing the known state of a GPIO pin from changing while updating the output value.

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14.2.3 GPIO Input Glitch Filtering and Synchronization

The GPIO module evaluates the state of input pins at the ULPCLK (PD0 bus clock) rate, synchronizing the pin state to ULPCLK through a 2-stage synchronizer before passing the GPIO state to the input glitch filter.

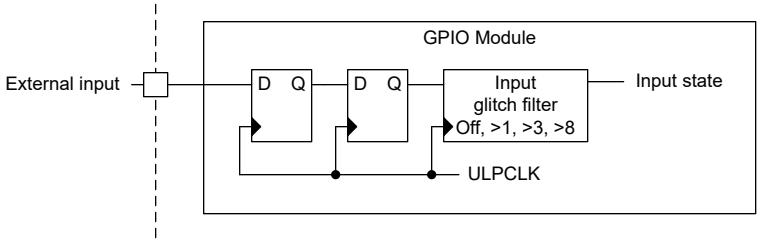


Figure 14-2. GPIO Input Synchronizer

A programmable input glitch filter is provided for suppressing noise on digital input pins. The glitch filter runs at ULPCLK rate. Four levels of user-specified input filtering are possible:

- Sampled input without filtering (the minimum reliably detected pulse width is one ULPCLK cycle due to synchronization)
- Synchronized inputs which are not greater than 1 ULPCLK periods are filtered out (glitch filter value of >1)
- Synchronized inputs which are not greater than 3 ULPCLK periods are filtered out (glitch filter value of >3)
- Synchronized inputs which are not greater than 8 ULPCLK periods are filtered out (glitch filter value of >8)

Note

Inputs are synchronized to ULPCLK, causing up to one ULPCLK cycle of uncertainty in the synchronization. Input signals that are shorter than one ULPCLK cycle can be missed.

Note

For pins with fast wake enable, there is an input delay time equal to the time between the edge of the un-synchronized input edge to the first MCLK edge in STANDBY0/1, STOP1/2 and SLEEP2 modes.

This feature allows users to easily implement input filtering in hardware for cases where fast switching on the input pin is needed to be filtered out. The bit fields in the FILTEREN31_16 and FILTEREN15_0 registers allow users to configure the level of filtering needed for the corresponding GPIO bit.

Input pulses of the same pulse length can be passed in some cases while being filtered in other cases due to the uncertainty in synchronization. GPIO Input Synchronizer and Glitch Filtering Scenarios demonstrates different scenarios and how synchronization affects input detection.

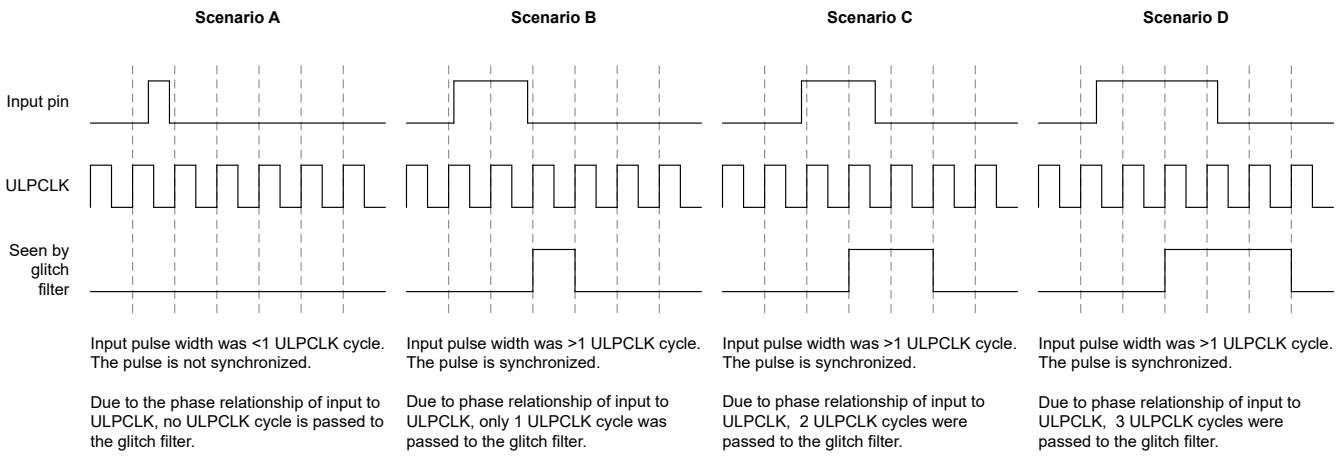


Figure 14-3. GPIO Input Synchronizer and Glitch Filtering Scenarios

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- In Scenario A, the input pulse is less than one ULPCLK cycle. Pulses less than one ULPCLK cycle may not be captured. To ensure that GPIO inputs are always captured, the GPIO input pulse width must be greater than the ULPCLK period.
- In Scenario B, the input pulse is nearly two ULPCLK cycles in length, but because the rising edge occurs just after the ULPCLK edge, the GPIO synchronizer only views the input pin as having been high for 1 ULPCLK period. This scenario would not be filtered out by the glitch filter when the glitch filter is disabled, but a glitch filter value of >1 would result in this pulse being filtered. Conversely, the same input pulse width in Scenario C results in the input pin being considered high for two ULPCLK periods, as the rising edge occurred just before the ULPCLK edge. In this case, this scenario would not be filtered out when a glitch filter value of >1 is specified.
- In Scenario D, three ULPCLK cycles are passed to the glitch filter. In this case, the scenario would not be filtered out when a glitch filter value of >1 is specified, but it would be filtered out for a glitch filter value of >3 or >8.

Note

When the fast wake mode is enabled (SYSOSC is requested asynchronously upon input pin activity), the ULPCLK will switch from off (as would be the case in STANDBY1) or 32kHz (as would be the case in STANDBY0) to 24Mhz/32MHz, resulting in the input synchronization logic and glitch filter running at 24Mhz/32MHz after some latency. See the device specific data sheet for the asynchronous fast clock request wake time, and budget this time into any minimum pulse width calculations when using fast wake.

14.2.4 GPIO Fast Wake

The fast wake feature in the GPIO peripheral allows the GPIO module to stay in a low-power state and detect interrupt events on the device pins without requiring a high-speed clock. This allows the device to support fast wakeup from low-power modes, such as STOP and STANDBY, on any GPIO pin.

Fast wake can be enabled on a bit-wise basis using the FASTWAKE register. Setting a bit in the FASTWAKE register enables the corresponding device pin signal to support fast wakeup functionality. The CTL register contains a bit field named FASTWAKEONLY which allows for global control of the fast wake feature. Setting the FASTWAKEONLY bit enables all of the bits in the corresponding GPIO port to support fast wakeup functionality.

Note

Do not enable fast wake in the GPIO while simultaneously blocking asynchronous fast clock requests in SYSCTL. When fast wake is enabled, the GPIO expects to handshake with SYSCTL for the fast clock. If SYSCTL ignores the request, the GPIO does not receive a clock until SYSCTL completes the asynchronous fast clock request handshake.

14.3 GPIO Interrupts & Triggers

14.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 14-3. CPU Interrupts Triggered by GPIO

NVIC Interrupt Name	Peripheral Instance Name	Register Group	GPIO Interrupt Configuration Registers	Description
GPIO0.CPU_INT	GPIO0	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO0 interrupt. Multiple OR'd, configurable source condition.
GPIO1.CPU_INT	GPIO1	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO1 interrupt. Multiple OR'd, configurable source condition.

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Table 14-3. CPU Interrupts Triggered by GPIO (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	GPIO Interrupt Configuration Registers	Description
GPIO2.CPU_INT	GPIO2	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO2 interrupt. Multiple OR'd, configurable source condition.
GPIO3.CPU_INT	GPIO3	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO3 interrupt. Multiple OR'd, configurable source condition.

14.3.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 14-4. DMA Triggers from the GPIO

Trigger Name	Peripheral Instance Name	Register Group	GPIO DMA Configuration Registers	Description
GPIO0.GEN_EVENT0	GPIO0	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO0 DMA trigger for bits 15 to 0. Multiple OR'd, configurable source conditions.
GPIO0.GEN_EVENT1	GPIO0	GEN_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO0 DMA trigger for bits 31 to 16. Multiple OR'd, configurable source conditions.
GPIO1.GEN_EVENT0	GPIO1	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO1 DMA trigger for bits 15 to 0. Multiple OR'd, configurable source conditions.
GPIO1.GEN_EVENT1	GPIO1	GEN_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO1 DMA trigger for bits 31 to 16. Multiple OR'd, configurable source conditions.
GPIO2.GEN_EVENT0	GPIO2	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO2 DMA trigger for bits 15 to 0. Multiple OR'd, configurable source conditions.
GPIO2.GEN_EVENT1	GPIO2	GEN_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO2 DMA trigger for bits 31 to 16. Multiple OR'd, configurable source conditions.

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Table 14-4. DMA Triggers from the GPIO (continued)

Trigger Name	Peripheral Instance Name	Register Group	GPIO DMA Configuration Registers	Description
GPIO3.GEN_EVENT0	GPIO3	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	GPIO3 DMA trigger for bits 15 to 0. Multiple OR'd, configurable source conditions.

14.4 GPIO Registers

This Section describes the GPIO Registers.

14.4.1 GPIO Base Address Table

Table 14-5. GPIO Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Gpio0Regs	GPIO_REGS	GPIO0	0x400F_0000
Gpio1Regs	GPIO_REGS	GPIO1	0x400F_2000
Gpio2Regs	GPIO_REGS	GPIO2	0x400F_4000
Gpio3Regs	GPIO_REGS	GPIO3	0x400F_6000

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14.4.2 GPIO_REGS Registers

Table 14-6 lists the memory-mapped registers for the GPIO_REGS registers. All register offset addresses not listed in Table 14-6 should be considered as reserved locations and the register contents should not be modified.

Table 14-6. GPIO_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1010h	CLKOVR	Clock Override		Go
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
1050h	IIDX	Interrupt index	GEN_EVENT0	Go
1058h	IMASK	Interrupt mask	GEN_EVENT0	Go
1060h	RIS	Raw interrupt status	GEN_EVENT0	Go
1068h	MIS	Masked interrupt status	GEN_EVENT0	Go
1070h	ISET	Interrupt set	GEN_EVENT0	Go
1078h	ICLR	Interrupt clear	GEN_EVENT0	Go
1080h	IIDX	Interrupt index	GEN_EVENT1	Go
1088h	IMASK	Interrupt mask	GEN_EVENT1	Go
1090h	RIS	Raw interrupt status	GEN_EVENT1	Go
1098h	MIS	Masked interrupt status	GEN_EVENT1	Go
10A0h	ISET	Interrupt set	GEN_EVENT1	Go
10A8h	ICLR	Interrupt clear	GEN_EVENT1	Go
10E0h	EVT_MODE	Event Mode		Go
10FCh	DESC	Module Description		Go
1200h	DOUT3_0	Data output 3 to 0		Go
1204h	DOUT7_4	Data output 7 to 4		Go
1208h	DOUT11_8	Data output 11 to 8		Go
120Ch	DOUT15_12	Data output 15 to 12		Go
1210h	DOUT19_16	Data output 19 to 16		Go
1214h	DOUT23_20	Data output 23 to 20		Go
1218h	DOUT27_24	Data output 27 to 24		Go
121Ch	DOUT31_28	Data output 31 to 28		Go
1280h	DOUT31_0	Data output 31 to 0		Go
1290h	DOUTSET31_0	Data output set 31 to 0		Go
12A0h	DOUTCLR31_0	Data output clear 31 to 0		Go
12B0h	DOUTTGL31_0	Data output toggle 31 to 0		Go
12C0h	DOE31_0	Data output enable 31 to 0		Go
12D0h	DOESET31_0	Data output enable set 31 to 0		Go
12E0h	DOECLR31_0	Data output enable clear 31 to 0		Go
1300h	DIN3_0	Data input 3 to 0		Go

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Table 14-6. GPIO_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1304h	DIN7_4	Data input 7 to 4		Go
1308h	DIN11_8	Data input 11 to 8		Go
130Ch	DIN15_12	Data input 15 to 12		Go
1310h	DIN19_16	Data input 19 to 16		Go
1314h	DIN23_20	Data input 23 to 20		Go
1318h	DIN27_24	Data input 27 to 24		Go
131Ch	DIN31_28	Data input 31 to 28		Go
1380h	DIN31_0	Data input 31 to 0		Go
1390h	POLARITY15_0	Polarity 15 to 0		Go
13A0h	POLARITY31_16	Polarity 31 to 16		Go
1400h	CTL	FAST WAKE GLOBAL EN		Go
1404h	FASTWAKE	FAST WAKE ENABLE		Go
1500h	SUB0CFG	Subscriber 0 configuration		Go
1508h	FILTEREN15_0	Filter Enable 15 to 0		Go
150Ch	FILTEREN31_16	Filter Enable 31 to 16		Go
1520h	SUB1CFG	Subscriber 1 configuration		Go

Complex bit access types are encoded to fit into small table cells. Table 14-7 shows the codes that are used for access types in this section.

Table 14-7. GPIO_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 14-4 and described in Table 14-8.

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Register to control the power state

Figure 14-4. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 14-9. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change Reset type: SYSRST 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power Reset type: SYSRST [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 14-5 and described in Table 14-9.

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Register to control reset assertion and de-assertion

Figure 14-5. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 14-11. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key Reset type: SYSRST B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register Reset type: SYSRST [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral Reset type: SYSRST [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 14-6 and described in Table 14-10.

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peripheral enable and reset status

Figure 14-6. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 14-13. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register Reset type: SYSRST 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 CLKOVR Register (Offset = 1010h) [Reset = 00000000h]

CLKOVR is shown in Figure 14-7 and described in Table 14-11.

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This register overrides the functional clock request by this peripheral to the system

Figure 14-7. CLKOVR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R/W-0h						R/W-0h	R/W-0h

Table 14-15. CLKOVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

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5 PDBGCTL Register (Offset = 1018h) [Reset = 00000001h]

PDBGCTL is shown in Figure 14-8 and described in Table 14-12.

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This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 14-8. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							FREE
R/W-0h							R/W-1h

Table 14-17. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	FREE	R/W	1h	Free run control Reset type: SYSRST 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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6 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 14-9 and described in Table 14-13.

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This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 14-9. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 14-19. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status Reset type: SYSRST 0h = No bit is set means there is no pending interrupt request 1h = DIO0 interrupt 2h = DIO1 interrupt 3h = DIO2 interrupt 4h = DIO3 interrupt 5h = DIO4 interrupt 6h = DIO5 interrupt 7h = DIO6 interrupt 8h = DIO7 interrupt 9h = DIO8 interrupt Ah = DIO9 interrupt Bh = DIO10 interrupt Ch = DIO11 interrupt Dh = DIO12 interrupt Eh = DIO13 interrupt Fh = DIO14 interrupt 10h = DIO15 interrupt 11h = DIO16 interrupt 12h = DIO17 interrupt 13h = DIO18 interrupt 14h = DIO19 interrupt 15h = DIO20 interrupt 16h = DIO21 interrupt 17h = DIO22 interrupt 18h = DIO23 interrupt 19h = DIO24 interrupt 1Ah = DIO25 interrupt 1Bh = DIO26 interrupt 1Ch = DIO27 interrupt 1Dh = DIO28 interrupt 1Eh = DIO29 interrupt 1Fh = DIO30 interrupt 20h = DIO31 interrupt

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7 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 14-10 and described in Table 14-14.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 14-10. IMASK Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 14-21. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R/W	0h	DIO31 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
30	DIO30	R/W	0h	DIO30 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
29	DIO29	R/W	0h	DIO29 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
28	DIO28	R/W	0h	DIO28 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
27	DIO27	R/W	0h	DIO27 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
26	DIO26	R/W	0h	DIO26 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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Table 14-21. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R/W	0h	DIO25 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
24	DIO24	R/W	0h	DIO24 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
23	DIO23	R/W	0h	DIO23 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
22	DIO22	R/W	0h	DIO22 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
21	DIO21	R/W	0h	DIO21 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
20	DIO20	R/W	0h	DIO20 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
19	DIO19	R/W	0h	DIO19 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
18	DIO18	R/W	0h	DIO18 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
17	DIO17	R/W	0h	DIO17 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
16	DIO16	R/W	0h	DIO16 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
15	DIO15	R/W	0h	DIO15 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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Table 14-21. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R/W	0h	DIO14 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
13	DIO13	R/W	0h	DIO13 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
12	DIO12	R/W	0h	DIO12 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
11	DIO11	R/W	0h	DIO11 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
10	DIO10	R/W	0h	DIO10 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
9	DIO9	R/W	0h	DIO9 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
8	DIO8	R/W	0h	DIO8 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
7	DIO7	R/W	0h	DIO7 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
6	DIO6	R/W	0h	DIO6 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
5	DIO5	R/W	0h	DIO5 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
4	DIO4	R/W	0h	DIO4 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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Table 14-21. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	R/W	0h	DIO3 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
2	DIO2	R/W	0h	DIO2 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
1	DIO1	R/W	0h	DIO1 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
0	DIO0	R/W	0h	DIO0 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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8 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 14-11 and described in Table 14-15.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 14-11. RIS Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14-23. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R	0h	DIO31 event Reset type: SYSRST 0h = DIO31 event did not occur 1h = DIO31 event occurred
30	DIO30	R	0h	DIO30 event Reset type: SYSRST 0h = DIO30 event did not occur 1h = DIO30 event occurred
29	DIO29	R	0h	DIO29 event Reset type: SYSRST 0h = DIO29 event did not occur 1h = DIO29 event occurred
28	DIO28	R	0h	DIO28 event Reset type: SYSRST 0h = DIO28 event did not occur 1h = DIO28 event occurred
27	DIO27	R	0h	DIO27 event Reset type: SYSRST 0h = DIO27 event did not occur 1h = DIO27 event occurred
26	DIO26	R	0h	DIO26 event Reset type: SYSRST 0h = DIO26 event did not occur 1h = DIO26 event occurred

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Table 14-23. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R	0h	DIO25 event Reset type: SYSRST 0h = DIO25 event did not occur 1h = DIO25 event occurred
24	DIO24	R	0h	DIO24 event Reset type: SYSRST 0h = DIO24 event did not occur 1h = DIO24 event occurred
23	DIO23	R	0h	DIO23 event Reset type: SYSRST 0h = DIO23 event did not occur 1h = DIO23 event occurred
22	DIO22	R	0h	DIO22 event Reset type: SYSRST 0h = DIO22 event did not occur 1h = DIO22 event occurred
21	DIO21	R	0h	DIO21 event Reset type: SYSRST 0h = DIO21 event did not occur 1h = DIO21 event occurred
20	DIO20	R	0h	DIO20 event Reset type: SYSRST 0h = DIO20 event did not occur 1h = DIO20 event occurred
19	DIO19	R	0h	DIO19 event Reset type: SYSRST 0h = DIO19 event did not occur 1h = DIO19 event occurred
18	DIO18	R	0h	DIO18 event Reset type: SYSRST 0h = DIO18 event did not occur 1h = DIO18 event occurred
17	DIO17	R	0h	DIO17 event Reset type: SYSRST 0h = DIO17 event did not occur 1h = DIO17 event occurred
16	DIO16	R	0h	DIO16 event Reset type: SYSRST 0h = DIO16 event did not occur 1h = DIO16 event occurred
15	DIO15	R	0h	DIO15 event Reset type: SYSRST 0h = DIO15 event did not occur 1h = DIO15 event occurred

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Table 14-23. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	DIO14 event Reset type: SYSRST 0h = DIO14 event did not occur 1h = DIO14 event occurred
13	DIO13	R	0h	DIO13 event Reset type: SYSRST 0h = DIO13 event did not occur 1h = DIO13 event occurred
12	DIO12	R	0h	DIO12 event Reset type: SYSRST 0h = DIO12 event did not occur 1h = DIO12 event occurred
11	DIO11	R	0h	DIO11 event Reset type: SYSRST 0h = DIO11 event did not occur 1h = DIO11 event occurred
10	DIO10	R	0h	DIO10 event Reset type: SYSRST 0h = DIO10 event did not occur 1h = DIO10 event occurred
9	DIO9	R	0h	DIO9 event Reset type: SYSRST 0h = DIO9 event did not occur 1h = DIO9 event occurred
8	DIO8	R	0h	DIO8 event Reset type: SYSRST 0h = DIO8 event did not occur 1h = DIO8 event occurred
7	DIO7	R	0h	DIO7 event Reset type: SYSRST 0h = DIO7 event did not occur 1h = DIO7 event occurred
6	DIO6	R	0h	DIO6 event Reset type: SYSRST 0h = DIO6 event did not occur 1h = DIO6 event occurred
5	DIO5	R	0h	DIO5 event Reset type: SYSRST 0h = DIO5 event did not occur 1h = DIO5 event occurred
4	DIO4	R	0h	DIO4 event Reset type: SYSRST 0h = DIO4 event did not occur 1h = DIO4 event occurred

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Table 14-23. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	R	0h	DIO3 event Reset type: SYSRST 0h = DIO3 event did not occur 1h = DIO3 event occurred
2	DIO2	R	0h	DIO2 event Reset type: SYSRST 0h = DIO2 event did not occur 1h = DIO2 event occurred
1	DIO1	R	0h	DIO1 event Reset type: SYSRST 0h = DIO1 event did not occur 1h = DIO1 event occurred
0	DIO0	R	0h	DIO0 event Reset type: SYSRST 0h = DIO0 event did not occur 1h = DIO0 event occurred

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9 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 14-12 and described in Table 14-16.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 14-12. MIS Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14-25. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R	0h	DIO31 event Reset type: SYSRST 0h = DIO31 event did not occur 1h = DIO31 event occurred
30	DIO30	R	0h	DIO30 event Reset type: SYSRST 0h = DIO30 event did not occur 1h = DIO30 event occurred
29	DIO29	R	0h	DIO29 event Reset type: SYSRST 0h = DIO29 event did not occur 1h = DIO29 event occurred
28	DIO28	R	0h	DIO28 event Reset type: SYSRST 0h = DIO28 event did not occur 1h = DIO28 event occurred
27	DIO27	R	0h	DIO27 event Reset type: SYSRST 0h = DIO27 event did not occur 1h = DIO27 event occurred
26	DIO26	R	0h	DIO26 event Reset type: SYSRST 0h = DIO26 event did not occur 1h = DIO26 event occurred

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Table 14-25. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R	0h	DIO25 event Reset type: SYSRST 0h = DIO25 event did not occur 1h = DIO25 event occurred
24	DIO24	R	0h	DIO24 event Reset type: SYSRST 0h = DIO24 event did not occur 1h = DIO24 event occurred
23	DIO23	R	0h	DIO23 event Reset type: SYSRST 0h = DIO23 event did not occur 1h = DIO23 event occurred
22	DIO22	R	0h	DIO22 event Reset type: SYSRST 0h = DIO22 event did not occur 1h = DIO22 event occurred
21	DIO21	R	0h	DIO21 event Reset type: SYSRST 0h = DIO21 event did not occur 1h = DIO21 event occurred
20	DIO20	R	0h	DIO20 event Reset type: SYSRST 0h = DIO20 event did not occur 1h = DIO20 event occurred
19	DIO19	R	0h	DIO19 event Reset type: SYSRST 0h = DIO19 event did not occur 1h = DIO19 event occurred
18	DIO18	R	0h	DIO18 event Reset type: SYSRST 0h = DIO18 event did not occur 1h = DIO18 event occurred
17	DIO17	R	0h	DIO17 event Reset type: SYSRST 0h = DIO17 event did not occur 1h = DIO17 event occurred
16	DIO16	R	0h	DIO16 event Reset type: SYSRST 0h = DIO16 event did not occur 1h = DIO16 event occurred
15	DIO15	R	0h	DIO15 event Reset type: SYSRST 0h = DIO15 event did not occur 1h = DIO15 event occurred

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Table 14-25. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	DIO14 event Reset type: SYSRST 0h = DIO14 event did not occur 1h = DIO14 event occurred
13	DIO13	R	0h	DIO13 event Reset type: SYSRST 0h = DIO13 event did not occur 1h = DIO13 event occurred
12	DIO12	R	0h	DIO12 event Reset type: SYSRST 0h = DIO12 event did not occur 1h = DIO12 event occurred
11	DIO11	R	0h	DIO11 event Reset type: SYSRST 0h = DIO11 event did not occur 1h = DIO11 event occurred
10	DIO10	R	0h	DIO10 event Reset type: SYSRST 0h = DIO10 event did not occur 1h = DIO10 event occurred
9	DIO9	R	0h	DIO9 event Reset type: SYSRST 0h = DIO9 event did not occur 1h = DIO9 event occurred
8	DIO8	R	0h	DIO8 event Reset type: SYSRST 0h = DIO8 event did not occur 1h = DIO8 event occurred
7	DIO7	R	0h	DIO7 event Reset type: SYSRST 0h = DIO7 event did not occur 1h = DIO7 event occurred
6	DIO6	R	0h	DIO6 event Reset type: SYSRST 0h = DIO6 event did not occur 1h = DIO6 event occurred
5	DIO5	R	0h	DIO5 event Reset type: SYSRST 0h = DIO5 event did not occur 1h = DIO5 event occurred
4	DIO4	R	0h	DIO4 event Reset type: SYSRST 0h = DIO4 event did not occur 1h = DIO4 event occurred

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Table 14-25. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	R	0h	DIO3 event Reset type: SYSRST 0h = DIO3 event did not occur 1h = DIO3 event occurred
2	DIO2	R	0h	DIO2 event Reset type: SYSRST 0h = DIO2 event did not occur 1h = DIO2 event occurred
1	DIO1	R	0h	DIO1 event Reset type: SYSRST 0h = DIO1 event did not occur 1h = DIO1 event occurred
0	DIO0	R	0h	DIO0 event Reset type: SYSRST 0h = DIO0 event did not occur 1h = DIO0 event occurred

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10 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 14-13 and described in Table 14-17.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 14-13. ISET Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-27. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	DIO31 event Reset type: SYSRST 0h = No effect 1h = Sets DIO31 in RIS register
30	DIO30	W	0h	DIO30 event Reset type: SYSRST 0h = No effect 1h = Sets DIO30 in RIS register
29	DIO29	W	0h	DIO29 event Reset type: SYSRST 0h = No effect 1h = Sets DIO29 in RIS register
28	DIO28	W	0h	DIO28 event Reset type: SYSRST 0h = No effect 1h = Sets DIO28 in RIS register
27	DIO27	W	0h	DIO27 event Reset type: SYSRST 0h = No effect 1h = Sets DIO27 in RIS register
26	DIO26	W	0h	DIO26 event Reset type: SYSRST 0h = No effect 1h = Sets DIO26 in RIS register

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Table 14-27. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	W	0h	DIO25 event Reset type: SYSRST 0h = No effect 1h = Sets DIO25 in RIS register
24	DIO24	W	0h	DIO24 event Reset type: SYSRST 0h = No effect 1h = Sets DIO24 in RIS register
23	DIO23	W	0h	DIO23 event Reset type: SYSRST 0h = No effect 1h = Sets DIO23 in RIS register
22	DIO22	W	0h	DIO22 event Reset type: SYSRST 0h = No effect 1h = Sets DIO22 in RIS register
21	DIO21	W	0h	DIO21 event Reset type: SYSRST 0h = No effect 1h = Sets DIO21 in RIS register
20	DIO20	W	0h	DIO20 event Reset type: SYSRST 0h = No effect 1h = Sets DIO20 in RIS register
19	DIO19	W	0h	DIO19 event Reset type: SYSRST 0h = No effect 1h = Sets DIO19 in RIS register
18	DIO18	W	0h	DIO18 event Reset type: SYSRST 0h = No effect 1h = Sets DIO18 in RIS register
17	DIO17	W	0h	DIO17 event Reset type: SYSRST 0h = No effect 1h = Sets DIO17 in RIS register
16	DIO16	W	0h	DIO16 event Reset type: SYSRST 0h = No effect 1h = Sets DIO16 in RIS register
15	DIO15	W	0h	DIO15 event Reset type: SYSRST 0h = No effect 1h = Sets DIO15 in RIS register

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Table 14-27. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	DIO14 event Reset type: SYSRST 0h = No effect 1h = Sets DIO14 in RIS register
13	DIO13	W	0h	DIO13 event Reset type: SYSRST 0h = No effect 1h = Sets DIO13 in RIS register
12	DIO12	W	0h	DIO12 event Reset type: SYSRST 0h = No effect 1h = Sets DIO12 in RIS register
11	DIO11	W	0h	DIO11 event Reset type: SYSRST 0h = No effect 1h = Sets DIO11 in RIS register
10	DIO10	W	0h	DIO10 event Reset type: SYSRST 0h = No effect 1h = Sets DIO10 in RIS register
9	DIO9	W	0h	DIO9 event Reset type: SYSRST 0h = No effect 1h = Sets DIO9 in RIS register
8	DIO8	W	0h	DIO8 event Reset type: SYSRST 0h = No effect 1h = Sets DIO8 in RIS register
7	DIO7	W	0h	DIO7 event Reset type: SYSRST 0h = No effect 1h = Sets DIO7 in RIS register
6	DIO6	W	0h	DIO6 event Reset type: SYSRST 0h = No effect 1h = Sets DIO6 in RIS register
5	DIO5	W	0h	DIO5 event Reset type: SYSRST 0h = No effect 1h = Sets DIO5 in RIS register
4	DIO4	W	0h	DIO4 event Reset type: SYSRST 0h = No effect 1h = Sets DIO4 in RIS register

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Table 14-27. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	W	0h	DIO3 event Reset type: SYSRST 0h = No effect 1h = Sets DIO3 in RIS register
2	DIO2	W	0h	DIO2 event Reset type: SYSRST 0h = No effect 1h = Sets DIO2 in RIS register
1	DIO1	W	0h	DIO1 event Reset type: SYSRST 0h = No effect 1h = Sets DIO1 in RIS register
0	DIO0	W	0h	DIO0 event Reset type: SYSRST 0h = No effect 1h = Sets DIO0 in RIS register

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11 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 14-14 and described in Table 14-18.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 14-14. ICLR Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-29. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	DIO31 event Reset type: SYSRST 0h = No effect 1h = Clears DIO31 in RIS register
30	DIO30	W	0h	DIO30 event Reset type: SYSRST 0h = No effect 1h = Clears DIO30 in RIS register
29	DIO29	W	0h	DIO29 event Reset type: SYSRST 0h = No effect 1h = Clears DIO29 in RIS register
28	DIO28	W	0h	DIO28 event Reset type: SYSRST 0h = No effect 1h = Clears DIO28 in RIS register
27	DIO27	W	0h	DIO27 event Reset type: SYSRST 0h = No effect 1h = Clears DIO27 in RIS register
26	DIO26	W	0h	DIO26 event Reset type: SYSRST 0h = No effect 1h = Clears DIO26 in RIS register

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Table 14-29. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	W	0h	DIO25 event Reset type: SYSRST 0h = No effect 1h = Clears DIO25 in RIS register
24	DIO24	W	0h	DIO24 event Reset type: SYSRST 0h = No effect 1h = Clears DIO24 in RIS register
23	DIO23	W	0h	DIO23 event Reset type: SYSRST 0h = No effect 1h = Clears DIO23 in RIS register
22	DIO22	W	0h	DIO22 event Reset type: SYSRST 0h = No effect 1h = Clears DIO22 in RIS register
21	DIO21	W	0h	DIO21 event Reset type: SYSRST 0h = No effect 1h = Clears DIO21 in RIS register
20	DIO20	W	0h	DIO20 event Reset type: SYSRST 0h = No effect 1h = Clears DIO20 in RIS register
19	DIO19	W	0h	DIO19 event Reset type: SYSRST 0h = No effect 1h = Clears DIO19 in RIS register
18	DIO18	W	0h	DIO18 event Reset type: SYSRST 0h = No effect 1h = Clears DIO18 in RIS register
17	DIO17	W	0h	DIO17 event Reset type: SYSRST 0h = No effect 1h = Clears DIO17 in RIS register
16	DIO16	W	0h	DIO16 event Reset type: SYSRST 0h = No effect 1h = Clears DIO16 in RIS register
15	DIO15	W	0h	DIO15 event Reset type: SYSRST 0h = No effect 1h = Clears DIO15 in RIS register

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Table 14-29. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	DIO14 event Reset type: SYSRST 0h = No effect 1h = Clears DIO14 in RIS register
13	DIO13	W	0h	DIO13 event Reset type: SYSRST 0h = No effect 1h = Clears DIO13 in RIS register
12	DIO12	W	0h	DIO12 event Reset type: SYSRST 0h = No effect 1h = Clears DIO12 in RIS register
11	DIO11	W	0h	DIO11 event Reset type: SYSRST 0h = No effect 1h = Clears DIO11 in RIS register
10	DIO10	W	0h	DIO10 event Reset type: SYSRST 0h = No effect 1h = Clears DIO10 in RIS register
9	DIO9	W	0h	DIO9 event Reset type: SYSRST 0h = No effect 1h = Clears DIO9 in RIS register
8	DIO8	W	0h	DIO8 event Reset type: SYSRST 0h = No effect 1h = Clears DIO8 in RIS register
7	DIO7	W	0h	DIO7 event Reset type: SYSRST 0h = No effect 1h = Clears DIO7 in RIS register
6	DIO6	W	0h	DIO6 event Reset type: SYSRST 0h = No effect 1h = Clears DIO6 in RIS register
5	DIO5	W	0h	DIO5 event Reset type: SYSRST 0h = No effect 1h = Clears DIO5 in RIS register
4	DIO4	W	0h	DIO4 event Reset type: SYSRST 0h = No effect 1h = Clears DIO4 in RIS register

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Table 14-29. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	W	0h	DIO3 event Reset type: SYSRST 0h = No effect 1h = Clears DIO3 in RIS register
2	DIO2	W	0h	DIO2 event Reset type: SYSRST 0h = No effect 1h = Clears DIO2 in RIS register
1	DIO1	W	0h	DIO1 event Reset type: SYSRST 0h = No effect 1h = Clears DIO1 in RIS register
0	DIO0	W	0h	DIO0 event Reset type: SYSRST 0h = No effect 1h = Clears DIO0 in RIS register

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12 IIDX Register (Offset = 1050h) [Reset = 00000000h] (GEN_EVENT0)

IIDX is shown in Figure 14-15 and described in Table 14-19.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 14-15. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 14-31. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status Reset type: SYSRST 0h = No bit is set means there is no pending interrupt request 1h = DIO0 interrupt 2h = DIO1 interrupt 3h = DIO2 interrupt 4h = DIO3 interrupt 5h = DIO4 interrupt 6h = DIO5 interrupt 7h = DIO6 interrupt 8h = DIO7 interrupt 9h = DIO8 interrupt Ah = DIO9 interrupt Bh = DIO10 interrupt Ch = DIO11 interrupt Dh = DIO12 interrupt Eh = DIO13 interrupt Fh = DIO14 interrupt 10h = DIO15 interrupt

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13 IMASK Register (Offset = 1058h) [Reset = 00000000h] (GEN_EVENT0)

IMASK is shown in Figure 14-16 and described in Table 14-20.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 14-16. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 14-33. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	DIO15	R/W	0h	DIO15 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
14	DIO14	R/W	0h	DIO14 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
13	DIO13	R/W	0h	DIO13 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
12	DIO12	R/W	0h	DIO12 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
11	DIO11	R/W	0h	DIO11 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
10	DIO10	R/W	0h	DIO10 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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Table 14-33. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DIO9	R/W	0h	DIO9 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
8	DIO8	R/W	0h	DIO8 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
7	DIO7	R/W	0h	DIO7 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
6	DIO6	R/W	0h	DIO6 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
5	DIO5	R/W	0h	DIO5 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
4	DIO4	R/W	0h	DIO4 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
3	DIO3	R/W	0h	DIO3 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
2	DIO2	R/W	0h	DIO2 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
1	DIO1	R/W	0h	DIO1 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
0	DIO0	R/W	0h	DIO0 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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14 RIS Register (Offset = 1060h) [Reset = 00000000h] (GEN_EVENT0)

RIS is shown in Figure 14-17 and described in Table 14-21.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 14-17. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14-35. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15	DIO15	R	0h	DIO15 event Reset type: SYSRST 0h = DIO15 event did not occur 1h = DIO15 event occurred
14	DIO14	R	0h	DIO14 event Reset type: SYSRST 0h = DIO14 event did not occur 1h = DIO14 event occurred
13	DIO13	R	0h	DIO13 event Reset type: SYSRST 0h = DIO13 event did not occur 1h = DIO13 event occurred
12	DIO12	R	0h	DIO12 event Reset type: SYSRST 0h = DIO12 event did not occur 1h = DIO12 event occurred
11	DIO11	R	0h	DIO11 event Reset type: SYSRST 0h = DIO11 event did not occur 1h = DIO11 event occurred

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Table 14-35. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIO10	R	0h	DIO10 event Reset type: SYSRST 0h = DIO10 event did not occur 1h = DIO10 event occurred
9	DIO9	R	0h	DIO9 event Reset type: SYSRST 0h = DIO9 event did not occur 1h = DIO9 event occurred
8	DIO8	R	0h	DIO8 event Reset type: SYSRST 0h = DIO8 event did not occur 1h = DIO8 event occurred
7	DIO7	R	0h	DIO7 event Reset type: SYSRST 0h = DIO7 event did not occur 1h = DIO7 event occurred
6	DIO6	R	0h	DIO6 event Reset type: SYSRST 0h = DIO6 event did not occur 1h = DIO6 event occurred
5	DIO5	R	0h	DIO5 event Reset type: SYSRST 0h = DIO5 event did not occur 1h = DIO5 event occurred
4	DIO4	R	0h	DIO4 event Reset type: SYSRST 0h = DIO4 event did not occur 1h = DIO4 event occurred
3	DIO3	R	0h	DIO3 event Reset type: SYSRST 0h = DIO3 event did not occur 1h = DIO3 event occurred
2	DIO2	R	0h	DIO2 event Reset type: SYSRST 0h = DIO2 event did not occur 1h = DIO2 event occurred
1	DIO1	R	0h	DIO1 event Reset type: SYSRST 0h = DIO1 event did not occur 1h = DIO1 event occurred
0	DIO0	R	0h	DIO0 event Reset type: SYSRST 0h = DIO0 event did not occur 1h = DIO0 event occurred

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15 MIS Register (Offset = 1068h) [Reset = 00000000h] (GEN_EVENT0)

MIS is shown in Figure 14-18 and described in Table 14-22.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 14-18. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14-37. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15	DIO15	R	0h	DIO15 event Reset type: SYSRST 0h = DIO15 event did not occur 1h = DIO15 event occurred
14	DIO14	R	0h	DIO14 event Reset type: SYSRST 0h = DIO14 event did not occur 1h = DIO14 event occurred
13	DIO13	R	0h	DIO13 event Reset type: SYSRST 0h = DIO13 event did not occur 1h = DIO13 event occurred
12	DIO12	R	0h	DIO12 event Reset type: SYSRST 0h = DIO12 event did not occur 1h = DIO12 event occurred
11	DIO11	R	0h	DIO11 event Reset type: SYSRST 0h = DIO11 event did not occur 1h = DIO11 event occurred
10	DIO10	R	0h	DIO10 event Reset type: SYSRST 0h = DIO10 event did not occur 1h = DIO10 event occurred

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Table 14-37. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DIO9	R	0h	DIO9 event Reset type: SYSRST 0h = DIO9 event did not occur 1h = DIO9 event occurred
8	DIO8	R	0h	DIO8 event Reset type: SYSRST 0h = DIO8 event did not occur 1h = DIO8 event occurred
7	DIO7	R	0h	DIO7 event Reset type: SYSRST 0h = DIO7 event did not occur 1h = DIO7 event occurred
6	DIO6	R	0h	DIO6 event Reset type: SYSRST 0h = DIO6 event did not occur 1h = DIO6 event occurred
5	DIO5	R	0h	DIO5 event Reset type: SYSRST 0h = DIO5 event did not occur 1h = DIO5 event occurred
4	DIO4	R	0h	DIO4 event Reset type: SYSRST 0h = DIO4 event did not occur 1h = DIO4 event occurred
3	DIO3	R	0h	DIO3 event Reset type: SYSRST 0h = DIO3 event did not occur 1h = DIO3 event occurred
2	DIO2	R	0h	DIO2 event Reset type: SYSRST 0h = DIO2 event did not occur 1h = DIO2 event occurred
1	DIO1	R	0h	DIO1 event Reset type: SYSRST 0h = DIO1 event did not occur 1h = DIO1 event occurred
0	DIO0	R	0h	DIO0 event Reset type: SYSRST 0h = DIO0 event did not occur 1h = DIO0 event occurred

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16 ISET Register (Offset = 1070h) [Reset = 00000000h] (GEN_EVENT0)

ISET is shown in Figure 14-19 and described in Table 14-23.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 14-19. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-39. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	W	0h	
15	DIO15	W	0h	DIO15 event Reset type: SYSRST 0h = No effect 1h = Sets DIO15 in RIS register
14	DIO14	W	0h	DIO14 event Reset type: SYSRST 0h = No effect 1h = Sets DIO14 in RIS register
13	DIO13	W	0h	DIO13 event Reset type: SYSRST 0h = No effect 1h = Sets DIO13 in RIS register
12	DIO12	W	0h	DIO12 event Reset type: SYSRST 0h = No effect 1h = Sets DIO12 in RIS register
11	DIO11	W	0h	DIO11 event Reset type: SYSRST 0h = No effect 1h = Sets DIO11 in RIS register

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Table 14-39. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DIO10	W	0h	DIO10 event Reset type: SYSRST 0h = No effect 1h = Sets DIO10 in RIS register
9	DIO9	W	0h	DIO9 event Reset type: SYSRST 0h = No effect 1h = Sets DIO9 in RIS register
8	DIO8	W	0h	DIO8 event Reset type: SYSRST 0h = No effect 1h = Sets DIO8 in RIS register
7	DIO7	W	0h	DIO7 event Reset type: SYSRST 0h = No effect 1h = Sets DIO7 in RIS register
6	DIO6	W	0h	DIO6 event Reset type: SYSRST 0h = No effect 1h = Sets DIO6 in RIS register
5	DIO5	W	0h	DIO5 event Reset type: SYSRST 0h = No effect 1h = Sets DIO5 in RIS register
4	DIO4	W	0h	DIO4 event Reset type: SYSRST 0h = No effect 1h = Sets DIO4 in RIS register
3	DIO3	W	0h	DIO3 event Reset type: SYSRST 0h = No effect 1h = Sets DIO3 in RIS register
2	DIO2	W	0h	DIO2 event Reset type: SYSRST 0h = No effect 1h = Sets DIO2 in RIS register
1	DIO1	W	0h	DIO1 event Reset type: SYSRST 0h = No effect 1h = Sets DIO1 in RIS register
0	DIO0	W	0h	DIO0 event Reset type: SYSRST 0h = No effect 1h = Sets DIO0 in RIS register

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17 ICLR Register (Offset = 1078h) [Reset = 00000000h] (GEN_EVENT0)

ICLR is shown in Figure 14-20 and described in Table 14-24.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 14-20. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-41. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	W	0h	
15	DIO15	W	0h	DIO15 event Reset type: SYSRST 0h = No effect 1h = Clears DIO15 in RIS register
14	DIO14	W	0h	DIO14 event Reset type: SYSRST 0h = No effect 1h = Clears DIO14 in RIS register
13	DIO13	W	0h	DIO13 event Reset type: SYSRST 0h = No effect 1h = Clears DIO13 in RIS register
12	DIO12	W	0h	DIO12 event Reset type: SYSRST 0h = No effect 1h = Clears DIO12 in RIS register
11	DIO11	W	0h	DIO11 event Reset type: SYSRST 0h = No effect 1h = Clears DIO11 in RIS register
10	DIO10	W	0h	DIO10 event Reset type: SYSRST 0h = No effect 1h = Clears DIO10 in RIS register

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Table 14-41. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	DIO9	W	0h	DIO9 event Reset type: SYSRST 0h = No effect 1h = Clears DIO9 in RIS register
8	DIO8	W	0h	DIO8 event Reset type: SYSRST 0h = No effect 1h = Clears DIO8 in RIS register
7	DIO7	W	0h	DIO7 event Reset type: SYSRST 0h = No effect 1h = Clears DIO7 in RIS register
6	DIO6	W	0h	DIO6 event Reset type: SYSRST 0h = No effect 1h = Clears DIO6 in RIS register
5	DIO5	W	0h	DIO5 event Reset type: SYSRST 0h = No effect 1h = Clears DIO5 in RIS register
4	DIO4	W	0h	DIO4 event Reset type: SYSRST 0h = No effect 1h = Clears DIO4 in RIS register
3	DIO3	W	0h	DIO3 event Reset type: SYSRST 0h = No effect 1h = Clears DIO3 in RIS register
2	DIO2	W	0h	DIO2 event Reset type: SYSRST 0h = No effect 1h = Clears DIO2 in RIS register
1	DIO1	W	0h	DIO1 event Reset type: SYSRST 0h = No effect 1h = Clears DIO1 in RIS register
0	DIO0	W	0h	DIO0 event Reset type: SYSRST 0h = No effect 1h = Clears DIO0 in RIS register

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18 IIDX Register (Offset = 1080h) [Reset = 00000000h] (GEN_EVENT1)

IIDX is shown in Figure 14-21 and described in Table 14-25.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 14-21. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 14-43. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status Reset type: SYSRST 0h = No bit is set means there is no pending interrupt request 1h = DIO0 interrupt 2h = DIO1 interrupt 3h = DIO2 interrupt 4h = DIO3 interrupt 5h = DIO4 interrupt 6h = DIO5 interrupt 7h = DIO6 interrupt 8h = DIO7 interrupt 9h = DIO8 interrupt Ah = DIO9 interrupt Bh = DIO10 interrupt Ch = DIO11 interrupt Dh = DIO12 interrupt Eh = DIO13 interrupt Fh = DIO14 interrupt 10h = DIO15 interrupt

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19 IMASK Register (Offset = 1088h) [Reset = 00000000h] (GEN_EVENT1)

IMASK is shown in Figure 14-22 and described in Table 14-26.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 14-22. IMASK Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 14-45. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R/W	0h	DIO31 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
30	DIO30	R/W	0h	DIO30 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
29	DIO29	R/W	0h	DIO29 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
28	DIO28	R/W	0h	DIO28 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
27	DIO27	R/W	0h	DIO27 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
26	DIO26	R/W	0h	DIO26 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked

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Table 14-45. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R/W	0h	DIO25 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
24	DIO24	R/W	0h	DIO24 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
23	DIO23	R/W	0h	DIO23 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
22	DIO22	R/W	0h	DIO22 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
21	DIO21	R/W	0h	DIO21 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
20	DIO20	R/W	0h	DIO20 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
19	DIO19	R/W	0h	DIO19 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
18	DIO18	R/W	0h	DIO18 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
17	DIO17	R/W	0h	DIO17 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
16	DIO16	R/W	0h	DIO16 event mask Reset type: SYSRST 0h = Event is masked 1h = Event is unmasked
15-0	RESERVED	R/W	0h	

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20 RIS Register (Offset = 1090h) [Reset = 00000000h] (GEN_EVENT1)

RIS is shown in Figure 14-23 and described in Table 14-27.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 14-23. RIS Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 14-47. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R	0h	DIO31 event Reset type: SYSRST 0h = DIO31 event did not occur 1h = DIO31 event occurred
30	DIO30	R	0h	DIO30 event Reset type: SYSRST 0h = DIO30 event did not occur 1h = DIO30 event occurred
29	DIO29	R	0h	DIO29 event Reset type: SYSRST 0h = DIO29 event did not occur 1h = DIO29 event occurred
28	DIO28	R	0h	DIO28 event Reset type: SYSRST 0h = DIO28 event did not occur 1h = DIO28 event occurred
27	DIO27	R	0h	DIO27 event Reset type: SYSRST 0h = DIO27 event did not occur 1h = DIO27 event occurred
26	DIO26	R	0h	DIO26 event Reset type: SYSRST 0h = DIO26 event did not occur 1h = DIO26 event occurred

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Table 14-47. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R	0h	DIO25 event Reset type: SYSRST 0h = DIO25 event did not occur 1h = DIO25 event occurred
24	DIO24	R	0h	DIO24 event Reset type: SYSRST 0h = DIO24 event did not occur 1h = DIO24 event occurred
23	DIO23	R	0h	DIO23 event Reset type: SYSRST 0h = DIO23 event did not occur 1h = DIO23 event occurred
22	DIO22	R	0h	DIO22 event Reset type: SYSRST 0h = DIO22 event did not occur 1h = DIO22 event occurred
21	DIO21	R	0h	DIO21 event Reset type: SYSRST 0h = DIO21 event did not occur 1h = DIO21 event occurred
20	DIO20	R	0h	DIO20 event Reset type: SYSRST 0h = DIO20 event did not occur 1h = DIO20 event occurred
19	DIO19	R	0h	DIO19 event Reset type: SYSRST 0h = DIO19 event did not occur 1h = DIO19 event occurred
18	DIO18	R	0h	DIO18 event Reset type: SYSRST 0h = DIO18 event did not occur 1h = DIO18 event occurred
17	DIO17	R	0h	DIO17 event Reset type: SYSRST 0h = DIO17 event did not occur 1h = DIO17 event occurred
16	DIO16	R	0h	DIO16 event Reset type: SYSRST 0h = DIO16 event did not occur 1h = DIO16 event occurred
15-0	RESERVED	R	0h	

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21 MIS Register (Offset = 1098h) [Reset = 00000000h] (GEN_EVENT1)

MIS is shown in Figure 14-24 and described in Table 14-28.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 14-24. MIS Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 14-49. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R	0h	DIO31 event Reset type: SYSRST 0h = DIO31 event did not occur 1h = DIO31 event occurred
30	DIO30	R	0h	DIO30 event Reset type: SYSRST 0h = DIO30 event did not occur 1h = DIO30 event occurred
29	DIO29	R	0h	DIO29 event Reset type: SYSRST 0h = DIO29 event did not occur 1h = DIO29 event occurred
28	DIO28	R	0h	DIO28 event Reset type: SYSRST 0h = DIO28 event did not occur 1h = DIO28 event occurred
27	DIO27	R	0h	DIO27 event Reset type: SYSRST 0h = DIO27 event did not occur 1h = DIO27 event occurred
26	DIO26	R	0h	DIO26 event Reset type: SYSRST 0h = DIO26 event did not occur 1h = DIO26 event occurred

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Table 14-49. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R	0h	DIO25 event Reset type: SYSRST 0h = DIO25 event did not occur 1h = DIO25 event occurred
24	DIO24	R	0h	DIO24 event Reset type: SYSRST 0h = DIO24 event did not occur 1h = DIO24 event occurred
23	DIO23	R	0h	DIO23 event Reset type: SYSRST 0h = DIO23 event did not occur 1h = DIO23 event occurred
22	DIO22	R	0h	DIO22 event Reset type: SYSRST 0h = DIO22 event did not occur 1h = DIO22 event occurred
21	DIO21	R	0h	DIO21 event Reset type: SYSRST 0h = DIO21 event did not occur 1h = DIO21 event occurred
20	DIO20	R	0h	DIO20 event Reset type: SYSRST 0h = DIO20 event did not occur 1h = DIO20 event occurred
19	DIO19	R	0h	DIO19 event Reset type: SYSRST 0h = DIO19 event did not occur 1h = DIO19 event occurred
18	DIO18	R	0h	DIO18 event Reset type: SYSRST 0h = DIO18 event did not occur 1h = DIO18 event occurred
17	DIO17	R	0h	DIO17 event Reset type: SYSRST 0h = DIO17 event did not occur 1h = DIO17 event occurred
16	DIO16	R	0h	DIO16 event Reset type: SYSRST 0h = DIO16 event did not occur 1h = DIO16 event occurred
15-0	RESERVED	R	0h	

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22 ISET Register (Offset = 10A0h) [Reset = 00000000h] (GEN_EVENT1)

ISET is shown in Figure 14-25 and described in Table 14-29.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 14-25. ISET Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							
W-0h							

Table 14-51. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	DIO31 event Reset type: SYSRST 0h = No effect 1h = Sets DIO31 in RIS register
30	DIO30	W	0h	DIO30 event Reset type: SYSRST 0h = No effect 1h = Sets DIO30 in RIS register
29	DIO29	W	0h	DIO29 event Reset type: SYSRST 0h = No effect 1h = Sets DIO29 in RIS register
28	DIO28	W	0h	DIO28 event Reset type: SYSRST 0h = No effect 1h = Sets DIO28 in RIS register
27	DIO27	W	0h	DIO27 event Reset type: SYSRST 0h = No effect 1h = Sets DIO27 in RIS register
26	DIO26	W	0h	DIO26 event Reset type: SYSRST 0h = No effect 1h = Sets DIO26 in RIS register

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Table 14-51. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	W	0h	DIO25 event Reset type: SYSRST 0h = No effect 1h = Sets DIO25 in RIS register
24	DIO24	W	0h	DIO24 event Reset type: SYSRST 0h = No effect 1h = Sets DIO24 in RIS register
23	DIO23	W	0h	DIO23 event Reset type: SYSRST 0h = No effect 1h = Sets DIO23 in RIS register
22	DIO22	W	0h	DIO22 event Reset type: SYSRST 0h = No effect 1h = Sets DIO22 in RIS register
21	DIO21	W	0h	DIO21 event Reset type: SYSRST 0h = No effect 1h = Sets DIO21 in RIS register
20	DIO20	W	0h	DIO20 event Reset type: SYSRST 0h = No effect 1h = Sets DIO20 in RIS register
19	DIO19	W	0h	DIO19 event Reset type: SYSRST 0h = No effect 1h = Sets DIO19 in RIS register
18	DIO18	W	0h	DIO18 event Reset type: SYSRST 0h = No effect 1h = Sets DIO18 in RIS register
17	DIO17	W	0h	DIO17 event Reset type: SYSRST 0h = No effect 1h = Sets DIO17 in RIS register
16	DIO16	W	0h	DIO16 event Reset type: SYSRST 0h = No effect 1h = Sets DIO16 in RIS register
15-0	RESERVED	W	0h	

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23 ICLR Register (Offset = 10A8h) [Reset = 00000000h] (GEN_EVENT1)

ICLR is shown in Figure 14-26 and described in Table 14-30.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 14-26. ICLR Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							
W-0h							

Table 14-53. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	DIO31 event Reset type: SYSRST 0h = No effect 1h = Clears DIO31 in RIS register
30	DIO30	W	0h	DIO30 event Reset type: SYSRST 0h = No effect 1h = Clears DIO30 in RIS register
29	DIO29	W	0h	DIO29 event Reset type: SYSRST 0h = No effect 1h = Clears DIO29 in RIS register
28	DIO28	W	0h	DIO28 event Reset type: SYSRST 0h = No effect 1h = Clears DIO28 in RIS register
27	DIO27	W	0h	DIO27 event Reset type: SYSRST 0h = No effect 1h = Clears DIO27 in RIS register
26	DIO26	W	0h	DIO26 event Reset type: SYSRST 0h = No effect 1h = Clears DIO26 in RIS register

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Table 14-53. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	W	0h	DIO25 event Reset type: SYSRST 0h = No effect 1h = Clears DIO25 in RIS register
24	DIO24	W	0h	DIO24 event Reset type: SYSRST 0h = No effect 1h = Clears DIO24 in RIS register
23	DIO23	W	0h	DIO23 event Reset type: SYSRST 0h = No effect 1h = Clears DIO23 in RIS register
22	DIO22	W	0h	DIO22 event Reset type: SYSRST 0h = No effect 1h = Clears DIO22 in RIS register
21	DIO21	W	0h	DIO21 event Reset type: SYSRST 0h = No effect 1h = Clears DIO21 in RIS register
20	DIO20	W	0h	DIO20 event Reset type: SYSRST 0h = No effect 1h = Clears DIO20 in RIS register
19	DIO19	W	0h	DIO19 event Reset type: SYSRST 0h = No effect 1h = Clears DIO19 in RIS register
18	DIO18	W	0h	DIO18 event Reset type: SYSRST 0h = No effect 1h = Clears DIO18 in RIS register
17	DIO17	W	0h	DIO17 event Reset type: SYSRST 0h = No effect 1h = Clears DIO17 in RIS register
16	DIO16	W	0h	DIO16 event Reset type: SYSRST 0h = No effect 1h = Clears DIO16 in RIS register
15-0	RESERVED	W	0h	

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24 EVT_MODE Register (Offset = 10E0h) [Reset = 00000000h]

EVT_MODE is shown in Figure 14-27 and described in Table 14-31.

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Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 14-27. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		EVT2_CFG		EVT1_CFG		INT0_CFG	
R/W-0h		R-0h		R-0h		R-0h	

Table 14-55. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-4	EVT2_CFG	R	2h	Event line mode select for event corresponding to [IPSTANDARD.GEN_EVENT1] Reset type: SYSRST 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
3-2	EVT1_CFG	R	2h	Event line mode select for event corresponding to [IPSTANDARD.GEN_EVENT0] Reset type: SYSRST 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
1-0	INT0_CFG	R	1h	Event line mode select for event corresponding to [IPSTANDARD.CPU_INT] Reset type: SYSRST 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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25 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 14-28 and described in Table 14-32.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 14-28. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R-0h				R-0h				R-0h				R-0h			

Table 14-57. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	RESERVED	R	0h	Reserved
11-8	RESERVED	R	0h	
7-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

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26 DOUT3_0 Register (Offset = 1200h) [Reset = 00000000h]

DOUT3_0 is shown in Figure 14-29 and described in Table 14-33.

Return to the Summary Table.

Data output for pins configured as DIO3 to DIO0. This is an alias register for byte access to bits 3 to 0 in DOUT31_0 register.

Figure 14-29. DOUT3_0 Register

31	30	29	28	27	26	25	24
RESERVED							DIO3
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO2
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO1
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO0
W-0h							W-0h

Table 14-59. DOUT3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO3	W	0h	This bit sets the value of the pin configured as DIO3 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO2	W	0h	This bit sets the value of the pin configured as DIO2 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO1	W	0h	This bit sets the value of the pin configured as DIO1 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO0	W	0h	This bit sets the value of the pin configured as DIO0 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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27 DOUT7_4 Register (Offset = 1204h) [Reset = 00000000h]

DOUT7_4 is shown in Figure 14-30 and described in Table 14-34.

Return to the Summary Table.

Data output for pins configured as DIO7 to DIO4. This is an alias register for byte access to bits 7 to 4 in DOUT31_0 register.

Figure 14-30. DOUT7_4 Register

31	30	29	28	27	26	25	24
RESERVED							DIO7
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO6
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO5
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO4
W-0h							W-0h

Table 14-61. DOUT7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO7	W	0h	This bit sets the value of the pin configured as DIO7 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO6	W	0h	This bit sets the value of the pin configured as DIO6 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO5	W	0h	This bit sets the value of the pin configured as DIO5 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO4	W	0h	This bit sets the value of the pin configured as DIO4 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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28 DOUT11_8 Register (Offset = 1208h) [Reset = 00000000h]

DOUT11_8 is shown in Figure 14-31 and described in Table 14-35.

Return to the Summary Table.

Data output for pins configured as DIO11 to DIO8. This is an alias register for byte access to bits 11 to 8 in DOUT31_0 register.

Figure 14-31. DOUT11_8 Register

31	30	29	28	27	26	25	24
RESERVED							DIO11
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO10
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO9
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO8
W-0h							W-0h

Table 14-63. DOUT11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO11	W	0h	This bit sets the value of the pin configured as DIO11 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO10	W	0h	This bit sets the value of the pin configured as DIO10 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO9	W	0h	This bit sets the value of the pin configured as DIO9 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO8	W	0h	This bit sets the value of the pin configured as DIO8 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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29 DOUT15_12 Register (Offset = 120Ch) [Reset = 00000000h]

DOUT15_12 is shown in Figure 14-32 and described in Table 14-36.

Return to the Summary Table.

Data output for pins configured as DIO15 to DIO12. This is an alias register for byte access to bits 15 to 12 in DOUT31_0 register.

Figure 14-32. DOUT15_12 Register

31	30	29	28	27	26	25	24
RESERVED							DIO15
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO14
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO13
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO12
W-0h							W-0h

Table 14-65. DOUT15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO15	W	0h	This bit sets the value of the pin configured as DIO15 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO14	W	0h	This bit sets the value of the pin configured as DIO14 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO13	W	0h	This bit sets the value of the pin configured as DIO13 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO12	W	0h	This bit sets the value of the pin configured as DIO12 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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30 DOUT19_16 Register (Offset = 1210h) [Reset = 00000000h]

DOUT19_16 is shown in Figure 14-33 and described in Table 14-37.

Return to the Summary Table.

Data output for pins configured as DIO19 to DIO16. This is an alias register for byte access to bits 19 to 16 in DOUT31_0 register.

Figure 14-33. DOUT19_16 Register

31	30	29	28	27	26	25	24
RESERVED							DIO19
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO18
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO17
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO16
W-0h							W-0h

Table 14-67. DOUT19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO19	W	0h	This bit sets the value of the pin configured as DIO19 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO18	W	0h	This bit sets the value of the pin configured as DIO18 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO17	W	0h	This bit sets the value of the pin configured as DIO17 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO16	W	0h	This bit sets the value of the pin configured as DIO16 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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31 DOUT23_20 Register (Offset = 1214h) [Reset = 00000000h]

DOUT23_20 is shown in Figure 14-34 and described in Table 14-38.

Return to the Summary Table.

Data output for pins configured as DIO23 to DIO20. This is an alias register for byte access to bits 23 to 20 in DOUT31_0 register.

Figure 14-34. DOUT23_20 Register

31	30	29	28	27	26	25	24
RESERVED							DIO23
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO22
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO21
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO20
W-0h							W-0h

Table 14-69. DOUT23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO23	W	0h	This bit sets the value of the pin configured as DIO23 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO22	W	0h	This bit sets the value of the pin configured as DIO22 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO21	W	0h	This bit sets the value of the pin configured as DIO21 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO20	W	0h	This bit sets the value of the pin configured as DIO20 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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32 DOUT27_24 Register (Offset = 1218h) [Reset = 00000000h]

DOUT27_24 is shown in Figure 14-35 and described in Table 14-39.

Return to the Summary Table.

Data output for pins configured as DIO27 to DIO24. This is an alias register for byte access to bits 27 to 24 in DOUT31_0 register.

Figure 14-35. DOUT27_24 Register

31	30	29	28	27	26	25	24
RESERVED							DIO27
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO26
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO25
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO24
W-0h							W-0h

Table 14-71. DOUT27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO27	W	0h	This bit sets the value of the pin configured as DIO27 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO26	W	0h	This bit sets the value of the pin configured as DIO26 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO25	W	0h	This bit sets the value of the pin configured as DIO25 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO24	W	0h	This bit sets the value of the pin configured as DIO24 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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33 DOUT31_28 Register (Offset = 121Ch) [Reset = 00000000h]

DOUT31_28 is shown in Figure 14-36 and described in Table 14-40.

Return to the Summary Table.

Data output for pins configured as DIO31 to DIO28. This is an alias register for byte access to bits 31 to 28 in DOUT31_0 register.

Figure 14-36. DOUT31_28 Register

31	30	29	28	27	26	25	24
RESERVED							DIO31
W-0h							W-0h
23	22	21	20	19	18	17	16
RESERVED							DIO30
W-0h							W-0h
15	14	13	12	11	10	9	8
RESERVED							DIO29
W-0h							W-0h
7	6	5	4	3	2	1	0
RESERVED							DIO28
W-0h							W-0h

Table 14-73. DOUT31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	0h	
24	DIO31	W	0h	This bit sets the value of the pin configured as DIO31 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23-17	RESERVED	W	0h	
16	DIO30	W	0h	This bit sets the value of the pin configured as DIO30 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15-9	RESERVED	W	0h	
8	DIO29	W	0h	This bit sets the value of the pin configured as DIO29 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7-1	RESERVED	W	0h	
0	DIO28	W	0h	This bit sets the value of the pin configured as DIO28 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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34 DOUT31_0 Register (Offset = 1280h) [Reset = 00000000h]

DOUT31_0 is shown in Figure 14-37 and described in Table 14-41.

Return to the Summary Table.

Data output for pins configured as DIO31 to DIO0.

Figure 14-37. DOUT31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 14-75. DOUT31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R/W	0h	This bit sets the value of the pin configured as DIO31 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
30	DIO30	R/W	0h	This bit sets the value of the pin configured as DIO30 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
29	DIO29	R/W	0h	This bit sets the value of the pin configured as DIO29 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
28	DIO28	R/W	0h	This bit sets the value of the pin configured as DIO28 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
27	DIO27	R/W	0h	This bit sets the value of the pin configured as DIO27 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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Table 14-75. DOUT31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DIO26	R/W	0h	This bit sets the value of the pin configured as DIO26 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
25	DIO25	R/W	0h	This bit sets the value of the pin configured as DIO25 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
24	DIO24	R/W	0h	This bit sets the value of the pin configured as DIO24 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
23	DIO23	R/W	0h	This bit sets the value of the pin configured as DIO23 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
22	DIO22	R/W	0h	This bit sets the value of the pin configured as DIO22 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
21	DIO21	R/W	0h	This bit sets the value of the pin configured as DIO21 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
20	DIO20	R/W	0h	This bit sets the value of the pin configured as DIO20 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
19	DIO19	R/W	0h	This bit sets the value of the pin configured as DIO19 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
18	DIO18	R/W	0h	This bit sets the value of the pin configured as DIO18 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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Table 14-75. DOUT31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIO17	R/W	0h	This bit sets the value of the pin configured as DIO17 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
16	DIO16	R/W	0h	This bit sets the value of the pin configured as DIO16 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
15	DIO15	R/W	0h	This bit sets the value of the pin configured as DIO15 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
14	DIO14	R/W	0h	This bit sets the value of the pin configured as DIO14 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
13	DIO13	R/W	0h	This bit sets the value of the pin configured as DIO13 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
12	DIO12	R/W	0h	This bit sets the value of the pin configured as DIO12 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
11	DIO11	R/W	0h	This bit sets the value of the pin configured as DIO11 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
10	DIO10	R/W	0h	This bit sets the value of the pin configured as DIO10 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
9	DIO9	R/W	0h	This bit sets the value of the pin configured as DIO9 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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Table 14-75. DOUT31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DIO8	R/W	0h	This bit sets the value of the pin configured as DIO8 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
7	DIO7	R/W	0h	This bit sets the value of the pin configured as DIO7 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
6	DIO6	R/W	0h	This bit sets the value of the pin configured as DIO6 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
5	DIO5	R/W	0h	This bit sets the value of the pin configured as DIO5 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
4	DIO4	R/W	0h	This bit sets the value of the pin configured as DIO4 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
3	DIO3	R/W	0h	This bit sets the value of the pin configured as DIO3 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
2	DIO2	R/W	0h	This bit sets the value of the pin configured as DIO2 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
1	DIO1	R/W	0h	This bit sets the value of the pin configured as DIO1 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1
0	DIO0	R/W	0h	This bit sets the value of the pin configured as DIO0 when the output is enabled through DOE31_0 register. Reset type: SYSRST 0h = Output is set to 0 1h = Output is set to 1

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35 DOUTSET31_0 Register (Offset = 1290h) [Reset = 00000000h]

DOUTSET31_0 is shown in Figure 14-38 and described in Table 14-42.

Return to the Summary Table.

Writing 1 to a bit position in this register sets the corresponding bit in the DOUT31_0 register.

Figure 14-38. DOUTSET31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-77. DOUTSET31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	Writing 1 to this bit sets the DIO31 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO31 in DOUT31_0
30	DIO30	W	0h	Writing 1 to this bit sets the DIO30 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO30 in DOUT31_0
29	DIO29	W	0h	Writing 1 to this bit sets the DIO29 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO29 in DOUT31_0
28	DIO28	W	0h	Writing 1 to this bit sets the DIO28 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO28 in DOUT31_0
27	DIO27	W	0h	Writing 1 to this bit sets the DIO27 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO27 in DOUT31_0

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Table 14-77. DOUTSET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DIO26	W	0h	Writing 1 to this bit sets the DIO26 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO26 in DOUT31_0
25	DIO25	W	0h	Writing 1 to this bit sets the DIO25 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO25 in DOUT31_0
24	DIO24	W	0h	Writing 1 to this bit sets the DIO24 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO24 in DOUT31_0
23	DIO23	W	0h	Writing 1 to this bit sets the DIO23 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO23 in DOUT31_0
22	DIO22	W	0h	Writing 1 to this bit sets the DIO22 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO22 in DOUT31_0
21	DIO21	W	0h	Writing 1 to this bit sets the DIO21 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO21 in DOUT31_0
20	DIO20	W	0h	Writing 1 to this bit sets the DIO20 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO20 in DOUT31_0
19	DIO19	W	0h	Writing 1 to this bit sets the DIO19 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO19 in DOUT31_0
18	DIO18	W	0h	Writing 1 to this bit sets the DIO18 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO18 in DOUT31_0

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Table 14-77. DOUTSET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIO17	W	0h	Writing 1 to this bit sets the DIO17 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO17 in DOUT31_0
16	DIO16	W	0h	Writing 1 to this bit sets the DIO16 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO16 in DOUT31_0
15	DIO15	W	0h	Writing 1 to this bit sets the DIO15 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO15 in DOUT31_0
14	DIO14	W	0h	Writing 1 to this bit sets the DIO14 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO14 in DOUT31_0
13	DIO13	W	0h	Writing 1 to this bit sets the DIO13 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO13 in DOUT31_0
12	DIO12	W	0h	Writing 1 to this bit sets the DIO12 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO12 in DOUT31_0
11	DIO11	W	0h	Writing 1 to this bit sets the DIO11 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO11 in DOUT31_0
10	DIO10	W	0h	Writing 1 to this bit sets the DIO10 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO10 in DOUT31_0
9	DIO9	W	0h	Writing 1 to this bit sets the DIO9 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO9 in DOUT31_0

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Table 14-77. DOUTSET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DIO8	W	0h	Writing 1 to this bit sets the DIO8 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO8 in DOUT31_0
7	DIO7	W	0h	Writing 1 to this bit sets the DIO7 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO7 in DOUT31_0
6	DIO6	W	0h	Writing 1 to this bit sets the DIO6 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO6 in DOUT31_0
5	DIO5	W	0h	Writing 1 to this bit sets the DIO5 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO5 in DOUT31_0
4	DIO4	W	0h	Writing 1 to this bit sets the DIO4 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO4 in DOUT31_0
3	DIO3	W	0h	Writing 1 to this bit sets the DIO3 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO3 in DOUT31_0
2	DIO2	W	0h	Writing 1 to this bit sets the DIO2 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO2 in DOUT31_0
1	DIO1	W	0h	Writing 1 to this bit sets the DIO1 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO1 in DOUT31_0
0	DIO0	W	0h	Writing 1 to this bit sets the DIO0 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO0 in DOUT31_0

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36 DOUTCLR31_0 Register (Offset = 12A0h) [Reset = 00000000h]

DOUTCLR31_0 is shown in Figure 14-39 and described in Table 14-43.

Return to the Summary Table.

Writing 1 to a bit position in this register clears the corresponding bit in the DOUT31_0 register.

Figure 14-39. DOUTCLR31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-79. DOUTCLR31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	Writing 1 to this bit clears the DIO31 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO31 in DOUT31_0
30	DIO30	W	0h	Writing 1 to this bit clears the DIO30 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO30 in DOUT31_0
29	DIO29	W	0h	Writing 1 to this bit clears the DIO29 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO29 in DOUT31_0
28	DIO28	W	0h	Writing 1 to this bit clears the DIO28 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO28 in DOUT31_0
27	DIO27	W	0h	Writing 1 to this bit clears the DIO27 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO27 in DOUT31_0

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Table 14-79. DOUTCLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DIO26	W	0h	Writing 1 to this bit clears the DIO26 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO26 in DOUT31_0
25	DIO25	W	0h	Writing 1 to this bit clears the DIO25 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO25 in DOUT31_0
24	DIO24	W	0h	Writing 1 to this bit clears the DIO24 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO24 in DOUT31_0
23	DIO23	W	0h	Writing 1 to this bit clears the DIO23 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO23 in DOUT31_0
22	DIO22	W	0h	Writing 1 to this bit clears the DIO22 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO22 in DOUT31_0
21	DIO21	W	0h	Writing 1 to this bit clears the DIO21 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO21 in DOUT31_0
20	DIO20	W	0h	Writing 1 to this bit clears the DIO20 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO20 in DOUT31_0
19	DIO19	W	0h	Writing 1 to this bit clears the DIO19 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO19 in DOUT31_0
18	DIO18	W	0h	Writing 1 to this bit clears the DIO18 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO18 in DOUT31_0

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Table 14-79. DOUTCLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIO17	W	0h	Writing 1 to this bit clears the DIO17 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO17 in DOUT31_0
16	DIO16	W	0h	Writing 1 to this bit clears the DIO16 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO16 in DOUT31_0
15	DIO15	W	0h	Writing 1 to this bit clears the DIO15 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO15 in DOUT31_0
14	DIO14	W	0h	Writing 1 to this bit clears the DIO14 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO14 in DOUT31_0
13	DIO13	W	0h	Writing 1 to this bit clears the DIO13 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO13 in DOUT31_0
12	DIO12	W	0h	Writing 1 to this bit clears the DIO12 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO12 in DOUT31_0
11	DIO11	W	0h	Writing 1 to this bit clears the DIO11 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO11 in DOUT31_0
10	DIO10	W	0h	Writing 1 to this bit clears the DIO10 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO10 in DOUT31_0
9	DIO9	W	0h	Writing 1 to this bit clears the DIO9 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO9 in DOUT31_0

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Table 14-79. DOUTCLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DIO8	W	0h	Writing 1 to this bit clears the DIO8 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO8 in DOUT31_0
7	DIO7	W	0h	Writing 1 to this bit clears the DIO7 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO7 in DOUT31_0
6	DIO6	W	0h	Writing 1 to this bit clears the DIO6 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO6 in DOUT31_0
5	DIO5	W	0h	Writing 1 to this bit clears the DIO5 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO5 in DOUT31_0
4	DIO4	W	0h	Writing 1 to this bit clears the DIO4 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO4 in DOUT31_0
3	DIO3	W	0h	Writing 1 to this bit clears the DIO3 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO3 in DOUT31_0
2	DIO2	W	0h	Writing 1 to this bit clears the DIO2 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO2 in DOUT31_0
1	DIO1	W	0h	Writing 1 to this bit clears the DIO1 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO1 in DOUT31_0
0	DIO0	W	0h	Writing 1 to this bit clears the DIO0 bit in the DOUT31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO0 in DOUT31_0

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37 DOUTTGL31_0 Register (Offset = 12B0h) [Reset = 00000000h]

DOUTTGL31_0 is shown in Figure 14-40 and described in Table 14-44.

Return to the Summary Table.

Writing 1 to a bit position in this register will invert the corresponding DIO output.

Figure 14-40. DOUTTGL31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-81. DOUTTGL31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	This bit is used to toggle DIO31 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
30	DIO30	W	0h	This bit is used to toggle DIO30 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
29	DIO29	W	0h	This bit is used to toggle DIO29 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
28	DIO28	W	0h	This bit is used to toggle DIO28 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
27	DIO27	W	0h	This bit is used to toggle DIO27 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
26	DIO26	W	0h	This bit is used to toggle DIO26 output. Reset type: SYSRST 0h = No effect 1h = Toggle output

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Table 14-81. DOUTTGL31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	W	0h	This bit is used to toggle DIO25 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
24	DIO24	W	0h	This bit is used to toggle DIO24 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
23	DIO23	W	0h	This bit is used to toggle DIO23 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
22	DIO22	W	0h	This bit is used to toggle DIO22 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
21	DIO21	W	0h	This bit is used to toggle DIO21 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
20	DIO20	W	0h	This bit is used to toggle DIO20 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
19	DIO19	W	0h	This bit is used to toggle DIO19 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
18	DIO18	W	0h	This bit is used to toggle DIO18 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
17	DIO17	W	0h	This bit is used to toggle DIO17 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
16	DIO16	W	0h	This bit is used to toggle DIO16 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
15	DIO15	W	0h	This bit is used to toggle DIO15 output. Reset type: SYSRST 0h = No effect 1h = Toggle output

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Table 14-81. DOUTTGL31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	W	0h	This bit is used to toggle DIO14 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
13	DIO13	W	0h	This bit is used to toggle DIO13 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
12	DIO12	W	0h	This bit is used to toggle DIO12 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
11	DIO11	W	0h	This bit is used to toggle DIO11 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
10	DIO10	W	0h	This bit is used to toggle DIO10 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
9	DIO9	W	0h	This bit is used to toggle DIO9 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
8	DIO8	W	0h	This bit is used to toggle DIO8 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
7	DIO7	W	0h	This bit is used to toggle DIO7 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
6	DIO6	W	0h	This bit is used to toggle DIO6 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
5	DIO5	W	0h	This bit is used to toggle DIO5 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
4	DIO4	W	0h	This bit is used to toggle DIO4 output. Reset type: SYSRST 0h = No effect 1h = Toggle output

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Table 14-81. DOUTTGL31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	W	0h	This bit is used to toggle DIO3 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
2	DIO2	W	0h	This bit is used to toggle DIO2 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
1	DIO1	W	0h	This bit is used to toggle DIO1 output. Reset type: SYSRST 0h = No effect 1h = Toggle output
0	DIO0	W	0h	This bit is used to toggle DIO0 output. Reset type: SYSRST 0h = No effect 1h = Toggle output

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38 DOE31_0 Register (Offset = 12C0h) [Reset = 00000000h]

DOE31_0 is shown in Figure 14-41 and described in Table 14-45.

Return to the Summary Table.

This register is used to enable the data outputs for DIO31 to DIO0.

Figure 14-41. DOE31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 14-83. DOE31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R/W	0h	Enables data output for DIO31. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
30	DIO30	R/W	0h	Enables data output for DIO30. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
29	DIO29	R/W	0h	Enables data output for DIO29. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
28	DIO28	R/W	0h	Enables data output for DIO28. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
27	DIO27	R/W	0h	Enables data output for DIO27. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
26	DIO26	R/W	0h	Enables data output for DIO26. Reset type: SYSRST 0h = Output disabled 1h = Output enabled

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Table 14-83. DOE31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R/W	0h	Enables data output for DIO25. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
24	DIO24	R/W	0h	Enables data output for DIO24. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
23	DIO23	R/W	0h	Enables data output for DIO23. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
22	DIO22	R/W	0h	Enables data output for DIO22. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
21	DIO21	R/W	0h	Enables data output for DIO21. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
20	DIO20	R/W	0h	Enables data output for DIO20. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
19	DIO19	R/W	0h	Enables data output for DIO19. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
18	DIO18	R/W	0h	Enables data output for DIO18. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
17	DIO17	R/W	0h	Enables data output for DIO17. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
16	DIO16	R/W	0h	Enables data output for DIO16. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
15	DIO15	R/W	0h	Enables data output for DIO15. Reset type: SYSRST 0h = Output disabled 1h = Output enabled

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Table 14-83. DOE31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R/W	0h	Enables data output for DIO14. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
13	DIO13	R/W	0h	Enables data output for DIO13. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
12	DIO12	R/W	0h	Enables data output for DIO12. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
11	DIO11	R/W	0h	Enables data output for DIO11. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
10	DIO10	R/W	0h	Enables data output for DIO10. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
9	DIO9	R/W	0h	Enables data output for DIO9. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
8	DIO8	R/W	0h	Enables data output for DIO8. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
7	DIO7	R/W	0h	Enables data output for DIO7. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
6	DIO6	R/W	0h	Enables data output for DIO6. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
5	DIO5	R/W	0h	Enables data output for DIO5. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
4	DIO4	R/W	0h	Enables data output for DIO4. Reset type: SYSRST 0h = Output disabled 1h = Output enabled

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Table 14-83. DOE31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	R/W	0h	Enables data output for DIO3. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
2	DIO2	R/W	0h	Enables data output for DIO2. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
1	DIO1	R/W	0h	Enables data output for DIO1. Reset type: SYSRST 0h = Output disabled 1h = Output enabled
0	DIO0	R/W	0h	Enables data output for DIO0. Reset type: SYSRST 0h = Output disabled 1h = Output enabled

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39 DOESET31_0 Register (Offset = 12D0h) [Reset = 00000000h]

DOESET31_0 is shown in Figure 14-42 and described in Table 14-46.

Return to the Summary Table.

Writing 1 to a bit position in this register sets the corresponding bit in the DOE31_0 register.

Figure 14-42. DOESET31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-85. DOESET31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	Writing 1 to this bit sets the DIO31 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO31 in DOE31_0
30	DIO30	W	0h	Writing 1 to this bit sets the DIO30 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO30 in DOE31_0
29	DIO29	W	0h	Writing 1 to this bit sets the DIO29 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO29 in DOE31_0
28	DIO28	W	0h	Writing 1 to this bit sets the DIO28 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO28 in DOE31_0
27	DIO27	W	0h	Writing 1 to this bit sets the DIO27 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO27 in DOE31_0

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Table 14-85. DOESET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DIO26	W	0h	Writing 1 to this bit sets the DIO26 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO26 in DOE31_0
25	DIO25	W	0h	Writing 1 to this bit sets the DIO25 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO25 in DOE31_0
24	DIO24	W	0h	Writing 1 to this bit sets the DIO24 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO24 in DOE31_0
23	DIO23	W	0h	Writing 1 to this bit sets the DIO23 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO23 in DOE31_0
22	DIO22	W	0h	Writing 1 to this bit sets the DIO22 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO22 in DOE31_0
21	DIO21	W	0h	Writing 1 to this bit sets the DIO21 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO21 in DOE31_0
20	DIO20	W	0h	Writing 1 to this bit sets the DIO20 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO20 in DOE31_0
19	DIO19	W	0h	Writing 1 to this bit sets the DIO19 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO19 in DOE31_0
18	DIO18	W	0h	Writing 1 to this bit sets the DIO18 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO18 in DOE31_0

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Table 14-85. DOESET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIO17	W	0h	Writing 1 to this bit sets the DIO17 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO17 in DOE31_0
16	DIO16	W	0h	Writing 1 to this bit sets the DIO16 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO16 in DOE31_0
15	DIO15	W	0h	Writing 1 to this bit sets the DIO15 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO15 in DOE31_0
14	DIO14	W	0h	Writing 1 to this bit sets the DIO14 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO14 in DOE31_0
13	DIO13	W	0h	Writing 1 to this bit sets the DIO13 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO13 in DOE31_0
12	DIO12	W	0h	Writing 1 to this bit sets the DIO12 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO12 in DOE31_0
11	DIO11	W	0h	Writing 1 to this bit sets the DIO11 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO11 in DOE31_0
10	DIO10	W	0h	Writing 1 to this bit sets the DIO10 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO10 in DOE31_0
9	DIO9	W	0h	Writing 1 to this bit sets the DIO9 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO9 in DOE31_0

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Table 14-85. DOESET31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DIO8	W	0h	Writing 1 to this bit sets the DIO8 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO8 in DOE31_0
7	DIO7	W	0h	Writing 1 to this bit sets the DIO7 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO7 in DOE31_0
6	DIO6	W	0h	Writing 1 to this bit sets the DIO6 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO6 in DOE31_0
5	DIO5	W	0h	Writing 1 to this bit sets the DIO5 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO5 in DOE31_0
4	DIO4	W	0h	Writing 1 to this bit sets the DIO4 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO4 in DOE31_0
3	DIO3	W	0h	Writing 1 to this bit sets the DIO3 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO3 in DOE31_0
2	DIO2	W	0h	Writing 1 to this bit sets the DIO2 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO2 in DOE31_0
1	DIO1	W	0h	Writing 1 to this bit sets the DIO1 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO1 in DOE31_0
0	DIO0	W	0h	Writing 1 to this bit sets the DIO0 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Sets DIO0 in DOE31_0

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40 DOECLR31_0 Register (Offset = 12E0h) [Reset = 00000000h]

DOECLR31_0 is shown in Figure 14-43 and described in Table 14-47.

Return to the Summary Table.

Writing 1 to a bit position in this register clears the corresponding bit in the DOE31_0 register.

Figure 14-43. DOECLR31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 14-87. DOECLR31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	W	0h	Writing 1 to this bit clears the DIO31 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO31 in DOE31_0
30	DIO30	W	0h	Writing 1 to this bit clears the DIO30 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO30 in DOE31_0
29	DIO29	W	0h	Writing 1 to this bit clears the DIO29 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO29 in DOE31_0
28	DIO28	W	0h	Writing 1 to this bit clears the DIO28 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO28 in DOE31_0
27	DIO27	W	0h	Writing 1 to this bit clears the DIO27 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO27 in DOE31_0

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Table 14-87. DOECLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	DIO26	W	0h	Writing 1 to this bit clears the DIO26 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO26 in DOE31_0
25	DIO25	W	0h	Writing 1 to this bit clears the DIO25 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO25 in DOE31_0
24	DIO24	W	0h	Writing 1 to this bit clears the DIO24 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO24 in DOE31_0
23	DIO23	W	0h	Writing 1 to this bit clears the DIO23 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO23 in DOE31_0
22	DIO22	W	0h	Writing 1 to this bit clears the DIO22 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO22 in DOE31_0
21	DIO21	W	0h	Writing 1 to this bit clears the DIO21 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO21 in DOE31_0
20	DIO20	W	0h	Writing 1 to this bit clears the DIO20 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO20 in DOE31_0
19	DIO19	W	0h	Writing 1 to this bit clears the DIO19 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO19 in DOE31_0
18	DIO18	W	0h	Writing 1 to this bit clears the DIO18 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO18 in DOE31_0

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Table 14-87. DOECLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIO17	W	0h	Writing 1 to this bit clears the DIO17 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO17 in DOE31_0
16	DIO16	W	0h	Writing 1 to this bit clears the DIO16 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO16 in DOE31_0
15	DIO15	W	0h	Writing 1 to this bit clears the DIO15 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO15 in DOE31_0
14	DIO14	W	0h	Writing 1 to this bit clears the DIO14 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO14 in DOE31_0
13	DIO13	W	0h	Writing 1 to this bit clears the DIO13 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO13 in DOE31_0
12	DIO12	W	0h	Writing 1 to this bit clears the DIO12 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO12 in DOE31_0
11	DIO11	W	0h	Writing 1 to this bit clears the DIO11 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO11 in DOE31_0
10	DIO10	W	0h	Writing 1 to this bit clears the DIO10 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO10 in DOE31_0
9	DIO9	W	0h	Writing 1 to this bit clears the DIO9 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO9 in DOE31_0

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Table 14-87. DOECLR31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DIO8	W	0h	Writing 1 to this bit clears the DIO8 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO8 in DOE31_0
7	DIO7	W	0h	Writing 1 to this bit clears the DIO7 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO7 in DOE31_0
6	DIO6	W	0h	Writing 1 to this bit clears the DIO6 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO6 in DOE31_0
5	DIO5	W	0h	Writing 1 to this bit clears the DIO5 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO5 in DOE31_0
4	DIO4	W	0h	Writing 1 to this bit clears the DIO4 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO4 in DOE31_0
3	DIO3	W	0h	Writing 1 to this bit clears the DIO3 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO3 in DOE31_0
2	DIO2	W	0h	Writing 1 to this bit clears the DIO2 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO2 in DOE31_0
1	DIO1	W	0h	Writing 1 to this bit clears the DIO1 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO1 in DOE31_0
0	DIO0	W	0h	Writing 1 to this bit clears the DIO0 bit in the DOE31_0 register. Writing 0 has no effect. Reset type: SYSRST 0h = No effect 1h = Clears DIO0 in DOE31_0

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41 DIN3_0 Register (Offset = 1300h) [Reset = 00000000h]

DIN3_0 is shown in Figure 14-44 and described in Table 14-48.

Return to the Summary Table.

Data input from pins configured as DIO3 to DIO0. This is an alias register for byte access to bits 3 to 0 in DIN31_0 register.

Figure 14-44. DIN3_0 Register

31	30	29	28	27	26	25	24
RESERVED							DIO3
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO2
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO1
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO0
R-0h							R-0h

Table 14-89. DIN3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO3	R	0h	This bit reads the data input value of DIO3. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO2	R	0h	This bit reads the data input value of DIO2. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO1	R	0h	This bit reads the data input value of DIO1. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO0	R	0h	This bit reads the data input value of DIO0. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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42 DIN7_4 Register (Offset = 1304h) [Reset = 00000000h]

DIN7_4 is shown in Figure 14-45 and described in Table 14-49.

Return to the Summary Table.

Data input from pins configured as DIO7 to DIO4. This is an alias register for byte access to bits 7 to 4 in DIN31_0 register.

Figure 14-45. DIN7_4 Register

31	30	29	28	27	26	25	24
RESERVED							DIO7
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO6
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO5
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO4
R-0h							R-0h

Table 14-91. DIN7_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO7	R	0h	This bit reads the data input value of DIO7. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO6	R	0h	This bit reads the data input value of DIO6. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO5	R	0h	This bit reads the data input value of DIO5. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO4	R	0h	This bit reads the data input value of DIO4. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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43 DIN11_8 Register (Offset = 1308h) [Reset = 00000000h]

DIN11_8 is shown in Figure 14-46 and described in Table 14-50.

Return to the Summary Table.

Data input from pins configured as DIO11 to DIO8. This is an alias register for byte access to bits 11 to 8 in DIN31_0 register.

Figure 14-46. DIN11_8 Register

31	30	29	28	27	26	25	24
RESERVED							DIO11
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO10
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO9
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO8
R-0h							R-0h

Table 14-93. DIN11_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO11	R	0h	This bit reads the data input value of DIO11. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO10	R	0h	This bit reads the data input value of DIO10. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO9	R	0h	This bit reads the data input value of DIO9. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO8	R	0h	This bit reads the data input value of DIO8. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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44 DIN15_12 Register (Offset = 130Ch) [Reset = 00000000h]

DIN15_12 is shown in Figure 14-47 and described in Table 14-51.

Return to the Summary Table.

Data input from pins configured as DIO15 to DIO12. This is an alias register for byte access to bits 15 to 12 in DIN31_0 register.

Figure 14-47. DIN15_12 Register

31	30	29	28	27	26	25	24
RESERVED							DIO15
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO14
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO13
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO12
R-0h							R-0h

Table 14-95. DIN15_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO15	R	0h	This bit reads the data input value of DIO15. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO14	R	0h	This bit reads the data input value of DIO14. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO13	R	0h	This bit reads the data input value of DIO13. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO12	R	0h	This bit reads the data input value of DIO12. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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45 DIN19_16 Register (Offset = 1310h) [Reset = 00000000h]

DIN19_16 is shown in Figure 14-48 and described in Table 14-52.

Return to the Summary Table.

Data input from pins configured as DIO19 to DIO16. This is an alias register for byte access to bits 19 to 16 in DIN31_0 register.

Figure 14-48. DIN19_16 Register

31	30	29	28	27	26	25	24
RESERVED							DIO19
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO18
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO17
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO16
R-0h							R-0h

Table 14-97. DIN19_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO19	R	0h	This bit reads the data input value of DIO19. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO18	R	0h	This bit reads the data input value of DIO18. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO17	R	0h	This bit reads the data input value of DIO17. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO16	R	0h	This bit reads the data input value of DIO16. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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46 DIN23_20 Register (Offset = 1314h) [Reset = 00000000h]

DIN23_20 is shown in Figure 14-49 and described in Table 14-53.

Return to the Summary Table.

Data input from pins configured as DIO23 to DIO20. This is an alias register for byte access to bits 23 to 20 in DIN31_0 register.

Figure 14-49. DIN23_20 Register

31	30	29	28	27	26	25	24
RESERVED							DIO23
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO22
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO21
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO20
R-0h							R-0h

Table 14-99. DIN23_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO23	R	0h	This bit reads the data input value of DIO23. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO22	R	0h	This bit reads the data input value of DIO22. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO21	R	0h	This bit reads the data input value of DIO21. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO20	R	0h	This bit reads the data input value of DIO20. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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47 DIN27_24 Register (Offset = 1318h) [Reset = 00000000h]

DIN27_24 is shown in Figure 14-50 and described in Table 14-54.

Return to the Summary Table.

Data input from pins configured as DIO27 to DIO24. This is an alias register for byte access to bits 27 to 24 in DIN31_0 register.

Figure 14-50. DIN27_24 Register

31	30	29	28	27	26	25	24
RESERVED							DIO27
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO26
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO25
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO24
R-0h							R-0h

Table 14-101. DIN27_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO27	R	0h	This bit reads the data input value of DIO27. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO26	R	0h	This bit reads the data input value of DIO26. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO25	R	0h	This bit reads the data input value of DIO25. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO24	R	0h	This bit reads the data input value of DIO24. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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48 DIN31_28 Register (Offset = 131Ch) [Reset = 00000000h]

DIN31_28 is shown in Figure 14-51 and described in Table 14-55.

Return to the Summary Table.

Data input from pins configured as DIO31 to DIO28. This is an alias register for byte access to bits 31 to 28 in DIN31_0 register.

Figure 14-51. DIN31_28 Register

31	30	29	28	27	26	25	24
RESERVED							DIO31
R-0h							R-0h
23	22	21	20	19	18	17	16
RESERVED							DIO30
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							DIO29
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							DIO28
R-0h							R-0h

Table 14-103. DIN31_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	
24	DIO31	R	0h	This bit reads the data input value of DIO31. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23-17	RESERVED	R	0h	
16	DIO30	R	0h	This bit reads the data input value of DIO30. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15-9	RESERVED	R	0h	
8	DIO29	R	0h	This bit reads the data input value of DIO29. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7-1	RESERVED	R	0h	
0	DIO28	R	0h	This bit reads the data input value of DIO28. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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49 DIN31_0 Register (Offset = 1380h) [Reset = 00000000h]

DIN31_0 is shown in Figure 14-52 and described in Table 14-56.

Return to the Summary Table.

Data input value for pins configured as DIO31 to DIO0.

Figure 14-52. DIN31_0 Register

31	30	29	28	27	26	25	24
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14-105. DIN31_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIO31	R	0h	This bit reads the data input value of DIO31. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
30	DIO30	R	0h	This bit reads the data input value of DIO30. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
29	DIO29	R	0h	This bit reads the data input value of DIO29. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
28	DIO28	R	0h	This bit reads the data input value of DIO28. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
27	DIO27	R	0h	This bit reads the data input value of DIO27. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
26	DIO26	R	0h	This bit reads the data input value of DIO26. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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Table 14-105. DIN31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIO25	R	0h	This bit reads the data input value of DIO25. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
24	DIO24	R	0h	This bit reads the data input value of DIO24. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
23	DIO23	R	0h	This bit reads the data input value of DIO23. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
22	DIO22	R	0h	This bit reads the data input value of DIO22. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
21	DIO21	R	0h	This bit reads the data input value of DIO21. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
20	DIO20	R	0h	This bit reads the data input value of DIO20. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
19	DIO19	R	0h	This bit reads the data input value of DIO19. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
18	DIO18	R	0h	This bit reads the data input value of DIO18. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
17	DIO17	R	0h	This bit reads the data input value of DIO17. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
16	DIO16	R	0h	This bit reads the data input value of DIO16. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
15	DIO15	R	0h	This bit reads the data input value of DIO15. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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Table 14-105. DIN31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIO14	R	0h	This bit reads the data input value of DIO14. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
13	DIO13	R	0h	This bit reads the data input value of DIO13. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
12	DIO12	R	0h	This bit reads the data input value of DIO12. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
11	DIO11	R	0h	This bit reads the data input value of DIO11. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
10	DIO10	R	0h	This bit reads the data input value of DIO10. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
9	DIO9	R	0h	This bit reads the data input value of DIO9. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
8	DIO8	R	0h	This bit reads the data input value of DIO8. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
7	DIO7	R	0h	This bit reads the data input value of DIO7. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
6	DIO6	R	0h	This bit reads the data input value of DIO6. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
5	DIO5	R	0h	This bit reads the data input value of DIO5. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
4	DIO4	R	0h	This bit reads the data input value of DIO4. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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Table 14-105. DIN31_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIO3	R	0h	This bit reads the data input value of DIO3. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
2	DIO2	R	0h	This bit reads the data input value of DIO2. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
1	DIO1	R	0h	This bit reads the data input value of DIO1. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1
0	DIO0	R	0h	This bit reads the data input value of DIO0. Reset type: SYSRST 0h = Input value is 0 1h = Input value is 1

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50 POLARITY15_0 Register (Offset = 1390h) [Reset = 00000000h]

POLARITY15_0 is shown in Figure 14-53 and described in Table 14-57.

Return to the Summary Table.

This register is used to enable and configure the polarity for input edge detection on DIO15 to DIO0. The corresponding DIO bits in RIS register will be set when the input event matches the configured polarity.

Figure 14-53. POLARITY15_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIO15		DIO14		DIO13		DIO12		DIO11		DIO10		DIO9		DIO8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIO7		DIO6		DIO5		DIO4		DIO3		DIO2		DIO1		DIO0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 14-107. POLARITY15_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DIO15	R/W	0h	Enables and configures edge detection polarity for DIO15. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
29-28	DIO14	R/W	0h	Enables and configures edge detection polarity for DIO14. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
27-26	DIO13	R/W	0h	Enables and configures edge detection polarity for DIO13. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
25-24	DIO12	R/W	0h	Enables and configures edge detection polarity for DIO12. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
23-22	DIO11	R/W	0h	Enables and configures edge detection polarity for DIO11. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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Table 14-107. POLARITY15_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	DIO10	R/W	0h	Enables and configures edge detection polarity for DIO10. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
19-18	DIO9	R/W	0h	Enables and configures edge detection polarity for DIO9. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
17-16	DIO8	R/W	0h	Enables and configures edge detection polarity for DIO8. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
15-14	DIO7	R/W	0h	Enables and configures edge detection polarity for DIO7. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
13-12	DIO6	R/W	0h	Enables and configures edge detection polarity for DIO6. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
11-10	DIO5	R/W	0h	Enables and configures edge detection polarity for DIO5. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
9-8	DIO4	R/W	0h	Enables and configures edge detection polarity for DIO4. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
7-6	DIO3	R/W	0h	Enables and configures edge detection polarity for DIO3. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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Table 14-107. POLARITY15_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DIO2	R/W	0h	Enables and configures edge detection polarity for DIO2. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
3-2	DIO1	R/W	0h	Enables and configures edge detection polarity for DIO1. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
1-0	DIO0	R/W	0h	Enables and configures edge detection polarity for DIO0. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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51 POLARITY31_16 Register (Offset = 13A0h) [Reset = 00000000h]

POLARITY31_16 is shown in Figure 14-54 and described in Table 14-58.

Return to the Summary Table.

This register is used to enable and configure the polarity for input edge detection on DIO31 to DIO16. The corresponding DIO bits in RIS register will be set when the input event matches the configured polarity.

Figure 14-54. POLARITY31_16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIO31		DIO30		DIO29		DIO28		DIO27		DIO26		DIO25		DIO24	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIO23		DIO22		DIO21		DIO20		DIO19		DIO18		DIO17		DIO16	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 14-109. POLARITY31_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DIO31	R/W	0h	Enables and configures edge detection polarity for DIO31. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
29-28	DIO30	R/W	0h	Enables and configures edge detection polarity for DIO30. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
27-26	DIO29	R/W	0h	Enables and configures edge detection polarity for DIO29. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
25-24	DIO28	R/W	0h	Enables and configures edge detection polarity for DIO28. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
23-22	DIO27	R/W	0h	Enables and configures edge detection polarity for DIO27. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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Table 14-109. POLARITY31_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	DIO26	R/W	0h	Enables and configures edge detection polarity for DIO26. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
19-18	DIO25	R/W	0h	Enables and configures edge detection polarity for DIO25. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
17-16	DIO24	R/W	0h	Enables and configures edge detection polarity for DIO24. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
15-14	DIO23	R/W	0h	Enables and configures edge detection polarity for DIO23. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
13-12	DIO22	R/W	0h	Enables and configures edge detection polarity for DIO22. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
11-10	DIO21	R/W	0h	Enables and configures edge detection polarity for DIO21. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
9-8	DIO20	R/W	0h	Enables and configures edge detection polarity for DIO20. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
7-6	DIO19	R/W	0h	Enables and configures edge detection polarity for DIO19. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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Table 14-109. POLARITY31_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DIO18	R/W	0h	Enables and configures edge detection polarity for DIO18. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
3-2	DIO17	R/W	0h	Enables and configures edge detection polarity for DIO17. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event
1-0	DIO16	R/W	0h	Enables and configures edge detection polarity for DIO16. Reset type: SYSRST 0h = Edge detection disabled 1h = Detects rising edge of input event 2h = Detects falling edge of input event 3h = Detects both rising and falling edge of input event

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52 CTL Register (Offset = 1400h) [Reset = 00000000h]

CTL is shown in Figure 14-55 and described in Table 14-59.

Return to the Summary Table.

GPIO Control Register

Figure 14-55. CTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							FASTWAKEONLY
R/W-0h							R/W-0h

Table 14-111. CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	FASTWAKEONLY	R/W	0h	FASTWAKEONLY for the global control of fastwake Reset type: SYSRST 0h = The global control of fastwake is not enabled, per bit fast wake feature depends on FASTWAKE.DIN 1h = The global control of fastwake is enabled

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53 FASTWAKE Register (Offset = 1404h) [Reset = 00000000h]

FASTWAKE is shown in Figure 14-56 and described in Table 14-60.

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This is per bit fast wake enable for the bit slice, allows the GPIO module to stay in a low power state and not require high speed clocking of the input synchronizer or filter

Figure 14-56. FASTWAKE Register

31	30	29	28	27	26	25	24
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 14-113. FASTWAKE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIN31	R/W	0h	Enable fastwake feature for DIN31 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
30	DIN30	R/W	0h	Enable fastwake feature for DIN30 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
29	DIN29	R/W	0h	Enable fastwake feature for DIN29 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
28	DIN28	R/W	0h	Enable fastwake feature for DIN29 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
27	DIN27	R/W	0h	Enable fastwake feature for DIN27 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
26	DIN26	R/W	0h	Enable fastwake feature for DIN26 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled

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Table 14-113. FASTWAKE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DIN25	R/W	0h	Enable fastwake feature for DIN25 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
24	DIN24	R/W	0h	Enable fastwake feature for DIN24 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
23	DIN23	R/W	0h	Enable fastwake feature for DIN23 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
22	DIN22	R/W	0h	Enable fastwake feature for DIN22 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
21	DIN21	R/W	0h	Enable fastwake feature for DIN21 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
20	DIN20	R/W	0h	Enable fastwake feature for DIN20 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
19	DIN19	R/W	0h	Enable fastwake feature for DIN19 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
18	DIN18	R/W	0h	Enable fastwake feature for DIN18 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
17	DIN17	R/W	0h	Enable fastwake feature for DIN17 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
16	DIN16	R/W	0h	Enable fastwake feature for DIN16 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
15	DIN15	R/W	0h	Enable fastwake feature for DIN15 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled

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Table 14-113. FASTWAKE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DIN14	R/W	0h	Enable fastwake feature for DIN14 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
13	DIN13	R/W	0h	Enable fastwake feature for DIN13 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
12	DIN12	R/W	0h	Enable fastwake feature for DIN12 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
11	DIN11	R/W	0h	Enable fastwake feature for DIN11 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
10	DIN10	R/W	0h	Enable fastwake feature for DIN10 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
9	DIN9	R/W	0h	Enable fastwake feature for DIN9 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
8	DIN8	R/W	0h	Enable fastwake feature for DIN8 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
7	DIN7	R/W	0h	Enable fastwake feature for DIN7 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
6	DIN6	R/W	0h	Enable fastwake feature for DIN6 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
5	DIN5	R/W	0h	Enable fastwake feature for DIN5 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
4	DIN4	R/W	0h	Enable fastwake feature for DIN4 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled

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Table 14-113. FASTWAKE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DIN3	R/W	0h	Enable fastwake feature for DIN3 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
2	DIN2	R/W	0h	Enable fastwake feature for DIN2 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
1	DIN1	R/W	0h	Enable fastwake feature for DIN1 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled
0	DIN0	R/W	0h	Enable fastwake feature for DIN0 Reset type: SYSRST 0h = fastwake feature is disabled 1h = fastwake feature is enabled

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54 SUB0CFG Register (Offset = 1500h) [Reset = 00000000h]

SUB0CFG is shown in Figure 14-57 and described in Table 14-61.

Return to the Summary Table.

This register is used to enable the subscriber 0 event and define the output policy on the selected DIO 0-15 pins.

Figure 14-57. SUB0CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						RESERVED	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-0h							R/W-0h

Table 14-115. SUB0CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	RESERVED	R/W	0h	Reserved
15-10	RESERVED	R/W	0h	
9-8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	0h	
0	RESERVED	R/W	0h	Reserved

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55 FILTEREN15_0 Register (Offset = 1508h) [Reset = 00000000h]

FILTEREN15_0 is shown in Figure 14-58 and described in Table 14-62.

Return to the Summary Table.

Programmable counter length of digital glitch filter for DIN0~15

Figure 14-58. FILTEREN15_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIN15		DIN14		DIN13		DIN12		DIN11		DIN10		DIN9		DIN8	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN7		DIN6		DIN5		DIN4		DIN3		DIN2		DIN1		DIN0	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 14-117. FILTEREN15_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DIN15	R/W	0h	Programmable counter length of digital glitch filter for DIN15 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
29-28	DIN14	R/W	0h	Programmable counter length of digital glitch filter for DIN14 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
27-26	DIN13	R/W	0h	Programmable counter length of digital glitch filter for DIN13 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
25-24	DIN12	R/W	0h	Programmable counter length of digital glitch filter for DIN12 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
23-22	DIN11	R/W	0h	Programmable counter length of digital glitch filter for DIN11 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
21-20	DIN10	R/W	0h	Programmable counter length of digital glitch filter for DIN10 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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Table 14-117. FILTEREN15_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-18	DIN9	R/W	0h	Programmable counter length of digital glitch filter for DIN9 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
17-16	DIN8	R/W	0h	Programmable counter length of digital glitch filter for DIN8 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
15-14	DIN7	R/W	0h	Programmable counter length of digital glitch filter for DIN7 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
13-12	DIN6	R/W	0h	Programmable counter length of digital glitch filter for DIN6 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
11-10	DIN5	R/W	0h	Programmable counter length of digital glitch filter for DIN5 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
9-8	DIN4	R/W	0h	Programmable counter length of digital glitch filter for DIN4 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
7-6	DIN3	R/W	0h	Programmable counter length of digital glitch filter for DIN3 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
5-4	DIN2	R/W	0h	Programmable counter length of digital glitch filter for DIN2 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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Table 14-117. FILTEREN15_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	DIN1	R/W	0h	Programmable counter length of digital glitch filter for DIN1 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
1-0	DIN0	R/W	0h	Programmable counter length of digital glitch filter for DIN0 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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56 FILTEREN31_16 Register (Offset = 150Ch) [Reset = 00000000h]

FILTEREN31_16 is shown in Figure 14-59 and described in Table 14-63.

Return to the Summary Table.

Programmable counter length of digital glitch filter for DIN16~31

Figure 14-59. FILTEREN31_16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIN31		DIN30		DIN29		DIN28		DIN27		DIN26		DIN25		DIN24	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN23		DIN22		DIN21		DIN20		DIN19		DIN18		DIN17		DIN16	
R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 14-119. FILTEREN31_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DIN31	R/W	0h	Programmable counter length of digital glitch filter for DIN31 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
29-28	DIN30	R/W	0h	Programmable counter length of digital glitch filter for DIN30 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
27-26	DIN29	R/W	0h	Programmable counter length of digital glitch filter for DIN29 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
25-24	DIN28	R/W	0h	Programmable counter length of digital glitch filter for DIN28 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
23-22	DIN27	R/W	0h	Programmable counter length of digital glitch filter for DIN27 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
21-20	DIN26	R/W	0h	Programmable counter length of digital glitch filter for DIN26 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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Table 14-119. FILTEREN31_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-18	DIN25	R/W	0h	Programmable counter length of digital glitch filter for DIN25 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
17-16	DIN24	R/W	0h	Programmable counter length of digital glitch filter for DIN24 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
15-14	DIN23	R/W	0h	Programmable counter length of digital glitch filter for DIN23 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
13-12	DIN22	R/W	0h	Programmable counter length of digital glitch filter for DIN22 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
11-10	DIN21	R/W	0h	Programmable counter length of digital glitch filter for DIN21 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
9-8	DIN20	R/W	0h	Programmable counter length of digital glitch filter for DIN20 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
7-6	DIN19	R/W	0h	Programmable counter length of digital glitch filter for DIN19 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
5-4	DIN18	R/W	0h	Programmable counter length of digital glitch filter for DIN18 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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Table 14-119. FILTEREN31_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	DIN17	R/W	0h	Programmable counter length of digital glitch filter for DIN17 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample
1-0	DIN16	R/W	0h	Programmable counter length of digital glitch filter for DIN16 Reset type: SYSRST 0h = No additional filter beyond the CDC synchronization sample 1h = 1 ULPCLK minimum sample 2h = 3 ULPCLK minimum sample 3h = 8 ULPCLK minimum sample

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57 SUB1CFG Register (Offset = 1520h) [Reset = 00000000h]

SUB1CFG is shown in Figure 14-60 and described in Table 14-64.

Return to the Summary Table.

This register is used to enable the subscriber 1 event and define the output policy on the selected DIO 16-31 pins.

Figure 14-60. SUB1CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						RESERVED	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-0h							R/W-0h

Table 14-121. SUB1CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	RESERVED	R/W	0h	Reserved
15-10	RESERVED	R/W	0h	
9-8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	0h	
0	RESERVED	R/W	0h	Reserved

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Chapter 15

Global Security Controller (GSC)

The Global Security Controller (GSC) peripheral is a system module that can configure the security firewalls for privileged and non-privileged context information to access on-chip memory and peripherals. After configuration, the GSC detects out of context transactions to the Flash, SRAM and peripherals, and generates interrupts when the privileged context is violated.

15.1 GSC Introduction 708
15.2 GSC Operation 708
15.3 GSC Registers 717

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15.1 GSC Introduction

The Global Security Controller (GSC) configures the privilege attribute for resources on the device. The GSC consists of multiple blocks that verifies the device's access properties are observed the same by all bus initiators. In essence, the GSC provides firewall access based on the priviliege property of the application code and initiators.

15.1.1 GSC Features

- Configures privileged and unprivileged attribute for memory and peripherals
- Write and erase protection for the Flash
- Direct monitoring of initiator access to memory and peripherals to generate interrupts for context violations
- Logs violation information in the EAM for the initiator and the destination address
- Hide protection control for the Flash in 2 KB sector size granularity

15.2 GSC Operation

The GSC comprises of three important sub-blocks: the Peripheral Protection Controller (PPC), the SRAM Protection Controller (SPC) and the Flash Protection Controller (FPC). A block diagram of the GSC is shown in *GSC Functional Block Diagram*.

15.2.1 Functional Block Diagram

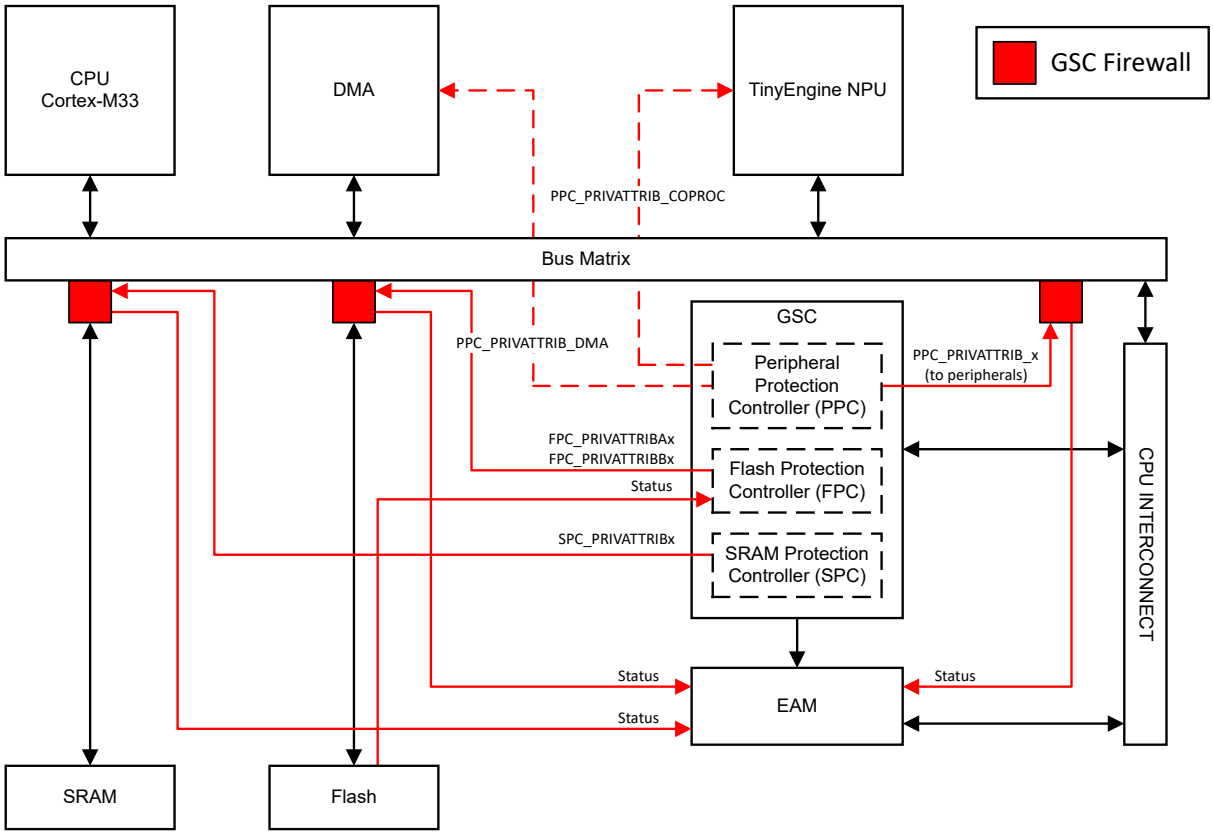


Figure 15-1. GSC Functional Block Diagram

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15.2.2 Peripheral Protection Controller

The Peripheral Protection Controller (PPC) configures the firewall for peripheral access. The PPC_PRIVATTRIB_x register for a given peripheral configures the firewall for privilege or non-privilege access. Please refer to Table 15-1 for the peripheral to PPC_PRIVATTRIB register mapping.

Table 15-1. PPC Priviliged Attribute Register Mapping

Peripheral	PPC Register
ADC	PPC_PRIVATTRIB_ADC
PWM, ECAP, EQEP, TIMG4, TIMG12	PPC_PRIVATTRIB_TIMER
UNICOMM	PPC_PRIVATTRIB_UNICOMM
GPIO	PPC_PRIVATTRIB_GPIO
MCAN	PPC_PRIVATTRIB_MCAN
CMPSS	PPC_PRIVATTRIB_CMPSS
WWDT	PPC_PRIVATTRIB_WDT
CRC	PPC_PRIVATTRIB_CRC
AES	PPC_PRIVATTRIB_AES
IOMUX	PPC_PRIVATTRIB_IOMUX
DEBUGSS	PPC_PRIVATTRIB_DEBUGSS
KEYSTORECTL	PPC_PRIVATTRIB_KEYSTORECTL
EAM	PPC_PRIVATTRIB_EAM
FLASH	PPC_PRIVATTRIB_FRIREGS
MEMCFG	PPC_PRIVATTRIB_MEMCFG
SYSCTL	PPC_PRIVATTRIB_SYSCTL
SDFM	PPC_PRIVATTRIB_SDFM
ETHERCAT	PPC_PRIVATTRIB_ETHERCAT
FSI	PPC_PRIVATTRIB_FSI
DMA	PPC_PRIVATTRIB_DMA
GSC	PPC_PRIVATTRIB_GSC
TINIE NPU	PPC_PRIVATTRIB_COPROC
PGA	PPC_PRIVATTRIB_PGA
XBAR	PPC_PRIVATTRIB_XBAR

Note

The CPU thread privilege mode is configured by the CONTROL register. Please refer to Section 4.2.2 for more details.

When a peripheral is configured as a privileged peripheral then only an initiator which is operating in the privileged context can access the peripheral configuration, status or data registers. Any initiator access not in the privilege context will generate a Non-Maskable Interrupt (NMI) that is logged in the EAM module.

In addition to generating a NMI, any write access that shall be ignored and a read access shall return all zeroes to the corresponding initiator. This prevents unpriviliged code or initiator from accessing or modifying data in the peripheral space at run time.

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Certain peripheral firewall are configured with the privilege attribute enabled (CRC, DEBUGSS, SYSCTL, DMA, and GSC). This allows the application code to leverage a default privileged setting of the device to implement bootloaders or authentication code.

15.2.2.1 DMA Security

The DMA is uniquely handled within the GSC framework as it is both an initiator and target. When the DMA privilege attribute is configured (PPC.PPC_PRIVATTRIB_DMA), then both the initiator and the target port for configuration/status are set to privileged.

The power-on reset value for the DMA is always privileged. Only the CPU in privileged mode can configure the DMA0 control and channel registers. Once configured, all write and read access generated by DMA0 initiator ports appear as privileged to the source and destination peripherals/memories. This ensures that after the device is powered on and the CPU begins code execution, the DMA0 is in a privileged context for moving data between peripherals and memory and does not require any additional configuration.

Note

The GSC is also privileged at power-on reset. Any non-privileged application code cannot directly modify the DMA property. This must be handled within privileged application code.

15.2.2.2 TinyEngine NPU Security

The TinyEngine NPU is also handled differently within the GSC framework as it is both an initiator and target. When the NPU's privilege attribute is configured (PPC_PRIVATTRIB_COPROC.PRIV_TINIE), then both the initiator and the target port are set to privileged.

Once configured, all transactions generated by NPU's initiator ports appear as privileged to the SRAM. Only the CPU in privileged mode can configure the NPU.

15.2.3 SRAM Protection Controller

The SRAM Protection Controller (SPC) configures the firewall for the SRAM and monitors the transactions from the initiators. Any violation of the security property set for the SRAM results in a NMI being triggered and the violation logged in the EAM. Similar to the PPC sub-block, the SPC provides the SPC_PRIVATTRIB[x] register to configure the firewall for privilege or non-privilege access.

To manage the SRAM firewall efficiently, the SRAM is partitioned into 16 KB pages. Each SPC_PRIVATTRIB[x] register controls four 16 KB pages. Further granularity is provided by partitioning each page into variable-sized chunks. These chunks are represented within the page control field of the SPC_PRIVATTRIB[x] register in sets of 8-bits as shown in Figure 15-2.

As mentioned above, each page is comprised of seven chunks of variable size. As a result, out of the 8-bits available for a page, only 7-bits are used with the most significant bit being reserved. The chunks in a SRAM page are comprised of the following sizes:

- 3 chunks of 4 KB
- 1 chunk of 2 KB
- 1 chunk of 1 KB
- 2 chunks of 512 B

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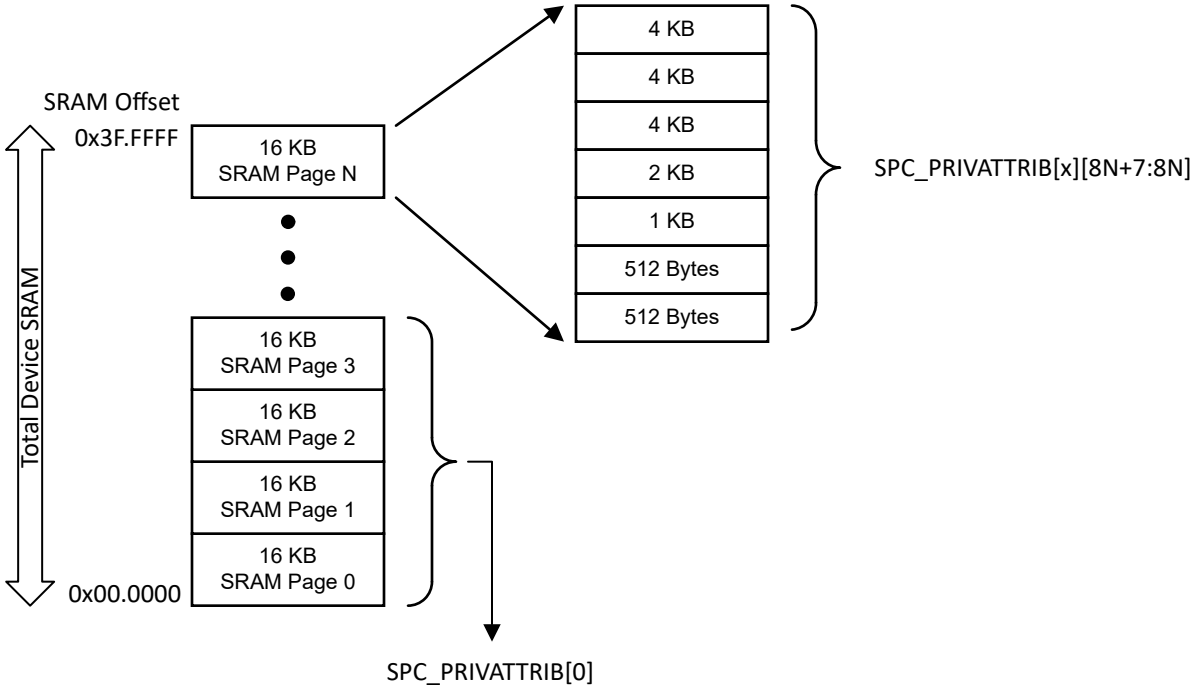


Figure 15-2. SRAM Page and Chunk Mapping

15.2.3.1 SRAM Page Use Model

Each chunk within a 16 KB SRAM page can be configured independently with the privilege attributes to maxmize SRAM usage for different security aspects of the application code.

For example, in Figure 15-3, each chunk within the 16 KB SRAM page is provisioned such that:

- 9 KB of SRAM can be accessed by a unprivileged initiator
- 7 KB of SRAM can be accessed by a privileged initiator

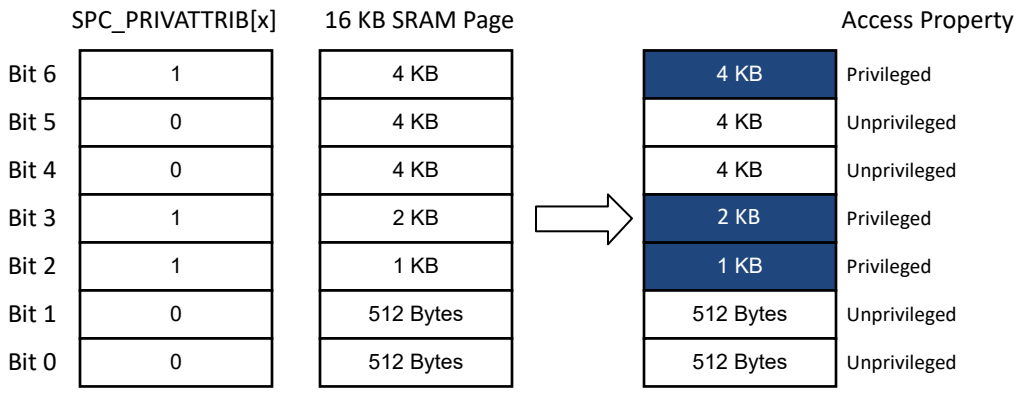


Figure 15-3. SRAM Page Use Example

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The SPC allows that privileged regions within the SRAM do not need to be continguous. Additionally, by default the SPC is configurable by a privileged initiator, which allows the privileged context to dynamically allocate memory properties. This is useful when SRAM has to be allocated for a critical application code from a common memory pool.

Note

Before changing the SRAM chunk memory property, it is the privileged applications responsibility to ensure that all initiators are properly configured and any data in SRAM is zero initialized.

15.2.4 Flash Protection Controller

The Flash Protection Controller (FPC) configures the firewall for the program and data flash, and monitors the transactions from the initiators. Any violation of the security property set for the flash results in a NMI being triggered and the violation logged in the EAM.

Similar to the PPC and SPC sub-blocks, the FPC provides the flash privilege access firewall registers FPC_PRIVATTRIBA[x] for the first 32 sectors of each main flash bank and FPC_PRIVATTRIBB[x] for the remaining sectors in each flash bank.

In addition, the FPC provides flash write/erase protection registers FPC_WEPROTA[x] and FPC_WEPROTB[x]. The FPC_WEPROTA[x] register provides write/erase protection for the first 32 sectors in each of the MAIN flash bank at 2 KB sector size. The FPC_WEPROTB[x] register provides write/erase protection for remaining flash sectors with each bit mapping to 8 sectors of 2 KB size (for a total of 16 KB size).

Note

Given AM13E232x devices can have up to two main flash banks available, security property registers with the suffix '0' control flash bank 0 and suffix '1' control flash bank 1. For example, FPC_WEPROTA0 controls bank 0 and FPC_WEPROTA1 controls bank 1.

To manage the flash firewalls efficiently, the FPC uses the sector information for each flash bank. Each flash bank consists of multiple 2 KB flash sectors. An illustration for 512 KB flash on AM13E232x devices is shown in Figure 15-4.

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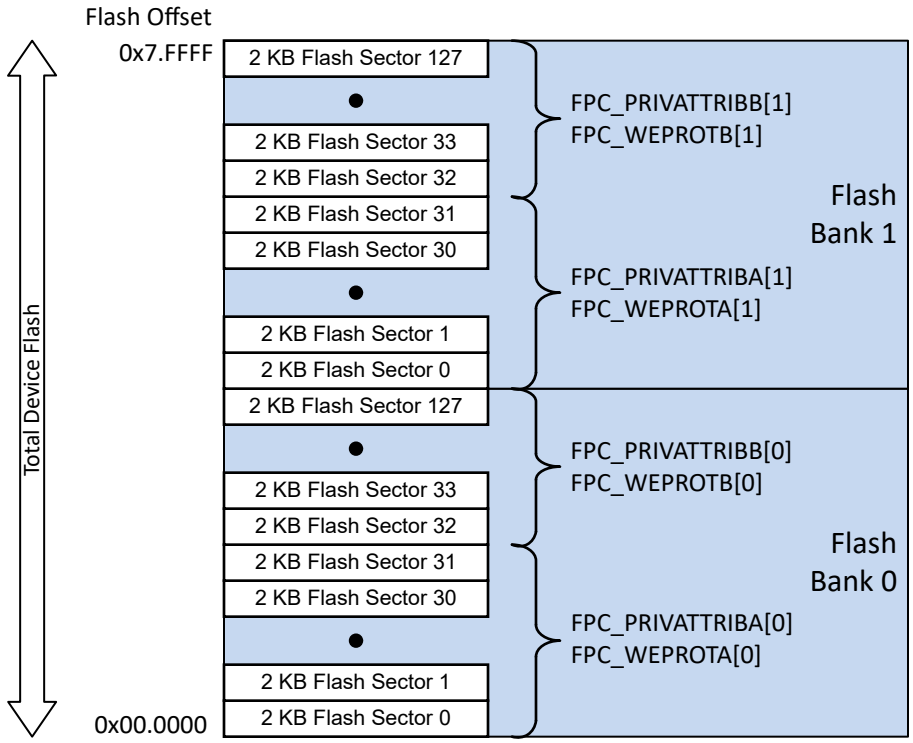


Figure 15-4. Flash Sector Mapping

15.2.4.1 Flash Bank Security Implementation

As mentioned earlier, the firewall control for the flash banks is at a 2KB sector level. To maintain maximum flexibility and reasonable ease of use, each privilege attribute register configures firewalls slightly differently:

- **FPC_PRIVATTRIBA[x], FPC_WEPROTA[x]**: Each bit is mapped to individual 2KB sector, starting at sector 0 up to sector 31. All 32-bits of the register are used for the mapping with bit 0 mapped to sector 0 and bit 31 mapped to sector 31.
- **FPC_PRIVATTRIBB[x], FPC_WEPROTB[x]**: Each bit is mapped to a set of eight sectors (total of 16 KB), starting at sector 32 up to sector 127.
  - With a 512 KB flash size, there are 96 sectors left after removing the first 32 sectors from each flash bank, so these registers use 12 bits. The first 4-bits of these registers are reserved. Bit 4 is mapped to sectors 32 to 39 and bit 15 is mapped to sector 120 to sector 127.

Note

The "x" in the above register names must be replaced by "0" for flash bank 0 and "1" for flash bank 1, for the dual-bank configuration on AM13E232x devices.

The Table 15-2 shows some example of the register mapping for 1 MB flash.

Table 15-2. FPC Firewall Register Decoding for 512 KB Flash

Flash Privilege Access Register	Flash Write-Erase Protect Register	Flash Sector (2KB)
FPC_PRIVATTRIBAx[0]	FPC_WEPROTAx[0]	0
FPC_PRIVATTRIBAx[1]	FPC_WEPROTAx[1]	1
FPC_PRIVATTRIBAx[2]	FPC_WEPROTAx[2]	2
FPC_PRIVATTRIBAx[3]	FPC_WEPROTAx[3]	3

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Table 15-2. FPC Firewall Register Decoding for 512 KB Flash (continued)

Flash Privilege Access Register	Flash Write-Erase Protect Register	Flash Sector (2KB)
FPC_PRIVATTRIBAx[4]	FPC_WEPROTAx[4]	4
FPC_PRIVATTRIBAx[5]	FPC_WEPROTAx[5]	5
FPC_PRIVATTRIBAx[6]	FPC_WEPROTAx[6]	6
FPC_PRIVATTRIBAx[7]	FPC_WEPROTAx[7]	7
FPC_PRIVATTRIBAx[8]	FPC_WEPROTAx[8]	8
FPC_PRIVATTRIBAx[9]	FPC_WEPROTAx[9]	9
FPC_PRIVATTRIBAx[10]	FPC_WEPROTAx[10]	10
FPC_PRIVATTRIBAx[11]	FPC_WEPROTAx[11]	11
FPC_PRIVATTRIBAx[12]	FPC_WEPROTAx[12]	12
FPC_PRIVATTRIBAx[13]	FPC_WEPROTAx[13]	13
FPC_PRIVATTRIBAx[14]	FPC_WEPROTAx[14]	14
FPC_PRIVATTRIBAx[15]	FPC_WEPROTAx[15]	15
FPC_PRIVATTRIBAx[16]	FPC_WEPROTAx[16]	16
FPC_PRIVATTRIBAx[17]	FPC_WEPROTAx[17]	17
FPC_PRIVATTRIBAx[18]	FPC_WEPROTAx[18]	18
FPC_PRIVATTRIBAx[19]	FPC_WEPROTAx[19]	19
FPC_PRIVATTRIBAx[20]	FPC_WEPROTAx[20]	20
FPC_PRIVATTRIBAx[21]	FPC_WEPROTAx[21]	21
FPC_PRIVATTRIBAx[22]	FPC_WEPROTAx[22]	22
FPC_PRIVATTRIBAx[23]	FPC_WEPROTAx[23]	23
FPC_PRIVATTRIBAx[24]	FPC_WEPROTAx[24]	24
FPC_PRIVATTRIBAx[25]	FPC_WEPROTAx[25]	25
FPC_PRIVATTRIBAx[26]	FPC_WEPROTAx[26]	26
FPC_PRIVATTRIBAx[27]	FPC_WEPROTAx[27]	27
FPC_PRIVATTRIBAx[28]	FPC_WEPROTAx[28]	28
FPC_PRIVATTRIBAx[29]	FPC_WEPROTAx[29]	29
FPC_PRIVATTRIBAx[30]	FPC_WEPROTAx[30]	30
FPC_PRIVATTRIBAx[31]	FPC_WEPROTAx[31]	31
FPC_PRIVATTRIBBx[4]	FPC_WEPROTBx[4]	32 - 39
FPC_PRIVATTRIBBx[5]	FPC_WEPROTBx[5]	40 - 47
FPC_PRIVATTRIBBx[6]	FPC_WEPROTBx[6]	48 - 55
FPC_PRIVATTRIBBx[7]	FPC_WEPROTBx[7]	56 - 63
FPC_PRIVATTRIBBx[8]	FPC_WEPROTBx[8]	64 - 71
FPC_PRIVATTRIBBx[9]	FPC_WEPROTBx[9]	72 - 79
FPC_PRIVATTRIBBx[10]	FPC_WEPROTBx[10]	80 - 87
FPC_PRIVATTRIBBx[11]	FPC_WEPROTBx[11]	88 - 95
FPC_PRIVATTRIBBx[12]	FPC_WEPROTBx[12]	96 - 103

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Table 15-2. FPC Firewall Register Decoding for 512 KB Flash (continued)

Flash Privilege Access Register	Flash Write-Erase Protect Register	Flash Sector (2KB)
FPC_PRIVATTRIBBx[13]	FPC_WEPROTBx[13]	104 - 111
FPC_PRIVATTRIBBx[14]	FPC_WEPROTBx[14]	112 - 119
FPC_PRIVATTRIBBx[15]	FPC_WEPROTBx[15]	120 - 127

15.2.4.2 Flash Hide Protection

The FPC is also responsible for managing the Hide Protection (HDP) function. The HDP function allows an application to execute a section of code one time, and prevent subsequent read or execute access to the code. As an example, this is useful feature especially when running a second stage authentication code allowing main application to be validated before execution and prevent access to any stored symmetric or private keys.

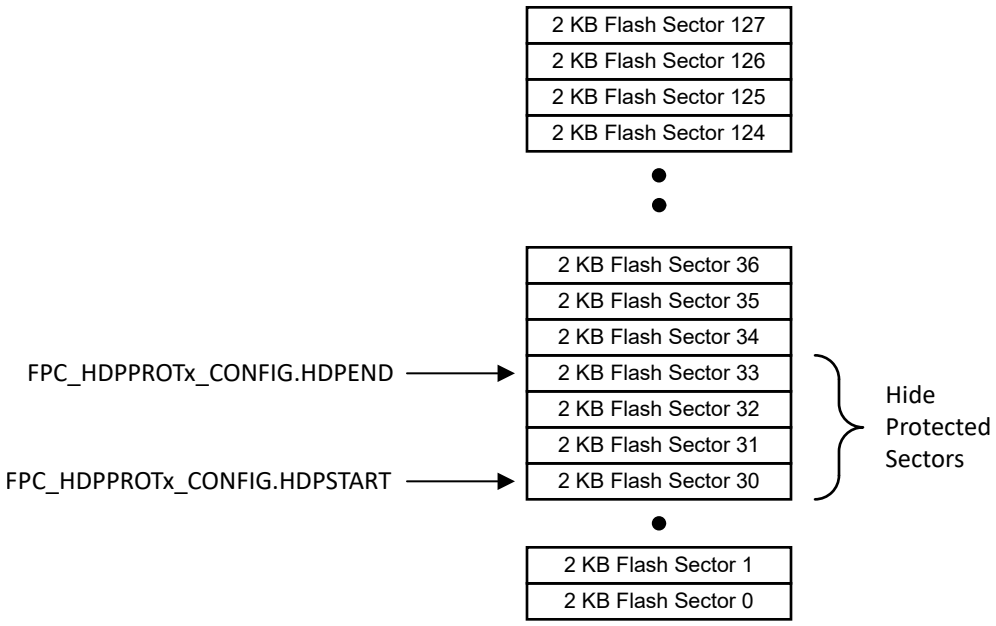


Figure 15-5. Flash Hide Protection Memory View

As shown in Figure 15-5, the HDPSTART and HDPEND fields in the FPC_HDPPROTx_CONFIG register define the start and end sector address which are to be hide protected.

Note

The "x" in the FPC_HDPPROTx_CONFIG must be replace by "0" for flash bank 0 and "1" for flash bank 1, for the dual-bank configuration on AM13E232x devices. In other words, there is an independent hide protection configuration register corresponding to each flash bank.

The Table 15-3 shows the valid configuration of values that define the sectors that can be hide protected.

Table 15-3. HDPSTART and HDPEND Rule

RULE	COMMENT
HDPSTART = HDPEND	Hide protection for exactly 1 sector identified by HDPSTART
HDPSTART < HDPEND	Hide protection for sectors from HDPSTART to HDPEND (inclusive)

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Table 15-3. HDPSTART and HDPEND Rule (continued)

RULE	COMMENT
HDPSTART > HDPEND	Invalid configuration defined, no hide protection

In addition to start and end sector address for HDP, there are two additional registers. The FPC_HDPPROT_CONTROL is used to validate the corresponding configuration register to be active. The FPC_HDPEN_CONTROL is to trigger the mechanism for hide protection. As shown in Figure 15-6, once the start sector, end sector and valid control bits are configured correctly, the HDP is ready. When CPU executes the HDP region code, the HDP is armed. Any function call or jump outside of the HDP automatically enables the mechanism, preventing the application code from re-entering the HDP region. An access, execute or read, generates an NMI.

Note

When executing code in HDP region followed by branch to SRAM, the SRAM code can access HDP region. Once all SRAM code execution is completed, the SRAM code must branch back and exit the HDP region to continue execution in flash (out of the HDP region) for the HDP mechanism to enable. If application does not want SRAM to access HDP region, then the code must implement a trampoline function to enable HDP before branching to SRAM code.

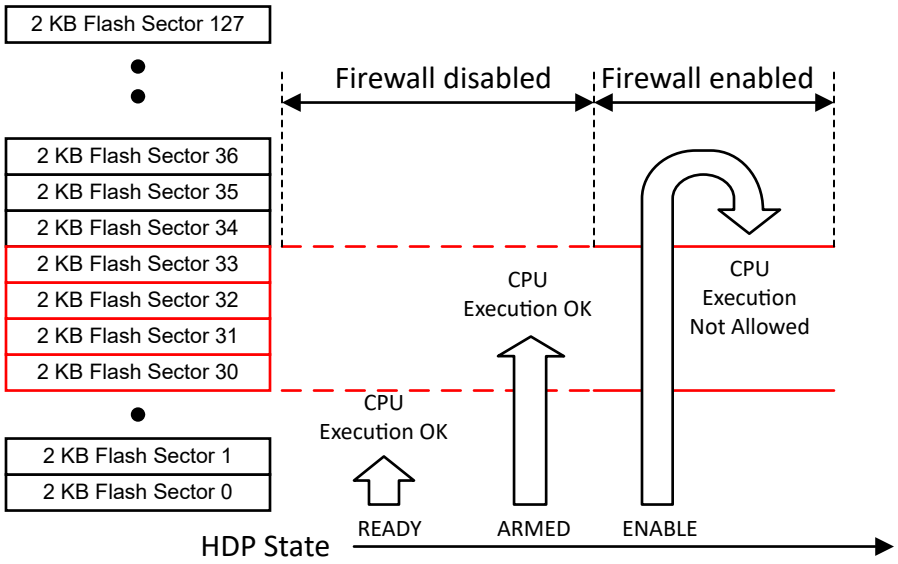


Figure 15-6. HDP Execution Flow

All the HDP registers are writeable once and can be set by the application code. A system reset does not allow the application to re-configure, therefore a BOOTRST is required.

15.2.5 Strict Privilege Context Protection

The firewall configurations in GSC prevents unprivileged initiators from accessing privileged peripherals and memory. However, an privileged initiator could still access unprivileged peripherals and memory. The attribute violation configuration registers (xPC_ATTRIBVIOL_CONFIG) for PPC, SPC and FPC can be configured to prevent the latter case.

Table 15-4. Privilege Attribute Violation Configuration Registers

Sub-Module	Attribute Violation Configuration Registers
PPC	PPC_ATTRIBVIOLP_CONFIG

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Table 15-4. Privilege Attribute Violation Configuration Registers (continued)

Sub-Module	Attribute Violation Configuration Registers
SPC	SPC_ATTRIBVIOLP_CONFIG
FPC	FPC_ATTRIBVIOLP_CONFIG

These registers are typically used when an application wants to avoid memory overflow or accidental peripheral access outside of the context. As shown in Table 15-5, on a violating access, the GSC generates a NMI for the CPU. A violating write has no effect and a read will return all zero.

Table 15-5. Attribute Violation Rule Table

xPC_ATTRIBVIOL_CONFIG	Bus Transaction	Privileged Target	Unprivileged Target
PRIVVIOL = 0	Privileged Initiator	Allowed	Allowed
	Unprivileged Initator	NMI	Allowed
PRIVVIOL = 1	Privileged Initiator	Allowed	NMI
	Unprivileged Initator	NMI	Allowed

Note

Careful design of the application (with an NMI handler) must be taken to avoid a lock-up scenario.

15.2.6 GSC Configuration Lock

The GSC also has the capability of locking and committing the security setting on a per region basis using the GSC_LOCK register. There are total of 6 regions which can be individually locked or committed.

- Attribute Violation Configuration
- PPC Attribute
- SPC Attribute
- FPC Attribute
- Vector Table Offset Register (VTOR)
- DMA trigger selection

When locked, the corresponding register in the region cannot be modified. To update a region register, the KEY of 0xA551 has to be written along with the modified register bit to unlock the register.

When commit control is applied using the GSC_COMMIT register, then the GSC_LOCK register cannot be updated even if the correct KEY is used. The only mechanism to update a commit is with a BOOTRST, before the application can make changes.

15.3 GSC Registers

This Section describes the GSC Registers.

15.3.1 GSC Base Address Table

Table 15-6. GSC Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
GscRegs	GSC_REGS	GSC	0x4004_6000

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15.3.2 GSC_LITE_REGS Registers

Table 15-7 lists the memory-mapped registers for the GSC_LITE_REGS registers. All register offset addresses not listed in Table 15-7 should be considered as reserved locations and the register contents should not be modified.

Table 15-7. GSC_LITE_REGS Registers

Offset	Acronym	Register Name	Group	Section
1004h	SPC_ATTRIBVIOLP_CONFIG	SRAM Privilege Access Attribute Violation Configuration Register		Go
1014h	PPC_ATTRIBVIOLP_CONFIG	Peripheral Privilege Access Attribute Violation Configuration Register		Go
1024h	FPC_ATTRIBVIOLP_CONFIG	Flash Privilege Access Attribute Violation Configuration Register		Go
1040h	FPC_HDPPROT0_CONFIG	Flash Hide Protection for Bank0 Configuration Register		Go
1044h	FPC_HDPPROT1_CONFIG	Flash Hide Protection for Bank1 Configuration Register		Go
104Ch	FPC_HDPPROT_CONTROL	Flash Hide Protection Control Register		Go
1050h	FPC_HDPEN_CONTROL	Flash Hide Protection Enable Control Register		Go
1104h	PPC_PRIVATTRIB_ADC	Peripheral Privilege Access ADC		Go
110Ch	PPC_PRIVATTRIB_TIMER	Peripheral Privilege Access Timer		Go
1114h	PPC_PRIVATTRIB_UNICOMM	Peripheral Privilege Access UniComm		Go
111Ch	PPC_PRIVATTRIB_GPIO	Peripheral Privilege Access GPIO		Go
1124h	PPC_PRIVATTRIB_MCAN	Peripheral Privilege Access CAN		Go
1134h	PPC_PRIVATTRIB_CMPSS	Peripheral Privilege Access CMPSS		Go
113Ch	PPC_PRIVATTRIB_WDT	Peripheral Privilege Access Watchdog		Go
114Ch	PPC_PRIVATTRIB_CRC	Peripheral Privilege Access CRC		Go
1154h	PPC_PRIVATTRIB_AES	Peripheral Privilege Access AES		Go
116Ch	PPC_PRIVATTRIB_IOMUX	Peripheral Privilege Access IOMUX		Go
1184h	PPC_PRIVATTRIB_DEBUGSS	Peripheral Privilege Access DEBUGSS		Go
1194h	PPC_PRIVATTRIB_KEYSTORECTL	Peripheral Privilege Access KEYSTORECTL		Go
119Ch	PPC_PRIVATTRIB_EAM	Peripheral Privilege Access EAM		Go
11ACh	PPC_PRIVATTRIB_FRIREGS	Peripheral Privilege Access FRIREGS		Go
11B4h	PPC_PRIVATTRIB_MEMCFG	Peripheral Privilege Access MEMCFG		Go
120Ch	PPC_PRIVATTRIB_SYSCTL	Peripheral Privilege Access System Control		Go
1214h	PPC_PRIVATTRIB_DMA	Peripheral Privilege Access DMA		Go
121Ch	PPC_PRIVATTRIB_GSC	Peripheral Privilege Access GSC		Go
1224h	PPC_PRIVATTRIB_COPROC	Peripheral Privilege Access Co-processor		Go
1234h	PPC_PRIVATTRIB_PGA	Peripheral Privilege Access PGA		Go
123Ch	PPC_PRIVATTRIB_XBAR	Peripheral Privilege Access XBAR		Go
1244h	PPC_PRIVATTRIB_ETHERCAT	Peripheral Privilege Access ETHERCAT		Go
124Ch	PPC_PRIVATTRIB_FSI	Peripheral Privilege Access FSI		Go
1254h	PPC_PRIVATTRIB_SDFM	Peripheral Privilege Access SDFM		Go
12C0h	SPC_PRIVATTRIB0	SRAM Privilege Attribute-0 Register		Go
12C4h	SPC_PRIVATTRIB1	SRAM Privilege Attribute-1 Register		Go
12C8h	SPC_PRIVATTRIB2	SRAM Privilege Attribute-2 Register		Go
1400h	FPC_PRIVATTRIBA0	Flash Privilege Attribute Register A0		Go
1404h	FPC_PRIVATTRIBA1	Flash Privilege Attribute Register A1		Go
1408h	FPC_PRIVATTRIBB0	Flash Privilege Attribute Register B0		Go

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Table 15-7. GSC_LITE_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
140Ch	FPC_PRIVATTRIBB1	Flash Privilege Attribute Register B1		Go
1600h	FPC_WEPROTA0	Flash Write Protect Attribute Register A0		Go
1604h	FPC_WEPROTA1	Flash Write Protect Attribute Register A1		Go
1608h	FPC_WEPROTB0	Flash Write Protect Attribute Register B0		Go
160Ch	FPC_WEPROTB1	Flash Write Protect Attribute Register B1		Go
1800h	FPC_FLSEMREQ	Flash semaphore request register		Go
1804h	FPC_FLSEMCLR	Flash semaphore release register		Go
1808h	FPC_FLSEMSTAT	Flash semaphore statys registers		Go
1B84h	VTOR_NS	Non - Secure Vector Table Offset Register		Go
1D80h	GSC_LOCK	GSC Lock configuration register		Go
1D84h	GSC_COMMIT	GSC commit configuration register		Go
1FFCh	GSC_REVISION	GSC Revision register		Go

Complex bit access types are encoded to fit into small table cells. Table 15-8 shows the codes that are used for access types in this section.

Table 15-8. GSC_LITE_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WOnce	W Once	Write Write once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 SPC_ATTRIBVIOLP_CONFIG Register (Offset = 1004h) [Reset = 00000000h]

SPC_ATTRIBVIOLP_CONFIG is shown in Figure 15-7 and described in Table 15-9.

Return to the Summary Table.

SRAM Privilege Access Attribute Violation Configuration Register

Figure 15-7. SPC_ATTRIBVIOLP_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIVVIOL
R-0h							R/W-0h

Table 15-10. SPC_ATTRIBVIOLP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIVVIOL	R/W	0h	Controls the behavior of privilege access to non-privilege SRAM 0: Access is allowed 1: Access generates bus-fault and NMI Reset type: XRSn

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2 PPC_ATTRIBVIOLP_CONFIG Register (Offset = 1014h) [Reset = 00000000h]

PPC_ATTRIBVIOLP_CONFIG is shown in Figure 15-8 and described in Table 15-10.

Return to the Summary Table.

Peripheral Privilege Access Attribute Violation Configuration Register

Figure 15-8. PPC_ATTRIBVIOLP_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIVVIOL
R-0h							R/W-0h

Table 15-12. PPC_ATTRIBVIOLP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIVVIOL	R/W	0h	Controls the behavior of privilege access to non-privilege peripherals 0: Access is allowed 1: Access generates bus-fault and NMI Reset type: XRSn

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3 FPC_ATTRIBVIOLP_CONFIG Register (Offset = 1024h) [Reset = 00000000h]

FPC_ATTRIBVIOLP_CONFIG is shown in Figure 15-9 and described in Table 15-11.

Return to the Summary Table.

Flash Privilege Access Attribute Violation Configuration Register

Figure 15-9. FPC_ATTRIBVIOLP_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIVVIOL
R-0h							R/W-0h

Table 15-14. FPC_ATTRIBVIOLP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIVVIOL	R/W	0h	Controls the behavior of privilege access to non-privilege Flash 0: Access is allowed 1: Access generates bus-fault and NMI Reset type: XRSn

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4 FPC_HDPPROT0_CONFIG Register (Offset = 1040h) [Reset = 00FF0000h]

FPC_HDPPROT0_CONFIG is shown in Figure 15-10 and described in Table 15-12.

Return to the Summary Table.

Flash Hide Protection for Bank0 Configuration Register

Figure 15-10. FPC_HDPPROT0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HDPSTART								RESERVED								HDPEND							
R-0h								WOnce-FFh								R-0h								WOnce-0h							

Table 15-16. FPC_HDPPROT0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	HDPSTART	WOnce	FFh	Sector number where hide protection starts Reset type: Rsn
15-8	RESERVED	R	0h	Reserved
7-0	HDPEND	WOnce	0h	Sector number where hide protection ends Reset type: Rsn

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5 FPC_HDPPROT1_CONFIG Register (Offset = 1044h) [Reset = 00FF0000h]

FPC_HDPPROT1_CONFIG is shown in Figure 15-11 and described in Table 15-13.

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Flash Hide Protection for Bank1 Configuration Register

Figure 15-11. FPC_HDPPROT1_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								HDPSTART								RESERVED								HDPEND							
R-0h								WOnce-FFh								R-0h								WOnce-0h							

Table 15-18. FPC_HDPPROT1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	HDPSTART	WOnce	FFh	Sector number where hide protection starts Reset type: Rsn
15-8	RESERVED	R	0h	Reserved
7-0	HDPEND	WOnce	0h	Sector number where hide protection ends Reset type: Rsn

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6 FPC_HDPPROT_CONTROL Register (Offset = 104Ch) [Reset = 00000000h]

FPC_HDPPROT_CONTROL is shown in Figure 15-12 and described in Table 15-14.

Return to the Summary Table.

Flash Hide Protection Control Register

Figure 15-12. FPC_HDPPROT_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						HDPPROT1ACCDIS	HDPPROT0ACCDIS
R-0h						R/W1S-0h	R/W1S-0h

Table 15-20. FPC_HDPPROT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	HDPPROT1ACCDIS	R/W1S	0h	Enables the FPC_HDPPROT1_CONFIG to take effect. 0: HDP region access is enabled 1: HDP region access is disabled Reset type: Rsn
0	HDPPROT0ACCDIS	R/W1S	0h	Enables the FPC_HDPPROT0_CONFIG to take effect. 0: HDP region access is enabled 1: HDP region access is disabled Reset type: Rsn

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7 FPC_HDPEN_CONTROL Register (Offset = 1050h) [Reset = 00000000h]

FPC_HDPEN_CONTROL is shown in Figure 15-13 and described in Table 15-15.

Return to the Summary Table.

Flash Hide Protection Enable Control Register

Figure 15-13. FPC_HDPEN_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HDPEN
R-0h							R/W1S-0h

Table 15-22. FPC_HDPEN_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HDPEN	R/W1S	0h	HDP mode enable. This bit is set in the OTP during provisioning. 0: HDP mode is not used 1: HDP mode is enabled Reset type: Rsn

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8 PPC_PRIVATTRIB_ADC Register (Offset = 1104h) [Reset = 00000000h]

PPC_PRIVATTRIB_ADC is shown in Figure 15-14 and described in Table 15-16.

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Peripheral Privilege Access ADC

Figure 15-14. PPC_PRIVATTRIB_ADC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PRIV_ADC2	PRIV_ADC1	PRIV_ADC0
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 15-24. PPC_PRIVATTRIB_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	PRIV_ADC2	R/W	0h	Privilege access enabled to ADC2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_ADC1	R/W	0h	Privilege access enabled to ADC1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_ADC0	R/W	0h	Privilege access enabled to ADC0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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9 PPC_PRIVATTRIB_TIMER Register (Offset = 110Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_TIMER is shown in Figure 15-15 and described in Table 15-17.

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Peripheral Privilege Access Timer

Figure 15-15. PPC_PRIVATTRIB_TIMER Register

31	30	29	28	27	26	25	24
PRIV_EPWM5	PRIV_EPWM4	PRIV_EPWM3	PRIV_EPWM2	PRIV_EPWM1	PRIV_EPWM0	PRIV_TIMG12_0	PRIV_TIMG4_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PRIV_OTTOCAL	RESERVED					PRIV_EQEP1	PRIV_EQEP0
R/W-0h	R-0h					R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED					PRIV_ECAP2	PRIV_ECAP1	PRIV_ECAP0
R-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PRIV_MCPWM2	PRIV_MCPWM1	PRIV_MCPWM0
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 15-26. PPC_PRIVATTRIB_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV_EPWM5	R/W	0h	Privilege access enabled to EPWM5 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
30	PRIV_EPWM4	R/W	0h	Privilege access enabled to EPWM4 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
29	PRIV_EPWM3	R/W	0h	Privilege access enabled to EPWM3 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
28	PRIV_EPWM2	R/W	0h	Privilege access enabled to EPWM2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
27	PRIV_EPWM1	R/W	0h	Privilege access enabled to EPWM1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
26	PRIV_EPWM0	R/W	0h	Privilege access enabled to EPWM0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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Table 15-26. PPC_PRIVATTRIB_TIMER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	PRIV_TIMG12_0	R/W	0h	Privilege access enabled to TIMG12_0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
24	PRIV_TIMG4_0	R/W	0h	Privilege access enabled to TIMG4_0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
23	PRIV_OTTOCAL	R/W	0h	Privilege access enabled to OTTOCAL 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
22-18	RESERVED	R	0h	Reserved
17	PRIV_EQEP1	R/W	0h	Privilege access enabled to EQEP1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
16	PRIV_EQEP0	R/W	0h	Privilege access enabled to EQEP0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
15-11	RESERVED	R	0h	Reserved
10	PRIV_ECAP2	R/W	0h	Privilege access enabled to ECAP2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
9	PRIV_ECAP1	R/W	0h	Privilege access enabled to ECAP1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
8	PRIV_ECAP0	R/W	0h	Privilege access enabled to ECAP0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
7-3	RESERVED	R	0h	Reserved
2	PRIV_MCPWM2	R/W	0h	Privilege access enabled to MCPWM2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_MCPWM1	R/W	0h	Privilege access enabled to MCPWM1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_MCPWM0	R/W	0h	Privilege access enabled to MCPWM0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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10 PPC_PRIVATTRIB_UNICOMM Register (Offset = 1114h) [Reset = 00000000h]

PPC_PRIVATTRIB_UNICOMM is shown in Figure 15-16 and described in Table 15-18.

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Peripheral Privilege Access UniComm

Figure 15-16. PPC_PRIVATTRIB_UNICOMM Register

31	30	29	28	27	26	25	24
RESERVED						PRIV_S1_COMMON	PRIV_S0_COMMON
R-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		PRIV_S1U5	PRIV_S1U4	PRIV_S1U3	PRIV_S0U2	PRIV_S0U1	PRIV_S0U0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 15-28. PPC_PRIVATTRIB_UNICOMM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	PRIV_S1_COMMON	R/W	0h	Privilege access enabled to UniComm S1 common region 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
24	PRIV_S0_COMMON	R/W	0h	Privilege access enabled to UniComm S0 common region 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
23-6	RESERVED	R	0h	Reserved
5	PRIV_S1U5	R/W	0h	Privilege access enabled to UniComm S1U5 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
4	PRIV_S1U4	R/W	0h	Privilege access enabled to UniComm S1U4 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
3	PRIV_S1U3	R/W	0h	Privilege access enabled to UniComm S1U3 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
2	PRIV_S0U2	R/W	0h	Privilege access enabled to UniComm S0U2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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Table 15-28. PPC_PRIVATTRIB_UNICOMM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRIV_S0U1	R/W	0h	Privilege access enabled to UniComm S0U1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_S0U0	R/W	0h	Privilege access enabled to UniComm S0U0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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11 PPC_PRIVATTRIB_GPIO Register (Offset = 111Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_GPIO is shown in Figure 15-17 and described in Table 15-19.

Return to the Summary Table.

Peripheral Privilege Access GPIO

Figure 15-17. PPC_PRIVATTRIB_GPIO Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PRIV_GPIO3	PRIV_GPIO2	PRIV_GPIO1	PRIV_GPIO0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 15-30. PPC_PRIVATTRIB_GPIO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PRIV_GPIO3	R/W	0h	Privilege access enabled to GPIO3 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
2	PRIV_GPIO2	R/W	0h	Privilege access enabled to GPIO2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_GPIO1	R/W	0h	Privilege access enabled to GPIO1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_GPIO0	R/W	0h	Privilege access enabled to GPIO0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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12 PPC_PRIVATTRIB_MCAN Register (Offset = 1124h) [Reset = 00000000h]

PPC_PRIVATTRIB_MCAN is shown in Figure 15-18 and described in Table 15-20.

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Peripheral Privilege Access CAN

Figure 15-18. PPC_PRIVATTRIB_MCAN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PRIV_MCAN1	PRIV_MCAN0
R-0h						R/W-0h	R/W-0h

Table 15-32. PPC_PRIVATTRIB_MCAN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	PRIV_MCAN1	R/W	0h	Privilege access enabled to MCAN1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_MCAN0	R/W	0h	Privilege access enabled to MCAN0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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13 PPC_PRIVATTRIB_CMPSS Register (Offset = 1134h) [Reset = 00000000h]

PPC_PRIVATTRIB_CMPSS is shown in Figure 15-19 and described in Table 15-21.

Return to the Summary Table.

Peripheral Privilege Access CMPSS

Figure 15-19. PPC_PRIVATTRIB_CMPSS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PRIV_CMPSS3	PRIV_CMPSS2	PRIV_CMPSS1	PRIV_CMPSS0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 15-34. PPC_PRIVATTRIB_CMPSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PRIV_CMPSS3	R/W	0h	Privilege access enabled to CMPSS3 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
2	PRIV_CMPSS2	R/W	0h	Privilege access enabled to CMPSS2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_CMPSS1	R/W	0h	Privilege access enabled to CMPSS1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_CMPSS0	R/W	0h	Privilege access enabled to CMPSS0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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14 PPC_PRIVATTRIB_WDT Register (Offset = 113Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_WDT is shown in Figure 15-20 and described in Table 15-22.

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Peripheral Privilege Access Watchdog

Figure 15-20. PPC_PRIVATTRIB_WDT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_WWDT
R-0h							R/W-0h

Table 15-36. PPC_PRIVATTRIB_WDT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_WWDT	R/W	0h	Privilege access enabled to Windowed Watchdog 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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15 PPC_PRIVATTRIB_CRC Register (Offset = 114Ch) [Reset = 00000001h]

PPC_PRIVATTRIB_CRC is shown in Figure 15-21 and described in Table 15-23.

Return to the Summary Table.

Peripheral Privilege Access CRC

Figure 15-21. PPC_PRIVATTRIB_CRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_CRC
R-0h							R/W-1h

Table 15-38. PPC_PRIVATTRIB_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_CRC	R/W	1h	Privilege access enabled to CRC 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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16 PPC_PRIVATTRIB_AES Register (Offset = 1154h) [Reset = 00000000h]

PPC_PRIVATTRIB_AES is shown in Figure 15-22 and described in Table 15-24.

Return to the Summary Table.

Peripheral Privilege Access AES

Figure 15-22. PPC_PRIVATTRIB_AES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_AES
R-0h							R/W-0h

Table 15-40. PPC_PRIVATTRIB_AES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_AES	R/W	0h	Privilege access enabled to AES 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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17 PPC_PRIVATTRIB_IOMUX Register (Offset = 116Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_IOMUX is shown in Figure 15-23 and described in Table 15-25.

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Peripheral Privilege Access IOMUX

Figure 15-23. PPC_PRIVATTRIB_IOMUX Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_IOMUX
R-0h							R/W-0h

Table 15-42. PPC_PRIVATTRIB_IOMUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_IOMUX	R/W	0h	Privilege access enabled to IOMUX 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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18 PPC_PRIVATTRIB_DEBUGSS Register (Offset = 1184h) [Reset = 00000001h]

PPC_PRIVATTRIB_DEBUGSS is shown in Figure 15-24 and described in Table 15-26.

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Peripheral Privilege Access DEBUGSS

Figure 15-24. PPC_PRIVATTRIB_DEBUGSS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_DEBUGSS
R-0h							R/W-1h

Table 15-44. PPC_PRIVATTRIB_DEBUGSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_DEBUGSS	R/W	1h	Privilege access enabled to DEBUGSS 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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19 PPC_PRIVATTRIB_KEYSTORECTL Register (Offset = 1194h) [Reset = 00000000h]

PPC_PRIVATTRIB_KEYSTORECTL is shown in Figure 15-25 and described in Table 15-27.

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Peripheral Privilege Access KEYSTORECTL

Figure 15-25. PPC_PRIVATTRIB_KEYSTORECTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_KEYSTORECTL
R-0h							R/W-0h

Table 15-46. PPC_PRIVATTRIB_KEYSTORECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_KEYSTORECTL	R/W	0h	Privilege access enabled to KEYSTORECTL 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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20 PPC_PRIVATTRIB_EAM Register (Offset = 119Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_EAM is shown in Figure 15-26 and described in Table 15-28.

Return to the Summary Table.

Peripheral Privilege Access EAM

Figure 15-26. PPC_PRIVATTRIB_EAM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_EAM
R-0h							R/W-0h

Table 15-48. PPC_PRIVATTRIB_EAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_EAM	R/W	0h	Privilege access enabled to EAM 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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21 PPC_PRIVATTRIB_FRIREGS Register (Offset = 11ACh) [Reset = 00000000h]

PPC_PRIVATTRIB_FRIREGS is shown in Figure 15-27 and described in Table 15-29.

Return to the Summary Table.

Peripheral Privilege Access FRIREGS

Figure 15-27. PPC_PRIVATTRIB_FRIREGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_FRIREGS
R-0h							R/W-0h

Table 15-50. PPC_PRIVATTRIB_FRIREGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_FRIREGS	R/W	0h	Privilege access enabled to FRIREGS 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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22 PPC_PRIVATTRIB_MEMCFG Register (Offset = 11B4h) [Reset = 00000000h]

PPC_PRIVATTRIB_MEMCFG is shown in Figure 15-28 and described in Table 15-30.

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Peripheral Privilege Access MEMCFG

Figure 15-28. PPC_PRIVATTRIB_MEMCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_MEMCFG
R-0h							R/W-0h

Table 15-52. PPC_PRIVATTRIB_MEMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_MEMCFG	R/W	0h	Privilege access enabled to MEMCFG 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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23 PPC_PRIVATTRIB_SYSCTL Register (Offset = 120Ch) [Reset = 00000001h]

PPC_PRIVATTRIB_SYSCTL is shown in Figure 15-29 and described in Table 15-31.

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Peripheral Privilege Access System Control

Figure 15-29. PPC_PRIVATTRIB_SYSCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_SYSCTL
R-0h							R/W-1h

Table 15-54. PPC_PRIVATTRIB_SYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_SYSCTL	R/W	1h	Privilege access enabled to SYSCTL 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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24 PPC_PRIVATTRIB_DMA Register (Offset = 1214h) [Reset = 00000001h]

PPC_PRIVATTRIB_DMA is shown in Figure 15-30 and described in Table 15-32.

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Peripheral Privilege Access DMA

Figure 15-30. PPC_PRIVATTRIB_DMA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_DMA
R-0h							R/W-1h

Table 15-56. PPC_PRIVATTRIB_DMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_DMA	R/W	1h	Privilege access enabled to DMA 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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25 PPC_PRIVATTRIB_GSC Register (Offset = 121Ch) [Reset = 00000001h]

PPC_PRIVATTRIB_GSC is shown in Figure 15-31 and described in Table 15-33.

Return to the Summary Table.

Peripheral Privilege Access GSC

Figure 15-31. PPC_PRIVATTRIB_GSC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_GSC
R-0h							R/W-1h

Table 15-58. PPC_PRIVATTRIB_GSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_GSC	R/W	1h	Privilege access enabled to GSC 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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26 PPC_PRIVATTRIB_COPROC Register (Offset = 1224h) [Reset = 00000000h]

PPC_PRIVATTRIB_COPROC is shown in Figure 15-32 and described in Table 15-34.

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Peripheral Privilege Access Co-processor

Figure 15-32. PPC_PRIVATTRIB_COPROC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_TINIE
R-0h							R/W-0h

Table 15-60. PPC_PRIVATTRIB_COPROC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_TINIE	R/W	0h	Privilege access enabled to TINIE 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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27 PPC_PRIVATTRIB_PGA Register (Offset = 1234h) [Reset = 00000000h]

PPC_PRIVATTRIB_PGA is shown in Figure 15-33 and described in Table 15-35.

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Peripheral Privilege Access PGA

Figure 15-33. PPC_PRIVATTRIB_PGA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PRIV_PGA2	PRIV_PGA1	PRIV_PGA0
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 15-62. PPC_PRIVATTRIB_PGA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	PRIV_PGA2	R/W	0h	Privilege access enabled to PGA2 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_PGA1	R/W	0h	Privilege access enabled to PGA1 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_PGA0	R/W	0h	Privilege access enabled to PGA0 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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28 PPC_PRIVATTRIB_XBAR Register (Offset = 123Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_XBAR is shown in Figure 15-34 and described in Table 15-36.

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Peripheral Privilege Access XBAR

Figure 15-34. PPC_PRIVATTRIB_XBAR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PRIV_OUTPUT_XBAR_FLAGS	PRIV_XBAR_INPUT_FLAGS	PRIV_ALL_XBAR_CONFIG
R-0h					R/W-0h	R/W-0h	R/W-0h

Table 15-64. PPC_PRIVATTRIB_XBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	PRIV_OUTPUT_XBAR_FLAGS	R/W	0h	Privilege access enabled to OUTPUT_XBAR_FLAGS 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
1	PRIV_XBAR_INPUT_FLAGS	R/W	0h	Privilege access enabled to XBAR_INPUT_FLAGS 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_ALL_XBAR_CONFIG	R/W	0h	Privilege access enabled to ALL_XBAR_CONFIG including SYNC_SOC_REGS 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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29 PPC_PRIVATTRIB_ETHERCAT Register (Offset = 1244h) [Reset = 00000000h]

PPC_PRIVATTRIB_ETHERCAT is shown in Figure 15-35 and described in Table 15-37.

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Peripheral Privilege Access ETHERCAT

Figure 15-35. PPC_PRIVATTRIB_ETHERCAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_ETHERCAT
R-0h							R/W-0h

Table 15-66. PPC_PRIVATTRIB_ETHERCAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_ETHERCAT	R/W	0h	Privilege access enabled to ETHERCAT (all apertures) 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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30 PPC_PRIVATTRIB_FSI Register (Offset = 124Ch) [Reset = 00000000h]

PPC_PRIVATTRIB_FSI is shown in Figure 15-36 and described in Table 15-38.

Return to the Summary Table.

Peripheral Privilege Access FSI

Figure 15-36. PPC_PRIVATTRIB_FSI Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PRIV_FSI_RX	PRIV_FSI_TX
R-0h						R/W-0h	R/W-0h

Table 15-68. PPC_PRIVATTRIB_FSI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	PRIV_FSI_RX	R/W	0h	Privilege access enabled to FSI_RX 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn
0	PRIV_FSI_TX	R/W	0h	Privilege access enabled to FSI_TX 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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31 PPC_PRIVATTRIB_SDFM Register (Offset = 1254h) [Reset = 00000000h]

PPC_PRIVATTRIB_SDFM is shown in Figure 15-37 and described in Table 15-39.

Return to the Summary Table.

Peripheral Privilege Access SDFM

Figure 15-37. PPC_PRIVATTRIB_SDFM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PRIV_SDFM
R-0h							R/W-0h

Table 15-70. PPC_PRIVATTRIB_SDFM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PRIV_SDFM	R/W	0h	Privilege access enabled to SDFM 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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32 SPC_PRIVATTRIB0 Register (Offset = 12C0h) [Reset = 7F7F7F7Fh]

SPC_PRIVATTRIB0 is shown in Figure 15-38 and described in Table 15-40.

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Controls first 64 KB range of device SRAM

Figure 15-38. SPC_PRIVATTRIB0 Register

31	30	29	28	27	26	25	24
RESERVED	C3B2_4KB	C3B1_4KB	C3B0_4KB	C3B0_2KB	C3B0_1KB	C3B1_512B	C3B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RESERVED	C2B2_4KB	C2B1_4KB	C2B0_4KB	C2B0_2KB	C2B0_1KB	C2B1_512B	C2B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	C1B2_4KB	C1B1_4KB	C1B0_4KB	C1B0_2KB	C1B0_1KB	C1B1_512B	C1B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED	C0B2_4KB	C0B1_4KB	C0B0_4KB	C0B0_2KB	C0B0_1KB	C0B1_512B	C0B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 15-72. SPC_PRIVATTRIB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	C3B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
29	C3B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
28	C3B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
27	C3B0_2KB	R/W	1h	privilege access enabled to 2KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
26	C3B0_1KB	R/W	1h	privilege access enabled to 1KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
25	C3B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-72. SPC_PRIVATTRIB0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	C3B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
23	RESERVED	R	0h	Reserved
22	C2B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
21	C2B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
20	C2B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
19	C2B0_2KB	R/W	1h	privilege access enabled to 2KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
18	C2B0_1KB	R/W	1h	privilege access enabled to 1KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
17	C2B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
16	C2B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
15	RESERVED	R	0h	Reserved
14	C1B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
13	C1B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
12	C1B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-72. SPC_PRIVATTRIB0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	C1B0_2KB	R/W	1h	privilege access enabled to 2KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
10	C1B0_1KB	R/W	1h	privilege access enabled to 1KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
9	C1B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
8	C1B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
7	RESERVED	R	0h	Reserved
6	C0B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
5	C0B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
4	C0B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
3	C0B0_2KB	R/W	1h	privilege access enabled to 2KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
2	C0B0_1KB	R/W	1h	privilege access enabled to 1KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
1	C0B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
0	C0B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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33 SPC_PRIVATTRIB1 Register (Offset = 12C4h) [Reset = 7F7F7F7Fh]

SPC_PRIVATTRIB1 is shown in Figure 15-39 and described in Table 15-41.

Return to the Summary Table.

Controls second 64 KB range of device SRAM

Figure 15-39. SPC_PRIVATTRIB1 Register

31	30	29	28	27	26	25	24
RESERVED	C3B2_4KB	C3B1_4KB	C3B0_4KB	C3B0_2KB	C3B0_1KB	C3B1_512B	C3B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RESERVED	C2B2_4KB	C2B1_4KB	C2B0_4KB	C2B0_2KB	C2B0_1KB	C2B1_512B	C2B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	C1B2_4KB	C1B1_4KB	C1B0_4KB	C1B0_2KB	C1B0_1KB	C1B1_512B	C1B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED	C0B2_4KB	C0B1_4KB	C0B0_4KB	C0B0_2KB	C0B0_1KB	C0B1_512B	C0B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 15-74. SPC_PRIVATTRIB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	C3B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
29	C3B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
28	C3B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
27	C3B0_2KB	R/W	1h	privilege access enabled to 2KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
26	C3B0_1KB	R/W	1h	privilege access enabled to 1KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
25	C3B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-74. SPC_PRIVATTRIB1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	C3B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
23	RESERVED	R	0h	Reserved
22	C2B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
21	C2B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
20	C2B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
19	C2B0_2KB	R/W	1h	privilege access enabled to 2KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
18	C2B0_1KB	R/W	1h	privilege access enabled to 1KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
17	C2B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
16	C2B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
15	RESERVED	R	0h	Reserved
14	C1B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
13	C1B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
12	C1B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-74. SPC_PRIVATTRIB1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	C1B0_2KB	R/W	1h	privilege access enabled to 2KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
10	C1B0_1KB	R/W	1h	privilege access enabled to 1KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
9	C1B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
8	C1B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
7	RESERVED	R	0h	Reserved
6	C0B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
5	C0B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
4	C0B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
3	C0B0_2KB	R/W	1h	privilege access enabled to 2KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
2	C0B0_1KB	R/W	1h	privilege access enabled to 1KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
1	C0B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
0	C0B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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34 SPC_PRIVATTRIB2 Register (Offset = 12C8h) [Reset = 7F7F7F7Fh]

SPC_PRIVATTRIB2 is shown in Figure 15-40 and described in Table 15-42.

Return to the Summary Table.

Controls third 64 KB range of device SRAM

Figure 15-40. SPC_PRIVATTRIB2 Register

31	30	29	28	27	26	25	24
RESERVED	C3B2_4KB	C3B1_4KB	C3B0_4KB	C3B0_2KB	C3B0_1KB	C3B1_512B	C3B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RESERVED	C2B2_4KB	C2B1_4KB	C2B0_4KB	C2B0_2KB	C2B0_1KB	C2B1_512B	C2B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED	C1B2_4KB	C1B1_4KB	C1B0_4KB	C1B0_2KB	C1B0_1KB	C1B1_512B	C1B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED	C0B2_4KB	C0B1_4KB	C0B0_4KB	C0B0_2KB	C0B0_1KB	C0B1_512B	C0B0_512B
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 15-76. SPC_PRIVATTRIB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	C3B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
29	C3B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
28	C3B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
27	C3B0_2KB	R/W	1h	privilege access enabled to 2KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
26	C3B0_1KB	R/W	1h	privilege access enabled to 1KB in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
25	C3B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-76. SPC_PRIVATTRIB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	C3B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-3 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
23	RESERVED	R	0h	Reserved
22	C2B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
21	C2B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
20	C2B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
19	C2B0_2KB	R/W	1h	privilege access enabled to 2KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
18	C2B0_1KB	R/W	1h	privilege access enabled to 1KB in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
17	C2B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
16	C2B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-2 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
15	RESERVED	R	0h	Reserved
14	C1B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
13	C1B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
12	C1B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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Table 15-76. SPC_PRIVATTRIB2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	C1B0_2KB	R/W	1h	privilege access enabled to 2KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
10	C1B0_1KB	R/W	1h	privilege access enabled to 1KB in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
9	C1B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
8	C1B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-1 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
7	RESERVED	R	0h	Reserved
6	C0B2_4KB	R/W	1h	privilege access enabled to 3rd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
5	C0B1_4KB	R/W	1h	privilege access enabled to 2nd 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
4	C0B0_4KB	R/W	1h	privilege access enabled to 1st 4KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
3	C0B0_2KB	R/W	1h	privilege access enabled to 2KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
2	C0B0_1KB	R/W	1h	privilege access enabled to 1KB in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
1	C0B1_512B	R/W	1h	privilege access enabled to 2nd 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
0	C0B0_512B	R/W	1h	privilege access enabled to 1st 512 byte in page-0 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn

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35 FPC_PRIVATTRIBA0 Register (Offset = 1400h) [Reset = FFFFFFFFh]

FPC_PRIVATTRIBA0 is shown in Figure 15-41 and described in Table 15-43.

Return to the Summary Table.

Flash Privilege Attribute Register A0

Figure 15-41. FPC_PRIVATTRIBA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIV_PAGE																															
R/W-FFFFFFFFh																															

Table 15-78. FPC_PRIVATTRIBA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRIV_PAGE	R/W	FFFFFFFFh	Privilege access enable for first 32 sectors of flash with each bit representing 1 sector of 2KB 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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36 FPC_PRIVATTRIBA1 Register (Offset = 1404h) [Reset = FFFFFFFFh]

FPC_PRIVATTRIBA1 is shown in Figure 15-42 and described in Table 15-44.

Return to the Summary Table.

Flash Privilege Attribute Register A1

Figure 15-42. FPC_PRIVATTRIBA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIV_PAGE																															
R/W-FFFFFFFFh																															

Table 15-80. FPC_PRIVATTRIBA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRIV_PAGE	R/W	FFFFFFFFh	Privilege access enable for first 32 sectors of flash with each bit representing 1 sector of 2KB 0: Non-Privilege access is enabled 1: Privilege access is enabled Reset type: XRSn

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37 FPC_PRIVATTRIBB0 Register (Offset = 1408h) [Reset = 0000FFF0h]

FPC_PRIVATTRIBB0 is shown in Figure 15-43 and described in Table 15-45.

Return to the Summary Table.

Flash Privilege Attribute Register B0

Figure 15-43. FPC_PRIVATTRIBB0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIV_PAGE												RESERVED			
R/W-FFFh												R-0h			

Table 15-82. FPC_PRIVATTRIBB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	PRIV_PAGE	R/W	FFFh	Privilege access enable for 64KB-256KB flash with each bit representing 8 sectors of 2KB 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
3-0	RESERVED	R	0h	Reserved

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38 FPC_PRIVATTRIBB1 Register (Offset = 140Ch) [Reset = 0000FFF0h]

FPC_PRIVATTRIBB1 is shown in Figure 15-44 and described in Table 15-46.

Return to the Summary Table.

Flash Privilege Attribute Register B1

Figure 15-44. FPC_PRIVATTRIBB1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIV_PAGE												RESERVED			
R/W-FFFh												R-0h			

Table 15-84. FPC_PRIVATTRIBB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	PRIV_PAGE	R/W	FFFh	Privilege access enable for 64KB-256KB flash with each bit representing 8 sectors of 2KB 0: Non-privilege access is enabled 1: privilege access is enabled Reset type: XRSn
3-0	RESERVED	R	0h	Reserved

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39 FPC_WEPROTA0 Register (Offset = 1600h) [Reset = 00000000h]

FPC_WEPROTA0 is shown in Figure 15-45 and described in Table 15-47.

Return to the Summary Table.

Flash Write Protect Attribute Register A0

Figure 15-45. FPC_WEPROTA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEPROT_PAGE																															
R/W1S-0h																															

Table 15-86. FPC_WEPROTA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WEPROT_PAGE	R/W1S	0h	Write protection enable for first 32 sectors of flash with each bit representing 1 sector of 2KB 0: Page is not erase/program protected 1: Page is erase/program protected Reset type: XRSn

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40 FPC_WEPROTA1 Register (Offset = 1604h) [Reset = 00000000h]

FPC_WEPROTA1 is shown in Figure 15-46 and described in Table 15-48.

Return to the Summary Table.

Flash Write Protect Attribute Register A1

Figure 15-46. FPC_WEPROTA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEPROT_PAGE																															
R/W1S-0h																															

Table 15-88. FPC_WEPROTA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WEPROT_PAGE	R/W1S	0h	Write protection enable for first 32 sectors of flash with each bit representing 1 sector of 2KB 0: Page is not erase/program protected 1: Page is erase/program protected Reset type: XRSn

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41 FPC_WEPROTB0 Register (Offset = 1608h) [Reset = 00000000h]

FPC_WEPROTB0 is shown in Figure 15-47 and described in Table 15-49.

Return to the Summary Table.

Flash Write Protect Attribute Register B0

Figure 15-47. FPC_WEPROTB0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEPROT_PAGE												RESERVED			
R/W1S-0h												R-0h			

Table 15-90. FPC_WEPROTB0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	WEPROT_PAGE	R/W1S	0h	Write Protection enable for 64KB-256KB flash with each bit representing 8 sectors of 2KB 0: Page is not erase/program protected 1: Page is erase/program protected Reset type: XRSn
3-0	RESERVED	R	0h	Reserved

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42 FPC_WEPROTB1 Register (Offset = 160Ch) [Reset = 00000000h]

FPC_WEPROTB1 is shown in Figure 15-48 and described in Table 15-50.

Return to the Summary Table.

Flash Write Protect Attribute Register B1

Figure 15-48. FPC_WEPROTB1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEPROT_PAGE												RESERVED			
R/W1S-0h												R-0h			

Table 15-92. FPC_WEPROTB1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-4	WEPROT_PAGE	R/W1S	0h	Write Protection enable for 64KB-256KB flash with each bit representing 8 sectors of 2KB 0: Page is not erase/program protected 1: Page is erase/program protected Reset type: XRSn
3-0	RESERVED	R	0h	Reserved

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43 FPC_FLSEMREQ Register (Offset = 1800h) [Reset = 00000000h]

FPC_FLSEMREQ is shown in Figure 15-49 and described in Table 15-51.

Return to the Summary Table.

Flash semaphore request register

Figure 15-49. FPC_FLSEMREQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															REQ
R-0h															R-0/W1S-0h

Table 15-94. FPC_FLSEMREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	REQ	R-0/W1S	0h	If the FLSEMSTAT.ASSIGNED bit is cleared, writing a '1' to this bit causes: 1) Load the Privilege attribute of the code performing the write into the FLSEMSTAT.PRIV bit field, and 2) Set the FLSEMSTAT.ASSIGNED bit. If the FLSEMSTAT.ASSIGNED is already set when a write to this bit occurs, the write will be ignored. If the above conditions are not met during the write, the write will be ignored with no error indicator. It is advised that the writing code perform a read of the FLSEMSTAT register to ensure it was set after writing to this bit. Reset type: XRSn

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44 FPC_FLSEMCLR Register (Offset = 1804h) [Reset = 00000000h]

FPC_FLSEMCLR is shown in Figure 15-50 and described in Table 15-52.

Return to the Summary Table.

Flash semaphore release register

Figure 15-50. FPC_FLSEMCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															CLR
R-0h															R-0/W1S-0h

Table 15-96. FPC_FLSEMCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLR	R-0/W1S	0h	If the following conditions are met, a write of '1' to this bit causes the FLSEMSTAT register to its reset state: 1) The FLSEMSTAT.PRIV of the code performing the write is 0x1 (i.e. privilege code can force relinquishing of the semaphore) or 2) FLSEMSTAT.ASSIGNED bit is set, and FLSEMSTAT.PRIV matches privilege attribute code performing the write. If the above conditions are not met during the write, the write will be ignored with no error indicated. It is advised that the writing code perform a read of the FLSEMSTAT register to ensure it was cleared after writing to this bit. Reset type: XRSn

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45 FPC_FLSEMSTAT Register (Offset = 1808h) [Reset = 00000000h]

FPC_FLSEMSTAT is shown in Figure 15-51 and described in Table 15-53.

Return to the Summary Table.

Flash semaphore statys registers

Figure 15-51. FPC_FLSEMSTAT Register

31	30	29	28	27	26	25	24
ASSIGNED	MATCH	RESERVED					
R-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							DBGACC
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							PRIV
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R-0h

Table 15-98. FPC_FLSEMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASSIGNED	R	0h	PRIV field is valid when this bit is set. 0 : PRIV is unassigned and flash controller is not accessible 1 : PRIV value is valid and the flash controller is currently assigned to the respective code Reset type: XRSn
30	MATCH	R	0h	On a read, this bit will reflect whether the reader's PRIV matches the ownership of the flash controller. 0 : Code performing read does not own the flash controller semaphore 1 : Code performing read owns the flash controller semphore. This avoids code from being required to know whether the current code segment owns the flash controller configuration. Reset type: XRSn
29-17	RESERVED	R	0h	Reserved
16	DBGACC	R	0h	Defines the flash controller semaphore owners debug access indication 0x0 : functional access 0x1 :Debug access Note : This bit is only an indication that the flash semaphore was last grabbed by the funtional/debug master. The other privileged master is still allowed to clear and grab the semaphore anytime. Also, if it was previously grabbed by a privileged master, the other privileged master can still access the flash controller. Reset type: XRSn
15-9	RESERVED	R	0h	Reserved
8	PRIV	R	0h	Defines the flash controller semaphore owners privilage attribute 0x0 : non-privilege 0x1 :prvilege Reset type: XRSn

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Table 15-98. FPC_FLSEMSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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46 VTOR_NS Register (Offset = 1B84h) [Reset = 01000001h]

VTOR_NS is shown in Figure 15-52 and described in Table 15-54.

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Non - Secure Vector Table Offset Register

Figure 15-52. VTOR_NS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTOR_NS																															
R/W-01000001h																															

Table 15-100. VTOR_NS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VTOR_NS	R/W	01000001h	value of INITNSVTOR port at CPUSS boundary Reset type: Rsn

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47 GSC_LOCK Register (Offset = 1D80h) [Reset = 00000000h]

GSC_LOCK is shown in Figure 15-53 and described in Table 15-55.

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GSC Lock configuration register

Figure 15-53. GSC_LOCK Register

31	30	29	28	27	26	25	24
KEY							
R-0/W-0h							
23	22	21	20	19	18	17	16
KEY							
R-0/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	VTOR	RESERVED	FPPC_AATRIB	SPC_AATRIB	PPC_AATRIB	ATTRIBVIOL_CONFIG
R/W-0h	R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 15-102. GSC_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R-0/W	0h	Write 0xA551 to update the register Reset type: XRSn
15-8	RESERVED	R-0	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R-0	0h	Reserved
5	VTOR	R/W	0h	Configuration impacts registers VTOR_* 0: Register configuration is not locked. 1: Register configuration is locked. Once register is locked - reads give the MMR data and writes are ignored Reset type: Rsn
4	RESERVED	R-0	0h	Reserved
3	FPPC_AATRIB	R/W	0h	Configuration impacts registers FPC_PRIVATTRIB_* 0: Register configuration is not locked. 1: Register configuration is locked. Once register is locked - reads give the MMR data and writes are ignored Reset type: XRSn
2	SPC_AATRIB	R/W	0h	Configuration impacts registers SPC_PRIVATTRIB_* 0: Register configuration is not locked. 1: Register configuration is locked. Once register is locked - reads give the MMR data and writes are ignored Reset type: XRSn

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Table 15-102. GSC_LOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PPC_AATRIB	R/W	0h	Configuration impacts registers PPC_PRIVATTRIB_* 0: Register configuration is not locked. 1: Register configuration is locked. Once register is locked - reads give the MMR data and writes are ignored Reset type: XRSn
0	ATTRIBVIOL_CONFIG	R/W	0h	Configuration impacts registers SPC_ATTRIBVIOLP_CONFIG, PPC_ATTRIBVIOLP_CONFIG, FPC_ATTRIBVIOLP_CONFIG 0: Register configuration is not locked. 1: Register configuration is locked. Once register is locked - reads give the MMR data and writes are ignored Reset type: XRSn

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48 GSC_COMMIT Register (Offset = 1D84h) [Reset = 00000000h]

GSC_COMMIT is shown in Figure 15-54 and described in Table 15-56.

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GSC commit configuration register

Figure 15-54. GSC_COMMIT Register

31	30	29	28	27	26	25	24
KEY							
R-0/W-0h							
23	22	21	20	19	18	17	16
KEY							
R-0/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	VTOR	RESERVED	FPPC_AATRIB	SPC_AATRIB	PPC_AATRIB	ATTRIBVIOL_CONFIG
R/W1S-0h	R-0-0h	R/W1S-0h	R-0-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

Table 15-104. GSC_COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R-0/W	0h	Write 0xA442 to update the register Reset type: XRSn
15-8	RESERVED	R-0	0h	Reserved
7	RESERVED	R/W1S	0h	Reserved
6	RESERVED	R-0	0h	Reserved
5	VTOR	R/W1S	0h	0: Register lock configuration is not committed. 1: Register configuration is committed. Commit configuration blocks the writes going to the lock register. Once configuration is committed, only reset can change the configuration. Reset type: Rsn
4	RESERVED	R-0	0h	Reserved
3	FPPC_AATRIB	R/W1S	0h	0: Register lock configuration is not committed. 1: Register configuration is committed. Commit configuration blocks the writes going to the lock register. Once configuration is committed, only reset can change the configuration. Reset type: XRSn
2	SPC_AATRIB	R/W1S	0h	0: Register lock configuration is not committed. 1: Register configuration is committed. Commit configuration blocks the writes going to the lock register. Once configuration is committed, only reset can change the configuration. Reset type: XRSn

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Table 15-104. GSC_COMMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PPC_AATRIB	R/W1S	0h	0: Register lock configuration is not committed. 1: Register configuration is committed. Commit configuration blocks the writes going to the lock register. Once configuration is committed, only reset can change the configuration. Reset type: XRSn
0	ATTRIBVIOL_CONFIG	R/W1S	0h	0: Register lock configuration is not committed. 1: Register configuration is committed. Commit configuration blocks the writes going to the lock register. Once configuration is committed, only reset can change the configuration. Reset type: XRSn

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49 GSC_REVISION Register (Offset = 1FFCh) [Reset = 00000000h]

GSC_REVISION is shown in Figure 15-55 and described in Table 15-57.

Return to the Summary Table.

GSC Revision register

Figure 15-55. GSC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MAJREV								MINREV							
R-0h																R-0h								R-0h							

Table 15-106. GSC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	MAJREV	R	0h	This hardcoded field defines the major revision of the IP. Reset type: XRSn
7-0	MINREV	R	0h	This hardcoded field defines the minor revision of the IP. Reset type: XRSn

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Chapter 16

Input-Output Mux (IOMUX)

The IOMUX controls the configuration of all device pins with digital input-output (IO) functions, including: digital function selection, inversion control, drive strength (if applicable), the pullup or pulldown resistor (if applicable), and wake-up configuration (if applicable on certain IOs for wakeup from SHUTDOWN mode).

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16.3 IOMUX Registers 786

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16.1 IOMUX Overview

The IOMUX manages the configuration of the digital IO pins through the Pin Control Management registers (PINCMx). Key functions configured by IOMUX include:

- Selection of which peripheral is multiplexed to each digital IO pin
- Digital Input Path Configuration
  - Input Path Enable/Disable
  - Input Signal Logic Inversion Control (Control bit shared with Output Logic Inversion)
- Digital Output Path Configuration
  - Drive Strength Control
  - Output Connection Enable/Disable
  - Output Signal Logic Inversion Control (Control bit shared with Input Logic Inversion)
- Wakeup Configuration (for Wakeup from SHUTDOWN mode on specified pins per table below)
  - Read wake up source from the WAKESTAT bit from the PINCMx register
  - Wake up compare level configuration to wake up on either a logic-low or logic-high
- Pull-up and Pull-down Resistor Control

16.1.1 IO Types and Analog Sharing

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. IOMUX also provides the controls for the output driver, input path, and the wakeup logic for wakeup from SHUTDOWN mode.

Digital IO Types

There are several digital IO types which can be included on a given device. Each digital IO type supports different features. Digital IO Features by IO Type lists the features which are included with each IO type. See the device-specific data sheet for which IO type is used on a given package pin.

Table 16-1. Digital IO Features by IO Type

IO Structure	Inversion Control	Drive Strength Control	Pullup Resistor	Pulldown Resistor	Wakeup Logic
Standard-drive (SDIO)	Y		Y	Y	
Standard-drive with wake (SDIO)	Y		Y	Y	Y
High-drive (HDIO)	Y	Y	Y	Y	
High-speed (HSIO)	Y	Y	Y	Y	

Digital IO Shared with Analog Functions

Certain pins on a device are digital only and do not have any analog functions connected to the pin. Other pins can have one or more analog functions connected to the pin in addition to the digital IO functions. Analog functions are never selected within the IOMUX; these are always configured within of the respective analog peripheral. Analog peripherals have no knowledge of, or interaction with, the IOMUX.

In general, when analog functionality is used on a pin which also has digital functions, the IOMUX configuration for that pin must be left in the default (high-Z) state so as to not interfere with the proper operation of the analog function. However, it is possible to have the IOMUX active on a pin when an analog peripheral is also interacting with the pin, provided that the application software verifies there is not a conflict between the functions. For example, it is possible to have the pullup or pulldown resistor on an IO enabled at the same time that the ADC is running a conversion on the same IO. However, an invalid configuration of enabling the output driver on an IO at the same time that an analog peripheral is driving the IO (for example, a CMPSSx_DACL or PGAx output). This creates an IO conflict.

Application software is responsible for making sure that the IOMUX settings do not conflict with any analog peripheral functions which can be enabled on a shared pad.

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IO Slice

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Superset IO Slice. Not all pins have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the Pin Configuration and Functions table within the device-specific data sheet for detailed information on what features and peripherals are supported on a specific pin. An example for a single pin is shown below in IOMUX Pin Example.

Table 16-2. IOMUX Pin Example

PINCMx	Pin Name	Analog [MuxMode]	Digital [MuxMode]	IO Structure
IOMUX_PA2	PA2	Unconnected	Unconnected	High-Drive
		ANALOG_AIN8 [ANALOG]	GPIO02 [1]	
		A0_3 [A0]	MCPWM4_2A [2]	
		CMP1_HN0 [A1]	MCPWM3_1B [3]	
		PGA0_OUT [A2]	MCPWM3_3A [4]	
			MCPWM4_3A [5]	
			MCPWM4_2B [6]	
			UC1_TX_SDA_PICO [7]	
			MCPWM3_1A [8]	
			UC0_TX_SDA_PICO [11]	
			OUTPUTXBAR5 [14]	

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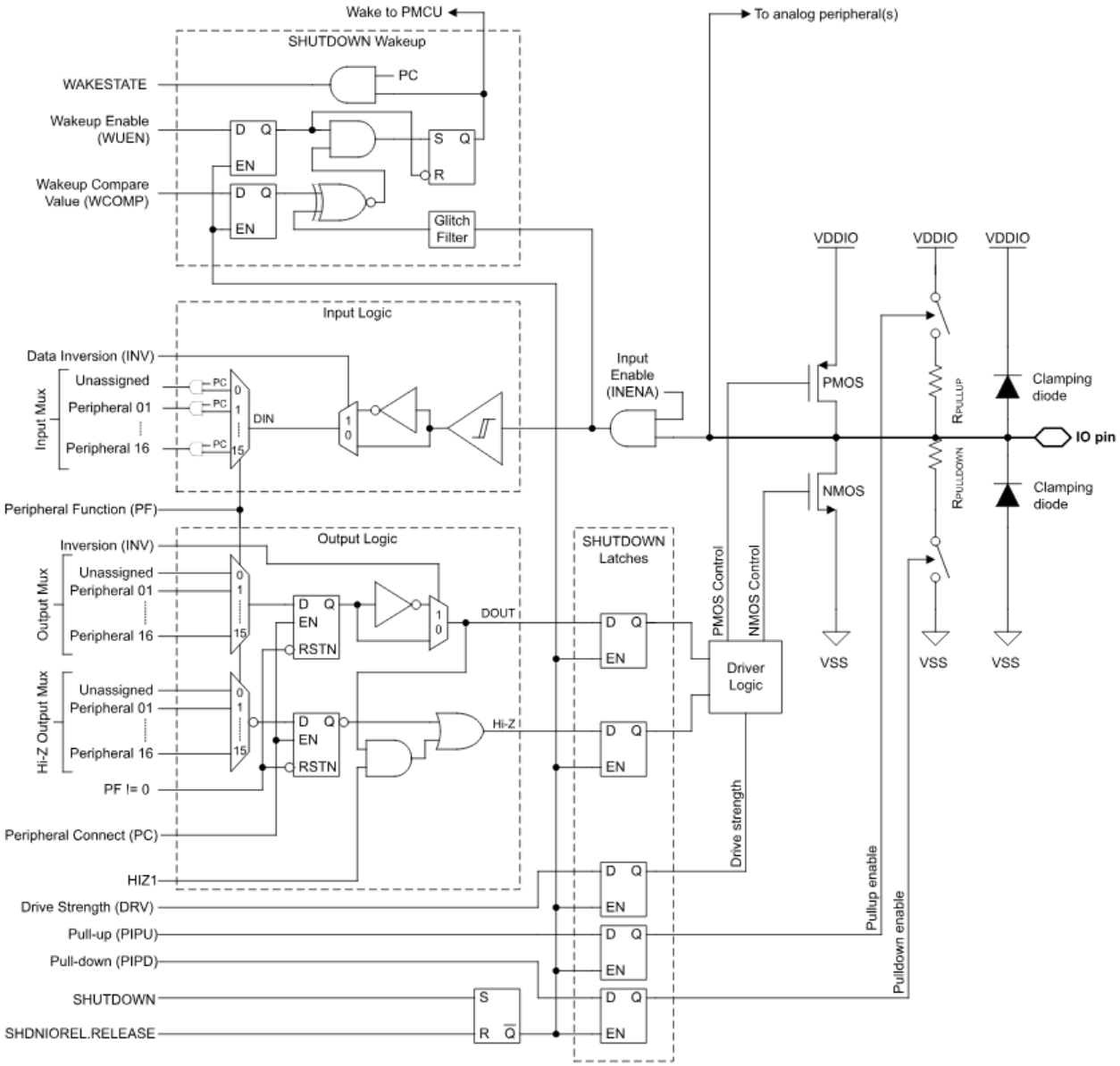


Figure 16-1. Superset IO Slice

Default IOMUX State

The initial state of the IOMUX pin slice for all digital IO after a BOOTRST is as follows:

- The digital IO is in a high-impedance state
- The peripheral function selection field (PINCMx.PF) is cleared such that no peripheral function is selected
- The digital IO output is disabled by clearing the peripheral connect (PINCMx.PC) bit
- The input enable (PINCMx.INENAx) bit is cleared (disabled)
- The inversion logic (PINCMx.INV) is disabled
- The Hi-Z output high (PINCMx.HIZ1) mode is disabled
- The pullup/pulldown (PINCMx.PIPU and PINCMx.PIPD) resistors are disabled
- The drive strength control (PINCMx.DRV) is reset
- The wakeup logic (PINCMx.WUEN) is disabled

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Note

The JTAG/serial wire debug (JTAG/SWD) pins are a specific exception to the above default state. The debug pins are configured in SWD mode by default, and can be switched to an alternate setting after start-up.

16.2 IOMUX Operation

Each digital IO on a device has a dedicated 32-bit PINCM register in the IOMUX peripheral register space which is used to configure the digital functions of the respective IO. See the device specific data sheet for determining the PINCM register index which corresponds to the IO to be configured.

16.2.1 Peripheral Function (PF) Assignment

When setting up the initial IOMUX configuration for an IO after a BOOTRST, application software can select which digital peripheral from the supported options is to be connect to an IO by writing the appropriate peripheral select value to the PF field while simultaneously setting the PC and INENA bits in the PINCMx register corresponding to the targeted pin. The IOMUX configurations for a given peripheral must be set before the peripheral connected to the IOs has been initialized for operation.

To change the peripheral function selection for a digital IO at runtime after a peripheral function has already been configured for that IO, the following procedure must be followed:

1. Disable the currently connected peripheral function
2. Clear the PC bit (input/output connect bit) and INENA (input connect bit) in the corresponding PINCMx register
3. Write 0x0 to the PF field in the PINCMx to clear the logic in the data path
4. Select the new peripheral function by writing the peripheral function ID to the PF register
5. Set the PC and INENA bits in the PINCMx register to connect the newly selected peripheral
6. Enable the newly selected peripheral for operation

At runtime, the INENA bit can be used to mask the input from the IO to the peripheral, if desired. When INENA is cleared, a connected digital peripheral sees a logic low (0) from the IO, regardless of the external state of the IO. If an IO supports wakeup from SHUTDOWN mode, the INENA bit also controls propagation of the IO state to the SHUTDOWN mode wakeup logic.

If a peripheral is assigned to an IO, but the peripheral is in a disabled state, the last valid output conditions (output logic level and Hi-Z state) are latched in the IOMUX output logic. When the peripheral is enabled, the IOMUX releases the latched state to allow the (now enabled) peripheral's output state to propagate to the IO. The PMCU indicates to the IOMUX when a peripheral is entering a disabled state via the IORET signal, which is combined with the PC signal via a logic OR to control the output state latches. This mechanism handles preservation of the last valid output state of peripherals in power domain 1 (PD1) when entering STOP or STANDBY mode, as PD1 peripherals are always temporarily disabled upon entry to STOP/STANDBY, and re-enabled upon exit from STOP/STANDBY modes.

When no peripheral function is selected (PF==0) the output latches are put into a reset state, causing the output NMOS and PMOS to be disabled (leaving the IO pin in a Hi-Z state with the exception of any enabled pullup/pulldown resistors). Note that the pullup/pulldown resistors are never controlled by either a connected peripheral or the peripheral muxing logic. These resistors are only controlled by the IOMUX control bits.

16.2.2 Logic High to Hi-Z Conversion

The IOMUX supports translating an output high signal from a connected peripheral into a Hi-Z output state at the IO pin. This functionality is particularly useful for open-drain digital input/output applications. When this functionality is enabled, the IO pin state as a function of the peripheral output is as shown in Table 16-3.

Table 16-3. Logic High to Hi-Z Truth Table

Connected Peripheral Output	IO Pin State (Z1 = 0x0)	IO Pin State (Z1 = 0x1)
Logic low (0)	Output low	Output low

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Table 16-3. Logic High to Hi-Z Truth Table (continued)

Connected Peripheral Output	IO Pin State (Z1 = 0x0)	IO Pin State (Z1 = 0x1)
Logic high (1)	Output high	High impedance (Hi-Z)

To enable logic high to Hi-Z conversion on a digital IO, set the Z1 bit in the corresponding PINCMx register.

16.2.3 Logic Inversion

The IOMUX supports logic inversion of the digital input/output path. Logic inversion is useful for scenarios where opposite polarity is required for UART functions or SPI chip select functions.

To enable logic inversion on a digital IO, set the INV bit in the corresponding PINCMx register. To disable logic inversion, clear the corresponding bit. Logic inversion is disabled by default.

16.2.4 SHUTDOWN Mode Wakeup Logic

In SHUTDOWN mode, the entire regulated core supply of the device is disabled and the device wakes only from a wake-capable IO that is configured for wakeup, from NRST, or from a SWD debug connection. The IO wake mechanism for exiting SHUTDOWN is managed by IOMUX and is level based. Specific standard-drive IOs, include the additional wakeup logic that can be used to wake the device from a SHUTDOWN operating mode upon a level match.

To configure a wake-capable IO for wakeup from SHUTDOWN mode:

1. Set the INENA bit to let the input state propagate from the IO to the wakeup logic.
2. Select the compare level to use for wake by setting or clearing the WCOMP bit in the PINCMx register corresponding to the targeted pin.
3. Enable wakeup by setting the WUEN bit in the PINCMx register corresponding to the targeted pin.

After the previous configuration, SHUTDOWN mode can be entered through the appropriate command in SYSCTL. Pins on the device that contain digital IO controlled by IOMUX retain the current state when the device enters into SHUTDOWN. While the digital IO state is latched upon entry into SHUTDOWN mode, the IOMUX configuration registers (all PINCMx registers) lose the contents as the regulated core supply is shut down.

After SHUTDOWN is entered, a level match on any pin configured for wakeup triggers the exit sequence from SHUTDOWN. When the device exits SHUTDOWN, a BOR-level reset occurs but the state of the digital IO remains latched through the reset, keeping the IO state present upon entry into SHUTDOWN. This state is held until the IO are released in SYSCTL. After the BOR, SYSCTL captures the cause of the reset as a SHUTDOWN exit so that software can identify this and take appropriate action to reconfigure the device.

If multiple pins are configured for wakeup from SHUTDOWN, application software can determine which wakeup-configured IO generated the wake by polling the WAKESTATE bit in any IOs enabled for wake before the SHUTDOWN exit.

Application software must apply the following process to restore the IO state upon exit from SHUTDOWN:

1. Check which IO triggered the wakeup from SHUTDOWN, if necessary, as follows:
   a. Reconfigure the PINCMx register corresponding to the IO to be tested for wakeup status and set the peripheral connect (PC) bit (the PC bit gates the WAKESTATE indication).
   b. Test the WAKESTATE bit in the PINCMx register corresponding to the IO to be tested to determine if that particular IO received a WAKE status based on the previously configured WCOMP and WUEN configuration.
2. Reconfigure any remaining IOMUX PINCM registers to the correct states.
3. Reconfigure the peripherals that are connected to pins through IOMUX, and enable them.
4. Release the SHUTDOWN IO lock in SYSCTL.
5. Clear the WUEN bit in the PINCMx register to reset the WAKESTATE status.

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Note

After waking from SHUTDOWN, if the WUEN bit is not cleared and the shutdown release bit in SYSCTL is not set, then reentering SHUTDOWN results in an immediate wake event, because the WAKESTATE status has not been cleared from the previous wake event.

16.2.5 Pullup/Pulldown Resistors

Programmable pullup/pulldown resistors are provided on most digital IO types, and are connected to VDD/VSS, respectively.

To enable the pullup or pulldown resistor on a digital IO, set the PIPU or PIPD bit, respectively, in the corresponding PINCMx register. To disable the pullup or pulldown resistor, clear the corresponding bit.

The pullup/pulldown resistors can be enabled at any time, and the configuration is independent from the peripheral function configuration. Enable a pullup/pulldown resistor while changing the selected peripheral function is possible.

Note

If both pull resistors are configured at the same time, the pullup resistor takes priority.

16.2.6 Drive Strength Control

The high-drive and high-speed digital IO types have programmable drive strength (low drive and high drive). The default drive strength is low drive. Application software can request high drive by setting the DRV bit in the PINCMx register corresponding to the target digital IO. Drive strength control is not available for standard drive IO type.

The drive strength control is completely independent of the selected peripheral function (PF) and can be changed by application software at any time.

For detailed electrical specifications on the drive performance in each drive mode for a given IO, see the Digital IO parameters in the device-specific data sheet.

16.3 IOMUX Registers

This Section describes the IOMUX Registers.

16.3.1 IOMUX Base Address Table

Table 16-4. IOMUX Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
IomuxRegs	IOMUX_REGS	IOMUX	0x400C_C000

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16.3.2 IOMUX_REGS Registers

Table 16-5 lists the memory-mapped registers for the IOMUX_REGS registers. All register offset addresses not listed in Table 16-5 should be considered as reserved locations and the register contents should not be modified.

Table 16-5. IOMUX_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	PINCM	Pin Control Management Register in SECCFG region		Go

Complex bit access types are encoded to fit into small table cells. Table 16-6 shows the codes that are used for access types in this section.

Table 16-6. IOMUX_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 PINCM Register (Offset = 0h) [Reset = 00X00000h]

PINCM is shown in Figure 16-2 and described in Table 16-7.

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Pin Control Management Register

Figure 16-2. PINCM Register

31	30	29	28	27	26	25	24
RESERVED			WCOMP	WUEN	INV	HIZ1	RESERVED
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-00Bh
23	22	21	20	19	18	17	16
RESERVED			DRV	HYSTEN	INENA	PIPU	PIPD
R/W-00Bh			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED		WAKESTAT	RESERVED				
R/W-0h		R-0h	R/W-0h				
7	6	5	4	3	2	1	0
PC	RESERVED	PF					
R/W-0h	R/W-0h	R/W-0h					

Table 16-8. PINCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	WCOMP	R/W	0h	Wakeup Compare Value bit 0h = Wakeup on a match of 0 1h = Wakeup on a match of 1
27	WUEN	R/W	0h	Wakeup Enable bit 0h = wakeup is disabled. 1h = wakeup is enabled
26	INV	R/W	0h	Data inversion selection 0h = Data inversion is disabled. 1h = Data inversion is enabled
25	HIZ1	R/W	0h	High output value will tri-state the output when this bit is enabled 0h = open-drain is disabled. 1h = open-drain is enabled.
24-21	RESERVED	R/W	00Bh	
20	DRV	R/W	0h	Drive strength control selection, for HS IOCELL only 0h = Drive setting of 0 selected 1h = Drive setting of 1 selected
19	HYSTEN	R/W	0h	Hystersis Enable Control Selection 0h = hysteresis is disabled. 1h = hysteresis is enabled
18	INENA	R/W	0h	Input Enable Control Selection 0h = Input enable is disabled. 1h = Input enable is enabled.
17	PIPU	R/W	0h	Pull Up control selection 0h = Pull up is disabled. 1h = Pull up is enabled
16	PIPD	R/W	0h	Pull Down control selection 0h = Pull down is disabled. 1h = Pull down is enabled
15-14	RESERVED	R/W	0h	

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Table 16-8. PINCM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	WAKESTAT	R	0h	This has the IOPAD WAKEUP signal as status bit. 0h = wakeup source is NOT from this IOCELL 1h = wakeup source is from this IOCELL
12-8	RESERVED	R/W	0h	
7	PC	R/W	0h	Peripheral is "Connected" 0h = The output of the peripheral (and its output enable) will not propagate to the IOCELL 1h = The output latch of the dataflow will be "transparent"
6	RESERVED	R/W	0h	
5-0	PF	R/W	0h	P channel Function selection bits 0h = Reserved as unconnected 3Fh = An encoding per function that can be connected to this pin.

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Chapter 17

Timers (TIMx)

The timer module (TIMx) is a general purpose timer counting module with multiple compare/capture blocks. The timers include many common features that can be used for a variety of functions such as measuring the input signal edge and period (capture mode) or generating output waveforms like PWMs (compare mode output).

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17.4 TIMERS Registers 819

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17.1 TIMx Overview

The timer module (TIMx) is a timer counting module with multiple compare/capture blocks. There are various types of timer instances available within the module defined by the values G0 to G14 that support different features. All timers use a common timer architecture, which allows for easy migration between timer instances with common functions. This minimizes the need to write extra software for timer-based applications and allows for easy porting and maintenance between TIMx instances.

Note

See Section 17.1.1 to determine the common features available between TIMx instances.

In this section:

- “TIMx” indicates a feature common across all timer instances.
- "TIMGx" indicates a feature available only on the specified TIMGx instances.

Note

The 'x' value in the TIMx and TIMGx nomenclature is separate from the 'xy' values used within the register naming within this chapter. The 'xy' value is used to represent the register arrays that exist in the timer module to group registers with same bit fields for different capture/compare ports. For example, TIMx.CC_01[0/1] is a register array that contains the capture/compare registers for both CCP0 and CCP1. Access TIMx.CC_01[0] to read the CC0 capture/compare value, and access TIMx.CC_01[1] to read the CC1 capture/compare value.

The TIMx module consists of 16-bit and 32-bit auto reload counters driven by a programmable prescaler with up to 4 capture/compare (CC) blocks and capture/compare pins (CCP) to enable multiple capture/compares, PWM outputs, and interval timing. TIMx also has extensive event generation capabilities, including counter overflow, reload, and capture/compare actions for a variety of use cases.

17.1.1 TIMx Instance Configuration

Table 17-1 shows the TIMx instance configuration for all TIMER instances.

Table 17-1. TIMx Instance Configuration

Instance	Counter Resolution	Prescaler	CCP Channels (External/Internal)	External PWM Channels	Shadow Load	Shadow CCs
TIMG4 (1x)	16-bit	8-bit	2	2	Yes	Yes
TIMG12 (1x)	32-bit	-	2	2	-	Yes

17.1.2 TIMG Features

Specific features for TIMG include:

- 16-bit (TIMG4) or 32-bit (TIMG12)up, down, or up-down counter, with repeat-reload mode
- 8-bit programmable prescaler to divide the counter clock frequency
- Up to four independent channels for
  - Output compare
  - Input capture
  - PWM output (Edge-Aligned and Center-Aligned)
  - One-shot mode
- Selectable and configurable clock source
- Shadow register mode for load and compare values (see Shadow Load and Shadow Compare)
- Supports synchronization and cross trigger among different TIMx instances in the same power domain (see Synchronization With Cross Trigger)
- Supports CPU interrupt generation, DMA trigger generation, and ADC sequencer trigger generation (see TIMx Interrupts & Triggers)

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17.1.3 Functional Block Diagram

TIMGx Functional Block Diagram shows the TIMx block diagram for AM13E23x.

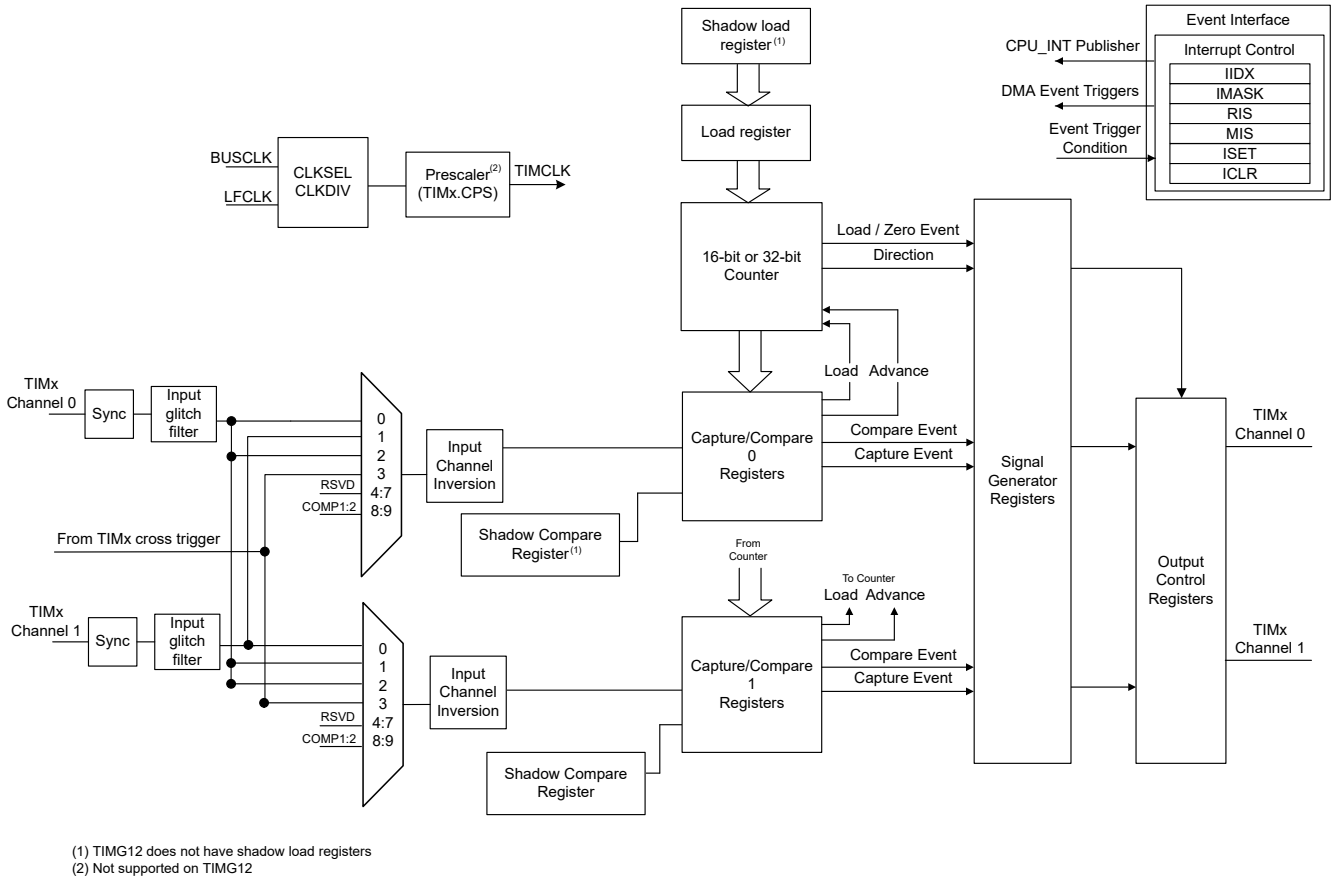


Figure 17-1. TIMGx Functional Block Diagram

17.2 TIMx Operation

The TIMx module is configured with user software. The setup and operation of TIMx is discussed in the following sections.

Note

There are register arrays in the timer module to group registers with same bit fields for different capture/compare ports. For example, TIMx.CC_01[0/1] is a register array that contains the capture/compare registers for both CCP0 and CCP1. Access TIMx.CC_01[0] to read the CC0 capture/compare value, and access TIMx.CC_01[1] to read the CC1 capture/compare value. This chapter uses 'xy' in place of the register array numbers to cover all register arrays (TIMx.CC01[0/1] becomes TIMx.CC_xy[0/1]).

17.2.1 Timer Counter

All TIMx instances have 16-bit counter blocks except for TIMG12 and TIMG13, which have 32-bit counter blocks. The timer counter register (TIMx.CTR) can count down, up-and-down, or up depending on the operation mode. It can also be read or written with software.

The counter can advance (increment or decrement) using the internal clock TIMCLK, with the rising and/or falling edge of an timer external input, or an internal trigger event from other peripherals (see advance condition). By default, each count occurs with each rising edge of the TIMCLK signal.

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Enabling the TIMx Counter

The counter is clocked by the prescaler output TIMCLK. The counter enable bit TIMx.CTRCTL.EN can be enabled in two ways:

- Set in software manually
- After a load condition (LCOND) or zero condition (ZCOND) is met, and the counter value after enable bit (TIMx.CTRCTL.CVAE) is set to the load value or zero value, respectively.

Note

The ability to write the counter register while TIMx is running is possible but should be avoided because the user write can collide with a load, zero, or advance event. Depending on the prescaler ratio, the application cannot predict the timing of the write, which can affect the correct timer period.

17.2.1.1 Clock Source Select and Prescaler

The TIMx clock (TIMCLK) can be sourced from an internal clock or an external signal trigger to advance the clock.

17.2.1.1.1 Internal Clock and Prescaler

The TIMx clock (TIMCLK) source is enabled by setting the TIMx.CLKSEL register. It can also be further divided by a ratio by setting the TIMx.CLKDIV register and the prescaler (TIMx.CPS). The selected source clock is always available and the frequency depends on the power mode. For more information, see the Clock Module (CKM) section.

The TIMCLK is sourced from MCLKDIV2. The clock source can be passed directly to TIMx or divided by the 8-bit prescaler. The prescaler setting can be configured with the TIMx.CPS.PCNT bit. The selected TIMCLK source is divided by a value of (PCNT+1). A PCNT value of 0 divides TIMCLK by 1, effectively bypassing the divider. A PCNT value of greater than 0 divides the TIMCLK source to generate a slower clock.

TIMx also has a software mechanism for disabling the timer clock. Set TIMx.CCLKCTL.CLKEN to 0 to put the timer in an IDLE state.

TIMCLK Configuration

To configure the clock source, divider, and prescaler:

1. Enable the TIMCLK clock source (MCLKDIV2) using the CLKSEL register.
2. Optionally divide the TIMCLK using CLKDIV.RATIO.
3. Optionally set a prescaler using CPS.PCNT.
4. Enable the TIMCLK by setting CCLKCTL.CLKEN = 1.

The frequency of TIMCLK is determined using Equation 13.

$$f_{TIMCLK} = \frac{f_{MCLKDIV2}}{((CLKDIV.RATIO + 1)*(CPS.PCNT + 1))} \quad (13)$$

17.2.1.1.2 External Signal Trigger

The counter can also advance (increment or decrement) by using an external signal on the timer input capture/compare pin (CCP) or by triggering from an event from other peripherals in the system. This can be configured by using the advance condition setting (TIMx.CCCTL_xy[0/1].ACOND) to specify what creates the advance event. To specify what event advances the counter, use the TIMx.CTRCTL.CAC setting.

17.2.2 Counting Mode Control

When the device is out of reset, TIMx is disabled. Writing 1 to the TIMx.CTRCTL.EN bit enables the counter. This bit is automatically cleared if TIMx.CTRCTL.REPEAT=0 (do not automatically reload the counter), and the counter value equals zero in down counting mode or the LOAD value in up counting mode.

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TIMx has three counting modes when enabled: down, up/down, and up. The operating mode is selected by TIMx.CTRCTL.CM bit (shown in TIMx Counting Modes (CM)). After the counter is enabled, the timer will start counting from the value specified by the TIMx.CTRCTL.CVAE bitfield.

Table 17-2. TIMx Counting Modes (CM)

TIMx.CTRCTL.CM	Counting Mode
0	Down
1	Up/Down
2	Up

Table 17-3. TIMx Counter Value after Enable (CVAE)

Count Value After Enable (CVAE)	Description	Supported Counting Modes
0	LOAD value	Up, up/down, down
1	Unchanged from current Counter value	Up/down
2	Zero value	Up, up/down, down

17.2.2.1 One-shot and Periodic Modes

One-shot and Periodic Mode Behavior shows TIMx working in both one-shot mode (left) and periodic mode (right).

One-shot Mode

When TIMx.CTRCTL.REPEAT bit is set to 0, TIMx does not advance when:

- TIMx.CTR value reaches 0 in either down- or up/down-counting mode
- TIMx.CTR value reaches TIMx.LOAD in up-counting mode

Periodic Mode (Counter Reload)

When TIMx.CTRCTL.REPEAT is set to 1h, TIMx automatically repeats once a zero or load event occurs. This happens when:

- TIMx.CTR reaches 0 in either down- or up/down-counting mode
  - In down-counting mode, a zero event is followed by a load event at the next advance condition
  - In up/down-counting mode, a zero event is followed by an advance event (+1), restarting the counter.
- TIMx.CTR reaches TIMx.LOAD in up-counting mode
  - A load event is followed by a zero at the next advance condition

TIMx.CTRCTL.REPEAT can also be set to 3h for TIMx to repeat only when not in a debug condition. If there is a debug condition, TIMx will count to the zero event and repeat only once the debug condition is removed.

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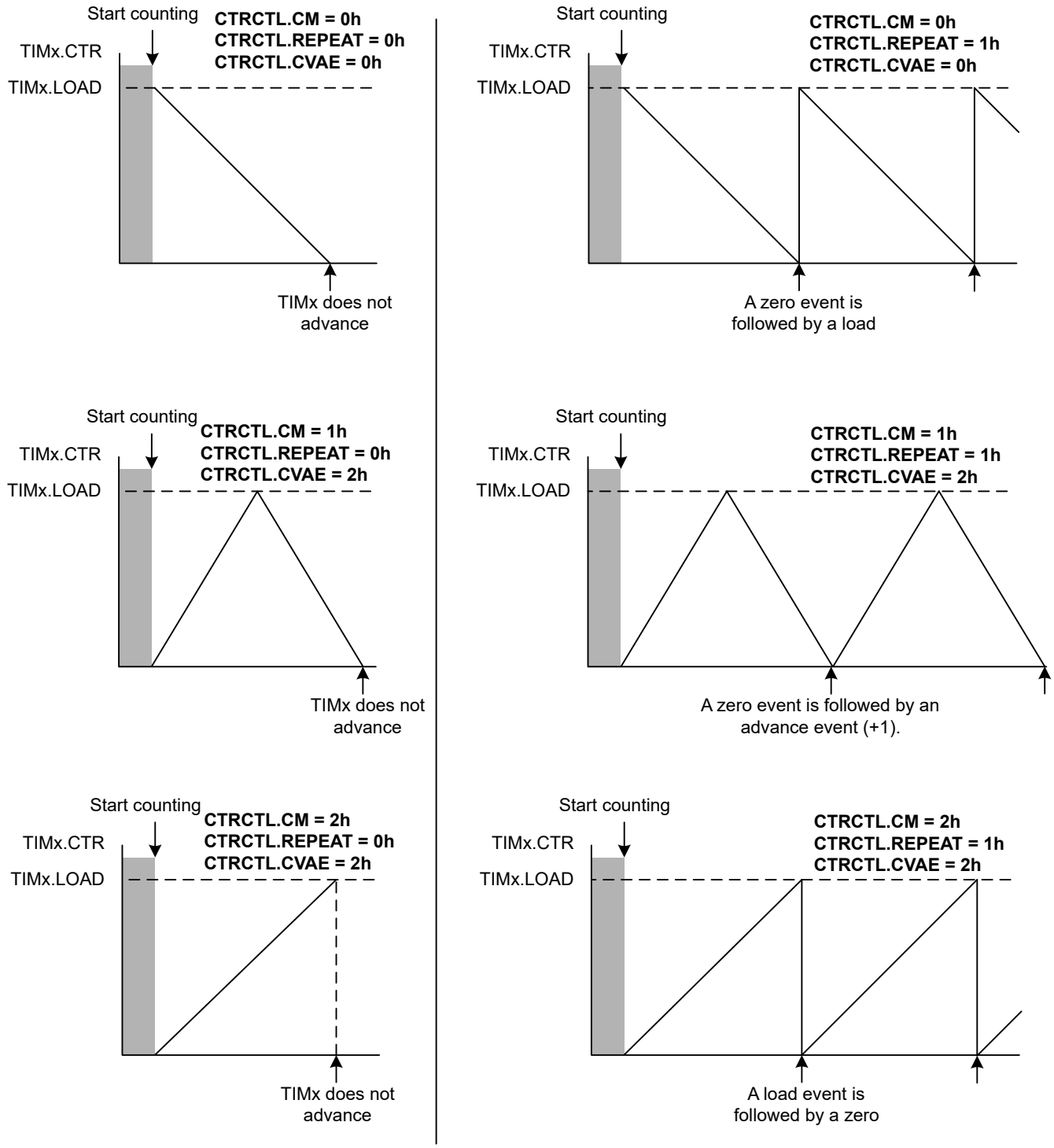


Figure 17-2. One-shot and Periodic Mode Behavior

17.2.2.2 Down Counting Mode

In down counting mode (CM = 0) when TIMx.CTRCTL.CVAE = 0, the TIMx.LOAD value is loaded into TIMx.CTR. Then TIMx counts from the LOAD value down to zero. When the TIMx.CTR value equals zero and TIMx.CTRCTL.REPEAT is set to 1 (periodic mode), the TIMx.LOAD value is once again loaded into TIMx.CTR and the timer repeats the down counting pattern as shown in Down Counting Mode, CVAE = 0.

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A zero event is generated when TIMx counts to zero. A load event is generated when TIMx counts from zero to the TIMx.LOAD value. Down Counting Mode Event Generation shows the event generating cycle.

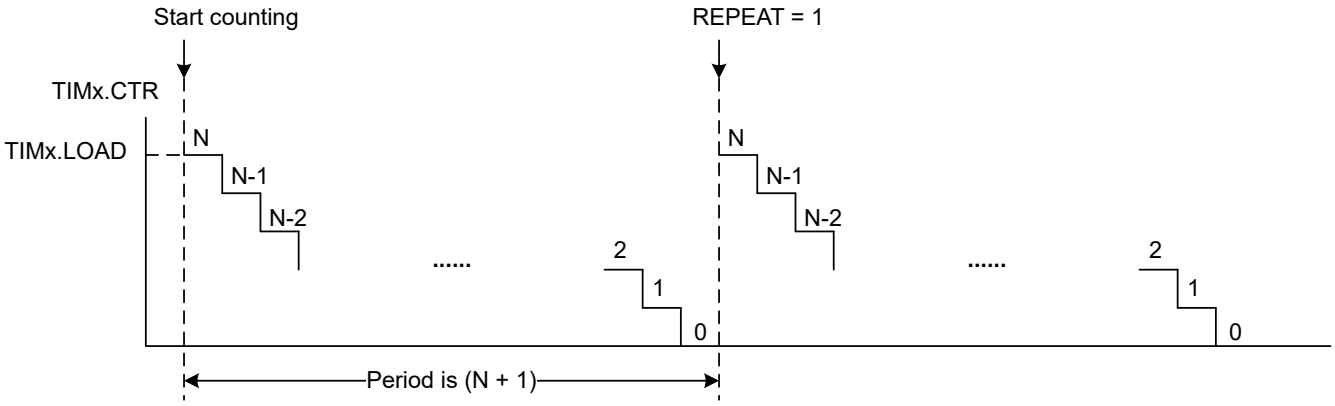


Figure 17-3. Down Counting Mode, CVAE = 0

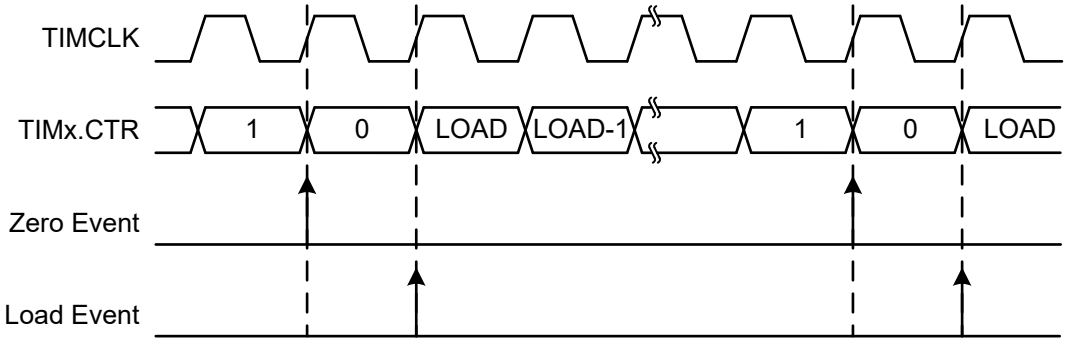


Figure 17-4. Down Counting Mode Event Generation

17.2.2.3 Up/Down Counting Mode

The Up/Down counting mode can count in an down-up direction or an up-down direction depending on TIMx.CTRCTL.CVAE value. The TIMx.CTRCTL.CVAE bits specify the initialization condition of the counter.

Table 17-4. Counter Value after Enable Initialization Conditions

TIMx.CTRCTL.CVAE Value	Counter Value After Enable
0x0	Load Value (down-up direction)
0x1	No Change
0x2	Zero (up-down direction)

Counting in down-up direction

When TIMx.CTRCTL.CVAE = 0, TIMx.CTR is set to TIMx.LOAD register value and TIMx counts in the down direction. When it reaches zero, a Zero event is generated and TIMx counts back up to TIMx.LOAD value. A Load event is generated when it reaches TIMx.LOAD value.

Down-up Counting Mode and Event Generation, CVAE = 0 shows TIMx counting in the down-up direction when TIMx.CTRCTL.CVAE = 0.

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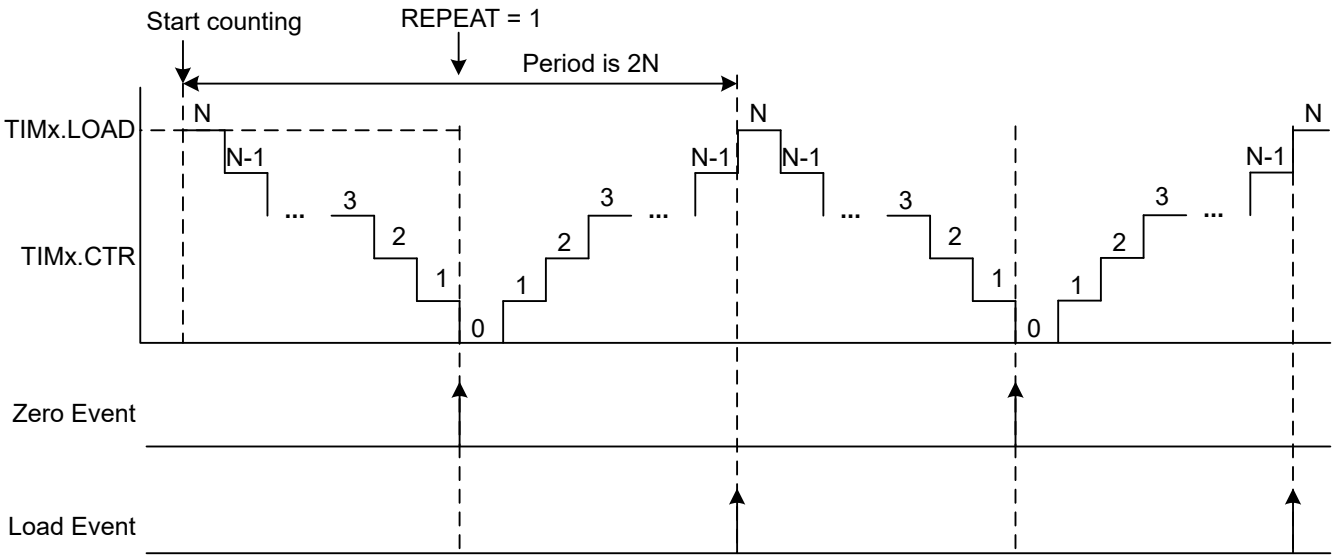


Figure 17-5. Down-up Counting Mode and Event Generation, CVAE = 0

Counting in up-down direction

When TIMx.CTRCTL.CVAE = 2, TIMx.CTR is set to zero and TIMx counts in the up direction. When it reaches TIMx.LOAD, a Load event is generated and TIMx counts back down to zero. A Zero event is generated when it reaches zero.

Up-down Counting Mode and Event Generation, CVAE = 2 shows TIMx counting in up-down direction when TIMx.CTRCTL.CVAE = 2.

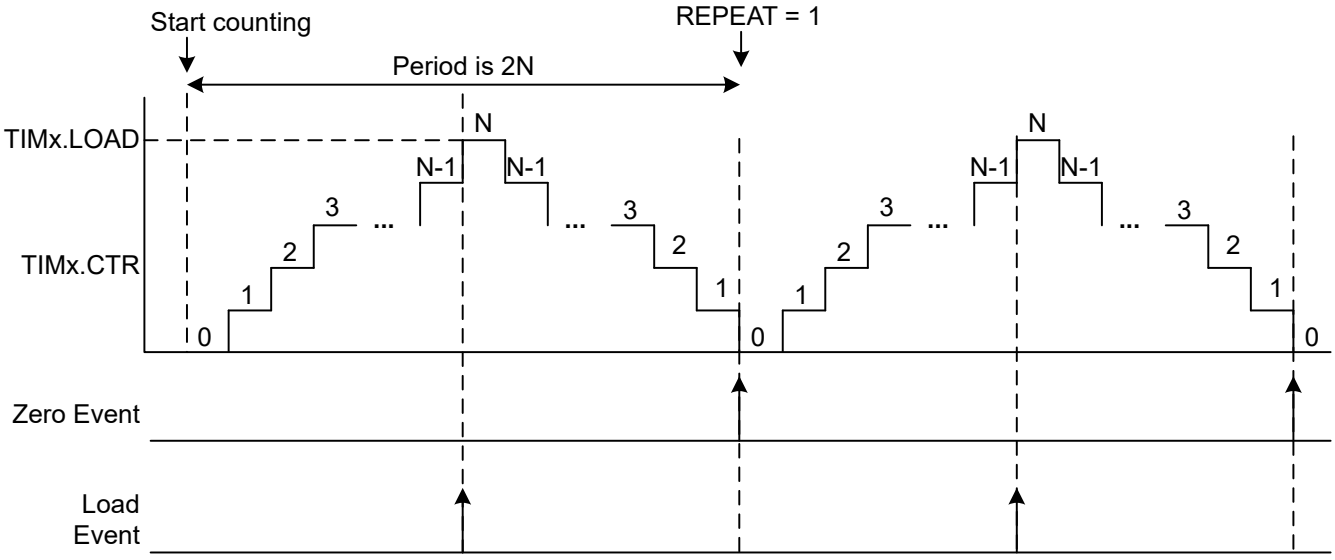


Figure 17-6. Up-down Counting Mode and Event Generation, CVAE = 2

17.2.2.4 Up Counting Mode

In up counting mode, TIMx counts from zero up to the value defined in TIMx.LOAD. When the TIMx.CTR value equals TIMx.LOAD and TIMx.CTRCTL.REPEAT is set to 1 (periodic mode), zero is loaded into TIMx.CTR and the timer repeats the up counting pattern as shown in Up Counting Mode, CVAE = 2.

A Load event is generated when TIMx counts to TIMx.LOAD. A Zero event is generated when TIMx counts from TIMx.LOAD to the zero value. Up Counting Mode Event Generation shows the event generating cycle.

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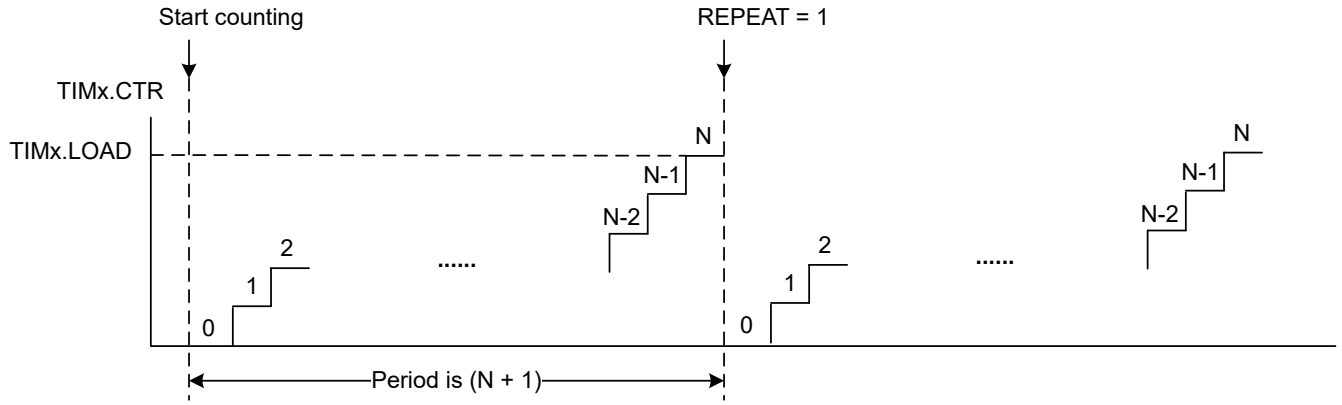


Figure 17-7. Up Counting Mode, CVAE = 2

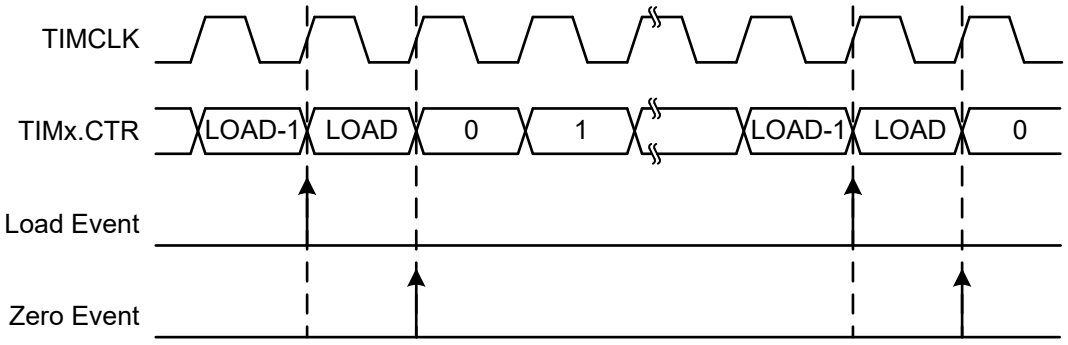


Figure 17-8. Up Counting Mode Event Generation

17.2.3 Capture/Compare Module

The capture/compare (CC) block is used for capture events or compare events. TIMG0 through TIMG13 have up to 2 identical capture/compare blocks and TIMG24 has up to 4 identical capture/compare blocks present to support external or internal signals. Any of the TIMx capture/compare blocks may be used to capture timings of an input signal or to generate time intervals.

Key registers for configuring capture/compare mode:

- **TIMx.LOAD**: the contents of this register are copied to counter (TIMx.CTR) on any operation designated to do a "load". This value is also used to compare with the counter value for generating a "Load Event" which can be used for interrupt, trigger, or signal generation actions.
- **TIMx.CC_xy[0/1]**: this is a register that can be used as either a capture register to acquire or record the next counter value on an event, or a compare register to the current counter to create an event.
- **TIMx.CCCTL_xy[0/1]**: this register controls the operations of the respective CC (capture/compare) blocks. In capture mode, it can configure whether a rising edge or falling edge generates a load, zero, advance, or capture condition. In compare mode, it controls which sources generate different types of compare events.
- **TIMx.CTRCTL**: this register provides control over the counter operation in different conditions.
- **TIMx.IFCTL_xy[0/1]**: this register controls the input filtering, input selection, and input inversion for the associated CC block.

Note

Capture and compare modes on a TIMx instance use the same registers. Therefore application cannot perform a capture and compare on the same channel at the same time.

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17.2.3.1 Capture Mode

Capture mode is selected when the TIMx.CCCTL_xy[0/1].COC bit is set to 1. Capture mode is used to generate capture events and record time intervals, which is useful for speed computation or time measurements.

17.2.3.1.1 Input Selection, Counter Conditions, and Inversion

The TIMx.IFCTL register is used for selecting input source, filtering, and final inversion options for the capture/compare block.

Figure 17-9 shows the block diagram for the TIMx capture block with two CC channels.

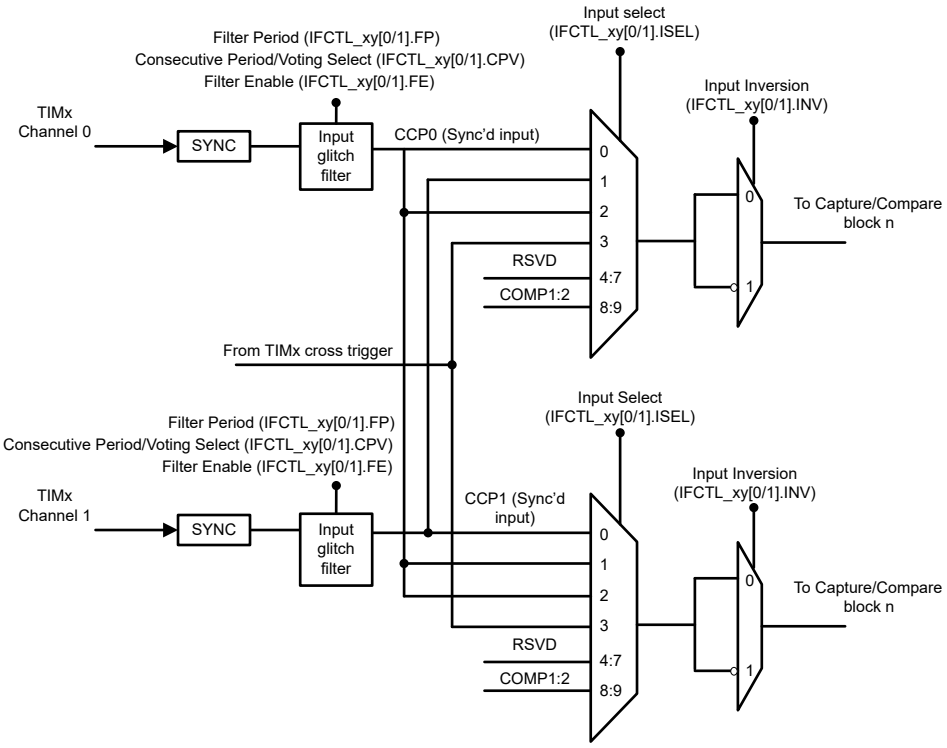


Figure 17-9. TIMx Capture Block Diagram

17.2.3.1.1.1 CCP Input Edge Synchronization

When using a capture/compare pin (CCP) as an input, configure the pin control management register (PINCMx) for the TIMx CCP input. See IOMUX for more information.

The CCP input signal is always passed through a synchronizer, and the input state (high or low) must be greater than one TIMCLK clock period for the synchronizer to detect the edge. CCP input edge detection requires at least one TIMCLK cycle (rise and fall) to synchronize the edge input. Timing in the first TIMCLK cycle is uncertain because the edge detection cannot be predicted in the first TIMCLK period.

When the capture condition occurs, an additional TIMCLK cycle is required to generate the capture event.

17.2.3.1.1.2 Input Selection

The input select bits TIMx.IFCTL_xy[0/1].ISEL select the input source to the filter input as the corresponding CCP input, the CCP pair of the current CCP input, or an external trigger.

Table 17-5. Input Selection Options for TIMx CC Instances

Input selection (TIMx.IFCTL_xy[0/1].ISEL)	Source
0h	TIMx CCP of the corresponding capture compare unit
1h	Input pair CCPx of the capture compare unit. [CCP0 for CCP1 and CCP1 for CCP0]

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Table 17-5. Input Selection Options for TIMx CC Instances (continued)

Input selection (TIMx.IFCTL_xy[0/1].ISEL)	Source
2h	TIMx CCP0

17.2.3.1.1.3 CCP Input Filtering

The input glitch filter can be enabled by setting the TIMx. IFCTL_01[0/1].FE bit. The filter period is configured by setting the TIMx. IFCTL_01[0/1].FP bit.

A consecutive period or majority voting format selected by the TIMx.IFCTL_xy[0/1].CPV bit is used to select the criteria for a CCP input signal.

- **Consecutive period** - The CCP input signal must be at the specified level for the defined number of FP timer clocks for the CCP input to be processed.
- **Majority voting** - The filter ignores one clock of opposite logic over the filter period. For example, over the number of FP samples of the input, up to 1 sample can be of an opposite logic value (glitch) without affecting the output.

The example shown in Consecutive Period and Majority Voting for Input Glitch Filtering using FP = 0 (3 TIMCLK cycles) shows the difference between consecutive period and majority voting formats with a digital filter implemented to capture a CCP input signal of 3 TIMCLK periods.

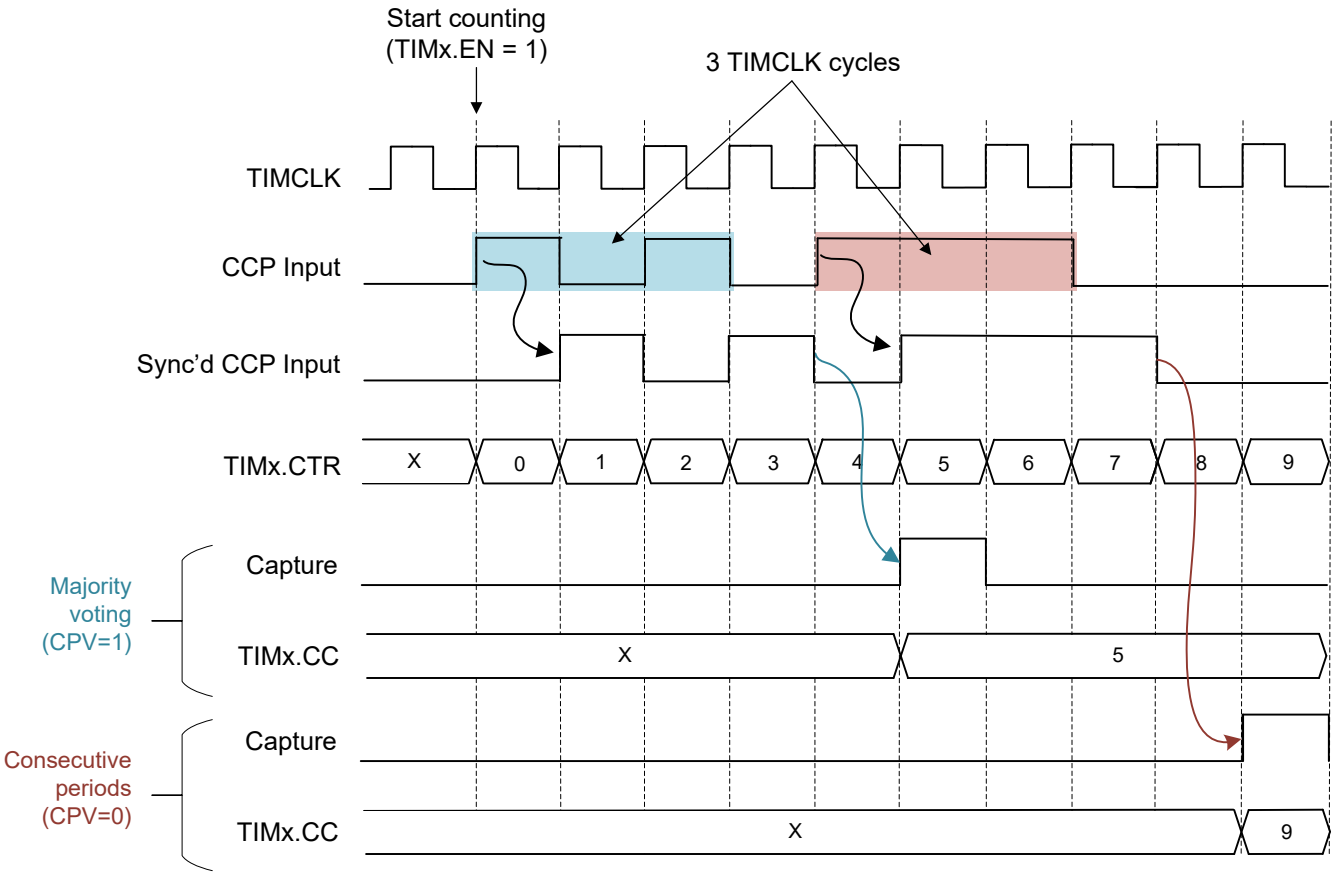


Figure 17-10. Consecutive Period and Majority Voting for Input Glitch Filtering using FP = 0 (3 TIMCLK cycles)

- For Majority Voting, the capture is made with the first CCP Input since the "glitch" period is less than one TIMCLK cycle.
- For Consecutive Period, the capture is made after the CCP Input remains high for 3 full TIMCLK cycles.

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17.2.3.1.1.4 CCP Input Pulse Conditions

The TIMx.CCCTL_xy[0/1] register can control whether each timer instance generates a condition pulse based on the edge or polarity of the CCP input signal or trigger edge. The conditions that can be generated are:

- Advance condition (ACOND)
- Load condition (LCOND)
- Zero condition (ZCOND)
- Capture condition (CCOND)

Advance conditions

By default, the timer advances based on each rising edge of TIMCLK (TIMx.CCCTL_xy[0/1]ACOND = 0h). However, the timer can also advance based off the specified TIMx.CCCTL_xy[0/1].ACOND settings below.

Table 17-6. Advance pulse condition settings (ACOND)

ACOND	Condition
0h	Each rising edge of TIMCLK
1h	Rising edge of CCP or trigger assertion edge
2h	Falling edge of CCP or trigger de-assertion edge
3h	Either edge of CCP or trigger
5h	CCP high or trigger assertion

Load, zero, and capture conditions

Load, zero, and capture condition pulses can be generated based on the LCOND, ZCOND, and CCOND bitfield settings below within the TIMx.CCCTL_xy[0/1] register.

Table 17-7. Load, zero, and capture condition settings (LCOND, ZCOND, CCOND)

LCOND	ZCOND	CCOND	Condition
N/A	N/A	0h	None
1h	1h	1h	Rising edge of CCP or trigger assertion edge
2h	2h	2h	Falling edge of CCP or trigger de-assertion edge
3h	3h	3h	Either edge of CCP or trigger

17.2.3.1.1.5 Counter Control Operation

To specify what CC instance controls the load, zero, or advance event, the CZC, CAC, and CLC bitfields are configured in the TIMx.CTRCTL register.

See Counter Zero Control (CZC) settings for counter zero control settings. For example, if a timer triggers a ZCOND event in Channel 1, then CZC must be set to 1h to register that a ZCOND event in channel 1 triggers the zero event.

Table 17-8. Counter Zero Control (CZC) settings

TIMx.CTRCTL.CZC	Setting
0h	Channel 0 ZCOND event zeroes the TIMx instance
1h	Channel 1 ZCOND event zeroes the TIMx instance

See Counter Load Control (CLC) settings for counter load control settings. For example, if a timer triggers a LCOND event in Channel 1, then CLC must be set to 1h to register that a LCOND event in channel 1 triggers the load event.

Table 17-9. Counter Load Control (CLC) settings

TIMx.CTRCTL.CLC	Setting
0h	Channel 0 LCOND event loads the TIMx instance

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Table 17-9. Counter Load Control (CLC) settings (continued)

TIMx.CTRCTL.CLC	Setting
1h	Channel 1 LCOND event loads the TIMx instance

See Counter Advance Control (CAC) settings for counter advance control settings. For example, if a timer triggers a ACOND event in Channel 1, then CAC must be set to 1h to register that a ACOND event in channel 1 triggers the advance event.

Table 17-10. Counter Advance Control (CAC) settings

TIMx.CTRCTL.CAC	Setting
0h	Channel 0 ACOND event advances the TIMx instance
1h	Channel 1 ACOND event advances the TIMx instance

17.2.3.1.2 Capture Mode Use Cases

Several different use cases can be achieved in capture mode and are discussed in the following sections.

17.2.3.1.2.1 Edge Time Capture

Edge time capture measures the time (in TIMCLK cycles) from the start of the capture operation to the signal edge. The counter is loaded when TIMx is enabled and counts with each TIMCLK period until the CCP edge is detected, which triggers the capture of the timer value and generates a capture event. The capture edge time is equivalent to the difference between the starting value of the counter and the capture value in TIMx.CC_xy[0/1] register.

Edge Time Capture Configuration

1. Set the TIMx.LOAD value.
2. In the CTRCTL register, set the desired counter control settings for:
   a. Counting mode (CM) and counter value after enable (CVAE) (see as described in Section 17.2.2)
   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
3. Set TIMx.CCCTL_xy[0/1].COC = 1 for capture mode.
4. Configure CCP as an input for the CC block by setting respective bit in the CCPD registers. For instance, if TIMx Channel 0 is an input, set CCPD.C0CCP0 = 0.
5. For the corresponding CC block control register (CCCTL_01[0/1]), set CCOND to the corresponding setting to capture events based off the input signal condition (rising and/or falling edge). Additionally, set ZCOND or LCOND depending on the counting mode used.
6. Configure input capture settings in the TIMx.IFCTL_xy[0/1] register as described in Section 17.2.3.1.1 .
7. Enable the counter by setting EN = 1 or waiting for a capture event to occur from the input edge.

Example using up-counting mode for rising edge capture

In up-counting mode starting from zero (CM = 2, CVAE = 2), TIMx can be configured to generate a zero pulse and start the counter from the configured capture event (CCOND) by setting ZCOND to 1.

The expected internal timing for a rising or positive edge time capture in up-counting mode is shown in Figure 17-11.

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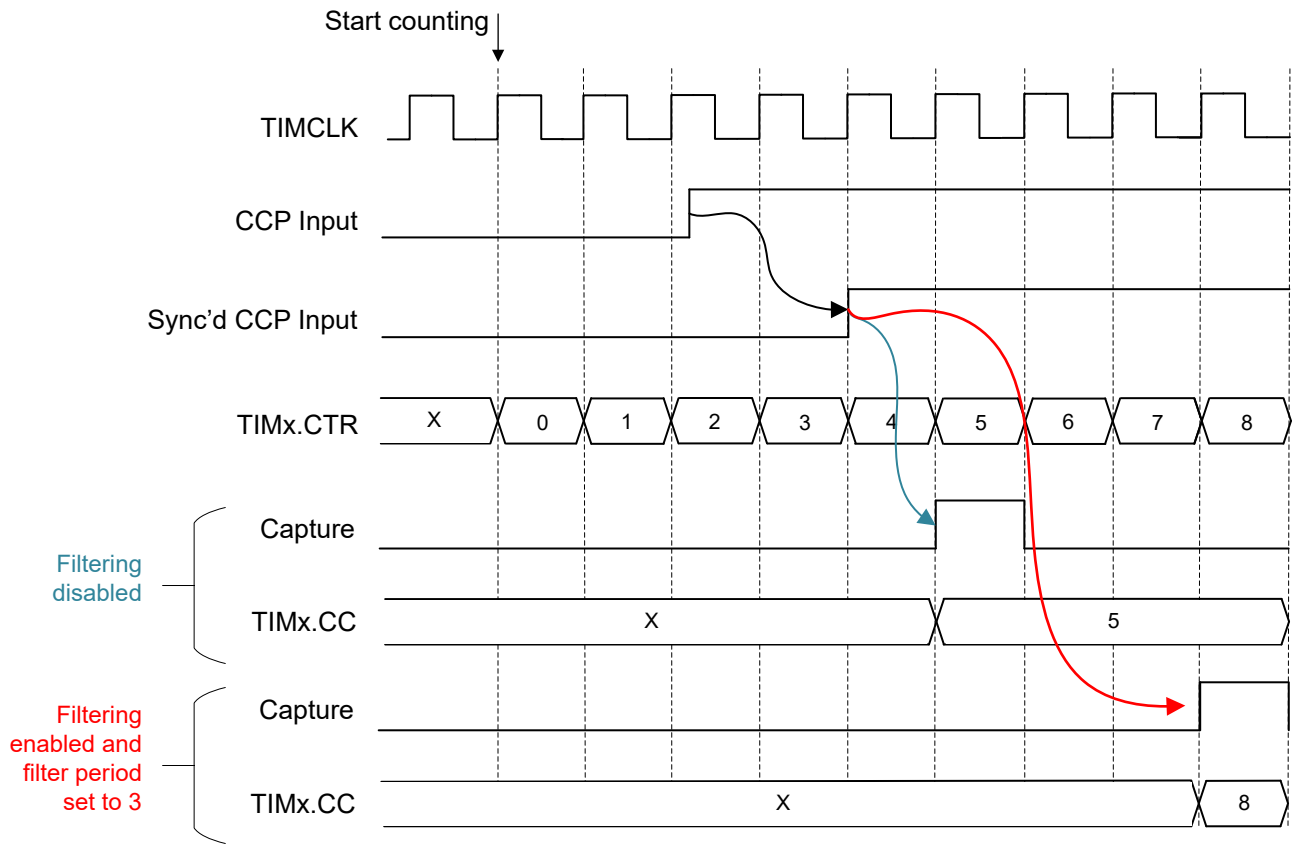


Figure 17-11. Edge Time Capture Mode in Up-Counting Mode, CVAE = 2

17.2.3.1.2.2 Period Capture

Period capture measures the period of a signal on an input CCP in TIMCLK cycles. On each positive (or negative) edge of the CCP input, the TIMx.CTR value is both captured into the TIMx.CC register to generate a capture event. The period capture time is equivalent to the difference between the starting value of the counter generated to the capture event, or time between reoccurring capture events for a periodic input signal.

Period Capture Configuration

1. Set the TIMx.LOAD value.
2. In the CTRCTL register, set the desired counter control settings for:
   a. Counting mode (CM) and counter value after enable (CVAE) (see as described in Section 17.2.2)
   b. Advance (CAC) to specify what condition controls advancing the counter
   c. Repeat or one-shot mode (REPEAT)
3. Set TIMx.CCCTL_xy[0/1].COC = 1 for capture mode.
4. Configure CCP as an input for the CC block by setting respective bit in the CCPD registers. For instance, if TIMx Channel 0 is an input, set CCPD.C0CCP0 = 0.
5. For the corresponding CC block control register (CCCTL_01[0/1]),
   a. Set CCOND to the corresponding setting to capture events based off the input signal condition (rising and/or falling edge)
   b. Set ZCOND or LCOND depending on the counting mode used
6. Configure input capture settings in the TIMx.IFCTL_xy[0/1] register as described in Section 17.2.3.1.1 .
7. Enable the counter by setting EN = 1 or waiting for a capture event to occur from the input edge.

Example using up-counting mode for rising-edge period capture

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In up-counting mode starting from zero (CM = 2, CVAE = 2), TIMx channel 0 can be configured to generate a capture event from a rising edge input by setting CCOND = 1h. After enabling the counter, when a rising edge input is detected, the counter will capture the counter value in TIMx.CC. After the capture event, set the TIMx.LOAD value back to 0 to reset the timer counter for the periodic CCP input signal.

The expected internal timing for a period capture in up-counting mode using two rising edges is shown in Figure 17-11.

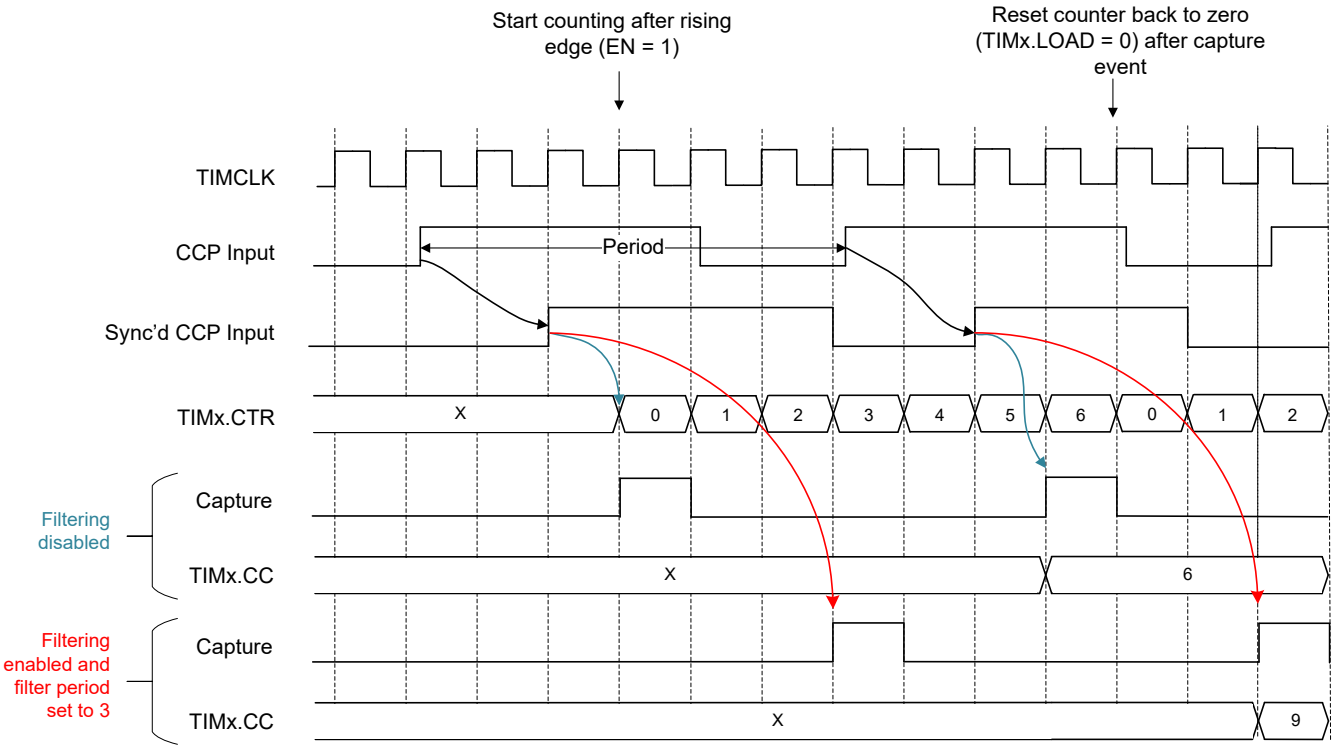


Figure 17-12. Period Capture Mode in Up-Counting Mode, CVAE = 2

17.2.3.1.2.3 Pulse Width Capture

Pulse width capture measures the high-time of a signal on CCP. The high time is the number of TIMCLK periods from rising edge to falling edge of the CCP input, and is useful for applications such as measuring the duty cycle of an PWM input signal. The counter is loaded at the positive edge and captured at the negative edge (capture event is generated).

Pulse-Width Capture Configuration

1. Set the TIMx.LOAD value.
2. In the CTRCTL register, set the desired counter control settings for:
   a. Counting mode (CM) and counter value after enable (CVAE) (see as described in Section 17.2.2)
   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
3. Set TIMx.CCCTL_xy[0/1].COC = 1 for capture mode.
4. Configure CCP as an input for the CC block by setting respective bit in the CCPD registers. For instance, if TIMx Channel 0 is an input, set CCPD.C0CCP0 = 0.
5. For the corresponding CC block control register (CCCTL_01[0/1]), set CCOND to the corresponding setting to capture events based off the input signal condition (rising and/or falling edge). Additionally, set ZCOND or LCOND depending on the counting mode used.
6. Configure input capture settings in the TIMx.IFCTL_xy[0/1] register as described in Section 17.2.3.1.1 .

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7. Enable the counter by setting EN = 1 or waiting for a capture event to occur from the input edge.

Example using up-counting mode for pulse width capture

In up-counting mode starting from zero (CM = 2, CVAE = 2), TIMx channel 0 can be configured to generate a zero pulse and start the counter from the configured capture event (CCOND) by setting ZCOND to 1. To start the counter, a load condition can be triggered from the CCP rising edge input by setting LCOND = 1.

The expected internal timing for a pulse width capture in up-counting mode using a rising and falling edge is shown in Figure 17-11.

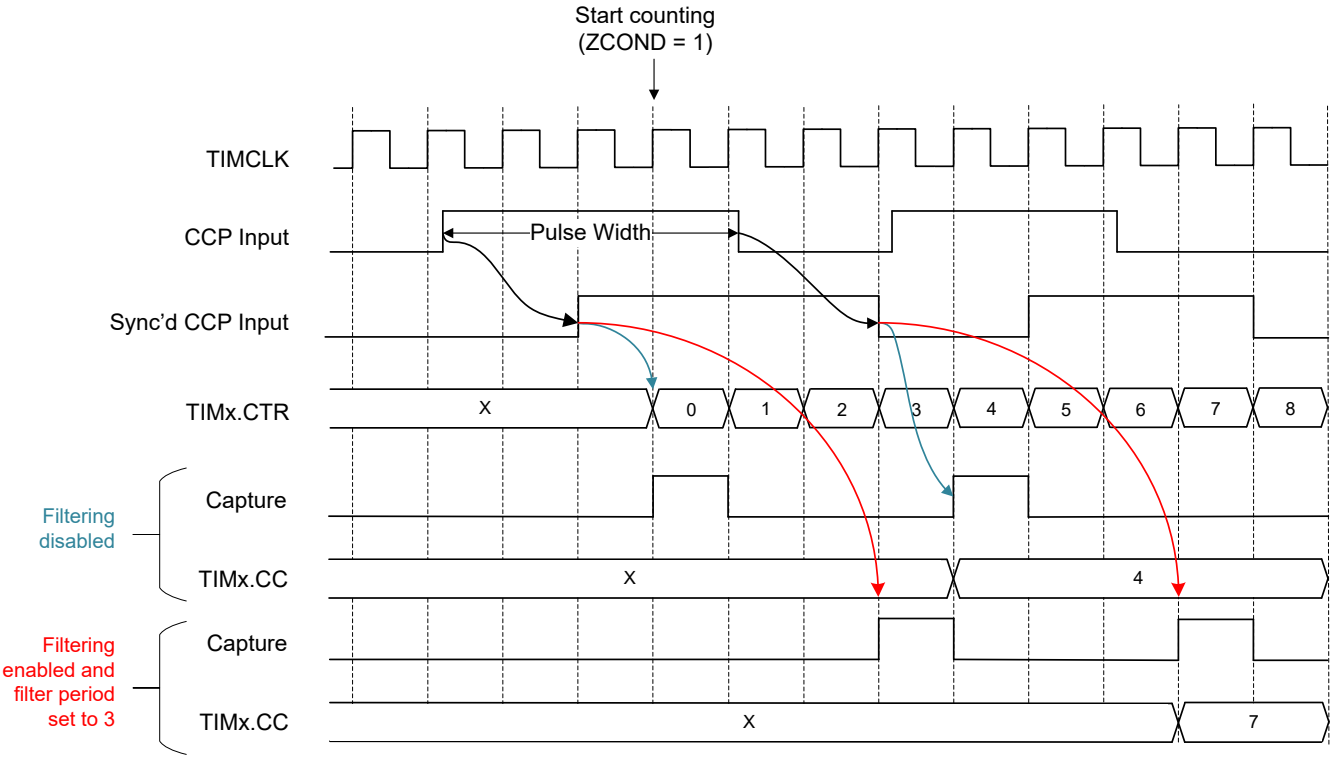


Figure 17-13. Pulse-Width Capture Mode

17.2.3.1.2.4 Combined Pulse Width and Period Time

Using two capture registers can combine pulse-width and period capture of a single input waveform. The input signal can be externally connected to CCP channel 0, and the IFCTL_01[1] register can be configured to have the input connected to CCP channel 1 internally so capture register 0 (TIMx.CC0) captures pulse width and capture register 1 (TIMx.CC1) captures period. The expected internal timing for combined pulse-width and period capture is shown in Figure 17-14.

Pulse-Width and Period Capture Configuration

1. Set the TIMx.LOAD value.
2. In the CTRCTL register, set the desired counter control settings for:
   a. Counting mode (CM) and counter value after enable (CVAE) (see as described in Section 17.2.2)
   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
3. Set TIMx.CCCTL_xy[0/1].COC = 1 for capture mode for each CC channel.
4. Configure CCP as an input for each CC block by setting respective bits in the CCPD register. For instance, if TIMx Channel 0 is an input, set CCPD.C0CCP0 = 0.
5. For the corresponding CC block control register (CCCTL_01[0/1]),

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a. Set CCOND to the corresponding setting to capture events based off the input signal condition (rising and/or falling edge)
b. Set ZCOND or LCOND depending on the counting mode used.

6. Configure input capture settings in the TIMx.IFCTL_xy[0/1] register as described in Section 17.2.3.1.1 .
7. Enable the counter by setting EN = 1 or waiting for a capture event to occur from the input edge.

Example using pulse-width and period time capture

In up counting mode, TIMx can be configured to generate a zero pulse and start the counter from the configured capture event (CCOND) by setting ZCOND to 1.

The expected internal timing for a pulse-width and period capture in up-counting mode using two CC blocks is shown in Figure 17-11.

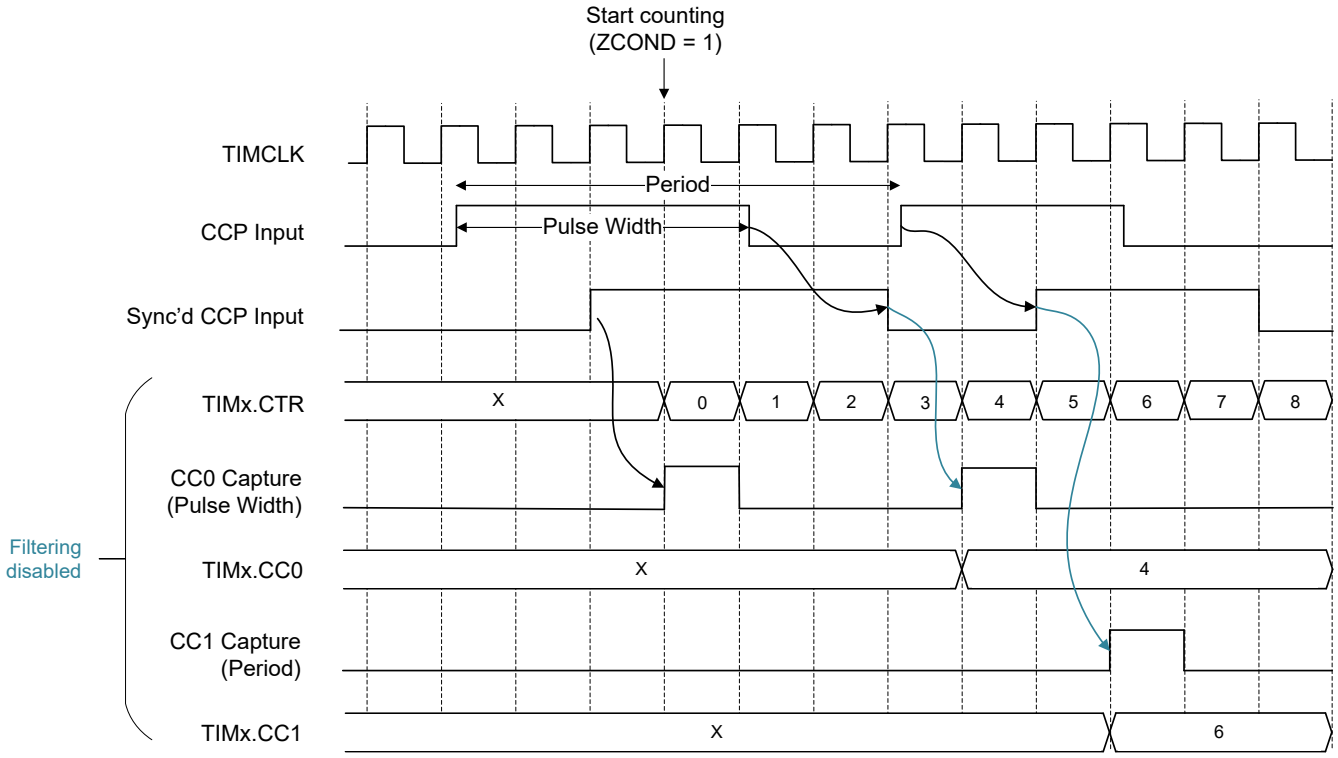


Figure 17-14. Combined Pulse-Width and Period Capture

17.2.3.2 Compare Mode

Compare mode is selected when TIMx.CCCTL_xy[0/1].COC = 0. Compare mode is used to generate a compare event to output PWM output signals at specific time intervals. Compare events can be used to generate a timing base internally or generate a PWM output with specific profiles using active, inactive, or toggle action behaviors, and optional deadband insertion.

Many types of compare mode events can be generated based on the configuration of the CC action register CCACT_xy[0/1]:

- Compare events: occurs for a CC channel when TIMx.CTR counts up (CCU) or down (CCD) to the value in TIMx.CC_xy[0/1]
- Secondary compare events: occurs when a secondary CCx block compare up (CC2U) or down (CC2U) is configured for another CCx block's CCU event or CCD event, respectively. This enables more flexible output generation from other external events such as comparator outputs or fault signals. It can be useful for real-time control applications, like digital power or motor control.

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Table 17-11 shows the types of compare mode events that can be generated and conditions to generate the events.

Table 17-11. Compare Mode Events

Event	Name	Event Condition
CCDn (n = CC channel)	Capture/compare down event	When timer is counting down, TIMx.CTR = TIMx.CC_xy[0/1]
CCUn (n = CC channel)	Capture/compare up event	When timer is counting up, TIMx.CTR = TIMx.CC_xy[0/1]
CC2Dn (n = CC channel)	Secondary capture/compare down event	Occurs when CC2SELD is configured for the source of the CCDn event
CC2Un (n = CC channel)	Secondary capture/compare up event	Occurs when CC2SELU is configured for the source of the CCUn event

Note

Look at the device specific data sheet to check how many CC channels are available in each TIMx instance on the device.

17.2.3.2.1 Edge Count

In addition to event or PWM output generation, compare mode can also be used for input signal edge counting to determine when a number of edges has been detected. In edge count operation, a CCP input edge can advance the counter based on the ACOND condition. The counter register is initialized with the starting value, and the number of detected CCP input edges at any time can increment or decrement depending on the counting mode configuration. The user can count rising edges, falling edges, or both edges by configuring the CCOND value.

Edge Count Configuration

1. Set TIMx.CCCTL_xy[0/1].COC = 0 for compare mode.
2. Optionally set the corresponding TIMx.CC_xy[0/1] to a compare value to generate a compare interrupt when the counter reaches this value.
3. In the CTRCTL register, set the desired counter control settings for:
   a. Counting mode (CM) and counter value after enable (CVAE) (see as described in Section 17.2.2)
   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
4. Set ACOND to a setting to advance the counter based on the input edge polarity.
5. Configure input capture settings as described in Section 17.2.3.1.1 , if desired.
6. Enable the counter by setting EN = 1.

Example using edge count operation using up-counting mode

In up-counting mode starting from zero (CM = 2, CVAE = 2), the expected internal timing for rising edge count operation to increment the counter is shown in Figure 17-15.

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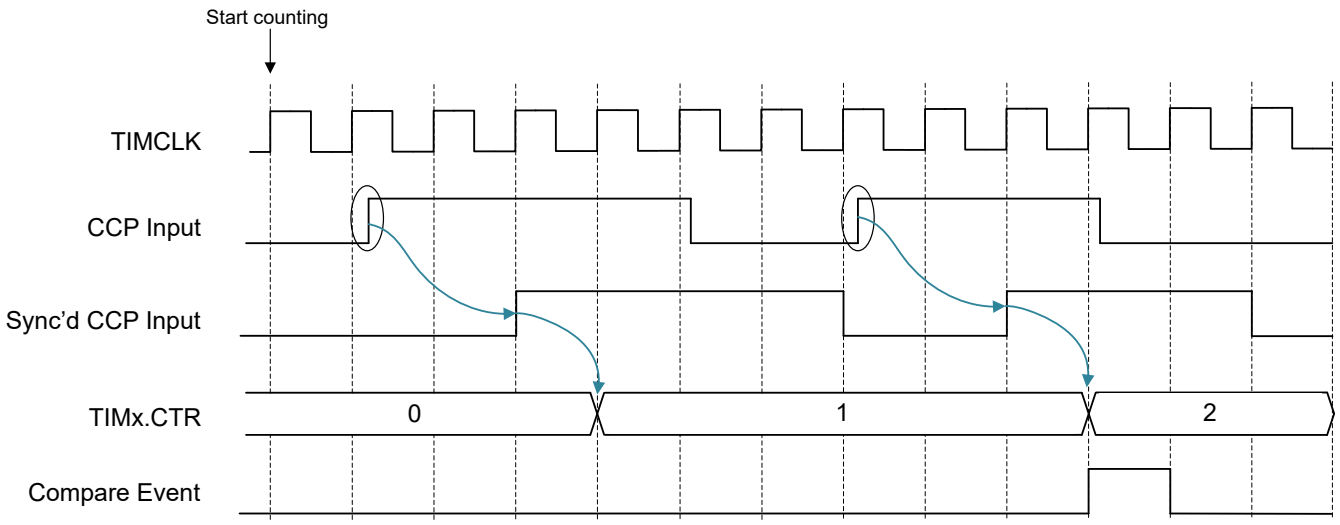


Figure 17-15. Edge Count Operation to Generate Compare Event (TIMx.CC = 2)

17.2.4 Shadow Load and Shadow Compare

Some timer modules have a shadow load and shadow compare register feature which gives the user the flexibility of holding the update of load and CC values until a certain event occurs. This is useful in timing-critical applications where PWM control signals need to be updated with correct timings, such as duty cycle updates. Refer to the timer features for specific configurations of the TIMx modules.

Note

See Section 17.1.1 and the device-specific data sheet for TIMx instances that support Shadow Load and Shadow Compare.

17.2.4.1 Shadow Load (TIMG4-7)

On shadow-load capable timers, the shadow load feature allows holding the update of load values until a zero event occurs. To enable shadow loading, set the TIMx.GCTL.SHDWLDEN bit while the timer is enabled (EN = 1).

If the TIMx module has a shadow load feature, there is an internal shadow register for the load value (TIMx.LOAD). The shadow register will update the load value at a zero event as shown in Figure 17-16.

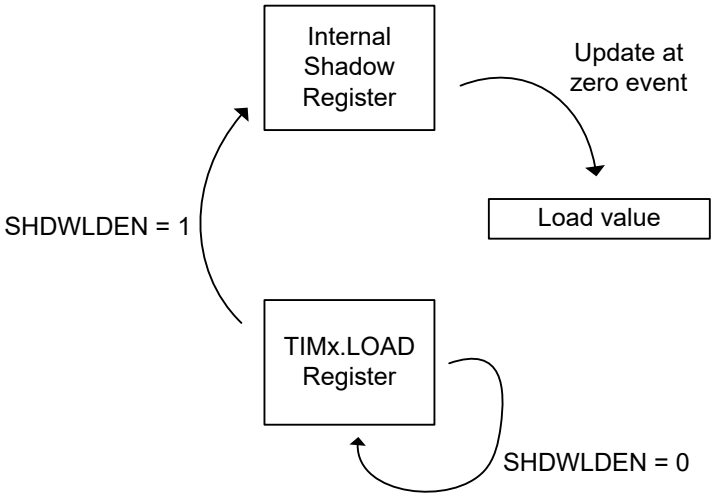
Note

On shadow-load capable timers, SHDWLDEN must be set or else the load value will not update.

If the timer instance does not have shadow load capability (standard timer), the load value will update immediately when TIMx.LOAD is written to.

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Shadow-load capable timers update the load value from the internal shadow register when:
- TIMx.CTRCTL.EN = 1
- GCTL.SHDWLDEN = 1
- Available for TIMG4-7, TIMAx



Standard timers update the load value from TIMx.LOAD immediately when:
- TIMx.CTRCTL.EN = 1
- Available for TIMG0-3, TIMG8-14

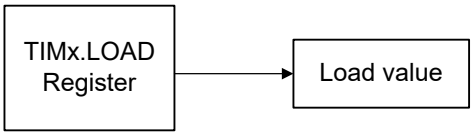


Figure 17-16. Load value updates for TIMx instances when EN=1

Note

To update the load value for shadow load capable timers, the timer must be disabled before changing the TIMx.LOAD value.

When TIMx.GCTL.SHDWLDEN = 1, load values update at zero events for all counting modes. Consult the counting mode operations below to determine if a shadow load is needed:

- In down-counting modes, since TIMx.LOAD value is updated when a zero event occurs, a shadow load is not needed in these modes.
- In up/down counting mode, TIMx.LOAD is compared with the counter value to determine if the peak is reached and when to start to counting down. A shadow load is necessary to ensure that TIMx counts up to the load value before the zero event, or else the load value can update immediately and cause incorrect timings.
- In up-counting mode, the timer counts to TIMx.LOAD. A shadow load is necessary to ensure that TIMx counts up to the load value before the zero event, or else the load value can update immediately and cause incorrect timings.

Figure 17-17 shows an example of how shadow load and shadow compare takes effect at the zero event for both the TIMx.LOAD and TIMx.CC value in up/down counting mode.

17.2.4.2 Shadow Compare (TIMG4-7, TIMG12-13)

When shadow compare is enabled for updating the capture/compare register (TIMx.CC), the value written to the respective compare register is first stored into a shadow compare register and then transferred to the compare register at different events configured by setting the TIMx.CCCTL_xy[0/1].CCUPD bits.

Additionally, the capture/compare action register (TIMx.CCACT) has the ability to update the action at different events configured by setting the TIMx.CCCTL_xy[0/1].CCACTUPD bits.

Table 17-12 shows the settings for configuring when shadow compare and actions occur at different events.

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Table 17-12. Shadow Compare and Action Update Behavior

Bit Field	Value	Description/Comment
CCUPD / CCACTUPD	0	The value written to TIMx.CC register take effect immediately.
	1	The value written to the TIMx.CC register is stored in a shadow compare register and gets transferred to the TIMx.CC register in the TIMCLK cycle following a zero event (TIMx.CTR value equals 0).
	2	The value written to the TIMx.CC register is stored in a shadow compare register and gets transferred to the TIMx.CC register in the TIMCLK cycle following a compare (down) event (TIMx.CTR value equals TIMx.CC)
	3	The value written to the TIMx.CC register is stored in a shadow compare register and gets transferred to the TIMx.CC register in the TIMCLK cycle following a compare (up) event (TIMx.CTR value equals TIMx.CC)
	4	The value written to the TIMx.CC register is stored in a shadow compare register and gets transferred to the TIMx.CC register in the TIMCLK cycle following a zero or load event (TIMx.CTR value equals 0 or TIMx.CTR equals TIMx.LOAD). **Note: this update mechanism is defined for use only in up/down counting mode.**
	5	The value written to the TIMx.CC register is stored in a shadow compare register and gets transferred to the TIMx.CC register in the TIMCLK cycle following a zero event and the repeat count equaling zero (TIMx.CTR value equals 0)
	6	The value written to the TIMx.CC register is stored in a shadow compare register, and gets transferred to the TIMx.CC register in the TIMCLK cycle following a trigger pulse. See Section 17.2.6 .

Figure 17-17 shows an example of how shadow load and shadow compare takes effect at the zero event for both the TIMx.LOAD and TIMx.CC value in up/down counting mode.

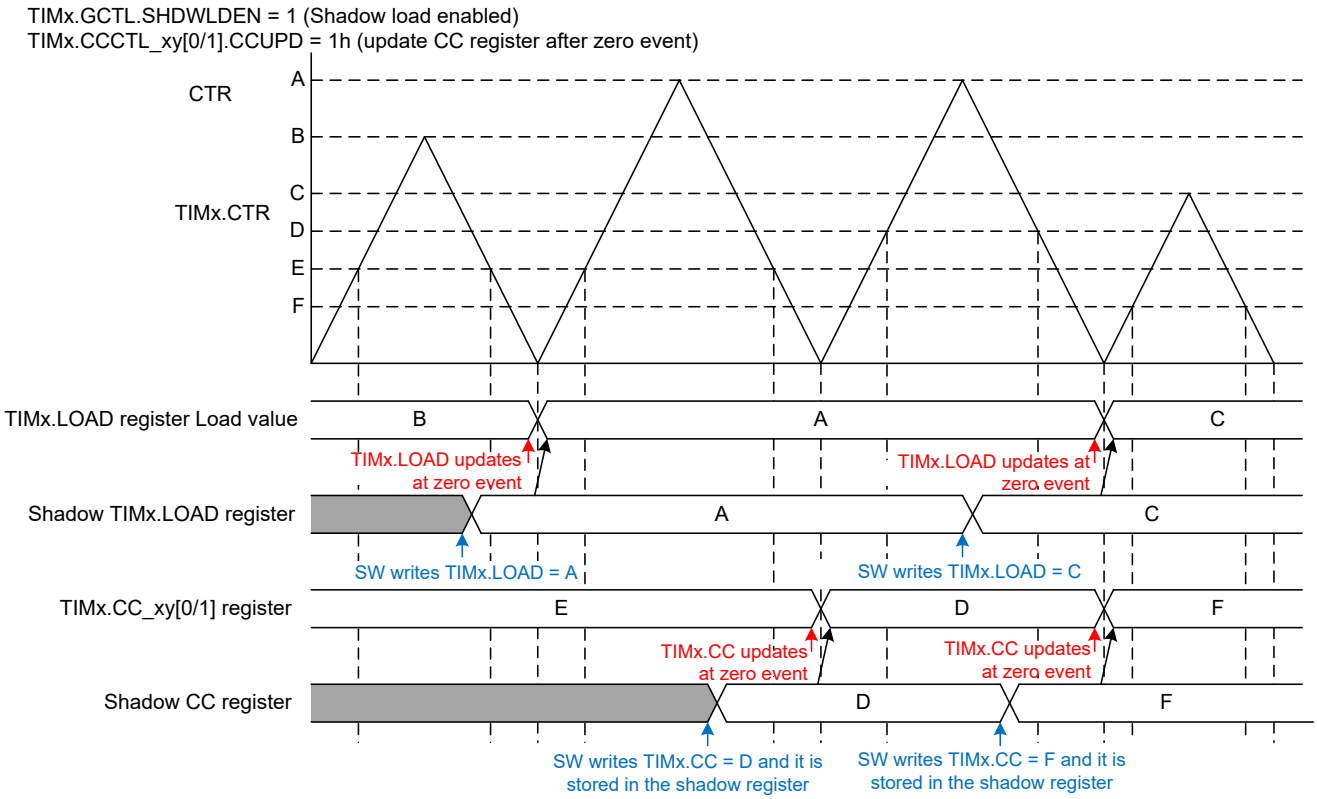


Figure 17-17. Shadow Load and Shadow Compare Taking Effect at Zero Event in Up/Down Mode

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17.2.5 Output Generator

The output signal generation unit can be used with the counter and capture/compare modules to generate desired pulse-width modulation (PWM) output waveforms, event signals, synchronized capture inputs, or the counter direction. Many output waveforms are generated from counter events (load, zero, counter direction) and a compare match within the capture/compare block.

The key registers for generation of output signals are:

- **LOAD**: the contents of this register are copied to the counter (TIMx.CTR) on any operation designated to do a "load". This value is also used to compare with the counter value for generating a "Load Event" that can be used for interrupt, trigger, or signal generator actions.
- **CCPD:** this register configures the direction of the CCP pins as inputs or outputs.
- **CC_xy[0/1]**: this is a register used as a compare value to the current counter to create an match event.
- **CTRCTL**: this register provides control over the counter operation in different conditions.
- **CCCTL_xy[0/1]**: this register controls the operations of the respective CC registers and the counter
- **OCTL_xy[0/1]**: this register controls the output of the capture-compare portion of the counter. This includes the ability to select the source of what is driven out along with initial condition values and final inversion options.
- **CCACT_xy[0/1]**: this register controls the actions of the signal generator of the capture-compare portion based on the events created in the counter block, the capture and compare block, and debug events.
- **ODIS:** this register disables the output signal selected by OCTL.CCPO (before conditional inversion) to allow software the ability to hold the CCP output low during configuration or shutdown.

Figure 17-18 shows the TIMx output block diagram.

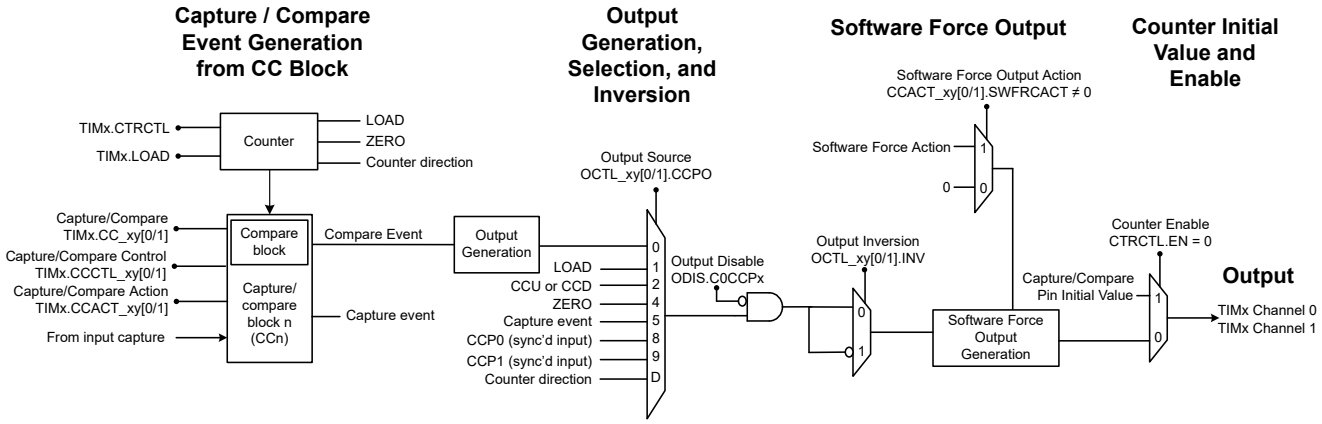


Figure 17-18. Output Connection for TIMx

Signal Generator Actions

Signal Generator Actions from Compare Event shows the types of signal generator actions capable by the output generator. Signal generator actions are configured in the CCACT_xy[0/1] register for zero, load, and compare events. For types of compare events, see Compare Mode Events.

Table 17-13. Signal Generator Actions from Compare Event

Value	Action
0h	Event is disabled and a lower priority event is selected if asserting
1h	CCP output value is set high
2h	CCP output value is set low
3h	CCP output value is toggled

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17.2.5.1 Configuration

There are five stages to configuring output signal generation in TIMx devices:

- Counter and CC Block Event Generation
- Output Generation, Selection and Inversion
- Software Force Output
- Counter Initial Value and Enable

Counter and CC Block Event Generation

The counter block contains the counter and produces a load event (L), zero event (Z), and direction of counting based on the counting mode used.

The CC blocks contain the CC register and can generate two types of output signals: compare match events and capture events. Please see Table 17-11 for the compare events that can be generated.

Output Generation, Selection and Inversion

The TIMx.CCACT register specifies the waveform generation of a CCP output depending on the counting mode and counter compare actions.

TIMx.OCTL_xy[0/1].CCPO controls the CCP output selection from the output generation unit, counter events, compare events, capture events, fault events, or signal inputs. The output disable register (ODIS) can optionally disable the CCP output to optionally hold the CCP output low during configuration or shutdown. TIMx.OCTL_xy[0/1].INV controls final inversion options.

Software Force Output

The output of the signal generator can be overwritten in software by setting CCCTL_xy[0/1].SWFRCACT to a nonzero setting.

For more information, see Section 17.2.5.3 .

Counter Compare Initial Value and Enable

To specify an initial value for the CCP output while the counter is disabled, set OCTL_xy[0/1].CCPIV to 0 for a low value or 1 for a high value. This is useful for applications where CCP outputs need to be in a default state before enabling the counter.

To enable the counter, set TIMx.CTRCTL.EN to 1.

17.2.5.2 Use Cases

Several different use cases can be achieved with the output generator and are discussed in the following sections.

17.2.5.2.1 Edge-Aligned PWM

To generate edge-aligned PWMs, TIMx can be configured for up- or down-counting mode. The waveform uses load, zero, and compare events to drive the CCPx output high or low depending on the configuration settings of the compare/capture block and counter.

In TIMCLK cycles, the PWM period is (TIMx.LOAD + 1) and the duty cycle is 1 - (TIMx.CC_xy[0/1] / TIMx.LOAD) for down counting mode and (TIMx.CC_xy[0/1] / TIMx.LOAD) for up counting mode.

Edge-Aligned PWM Configuration

To generate edge-aligned PWMs using compare match events from the counter:

1. In the TIMx.CTRCTL register, set the desired counter control settings for:
   a. Up-counting (CM = 2) or down-counting mode (CM = 0) and counter value after enable (CVAE) (see as described in Section 17.2.2)

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   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
2. Set the TIMx.LOAD value to configure the PWM period.
3. Set the TIMx.CC_xy[0/1] value to configure the duty cycle.
4. Set TIMx.CCCTL_xy[0/1].COC = 1 for compare mode.
5. Configure CCP as an output for the CC block by setting respective bit in the CCPD registers. For instance, if TIMx Channel 0 is an output, set CCPD.C0CCP0 = 1.
6. In TIMx.CCACT_xy[0/1], set the CCP output action settings for compare events, zero events, load events, or software force action.
7. In TIMx.OCTL_xy[0/1], set CCPO = 0 to select the signal generator output.
8. Enable the corresponding CCP output by setting ODIS.C0CCPn to 1 for the corresponding counter n.
9. Configure polarity of the signal using the CCPOINV bit, and configure CCPIV to specify the CCP output state while disabled.
10. Enable the counter by setting TIMx.CTRCTL.EN = 1.

Example using edge-aligned PWM in down-counting mode

A typical 2-channel edge-aligned PWM generation for down-counting mode is shown in Figure 17-19 with the following edge-aligned PWM output waveforms:

- CCP0 output generates:
  - High pulse-width from TIMx.LOAD to TIMx.CC0 value (LACT = 1h)
  - Low pulse-width from TIMx.CC0 value to zero (CDACT = 2h)
- CCP1 output generates:
  - High pulse-width from TIMx.LOAD to TIMx.CC1 value (LACT = 1h)
  - Low pulse-width from TIMx.CC1 value to zero (CDACT = 2h)

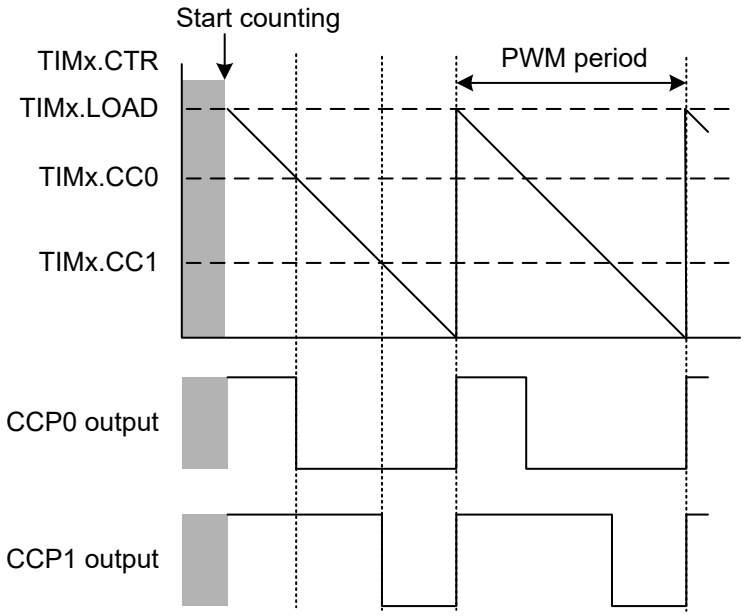


Figure 17-19. Edge-Aligned PWM Signals in Down-Counting Mode

Example using edge-aligned PWM in up-counting mode

A typical 2-channel edge-aligned PWM generation for up-counting mode is shown in Figure 17-19 with the following edge-aligned PWM output waveforms:

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- CCP0 output generates:
  - High pulse-width from zero to TIMx.CC0 value (ZACT = 1h)
  - Low pulse-width from TIMx.CC0 value to TIMx.LOAD (CUACT = 2h)
- CCP1 output generates:
  - High pulse-width from zero to TIMx.CC1 value (ZACT = 1h)
  - Low pulse-width from TIMx.CC1 value to TIMx.LOAD (CUACT = 2h)

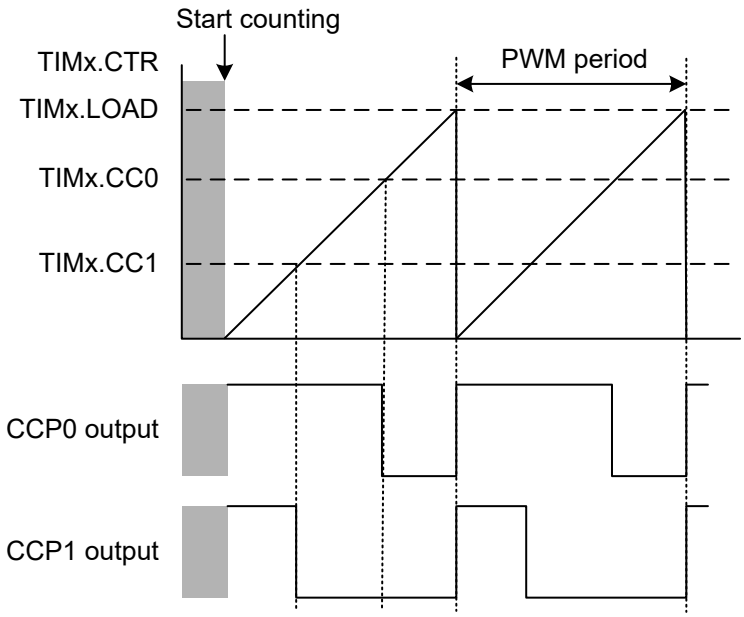


Figure 17-20. Edge-Aligned PWM Signals in Up-Counting Mode

17.2.5.2.2 Center-Aligned PWM

To generate center-aligned PWMs, TIMx is configured for up/down counting mode and the TIMx.LOAD value contains the half-period. The waveform uses up compare events and down compare events to drive the CCPx output high or low depending on the configuration settings of the compare/capture block and counter.

In TIMCLK cycles, the PWM period is (2 * TIMx.LOAD) and the duty cycle is 1 - (TIMx.CC_xy[0/1] / TIMx.LOAD).

Center-Aligned PWM Configuration

To generate center-aligned PWMs using compare match events from the counter:

1. In the TIMx.CTRCTL register, set the desired counter control settings for:
   a. Up/down counting mode (CM = 1) and counter value after enable (CVAE) (as shown in Section 17.2.2)
   b. Zero (CZC), advance (CAC), and load control (CLC) to specify what condition controls zeroing, advancing, or loading the counter
   c. Repeat or one-shot mode (REPEAT)
2. Set the TIMx.LOAD value to configure the PWM period.
3. Set the TIMx.CC_xy[0/1] value to configure the duty cycle.
4. Set TIMx.CCCTL_xy[0/1].COC = 1 for compare mode.
5. Configure CCP as an output for the CC block by setting respective bit in the CCPD registers. For instance, if TIMx Channel 0 is an output, set CCPD.C0CCP0 = 1.
6. In TIMx.CCACT_xy[0/1], set the CCP output action settings for compare events, zero events, load events, or software force action.
7. In TIMx.OCTL_xy[0/1], set CCPO = 0 to select the signal generator output.
8. Enable the corresponding CCP output by setting ODIS.C0CCPn to 1 for the corresponding counter n.
9. Configure polarity of the signal using the CCPOINV bit, and configure CCPIV to specify the CCP output state while disabled.

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10. Enable the counter by setting TIMx.CTRCTL.EN = 1.

Example using center-aligned PWM in up/down counting mode

A typical 2-channel center-aligned PWM generation using up/down counting mode is shown in Figure 17-21 with the following center-aligned PWM output waveforms:

- CCP0 output generates:
  - High pulse-width from TIMx.CC0 compare up event to TIMx.CC0 compare down event (CUACT = 1h)
  - Low pulse-width from TIMx.CC0 compare down event to TIMx.CC0 compare up event (CDACT = 2h)
- CCP1 output generates:
  - High pulse-width from TIMx.CC0 compare up event to TIMx.CC0 compare down event (CUACT = 1h)
  - Low pulse-width from TIMx.CC0 compare down event to TIMx.CC0 compare up event (CDACT = 2h)

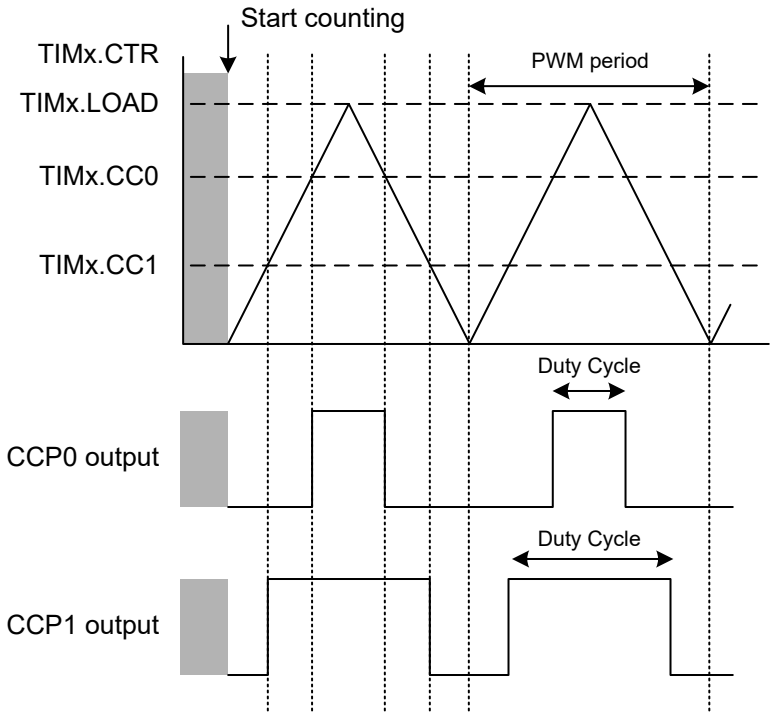


Figure 17-21. Center-Aligned PWM

17.2.5.3 Forced Output

Each output channel signal can be forced to a high or low level directly by software, independently of any comparison between the compare register and the counter. A shadow register exists to ensure the forced output action occurs at the end of the timer period.

The output of the CCP channel can be forced to high or low by setting the SWFRCACT bit in the TIMx.CCACT_xy[0/1] register.

Force Output Action Configuration shows the software force output action configuration options.

Table 17-14. Force Output Action Configuration

Bit Field	Value	Description/Comment
SWFRCACT	0	No forced output. Output is directly from the signal generation block.
	1	Force output high
	2	Force output low

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17.2.6 Synchronization With Cross Trigger

When using a main-secondary timer configuration by connecting multiple timers together, the cross-trigger feature can instruct multiple timer modules in the same power domain or across different power domains using the event fabric to start counting simultaneously.

Cross-triggers can be enabled using software, compare events from other timer instances, zero or load events, or generic subscriber events. Some applications may require more than one counter block that can be simultaneously started across the same power domain (such as TIMA0 and TIMA1) or different power domains (such as TIMA0 and TIMG0).

This configuration uses cross triggers from a main timer module as the input trigger condition for the secondary timers. The timer cross trigger is essentially the combined logic of the hardware and software conditions that control the EN bit in the TIMx.CTRCTL register.

The cross triggers that are outputted from the main timer are connected to the external trigger input of other secondary timer modules. As shown in Figure 17-22, TIMGx is the main timer and TIMAx is the secondary timer that will be cross triggered in the configuration example.

Note

For power domains and cross trigger selection sources enabled for timer instances, refer to the device-specific data sheet.

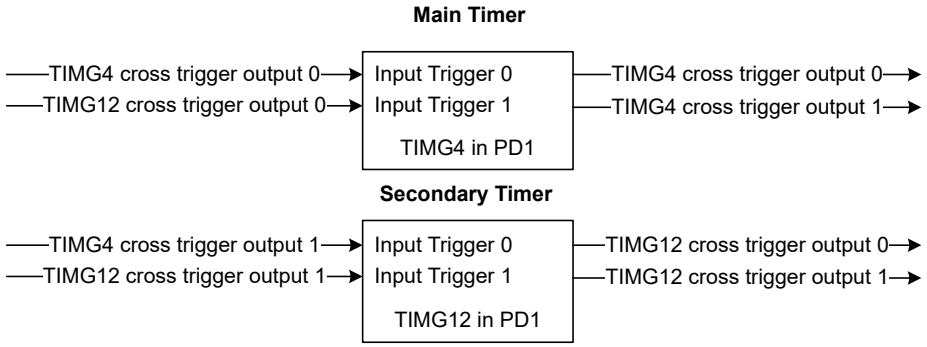


Figure 17-22. Cross Trigger Connections for Main Timer (TIMGx) and Secondary Timer (TIMAx) in Power Domain 1

17.2.6.1 Main Timer Cross Trigger Configuration

The following steps are used to configure the main timer cross trigger (which is TIMGx in this example):

1. Configure the main timer (which triggers other secondary timers) for the desired function, such as PWM output generation or using compare mode, to trigger other peripherals. See Section 17.2.5 for how to configure for PWM generation.
2. Select which cross trigger output needs to be generated. For example, in Figure 17-22, TIMGx cross trigger 1 can be used to trigger TIMAx and TIMGx cross trigger 0 can be used to trigger itself.
3. Enable the cross trigger output function by setting TIMx.CTTRIGCTL.CTEN bit to 1.
4. Choose how to trigger the start of these connected timers, which can be a software trigger or hardware trigger from a subscriber port, zero, load, or compare event.
   a. For a software event trigger, set the TIMx.CTTRIG.TRIG bit.
   b. For a hardware trigger event, select the source for the trigger using TIMx.CTTRIGCTL.EVTCTTRIGSEL and enable the hardware trigger by setting TIMx.CTTRIGCTL.EVTCTEN.

Figure 17-23 shows the connection logic and registers.

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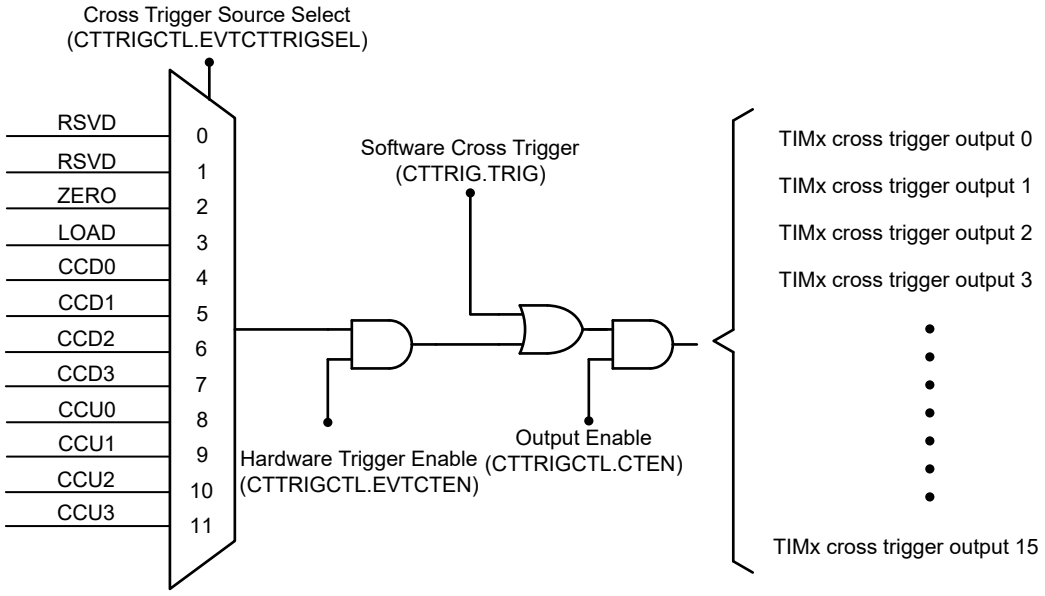


Figure 17-23. Main Timer Cross Trigger Output Configuration

17.2.6.2 Secondary Timer Cross Trigger Configuration

The following steps are used to configure the secondary timer cross trigger (which is TIMAx in this example):

1. Configure the secondary timer (triggered by the main timer) for the desired function for this timer, such as PWM output generation or using compare mode, to trigger other peripherals. See Section 17.2.5 for how to configure for PWM generation.
2. Select which input trigger to use according to the device-specific data sheet. Using the example connection in Figure 17-22, TIMAx must be triggered by TIMGx and the cross trigger output 1 of TIMGx is connected to input trigger 0 of TIMAx. Therefore, select input trigger 0 of TIMAx by setting TIMA.TSEL.ETSEL bit to 0.
3. Enable the input trigger function by setting the TIMA.TSEL.TE bit to 1.
4. Set TIMAx.IFCTL_01[0].ISEL = 3 and TIMAx.IFCTL_01[1].ISEL = 3 to select the trigger as the input source.
   a. For a center-aligned PWM, set the TIMA.CCCTL_01[0].ZCOND and TIMA.CCCTL_01[1].ZCOND bits to 1 to use a trigger assertion edge for a zero event.
   b. For an edge-aligned PWM, set the TIMA.CCCTL_01[0].LCOND and TIMA.CCCTL_01[1].LCOND bits to 1 to use the trigger assertion edge for a load event.
5. The TIMx.CTRCTL.EN bit is set as the result of an LCOND or ZCOND condition being met, and the counter value changes to the load value or zero value, respectively.

As the main timer TIMGx must also trigger itself, complete the previous configuration steps for TIMAx to trigger TIMGx itself.

Figure 17-24 shows the logic connection.

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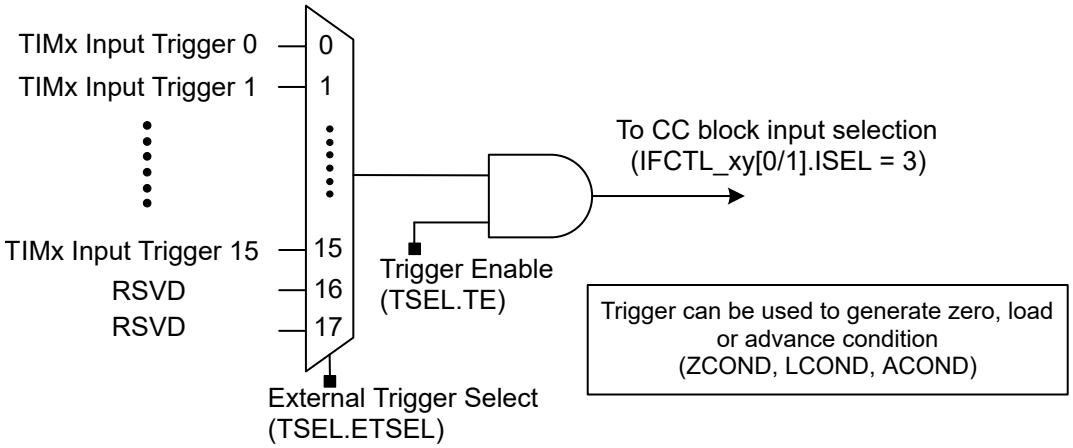


Figure 17-24. Secondary Timer Cross Trigger Input Configuration

Note

Refer to "TIMx Cross Trigger Map" in the device-specific data sheet for enabled cross trigger mapping using the ETSEL bit. For instance, if the timer instances of a device all use trigger input 0 (TRIG0) to cross trigger other timers, then only TRIG0 can be used to cross trigger other instances.

17.2.7 Low Power Operation

For detailed information on the low power modes in terms of available clock source and behaviors, refer to *Power Domains*.

Timer modules in power domain PD0 can be active and configured to continue counting in all power modes except SHUTDOWN mode. See *Power Domains* for the available clock sources in each low-power mode. The user needs to configure the proper clock to source the timer in low-power mode.

Timer modules in power domain PD1 can only be active in RUN and SLEEP modes. When the system goes to STOP or STANDBY mode, the timer modules will be forced to a disabled state and resume when the systems moves back to RUN or SLEEP modes.

17.2.8

Note

MFCLK refers to a 4MHz fixed frequency clock that is not configured on AM13E230x devices. Please disregard any mention of MFCLK within the following registers.

17.3 TIMx Interrupts & Triggers

17.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 17-15. CPU Interrupts Triggered by TIMx

NVIC Interrupt Name	Peripheral Instance Name	Register Group	TIMx Interrupt Configuration Registers	Description
TIMG4.CPU_INT	TIMG4	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG4 Timer CPU interrupt. Multiple OR'd, configurable source condition.

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Table 17-15. CPU Interrupts Triggered by TIMx (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	TIMx Interrupt Configuration Registers	Description
TIMG12.CPU_INT	TIMG12	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG12 Timer CPU interrupt. Multiple OR'd, configurable source condition.

17.3.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 17-16. DMA Triggers from the TIMx

Trigger Name	Peripheral Instance Name	Register Group	TIMx DMA Configuration Registers	Description
TIMG4.GEN_EVENT1	TIMG4	GEN_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG4 Timer DMA trigger. Multiple OR'd, configurable source condition.
TIMG12.GEN_EVENT1	TIMG12	GEN_EVENT1	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG12 Timer DMA trigger. Multiple OR'd, configurable source condition.

17.3.3 ADC Sequencer Triggers

See the Section 20.3.3 section for more details about how to configure triggers for individual ADC sequencers.

Table 17-17. ADC Triggers from the TIMx

Trigger Name	Peripheral Instance Name	Register Group	TIMx ADC Trigger Configuration Registers	Description
TIMG4.GEN_EVENT0	TIMG4	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG4 ADC Sequencer trigger. Multiple OR'd, configurable source condition.
TIMG12.GEN_EVENT0	TIMG12	GEN_EVENT0	IIDX, IMASK, RIS, MIS, ISET, ICLR	TIMG12 ADC Sequencer trigger. Multiple OR'd, configurable source condition.

17.4 TIMERS Registers

This Section describes the TIMERS Registers.

17.4.1 TIMERS Base Address Table

Table 17-18. TIMERS Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Timg4Regs	TIMG4_REGS	TIMG4	0x4018_0000
Timg12Regs	TIMG12_REGS	TIMG12	0x4018_8000

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17.4.2 TIMG4_REGS Registers

Table 17-19 lists the memory-mapped registers for the TIMG4_REGS registers. All register offset addresses not listed in Table 17-19 should be considered as reserved locations and the register contents should not be modified.

Table 17-19. TIMG4_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1000h	CLKDIV	Clock Divider		Go
1008h	CLKSEL	Clock Select for Ultra Low Power peripherals		Go
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
1050h	IIDX	Interrupt index	GEN_EVENT0	Go
1058h	IMASK	Interrupt mask	GEN_EVENT0	Go
1060h	RIS	Raw interrupt status	GEN_EVENT0	Go
1068h	MIS	Masked interrupt status	GEN_EVENT0	Go
1070h	ISET	Interrupt set	GEN_EVENT0	Go
1078h	ICLR	Interrupt clear	GEN_EVENT0	Go
1080h	IIDX	Interrupt index	GEN_EVENT1	Go
1088h	IMASK	Interrupt mask	GEN_EVENT1	Go
1090h	RIS	Raw interrupt status	GEN_EVENT1	Go
1098h	MIS	Masked interrupt status	GEN_EVENT1	Go
10A0h	ISET	Interrupt set	GEN_EVENT1	Go
10A8h	ICLR	Interrupt clear	GEN_EVENT1	Go
10E0h	EVT_MODE	Event Mode		Go
10FCh	DESC	Module Description		Go
1100h	CCPD	CCP Direction		Go
1104h	ODIS	Output Disable		Go
1108h	CCLKCTL	Counter Clock Control Register		Go
110Ch	CPS	Clock Prescale Register		Go
1110h	CPSV	Clock prescale count status register		Go
1114h	CTTRIGCTL	Timer Cross Trigger Control Register		Go
111Ch	CTTRIG	Timer Cross Trigger Register		Go
1120h	FSCTL	Fault Source Control		Go
1124h	GCTL	Global control register		Go
1800h	CTR	Counter Register		Go
1804h	CTRCTL	Counter Control Register		Go
1808h	LOAD	Load Register		Go
1810h + formula	CC_01_y	Capture or Compare Register 0/1		Go

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Table 17-19. TIMG4_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1818h + formula	CC_23_y	Capture or Compare Register 2/3		Go
1820h + formula	CC_45_y	The CC_45 register are a registers which can be used as compare to the current CTR to create an events CC4U, CC4D, CC5U and CC5D.		Go
1830h + formula	CCCTL_01_y	Capture or Compare Control Registers 0/1		Go
1838h + formula	CCCTL_23_y	Capture or Compare Control Registers 2/3		Go
1840h + formula	CCCTL_45_y	Capture or Compare Control Registers 4/5		Go
1850h + formula	OCTL_01_y	CCP Output Control Registers 0/1		Go
1858h + formula	OCTL_23_y	CCP Output Control Registers 2/3		Go
1870h + formula	CCACT_01_y	Capture or Compare Action Registers 0/1		Go
1878h + formula	CCACT_23_y	Capture or Compare Action Registers 2/3		Go
1880h + formula	IFCTL_01_y	Input Filter Control Register 0/1		Go
1888h + formula	IFCTL_23_y	Input Filter Control Register 2/3		Go
18A0h	PL	Phase Load Register		Go
18A4h	DBCTL	Dead Band insertion control register		Go
18B0h	TSEL	Trigger Select Register		Go
18B4h	RC	Repeat counter Register		Go
18B8h	RCLD	Repeat counter load Register		Go
18BCh	QDIR	QEI Count Direction Register		Go
18D0h	FCTL	Fault Control Register		Go
18D4h	FIFCTL	Fault input Filter control register		Go

Complex bit access types are encoded to fit into small table cells. Table 17-20 shows the codes that are used for access types in this section.

Table 17-20. TIMG4_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		

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Table 17-20. TIMG4_REGS Access Type Codes (continued)

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 17-25 and described in Table 17-21.

Return to the Summary Table.

Register to control the power state

Figure 17-25. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 17-22. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 17-26 and described in Table 17-22.

Return to the Summary Table.

Register to control reset assertion and de-assertion

Figure 17-26. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 17-24. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 17-27 and described in Table 17-23.

Return to the Summary Table.

peripheral enable and reset status

Figure 17-27. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 17-26. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 CLKDIV Register (Offset = 1000h) [Reset = 00000000h]

CLKDIV is shown in Figure 17-28 and described in Table 17-24.

Return to the Summary Table.

This register is used to specify module-specific divide ratio of the functional clock

Figure 17-28. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 17-28. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

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5 CLKSEL Register (Offset = 1008h) [Reset = 00000000h]

CLKSEL is shown in Figure 17-29 and described in Table 17-25.

Return to the Summary Table.

Clock Source Select Register

Figure 17-29. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	BUSCLK_SEL	MFCLK_SEL	LFCLK_SEL	RESERVED
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-30. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	RESERVED	R/W	0h	Reserved
3	BUSCLK_SEL	R/W	0h	Selects BUSCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
2	MFCLK_SEL	R/W	0h	Selects MFCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
1	LFCLK_SEL	R/W	0h	Selects LFCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
0	RESERVED	R/W	0h	

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6 PDBGCTL Register (Offset = 1018h) [Reset = 00000000h]

PDBGCTL is shown in Figure 17-30 and described in Table 17-26.

Return to the Summary Table.

This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 17-30. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 17-32. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft halt boundary control. This function is only available, if [FREE] is set to 'STOP' 0h = The peripheral will halt immediately, even if the resultant state will result in corruption if the system is restarted 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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7 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 17-31 and described in Table 17-27.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-31. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-34. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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8 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 17-32 and described in Table 17-28.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-32. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-36. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-36. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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9 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 17-33 and described in Table 17-29.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-33. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-38. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-38. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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10 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 17-34 and described in Table 17-30.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-34. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-40. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-40. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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11 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 17-35 and described in Table 17-31.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-35. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-42. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-42. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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12 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 17-36 and described in Table 17-32.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-36. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-44. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-44. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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13 IIDX Register (Offset = 1050h) [Reset = 00000000h] (GEN_EVENT0)

IIDX is shown in Figure 17-37 and described in Table 17-33.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-37. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-46. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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14 IMASK Register (Offset = 1058h) [Reset = 00000000h] (GEN_EVENT0)

IMASK is shown in Figure 17-38 and described in Table 17-34.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-38. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-48. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-48. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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15 RIS Register (Offset = 1060h) [Reset = 00000000h] (GEN_EVENT0)

RIS is shown in Figure 17-39 and described in Table 17-35.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-39. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-50. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-50. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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16 MIS Register (Offset = 1068h) [Reset = 00000000h] (GEN_EVENT0)

MIS is shown in Figure 17-40 and described in Table 17-36.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-40. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-52. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-52. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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17 ISET Register (Offset = 1070h) [Reset = 00000000h] (GEN_EVENT0)

ISET is shown in Figure 17-41 and described in Table 17-37.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-41. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-54. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-54. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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18 ICLR Register (Offset = 1078h) [Reset = 00000000h] (GEN_EVENT0)

ICLR is shown in Figure 17-42 and described in Table 17-38.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-42. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-56. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-56. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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19 IIDX Register (Offset = 1080h) [Reset = 00000000h] (GEN_EVENT1)

IIDX is shown in Figure 17-43 and described in Table 17-39.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-43. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-58. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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20 IMASK Register (Offset = 1088h) [Reset = 00000000h] (GEN_EVENT1)

IMASK is shown in Figure 17-44 and described in Table 17-40.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-44. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-60. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-60. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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21 RIS Register (Offset = 1090h) [Reset = 00000000h] (GEN_EVENT1)

RIS is shown in Figure 17-45 and described in Table 17-41.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-45. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-62. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-62. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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22 MIS Register (Offset = 1098h) [Reset = 00000000h] (GEN_EVENT1)

MIS is shown in Figure 17-46 and described in Table 17-42.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-46. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-64. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-64. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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23 ISET Register (Offset = 10A0h) [Reset = 00000000h] (GEN_EVENT1)

ISET is shown in Figure 17-47 and described in Table 17-43.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-47. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-66. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-66. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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24 ICLR Register (Offset = 10A8h) [Reset = 00000000h] (GEN_EVENT1)

ICLR is shown in Figure 17-48 and described in Table 17-44.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-48. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-68. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-68. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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25 EVT_MODE Register (Offset = 10E0h) [Reset = 00000029h]

EVT_MODE is shown in Figure 17-49 and described in Table 17-45.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 17-49. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		EVT2_CFG		EVT1_CFG		EVT0_CFG	
R/W-0h		R-2h		R-2h		R-1h	

Table 17-70. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-4	EVT2_CFG	R	2h	Event line mode select for event corresponding to GEN_EVENT1 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
3-2	EVT1_CFG	R	2h	Event line mode select for event corresponding to GEN_EVENT0 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
1-0	EVT0_CFG	R	1h	Event line mode select for event corresponding to CPU_INT 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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26 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 17-50 and described in Table 17-46.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 17-50. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				INSTNUM				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 17-72. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	1111h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	0h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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27 CCPD Register (Offset = 1100h) [Reset = 00000000h]

CCPD is shown in Figure 17-51 and described in Table 17-47.

Return to the Summary Table.

CCP Direction. Controls whether CCP is used as an input or an output.

Figure 17-51. CCPD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	C0CCP2	C0CCP1	C0CCP0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-74. CCPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	RESERVED	R/W	0h	Reserved
2	C0CCP2	R/W	0h	CCP2 direction 0h = input 1h = Output
1	C0CCP1	R/W	0h	CCP1 direction 0h = Input 1h = Output
0	C0CCP0	R/W	0h	CCP0 direction 0h = Input 1h = Output

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28 ODIS Register (Offset = 1104h) [Reset = 00000000h]

ODIS is shown in Figure 17-52 and described in Table 17-48.

Return to the Summary Table.

The ODIS register output is inverted and then ANDed with the output signal selected by the OCTL register CCPO field (before conditional inversion) to allow software the ability to hold the CCP output low during configuration or shutdown.

Figure 17-52. ODIS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				C0CCP3	C0CCP2	C0CCP1	C0CCP0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-76. ODIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	C0CCP3	R/W	0h	Counter CCP3 Disable Mask Defines whether CCP3 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to occpout[2]. 1h = CCP output occpout[3] is forced low.
2	C0CCP2	R/W	0h	Counter CCP2 Disable Mask Defines whether CCP2 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[2] is forced low.
1	C0CCP1	R/W	0h	Counter CCP1 Disable Mask Defines whether CCP0 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[1] is forced low.
0	C0CCP0	R/W	0h	Counter CCP0 Disable Mask Defines whether CCP0 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[0] is forced low.

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29 CCLKCTL Register (Offset = 1108h) [Reset = 00000000h]

CCLKCTL is shown in Figure 17-53 and described in Table 17-49.

Return to the Summary Table.

The CCLKCTL register provides a SW mechanism for gating the TIMER clock if the module is expected not to be used but the power domain is alive. This effectively puts the IP in an IDLE state

Figure 17-53. CCLKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							CLKEN
R/W-0h							R/W-0h

Table 17-78. CCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	CLKEN	R/W	0h	Clock Enable Disables the clock gating to the module. SW has to explicitly program the value to 0 to gate the clock. 0h = Clock is disabled. 1h = Clock is enabled

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30 CPS Register (Offset = 110Ch) [Reset = 00000000h]

CPS is shown in Figure 17-54 and described in Table 17-50.

Return to the Summary Table.

The CPS register provides the value for the clock pre-scaler.

Figure 17-54. CPS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PCNT							
R/W-0h																								R/W-0h							

Table 17-80. CPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	PCNT	R/W	0h	Pre-Scale Count This field specifies the pre-scale count value. The selected TIMCLK source is divided by a value of (PCNT+1). A PCNT value of 0 divides TIMCLK by 1, effectively bypassing the divider. A PCNT value of greater than 0 divides the TIMCLK source generating a slower clock 0h = Minimum value FFh = Maximum Value

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31 CPSV Register (Offset = 1110h) [Reset = 00000000h]

CPSV is shown in Figure 17-55 and described in Table 17-51.

Return to the Summary Table.

The CPSV register provides the ability to read the current clock prescale count value.

Figure 17-55. CPSV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CPSVAL							
R-0h																								R-0h							

Table 17-82. CPSV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	CPSVAL	R	0h	Current Prescale Count Value 0h = Minimum value FFh = Maximum Value

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32 CTTRIGCTL Register (Offset = 1114h) [Reset = 00000000h]

CTTRIGCTL is shown in Figure 17-56 and described in Table 17-52.

Return to the Summary Table.

Cross Timer Trigger Control Register
This register is used to control the cross trigger connections for enables and faults of different timer instances in the same power domain. Please refer to sections Timer Module Cross Trigger (In/Out) and Fault Cross Triggering for details.

Figure 17-56. CTTRIGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				EVTCTTRIGSEL			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						EVTCTEN	CTEN
R/W-0h						R/W-0h	R/W-0h

Table 17-84. CTTRIGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	EVTCTTRIGSEL	R/W	0h	Used to Select the subscriber port that should be used for input cross trigger. 0h = Use FSUB0 as cross trigger source. 1h = Use FSUB1 as cross trigger source. 2h = Use Zero event as cross trigger source. 3h = Use Load event as cross trigger source. 4h = Use CCD0 event as cross trigger source. 5h = Use CCD1 event as cross trigger source. 6h = Use CCD2 event as cross trigger source. 7h = Use CCD3 event as cross trigger source. 8h = Use CCU0 event as cross trigger source. 9h = Use CCU1 event as cross trigger source. Ah = Use CCU2 event as cross trigger source. Bh = Use CCU3 event as cross trigger source.
15-2	RESERVED	R/W	0h	
1	EVTCTEN	R/W	0h	Enable the Input Trigger Conditions to the Timer module as a condition for Cross Triggers. 0h = Cross trigger generation disabled. 1h = Cross trigger generation enabled
0	CTEN	R/W	0h	Timer Cross trigger enable. This field is used to enable whether the SW or HW logic can generate a timer cross trigger event in the system. These cross triggers are connected to the respective timer trigger in of the other timer IPs in the SOC power domain. The timer cross trigger is essentially the combined logic of the HW and SW conditions controlling EN bit in the CTRCTL register. 0h = Cross trigger generation disabled. 1h = Cross trigger generation enabled

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33 CTTRIG Register (Offset = 111Ch) [Reset = 00000000h]

CTTRIG is shown in Figure 17-57 and described in Table 17-53.

Return to the Summary Table.

Cross Timer Trigger Register
This register is used to trigger the timer instances connected and enabled using CTTRIGCTL and CTTRIGMSK registers.

Figure 17-57. CTTRIG Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG
W-0h							W-0h

Table 17-86. CTTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG	W	0h	Generate Cross Trigger This bit when programmed will generate a synchronized trigger condition all the cross trigger enabled Timer instances including current timer instance. 0h = Cross trigger generation disabled 1h = Generate Cross trigger pulse

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34 FSCTL Register (Offset = 1120h) [Reset = 00000000h]

FSCTL is shown in Figure 17-58 and described in Table 17-54.

Return to the Summary Table.

The FSCTL register controls the fault source selection and enable. There are 5 input fault sources either through synchronous path processing or asynchronous path.

Figure 17-58. FSCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	FEX2EN	FEX1EN	FEX0EN	FAC2EN	FAC1EN	FAC0EN	FCEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-88. FSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6	FEX2EN	R/W	0h	This field controls whether the fault is caused by external fault pin 2. 0h = Disable 1h = Enable
5	FEX1EN	R/W	0h	This field controls whether the fault is caused by external fault pin 1. 0h = Disable 1h = Enable
4	FEX0EN	R/W	0h	This field controls whether the fault is caused by external fault pin 0. 0h = Disable 1h = Enable
3	FAC2EN	R/W	0h	This field controls whether the fault is caused by COMP2 output. 0h = Disable 1h = Enable
2	FAC1EN	R/W	0h	This field controls whether the fault is caused by COMP1 output. 0h = Disable 1h = Enable
1	FAC0EN	R/W	0h	This field controls whether the fault signal is caused by COMP0 output. 0h = Disable 1h = Enable
0	FCEN	R/W	0h	This field controls whether the fault is caused by the system clock fault. 0h = Disable 1h = Enable

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35 GCTL Register (Offset = 1124h) [Reset = 00000000h]

GCTL is shown in Figure 17-59 and described in Table 17-55.

Return to the Summary Table.

Global control register

Figure 17-59. GCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							SHDWLDEN
R/W-0h							R/W-0h

Table 17-90. GCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	SHDWLDEN	R/W	1h	Enables shadow to active load of bufferred registers and register fields. 0h = Disable 1h = Enable

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36 CTR Register (Offset = 1800h) [Reset = 00000000h]

CTR is shown in Figure 17-60 and described in Table 17-56.

Return to the Summary Table.

This is the TIMER counter register.
This can be set by SW. However, the writes will be unpredictable if the software tries to set a value while the counter is running.

Figure 17-60. CTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCTR																															
R/W-0h																															

Table 17-92. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCTR	R/W	0h	Current Counter value 0h = Minimum value FFFFFFFFh = Maximum Value

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37 CTRCTL Register (Offset = 1804h) [Reset = 0000FF80h]

CTRCTL is shown in Figure 17-61 and described in Table 17-57.

Return to the Summary Table.

This register provides control over the counter operation.
The configuration can change as well as setting the EN bit in a single write.
There is no requirement to change the configuration first and then do an additional write to set the EN bit.

Figure 17-61. CTRCTL Register

31	30	29	28	27	26	25	24
RESERVED		CVAE		RESERVED			PLEN
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
SLZERCNEZ	RESERVED			FRB	FB	DRB	RESERVED
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CZC				CAC		CLC	
R/W-7h				R/W-7h		R/W-7h	
7	6	5	4	3	2	1	0
CLC	RESERVED	CM		REPEAT			EN
R/W-7h	R/W-0h	R/W-0h		R/W-0h			R/W-0h

Table 17-94. CTRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29-28	CVAE	R/W	0h	Counter Value After Enable. This field specifies the initialization condition of the counter when the EN bit is changed from 0 to 1 by a write to the CTRCTL register. Note that an external event can also cause the EN bit to go active. 0h = The counter is set to the LOAD register value 1h = The counter value is unchanged from its current value which could have been initialized by software 2h = The counter is set to zero
27-25	RESERVED	R/W	0h	
24	PLEN	R/W	0h	Phase Load Enable. This bit allows the timer to have phase load feature. 0h = Disabled 1h = Enabled
23	SLZERCNEZ	R/W	0h	Suppress Load and Zero Events if Repeat Counter is Not Equal to Zero. This bit suppresses the generation of the Z (zero) and L (load) events from the counter when the repeat counter (RC) value is not 0. 0h = Disabled. Z and L events are always generated from the counter when their conditions are generated. 1h = Enabled. Z and L events are generated from the counter when their conditions are generated and the RC register value is 0.
22-20	RESERVED	R/W	0h	
19	FRB	R/W	0h	Fault Resume Behavior This bit specifies what the device does following the release/exit of fault condition. 0h = Resume counting 1h = Perform the action as specified by the CVAE field.

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Table 17-94. CTRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	FB	R/W	0h	Fault Behavior This bit specifies whether the counter continues running or suspends during a fault mode. There is a separate control under REPEAT to indicate whether counting is to suspend at next Counter==0 0h = Continues counting 1h = Suspends counting
17	DRB	R/W	0h	Debug Resume Behavior This bit specifies what the device does following the release/exit of debug mode. 0h = Resume counting 1h = Perform the action as specified by the CVAE field.
16	RESERVED	R/W	0h	
15-13	CZC	R/W	7h	Counter Zero Control This field specifies what controls the counter operation with respect to zeroing the counter value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 ZCOND 1h = CCCTL_1 ZCOND 2h = CCCTL_2 ZCOND This value exists when there are 4 channels. 3h = CCCTL_3 ZCOND This value exists when there are 4 channels. 4h = Controlled by 2-input QEI mode This value exists when TIMER support QEI feature. 5h = Controlled by 3-input QEI mode This value exists when TIMER support QEI feature.
12-10	CAC	R/W	7h	Counter Advance Control. This field specifies what controls the counter operation with respect to advancing (incrementing or decrementing) the counter value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 ACOND 1h = CCCTL_1 ACOND 2h = CCCTL_2 ACOND This value exists when there are 4 channels. 3h = CCCTL_3 ACOND This value exists when there are 4 channels. 4h = Controlled by 2-input QEI mode This value exists when TIMER support QEI feature. 5h = Controlled by 3-input QEI mode This value exists when TIMER support QEI feature.
9-7	CLC	R/W	7h	Counter Load Control. This field specifies what controls the counter operation with respect to setting the counter to the LD register value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 LCOND 1h = CCCTL_1 LCOND 2h = CCCTL_2 LCOND This value exists when there are 4 channels. 3h = CCCTL_3 LCOND This value exists when there are 4 channels. 4h = Controlled by 2 input QEI mode. This value exists when TIMER support QEI feature. 5h = Controlled by 3 input QEI mode. This value exists when TIMER support QEI feature.
6	RESERVED	R/W	0h	

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Table 17-94. CTRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	CM	R/W	0h	Count Mode 0h = Down 1h = Up/Down 2h = Counter counts up.
3-1	REPEAT	R/W	0h	Repeat. The repeat bit controls whether the counter continues to advance following a zero event, or the exiting of a debug or fault condition. If counting down, a zero event is followed by a load at the next advance condition. If counting up-down, a zero event is followed by an advance event (+1). The intent of encoding 3 is that if the debug condition is in effect, the generation of the load pulse is deferred until the debug condition is over. This allows the counter to reach zero before counting is suspended. 0h = Does not automatically advance following a zero event. 1h = Continues to advance following a zero event. 2h = Reserved 3h = Continues to advance following a zero event if the debug mode is not in effect, or following the release of the debug mode. 4h = Reserved
0	EN	R/W	0h	Counter Enable. This bit allows the timer to advance This bit is automatically cleared if REPEAT=0 (do not automatically reload) and the counter value equals zero. CPU Write: A register write that sets the EN bit, the counter value is set per the CVAE value. Hardware: This bit may also be set as the result of an LCOND or ZCOND condition being met and the counter value changed to the load value or zero value, respectively. 0h = Disabled 1h = Enabled

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38 LOAD Register (Offset = 1808h) [Reset = 00000000h]

LOAD is shown in Figure 17-62 and described in Table 17-58.

Return to the Summary Table.

The contents of LOAD register are copied to CTR on any operation designated to do a "LOAD". The LOAD is used to compare with the CTR for generating a "Load Event" that can be used for interrupt, trigger, or signal generator actions.

Figure 17-62. LOAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD																															
R/W-0h																															

Table 17-96. LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LD	R/W	0h	Load Value 0h = Minimum value FFFFFFFFh = Maximum Value

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39 CC_01_y Register (Offset = 1810h + formula) [Reset = 00000000h]

CC_01_y is shown in Figure 17-63 and described in Table 17-59.

Return to the Summary Table.

The CC_01 register is a register that can be used as either a capture register, to capture the next CTR value on an event, or a compare to the current CTR to create an event. It cannot operate concurrently as both. There are two Capture-Compare slices of hardware for each counter, hence there are two CC_01 registers per timer. On a capture event, the next value of the CTR is loaded so that CTR and CC_01 (which captured) will be equal on the cycle that an interrupt or trigger is created from the capture action.

Offset = 1810h + (y * 4h); where y = 0h to 1h

Figure 17-63. CC_01_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-98. CC_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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40 CC_23_y Register (Offset = 1818h + formula) [Reset = 00000000h]

CC_23_y is shown in Figure 17-64 and described in Table 17-60.

Return to the Summary Table.

The CC_23 register is a register that can be used as either a capture register, to capture the next CTR value on an event, or a compare to the current CTR to create an event. It cannot operate concurrently as both. There are two Capture-Compare slices of hardware for each counter, hence there are two CC_01 registers per timer. On a capture event, the next value of the CTR is loaded so that CTR and CC_01 (which captured) will be equal on the cycle that an interrupt or trigger is created from the capture action.

Offset = 1818h + (y * 4h); where y = 0h to 1h

Figure 17-64. CC_23_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-100. CC_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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41 CC_45_y Register (Offset = 1820h + formula) [Reset = 00000000h]

CC_45_y is shown in Figure 17-65 and described in Table 17-61.

Return to the Summary Table.

The CC_45 register are a registers which can be used as compare to the current CTR to create an events CC4U, CC4D, CC5U and CC5D.

Offset = 1820h + (y * 4h); where y = 0h to 1h

Figure 17-65. CC_45_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-102. CC_45_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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42 CCCTL_01_y Register (Offset = 1830h + formula) [Reset = 00000000h]

CCCTL_01_y is shown in Figure 17-66 and described in Table 17-62.

Return to the Summary Table.

The CCCTL_01 registers control the operations of the respective CC registers and the counter.

Offset = 1830h + (y * 4h); where y = 0h to 1h

Figure 17-66. CCCTL_01_y Register

31	30	29	28	27	26	25	24
CC2SELD			CCACTUPD			SCERCNEZ	CC2SELU
R/W-0h			R/W-0h			R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CC2SELU		RESERVED	CCUPD			COC	RESERVED
R/W-0h		R/W-0h	R/W-0h			R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	ZCOND			RESERVED	LCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	ACOND			RESERVED	CCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 17-104. CCCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CC2SELD	R/W	0h	Selects the source second CCD event. 0h = Selects CCD from CC0. 1h = Selects CCD from CC1. 2h = Selects CCD from CC2. 3h = Selects CCD from CC3. 4h = Selects CCD from CC4. 5h = Selects CCD from CC5.

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Table 17-104. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-26	CCACTUPD	R/W	0h	CCACT shadow register Update Method This field controls how updates to the CCACT shadow register are performed 0h = Value written to the CCACT register has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR = LOAD) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = On a TRIG pulse, the value stored in CCACT_xy shadow register is loaded into CCACT_xy register.
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RC) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.

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Table 17-104. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	CC2SELU	R/W	0h	Selects the source second CCU event. 0h = Selects CCU from CC0. 1h = Selects CCU from CC1. 2h = Selects CCU from CC2. 3h = Selects CCU from CC3. 4h = Selects CCU from CC4. 5h = Selects CCU from CC5.
21	RESERVED	R/W	0h	
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event(CTR=0) or load event (CTR=LOAD) Writes to the CCx_y register are stored in shadow register and transferred to ECCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LD. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y

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Table 17-104. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	COC	R/W	0h	Capture or Compare. Specifies whether the corresponding CC register is used as a capture register or a compare register (never both). 0h = Compare 1h = Capture
16-15	RESERVED	R/W	0h	
14-12	ZCOND	R/W	0h	Zero Condition. This field specifies the condition that generates a zero pulse. 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
11	RESERVED	R/W	0h	
10-8	LCOND	R/W	0h	Load Condition. Specifies the condition that generates a load pulse. 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
7	RESERVED	R/W	0h	
6-4	ACOND	R/W	0h	Advance Condition. Specifies the condition that generates an advance pulse. 0h = Each TIMCLK 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge) 5h = CCP High or Trigger assertion (level)
3	RESERVED	R/W	0h	
2-0	CCOND	R/W	0h	Capture Condition. Specifies the condition that generates a capture pulse. 0h = None (never captures) 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)

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43 CCCTL_23_y Register (Offset = 1838h + formula) [Reset = 00000000h]

CCCTL_23_y is shown in Figure 17-67 and described in Table 17-63.

Return to the Summary Table.

The CCCTL registers control the operations of the respective CC registers and the counter.

Offset = 1838h + (y * 4h); where y = 0h to 1h

Figure 17-67. CCCTL_23_y Register

31	30	29	28	27	26	25	24
CC2SELD			CCACTUPD			SCERCNEZ	CC2SELU
R/W-0h			R/W-0h			R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CC2SELU		RESERVED	CCUPD			COC	RESERVED
R/W-0h		R/W-0h	R/W-0h			R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	ZCOND			RESERVED	LCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	ACOND			RESERVED	CCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 17-106. CCCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CC2SELD	R/W	0h	Selects the source second CCD event. 0h = Selects CCD from CC0. 1h = Selects CCD from CC1. 2h = Selects CCD from CC2. 3h = Selects CCD from CC3. 4h = Selects CCD from CC4. 5h = Selects CCD from CC5.

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Table 17-106. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-26	CCACTUPD	R/W	0h	CCACT shadow register Update Method This field controls how updates to the CCCACT shadow register are performed 0h = Value written to the CCACTx_y register has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=cc_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR=LOAD) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = On a TRIG pulse, the value stored in CCACTx_y shadow register is loaded into CCACTx_y active register.
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RCn) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.

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Table 17-106. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	CC2SELU	R/W	0h	Selects the source second CCU event. 0h = Selects CCU from CC0. 1h = Selects CCU from CC1. 2h = Selects CCU from CC2. 3h = Selects CCU from CC3. 4h = Selects CCU from CC4. 5h = Selects CCU from CC5.
21	RESERVED	R/W	0h	
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero or load event Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y #xD 0.

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Table 17-106. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	COC	R/W	0h	Capture or Compare. Specifies whether the corresponding CC register is used as a capture register or a compare register (never both). 0h = Compare 1h = Capture
16-15	RESERVED	R/W	0h	
14-12	ZCOND	R/W	0h	Zero Condition. This field specifies the condition that generates a zero pulse. 4h-Fh = Reserved 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
11	RESERVED	R/W	0h	
10-8	LCOND	R/W	0h	Load Condition. Specifies the condition that generates a load pulse. 4h-Fh = Reserved 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
7	RESERVED	R/W	0h	
6-4	ACOND	R/W	0h	Advance Condition. Specifies the condition that generates an advance pulse. 6h-Fh = Reserved 0h = Each TIMCLK 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge) 5h = CCP High or Trigger assertion (level)
3	RESERVED	R/W	0h	
2-0	CCOND	R/W	0h	Capture Condition. Specifies the condition that generates a capture pulse. 4h-Fh = Reserved 0h = None (never captures) 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)

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44 CCCTL_45_y Register (Offset = 1840h + formula) [Reset = 00000000h]

CCCTL_45_y is shown in Figure 17-68 and described in Table 17-64.

Return to the Summary Table.

The CCCTL registers control the operations of the respective CC registers and the counter.

Offset = 1840h + (y * 4h); where y = 0h to 1h

Figure 17-68. CCCTL_45_y Register

31	30	29	28	27	26	25	24
RESERVED						SCERCNEZ	RESERVED
R/W-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED			CCUPD			RESERVED	
R/W-0h			R/W-0h			R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 17-108. CCCTL_45_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	0h	
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RC) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.
24-21	RESERVED	R/W	0h	

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Table 17-108. CCCTL_45_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to ECCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR=LOAD) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LD. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y #xD 0.
17-0	RESERVED	R/W	0h	

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45 OCTL_01_y Register (Offset = 1850h + formula) [Reset = 00000000h]

OCTL_01_y is shown in Figure 17-69 and described in Table 17-65.

Return to the Summary Table.

The OCTL_01 register controls the CCP output of the Capture-Compare slice of the counter. This includes the ability to select the source of what is driven out along with initial condition values and final inversion options.

Offset = 1850h + (y * 4h); where y = 0h to 1h

Figure 17-69. OCTL_01_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		CCPIV	CCPOINV	CCPO			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			

Table 17-110. OCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	CCPIV	R/W	0h	CCP Initial Value This bit specifies the logical value put on the signal generator state while the counter is disabled (CTRCTL.EN == 0). 0h = Low 1h = High
4	CCPOINV	R/W	0h	CCP Output Invert The output as selected by CCPO is conditionally inverted. 0h = No inversion 1h = Invert
3-0	CCPO	R/W	0h	CCP Output Source 0h = Signal generator value (for example, PWM, triggered PWM) 1h = Load event 2h = CCU event or CCD event 4h = Zero event 5h = Capture event 6h = Fault condition 8h = Mirror CCP of first capture and compare register to other capture compare blocks 9h = Mirror CCP of second capture and compare register in other capture compare blocks Ch = Signal generator output after deadband insertion Dh = Counter direction

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46 OCTL_23_y Register (Offset = 1858h + formula) [Reset = 00000000h]

OCTL_23_y is shown in Figure 17-70 and described in Table 17-66.

Return to the Summary Table.

The OCTL register controls the CCP output of the Capture-Compare slice of the counter. This includes the ability to select the source of what is driven out along with initial condition values and final inversion options.

Offset = 1858h + (y * 4h); where y = 0h to 1h

Figure 17-70. OCTL_23_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		CCPIV	CCPOINV	CCPO			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			

Table 17-112. OCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	CCPIV	R/W	0h	CCP Initial Value This bit specifies the logical value put on the signal generator state while the counter is disabled (CTRCTL.EN == 0). 0h = Low 1h = High
4	CCPOINV	R/W	0h	CCP Output Invert The output as selected by CCPO is conditionally inverted. 0h = No inversion 1h = Invert
3-0	CCPO	R/W	0h	CCP Output Source 0h = Signal generator value (for example, PWM, triggered PWM) 1h = Load condition 2h = CCU event or CCD event 4h = Zero event 5h = Capture event 6h = Fault Condition 8h = Mirror CCP of first capture and compare register in other capture compare blocks 9h = Mirror CCP of second capture and compare register in other capture compare blocksi /bn,. Ch = Deadband Inserted Output Dh = Counter direction

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47 CCACT_01_y Register (Offset = 1870h + formula) [Reset = 00000000h]

CCACT_01_y is shown in Figure 17-71 and described in Table 17-67.

Return to the Summary Table.

The CCACT_01 register controls the actions of the signal generator of the capture-compare slice based on the events created in the counter block, the capture and compare block and debug events.

Offset = 1870h + (y * 4h); where y = 0h to 1h

Figure 17-71. CCACT_01_y Register

31	30	29	28	27	26	25	24
SWFRCACT_CMPL		SWFRCACT		FEXACT			FENACT
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
FENACT		RESERVED					CC2UACT
R/W-0h		R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
CC2UACT	RESERVED	CC2DACT		RESERVED	CUACT		RESERVED
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
CDACT		RESERVED	LACT		RESERVED	ZACT	
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	

Table 17-114. CCACT_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SWFRCACT_CMPL	R/W	0h	CCP Complimentary output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP Complimentary output value is set high 2h = CCP Complimentary output value is set low
29-28	SWFRCACT	R/W	0h	CCP Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low
27-25	FEXACT	R/W	0h	CCP Output Action on Fault Exit This field describes the resulting action of the signal generator upon exiting the fault condition. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated

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Table 17-114. CCACT_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	FENACT	R/W	0h	CCP Output Action on Fault Entry This field describes the resulting action of the signal generator upon detecting a fault. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated
21-17	RESERVED	R/W	0h	
16-15	CC2UACT	R/W	0h	CCP Output Action on CC2U event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
14	RESERVED	R/W	0h	
13-12	CC2DACT	R/W	0h	CCP Output Action on CC2D event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
11	RESERVED	R/W	0h	
10-9	CUACT	R/W	0h	CCP Output Action on Compare (Up) This field describes the resulting action of the signal generator upon detecting a compare event while counting up. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
8	RESERVED	R/W	0h	
7-6	CDACT	R/W	0h	CCP Output Action on Compare (Down) This field describes the resulting action of the signal generator upon detecting a compare event while counting down. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
5	RESERVED	R/W	0h	
4-3	LACT	R/W	0h	CCP Output Action on Load Specifies what changes occur to CCP output as the result of a load event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
2	RESERVED	R/W	0h	
1-0	ZACT	R/W	0h	CCP Output Action on Zero Specifies what changes occur to CCP output as the result of a zero event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled

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48 CCACT_23_y Register (Offset = 1878h + formula) [Reset = 00000000h]

CCACT_23_y is shown in Figure 17-72 and described in Table 17-68.

Return to the Summary Table.

The CCACT register controls the actions of the signal generator of the capture-compare slice based on the events created in the counter block, the capture and compare block and debug events.

Offset = 1878h + (y * 4h); where y = 0h to 1h

Figure 17-72. CCACT_23_y Register

31	30	29	28	27	26	25	24
SWFRCACT_CMPL		SWFRCACT		FEXACT			FENACT
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
FENACT		RESERVED					CC2UACT
R/W-0h		R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
CC2UACT	RESERVED	CC2DACT		RESERVED	CUACT		RESERVED
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
CDACT		RESERVED	LACT		RESERVED	ZACT	
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	

Table 17-116. CCACT_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SWFRCACT_CMPL	R/W	0h	CCP Complimentary Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP Complimentary output value is set high 2h = CCP Complimentary output value is set low
29-28	SWFRCACT	R/W	0h	CCP Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low
27-25	FEXACT	R/W	0h	CCP Output Action on Fault Exit This field describes the resulting action of the signal generator upon exiting the fault condition. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated

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Table 17-116. CCACT_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	FENACT	R/W	0h	CCP Output Action on Fault Entry This field describes the resulting action of the signal generator upon detecting a fault. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated
21-17	RESERVED	R/W	0h	
16-15	CC2UACT	R/W	0h	CCP Output Action on CC2U event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
14	RESERVED	R/W	0h	
13-12	CC2DACT	R/W	0h	CCP Output Action on CC2D event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
11	RESERVED	R/W	0h	
10-9	CUACT	R/W	0h	CCP Output Action on Compare (Up) This field describes the resulting action of the signal generator upon detecting a compare event while counting up. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
8	RESERVED	R/W	0h	
7-6	CDACT	R/W	0h	CCP Output Action on Compare (Down) This field describes the resulting action of the signal generator upon detecting a compare event while counting down. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
5	RESERVED	R/W	0h	
4-3	LACT	R/W	0h	CCP Output Action on Load Specifies what changes occur to CCP output as the result of a load event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
2	RESERVED	R/W	0h	
1-0	ZACT	R/W	0h	CCP Output Action on Zero Specifies what changes occur to CCP output as the result of a zero event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled

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49 IFCTL_01_y Register (Offset = 1880h + formula) [Reset = 00000000h]

IFCTL_01_y is shown in Figure 17-73 and described in Table 17-69.

Return to the Summary Table.

The IFCTL_01 register controls the input selection and inversion for the associated Capture-Compare slice.

Offset = 1880h + (y * 4h); where y = 0h to 1h

Figure 17-73. IFCTL_01_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			FE	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
INV	RESERVED			ISEL			
R/W-0h	R/W-0h			R/W-0h			

Table 17-118. IFCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	FE	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to the edge detect. 0h = Bypass. 1h = Filtered.
11	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output.
10	RESERVED	R/W	0h	
9-8	FP	R/W	0h	Filter Period. This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = The division factor is 3 1h = The division factor is 5 2h = The division factor is 8

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Table 17-118. IFCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INV	R/W	0h	Input Inversion This bit controls whether the selected input is inverted. 0h = Noninverted 1h = Inverted
6-4	RESERVED	R/W	0h	
3-0	ISEL	R/W	0h	Input Select (CCP0) This field selects the input source to the filter input. 4h-7h = Reserved 0h = CCP of the corresponding capture compare unit 1h = Input pair CCPX of the capture compare unit. For CCP0 input pair is CCP1 and for CCP1 input pair is CCP0. 2h = CCP0 of the counter 3h = Trigger 4h = XOR of CCP inputs as input source (Used in Hall input mode). 5h = subscriber 0 event as input source. 6h = subscriber 1 event as input source. 7h = Comparator 0 output. 8h = Comparator 1 output. 9h = Comparator 2 output.

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50 IFCTL_23_y Register (Offset = 1888h + formula) [Reset = 00000000h]

IFCTL_23_y is shown in Figure 17-74 and described in Table 17-70.

Return to the Summary Table.

The IFCTL register controls the input selection and inversion for the associated Capture-Compare slice.

Offset = 1888h + (y * 4h); where y = 0h to 1h

Figure 17-74. IFCTL_23_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			FE	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
INV	RESERVED			ISEL			
R/W-0h	R/W-0h			R/W-0h			

Table 17-120. IFCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	FE	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to the edge detect. 0h = Bypass. 1h = Filtered.
11	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output.
10	RESERVED	R/W	0h	
9-8	FP	R/W	0h	Filter Period. This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = The division factor is 3 1h = The division factor is 5 2h = The division factor is 8

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Table 17-120. IFCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INV	R/W	0h	Input Inversion This bit controls whether the selected input is inverted. 0h = Noninverted 1h = Inverted
6-4	RESERVED	R/W	0h	
3-0	ISEL	R/W	0h	Input Select (CCP0) This field selects the input source to the filter input. 4h-7h = Reserved 0h = CCP of the corresponding capture compare unit 1h = Input pair CCPX of the capture compare unit. For CCP0 input pair is CCP1 and for CCP1 input pair is CCP0. 2h = CCP0 of the counter 3h = Trigger 4h = XOR of CCP inputs as input source (Used in Hall input mode). 5h = subscriber 0 event as input source. 6h = subscriber 1 event as input source. 7h = Comparator 0 output. 8h = Comparator 1 output. 9h = Comparator 2 output.

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51 PL Register (Offset = 18A0h) [Reset = 00000000h]

PL is shown in Figure 17-75 and described in Table 17-71.

Return to the Summary Table.

This is the phase load register.

Figure 17-75. PL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHASE															
R/W-0h																R/W-0h															

Table 17-122. PL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	PHASE	R/W	0h	Phase Load value 0h = Minimum value FFFFFFFFh = Maximum Value

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52 DBCTL Register (Offset = 18A4h) [Reset = 00000000h]

DBCTL is shown in Figure 17-76 and described in Table 17-72.

Return to the Summary Table.

The DBCTL register controls the dead band insertion of the pulse width modulated output.

Figure 17-76. DBCTL Register

31	30	29	28	27	26	25	24
RESERVED				FALLDELAY			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
FALLDELAY							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			M1_ENABLE	RISEDELAY			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
RISEDELAY							
R/W-0h							

Table 17-124. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	
27-16	FALLDELAY	R/W	0h	Fall Delay The number of TIMCLK periods inserted between the fall edge of CCP signal and the rise edge of CCP complimentary signal. 0h = Minimum value FFFh = Maximum Value
15-13	RESERVED	R/W	0h	
12	M1_ENABLE	R/W	0h	Dead Band Mode 1 Enable. 0h = Disabled 1h = Enabled
11-0	RISEDELAY	R/W	0h	Rise Delay The number of TIMCLK periods inserted between the fall edge of CCP signal and the rise edge of CCP complimentary signal. 0h = Minimum value FFFh = Maximum Value

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53 TSEL Register (Offset = 18B0h) [Reset = 00000000h]

TSEL is shown in Figure 17-77 and described in Table 17-73.

Return to the Summary Table.

The TSEL register controls the input trigger enable and selection of the trigger source. Trigger sources are generated by other SoC elements through their respective publisher ports (subscribed in by the timer's subscriber port).

Figure 17-77. TSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TE	RESERVED				ETSEL				
R/W-0h						R/W-0h	R/W-0h				R/W-0h				

Table 17-126. TSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	TE	R/W	0h	Trigger Enable. This selects whether a trigger is enabled or not for this counter 0x0 = Triggers are not used 0x1 = Triggers are used as selected by the ETSEL field 0h = Triggers are not used. 1h = Triggers are used as selected by the IE, ITSEL and ETSEL fields.
8-5	RESERVED	R/W	0h	
4-0	ETSEL	R/W	0h	External Trigger Select. This selects which System Event is used if the input filter selects trigger. Triggers 0-15 are used to connect triggers generated by other timer modules. Refer to the SoC datasheet for details related to timer trigger sources. Triggers 16 and 17 are connected to event manager subscriber ports. Event lines 18-31 are reserved for future use. 0h = TRIGx = External trigger input from TIM x. 1h = TRIGx = External trigger input from TIM x. 2h = TRIGx = External trigger input from TIM x. 3h = TRIGx = External trigger input from TIM x. 4h = TRIGx = External trigger input from TIM x. 5h = TRIGx = External trigger input from TIM x. 6h = TRIGx = External trigger input from TIM x. 7h = TRIGx = External trigger input from TIM x. 8h = TRIGx = External trigger input from TIM x. 9h = TRIGx = External trigger input from TIM x. Ah = TRIGx = External trigger input from TIM x. Bh = TRIGx = External trigger input from TIM x. Ch = TRIGx = External trigger input from TIM x. Dh = TRIGx = External trigger input from TIM x. Eh = TRIGx = External trigger input from TIM x. Fh = TRIGx = External trigger input from TIM x. 10h = TRIG_SUBx = External trigger input from subscriber port x. 11h = TRIG_SUBx = External trigger input from subscriber port x.

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54 RC Register (Offset = 18B4h) [Reset = 00000000h]

RC is shown in Figure 17-78 and described in Table 17-74.

Return to the Summary Table.

Repeat counter is to reduce interrupt overhead. The repeat counter provides the mechanism to suppress un-necessary interrupts
reducing the number of interrupts generated by each event type to 1 for the program number of periods. Specifically, the repeat timer may suppress Load, Compare (up/down, normal/shadow), and Zero events.

Figure 17-78. RC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RC							
R-0h																								R-0h							

Table 17-128. RC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RC	R	0h	Repeat Counter Value 0h = Minimum value FFh = Maximum Value

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55 RCLD Register (Offset = 18B8h) [Reset = 00000000h]

RCLD is shown in Figure 17-79 and described in Table 17-75.

Return to the Summary Table.

The load register value is transferred to the counter when the counter load input is asserted.

Figure 17-79. RCLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RCLD							
R/W-0h																								R/W-0h							

Table 17-130. RCLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	RCLD	R/W	0h	Repeat Counter Load Value This field provides the value loaded into the repeat counter at a load event following the repeat counter value equaling 0. 0h = Minimum value FFh = Maximum Value

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56 QDIR Register (Offset = 18BCh) [Reset = 00000000h]

QDIR is shown in Figure 17-80 and described in Table 17-76.

Return to the Summary Table.

The QDIR register provides the direction of count which is intended for use when operating the counter in QEI.

Figure 17-80. QDIR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DIR
R-0h															R-0h

Table 17-132. QDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	DIR	R	0h	Direction of count 0h = Down (Phase B leads Phase A) 1h = Up (Phase A leads Phase B)

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57 FCTL Register (Offset = 18D0h) [Reset = 00000000h]

FCTL is shown in Figure 17-81 and described in Table 17-77.

Return to the Summary Table.

The FCTL register controls the fault inputs, fault detection and error handling behavior.

Figure 17-81. FCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		FSENEXT2	FSENEXT1	FSENEXT0	FSENAC2	FSENAC1	FSENAC0
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TFIM	RESERVED		FL		FI	RESERVED	FIEN
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h

Table 17-134. FCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	0h	
13	FSENEXT2	R/W	0h	Specifies whether the external fault pin2 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
12	FSENEXT1	R/W	0h	Specifies whether the external fault pin1 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
11	FSENEXT0	R/W	0h	Specifies whether the external fault pin0 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
10	FSENAC2	R/W	0h	Specifies whether the COMP2 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
9	FSENAC1	R/W	0h	Specifies whether the COMP1 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
8	FSENAC0	R/W	0h	Specifies whether the COMP0 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
7	TFIM	R/W	0h	Trigger Fault Input Mask Specifies whether the selected trigger participates as a fault input. If enabled and the trigger asserts, the trigger is treated as a fault. 0h = Selected trigger does not participate in fault condition generation 1h = Selected trigger participates in fault condition generation
6-5	RESERVED	R/W	0h	

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Table 17-134. FCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	FL	R/W	0h	Fault Latch mode Specifies whether the fault condition is latched and configures the latch clear conditions. 0h = Overall fault condition is not dependent on the F bit in RIS 1h = Overall fault condition is dependent on the F bit in RIS 2h = Fault condition is latched. Fault condition is cleared on a zero event if the fault input is 0. 3h = Fault condition is latched. Fault condition is cleared on a load event if the fault input is 0.
2	FI	R/W	0h	Fault Input Specifies whether the overall fault condition is dependent on the sensed fault pin. 0h = Overall Fault condition is not dependent on sensed input. 1h = Overall Fault condition is dependent on sensed input.
1	RESERVED	R/W	0h	
0	FIEN	R/W	0h	Fault Input Enable This bit enables the input for fault detection. 0h = Fault Input Disabled 1h = Fault Input Enabled

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58 FIFCTL Register (Offset = 18D4h) [Reset = 00000000h]

FIFCTL is shown in Figure 17-82 and described in Table 17-78.

Return to the Summary Table.

The FIFCTL register controls the filtering for the fault input.

Figure 17-82. FIFCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			FILTEN	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 17-136. FIFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	FILTEN	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to go directly to the optional pre-scale filter and then to the edge detect. 0h = Bypass 1h = Filtered.
3	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods. The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting. The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output
2	RESERVED	R/W	0h	
1-0	FP	R/W	0h	Filter Period This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = Filter Period 3 1h = Filter Period 5 2h = Filter Period 8

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17.4.3 TIMG12_REGS Registers

Table 17-79 lists the memory-mapped registers for the TIMG12_REGS registers. All register offset addresses not listed in Table 17-79 should be considered as reserved locations and the register contents should not be modified.

Table 17-137. TIMG12_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1000h	CLKDIV	Clock Divider		Go
1008h	CLKSEL	Clock Select for Ultra Low Power peripherals		Go
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
1050h	IIDX	Interrupt index	GEN_EVENT0	Go
1058h	IMASK	Interrupt mask	GEN_EVENT0	Go
1060h	RIS	Raw interrupt status	GEN_EVENT0	Go
1068h	MIS	Masked interrupt status	GEN_EVENT0	Go
1070h	ISET	Interrupt set	GEN_EVENT0	Go
1078h	ICLR	Interrupt clear	GEN_EVENT0	Go
1080h	IIDX	Interrupt index	GEN_EVENT1	Go
1088h	IMASK	Interrupt mask	GEN_EVENT1	Go
1090h	RIS	Raw interrupt status	GEN_EVENT1	Go
1098h	MIS	Masked interrupt status	GEN_EVENT1	Go
10A0h	ISET	Interrupt set	GEN_EVENT1	Go
10A8h	ICLR	Interrupt clear	GEN_EVENT1	Go
10E0h	EVT_MODE	Event Mode		Go
10FCh	DESC	Module Description		Go
1100h	CCPD	CCP Direction		Go
1104h	ODIS	Output Disable		Go
1108h	CCLKCTL	Counter Clock Control Register		Go
110Ch	CPS	Clock Prescale Register		Go
1110h	CPSV	Clock prescale count status register		Go
1114h	CTTRIGCTL	Timer Cross Trigger Control Register		Go
111Ch	CTTRIG	Timer Cross Trigger Register		Go
1120h	FSCTL	Fault Source Control		Go
1124h	GCTL	Global control register		Go
1800h	CTR	Counter Register		Go
1804h	CTRCTL	Counter Control Register		Go
1808h	LOAD	Load Register		Go
1810h + formula	CC_01_y	Capture or Compare Register 0/1		Go

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Table 17-137. TIMG12_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1818h + formula	CC_23_y	Capture or Compare Register 2/3		Go
1820h + formula	CC_45_y	The CC_45 register are a registers which can be used as compare to the current CTR to create an events CC4U, CC4D, CC5U and CC5D.		Go
1830h + formula	CCCTL_01_y	Capture or Compare Control Registers 0/1		Go
1838h + formula	CCCTL_23_y	Capture or Compare Control Registers 2/3		Go
1840h + formula	CCCTL_45_y	Capture or Compare Control Registers 4/5		Go
1850h + formula	OCTL_01_y	CCP Output Control Registers 0/1		Go
1858h + formula	OCTL_23_y	CCP Output Control Registers 2/3		Go
1870h + formula	CCACT_01_y	Capture or Compare Action Registers 0/1		Go
1878h + formula	CCACT_23_y	Capture or Compare Action Registers 2/3		Go
1880h + formula	IFCTL_01_y	Input Filter Control Register 0/1		Go
1888h + formula	IFCTL_23_y	Input Filter Control Register 2/3		Go
18A0h	PL	Phase Load Register		Go
18A4h	DBCTL	Dead Band insertion control register		Go
18B0h	TSEL	Trigger Select Register		Go
18B4h	RC	Repeat counter Register		Go
18B8h	RCLD	Repeat counter load Register		Go
18BCh	QDIR	QEI Count Direction Register		Go
18D0h	FCTL	Fault Control Register		Go
18D4h	FIFCTL	Fault input Filter control register		Go

Complex bit access types are encoded to fit into small table cells. Table 17-80 shows the codes that are used for access types in this section.

Table 17-138. TIMG12_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		

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Table 17-138. TIMG12_REGS Access Type Codes (continued)

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 17-83 and described in Table 17-81.

Return to the Summary Table.

Register to control the power state

Figure 17-83. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 17-140. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 17-84 and described in Table 17-82.

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Register to control reset assertion and de-assertion

Figure 17-84. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 17-142. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 17-85 and described in Table 17-83.

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peripheral enable and reset status

Figure 17-85. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 17-144. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 CLKDIV Register (Offset = 1000h) [Reset = 00000000h]

CLKDIV is shown in Figure 17-86 and described in Table 17-84.

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This register is used to specify module-specific divide ratio of the functional clock

Figure 17-86. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 17-146. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

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5 CLKSEL Register (Offset = 1008h) [Reset = 00000000h]

CLKSEL is shown in Figure 17-87 and described in Table 17-85.

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Clock Source Select Register

Figure 17-87. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	BUSCLK_SEL	MFCLK_SEL	LFCLK_SEL	RESERVED
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-148. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	RESERVED	R/W	0h	Reserved
3	BUSCLK_SEL	R/W	0h	Selects BUSCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
2	MFCLK_SEL	R/W	0h	Selects MFCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
1	LFCLK_SEL	R/W	0h	Selects LFCLK as clock source if enabled 0h = Does not select this clock as a source 1h = Select this clock as a source
0	RESERVED	R/W	0h	

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6 PDBGCTL Register (Offset = 1018h) [Reset = 00000000h]

PDBGCTL is shown in Figure 17-88 and described in Table 17-86.

Return to the Summary Table.

This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 17-88. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 17-150. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft halt boundary control. This function is only available, if [FREE] is set to 'STOP' 0h = The peripheral will halt immediately, even if the resultant state will result in corruption if the system is restarted 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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7 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 17-89 and described in Table 17-87.

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This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-89. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-152. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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8 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 17-90 and described in Table 17-88.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-90. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-154. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-154. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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9 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 17-91 and described in Table 17-89.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-91. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-156. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-156. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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10 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 17-92 and described in Table 17-90.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-92. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-158. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-158. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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11 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 17-93 and described in Table 17-91.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-93. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-160. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-160. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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12 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 17-94 and described in Table 17-92.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-94. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-162. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-162. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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13 IIDX Register (Offset = 1050h) [Reset = 00000000h] (GEN_EVENT0)

IIDX is shown in Figure 17-95 and described in Table 17-93.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-95. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-164. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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14 IMASK Register (Offset = 1058h) [Reset = 00000000h] (GEN_EVENT0)

IMASK is shown in Figure 17-96 and described in Table 17-94.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-96. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-166. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-166. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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15 RIS Register (Offset = 1060h) [Reset = 00000000h] (GEN_EVENT0)

RIS is shown in Figure 17-97 and described in Table 17-95.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-97. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-168. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-168. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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16 MIS Register (Offset = 1068h) [Reset = 00000000h] (GEN_EVENT0)

MIS is shown in Figure 17-98 and described in Table 17-96.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-98. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-170. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-170. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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17 ISET Register (Offset = 1070h) [Reset = 00000000h] (GEN_EVENT0)

ISET is shown in Figure 17-99 and described in Table 17-97.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-99. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-172. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-172. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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18 ICLR Register (Offset = 1078h) [Reset = 00000000h] (GEN_EVENT0)

ICLR is shown in Figure 17-100 and described in Table 17-98.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-100. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-174. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-174. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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19 IIDX Register (Offset = 1080h) [Reset = 00000000h] (GEN_EVENT1)

IIDX is shown in Figure 17-101 and described in Table 17-99.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 17-101. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 17-176. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 01h = Interrupt Source: Zero event (Z) 02h = nterrupt Source: Load event (L) 05h = Interrupt Source: Capture or compare down event (CCD0) 06h = Interrupt Source: Capture or compare down event (CCD1) 07h = Interrupt Source: Capture or compare down event (CCD2) 08h = Interrupt Source: Capture or compare down event (CCD3) 09h = Interrupt Source: Capture or compare up event (CCU0) 0Ah = Interrupt Source: Capture or compare up event (CCU1) 0Bh = Interrupt Source: Capture or compare up event (CCU2) 0Ch = Interrupt Source: Capture or compare up event (CCU3) 0Dh = Interrupt Source: Compare down event (CCD4) 0Eh = Interrupt Source: Compare down event (CCD5) 0Fh = Interrupt Source: Compare down event (CCU4) 10h = Interrupt Source: Compare down event (CCU5) 19h = Interrupt Source: Fault Event generated an interrupt. (F) 1Ah = Interrupt Source: Trigger overflow (TOV) 1Bh = Interrupt Source: Repeat Counter Zero (REPC) 1Ch = Interrupt Source: Direction Change (DC) 1Dh = Interrupt Source:QEI Incorrect state transition error (QEIERR)

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20 IMASK Register (Offset = 1088h) [Reset = 00000000h] (GEN_EVENT1)

IMASK is shown in Figure 17-102 and described in Table 17-100.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 17-102. IMASK Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 17-178. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	QEIERR	R/W	0h	QEIERR Event mask 0h = Disable Event 1h = Enable Event
27	DC	R/W	0h	Direction Change Event mask 0h = Disable Event 1h = Enable Event
26	REPC	R/W	0h	Repeat Counter Zero Event mask 0h = Disable Event 1h = Enable Event
25	TOV	R/W	0h	Trigger Overflow Event mask 0h = Disable Event 1h = Enable Event
24	F	R/W	0h	Fault Event mask 0h = Disable Event 1h = Enable Event
23-16	RESERVED	R/W	0h	
15	CCU5	R/W	0h	Compare UP event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CCU4	R/W	0h	Compare UP event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
13	CCD5	R/W	0h	Compare DN event mask CCP5 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	CCD4	R/W	0h	Compare DN event mask CCP4 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 17-178. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R/W	0h	Capture or Compare UP event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	CCU2	R/W	0h	Capture or Compare UP event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	CCU1	R/W	0h	Capture or Compare UP event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	CCU0	R/W	0h	Capture or Compare UP event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	CCD3	R/W	0h	Capture or Compare DN event mask CCP3 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	CCD2	R/W	0h	Capture or Compare DN event mask CCP2 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	CCD1	R/W	0h	Capture or Compare DN event mask CCP1 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	CCD0	R/W	0h	Capture or Compare DN event mask CCP0 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3-2	RESERVED	R/W	0h	
1	L	R/W	0h	Load Event mask 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	Z	R/W	0h	Zero Event mask 0h = Disable Event 1h = Enable Event

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21 RIS Register (Offset = 1090h) [Reset = 00000000h] (GEN_EVENT1)

RIS is shown in Figure 17-103 and described in Table 17-101.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 17-103. RIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-180. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR, set on an incorrect state transition on the encoder interface. 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCU4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCD5 0h = Event Cleared 1h = Event Set

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Table 17-180. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CCD4	R	0h	Compare down event generated an interrupt CCD4 0h = Event Cleared 1h = Event Set
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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22 MIS Register (Offset = 1098h) [Reset = 00000000h] (GEN_EVENT1)

MIS is shown in Figure 17-104 and described in Table 17-102.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 17-104. MIS Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
R-0h	R-0h	R-0h	R-0h	R-0h		R-0h	R-0h

Table 17-182. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28	QEIERR	R	0h	QEIERR 0h = Event Cleared 1h = Event Set
27	DC	R	0h	Direction Change 0h = Event Cleared 1h = Event Set
26	REPC	R	0h	Repeat Counter Zero 0h = Event Cleared 1h = Event Set
25	TOV	R	0h	Trigger overflow 0h = Event Cleared 1h = Event Set
24	F	R	0h	Fault 0h = Event Cleared 1h = Event Set
23-16	RESERVED	R	0h	
15	CCU5	R	0h	Compare up event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
14	CCU4	R	0h	Compare up event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set
13	CCD5	R	0h	Compare down event generated an interrupt CCP5 0h = Event Cleared 1h = Event Set
12	CCD4	R	0h	Compare down event generated an interrupt CCP4 0h = Event Cleared 1h = Event Set

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Table 17-182. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	R	0h	Capture or compare up event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
10	CCU2	R	0h	Capture or compare up event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
9	CCU1	R	0h	Capture or compare up event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
8	CCU0	R	0h	Capture or compare up event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
7	CCD3	R	0h	Capture or compare down event generated an interrupt CCP3 0h = Event Cleared 1h = Event Set
6	CCD2	R	0h	Capture or compare down event generated an interrupt CCP2 0h = Event Cleared 1h = Event Set
5	CCD1	R	0h	Capture or compare down event generated an interrupt CCP1 0h = Event Cleared 1h = Event Set
4	CCD0	R	0h	Capture or compare down event generated an interrupt CCP0 0h = Event Cleared 1h = Event Set
3-2	RESERVED	R	0h	
1	L	R	0h	Load event generated an interrupt. 0h = Event Cleared 1h = Event Set
0	Z	R	0h	Zero event generated an interrupt. 0h = Event Cleared 1h = Event Set

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23 ISET Register (Offset = 10A0h) [Reset = 00000000h] (GEN_EVENT1)

ISET is shown in Figure 17-105 and described in Table 17-103.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 17-105. ISET Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-184. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event SET 0h = Writing 0 has no effect. 1h = Event Set
27	DC	W	0h	Direction Change event SET 0h = Writing 0 has no effect. 1h = Event Set
26	REPC	W	0h	Repeat Counter Zero event SET 0h = Writing 0 has no effect. 1h = Event Set
25	TOV	W	0h	Trigger Overflow event SET 0h = Writing 0 has no effect. 1h = Event Set
24	F	W	0h	Fault event SET 0h = Writing 0 has no effect. 1h = Event Set
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
14	CCU4	W	0h	Compare up event 4 SET 0h = Writing 0 has no effect. 1h = Event Set
13	CCD5	W	0h	Compare down event 5 SET 0h = Writing 0 has no effect. 1h = Event Set
12	CCD4	W	0h	Compare down event 4 SET 0h = Writing 0 has no effect. 1h = Event Set

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Table 17-184. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
10	CCU2	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
9	CCU1	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
8	CCU0	W	0h	Capture or compare up event SET 0h = Writing 0 has no effect. 1h = Event Set
7	CCD3	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
6	CCD2	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
5	CCD1	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
4	CCD0	W	0h	Capture or compare down event SET 0h = Writing 0 has no effect. 1h = Event Set
3-2	RESERVED	W	0h	
1	L	W	0h	Load event SET 0h = Writing 0 has no effect. 1h = Event Set
0	Z	W	0h	Zero event SET 0h = Writing 0 has no effect. 1h = Event Set

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24 ICLR Register (Offset = 10A8h) [Reset = 00000000h] (GEN_EVENT1)

ICLR is shown in Figure 17-106 and described in Table 17-104.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 17-106. ICLR Register

31	30	29	28	27	26	25	24
RESERVED			QEIERR	DC	REPC	TOV	F
W-0h			W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
CCU5	CCU4	CCD5	CCD4	CCU3	CCU2	CCU1	CCU0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CCD3	CCD2	CCD1	CCD0	RESERVED		L	Z
W-0h	W-0h	W-0h	W-0h	W-0h		W-0h	W-0h

Table 17-186. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	W	0h	
28	QEIERR	W	0h	QEIERR event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
27	DC	W	0h	Direction Change event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
26	REPC	W	0h	Repeat Counter Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
25	TOV	W	0h	Trigger Overflow event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
24	F	W	0h	Fault event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
23-16	RESERVED	W	0h	
15	CCU5	W	0h	Compare up event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
14	CCU4	W	0h	Compare up event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
13	CCD5	W	0h	Compare down event 5 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
12	CCD4	W	0h	Compare down event 4 CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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Table 17-186. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CCU3	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
10	CCU2	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
9	CCU1	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
8	CCU0	W	0h	Capture or compare up event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
7	CCD3	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
6	CCD2	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
5	CCD1	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
4	CCD0	W	0h	Capture or compare down event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
3-2	RESERVED	W	0h	
1	L	W	0h	Load event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear
0	Z	W	0h	Zero event CLEAR 0h = Writing 0 has no effect. 1h = Event Clear

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25 EVT_MODE Register (Offset = 10E0h) [Reset = 00000029h]

EVT_MODE is shown in Figure 17-107 and described in Table 17-105.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 17-107. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		EVT2_CFG		EVT1_CFG		EVT0_CFG	
R/W-0h		R-2h		R-2h		R-1h	

Table 17-188. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-4	EVT2_CFG	R	2h	Event line mode select for event corresponding to GEN_EVENT1 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
3-2	EVT1_CFG	R	2h	Event line mode select for event corresponding to GEN_EVENT0 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.
1-0	EVT0_CFG	R	1h	Event line mode select for event corresponding to CPU_INT 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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26 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 17-108 and described in Table 17-106.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 17-108. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				INSTNUM				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 17-190. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	1111h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	0h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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27 CCPD Register (Offset = 1100h) [Reset = 00000000h]

CCPD is shown in Figure 17-109 and described in Table 17-107.

Return to the Summary Table.

CCP Direction. Controls whether CCP is used as an input or an output.

Figure 17-109. CCPD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				RESERVED	C0CCP2	C0CCP1	C0CCP0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-192. CCPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	RESERVED	R/W	0h	Reserved
2	C0CCP2	R/W	0h	CCP2 direction 0h = input 1h = Output
1	C0CCP1	R/W	0h	CCP1 direction 0h = Input 1h = Output
0	C0CCP0	R/W	0h	CCP0 direction 0h = Input 1h = Output

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28 ODIS Register (Offset = 1104h) [Reset = 00000000h]

ODIS is shown in Figure 17-110 and described in Table 17-108.

Return to the Summary Table.

The ODIS register output is inverted and then ANDed with the output signal selected by the OCTL register CCPO field (before conditional inversion) to allow software the ability to hold the CCP output low during configuration or shutdown.

Figure 17-110. ODIS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				C0CCP3	C0CCP2	C0CCP1	C0CCP0
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-194. ODIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	C0CCP3	R/W	0h	Counter CCP3 Disable Mask Defines whether CCP3 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to occpout[2]. 1h = CCP output occpout[3] is forced low.
2	C0CCP2	R/W	0h	Counter CCP2 Disable Mask Defines whether CCP2 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[2] is forced low.
1	C0CCP1	R/W	0h	Counter CCP1 Disable Mask Defines whether CCP0 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[1] is forced low.
0	C0CCP0	R/W	0h	Counter CCP0 Disable Mask Defines whether CCP0 of Counter n is forced low or not 0h = Output function as selected by the OCTL register CCPO field are provided to output inversion block. 1h = CCP output occpout[0] is forced low.

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29 CCLKCTL Register (Offset = 1108h) [Reset = 00000000h]

CCLKCTL is shown in Figure 17-111 and described in Table 17-109.

Return to the Summary Table.

The CCLKCTL register provides a SW mechanism for gating the TIMER clock if the module is expected not to be used but the power domain is alive. This effectively puts the IP in an IDLE state

Figure 17-111. CCLKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							CLKEN
R/W-0h							R/W-0h

Table 17-196. CCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	CLKEN	R/W	0h	Clock Enable Disables the clock gating to the module. SW has to explicitly program the value to 0 to gate the clock. 0h = Clock is disabled. 1h = Clock is enabled

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30 CPS Register (Offset = 110Ch) [Reset = 00000000h]

CPS is shown in Figure 17-112 and described in Table 17-110.

Return to the Summary Table.

The CPS register provides the value for the clock pre-scaler.

Figure 17-112. CPS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PCNT							
R/W-0h																								R/W-0h							

Table 17-198. CPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	PCNT	R/W	0h	Pre-Scale Count This field specifies the pre-scale count value. The selected TIMCLK source is divided by a value of (PCNT+1). A PCNT value of 0 divides TIMCLK by 1, effectively bypassing the divider. A PCNT value of greater than 0 divides the TIMCLK source generating a slower clock 0h = Minimum value FFh = Maximum Value

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31 CPSV Register (Offset = 1110h) [Reset = 00000000h]

CPSV is shown in Figure 17-113 and described in Table 17-111.

Return to the Summary Table.

The CPSV register provides the ability to read the current clock prescale count value.

Figure 17-113. CPSV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CPSVAL							
R-0h																								R-0h							

Table 17-200. CPSV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	CPSVAL	R	0h	Current Prescale Count Value 0h = Minimum value FFh = Maximum Value

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32 CTTRIGCTL Register (Offset = 1114h) [Reset = 00000000h]

CTTRIGCTL is shown in Figure 17-114 and described in Table 17-112.

Return to the Summary Table.

Cross Timer Trigger Control Register
This register is used to control the cross trigger connections for enables and faults of different timer instances in the same power domain. Please refer to sections Timer Module Cross Trigger (In/Out) and Fault Cross Triggering for details.

Figure 17-114. CTTRIGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				EVTCTTRIGSEL			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						EVTCTEN	CTEN
R/W-0h						R/W-0h	R/W-0h

Table 17-202. CTTRIGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	EVTCTTRIGSEL	R/W	0h	Used to Select the subscriber port that should be used for input cross trigger. 0h = Use FSUB0 as cross trigger source. 1h = Use FSUB1 as cross trigger source. 2h = Use Zero event as cross trigger source. 3h = Use Load event as cross trigger source. 4h = Use CCD0 event as cross trigger source. 5h = Use CCD1 event as cross trigger source. 6h = Use CCD2 event as cross trigger source. 7h = Use CCD3 event as cross trigger source. 8h = Use CCU0 event as cross trigger source. 9h = Use CCU1 event as cross trigger source. Ah = Use CCU2 event as cross trigger source. Bh = Use CCU3 event as cross trigger source.
15-2	RESERVED	R/W	0h	
1	EVTCTEN	R/W	0h	Enable the Input Trigger Conditions to the Timer module as a condition for Cross Triggers. 0h = Cross trigger generation disabled. 1h = Cross trigger generation enabled
0	CTEN	R/W	0h	Timer Cross trigger enable. This field is used to enable whether the SW or HW logic can generate a timer cross trigger event in the system. These cross triggers are connected to the respective timer trigger in of the other timer IPs in the SOC power domain. The timer cross trigger is essentially the combined logic of the HW and SW conditions controlling EN bit in the CTRCTL register. 0h = Cross trigger generation disabled. 1h = Cross trigger generation enabled

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33 CTTRIG Register (Offset = 111Ch) [Reset = 00000000h]

CTTRIG is shown in Figure 17-115 and described in Table 17-113.

Return to the Summary Table.

Cross Timer Trigger Register
This register is used to trigger the timer instances connected and enabled using CTTRIGCTL and CTTRIGMSK registers.

Figure 17-115. CTTRIG Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							TRIG
W-0h							W-0h

Table 17-204. CTTRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	TRIG	W	0h	Generate Cross Trigger This bit when programmed will generate a synchronized trigger condition all the cross trigger enabled Timer instances including current timer instance. 0h = Cross trigger generation disabled 1h = Generate Cross trigger pulse

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34 FSCTL Register (Offset = 1120h) [Reset = 00000000h]

FSCTL is shown in Figure 17-116 and described in Table 17-114.

Return to the Summary Table.

The FSCTL register controls the fault source selection and enable. There are 5 input fault sources either through synchronous path processing or asynchronous path.

Figure 17-116. FSCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	FEX2EN	FEX1EN	FEX0EN	FAC2EN	FAC1EN	FAC0EN	FCEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17-206. FSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6	FEX2EN	R/W	0h	This field controls whether the fault is caused by external fault pin 2. 0h = Disable 1h = Enable
5	FEX1EN	R/W	0h	This field controls whether the fault is caused by external fault pin 1. 0h = Disable 1h = Enable
4	FEX0EN	R/W	0h	This field controls whether the fault is caused by external fault pin 0. 0h = Disable 1h = Enable
3	FAC2EN	R/W	0h	This field controls whether the fault is caused by COMP2 output. 0h = Disable 1h = Enable
2	FAC1EN	R/W	0h	This field controls whether the fault is caused by COMP1 output. 0h = Disable 1h = Enable
1	FAC0EN	R/W	0h	This field controls whether the fault signal is caused by COMP0 output. 0h = Disable 1h = Enable
0	FCEN	R/W	0h	This field controls whether the fault is caused by the system clock fault. 0h = Disable 1h = Enable

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35 GCTL Register (Offset = 1124h) [Reset = 00000000h]

GCTL is shown in Figure 17-117 and described in Table 17-115.

Return to the Summary Table.

Global control register

Figure 17-117. GCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							SHDWLDEN
R/W-0h							R/W-0h

Table 17-208. GCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	SHDWLDEN	R/W	1h	Enables shadow to active load of bufferred registers and register fields. 0h = Disable 1h = Enable

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36 CTR Register (Offset = 1800h) [Reset = 00000000h]

CTR is shown in Figure 17-118 and described in Table 17-116.

Return to the Summary Table.

This is the TIMER counter register.
This can be set by SW. However, the writes will be unpredictable if the software tries to set a value while the counter is running.

Figure 17-118. CTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCTR																															
R/W-0h																															

Table 17-210. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCTR	R/W	0h	Current Counter value 0h = Minimum value FFFFFFFFh = Maximum Value

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37 CTRCTL Register (Offset = 1804h) [Reset = 0000FF80h]

CTRCTL is shown in Figure 17-119 and described in Table 17-117.

Return to the Summary Table.

This register provides control over the counter operation.
The configuration can change as well as setting the EN bit in a single write.
There is no requirement to change the configuration first and then do an additional write to set the EN bit.

Figure 17-119. CTRCTL Register

31	30	29	28	27	26	25	24
RESERVED		CVAE		RESERVED			PLEN
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
SLZERCNEZ	RESERVED			FRB	FB	DRB	RESERVED
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CZC				CAC		CLC	
R/W-7h				R/W-7h		R/W-7h	
7	6	5	4	3	2	1	0
CLC	RESERVED	CM		REPEAT			EN
R/W-7h	R/W-0h	R/W-0h		R/W-0h			R/W-0h

Table 17-212. CTRCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29-28	CVAE	R/W	0h	Counter Value After Enable. This field specifies the initialization condition of the counter when the EN bit is changed from 0 to 1 by a write to the CTRCTL register. Note that an external event can also cause the EN bit to go active. 0h = The counter is set to the LOAD register value 1h = The counter value is unchanged from its current value which could have been initialized by software 2h = The counter is set to zero
27-25	RESERVED	R/W	0h	
24	PLEN	R/W	0h	Phase Load Enable. This bit allows the timer to have phase load feature. 0h = Disabled 1h = Enabled
23	SLZERCNEZ	R/W	0h	Suppress Load and Zero Events if Repeat Counter is Not Equal to Zero. This bit suppresses the generation of the Z (zero) and L (load) events from the counter when the repeat counter (RC) value is not 0. 0h = Disabled. Z and L events are always generated from the counter when their conditions are generated. 1h = Enabled. Z and L events are generated from the counter when their conditions are generated and the RC register value is 0.
22-20	RESERVED	R/W	0h	
19	FRB	R/W	0h	Fault Resume Behavior This bit specifies what the device does following the release/exit of fault condition. 0h = Resume counting 1h = Perform the action as specified by the CVAE field.

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Table 17-212. CTRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	FB	R/W	0h	Fault Behavior This bit specifies whether the counter continues running or suspends during a fault mode. There is a separate control under REPEAT to indicate whether counting is to suspend at next Counter==0 0h = Continues counting 1h = Suspends counting
17	DRB	R/W	0h	Debug Resume Behavior This bit specifies what the device does following the release/exit of debug mode. 0h = Resume counting 1h = Perform the action as specified by the CVAE field.
16	RESERVED	R/W	0h	
15-13	CZC	R/W	7h	Counter Zero Control This field specifies what controls the counter operation with respect to zeroing the counter value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 ZCOND 1h = CCCTL_1 ZCOND 2h = CCCTL_2 ZCOND This value exists when there are 4 channels. 3h = CCCTL_3 ZCOND This value exists when there are 4 channels. 4h = Controlled by 2-input QEI mode This value exists when TIMER support QEI feature. 5h = Controlled by 3-input QEI mode This value exists when TIMER support QEI feature.
12-10	CAC	R/W	7h	Counter Advance Control. This field specifies what controls the counter operation with respect to advancing (incrementing or decrementing) the counter value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 ACOND 1h = CCCTL_1 ACOND 2h = CCCTL_2 ACOND This value exists when there are 4 channels. 3h = CCCTL_3 ACOND This value exists when there are 4 channels. 4h = Controlled by 2-input QEI mode This value exists when TIMER support QEI feature. 5h = Controlled by 3-input QEI mode This value exists when TIMER support QEI feature.
9-7	CLC	R/W	7h	Counter Load Control. This field specifies what controls the counter operation with respect to setting the counter to the LD register value. Encodings 1-3 are present based on the CCPC parameter value. Bits 4-5 are present based on the HQEI parameter value. Any encodings not provided are documented as reserved. 0h = CCCTL_0 LCOND 1h = CCCTL_1 LCOND 2h = CCCTL_2 LCOND This value exists when there are 4 channels. 3h = CCCTL_3 LCOND This value exists when there are 4 channels. 4h = Controlled by 2 input QEI mode. This value exists when TIMER support QEI feature. 5h = Controlled by 3 input QEI mode. This value exists when TIMER support QEI feature.
6	RESERVED	R/W	0h	

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Table 17-212. CTRCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	CM	R/W	0h	Count Mode 0h = Down 1h = Up/Down 2h = Counter counts up.
3-1	REPEAT	R/W	0h	Repeat. The repeat bit controls whether the counter continues to advance following a zero event, or the exiting of a debug or fault condition. If counting down, a zero event is followed by a load at the next advance condition. If counting up-down, a zero event is followed by an advance event (+1). The intent of encoding 3 is that if the debug condition is in effect, the generation of the load pulse is deferred until the debug condition is over. This allows the counter to reach zero before counting is suspended. 0h = Does not automatically advance following a zero event. 1h = Continues to advance following a zero event. 2h = Reserved 3h = Continues to advance following a zero event if the debug mode is not in effect, or following the release of the debug mode. 4h = Reserved
0	EN	R/W	0h	Counter Enable. This bit allows the timer to advance This bit is automatically cleared if REPEAT=0 (do not automatically reload) and the counter value equals zero. CPU Write: A register write that sets the EN bit, the counter value is set per the CVAE value. Hardware: This bit may also be set as the result of an LCOND or ZCOND condition being met and the counter value changed to the load value or zero value, respectively. 0h = Disabled 1h = Enabled

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38 LOAD Register (Offset = 1808h) [Reset = 00000000h]

LOAD is shown in Figure 17-120 and described in Table 17-118.

Return to the Summary Table.

The contents of LOAD register are copied to CTR on any operation designated to do a "LOAD". The LOAD is used to compare with the CTR for generating a "Load Event" that can be used for interrupt, trigger, or signal generator actions.

Figure 17-120. LOAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD																															
R/W-0h																															

Table 17-214. LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LD	R/W	0h	Load Value 0h = Minimum value FFFFFFFFh = Maximum Value

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39 CC_01_y Register (Offset = 1810h + formula) [Reset = 00000000h]

CC_01_y is shown in Figure 17-121 and described in Table 17-119.

Return to the Summary Table.

The CC_01 register is a register that can be used as either a capture register, to capture the next CTR value on an event, or a compare to the current CTR to create an event. It cannot operate concurrently as both. There are two Capture-Compare slices of hardware for each counter, hence there are two CC_01 registers per timer. On a capture event, the next value of the CTR is loaded so that CTR and CC_01 (which captured) will be equal on the cycle that an interrupt or trigger is created from the capture action.

Offset = 1810h + (y * 4h); where y = 0h to 1h

Figure 17-121. CC_01_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-216. CC_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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40 CC_23_y Register (Offset = 1818h + formula) [Reset = 00000000h]

CC_23_y is shown in Figure 17-122 and described in Table 17-120.

Return to the Summary Table.

The CC_23 register is a register that can be used as either a capture register, to capture the next CTR value on an event, or a compare to the current CTR to create an event. It cannot operate concurrently as both. There are two Capture-Compare slices of hardware for each counter, hence there are two CC_01 registers per timer. On a capture event, the next value of the CTR is loaded so that CTR and CC_01 (which captured) will be equal on the cycle that an interrupt or trigger is created from the capture action.

Offset = 1818h + (y * 4h); where y = 0h to 1h

Figure 17-122. CC_23_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-218. CC_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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41 CC_45_y Register (Offset = 1820h + formula) [Reset = 00000000h]

CC_45_y is shown in Figure 17-123 and described in Table 17-121.

Return to the Summary Table.

The CC_45 register are a registers which can be used as compare to the current CTR to create an events CC4U, CC4D, CC5U and CC5D.

Offset = 1820h + (y * 4h); where y = 0h to 1h

Figure 17-123. CC_45_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCVAL																															
R/W-0h																															

Table 17-220. CC_45_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CCVAL	R/W	0h	Capture or compare value 0h = Minimum value FFFFFFFFh = Maximum Value

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42 CCCTL_01_y Register (Offset = 1830h + formula) [Reset = 00000000h]

CCCTL_01_y is shown in Figure 17-124 and described in Table 17-122.

Return to the Summary Table.

The CCCTL_01 registers control the operations of the respective CC registers and the counter.

Offset = 1830h + (y * 4h); where y = 0h to 1h

Figure 17-124. CCCTL_01_y Register

31	30	29	28	27	26	25	24
CC2SELD			CCACTUPD			SCERCNEZ	CC2SELU
R/W-0h			R/W-0h			R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CC2SELU		RESERVED	CCUPD			COC	RESERVED
R/W-0h		R/W-0h	R/W-0h			R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	ZCOND			RESERVED	LCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	ACOND			RESERVED	CCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 17-222. CCCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CC2SELD	R/W	0h	Selects the source second CCD event. 0h = Selects CCD from CC0. 1h = Selects CCD from CC1. 2h = Selects CCD from CC2. 3h = Selects CCD from CC3. 4h = Selects CCD from CC4. 5h = Selects CCD from CC5.

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Table 17-222. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-26	CCACTUPD	R/W	0h	CCACT shadow register Update Method This field controls how updates to the CCACT shadow register are performed 0h = Value written to the CCACT register has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR = LOAD) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = On a TRIG pulse, the value stored in CCACT_xy shadow register is loaded into CCACT_xy register.
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RC) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.

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Table 17-222. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	CC2SELU	R/W	0h	Selects the source second CCU event. 0h = Selects CCU from CC0. 1h = Selects CCU from CC1. 2h = Selects CCU from CC2. 3h = Selects CCU from CC3. 4h = Selects CCU from CC4. 5h = Selects CCU from CC5.
21	RESERVED	R/W	0h	
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event(CTR=0) or load event (CTR=LOAD) Writes to the CCx_y register are stored in shadow register and transferred to ECCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LD. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y

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Table 17-222. CCCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	COC	R/W	0h	Capture or Compare. Specifies whether the corresponding CC register is used as a capture register or a compare register (never both). 0h = Compare 1h = Capture
16-15	RESERVED	R/W	0h	
14-12	ZCOND	R/W	0h	Zero Condition. This field specifies the condition that generates a zero pulse. 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
11	RESERVED	R/W	0h	
10-8	LCOND	R/W	0h	Load Condition. Specifies the condition that generates a load pulse. 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
7	RESERVED	R/W	0h	
6-4	ACOND	R/W	0h	Advance Condition. Specifies the condition that generates an advance pulse. 0h = Each TIMCLK 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge) 5h = CCP High or Trigger assertion (level)
3	RESERVED	R/W	0h	
2-0	CCOND	R/W	0h	Capture Condition. Specifies the condition that generates a capture pulse. 0h = None (never captures) 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)

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43 CCCTL_23_y Register (Offset = 1838h + formula) [Reset = 00000000h]

CCCTL_23_y is shown in Figure 17-125 and described in Table 17-123.

Return to the Summary Table.

The CCCTL registers control the operations of the respective CC registers and the counter.

Offset = 1838h + (y * 4h); where y = 0h to 1h

Figure 17-125. CCCTL_23_y Register

31	30	29	28	27	26	25	24
CC2SELD			CCACTUPD			SCERCNEZ	CC2SELU
R/W-0h			R/W-0h			R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CC2SELU		RESERVED	CCUPD			COC	RESERVED
R/W-0h		R/W-0h	R/W-0h			R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	ZCOND			RESERVED	LCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	ACOND			RESERVED	CCOND		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 17-224. CCCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CC2SELD	R/W	0h	Selects the source second CCD event. 0h = Selects CCD from CC0. 1h = Selects CCD from CC1. 2h = Selects CCD from CC2. 3h = Selects CCD from CC3. 4h = Selects CCD from CC4. 5h = Selects CCD from CC5.

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Table 17-224. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-26	CCACTUPD	R/W	0h	CCACT shadow register Update Method This field controls how updates to the CCCACT shadow register are performed 0h = Value written to the CCACTx_y register has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=cc_xy) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR=LOAD) Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCACTx_y register are stored in shadow register and transferred to CCACTx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = On a TRIG pulse, the value stored in CCACTx_y shadow register is loaded into CCACTx_y active register.
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RCn) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.

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Table 17-224. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	CC2SELU	R/W	0h	Selects the source second CCU event. 0h = Selects CCU from CC0. 1h = Selects CCU from CC1. 2h = Selects CCU from CC2. 3h = Selects CCU from CC3. 4h = Selects CCU from CC4. 5h = Selects CCU from CC5.
21	RESERVED	R/W	0h	
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero or load event Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LDn. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y #xD 0.

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Table 17-224. CCCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	COC	R/W	0h	Capture or Compare. Specifies whether the corresponding CC register is used as a capture register or a compare register (never both). 0h = Compare 1h = Capture
16-15	RESERVED	R/W	0h	
14-12	ZCOND	R/W	0h	Zero Condition. This field specifies the condition that generates a zero pulse. 4h-Fh = Reserved 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
11	RESERVED	R/W	0h	
10-8	LCOND	R/W	0h	Load Condition. Specifies the condition that generates a load pulse. 4h-Fh = Reserved 0h = CCP edges have no effect 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)
7	RESERVED	R/W	0h	
6-4	ACOND	R/W	0h	Advance Condition. Specifies the condition that generates an advance pulse. 6h-Fh = Reserved 0h = Each TIMCLK 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge) 5h = CCP High or Trigger assertion (level)
3	RESERVED	R/W	0h	
2-0	CCOND	R/W	0h	Capture Condition. Specifies the condition that generates a capture pulse. 4h-Fh = Reserved 0h = None (never captures) 1h = Rising edge of CCP or trigger assertion edge 2h = Falling edge of CCP or trigger de-assertion edge 3h = Either edge of CCP or trigger change (assertion/de-assertion edge)

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44 CCCTL_45_y Register (Offset = 1840h + formula) [Reset = 00000000h]

CCCTL_45_y is shown in Figure 17-126 and described in Table 17-124.

Return to the Summary Table.

The CCCTL registers control the operations of the respective CC registers and the counter.

Offset = 1840h + (y * 4h); where y = 0h to 1h

Figure 17-126. CCCTL_45_y Register

31	30	29	28	27	26	25	24
RESERVED						SCERCNEZ	RESERVED
R/W-0h						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED			CCUPD			RESERVED	
R/W-0h			R/W-0h			R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 17-226. CCCTL_45_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	0h	
25	SCERCNEZ	R/W	0h	Suppress Compare Event if Repeat Counter is Not Equal to Zero This bit suppresses the generation of the compare (CCD, CCU and RC) events from the counter when the repeat counter (RC) value is not 0. 0h = CCD, CCU and RC events are always generated from the counter when their conditions are generated. 1h = CCD, CCU and RC events are generated from the counter when their conditions are generated and the RC register value is 0.
24-21	RESERVED	R/W	0h	

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Table 17-226. CCCTL_45_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-18	CCUPD	R/W	0h	Capture and Compare Update Method This field controls how updates to the shadow capture and compare register are performed (when operating in compare mode, COC=0). 0h = Writes to the CCx_y register is written to the register directly and has immediate effect. 1h = Following a zero event (CTR=0) Writes to the CCx_y register are stored in shadow register and transferred to ECCx_y in the TIMCLK cycle following CTR equals 0. 2h = Following a CCD event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 3h = Following a CCU event (CTR=CC_xy) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals the CCx_y register value. 4h = Following a zero event (CTR=0) or load event (CTR=LOAD) Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 or CTR. Equals LD. Note this update mechanism is defined for use only in configurations using up/down counting. This mode is not intended for use in down count configurations. 5h = Following a zero event (CTR=0) with repeat count also zero (RC=0). Writes to the CCx_y register are stored in shadow register and transferred to CCx_y in the TIMCLK cycle following CTR equals 0 and if RC equal 0. 6h = Following a TRIG pulse. Writes to the CCx_y register are stored in shadow register and transferred to CCx_y #xD 0.
17-0	RESERVED	R/W	0h	

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45 OCTL_01_y Register (Offset = 1850h + formula) [Reset = 00000000h]

OCTL_01_y is shown in Figure 17-127 and described in Table 17-125.

Return to the Summary Table.

The OCTL_01 register controls the CCP output of the Capture-Compare slice of the counter. This includes the ability to select the source of what is driven out along with initial condition values and final inversion options.

Offset = 1850h + (y * 4h); where y = 0h to 1h

Figure 17-127. OCTL_01_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		CCPIV	CCPOINV	CCPO			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			

Table 17-228. OCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	CCPIV	R/W	0h	CCP Initial Value This bit specifies the logical value put on the signal generator state while the counter is disabled (CTRCTL.EN == 0). 0h = Low 1h = High
4	CCPOINV	R/W	0h	CCP Output Invert The output as selected by CCPO is conditionally inverted. 0h = No inversion 1h = Invert
3-0	CCPO	R/W	0h	CCP Output Source 0h = Signal generator value (for example, PWM, triggered PWM) 1h = Load event 2h = CCU event or CCD event 4h = Zero event 5h = Capture event 6h = Fault condition 8h = Mirror CCP of first capture and compare register to other capture compare blocks 9h = Mirror CCP of second capture and compare register in other capture compare blocks Ch = Signal generator output after deadband insertion Dh = Counter direction

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46 OCTL_23_y Register (Offset = 1858h + formula) [Reset = 00000000h]

OCTL_23_y is shown in Figure 17-128 and described in Table 17-126.

Return to the Summary Table.

The OCTL register controls the CCP output of the Capture-Compare slice of the counter. This includes the ability to select the source of what is driven out along with initial condition values and final inversion options.

Offset = 1858h + (y * 4h); where y = 0h to 1h

Figure 17-128. OCTL_23_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		CCPIV	CCPOINV	CCPO			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			

Table 17-230. OCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	CCPIV	R/W	0h	CCP Initial Value This bit specifies the logical value put on the signal generator state while the counter is disabled (CTRCTL.EN == 0). 0h = Low 1h = High
4	CCPOINV	R/W	0h	CCP Output Invert The output as selected by CCPO is conditionally inverted. 0h = No inversion 1h = Invert
3-0	CCPO	R/W	0h	CCP Output Source 0h = Signal generator value (for example, PWM, triggered PWM) 1h = Load condition 2h = CCU event or CCD event 4h = Zero event 5h = Capture event 6h = Fault Condition 8h = Mirror CCP of first capture and compare register in other capture compare blocks 9h = Mirror CCP of second capture and compare register in other capture compare blocksi /bn,. Ch = Deadband Inserted Output Dh = Counter direction

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47 CCACT_01_y Register (Offset = 1870h + formula) [Reset = 00000000h]

CCACT_01_y is shown in Figure 17-129 and described in Table 17-127.

Return to the Summary Table.

The CCACT_01 register controls the actions of the signal generator of the capture-compare slice based on the events created in the counter block, the capture and compare block and debug events.

Offset = 1870h + (y * 4h); where y = 0h to 1h

Figure 17-129. CCACT_01_y Register

31	30	29	28	27	26	25	24
SWFRCACT_CMPL		SWFRCACT		FEXACT			FENACT
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
FENACT		RESERVED					CC2UACT
R/W-0h		R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
CC2UACT	RESERVED	CC2DACT		RESERVED	CUACT		RESERVED
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
CDACT		RESERVED	LACT		RESERVED	ZACT	
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	

Table 17-232. CCACT_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SWFRCACT_CMPL	R/W	0h	CCP Complimentary output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP Complimentary output value is set high 2h = CCP Complimentary output value is set low
29-28	SWFRCACT	R/W	0h	CCP Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low
27-25	FEXACT	R/W	0h	CCP Output Action on Fault Exit This field describes the resulting action of the signal generator upon exiting the fault condition. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated

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Table 17-232. CCACT_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	FENACT	R/W	0h	CCP Output Action on Fault Entry This field describes the resulting action of the signal generator upon detecting a fault. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated
21-17	RESERVED	R/W	0h	
16-15	CC2UACT	R/W	0h	CCP Output Action on CC2U event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
14	RESERVED	R/W	0h	
13-12	CC2DACT	R/W	0h	CCP Output Action on CC2D event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
11	RESERVED	R/W	0h	
10-9	CUACT	R/W	0h	CCP Output Action on Compare (Up) This field describes the resulting action of the signal generator upon detecting a compare event while counting up. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
8	RESERVED	R/W	0h	
7-6	CDACT	R/W	0h	CCP Output Action on Compare (Down) This field describes the resulting action of the signal generator upon detecting a compare event while counting down. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
5	RESERVED	R/W	0h	
4-3	LACT	R/W	0h	CCP Output Action on Load Specifies what changes occur to CCP output as the result of a load event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
2	RESERVED	R/W	0h	
1-0	ZACT	R/W	0h	CCP Output Action on Zero Specifies what changes occur to CCP output as the result of a zero event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled

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48 CCACT_23_y Register (Offset = 1878h + formula) [Reset = 00000000h]

CCACT_23_y is shown in Figure 17-130 and described in Table 17-128.

Return to the Summary Table.

The CCACT register controls the actions of the signal generator of the capture-compare slice based on the events created in the counter block, the capture and compare block and debug events.

Offset = 1878h + (y * 4h); where y = 0h to 1h

Figure 17-130. CCACT_23_y Register

31	30	29	28	27	26	25	24
SWFRCACT_CMPL		SWFRCACT		FEXACT			FENACT
R/W-0h		R/W-0h		R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
FENACT		RESERVED					CC2UACT
R/W-0h		R/W-0h					R/W-0h
15	14	13	12	11	10	9	8
CC2UACT	RESERVED	CC2DACT		RESERVED	CUACT		RESERVED
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
CDACT		RESERVED	LACT		RESERVED	ZACT	
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	

Table 17-234. CCACT_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SWFRCACT_CMPL	R/W	0h	CCP Complimentary Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP Complimentary output value is set high 2h = CCP Complimentary output value is set low
29-28	SWFRCACT	R/W	0h	CCP Output Action on Software Force Output This field describes the resulting action of software force. This action has a shadow register, which will be updated under specific condition. So that this register cannot take into effect immediately. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low
27-25	FEXACT	R/W	0h	CCP Output Action on Fault Exit This field describes the resulting action of the signal generator upon exiting the fault condition. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated

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Table 17-234. CCACT_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	FENACT	R/W	0h	CCP Output Action on Fault Entry This field describes the resulting action of the signal generator upon detecting a fault. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled 4h = CCP output value is tristated
21-17	RESERVED	R/W	0h	
16-15	CC2UACT	R/W	0h	CCP Output Action on CC2U event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
14	RESERVED	R/W	0h	
13-12	CC2DACT	R/W	0h	CCP Output Action on CC2D event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
11	RESERVED	R/W	0h	
10-9	CUACT	R/W	0h	CCP Output Action on Compare (Up) This field describes the resulting action of the signal generator upon detecting a compare event while counting up. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
8	RESERVED	R/W	0h	
7-6	CDACT	R/W	0h	CCP Output Action on Compare (Down) This field describes the resulting action of the signal generator upon detecting a compare event while counting down. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
5	RESERVED	R/W	0h	
4-3	LACT	R/W	0h	CCP Output Action on Load Specifies what changes occur to CCP output as the result of a load event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled
2	RESERVED	R/W	0h	
1-0	ZACT	R/W	0h	CCP Output Action on Zero Specifies what changes occur to CCP output as the result of a zero event. 0h = This event is disabled and a lower priority event is selected if asserting. The CCP output value is unaffected by the event. 1h = CCP output value is set high 2h = CCP output value is set low 3h = CCP output value is toggled

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49 IFCTL_01_y Register (Offset = 1880h + formula) [Reset = 00000000h]

IFCTL_01_y is shown in Figure 17-131 and described in Table 17-129.

Return to the Summary Table.

The IFCTL_01 register controls the input selection and inversion for the associated Capture-Compare slice.

Offset = 1880h + (y * 4h); where y = 0h to 1h

Figure 17-131. IFCTL_01_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			FE	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
INV	RESERVED			ISEL			
R/W-0h	R/W-0h			R/W-0h			

Table 17-236. IFCTL_01_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	FE	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to the edge detect. 0h = Bypass. 1h = Filtered.
11	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output.
10	RESERVED	R/W	0h	
9-8	FP	R/W	0h	Filter Period. This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = The division factor is 3 1h = The division factor is 5 2h = The division factor is 8

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Table 17-236. IFCTL_01_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INV	R/W	0h	Input Inversion This bit controls whether the selected input is inverted. 0h = Noninverted 1h = Inverted
6-4	RESERVED	R/W	0h	
3-0	ISEL	R/W	0h	Input Select (CCP0) This field selects the input source to the filter input. 4h-7h = Reserved 0h = CCP of the corresponding capture compare unit 1h = Input pair CCPX of the capture compare unit. For CCP0 input pair is CCP1 and for CCP1 input pair is CCP0. 2h = CCP0 of the counter 3h = Trigger 4h = XOR of CCP inputs as input source (Used in Hall input mode). 5h = subscriber 0 event as input source. 6h = subscriber 1 event as input source. 7h = Comparator 0 output. 8h = Comparator 1 output. 9h = Comparator 2 output.

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50 IFCTL_23_y Register (Offset = 1888h + formula) [Reset = 00000000h]

IFCTL_23_y is shown in Figure 17-132 and described in Table 17-130.

Return to the Summary Table.

The IFCTL register controls the input selection and inversion for the associated Capture-Compare slice.

Offset = 1888h + (y * 4h); where y = 0h to 1h

Figure 17-132. IFCTL_23_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			FE	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
INV	RESERVED			ISEL			
R/W-0h	R/W-0h			R/W-0h			

Table 17-238. IFCTL_23_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	FE	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to the edge detect. 0h = Bypass. 1h = Filtered.
11	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output.
10	RESERVED	R/W	0h	
9-8	FP	R/W	0h	Filter Period. This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = The division factor is 3 1h = The division factor is 5 2h = The division factor is 8

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Table 17-238. IFCTL_23_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	INV	R/W	0h	Input Inversion This bit controls whether the selected input is inverted. 0h = Noninverted 1h = Inverted
6-4	RESERVED	R/W	0h	
3-0	ISEL	R/W	0h	Input Select (CCP0) This field selects the input source to the filter input. 4h-7h = Reserved 0h = CCP of the corresponding capture compare unit 1h = Input pair CCPX of the capture compare unit. For CCP0 input pair is CCP1 and for CCP1 input pair is CCP0. 2h = CCP0 of the counter 3h = Trigger 4h = XOR of CCP inputs as input source (Used in Hall input mode). 5h = subscriber 0 event as input source. 6h = subscriber 1 event as input source. 7h = Comparator 0 output. 8h = Comparator 1 output. 9h = Comparator 2 output.

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51 PL Register (Offset = 18A0h) [Reset = 00000000h]

PL is shown in Figure 17-133 and described in Table 17-131.

Return to the Summary Table.

This is the phase load register.

Figure 17-133. PL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHASE															
R/W-0h																R/W-0h															

Table 17-240. PL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	PHASE	R/W	0h	Phase Load value 0h = Minimum value FFFFFFFFh = Maximum Value

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52 DBCTL Register (Offset = 18A4h) [Reset = 00000000h]

DBCTL is shown in Figure 17-134 and described in Table 17-132.

Return to the Summary Table.

The DBCTL register controls the dead band insertion of the pulse width modulated output.

Figure 17-134. DBCTL Register

31	30	29	28	27	26	25	24
RESERVED				FALLDELAY			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
FALLDELAY							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			M1_ENABLE	RISEDELAY			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
RISEDELAY							
R/W-0h							

Table 17-242. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	
27-16	FALLDELAY	R/W	0h	Fall Delay The number of TIMCLK periods inserted between the fall edge of CCP signal and the rise edge of CCP complimentary signal. 0h = Minimum value FFFh = Maximum Value
15-13	RESERVED	R/W	0h	
12	M1_ENABLE	R/W	0h	Dead Band Mode 1 Enable. 0h = Disabled 1h = Enabled
11-0	RISEDELAY	R/W	0h	Rise Delay The number of TIMCLK periods inserted between the fall edge of CCP signal and the rise edge of CCP complimentary signal. 0h = Minimum value FFFh = Maximum Value

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53 TSEL Register (Offset = 18B0h) [Reset = 00000000h]

TSEL is shown in Figure 17-135 and described in Table 17-133.

Return to the Summary Table.

The TSEL register controls the input trigger enable and selection of the trigger source. Trigger sources are generated by other SoC elements through their respective publisher ports (subscribed in by the timer's subscriber port).

Figure 17-135. TSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TE	RESERVED				ETSEL				
R/W-0h						R/W-0h	R/W-0h				R/W-0h				

Table 17-244. TSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	TE	R/W	0h	Trigger Enable. This selects whether a trigger is enabled or not for this counter 0x0 = Triggers are not used 0x1 = Triggers are used as selected by the ETSEL field 0h = Triggers are not used. 1h = Triggers are used as selected by the IE, ITSEL and ETSEL fields.
8-5	RESERVED	R/W	0h	
4-0	ETSEL	R/W	0h	External Trigger Select. This selects which System Event is used if the input filter selects trigger. Triggers 0-15 are used to connect triggers generated by other timer modules. Refer to the SoC datasheet for details related to timer trigger sources. Triggers 16 and 17 are connected to event manager subscriber ports. Event lines 18-31 are reserved for future use. 0h = TRIGx = External trigger input from TIM x. 1h = TRIGx = External trigger input from TIM x. 2h = TRIGx = External trigger input from TIM x. 3h = TRIGx = External trigger input from TIM x. 4h = TRIGx = External trigger input from TIM x. 5h = TRIGx = External trigger input from TIM x. 6h = TRIGx = External trigger input from TIM x. 7h = TRIGx = External trigger input from TIM x. 8h = TRIGx = External trigger input from TIM x. 9h = TRIGx = External trigger input from TIM x. Ah = TRIGx = External trigger input from TIM x. Bh = TRIGx = External trigger input from TIM x. Ch = TRIGx = External trigger input from TIM x. Dh = TRIGx = External trigger input from TIM x. Eh = TRIGx = External trigger input from TIM x. Fh = TRIGx = External trigger input from TIM x. 10h = TRIG_SUBx = External trigger input from subscriber port x. 11h = TRIG_SUBx = External trigger input from subscriber port x.

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54 RC Register (Offset = 18B4h) [Reset = 00000000h]

RC is shown in Figure 17-136 and described in Table 17-134.

Return to the Summary Table.

Repeat counter is to reduce interrupt overhead. The repeat counter provides the mechanism to suppress un-necessary interrupts
reducing the number of interrupts generated by each event type to 1 for the program number of periods. Specifically, the repeat timer may suppress Load, Compare (up/down, normal/shadow), and Zero events.

Figure 17-136. RC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RC							
R-0h																								R-0h							

Table 17-246. RC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RC	R	0h	Repeat Counter Value 0h = Minimum value FFh = Maximum Value

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55 RCLD Register (Offset = 18B8h) [Reset = 00000000h]

RCLD is shown in Figure 17-137 and described in Table 17-135.

Return to the Summary Table.

The load register value is transferred to the counter when the counter load input is asserted.

Figure 17-137. RCLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RCLD							
R/W-0h																								R/W-0h							

Table 17-248. RCLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	RCLD	R/W	0h	Repeat Counter Load Value This field provides the value loaded into the repeat counter at a load event following the repeat counter value equaling 0. 0h = Minimum value FFh = Maximum Value

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56 QDIR Register (Offset = 18BCh) [Reset = 00000000h]

QDIR is shown in Figure 17-138 and described in Table 17-136.

Return to the Summary Table.

The QDIR register provides the direction of count which is intended for use when operating the counter in QEI.

Figure 17-138. QDIR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DIR
R-0h															R-0h

Table 17-250. QDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	DIR	R	0h	Direction of count 0h = Down (Phase B leads Phase A) 1h = Up (Phase A leads Phase B)

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57 FCTL Register (Offset = 18D0h) [Reset = 00000000h]

FCTL is shown in Figure 17-139 and described in Table 17-137.

Return to the Summary Table.

The FCTL register controls the fault inputs, fault detection and error handling behavior.

Figure 17-139. FCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		FSENEXT2	FSENEXT1	FSENEXT0	FSENAC2	FSENAC1	FSENAC0
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TFIM	RESERVED		FL		FI	RESERVED	FIEN
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h

Table 17-252. FCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	0h	
13	FSENEXT2	R/W	0h	Specifies whether the external fault pin2 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
12	FSENEXT1	R/W	0h	Specifies whether the external fault pin1 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
11	FSENEXT0	R/W	0h	Specifies whether the external fault pin0 high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
10	FSENAC2	R/W	0h	Specifies whether the COMP2 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
9	FSENAC1	R/W	0h	Specifies whether the COMP1 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
8	FSENAC0	R/W	0h	Specifies whether the COMP0 output high/low is treated as fault condition. 0h = Fault Input is active low. 1h = Fault Input is active high.
7	TFIM	R/W	0h	Trigger Fault Input Mask Specifies whether the selected trigger participates as a fault input. If enabled and the trigger asserts, the trigger is treated as a fault. 0h = Selected trigger does not participate in fault condition generation 1h = Selected trigger participates in fault condition generation
6-5	RESERVED	R/W	0h	

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Table 17-252. FCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	FL	R/W	0h	Fault Latch mode Specifies whether the fault condition is latched and configures the latch clear conditions. 0h = Overall fault condition is not dependent on the F bit in RIS 1h = Overall fault condition is dependent on the F bit in RIS 2h = Fault condition is latched. Fault condition is cleared on a zero event if the fault input is 0. 3h = Fault condition is latched. Fault condition is cleared on a load event if the fault input is 0.
2	FI	R/W	0h	Fault Input Specifies whether the overall fault condition is dependent on the sensed fault pin. 0h = Overall Fault condition is not dependent on sensed input. 1h = Overall Fault condition is dependent on sensed input.
1	RESERVED	R/W	0h	
0	FIEN	R/W	0h	Fault Input Enable This bit enables the input for fault detection. 0h = Fault Input Disabled 1h = Fault Input Enabled

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58 FIFCTL Register (Offset = 18D4h) [Reset = 00000000h]

FIFCTL is shown in Figure 17-140 and described in Table 17-138.

Return to the Summary Table.

The FIFCTL register controls the filtering for the fault input.

Figure 17-140. FIFCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			FILTEN	CPV	RESERVED	FP	
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 17-254. FIFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	FILTEN	R/W	0h	Filter Enable This bit controls whether the input is filtered by the input filter or bypasses to go directly to the optional pre-scale filter and then to the edge detect. 0h = Bypass 1h = Filtered.
3	CPV	R/W	0h	Consecutive Period/Voting Select This bit controls whether the input filter uses a stricter consecutive period count or majority voting. 0h = Consecutive Periods. The input must be at a specific logic level for the period defined by FP before it is passed to the filter output. 1h = Voting. The filter ignores one clock of opposite logic over the filter period. I.e. Over FP samples of the input, up to 1 sample may be of an opposite logic value (glitch) without affecting the output
2	RESERVED	R/W	0h	
1-0	FP	R/W	0h	Filter Period This field specifies the sample period for the input filter. I.e. The input is sampled for FP timer clocks during filtering. 0h = Filter Period 3 1h = Filter Period 5 2h = Filter Period 8

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Chapter 18

Window Watchdog Timer (WWDT)

The window watchdog timer (WWDT) supervises code execution. If the application software does not successfully reset the window watchdog within the programmed open time window, the window watchdog generates a reset.

18.1 WWDT Overview 1001
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18.3 WWDT Interrupts & Triggers 1005
18.4 WWDT Registers 1006

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18.1 WWDT Overview

The primary function of the window watchdog timer (WWDT) is to initiate a reset when correct operation of the device has failed due to an unexpected software or system delay. The WWDT can be programmed with a predefined time window within which the application software must restart the timer, indicating that application execution is proceeding normally. If application software fails to restart the timer within the specified window, the WWDT will issue a WWDT violation signal to SYSCTL to generate a BOOTRST, which resets the peripheral and CPU state and also causes the boot configuration routine (BCR) to run.

If watchdog functionality is not required in an application, the WWDT can also be configured as a basic system interval timer which is capable of generating periodic maskable interrupts to the CPU through the WWDT CPU_INT event.

Key features of the WWDT include:

- A 25-bit counter with closed and open window spans
- Counter driven from LFCLK (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods
  - Eight selectable closed window percentages to further refine the open window span
  - Two configurable closed window spans to alter open window span after WWDT has been enabled
- Optional automatic suspension of counter when operating in low power modes
- Support for standard window watchdog mode or interval timer (nonwatchdog) mode

18.1.1 Watchdog Mode

In watchdog mode, the WWDT is configured to count up to the specified WWDT period determined by the CLKDIV and PER bits of the WWDTCTL0 register (see WWDT Period Timing Options). The WWDT period consists of a closed window span and an open window span. The WWDT counter must be restarted with the configured open window of the WWDT period, or the WWDT will assert a WWDT violation to SYSCTL and a reset will be generated.

The window watchdog timer supports detecting both a "too late" response as well as a "too early" response through the use of the closed window, as shown in Watchdog Functionality. The closed window span begins first, followed by the open window span. The WWDT can only be restarted during the open window span. Restarting the WWDT during the open window span restarts the WWDT counter and the closed window span begins again. Any attempt to restart the WWDT during the closed window span results in a violation. Following the closed window, if the WWDT is not restarted before the end of the open window, the WWDT period expires and a WWDT violation is generated.

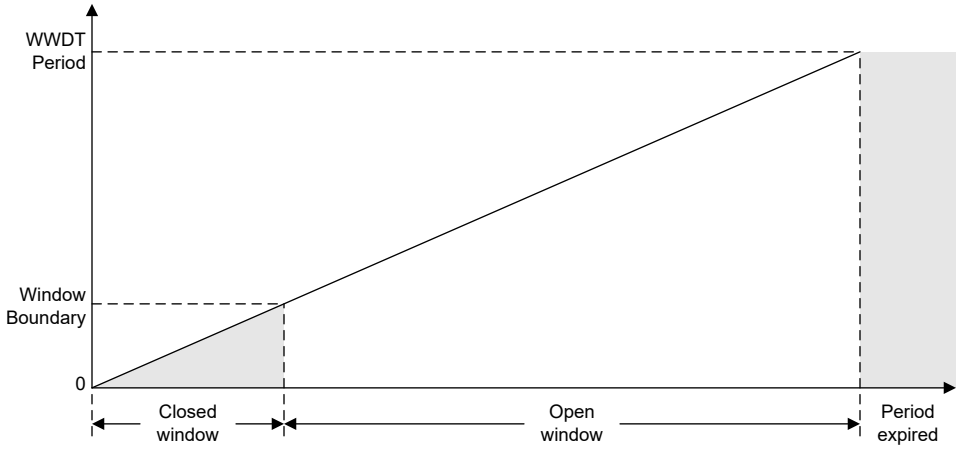


Figure 18-1. WWDT Functionality

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If the closed window functionality is not desired, it can be disabled by setting the closed window span to 0%, giving traditional watchdog timer functionality where the WWDT can be reset any time before the WWDT period expires.

18.1.2 Interval Timer Mode

The WWDT can be used in interval timer mode to generate periodic interrupts to the CPU when not using the watchdog functionality. When used in interval timer mode, a WWDT interrupt is generated when the WWDT period expires, or when an incorrect password is applied to the WWDT control registers (WWDTCTL0 and WWDTCTL1). The WWDT counter restarts itself once the WWDT period expires. A write of the RESTART value to the WWDTCNTRST register will restart the WWDT interval timer mode, keeping the period from expiring and a WWDT interrupt from generating.

18.2 WWDT Operation

The WWDT must be enabled before being configured for use through the PWREN register by writing the ENABLE bit with the correct KEY value to the PWREN register (see peripheral power enable).

The WWDT is configured through the WWDTCTL0 and WWDTCTL1 registers. These registers are password protected. Any register access (read or write) must be a 32-bit access. Write access must also include the corresponding password in the most significant byte (0xC9 for WWDTCTL0 and 0xBE for WWDTCTL1). Attempting a register write without the correct password or attempting a write with an access other than a 32-bit access generates a WWDT violation to SYSCTL, generating a BOOTRST. The password byte always reads as 0x00.

The WWDT is disabled and cleared after a SYSRST, which resets the peripherals and CPU state but does not trigger execution of the BCR, or a BOOTRST. A WWDT violation does not generate a SYSRST. Please see Resets and Device Initialization for more information on resets.

The WWDTCTL0 register sets the static configuration of the WWDT, including: the clock divider (CLKDIV), the timer period (PER), the two closed window percentages (WINDOW0 and WINDOW1), the timer mode (MODE), and the stop-in-sleep status (STISM). The WWDTCTL1 register controls which closed window percentage is being used by the WWDT through the WINSEL bit.

The first write (with a key match) to the WWDTCTL0 register enables the WWDT. Once the WWDT is enabled, the WWDTCTL0 register becomes write protected. Any attempt to write to the WWDTCTL0 register after the WWDT is enabled generates a WWDT violation to SYSCTL. In order to reconfigure the WWDT after it is enabled, the device must undergo either SYSRST or BOOTRST. The RUN bit in the WWDTSTAT register indicates that the WWDT is running.

WWDT Diagram shows the WWDT functional block diagram.

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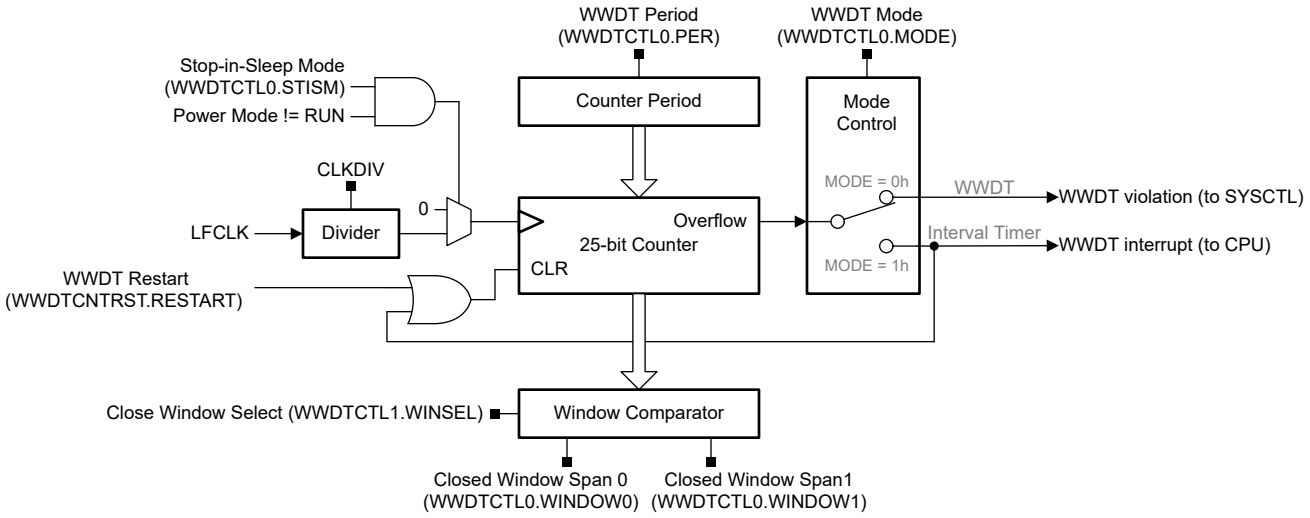


Figure 18-2. WWDT Diagram

18.2.1 Mode Selection

The WWDT operating mode (watchdog mode or interval timer mode) is selected by the MODE bit in the WWDTCTL0 register. Watchdog mode is the default mode (MODE cleared). Setting the MODE bit configures the WWDT for interval mode.

When the WWDT is in watchdog mode, the WWDT counter must be restarted within the open window period by writing the RESTART value (0x000000A7) to the WWDTCNTRST register. After a reset or restart, the WWDT counter will restart from zero. A failure to restart the WWDT within the open window or an attempt to restart the WWDT counter during the closed window will generate a WWDT violation to SYSCTL. Writing any value other than the RESTART value to the WWDTCNTRST register also generates a WWDT violation.

When the WWDT is in interval mode, the timer acts as an interval timer, generating WWDT interrupts to the CPU as specified by the WWDT period. As soon as the WWDT is enabled in interval mode, the WWDT interval timer interrupt will be asserted after the expiration of the timer. It is not necessary to restart the WWDT in interval timer mode.

18.2.2 Clock Configuration

The WWDT runs from the 32kHz low-frequency clock (LFCLK). A clock divider supports dividing the input clock from /1 (no divide) to /8 (divide-by-8) using the CLKDIV field in the WWDTCTL0 register. The default CLKDIV setting is 0x03 (32kHz divided by 4, or 8kHz).

By running from the LFCLK, the WWDT time base is independent of the main clock (MCLK) and CPU clock (CPUCLK) time base, provided that these clocks are not also configured to be running from the LFCLK. While the time base may be considered as independent and derived from a separate oscillator source, LFCLK edges are synchronized to the MCLK before sourcing the WWDT to enable simple access to the memory-mapped registers from application software. A simplified view of the clock scheme is given in WWDT Simplified Clock Source Tree. In WWDT Simplified Clock Source Tree, the internal LFOSC is configured to set the LFCLK rate, and the internal SYSOSC sets the MCLK/CPUCLK rate. Clock selection muxes and dividers are excluded from the figure to simplify the view; the complete clock tree is provided in Clock Tree.

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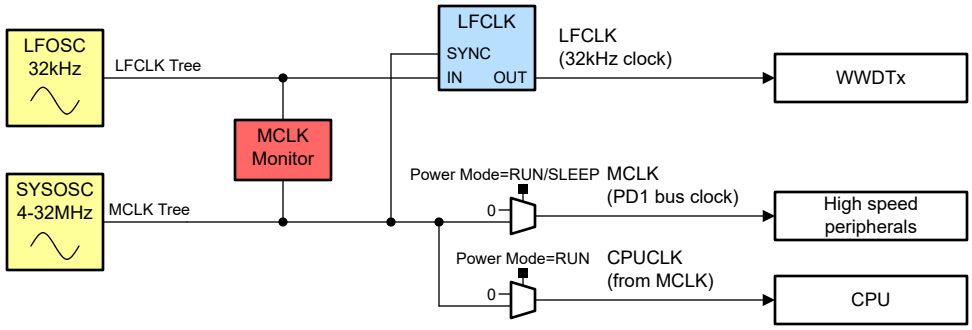


Figure 18-3. WWDT Simplified Clock Source Tree

In the event that the MCLK fails and synchronization of the LFCLK to the MCLK is lost, this failure may be detected by enabling the continuous MCLK monitor. When the MCLK monitor is enabled, a loss of MCLK is always a catastrophic failure which generates a BOOTRST within 12 LFCLK cycles. As a result, a loss of the MCLK tree, and corresponding loss of synchronization, does not prevent a BOOTRST from being generated.

Period Selection

The WWDT has a 25-bit counter which is initially stopped after a SYSRST. The WWDT period (total time interval) is set by the PER field in the WWDTCTL0 register. The total WWDT period is calculated as follows:

$$T_{WWDT} = (CLKDIV + 1) * PER_{COUNT} / 32768Hz \quad (14)$$

The total timer count PER_{COUNT} is selected to be one of 8 possible period count values, with the encoding given in WWDT Period Total Timer Count.

Table 18-1. WWDT Period Total Timer Count

PER	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
PER_{COUNT}	2^{25}	2^{21}	2^{18}	2^{15}	2^{12}	2^{10}	2^{8}	2^{6}

The combination of the period selection (PER) and clock divider (CLKDIV) enable a wide range of WWDT periods, from as short as 1.95ms to as long as 136.53 minutes. WWDT Period Timing Options gives all possible WWDT periods for a given combination of PER and CLKDIV.

Table 18-2. WWDT Period Timing Options

CLKDIV	PER							
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
	min	*min*	*s*	*s*	*s*	*ms*	*ms*	*ms*
0x0 (/1)	17.07	1.07	8.00	1.00	0.13	31.25	7.81	1.95
0x1 (/2)	34.13	2.13	16.00	2.00	0.25	62.50	15.63	3.91
0x2 (/3)	51.20	3.20	24.00	3.00	0.38	93.75	23.44	5.86
0x3 (/4)	68.27	4.27	32.00	4.00	0.50	125.00	32.25	7.81
0x4 (/5)	85.33	5.33	40.00	5.00	0.63	156.25	39.06	9.77
0x5 (/6)	102.40	6.40	48.00	6.00	0.75	187.50	46.88	11.72
0x6 (/7)	119.47	7.47	56.00	7.00	0.88	218.75	54.69	13.67
0x7 (/8)	136.53	8.53	64.00	8.00	1.00	250.00	62.50	15.63

The default setting for the WWDT upon reset is 0.5s (CLKDIV = 0x3 and PER = 0x4).

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Synchronization Delay

When starting or re-starting the WWDT counter, a maximum synchronization delay of one 32kHz clock cycle (30.5µs) can occur before the WWDT counter begins counting from zero. The periods given in WWDT Period Timing Options do not include this synchronization delay.

Closed Window Selection

Once the WWDT is enabled, the configuration of the WWDT cannot be changed except for the capability to switch the active closed window selection between two closed window spans. Configuration of two closed window spans is supported by setting the WINDOW0 and WINDOW1 fields in the WWDTCTL0 register. The WINSEL bit in the WWDTCTL1 register determines the active window (either WINDOW0 or WINDOW1). Either window can be set to one of 8 possible window settings.

Table 18-3. WWDT Window Options

WINDOW	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
Closed window	0%	12.5%	18.75%	25%	50%	75%	81.25%	87.5%

Setting a WINDOWx value to 0x0 (0% closed, 100% open) is equivalent to disabling the window function of the WWDT. In this configuration, the WWDT can be restarted at any point during the WWDT period.

By configuring both WINDOW0 and WINDOW1 within the WWDTCTL0 register, the active window selection can be changed after the WWDT has been enabled by changing the WINSEL bit. When the WWDT is restarted by writing the RESTART value to the WWDTCNTRST register, the closed window selection (WINSEL) must not be changed for at least four 32kHz clock cycles (≈122µs).

18.2.3 Low-Power Mode Behavior

The WWDT counter can be configured to continue counting when the device is in a low-power mode (CPU is disabled) or to continue to run when the device is in a low-power mode.

The STISM bit in the WWDTCTL0 register controls if the WWDT counter stops counting in sleep mode. By default, the STISM bit is cleared, indicating that the WWDT continues to count in low-power modes. To stop the WWDT from counting in low-power modes, set the STISM bit when loading the WWDTCTL0 configuration to start the WWDT. In this case, when the low-power mode is exited and the CPU returns to operation, the WWDT counter resumes counting from the same value it held before entering the low-power mode.

18.2.4 Debug Behavior

The WWDT can be configured to stop counting or continue counting when the CPU is halted for debug by the debug subsystem. By default, the WWDT stops counting when the CPU is halted for debug and the device is in a debug state. To allow the WWDT to continue to free run when the CPU is stopped for debug, set the FREE bit in the PDBGCTL register.

18.3 WWDT Interrupts & Triggers

18.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 18-4. CPU Interrupts Triggered by WWDT

NVIC Interrupt Name	Peripheral Instance Name	Register Group	WWDT Interrupt Configuration Registers	Description
WWDT	WWDT	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	WWDT interrupt. Multiple OR'd, configurable source conditions.

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18.4 WWDT Registers

This Section describes the WWDT Registers.

18.4.1 WWDT Base Address Table

Table 18-5. WWDT Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
WwdtRegs	WWDT_REGS	WWDT	0x400D_0000

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18.4.2 WWDT_REGS Registers

Table 18-6 lists the memory-mapped registers for the WWDT_REGS registers. All register offset addresses not listed in Table 18-6 should be considered as reserved locations and the register contents should not be modified.

Table 18-6. WWDT_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1018h	PDBGCTL	Peripheral Debug Control		Go
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
10E0h	EVT_MODE	Event Mode		Go
10FCh	DESC	Module Description		Go
1100h	WWDTCTL0	Window Watchdog Timer Control Register 0		Go
1104h	WWDTCTL1	Window Watchdog Timer Control Register 0		Go
1108h	WWDTCNTRST	Window Watchdog Timer Counter Reset Register		Go
110Ch	WWDTSTAT	Window Watchdog Timer Status Register		Go

Complex bit access types are encoded to fit into small table cells. Table 18-7 shows the codes that are used for access types in this section.

Table 18-7. WWDT_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 18-4 and described in Table 18-8.

Return to the Summary Table.

Register to control the power state

Figure 18-4. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 18-9. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power Note: For safety devices the power cannot be disabled once enabled. [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 18-5 and described in Table 18-9.

Return to the Summary Table.

Register to control reset assertion and de-assertion

Figure 18-5. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 18-11. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear [GPRCM.STAT.RESETSTKY] [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral Note: For safety devices a watchdog reset by software is not possible. [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 18-6 and described in Table 18-10.

Return to the Summary Table.

peripheral enable and reset status

Figure 18-6. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 18-13. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 PDBGCTL Register (Offset = 1018h) [Reset = 00000000h]

PDBGCTL is shown in Figure 18-7 and described in Table 18-11.

Return to the Summary Table.

This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 18-7. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							FREE
R/W-0h							R/W-0h

Table 18-15. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	FREE	R/W	0h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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5 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 18-8 and described in Table 18-12.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index.

Figure 18-8. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											STAT					
R-0h																											R-0h					

Table 18-17. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	STAT	R	0h	Module Interrupt Vector Value. This register provides the highest priority interrupt index. A read clears the corresponding interrupt flag in RIS and MISC. 0h = No interrupt pending 1h = Interval Timer Interrupt Interrupt Flag: INTTIM Interrupt Priority: Highest

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6 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 18-9 and described in Table 18-13.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS."

Figure 18-9. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTTIM
R/W-0h							R/W-0h

Table 18-19. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	INTTIM	R/W	0h	Interval Timer Interrupt. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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7 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 18-10 and described in Table 18-14.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 18-10. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							INTTIM
R-0h							R-0h

Table 18-21. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	INTTIM	R	0h	Interval Timer Interrupt. 0h = Interrupt did not occur 1h = Interrupt occurred

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8 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 18-11 and described in Table 18-15.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 18-11. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							INTTIM
R-0h							R-0h

Table 18-23. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	INTTIM	R	0h	Interval Timer Interrupt. 0h = Interrupt did not occur 1h = Interrupt occurred

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9 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 18-12 and described in Table 18-16.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 18-12. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTTIM
W-0h							W-0h

Table 18-25. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTTIM	W	0h	Interval Timer Interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt

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10 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 18-13 and described in Table 18-17.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 18-13. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTTIM
W-0h							W-0h

Table 18-27. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTTIM	W	0h	Interval Timer Interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt

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11 EVT_MODE Register (Offset = 10E0h) [Reset = 00000000h]

EVT_MODE is shown in Figure 18-14 and described in Table 18-18.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 18-14. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						INT0_CFG	
R/W-0h						R-0h	

Table 18-29. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	INT0_CFG	R	1h	Event line mode select for event corresponding to [IPSTANDARD.CPU_INT] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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12 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 18-15 and described in Table 18-19.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 18-15. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				INSTNUM				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 18-31. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	1F11h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	7h	Feature Set for the module *instance* 0h = Smallest value Fh = Highest possible value
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances 0h = Smallest value Fh = Highest possible value
7-4	MAJREV	R	1h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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13 WWDTCTL0 Register (Offset = 1100h) [Reset = 00000043h]

WWDTCTL0 is shown in Figure 18-16 and described in Table 18-20.

Return to the Summary Table.

Window Watchdog Timer Control 0 Register
NOTE: Write to this register is enabled after System Reset. The first successful write (key match) enables the Watchdog. When the watchdog is enabled all subsequent writes to this register activate the WWDT error signal to the ESM.

Figure 18-16. WWDTCTL0 Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED						STISM	MODE
R/W-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	WINDOW1			RESERVED	WINDOW0		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PER			RESERVED	CLKDIV		
R/W-0h	R/W-4h			R/W-0h	R/W-3h		

Table 18-33. WWDTCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow write access to this register. Writing to this register with an incorrect key activates the WWDT error signal to the ESM. Read as 0. C9h (W) = KEY to allow write access to this register
23-18	RESERVED	R/W	0h	
17	STISM	R/W	0h	Stop In Sleep Mode. The functionality of this bit requires that POLICY.HWCEN = 0. If POLICY.HWCEN = 1 the WWDT resets during sleep and needs re-configuration. Note: This bit has no effect for the global Window Watchdog as Sleep Mode is not supported. 0h = The WWDT continues to function in Sleep mode. 1h = The WWDT stops in Sleep mode and resumes where it was stopped after wakeup.
16	MODE	R/W	0h	Window Watchdog Timer Mode 0h = Window Watchdog Timer Mode. The WWDT will generate a error signal to the ESM when following conditions occur: - Timer Expiration (Timeout) - Reset WWDT during the active window closed period - Keyword violation 1h = Interval Timer Mode. The WWDT acts as an interval timer. It generates an interrupt on timeout.
15	RESERVED	R/W	0h	

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Table 18-33. WWDTCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	WINDOW1	R/W	0h	Closed window period in percentage of the timer interval. WWDTCTL1.WINSEL determines the active window setting (WWDTCTL0.WINDOW0 or WWDTCTL0.WINDOW1). 0h = 0% (No closed Window) 1h = 12.50% of the total timer period is closed window 2h = 18.75% of the total timer period is closed window 3h = 25% of the total timer period is closed window 4h = 50% of the total timer period is closed window 5h = 75% of the total timer period is closed window 6h = 81.25% of the total timer period is closed window 7h = 87.50% of the total timer period is closed window
11	RESERVED	R/W	0h	
10-8	WINDOW0	R/W	0h	Closed window period in percentage of the timer interval. WWDTCTL1.WINSEL determines the active window setting (WWDTCTL0.WINDOW0 or WWDTCTL0.WINDOW1). 0h = 0% (No closed Window) 1h = 12.50% of the total timer period is closed window 2h = 18.75% of the total timer period is closed window 3h = 25% of the total timer period is closed window 4h = 50% of the total timer period is closed window 5h = 75% of the total timer period is closed window 6h = 81.25% of the total timer period is closed window 7h = 87.50% of the total timer period is closed window
7	RESERVED	R/W	0h	
6-4	PER	R/W	4h	Timer Period of the WWDT. These bits select the total watchdog timer count. 0h = Total timer count is 2^{25} 1h = Total timer count is 2^{21} 2h = Total timer count is 2^{18} 3h = Total timer count is 2^{15} 4h = Total timer count is 2^{12} (default) 5h = Total timer count is 2^{10} 6h = Total timer count is 2^{8} 7h = Total timer count is 2^{6}
3	RESERVED	R/W	0h	
2-0	CLKDIV	R/W	3h	Module Clock Divider, Divide the clock source by CLKDIV+1. Divider values from /1 to /8 are possible. The clock divider is currently 4 bits. Bit 4 has no effect and should always be written with 0. 0h = Minimum value 7h = Maximum value

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14 WWDTCTL1 Register (Offset = 1104h) [Reset = 00000000h]

WWDTCTL1 is shown in Figure 18-17 and described in Table 18-21.

Return to the Summary Table.

Window Watchdog Timer Control 1 Register

Figure 18-17. WWDTCTL1 Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							WINSEL
R/W-0h							R/W-0h

Table 18-35. WWDTCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow write access to this register. Writing to this register with an incorrect key activates the WWDT error signal to the ESM. Read as 0. BEh (W) = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	WINSEL	R/W	0h	Close Window Select 0h = In window mode field WINDOW0 of WDDTCTL0 defines the closed window size. 1h = In window mode field WINDOW1 of WDDTCTL0 defines the closed window size.

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15 WWDTCNTRST Register (Offset = 1108h) [Reset = 00000000h]

WWDTCNTRST is shown in Figure 18-18 and described in Table 18-22.

Return to the Summary Table.

Window Watchdog Timer Counter Restart Register

Figure 18-18. WWDTCNTRST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESTART																															
R/W-0h																															

Table 18-37. WWDTCNTRST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESTART	R/W	0h	Window Watchdog Timer Counter Restart Writing 00A7h to this register restarts the WWDT Counter. Writing any other value causes an error generation to the ESM. Read as 0. 0h = Minimum value FFFFFFFFh = Maximum value

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16 WWDTSTAT Register (Offset = 110Ch) [Reset = 00000000h]

WWDTSTAT is shown in Figure 18-19 and described in Table 18-23.

Return to the Summary Table.

Window Watchdog Timer Status Register
A write to this register has no effect.

Figure 18-19. WWDTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RUN
R-0h															R-0h

Table 18-39. WWDTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	RUN	R	0h	Watchdog running status flag. 0h = Watchdog counter stopped. 1h = Watchdog running.

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Chapter 19

Crossbar (X-BAR)

The crossbars (referred to as X-BAR throughout this chapter) provide flexibility to connect device inputs, outputs, and internal resources in a variety of configurations.

19.1 Input X-BAR 1026
19.2 PWM X-BAR 1028
19.3 GPIO Output X-BAR 1031
19.4 X-BAR Flags 1034
19.5 XBAR Interrupts & Triggers 1035
19.6 XBAR Registers 1035

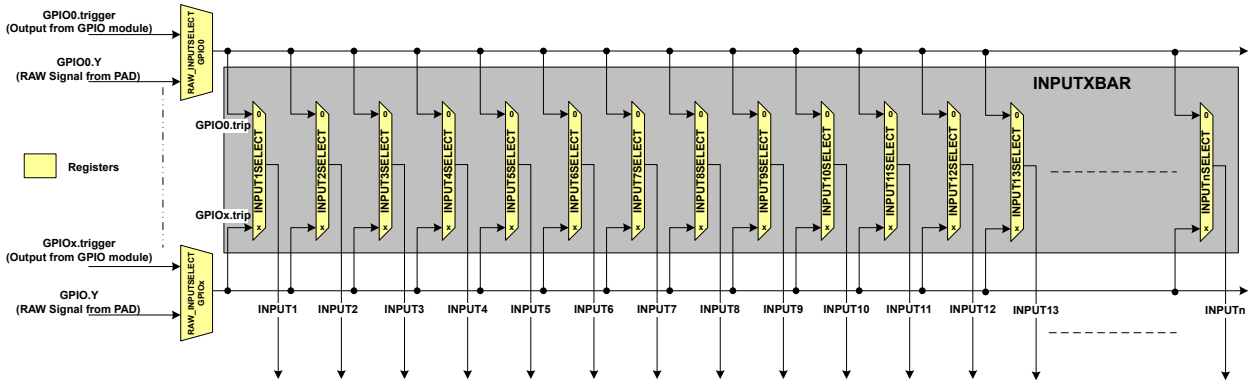
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19.1 Input X-BAR

On this device, the Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADC, eCAP, ePWM, eQEP, EtherCAT, and CMPSS. The input of each Input X-BAR instance (INPUTx) can be any GPIO, while the output of each instance connects to various IP blocks in the device. This flexibility relieves some of the constraints on peripheral muxing by allowing the user to connect any GPIO to the specified outputs of each Input X-BAR instance. Note that the GPIO selected by the Input X-BAR can be configured as either an input or an output. The Input X-BAR simply connects the signal on the input buffer to the output of the selected Input X-BAR instance. Therefore, you can do things such as route the output of a PWM to the eCAP module for a frequency test.

The Input X-BAR is configured by way of the INPUTxSELECT registers. The destinations for each INPUTx are shown in Figure 19-1. For additional details on how each Input X-BAR connects to other IP blocks throughout the device, look for references to Input X-BAR in the chapter associated with that IP. Note that the destinations of each INPUTx are fixed and are not user-configurable. For more information on configuring the Input X-BAR, see the INPUT_XBAR_REGS register definitions in the *XBAR Registers* section.

Figure 19-1. Input X-BAR Architecture



The diagram below shows this interconnect of the INPUTXBAR in the AM13E232x.

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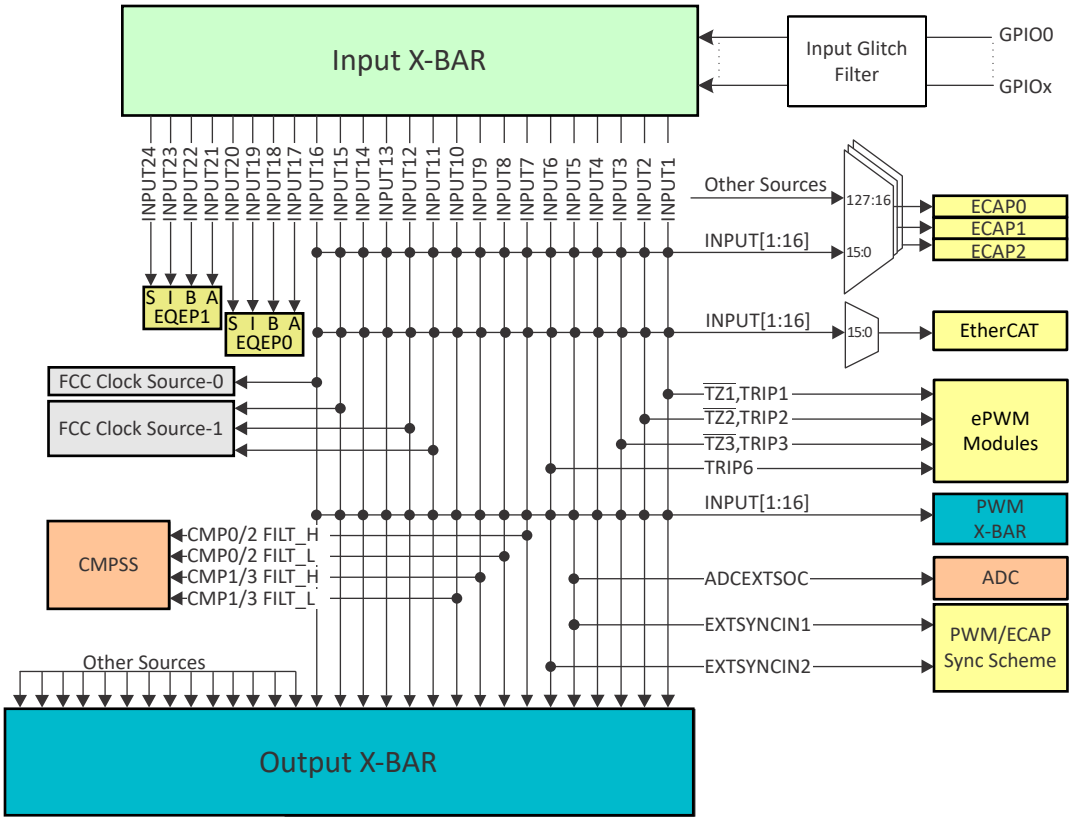


Figure 19-2. INPUTXBAR Connectivity

Note

INPUTXBARx, INPUTXBAR_INPUTx, and INPUTx (when referenced in the context of Input X-BAR) are equivalent in software and documentation.

Table 19-1. Input X-BAR Destinations

OUTPUT	ECAP	EQEP	PWM XBAR	OUTPUT XBAR	EPWM TRIP	ADC START OF CONVERSION	PWM/ ECAP/ADC SYNC	FCC	CMPSS	ECAT
1	Yes	-	Yes	Yes	TZ1, TRIP1	-	-	-	-	Yes
2	Yes	-	Yes	Yes	TZ2, TRIP2	-	-	-	-	Yes
3	Yes	-	Yes	Yes	TZ3, TRIP3	-	-	-	-	Yes
4	Yes	-	Yes	Yes	-	-	-	-	-	Yes
5	Yes	-	Yes	Yes	-	ADCEXTSOC	EXTSYNCIN1	-	-	Yes
6	Yes	-	Yes	Yes	TRIP6	-	EXTSYNCIN2	-	-	Yes
7	Yes	-	Yes	Yes	-	-	-	-	CMPSS0_EXT_FILTIN_H[1] / CMPSS2_EXT_FILTIN_H[1]	Yes

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Table 19-1. Input X-BAR Destinations (continued)

OUTPUT	ECAP	EQEP	PWM XBAR	OUTPUT XBAR	EPWM TRIP	ADC START OF CONVERSION	PWM/ ECAP/ADC SYNC	FCC	CMPSS	ECAT
8	Yes	-	Yes	Yes	-	-	-	-	CMPSS0_EXT_FILTIN_L[1] / CMPSS2_EXT_FILTIN_L[1]	Yes
9	Yes	-	Yes	Yes	-	-	-	-	CMPSS1_EXT_FILTIN_H[1] / CMPSS3_EXT_FILTIN_H[1]	Yes
10	Yes	-	Yes	Yes	-	-	-	-	CMPSS1_EXT_FILTIN_L[1] / CMPSS3_EXT_FILTIN_L[1]	Yes
11	Yes	-	Yes	Yes	-	-	-	CLK1	-	Yes
12	Yes	-	Yes	Yes	-	-	-	CLK1	-	Yes
13	Yes	-	Yes	Yes	-	-	-	-	-	Yes
14	Yes	-	Yes	Yes	-	-	-	-	-	Yes
15	Yes	-	Yes	Yes	-	-	-	CLK1	-	Yes
16	Yes	-	Yes	Yes	-	-	-	CLK0	-	Yes
17	-	EQEP0A	-	-	-	-	-	-	-	-
18	-	EQEP0B	-	-	-	-	-	-	-	-
19	-	EQEP0I	-	-	-	-	-	-	-	-
20	-	EQEP0S	-	-	-	-	-	-	-	-
21	-	EQEP1A	-	-	-	-	-	-	-	-
22	-	EQEP1B	-	-	-	-	-	-	-	-
23	-	EQEP1I	-	-	-	-	-	-	-	-
24	-	EQEP1S	-	-	-	-	-	-	-	-
25	-	-	-	-	-	-	-	-	-	-
26	-	-	-	-	-	-	-	-	-	-
27	-	-	-	-	-	-	-	-	-	-
28	-	-	-	-	-	-	-	-	-	-
29	-	-	-	-	-	-	-	-	-	-
30	-	-	-	-	-	-	-	-	-	-
31	-	-	-	-	-	-	-	-	-	-
32	-	-	-	-	-	-	-	-	-	-

19.2 PWM X-BAR

The PWM X-BAR brings 8 signals to the MCPWM and ePWM modules. Specifically, the 8 PWM X-BAR outputs are routed to the TZ1-TZ8 inputs of each of the MCPWM instances, and also connected to the TRIP4-5 and TRIP7-12 of each of the ePWM instances respectively. Note that the architecture of the PWM X-BAR is identical to the architecture of the GPIO Output X-BAR (with the exception of the output latch).

19.2.1 PWM Crossbar Architecture

The PWM X-BAR has eight outputs which are routed to both the MCPWM and ePWM module. Figure 19-3 represents the architecture of a single output, but this output is identical to the architecture of all of the other outputs.

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First, determine the signals that can be passed to the MCPWM/ePWM by referencing the PWM XBAR Mux Configuration Options. Select up to one signal for each output. Select the inputs to the PWM X-BAR using the PWMXBARGxSEL registers. All input signals are logically ORed before being passed on to the respective TZx signal on the MCPWM or TRIPx signal on the ePWM. To optionally invert the signal, set the corresponding bit in the PWMXBAROutInvert register.

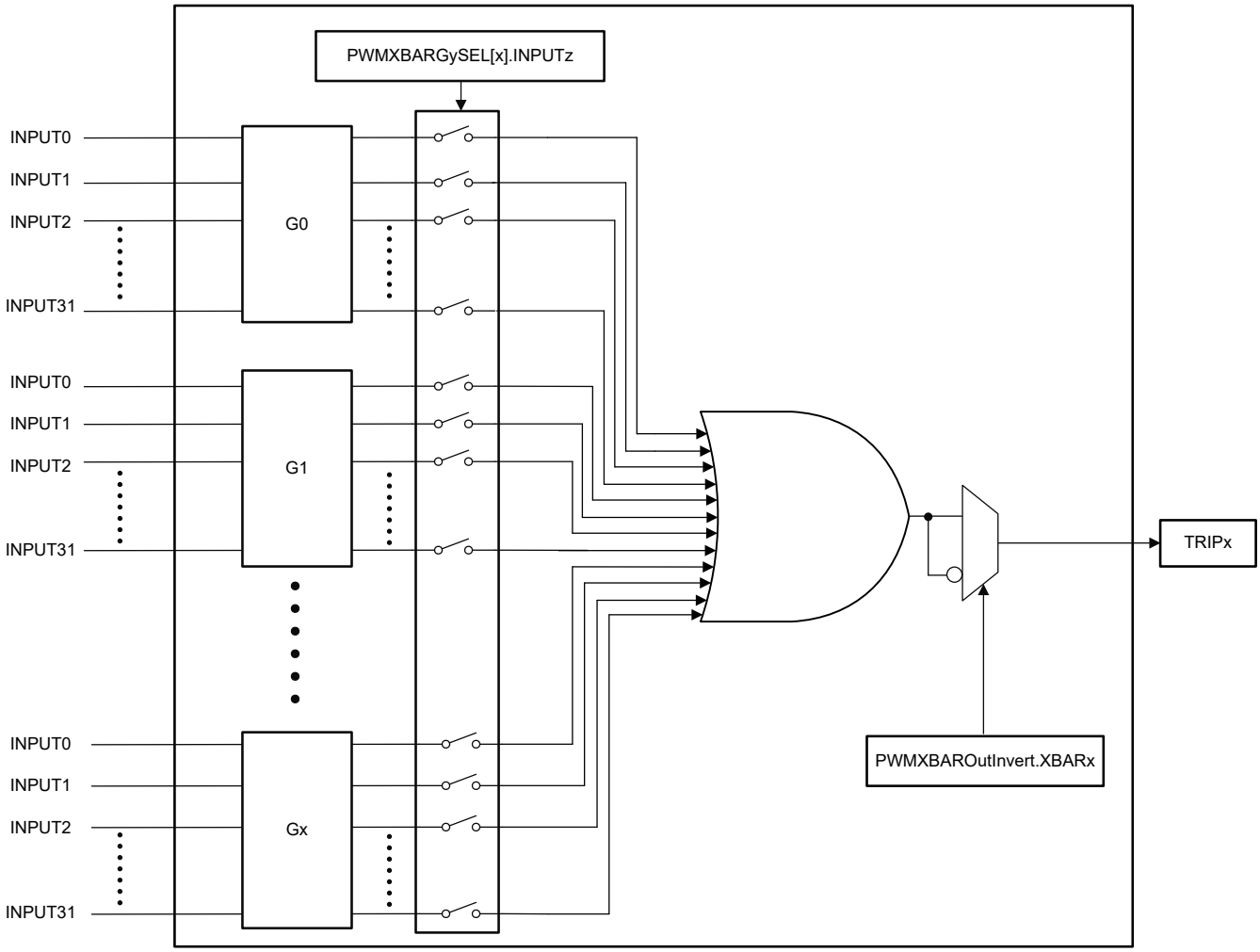


Figure 19-3. PWM X-BAR Architecture - Single Output

Table 19-2. PWM X-BAR Mux Configuration Table

Group	Bit	Input Signal
G0	0	CMPSS0_CTRIPH
G0	1	CMPSS0_CTRIPL
G0	2	CMPSS1_CTRIPH
G0	3	CMPSS1_CTRIPL
G0	4	CMPSS2_CTRIPH
G0	5	CMPSS2_CTRIPL
G0	6	CMPSS3_CTRIPH
G0	7	CMPSS3_CTRIPL
G0	8	ADC0EVT1
G0	9	ADC0EVT2
G0	10	ADC0EVT3

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Table 19-2. PWM X-BAR Mux Configuration Table (continued)

Group	Bit	Input Signal
G0	11	ADC0EVT4
G0	12	ADC1EVT1
G0	13	ADC1EVT2
G0	14	ADC1EVT3
G0	15	ADC1EVT4
G0	16	ADC2EVT1
G0	17	ADC2EVT2
G0	18	ADC2EVT3
G0	19	ADC2EVT4
G0	20	INPUTXBAR1
G0	21	INPUTXBAR2
G0	22	INPUTXBAR3
G0	23	INPUTXBAR4
G0	24	INPUTXBAR5
G0	25	INPUTXBAR6
G0	26	INPUTXBAR7
G0	27	INPUTXBAR8
G0	28	INPUTXBAR9
G0	29	INPUTXBAR10
G0	30	INPUTXBAR11
G0	31	INPUTXBAR12
G1	0	INPUTXBAR13
G1	1	INPUTXBAR14
G1	2	INPUTXBAR15
G1	3	INPUTXBAR16
G1	4	ECAP0_OUT
G1	5	ECAP1_OUT
G1	6	ADCSOCA
G1	7	ADCSOCB
G1	8	EXTSYNCOUT
G1	9	MCAN0_INT0
G1	10	MCAN1_INT0
G1	11	Reserved (Tie Low)
G1	12	EQEP0_ERR
G1	13	EQEP1_ERR
G1	14	Reserved (Tie Low)
G1	15	CPU_HALTED
G1	16	ECAP2_OUT
G1	17	SDFLT1_COMPH
G1	18	SDFLT1_COMPL
G1	19	SDFLT1_COMPH_OR_COMPL
G1	20	SDFLT2_COMPH
G1	21	SDFLT2_COMPL
G1	22	SDFLT2_COMPH_OR_COMPL
G1	23	SDFLT3_COMPH

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Table 19-2. PWM X-BAR Mux Configuration Table (continued)

Group	Bit	Input Signal
G1	24	SDFLT3_COMPL
G1	25	SDFLT3_COMPH_OR_COMPL
G1	26	SDFLT4_COMPH
G1	27	SDFLT4_COMPL
G1	28	SDFLT4_COMPH_OR_COMPL
G1	29	FSIRXA_TRIG1
G1	30	ECAT_SYNC0
G1	31	ECAT_SYNC1

19.3 GPIO Output X-BAR

The GPIO Output X-BAR takes signals from inside the device and brings them out to a GPIO. The Output X-BAR contains eight outputs and each contains at least one position on the GPIO mux, denoted as OUTPUTXBARx. The X-BAR allows the selection of a single input or a logical-OR of many inputs.

Note

Refer to the device data sheet for the exact number of GPIO signals available for a given package.

19.3.1 GPIO Output XBAR Architecture

The GPIO Output X-BAR has eight outputs that are routed to the GPIO module. Figure 19-4represents the architecture of a single output, but this output is identical to the architecture of all of the other outputs.

First, determine the signals that can be passed to the GPIO by referencing the GPIO Output XBAR Mux Configuration Options. Each of these signals are enabled or disabled using the OUTPUTBARGxSEL registers before being passed through an OR gate. In contrast to the other XBAR modules, there are also features for output stretching, latching the output, and inverting the output either at the flag or final output stage. Figure 19-4 shows these features. The final output is only recognized on the GPIO if the proper OUTPUTx muxing options are selected using the IOMUX registers.

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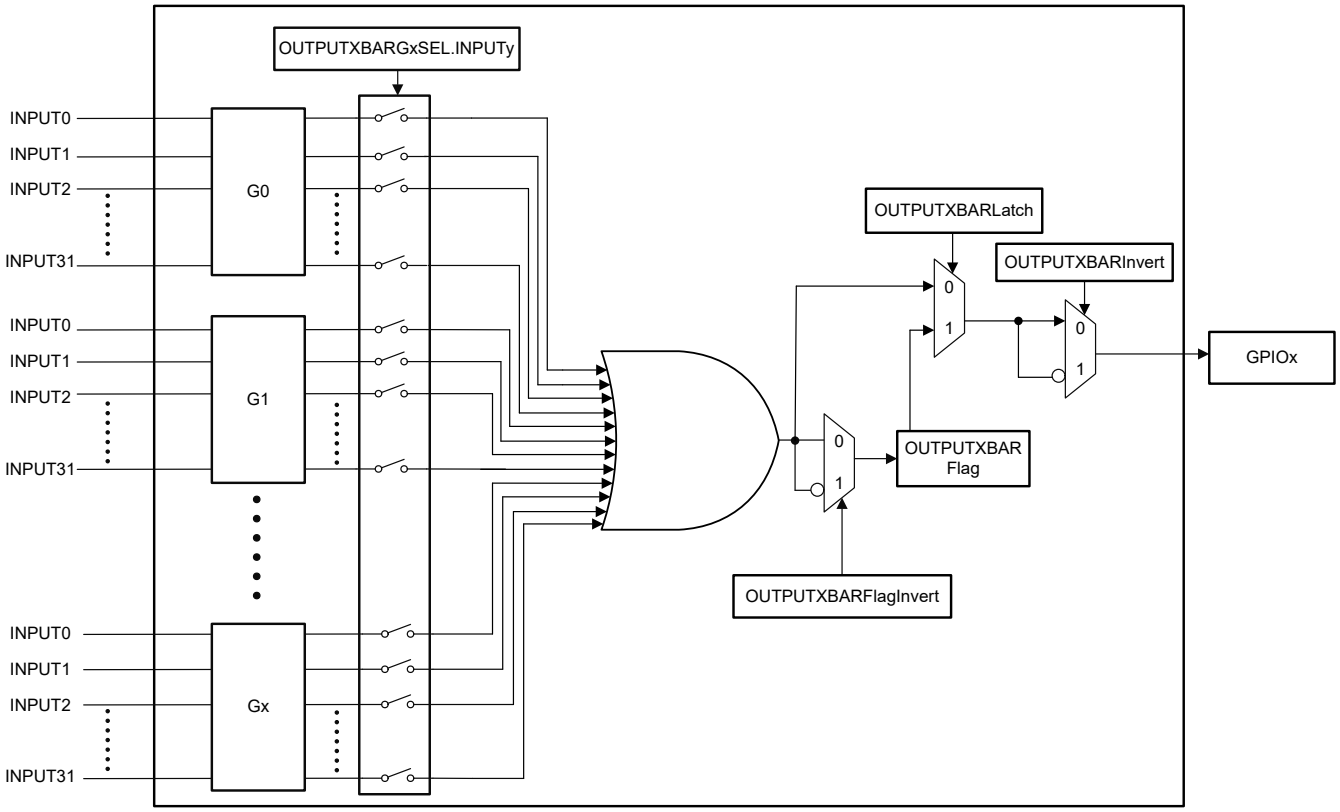


Figure 19-4. GPIO Output X-BAR Architecture

Table 19-3. Output X-BAR Mux Configuration Table

Group	Bit	Input Signal
G0	0	CMPSS0_CTRIPOUTH
G0	1	CMPSS0_CTRIPOUTL
G0	2	CMPSS1_CTRIPOUTH
G0	3	CMPSS1_CTRIPOUTL
G0	4	CMPSS2_CTRIPOUTH
G0	5	CMPSS2_CTRIPOUTL
G0	6	CMPSS3_CTRIPOUTH
G0	7	CMPSS3_CTRIPOUTL
G0	8	ADC0EVT1
G0	9	ADC0EVT2
G0	10	ADC0EVT3
G0	11	ADC0EVT4
G0	12	ADC1EVT1
G0	13	ADC1EVT2
G0	14	ADC1EVT3
G0	15	ADC1EVT4
G0	16	ADC2EVT1
G0	17	ADC2EVT2
G0	18	ADC2EVT3
G0	19	ADC2EVT4
G0	20	INPUTXBAR1

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Table 19-3. Output X-BAR Mux Configuration Table (continued)

Group	Bit	Input Signal
G0	21	INPUTXBAR2
G0	22	INPUTXBAR3
G0	23	INPUTXBAR4
G0	24	INPUTXBAR5
G0	25	INPUTXBAR6
G0	26	INPUTXBAR7
G0	27	INPUTXBAR8
G0	28	INPUTXBAR9
G0	29	INPUTXBAR10
G0	30	INPUTXBAR11
G0	31	INPUTXBAR12
G1	0	INPUTXBAR13
G1	1	INPUTXBAR14
G1	2	INPUTXBAR15
G1	3	INPUTXBAR16
G1	4	ECAP0_OUT
G1	5	ECAP1_OUT
G1	6	ADCSOCA
G1	7	ADCSOCB
G1	8	EXTSYNCOUT
G1	9	MCAN0_INT0
G1	10	MCAN1_INT0
G1	11	Reserved
G1	12	EQEP0_ERR
G1	13	EQEP1_ERR
G1	14	Reserved
G1	15	EQEP0_INDEX_SYNCOUT
G1	16	EQEP0_STROBE_SYNCOUT
G1	17	EQEP1_INDEX_SYNCOUT
G1	18	EQEP1_STROBE_SYNCOUT
G1	19	Reserved
G1	20	Reserved
G1	21	XCLKOUT
G1	22	ECAP2_OUT
G1	23	SDFLT1_COMPH
G1	24	SDFLT1_COMPL
G1	25	SDFLT1_COMPH_OR_COMPL
G1	26	SDFLT2_COMPH
G1	27	SDFLT2_COMPL
G1	28	SDFLT2_COMPH_OR_COMPL
G1	29	SDFLT3_COMPH
G1	30	SDFLT3_COMPL
G1	31	SDFLT3_COMPH_OR_COMPL
G2	0	SDFLT4_COMPH
G2	1	SDFLT4_COMPL

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Table 19-3. Output X-BAR Mux Configuration Table (continued)

Group	Bit	Input Signal
G2	2	SDFLT4_COMPH_OR_COMPL
G2	3	FSIRX_TRIG2
G2	4	ECAT_SYNC0
G2	5	ECAT_SYNC1

19.4 X-BAR Flags

The PWM X-BAR and the Output X-BAR have all of the same input signals. Due to this, all X-BAR modules leverage a single set of input flags to indicate which input signals have been triggered. This allows software to check the input flags when an event occurs. See Figure 19-5 for more information.

There is a bit allocated for each input signal in one of the XBARFLGx registers. The flag remains set until cleared through the appropriate XBARCLRx register. The XBARFLGx and XBARCLRx registers can be found in the INPUT_FLAG_XBAR_REGS register set.

Note

Not all input sources are routed to all X-BAR modules. Refer to the X-BAR specific configuration tables for exact connections.

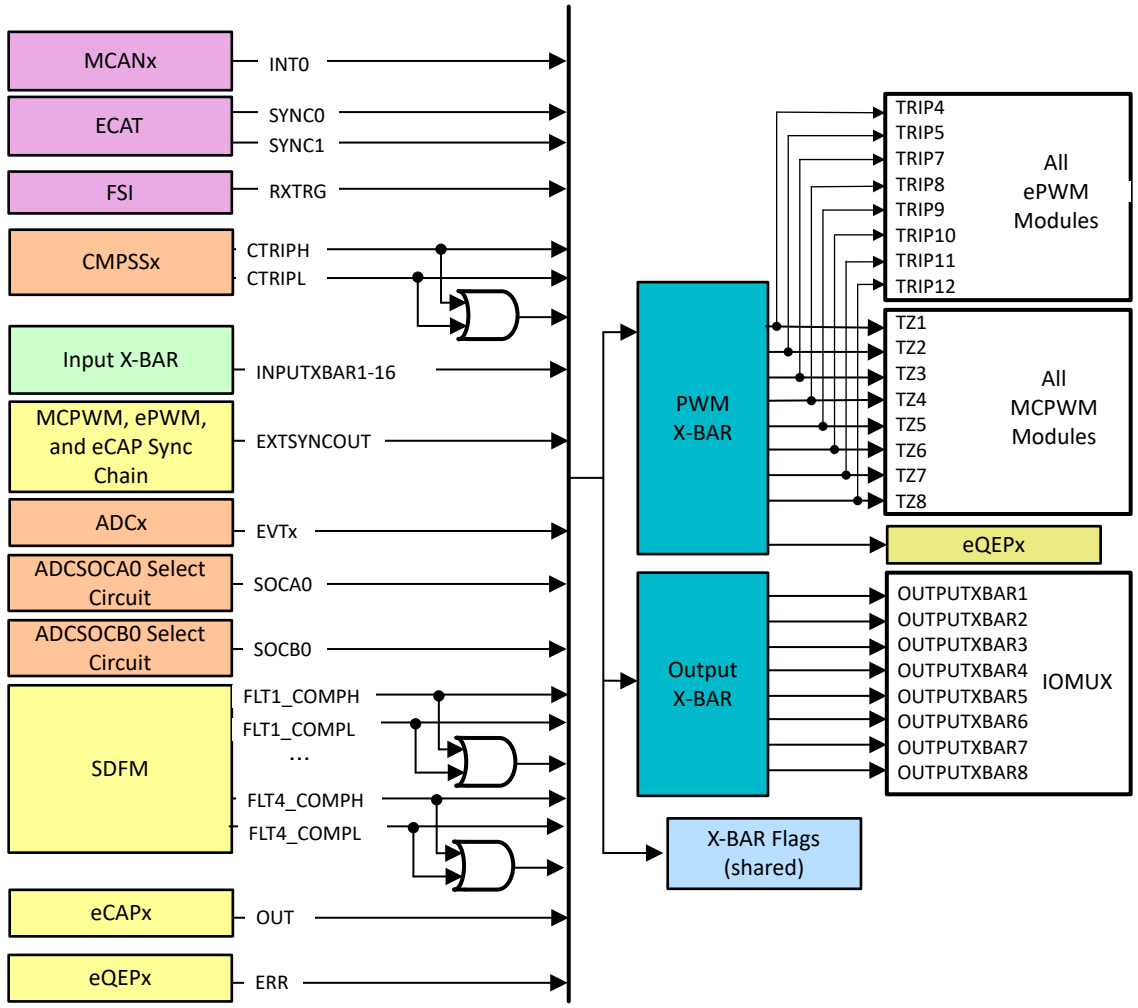


Figure 19-5. X-BAR Input Sources

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19.5 XBAR Interrupts & Triggers

19.5.1 ADC Sequencer Triggers

See the Section 20.3.3 section for more details about how to configure triggers for individual ADC sequencers.

Table 19-4. ADC Triggers from the TIMx

Trigger Name	Peripheral Instance Name	Register Group	XBAR ADC Trigger Configuration Registers	Description
INPUTXBAR5	INPUTXBAR	N/A	INPUTSELECT.SELECT	INPUTXBAR ADCEXTSOC ADC Sequencer trigger. Single configurable source condition.

19.6 XBAR Registers

This Section describes the XBAR Registers.

19.6.1 XBAR Base Address Table

Table 19-5. XBAR Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
InputXbarRegs	INPUT_XBAR_REGS	INPUTXBAR	0x4046_8000
PwmXbarRegs	PWM_XBAR_REGS	PWMXBAR	0x4046_9000
OutputXbarRegs	OUTPUTXBAR_REGS	OUTPUTXBAR	0x4046_A000
SyncRegs	SYNC_SOC_REGS	SYNC	0x4046_B000
Outputxbar0flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR0_FLAGS	0x4047_0000
Outputxbar1flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR1_FLAGS	0x4047_1000
Outputxbar2flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR2_FLAGS	0x4047_2000
Outputxbar3flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR3_FLAGS	0x4047_3000
Outputxbar4flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR4_FLAGS	0x4047_4000
Outputxbar5flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR5_FLAGS	0x4047_5000
Outputxbar6flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR6_FLAGS	0x4047_6000
Outputxbar7flagsRegs	OUTPUTXBAR_FLAG_REGS	OUTPUTXBAR7_FLAGS	0x4047_7000
InputxbarflagsRegs	INPUT_FLAG_XBAR_REGS	INPUTXBAR_FLAGS	0x4049_0000

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19.6.2 INPUT_XBAR_REGS Registers

Table 19-6 lists the memory-mapped registers for the INPUT_XBAR_REGS registers. All register offset addresses not listed in Table 19-6 should be considered as reserved locations and the register contents should not be modified.

Table 19-6. INPUT_XBAR_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	INPUTSELECT	Input Select Register (GPIO0 to x)		Go
400h	INPUTSELECTLOCK1	Input Select Lock Register 1		Go
410h	RAW_INPUTSELECT_PA	Raw Input Select Register for Port-A GPIOs		Go
414h	RAW_INPUTSELECT_PB	Raw Input Select Register for Port-B GPIOs		Go
418h	RAW_INPUTSELECT_PC	Raw Input Select Register for Port-C GPIOs		Go
41Ch	RAW_INPUTSELECT_PD	Raw Input Select Register for Port-D GPIOs		Go

Complex bit access types are encoded to fit into small table cells. Table 19-7 shows the codes that are used for access types in this section.

Table 19-7. INPUT_XBAR_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 INPUTSELECT Register (Offset = 0h) [Reset = 000000FEh]

INPUTSELECT is shown in Figure 19-6 and described in Table 19-8.

Return to the Summary Table.

Input Select Register (GPIO0 to x)

Figure 19-6. INPUTSELECT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SELECT							
R-0-0h																								R/W-FEh							

Table 19-9. INPUTSELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R-0	0h	Reserved
7-0	SELECT	R/W	FEh	Select GPIO for INPUT{#} signal: 0x0 : Select GPIO0 0x1 : Select GPIO1 0x2 : Select GPIO2 ... 0xFD: '1' will be driven to the destination 0xFE: '1' will be driven to the destination 0xFF: '0' will be driven to the destination NOTE: SELECT value greater than the available number of GPIO pins on a device (except 0xFF) will cause the destination to be driven '1'. Reset type: XRSn

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2 INPUTSELECTLOCK1 Register (Offset = 400h) [Reset = 00000000h]

INPUTSELECTLOCK1 is shown in Figure 19-7 and described in Table 19-9.

Return to the Summary Table.

Input Select Lock Register.
Any bit in this register, once set can only be cleared through SYSRSn. Write of 0 to any bit of this register has no effect. Reads to the registers which have LOCK protection are always allowed.

Figure 19-7. INPUTSELECTLOCK1 Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	RESERVED	INPUT28SELECT	INPUT27SELECT	INPUT26SELECT	INPUT25SELECT
R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h
23	22	21	20	19	18	17	16
INPUT24SELECT	INPUT23SELECT	INPUT22SELECT	INPUT21SELECT	INPUT20SELECT	INPUT19SELECT	INPUT18SELECT	INPUT17SELECT
R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h
15	14	13	12	11	10	9	8
INPUT16SELECT	INPUT15SELECT	INPUT14SELECT	INPUT13SELECT	INPUT12SELECT	INPUT11SELECT	INPUT10SELECT	INPUT9SELECT
R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h
7	6	5	4	3	2	1	0
INPUT8SELECT	INPUT7SELECT	INPUT6SELECT	INPUT5SELECT	INPUT4SELECT	INPUT3SELECT	INPUT2SELECT	INPUT1SELECT
R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h

Table 19-11. INPUTSELECTLOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/WSonce	0h	Reserved
30	RESERVED	R/WSonce	0h	Reserved
29	RESERVED	R/WSonce	0h	Reserved
28	RESERVED	R/WSonce	0h	Reserved
27	INPUT28SELECT	R/WSonce	0h	Lock bit for INPUT28SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
26	INPUT27SELECT	R/WSonce	0h	Lock bit for INPUT27SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
25	INPUT26SELECT	R/WSonce	0h	Lock bit for INPUT26SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
24	INPUT25SELECT	R/WSonce	0h	Lock bit for INPUT25SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn

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Table 19-11. INPUTSELECTLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INPUT24SELECT	R/WSonce	0h	Lock bit for INPUT24SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
22	INPUT23SELECT	R/WSonce	0h	Lock bit for INPUT23SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
21	INPUT22SELECT	R/WSonce	0h	Lock bit for INPUT22SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
20	INPUT21SELECT	R/WSonce	0h	Lock bit for INPUT21SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
19	INPUT20SELECT	R/WSonce	0h	Lock bit for INPUT20SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
18	INPUT19SELECT	R/WSonce	0h	Lock bit for INPUT19SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
17	INPUT18SELECT	R/WSonce	0h	Lock bit for INPUT18SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
16	INPUT17SELECT	R/WSonce	0h	Lock bit for INPUT17SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
15	INPUT16SELECT	R/WSonce	0h	Lock bit for INPUT16SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
14	INPUT15SELECT	R/WSonce	0h	Lock bit for INPUT15SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
13	INPUT14SELECT	R/WSonce	0h	Lock bit for INPUT14SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn

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Table 19-11. INPUTSELECTLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INPUT13SELECT	R/WSonce	0h	Lock bit for INPUT13SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
11	INPUT12SELECT	R/WSonce	0h	Lock bit for INPUT12SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
10	INPUT11SELECT	R/WSonce	0h	Lock bit for INPUT11SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
9	INPUT10SELECT	R/WSonce	0h	Lock bit for INPUT10SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
8	INPUT9SELECT	R/WSonce	0h	Lock bit for INPUT9SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
7	INPUT8SELECT	R/WSonce	0h	Lock bit for INPUT8SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
6	INPUT7SELECT	R/WSonce	0h	Lock bit for INPUT7SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
5	INPUT6SELECT	R/WSonce	0h	Lock bit for INPUT6SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
4	INPUT5SELECT	R/WSonce	0h	Lock bit for INPUT5SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
3	INPUT4SELECT	R/WSonce	0h	Lock bit for INPUT4SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
2	INPUT3SELECT	R/WSonce	0h	Lock bit for INPUT3SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn

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Table 19-11. INPUTSELECTLOCK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INPUT2SELECT	R/WSonce	0h	Lock bit for INPUT2SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn
0	INPUT1SELECT	R/WSonce	0h	Lock bit for INPUT1SELECT Register 0: Register is not locked 1: Register is locked Reset type: XRSn

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3 RAW_INPUTSELECT_PA Register (Offset = 410h) [Reset = 00000000h]

RAW_INPUTSELECT_PA is shown in Figure 19-8 and described in Table 19-10.

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Raw Input Select Register for Port-A GPIOs
This selection is common to all the INPUTXBARx output channels

Figure 19-8. RAW_INPUTSELECT_PA Register

31	30	29	28	27	26	25	24
SEL31	SEL30	SEL29	SEL28	SEL27	SEL26	SEL25	SEL24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SEL23	SEL22	SEL21	SEL20	SEL19	SEL18	SEL17	SEL16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
SEL15	SEL14	SEL13	SEL12	SEL11	SEL10	SEL9	SEL8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-13. RAW_INPUTSELECT_PA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL31	R/W	0h	Raw input select bit for PA31 0: Input signal from the PA31 pad processed through the GPIO module is selected 1: Raw input signal from the PA31 pad is selected Reset type: XRSn
30	SEL30	R/W	0h	Raw input select bit for PA30 0: Input signal from the PA30 pad processed through the GPIO module is selected 1: Raw input signal from the PA30 pad is selected Reset type: XRSn
29	SEL29	R/W	0h	Raw input select bit for PA29 0: Input signal from the PA29 pad processed through the GPIO module is selected 1: Raw input signal from the PA29 pad is selected Reset type: XRSn
28	SEL28	R/W	0h	Raw input select bit for PA28 0: Input signal from the PA28 pad processed through the GPIO module is selected 1: Raw input signal from the PA28 pad is selected Reset type: XRSn
27	SEL27	R/W	0h	Raw input select bit for PA27 0: Input signal from the PA27 pad processed through the GPIO module is selected 1: Raw input signal from the PA27 pad is selected Reset type: XRSn

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Table 19-13. RAW_INPUTSELECT_PA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	SEL26	R/W	0h	Raw input select bit for PA26 0: Input signal from the PA26 pad processed through the GPIO module is selected 1: Raw input signal from the PA26 pad is selected Reset type: XRSn
25	SEL25	R/W	0h	Raw input select bit for PA25 0: Input signal from the PA25 pad processed through the GPIO module is selected 1: Raw input signal from the PA25 pad is selected Reset type: XRSn
24	SEL24	R/W	0h	Raw input select bit for PA24 0: Input signal from the PA24 pad processed through the GPIO module is selected 1: Raw input signal from the PA24 pad is selected Reset type: XRSn
23	SEL23	R/W	0h	Raw input select bit for PA23 0: Input signal from the PA23 pad processed through the GPIO module is selected 1: Raw input signal from the PA23 pad is selected Reset type: XRSn
22	SEL22	R/W	0h	Raw input select bit for PA22 0: Input signal from the PA22 pad processed through the GPIO module is selected 1: Raw input signal from the PA22 pad is selected Reset type: XRSn
21	SEL21	R/W	0h	Raw input select bit for PA21 0: Input signal from the PA21 pad processed through the GPIO module is selected 1: Raw input signal from the PA21 pad is selected Reset type: XRSn
20	SEL20	R/W	0h	Raw input select bit for PA20 0: Input signal from the PA20 pad processed through the GPIO module is selected 1: Raw input signal from the PA20 pad is selected Reset type: XRSn
19	SEL19	R/W	0h	Raw input select bit for PA19 0: Input signal from the PA19 pad processed through the GPIO module is selected 1: Raw input signal from the PA19 pad is selected Reset type: XRSn
18	SEL18	R/W	0h	Raw input select bit for PA18 0: Input signal from the PA18 pad processed through the GPIO module is selected 1: Raw input signal from the PA18 pad is selected Reset type: XRSn
17	SEL17	R/W	0h	Raw input select bit for PA17 0: Input signal from the PA17 pad processed through the GPIO module is selected 1: Raw input signal from the PA17 pad is selected Reset type: XRSn

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Table 19-13. RAW_INPUTSELECT_PA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SEL16	R/W	0h	Raw input select bit for PA16 0: Input signal from the PA16 pad processed through the GPIO module is selected 1: Raw input signal from the PA16 pad is selected Reset type: XRSn
15	SEL15	R/W	0h	Raw input select bit for PA15 0: Input signal from the PA15 pad processed through the GPIO module is selected 1: Raw input signal from the PA15 pad is selected Reset type: XRSn
14	SEL14	R/W	0h	Raw input select bit for PA14 0: Input signal from the PA14 pad processed through the GPIO module is selected 1: Raw input signal from the PA14 pad is selected Reset type: XRSn
13	SEL13	R/W	0h	Raw input select bit for PA13 0: Input signal from the PA13 pad processed through the GPIO module is selected 1: Raw input signal from the PA13 pad is selected Reset type: XRSn
12	SEL12	R/W	0h	Raw input select bit for PA12 0: Input signal from the PA12 pad processed through the GPIO module is selected 1: Raw input signal from the PA12 pad is selected Reset type: XRSn
11	SEL11	R/W	0h	Raw input select bit for PA11 0: Input signal from the PA11 pad processed through the GPIO module is selected 1: Raw input signal from the PA11 pad is selected Reset type: XRSn
10	SEL10	R/W	0h	Raw input select bit for PA10 0: Input signal from the PA10 pad processed through the GPIO module is selected 1: Raw input signal from the PA10 pad is selected Reset type: XRSn
9	SEL9	R/W	0h	Raw input select bit for PA9 0: Input signal from the PA9 pad processed through the GPIO module is selected 1: Raw input signal from the PA9 pad is selected Reset type: XRSn
8	SEL8	R/W	0h	Raw input select bit for PA8 0: Input signal from the PA8 pad processed through the GPIO module is selected 1: Raw input signal from the PA8 pad is selected Reset type: XRSn
7	SEL7	R/W	0h	Raw input select bit for PA7 0: Input signal from the PA7 pad processed through the GPIO module is selected 1: Raw input signal from the PA7 pad is selected Reset type: XRSn

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Table 19-13. RAW_INPUTSELECT_PA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SEL6	R/W	0h	Raw input select bit for PA6 0: Input signal from the PA6 pad processed through the GPIO module is selected 1: Raw input signal from the PA6 pad is selected Reset type: XRSn
5	SEL5	R/W	0h	Raw input select bit for PA5 0: Input signal from the PA5 pad processed through the GPIO module is selected 1: Raw input signal from the PA5 pad is selected Reset type: XRSn
4	SEL4	R/W	0h	Raw input select bit for PA4 0: Input signal from the PA4 pad processed through the GPIO module is selected 1: Raw input signal from the PA4 pad is selected Reset type: XRSn
3	SEL3	R/W	0h	Raw input select bit for PA3 0: Input signal from the PA3 pad processed through the GPIO module is selected 1: Raw input signal from the PA3 pad is selected Reset type: XRSn
2	SEL2	R/W	0h	Raw input select bit for PA2 0: Input signal from the PA2 pad processed through the GPIO module is selected 1: Raw input signal from the PA2 pad is selected Reset type: XRSn
1	SEL1	R/W	0h	Raw input select bit for PA1 0: Input signal from the PA1 pad processed through the GPIO module is selected 1: Raw input signal from the PA1 pad is selected Reset type: XRSn
0	SEL0	R/W	0h	Raw input select bit for PA0 0: Input signal from the PA0 pad processed through the GPIO module is selected 1: Raw input signal from the PA0 pad is selected Reset type: XRSn

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4 RAW_INPUTSELECT_PB Register (Offset = 414h) [Reset = 00000000h]

RAW_INPUTSELECT_PB is shown in Figure 19-9 and described in Table 19-11.

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Raw Input Select Register for Port-B GPIOs
This selection is common to all the INPUTXBARx output channels

Figure 19-9. RAW_INPUTSELECT_PB Register

31	30	29	28	27	26	25	24
SEL31	SEL30	SEL29	SEL28	SEL27	SEL26	SEL25	SEL24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SEL23	SEL22	SEL21	SEL20	SEL19	SEL18	SEL17	SEL16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
SEL15	SEL14	SEL13	SEL12	SEL11	SEL10	SEL9	SEL8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-15. RAW_INPUTSELECT_PB Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL31	R/W	0h	Raw input select bit for PB31 0: Input signal from the PB31 pad processed through the GPIO module is selected 1: Raw input signal from the PB31 pad is selected Reset type: XRSn
30	SEL30	R/W	0h	Raw input select bit for PB30 0: Input signal from the PB30 pad processed through the GPIO module is selected 1: Raw input signal from the PB30 pad is selected Reset type: XRSn
29	SEL29	R/W	0h	Raw input select bit for PB29 0: Input signal from the PB29 pad processed through the GPIO module is selected 1: Raw input signal from the PB29 pad is selected Reset type: XRSn
28	SEL28	R/W	0h	Raw input select bit for PB28 0: Input signal from the PB28 pad processed through the GPIO module is selected 1: Raw input signal from the PB28 pad is selected Reset type: XRSn
27	SEL27	R/W	0h	Raw input select bit for PB27 0: Input signal from the PB27 pad processed through the GPIO module is selected 1: Raw input signal from the PB27 pad is selected Reset type: XRSn

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Table 19-15. RAW_INPUTSELECT_PB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	SEL26	R/W	0h	Raw input select bit for PB26 0: Input signal from the PB26 pad processed through the GPIO module is selected 1: Raw input signal from the PB26 pad is selected Reset type: XRSn
25	SEL25	R/W	0h	Raw input select bit for PB25 0: Input signal from the PB25 pad processed through the GPIO module is selected 1: Raw input signal from the PB25 pad is selected Reset type: XRSn
24	SEL24	R/W	0h	Raw input select bit for PB24 0: Input signal from the PB24 pad processed through the GPIO module is selected 1: Raw input signal from the PB24 pad is selected Reset type: XRSn
23	SEL23	R/W	0h	Raw input select bit for PB23 0: Input signal from the PB23 pad processed through the GPIO module is selected 1: Raw input signal from the PB23 pad is selected Reset type: XRSn
22	SEL22	R/W	0h	Raw input select bit for PB22 0: Input signal from the PB22 pad processed through the GPIO module is selected 1: Raw input signal from the PB22 pad is selected Reset type: XRSn
21	SEL21	R/W	0h	Raw input select bit for PB21 0: Input signal from the PB21 pad processed through the GPIO module is selected 1: Raw input signal from the PB21 pad is selected Reset type: XRSn
20	SEL20	R/W	0h	Raw input select bit for PB20 0: Input signal from the PB20 pad processed through the GPIO module is selected 1: Raw input signal from the PB20 pad is selected Reset type: XRSn
19	SEL19	R/W	0h	Raw input select bit for PB19 0: Input signal from the PB19 pad processed through the GPIO module is selected 1: Raw input signal from the PB19 pad is selected Reset type: XRSn
18	SEL18	R/W	0h	Raw input select bit for PB18 0: Input signal from the PB18 pad processed through the GPIO module is selected 1: Raw input signal from the PB18 pad is selected Reset type: XRSn
17	SEL17	R/W	0h	Raw input select bit for PB17 0: Input signal from the PB17 pad processed through the GPIO module is selected 1: Raw input signal from the PB17 pad is selected Reset type: XRSn

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Table 19-15. RAW_INPUTSELECT_PB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SEL16	R/W	0h	Raw input select bit for PB16 0: Input signal from the PB16 pad processed through the GPIO module is selected 1: Raw input signal from the PB16 pad is selected Reset type: XRSn
15	SEL15	R/W	0h	Raw input select bit for PB15 0: Input signal from the PB15 pad processed through the GPIO module is selected 1: Raw input signal from the PB15 pad is selected Reset type: XRSn
14	SEL14	R/W	0h	Raw input select bit for PB14 0: Input signal from the PB14 pad processed through the GPIO module is selected 1: Raw input signal from the PB14 pad is selected Reset type: XRSn
13	SEL13	R/W	0h	Raw input select bit for PB13 0: Input signal from the PB13 pad processed through the GPIO module is selected 1: Raw input signal from the PB13 pad is selected Reset type: XRSn
12	SEL12	R/W	0h	Raw input select bit for PB12 0: Input signal from the PB12 pad processed through the GPIO module is selected 1: Raw input signal from the PB12 pad is selected Reset type: XRSn
11	SEL11	R/W	0h	Raw input select bit for PB11 0: Input signal from the PB11 pad processed through the GPIO module is selected 1: Raw input signal from the PB11 pad is selected Reset type: XRSn
10	SEL10	R/W	0h	Raw input select bit for PB10 0: Input signal from the PB10 pad processed through the GPIO module is selected 1: Raw input signal from the PB10 pad is selected Reset type: XRSn
9	SEL9	R/W	0h	Raw input select bit for PB9 0: Input signal from the PB9 pad processed through the GPIO module is selected 1: Raw input signal from the PB9 pad is selected Reset type: XRSn
8	SEL8	R/W	0h	Raw input select bit for PB8 0: Input signal from the PB8 pad processed through the GPIO module is selected 1: Raw input signal from the PB8 pad is selected Reset type: XRSn
7	SEL7	R/W	0h	Raw input select bit for PB7 0: Input signal from the PB7 pad processed through the GPIO module is selected 1: Raw input signal from the PB7 pad is selected Reset type: XRSn

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Table 19-15. RAW_INPUTSELECT_PB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SEL6	R/W	0h	Raw input select bit for PB6 0: Input signal from the PB6 pad processed through the GPIO module is selected 1: Raw input signal from the PB6 pad is selected Reset type: XRSn
5	SEL5	R/W	0h	Raw input select bit for PB5 0: Input signal from the PB5 pad processed through the GPIO module is selected 1: Raw input signal from the PB5 pad is selected Reset type: XRSn
4	SEL4	R/W	0h	Raw input select bit for PB4 0: Input signal from the PB4 pad processed through the GPIO module is selected 1: Raw input signal from the PB4 pad is selected Reset type: XRSn
3	SEL3	R/W	0h	Raw input select bit for PB3 0: Input signal from the PB3 pad processed through the GPIO module is selected 1: Raw input signal from the PB3 pad is selected Reset type: XRSn
2	SEL2	R/W	0h	Raw input select bit for PB2 0: Input signal from the PB2 pad processed through the GPIO module is selected 1: Raw input signal from the PB2 pad is selected Reset type: XRSn
1	SEL1	R/W	0h	Raw input select bit for PB1 0: Input signal from the PB1 pad processed through the GPIO module is selected 1: Raw input signal from the PB1 pad is selected Reset type: XRSn
0	SEL0	R/W	0h	Raw input select bit for PB0 0: Input signal from the PB0 pad processed through the GPIO module is selected 1: Raw input signal from the PB0 pad is selected Reset type: XRSn

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5 RAW_INPUTSELECT_PC Register (Offset = 418h) [Reset = 00000000h]

RAW_INPUTSELECT_PC is shown in Figure 19-10 and described in Table 19-12.

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Raw Input Select Register for Port-C GPIOs
This selection is common to all the INPUTXBARx output channels

Figure 19-10. RAW_INPUTSELECT_PC Register

31	30	29	28	27	26	25	24
SEL31	SEL30	SEL29	SEL28	SEL27	SEL26	SEL25	SEL24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SEL23	SEL22	SEL21	SEL20	SEL19	SEL18	SEL17	SEL16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
SEL15	SEL14	SEL13	SEL12	SEL11	SEL10	SEL9	SEL8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-17. RAW_INPUTSELECT_PC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEL31	R/W	0h	Raw input select bit for PC31 0: Input signal from the PC31 pad processed through the GPIO module is selected 1: Raw input signal from the PC31 pad is selected Reset type: XRSn
30	SEL30	R/W	0h	Raw input select bit for PC30 0: Input signal from the PC30 pad processed through the GPIO module is selected 1: Raw input signal from the PC30 pad is selected Reset type: XRSn
29	SEL29	R/W	0h	Raw input select bit for PC29 0: Input signal from the PC29 pad processed through the GPIO module is selected 1: Raw input signal from the PC29 pad is selected Reset type: XRSn
28	SEL28	R/W	0h	Raw input select bit for PC28 0: Input signal from the PC28 pad processed through the GPIO module is selected 1: Raw input signal from the PC28 pad is selected Reset type: XRSn
27	SEL27	R/W	0h	Raw input select bit for PC27 0: Input signal from the PC27 pad processed through the GPIO module is selected 1: Raw input signal from the PC27 pad is selected Reset type: XRSn

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Table 19-17. RAW_INPUTSELECT_PC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	SEL26	R/W	0h	Raw input select bit for PC26 0: Input signal from the PC26 pad processed through the GPIO module is selected 1: Raw input signal from the PC26 pad is selected Reset type: XRSn
25	SEL25	R/W	0h	Raw input select bit for PC25 0: Input signal from the PC25 pad processed through the GPIO module is selected 1: Raw input signal from the PC25 pad is selected Reset type: XRSn
24	SEL24	R/W	0h	Raw input select bit for PC24 0: Input signal from the PC24 pad processed through the GPIO module is selected 1: Raw input signal from the PC24 pad is selected Reset type: XRSn
23	SEL23	R/W	0h	Raw input select bit for PC23 0: Input signal from the PC23 pad processed through the GPIO module is selected 1: Raw input signal from the PC23 pad is selected Reset type: XRSn
22	SEL22	R/W	0h	Raw input select bit for PC22 0: Input signal from the PC22 pad processed through the GPIO module is selected 1: Raw input signal from the PC22 pad is selected Reset type: XRSn
21	SEL21	R/W	0h	Raw input select bit for PC21 0: Input signal from the PC21 pad processed through the GPIO module is selected 1: Raw input signal from the PC21 pad is selected Reset type: XRSn
20	SEL20	R/W	0h	Raw input select bit for PC20 0: Input signal from the PC20 pad processed through the GPIO module is selected 1: Raw input signal from the PC20 pad is selected Reset type: XRSn
19	SEL19	R/W	0h	Raw input select bit for PC19 0: Input signal from the PC19 pad processed through the GPIO module is selected 1: Raw input signal from the PC19 pad is selected Reset type: XRSn
18	SEL18	R/W	0h	Raw input select bit for PC18 0: Input signal from the PC18 pad processed through the GPIO module is selected 1: Raw input signal from the PC18 pad is selected Reset type: XRSn
17	SEL17	R/W	0h	Raw input select bit for PC17 0: Input signal from the PC17 pad processed through the GPIO module is selected 1: Raw input signal from the PC17 pad is selected Reset type: XRSn

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Table 19-17. RAW_INPUTSELECT_PC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SEL16	R/W	0h	Raw input select bit for PC16 0: Input signal from the PC16 pad processed through the GPIO module is selected 1: Raw input signal from the PC16 pad is selected Reset type: XRSn
15	SEL15	R/W	0h	Raw input select bit for PC15 0: Input signal from the PC15 pad processed through the GPIO module is selected 1: Raw input signal from the PC15 pad is selected Reset type: XRSn
14	SEL14	R/W	0h	Raw input select bit for PC14 0: Input signal from the PC14 pad processed through the GPIO module is selected 1: Raw input signal from the PC14 pad is selected Reset type: XRSn
13	SEL13	R/W	0h	Raw input select bit for PC13 0: Input signal from the PC13 pad processed through the GPIO module is selected 1: Raw input signal from the PC13 pad is selected Reset type: XRSn
12	SEL12	R/W	0h	Raw input select bit for PC12 0: Input signal from the PC12 pad processed through the GPIO module is selected 1: Raw input signal from the PC12 pad is selected Reset type: XRSn
11	SEL11	R/W	0h	Raw input select bit for PC11 0: Input signal from the PC11 pad processed through the GPIO module is selected 1: Raw input signal from the PC11 pad is selected Reset type: XRSn
10	SEL10	R/W	0h	Raw input select bit for PC10 0: Input signal from the PC10 pad processed through the GPIO module is selected 1: Raw input signal from the PC10 pad is selected Reset type: XRSn
9	SEL9	R/W	0h	Raw input select bit for PC9 0: Input signal from the PC9 pad processed through the GPIO module is selected 1: Raw input signal from the PC9 pad is selected Reset type: XRSn
8	SEL8	R/W	0h	Raw input select bit for PC8 0: Input signal from the PC8 pad processed through the GPIO module is selected 1: Raw input signal from the PC8 pad is selected Reset type: XRSn
7	SEL7	R/W	0h	Raw input select bit for PC7 0: Input signal from the PC7 pad processed through the GPIO module is selected 1: Raw input signal from the PC7 pad is selected Reset type: XRSn

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Table 19-17. RAW_INPUTSELECT_PC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SEL6	R/W	0h	Raw input select bit for PC6 0: Input signal from the PC6 pad processed through the GPIO module is selected 1: Raw input signal from the PC6 pad is selected Reset type: XRSn
5	SEL5	R/W	0h	Raw input select bit for PC5 0: Input signal from the PC5 pad processed through the GPIO module is selected 1: Raw input signal from the PC5 pad is selected Reset type: XRSn
4	SEL4	R/W	0h	Raw input select bit for PC4 0: Input signal from the PC4 pad processed through the GPIO module is selected 1: Raw input signal from the PC4 pad is selected Reset type: XRSn
3	SEL3	R/W	0h	Raw input select bit for PC3 0: Input signal from the PC3 pad processed through the GPIO module is selected 1: Raw input signal from the PC3 pad is selected Reset type: XRSn
2	SEL2	R/W	0h	Raw input select bit for PC2 0: Input signal from the PC2 pad processed through the GPIO module is selected 1: Raw input signal from the PC2 pad is selected Reset type: XRSn
1	SEL1	R/W	0h	Raw input select bit for PC1 0: Input signal from the PC1 pad processed through the GPIO module is selected 1: Raw input signal from the PC1 pad is selected Reset type: XRSn
0	SEL0	R/W	0h	Raw input select bit for PC0 0: Input signal from the PC0 pad processed through the GPIO module is selected 1: Raw input signal from the PC0 pad is selected Reset type: XRSn

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6 RAW_INPUTSELECT_PD Register (Offset = 41Ch) [Reset = 00000000h]

RAW_INPUTSELECT_PD is shown in Figure 19-11 and described in Table 19-13.

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Raw Input Select Register for Port-D GPIOs
This selection is common to all the INPUTXBARx output channels

Figure 19-11. RAW_INPUTSELECT_PD Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	SEL11	RESERVED	SEL9	SEL8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-19. RAW_INPUTSELECT_PD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	RESERVED	R/W	0h	Reserved
29	RESERVED	R/W	0h	Reserved
28	RESERVED	R/W	0h	Reserved
27	RESERVED	R/W	0h	Reserved
26	RESERVED	R/W	0h	Reserved
25	RESERVED	R/W	0h	Reserved
24	RESERVED	R/W	0h	Reserved
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	0h	Reserved
20	RESERVED	R/W	0h	Reserved
19	RESERVED	R/W	0h	Reserved
18	RESERVED	R/W	0h	Reserved
17	RESERVED	R/W	0h	Reserved
16	RESERVED	R/W	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	SEL11	R/W	0h	Raw input select bit for PD11 0: Input signal from the PD11 pad processed through the GPIO module is selected 1: Raw input signal from the PD11 pad is selected Reset type: XRSn

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Table 19-19. RAW_INPUTSELECT_PD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED	R/W	0h	Reserved
9	SEL9	R/W	0h	Raw input select bit for PD9 0: Input signal from the PD9 pad processed through the GPIO module is selected 1: Raw input signal from the PD9 pad is selected Reset type: XRSn
8	SEL8	R/W	0h	Raw input select bit for PD8 0: Input signal from the PD8 pad processed through the GPIO module is selected 1: Raw input signal from the PD8 pad is selected Reset type: XRSn
7	SEL7	R/W	0h	Raw input select bit for PD7 0: Input signal from the PD7 pad processed through the GPIO module is selected 1: Raw input signal from the PD7 pad is selected Reset type: XRSn
6	SEL6	R/W	0h	Raw input select bit for PD6 0: Input signal from the PD6 pad processed through the GPIO module is selected 1: Raw input signal from the PD6 pad is selected Reset type: XRSn
5	SEL5	R/W	0h	Raw input select bit for PD5 0: Input signal from the PD5 pad processed through the GPIO module is selected 1: Raw input signal from the PD5 pad is selected Reset type: XRSn
4	SEL4	R/W	0h	Raw input select bit for PD4 0: Input signal from the PD4 pad processed through the GPIO module is selected 1: Raw input signal from the PD4 pad is selected Reset type: XRSn
3	SEL3	R/W	0h	Raw input select bit for PD3 0: Input signal from the PD3 pad processed through the GPIO module is selected 1: Raw input signal from the PD3 pad is selected Reset type: XRSn
2	SEL2	R/W	0h	Raw input select bit for PD2 0: Input signal from the PD2 pad processed through the GPIO module is selected 1: Raw input signal from the PD2 pad is selected Reset type: XRSn
1	SEL1	R/W	0h	Raw input select bit for PD1 0: Input signal from the PD1 pad processed through the GPIO module is selected 1: Raw input signal from the PD1 pad is selected Reset type: XRSn

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Table 19-19. RAW_INPUTSELECT_PD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SEL0	R/W	0h	Raw input select bit for PD0 0: Input signal from the PD0 pad processed through the GPIO module is selected 1: Raw input signal from the PD0 pad is selected Reset type: XRSn

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19.6.3 PWM_XBAR_REGS Registers

Table 19-14 lists the memory-mapped registers for the PWM_XBAR_REGS registers. All register offset addresses not listed in Table 19-14 should be considered as reserved locations and the register contents should not be modified.

Table 19-20. PWM_XBAR_REGS Registers

Offset	Acronym	Register Name	Group	Section
30h	PWMXBAROutInvert	Output Signal Invert Select		Go
80h	PWMXBARLock	Configuration Lock register		Go
100h + formula	PWMXBARG0SEL_j	PWMXBAR G0 Input Select		Go
104h + formula	PWMXBARG1SEL_j	PWMXBAR G1 Input Select		Go

Complex bit access types are encoded to fit into small table cells. Table 19-15 shows the codes that are used for access types in this section.

Table 19-21. PWM_XBAR_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PWMXBAROutInvert Register (Offset = 30h) [Reset = 00000000h]

PWMXBAROutInvert is shown in Figure 19-12 and described in Table 19-16.

Return to the Summary Table.

Output Signal Invert Select

Figure 19-12. PWMXBAROutInvert Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XBAR8	XBAR7	XBAR6	XBAR5	XBAR4	XBAR3	XBAR2	XBAR1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-23. PWMXBAROutInvert Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	XBAR8	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
6	XBAR7	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
5	XBAR6	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
4	XBAR5	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn

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Table 19-23. PWMXBAROutInvert Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	XBAR4	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
2	XBAR3	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
1	XBAR2	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
0	XBAR1	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn

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2 PWMXBARLock Register (Offset = 80h) [Reset = 00000000h]

PWMXBARLock is shown in Figure 19-13 and described in Table 19-17.

Return to the Summary Table.

Configuration Lock register

Figure 19-13. PWMXBARLock Register

31	30	29	28	27	26	25	24
KEY							
R-0/W-0h							
23	22	21	20	19	18	17	16
KEY							
R-0/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0-0h							R/WSonce-0h

Table 19-25. PWMXBARLock Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R-0/W	0h	Bit-0 of this register can be set only if KEY= 0x5a5a Reset type: XRSn
15-1	RESERVED	R-0	0h	Reserved
0	LOCK	R/WSonce	0h	Locks the configuration for EPWM-XBAR. Once the configuration is locked, writes to the below registers for EPWM-XBAR is blocked. Registers Affected by the LOCK mechanism: PWMXBAR Gx SEL PWMXBAR.Invert 0: Writes to the above registers are allowed 1: Writes to the above registers are blocked Note: [1] LOCK mechanism only apples to writes. Reads are never blocked. Reset type: XRSn

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3 PWMXBARG0SEL_j Register (Offset = 100h + formula) [Reset = 00000000h]

PWMXBARG0SEL_j is shown in Figure 19-14 and described in Table 19-18.

Return to the Summary Table.

PWMXBAR G0 Input Select

Offset = 100h + (j * 40h); where j = 0h to 7h

Figure 19-14. PWMXBARG0SEL_j Register

31	30	29	28	27	26	25	24
INPUT31	INPUT30	INPUT29	INPUT28	INPUT27	INPUT26	INPUT25	INPUT24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INPUT23	INPUT22	INPUT21	INPUT20	INPUT19	INPUT18	INPUT17	INPUT16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INPUT15	INPUT14	INPUT13	INPUT12	INPUT11	INPUT10	INPUT9	INPUT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INPUT7	INPUT6	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1	INPUT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-27. PWMXBARG0SEL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT31	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
30	INPUT30	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
29	INPUT29	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
28	INPUT28	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
27	INPUT27	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
26	INPUT26	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-27. PWMXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INPUT25	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
24	INPUT24	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
23	INPUT23	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
22	INPUT22	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
21	INPUT21	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
20	INPUT20	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
19	INPUT19	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
18	INPUT18	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
17	INPUT17	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
16	INPUT16	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
15	INPUT15	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-27. PWMXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INPUT14	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
13	INPUT13	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
12	INPUT12	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
11	INPUT11	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
10	INPUT10	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
9	INPUT9	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
8	INPUT8	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
7	INPUT7	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
6	INPUT6	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
5	INPUT5	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
4	INPUT4	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-27. PWMXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INPUT3	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
2	INPUT2	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
1	INPUT1	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
0	INPUT0	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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4 PWMXBARG1SEL_j Register (Offset = 104h + formula) [Reset = 00000000h]

PWMXBARG1SEL_j is shown in Figure 19-15 and described in Table 19-19.

Return to the Summary Table.

PWMXBAR G1 Input Select

Offset = 104h + (j * 40h); where j = 0h to 7h

Figure 19-15. PWMXBARG1SEL_j Register

31	30	29	28	27	26	25	24
INPUT31	INPUT30	INPUT29	INPUT28	INPUT27	INPUT26	INPUT25	INPUT24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INPUT23	INPUT22	INPUT21	INPUT20	INPUT19	INPUT18	INPUT17	INPUT16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INPUT15	INPUT14	INPUT13	INPUT12	INPUT11	INPUT10	INPUT9	INPUT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INPUT7	INPUT6	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1	INPUT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-29. PWMXBARG1SEL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT31	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
30	INPUT30	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
29	INPUT29	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
28	INPUT28	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
27	INPUT27	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
26	INPUT26	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-29. PWMXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INPUT25	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
24	INPUT24	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
23	INPUT23	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
22	INPUT22	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
21	INPUT21	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
20	INPUT20	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
19	INPUT19	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
18	INPUT18	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
17	INPUT17	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
16	INPUT16	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
15	INPUT15	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-29. PWMXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INPUT14	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
13	INPUT13	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
12	INPUT12	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
11	INPUT11	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
10	INPUT10	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
9	INPUT9	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
8	INPUT8	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
7	INPUT7	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
6	INPUT6	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
5	INPUT5	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
4	INPUT4	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-29. PWMXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INPUT3	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
2	INPUT2	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
1	INPUT1	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
0	INPUT0	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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19.6.4 OUTPUTXBAR_REGS Registers

Table 19-20 lists the memory-mapped registers for the OUTPUTXBAR_REGS registers. All register offset addresses not listed in Table 19-20 should be considered as reserved locations and the register contents should not be modified.

Table 19-30. OUTPUTXBAR_REGS Registers

Offset	Acronym	Register Name	Group	Section
14h	OUTPUTXBARFlagInvert	Output Signal inversion register		Go
24h	OUTPUTXBAROutLatch	Output Signal Select Latch		Go
30h	OUTPUTXBAROutInvert	Output Signal Invert Select		Go
80h	OUTPUTXBARLock	Configuration Lock register		Go
100h + formula	OUTPUTXBARG0SEL_j	OUTPUTXBAR G0 Input Select		Go
104h + formula	OUTPUTXBARG1SEL_j	OUTPUTXBAR G1 Input Select		Go

Complex bit access types are encoded to fit into small table cells. Table 19-21 shows the codes that are used for access types in this section.

Table 19-31. OUTPUTXBAR_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 OUTPUTXBARFlagInvert Register (Offset = 14h) [Reset = 00000000h]

OUTPUTXBARFlagInvert is shown in Figure 19-16 and described in Table 19-22.

Return to the Summary Table.

Output Signal inversion register

Figure 19-16. OUTPUTXBARFlagInvert Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XBAR8	XBAR7	XBAR6	XBAR5	XBAR4	XBAR3	XBAR2	XBAR1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-33. OUTPUTXBARFlagInvert Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	XBAR8	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
6	XBAR7	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
5	XBAR6	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
4	XBAR5	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn

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Table 19-33. OUTPUTXBARFlagInvert Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	XBAR4	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
2	XBAR3	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
1	XBAR2	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn
0	XBAR1	R/W	0h	Output Signal Invert Before Latch: 0 Signal Is Not Inverted 1 Signal Is Inverted Reset type: XRSn

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2 OUTPUTXBAROutLatch Register (Offset = 24h) [Reset = 00000000h]

OUTPUTXBAROutLatch is shown in Figure 19-17 and described in Table 19-23.

Return to the Summary Table.

Output Signal Select Latch

Figure 19-17. OUTPUTXBAROutLatch Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XBAR8	XBAR7	XBAR6	XBAR5	XBAR4	XBAR3	XBAR2	XBAR1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-35. OUTPUTXBAROutLatch Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	XBAR8	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
6	XBAR7	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
5	XBAR6	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
4	XBAR5	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn

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Table 19-35. OUTPUTXBAROutLatch Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	XBAR4	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
2	XBAR3	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
1	XBAR2	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn
0	XBAR1	R/W	0h	Output Signal Select Latch: 0 Latch Event Not Selected As Output 1 Latched Event Selected As Output Reset type: XRSn

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3 OUTPUTXBAROutInvert Register (Offset = 30h) [Reset = 00000000h]

OUTPUTXBAROutInvert is shown in Figure 19-18 and described in Table 19-24.

Return to the Summary Table.

Output Signal Invert Select

Figure 19-18. OUTPUTXBAROutInvert Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XBAR8	XBAR7	XBAR6	XBAR5	XBAR4	XBAR3	XBAR2	XBAR1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-37. OUTPUTXBAROutInvert Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	XBAR8	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
6	XBAR7	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
5	XBAR6	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
4	XBAR5	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn

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Table 19-37. OUTPUTXBAROutInvert Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	XBAR4	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
2	XBAR3	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
1	XBAR2	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn
0	XBAR1	R/W	0h	Select Output: 0 No inversion 1 Output inverted Reset type: XRSn

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4 OUTPUTXBARLock Register (Offset = 80h) [Reset = 00000000h]

OUTPUTXBARLock is shown in Figure 19-19 and described in Table 19-25.

Return to the Summary Table.

Configuration Lock register

Figure 19-19. OUTPUTXBARLock Register

31	30	29	28	27	26	25	24
KEY							
R-0/W-0h							
23	22	21	20	19	18	17	16
KEY							
R-0/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0-0h							R/WSonce-0h

Table 19-39. OUTPUTXBARLock Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R-0/W	0h	Bit-0 of this register can be set only if KEY= 0x5a5a Reset type: XRSn
15-1	RESERVED	R-0	0h	Reserved
0	LOCK	R/WSonce	0h	Locks the configuration for EOUTPUT-XBAR. Once the configuration is locked, writes to the below registers for EOUTPUT-XBAR is blocked. Registers Affected by the LOCK mechanism: OUTPUTXBAR Gx SEL OUTPUTXBAR.Invert OUTPUTXBARFlagInvert OUTPUTXBAROutLatch OUTPUTXBAROutStretch OUTPUTXBAROutLength 0: Writes to the above registers are allowed 1: Writes to the above registers are blocked Note: [1] LOCK mechanism only apples to writes. Reads are never blocked. Reset type: XRSn

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5 OUTPUTXBARG0SEL_j Register (Offset = 100h + formula) [Reset = 00000000h]

OUTPUTXBARG0SEL_j is shown in Figure 19-20 and described in Table 19-26.

Return to the Summary Table.

OUTPUTXBAR G0 Input Select

Offset = 100h + (j * 40h); where j = 0h to 7h

Figure 19-20. OUTPUTXBARG0SEL_j Register

31	30	29	28	27	26	25	24
INPUT31	INPUT30	INPUT29	INPUT28	INPUT27	INPUT26	INPUT25	INPUT24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INPUT23	INPUT22	INPUT21	INPUT20	INPUT19	INPUT18	INPUT17	INPUT16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INPUT15	INPUT14	INPUT13	INPUT12	INPUT11	INPUT10	INPUT9	INPUT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INPUT7	INPUT6	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1	INPUT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-41. OUTPUTXBARG0SEL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT31	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
30	INPUT30	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
29	INPUT29	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
28	INPUT28	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
27	INPUT27	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
26	INPUT26	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-41. OUTPUTXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INPUT25	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
24	INPUT24	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
23	INPUT23	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
22	INPUT22	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
21	INPUT21	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
20	INPUT20	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
19	INPUT19	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
18	INPUT18	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
17	INPUT17	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
16	INPUT16	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
15	INPUT15	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-41. OUTPUTXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INPUT14	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
13	INPUT13	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
12	INPUT12	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
11	INPUT11	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
10	INPUT10	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
9	INPUT9	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
8	INPUT8	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
7	INPUT7	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
6	INPUT6	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
5	INPUT5	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
4	INPUT4	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-41. OUTPUTXBARG0SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INPUT3	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
2	INPUT2	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
1	INPUT1	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
0	INPUT0	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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6 OUTPUTXBARG1SEL_j Register (Offset = 104h + formula) [Reset = 00000000h]

OUTPUTXBARG1SEL_j is shown in Figure 19-21 and described in Table 19-27.

Return to the Summary Table.

OUTPUTXBAR G1 Input Select

Offset = 104h + (j * 40h); where j = 0h to 7h

Figure 19-21. OUTPUTXBARG1SEL_j Register

31	30	29	28	27	26	25	24
INPUT31	INPUT30	INPUT29	INPUT28	INPUT27	INPUT26	INPUT25	INPUT24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
INPUT23	INPUT22	INPUT21	INPUT20	INPUT19	INPUT18	INPUT17	INPUT16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
INPUT15	INPUT14	INPUT13	INPUT12	INPUT11	INPUT10	INPUT9	INPUT8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INPUT7	INPUT6	INPUT5	INPUT4	INPUT3	INPUT2	INPUT1	INPUT0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 19-43. OUTPUTXBARG1SEL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUT31	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
30	INPUT30	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
29	INPUT29	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
28	INPUT28	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
27	INPUT27	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
26	INPUT26	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-43. OUTPUTXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INPUT25	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
24	INPUT24	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
23	INPUT23	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
22	INPUT22	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
21	INPUT21	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
20	INPUT20	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
19	INPUT19	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
18	INPUT18	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
17	INPUT17	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
16	INPUT16	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
15	INPUT15	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-43. OUTPUTXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	INPUT14	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
13	INPUT13	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
12	INPUT12	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
11	INPUT11	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
10	INPUT10	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
9	INPUT9	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
8	INPUT8	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
7	INPUT7	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
6	INPUT6	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
5	INPUT5	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
4	INPUT4	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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Table 19-43. OUTPUTXBARG1SEL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	INPUT3	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
2	INPUT2	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
1	INPUT1	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn
0	INPUT0	R/W	0h	Select input: 0 Not Selected 1 Input Selected Reset type: XRSn

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19.6.5 SYNC_SOC_REGS Registers

Table 19-28 lists the memory-mapped registers for the SYNC_SOC_REGS registers. All register offset addresses not listed in Table 19-28 should be considered as reserved locations and the register contents should not be modified.

Table 19-44. SYNC_SOC_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	SYNCSELECT	Sync Input and Output Select Register		Go
4h	ADCSOCOUTSELECT	External ADCSOC Select Register		Go
8h	SYNCSOCLOCK	SYNCSEL and EXTADCSOC Select Lock register		Go

Complex bit access types are encoded to fit into small table cells. Table 19-29 shows the codes that are used for access types in this section.

Table 19-45. SYNC_SOC_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 SYNCSELECT Register (Offset = 0h) [Reset = 00000000h]

SYNCSELECT is shown in Figure 19-22 and described in Table 19-30.

Return to the Summary Table.

Sync Input and Output Select Register

Figure 19-22. SYNCSELECT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SYNCOUT					RESERVED							
R-0-0h			R/W-0h					R-0-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R-0-0h															

Table 19-47. SYNCSELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R-0	0h	Reserved
28-24	SYNCOUT	R/W	0h	Select Syncout Source: 00000: MCPWM0SYNCOUT selected to drive the EXTSYNCOUT pin 00001: MCPWM1SYNCOUT selected to drive the EXTSYNCOUT pin 00010: MCPWM2SYNCOUT selected to drive the EXTSYNCOUT pin 00011: Reserved 00100: Reserved 00101: EPWM0SYNCOUT selected to drive the EXTSYNCOUT pin 00110: EPWM1SYNCOUT selected to drive the EXTSYNCOUT pin 00111: EPWM2SYNCOUT selected to drive the EXTSYNCOUT pin 01000: EPWM3SYNCOUT selected to drive the EXTSYNCOUT pin 01001: EPWM4SYNCOUT selected to drive the EXTSYNCOUT pin 01010: EPWM5SYNCOUT selected to drive the EXTSYNCOUT pin 01011: Reserved 01100: Reserved 01101: Reserved 01110: Reserved 01111: Reserved 10000: Reserved 10001: Reserved 10010: Reserved 10011: Reserved 10100: Reserved 10101: Reserved 10110: Reserved 10111: Reserved 11000: ECAP0SYNCOUT selected to drive the EXTSYNCOUT pin 11001: ECAP1SYNCOUT selected to drive the EXTSYNCOUT pin 11010: ECAP2SYNCOUT selected to drive the EXTSYNCOUT pin 11011: Reserved 11100: Reserved 11101: Reserved 11110: Reserved 11111: Reserved Notes: [1] Reserved position defaults to 00 selection Reset type: SYSRSn
23-0	RESERVED	R-0	0h	Reserved

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2 ADCSOCOUTSELECT Register (Offset = 4h) [Reset = 00000000h]

ADCSOCOUTSELECT is shown in Figure 19-23 and described in Table 19-31.

Return to the Summary Table.

External ADCSOC Select Register

Figure 19-23. ADCSOCOUTSELECT Register

31	30	29	28	27	26	25	24
RESERVED					EPWM5SOCBEN	EPWM4SOCBEN	EPWM3SOCBEN
R-0-0h					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
EPWM2SOCBEN	EPWM1SOCBEN	EPWM0SOCBEN	RESERVED		MCPWM2SOCBEN	MCPWM1SOCBEN	MCPWM0SOCBEN
R/W-0h	R/W-0h	R/W-0h	R-0-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED					EPWM5SOCAEN	EPWM4SOCAEN	EPWM3SOCAEN
R-0-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EPWM2SOCAEN	EPWM1SOCAEN	EPWM0SOCAEN	RESERVED		MCPWM2SOCAEN	MCPWM1SOCAEN	MCPWM0SOCAEN
R/W-0h	R/W-0h	R/W-0h	R-0-0h		R/W-0h	R/W-0h	R/W-0h

Table 19-49. ADCSOCOUTSELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R-0	0h	Reserved
26	EPWM5SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
25	EPWM4SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
24	EPWM3SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
23	EPWM2SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
22	EPWM1SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn

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Table 19-49. ADCSOCOUTSELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	EPWM0SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
20-19	RESERVED	R-0	0h	Reserved
18	MCPWM2SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
17	MCPWM1SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
16	MCPWM0SOCBEN	R/W	0h	ADCSOCBOn source select: 0: Respective PWM SOCB output is not selected 1: Respective PWM SOCB output is selected Reset type: SYSRSn
15-11	RESERVED	R-0	0h	Reserved
10	EPWM5SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
9	EPWM4SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
8	EPWM3SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
7	EPWM2SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
6	EPWM1SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
5	EPWM0SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
4-3	RESERVED	R-0	0h	Reserved
2	MCPWM2SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn

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Table 19-49. ADCSOCOUTSELECT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MCPWM1SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn
0	MCPWM0SOCAEN	R/W	0h	ADCSOCAOn source select: 0: Respective PWM SOCA output is not selected 1: Respective PWM SOCA output is selected Reset type: SYSRSn

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3 SYNCSOCLOCK Register (Offset = 8h) [Reset = 00000000h]

SYNCSOCLOCK is shown in Figure 19-24 and described in Table 19-32.

Return to the Summary Table.

SYNCSEL and EXTADCSOC Select Lock register

Figure 19-24. SYNCSOCLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						ADCSOCOUTSELECT	SYNCSELECT
R-0-0h						R/WSonce-0h	R/WSonce-0h

Table 19-51. SYNCSOCLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	ADCSOCOUTSELECT	R/WSonce	0h	ADCSOCOUTSELECT Register Lock bit: 0: Respective register is not locked 1: Respective register is locked. Notes: [1] Any bit in this register, once set can only be creaed through a SYSRSn. Write of 0 to any bit of this regtister has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed Reset type: SYSRSn
0	SYNCSELECT	R/WSonce	0h	SYNCSELECT Register Lock bit: 0: Respective register is not locked 1: Respective register is locked. Notes: [1] Any bit in this register, once set can only be creaed through a SYSRSn. Write of 0 to any bit of this regtister has no effect [2] The locking mechanism applies to only writes. Reads to the registers which have LOCK protection are always allowed Reset type: SYSRSn

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19.6.6 OUTPUTXBAR_FLAG_REGS Registers

Table 19-33 lists the memory-mapped registers for the OUTPUTXBAR_FLAG_REGS registers. All register offset addresses not listed in Table 19-33 should be considered as reserved locations and the register contents should not be modified.

Table 19-52. OUTPUTXBAR_FLAG_REGS Registers

Offset	Acronym	Register Name	Group	Section
10h	OUTPUTXBARStatus	Output Signal Status register		Go
18h	OUTPUTXBARFlag	Output latched flag register		Go
1Ch	OUTPUTXBARFlagClear	Output latched flag clear register		Go
20h	OUTPUTXBARFlagForce	Output latched flag Force register		Go

Complex bit access types are encoded to fit into small table cells. Table 19-34 shows the codes that are used for access types in this section.

Table 19-53. OUTPUTXBAR_FLAG_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 OUTPUTXBARStatus Register (Offset = 10h) [Reset = 00000000h]

OUTPUTXBARStatus is shown in Figure 19-25 and described in Table 19-35.

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Output Signal Status register

Figure 19-25. OUTPUTXBARStatus Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															STS
R-0-0h															R-0h

Table 19-55. OUTPUTXBARStatus Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	STS	R	0h	Output Signal Status: 0 Low State 1 High State Reset type: XRSn

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2 OUTPUTXBARFlag Register (Offset = 18h) [Reset = 00000000h]

OUTPUTXBARFlag is shown in Figure 19-26 and described in Table 19-36.

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Output latched flag register

Figure 19-26. OUTPUTXBARFlag Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FLG
R-0-0h															R-0h

Table 19-57. OUTPUTXBARFlag Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	FLG	R	0h	Output Signal Latched Flag: 0 No Input Latched Event 1 Latched Event Reset type: XRSn

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3 OUTPUTXBARFlagClear Register (Offset = 1Ch) [Reset = 00000000h]

OUTPUTXBARFlagClear is shown in Figure 19-27 and described in Table 19-37.

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Output latched flag clear register

Figure 19-27. OUTPUTXBARFlagClear Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FLG
R-0-0h															R-0/W1S-0h

Table 19-59. OUTPUTXBARFlagClear Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	FLG	R-0/W1S	0h	Output Signal Latched Flag Clear: Write of 1 will clear flag. If Flag is being cleared by S/W and a new flag is being latched, hardware has priority. Reset type: XRSn

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4 OUTPUTXBARFlagForce Register (Offset = 20h) [Reset = 00000000h]

OUTPUTXBARFlagForce is shown in Figure 19-28 and described in Table 19-38.

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Output latched flag Force register

Figure 19-28. OUTPUTXBARFlagForce Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															FLG
R-0-0h															R-0/W1S-0h

Table 19-61. OUTPUTXBARFlagForce Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	FLG	R-0/W1S	0h	Output Signal Latched Flag Force: Write of 1 will set flag. Reset type: XRSn

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19.6.7 INPUT_FLAG_XBAR_REGS Registers

Table 19-39 lists the memory-mapped registers for the INPUT_FLAG_XBAR_REGS registers. All register offset addresses not listed in Table 19-39 should be considered as reserved locations and the register contents should not be modified.

Table 19-62. INPUT_FLAG_XBAR_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	XBARFLG1	X-Bar Input Flag Register 1		Go
4h	XBARFLG2	X-Bar Input Flag Register 2		Go
8h	XBARFLG3	X-Bar Input Flag Register 3		Go
10h	XBARCLR1	X-Bar Input Flag Clear Register 1		Go
14h	XBARCLR2	X-Bar Input Flag Clear Register 2		Go
18h	XBARCLR3	X-Bar Input Flag Clear Register 3		Go

Complex bit access types are encoded to fit into small table cells. Table 19-40 shows the codes that are used for access types in this section.

Table 19-63. INPUT_FLAG_XBAR_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 XBARFLG1 Register (Offset = 0h) [Reset = 00000000h]

XBARFLG1 is shown in Figure 19-29 and described in Table 19-41.

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X-Bar Input Flag Register 1

Figure 19-29. XBARFLG1 Register

31	30	29	28	27	26	25	24
INPUTXBAR12	INPUTXBAR11	INPUTXBAR10	INPUTXBAR9	INPUTXBAR8	INPUTXBAR7	INPUTXBAR6	INPUTXBAR5
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
INPUTXBAR4	INPUTXBAR3	INPUTXBAR2	INPUTXBAR1	ADC2EVT4	ADC2EVT3	ADC2EVT2	ADC2EVT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
ADC1EVT4	ADC1EVT3	ADC1EVT2	ADC1EVT1	ADC0EVT4	ADC0EVT3	ADC0EVT2	ADC0EVT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CMPSS3_CTRIPL	CMPSS3_CTRIPH	CMPSS2_CTRIPL	CMPSS2_CTRIPH	CMPSS1_CTRIPL	CMPSS1_CTRIPH	CMPSS0_CTRIPL	CMPSS0_CTRIPH
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 19-65. XBARFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUTXBAR12	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
30	INPUTXBAR11	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
29	INPUTXBAR10	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
28	INPUTXBAR9	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-65. XBARFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	INPUTXBAR8	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
26	INPUTXBAR7	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
25	INPUTXBAR6	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
24	INPUTXBAR5	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
23	INPUTXBAR4	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
22	INPUTXBAR3	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
21	INPUTXBAR2	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-65. XBARFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	INPUTXBAR1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
19	ADC2EVT4	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
18	ADC2EVT3	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
17	ADC2EVT2	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
16	ADC2EVT1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
15	ADC1EVT4	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
14	ADC1EVT3	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-65. XBARFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADC1EVT2	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
12	ADC1EVT1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
11	ADC0EVT4	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
10	ADC0EVT3	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
9	ADC0EVT2	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
8	ADC0EVT1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
7	CMPSS3_CTRIPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-65. XBARFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CMPSS3_CTRIPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
5	CMPSS2_CTRIPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
4	CMPSS2_CTRIPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
3	CMPSS1_CTRIPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
2	CMPSS1_CTRIPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
1	CMPSS0_CTRIPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
0	CMPSS0_CTRIPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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2 XBARFLG2 Register (Offset = 4h) [Reset = 00000000h]

XBARFLG2 is shown in Figure 19-30 and described in Table 19-42.

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X-Bar Input Flag Register 2

Figure 19-30. XBARFLG2 Register

31	30	29	28	27	26	25	24
RESERVED	ECAP2_OUT	CPU_HALTED	CMPSS3_CTRIPOUTL	CMPSS3_CTRIPOUTH	CMPSS2_CTRIPOUTL	CMPSS2_CTRIPOUTH	CMPSS1_CTRIPOUTL
R-0-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
CMPSS1_CTRIPOUTH	CMPSS0_CTRIPOUTL	CMPSS0_CTRIPOUTH	RESERVED	RESERVED	EQEP1_STROBE_SYNCOUT	EQEP1_INDEX_SYNCOUT	EQEP0_STROBE_SYNCOUT
R-0h	R-0h	R-0h	R-0-0h	R-0-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
EQEP0_INDEX_SYNCOUT	RESERVED	EQEP1_ERR	EQEP0_ERR	RESERVED	MCAN1_INT0	MCAN0_INT0	EXTSYNCOUT
R-0h	R-0-0h	R-0h	R-0h	R-0-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ADCSOCB	ADCSOCA	ECAP1_OUT	ECAP0_OUT	INPUTXBAR16	INPUTXBAR15	INPUTXBAR14	INPUTXBAR13
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 19-67. XBARFLG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R-0	0h	Reserved
30	ECAP2_OUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
29	CPU_HALTED	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
28	CMPSS3_CTRIPOUTL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-67. XBARFLG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMPSS3_CTRIPOUTH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
26	CMPSS2_CTRIPOUTL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
25	CMPSS2_CTRIPOUTH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
24	CMPSS1_CTRIPOUTL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
23	CMPSS1_CTRIPOUTH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
22	CMPSS0_CTRIPOUTL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
21	CMPSS0_CTRIPOUTH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
20	RESERVED	R-0	0h	Reserved
19	RESERVED	R-0	0h	Reserved

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Table 19-67. XBARFLG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	EQEP1_STROBE_SYNCOUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
17	EQEP1_INDEX_SYNCOUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
16	EQEP0_STROBE_SYNCOUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
15	EQEP0_INDEX_SYNCOUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
14	RESERVED	R-0	0h	Reserved
13	EQEP1_ERR	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
12	EQEP0_ERR	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
11	RESERVED	R-0	0h	Reserved
10	MCAN1_INT0	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-67. XBARFLG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MCAN0_INT0	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
8	EXTSYNCOUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
7	ADCSOCB	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
6	ADCSOCA	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
5	ECAP1_OUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
4	ECAP0_OUT	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
3	INPUTXBAR16	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-67. XBARFLG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INPUTXBAR15	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
1	INPUTXBAR14	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
0	INPUTXBAR13	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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3 XBARFLG3 Register (Offset = 8h) [Reset = 00000000h]

XBARFLG3 is shown in Figure 19-31 and described in Table 19-43.

Return to the Summary Table.

X-Bar Input Flag Register 3

Figure 19-31. XBARFLG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED				ECAT_SYNC1	ECAT_SYNC0	FSIRXA_TRIG2	FSIRXA_TRIG1
R-0-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SD0FLT4_COMPL	SD0FLT4_COMPH	SD0FLT3_COMPL	SD0FLT3_COMPH	SD0FLT2_COMPL	SD0FLT2_COMPH	SD0FLT1_COMPL	SD0FLT1_COMPH
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 19-69. XBARFLG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11	ECAT_SYNC1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
10	ECAT_SYNC0	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
9	FSIRXA_TRIG2	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
8	FSIRXA_TRIG1	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-69. XBARFLG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SD0FLT4_COMPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
6	SD0FLT4_COMPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
5	SD0FLT3_COMPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
4	SD0FLT3_COMPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
3	SD0FLT2_COMPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
2	SD0FLT2_COMPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn
1	SD0FLT1_COMPL	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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Table 19-69. XBARFLG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD0FLT1_COMPH	R	0h	This register is used to Flag the inputs of the X-Bars to provide software knowledge of the input sources which got triggered. 1: Corresponding Input was triggered 0: Corresponding Input was not triggered Note: [1] setting of this bit has priority over clear by software Reset type: CPU1.SYSRSn

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4 XBARCLR1 Register (Offset = 10h) [Reset = 00000000h]

XBARCLR1 is shown in Figure 19-32 and described in Table 19-44.

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X-Bar Input Flag Clear Register 1

Figure 19-32. XBARCLR1 Register

31	30	29	28	27	26	25	24
INPUTXBAR12	INPUTXBAR11	INPUTXBAR10	INPUTXBAR9	INPUTXBAR8	INPUTXBAR7	INPUTXBAR6	INPUTXBAR5
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
23	22	21	20	19	18	17	16
INPUTXBAR4	INPUTXBAR3	INPUTXBAR2	INPUTXBAR1	ADC2EVT4	ADC2EVT3	ADC2EVT2	ADC2EVT1
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
15	14	13	12	11	10	9	8
ADC1EVT4	ADC1EVT3	ADC1EVT2	ADC1EVT1	ADC0EVT4	ADC0EVT3	ADC0EVT2	ADC0EVT1
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
CMPSS3_CTRIPL	CMPSS3_CTRIPH	CMPSS2_CTRIPL	CMPSS2_CTRIPH	CMPSS1_CTRIPL	CMPSS1_CTRIPH	CMPSS0_CTRIPL	CMPSS0_CTRIPH
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 19-71. XBARCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INPUTXBAR12	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
30	INPUTXBAR11	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
29	INPUTXBAR10	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
28	INPUTXBAR9	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
27	INPUTXBAR8	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
26	INPUTXBAR7	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-71. XBARCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INPUTXBAR6	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
24	INPUTXBAR5	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
23	INPUTXBAR4	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
22	INPUTXBAR3	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
21	INPUTXBAR2	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
20	INPUTXBAR1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
19	ADC2EVT4	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
18	ADC2EVT3	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
17	ADC2EVT2	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
16	ADC2EVT1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
15	ADC1EVT4	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-71. XBARCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ADC1EVT3	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
13	ADC1EVT2	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
12	ADC1EVT1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
11	ADC0EVT4	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
10	ADC0EVT3	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
9	ADC0EVT2	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
8	ADC0EVT1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
7	CMPSS3_CTRIPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
6	CMPSS3_CTRIPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
5	CMPSS2_CTRIPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
4	CMPSS2_CTRIPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-71. XBARCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMPSS1_CTRIPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
2	CMPSS1_CTRIPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
1	CMPSS0_CTRIPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
0	CMPSS0_CTRIPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG1 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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5 XBARCLR2 Register (Offset = 14h) [Reset = 00000000h]

XBARCLR2 is shown in Figure 19-33 and described in Table 19-45.

Return to the Summary Table.

X-Bar Input Flag Clear Register 2

Figure 19-33. XBARCLR2 Register

31	30	29	28	27	26	25	24
RESERVED	ECAP2_OUT	CPU_HALTED	CMPSS3_CTRIPOUTL	CMPSS3_CTRIPOUTH	CMPSS2_CTRIPOUTL	CMPSS2_CTRIPOUTH	CMPSS1_CTRIPOUTL
R-0-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
23	22	21	20	19	18	17	16
CMPSS1_CTRIPOUTH	CMPSS0_CTRIPOUTL	CMPSS0_CTRIPOUTH	RESERVED	RESERVED	EQEP1_STROBE_SYNCOUT	EQEP1_INDEX_SYNCOUT	EQEP0_STROBE_SYNCOUT
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0-0h	R-0-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
15	14	13	12	11	10	9	8
EQEP0_INDEX_SYNCOUT	RESERVED	EQEP1_ERR	EQEP0_ERR	RESERVED	MCAN1_INT0	MCAN0_INT0	EXTSYNCOUT
R-0/W1C-0h	R-0-0h	R-0/W1C-0h	R-0/W1C-0h	R-0-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
ADCSOCB	ADCSOCA	ECAP1_OUT	ECAP0_OUT	INPUTXBAR16	INPUTXBAR15	INPUTXBAR14	INPUTXBAR13
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 19-73. XBARCLR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R-0	0h	Reserved
30	ECAP2_OUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
29	CPU_HALTED	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
28	CMPSS3_CTRIPOUTL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
27	CMPSS3_CTRIPOUTH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
26	CMPSS2_CTRIPOUTL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-73. XBARCLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	CMPSS2_CTRIPOUTH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
24	CMPSS1_CTRIPOUTL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
23	CMPSS1_CTRIPOUTH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
22	CMPSS0_CTRIPOUTL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
21	CMPSS0_CTRIPOUTH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
20	RESERVED	R-0	0h	Reserved
19	RESERVED	R-0	0h	Reserved
18	EQEP1_STROBE_SYNCOUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
17	EQEP1_INDEX_SYNCOUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
16	EQEP0_STROBE_SYNCOUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
15	EQEP0_INDEX_SYNCOUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
14	RESERVED	R-0	0h	Reserved
13	EQEP1_ERR	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
12	EQEP0_ERR	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-73. XBARCLR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESERVED	R-0	0h	Reserved
10	MCAN1_INT0	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
9	MCAN0_INT0	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
8	EXTSYNCOUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
7	ADCSOCB	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
6	ADCSOCA	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
5	ECAP1_OUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
4	ECAP0_OUT	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
3	INPUTXBAR16	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
2	INPUTXBAR15	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
1	INPUTXBAR14	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
0	INPUTXBAR13	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG2 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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6 XBARCLR3 Register (Offset = 18h) [Reset = 00000000h]

XBARCLR3 is shown in Figure 19-34 and described in Table 19-46.

Return to the Summary Table.

X-Bar Input Flag Clear Register 3

Figure 19-34. XBARCLR3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED				ECAT_SYNC1	ECAT_SYNC0	FSIRXA_TRIG2	FSIRXA_TRIG1
R-0-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
SD0FLT4_COMPL	SD0FLT4_COMPH	SD0FLT3_COMPL	SD0FLT3_COMPH	SD0FLT2_COMPL	SD0FLT2_COMPH	SD0FLT1_COMPL	SD0FLT1_COMPH
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 19-75. XBARCLR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11	ECAT_SYNC1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
10	ECAT_SYNC0	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
9	FSIRXA_TRIG2	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
8	FSIRXA_TRIG1	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
7	SD0FLT4_COMPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
6	SD0FLT4_COMPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Table 19-75. XBARCLR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SD0FLT3_COMPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
4	SD0FLT3_COMPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
3	SD0FLT2_COMPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
2	SD0FLT2_COMPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
1	SD0FLT1_COMPL	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn
0	SD0FLT1_COMPH	R-0/W1C	0h	Writing 1 to a bit in this register clears the corresponding bit in the XBARFLG3 register. Writing 0 has no effect Reset type: CPU1.SYSRSn

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Chapter 20

Analog-to-Digital Converter (ADC)

The analog-to-digital converter (ADC) module is described in this chapter.

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20.1 Introduction

The ADC module is a 12-bit successive approximation (SAR) style ADC.. The ADC is composed of an analog core and a digital wrapper. The core is composed of the analog circuits which include the channel select MUX, the sample-and-hold (S+H) circuit, the successive approximation circuits, voltage reference circuits, and other support circuitry. The wrapper is composed of the digital circuits that configure and control the ADC. These circuits include the logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC core consists of a single sample-and-hold (S+H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is sequencer (SEQ) based.

20.1.1 Features

Each ADC supports the following features:

- 12-bit resolution
- External reference set by VREFHI and VREFLO pins
- Selectable internal reference (Note: Refer to device Datasheet for internal ADC reference voltages)
- Single-ended (SE) signal conversions
- Input multiplexer with up to 32 channels (Note: Refer to the device Datasheet for pinned-out ADC Input channels)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources:
  - S/W - software immediate start
  - All PWMs - ADCSOC A, B, C or D
  - TIMG4_0.GEN_EVENT0/TIMG12_0_GEN_EVENT0
  - GPIO: INPUTXBAR[5]
  - ADCINT1/2
- Four flexible NVIC interrupts and four DMA triggers
- Configurable interrupt placement
- Four post-processing blocks, each with:
  - High, low, zero-crossing and in-limit compare, with interrupt and PWM trip capability
  - Aggregation functions: sum and average (binary shift)

Note

Not every channel is pinned out from all ADCs. Check the device data sheet to determine which channels are available.

20.1.2 ADC Related Collateral

Foundational Materials

- *ADC Input Circuit Evaluation for C2000 MCUs (PSPICE for TI) Application Report*
- *ADC Input Circuit Evaluation for C2000 MCUs (TINA-TI) Application Report*
- PSpice for TI design and simulation tool
- *Real-Time Control Reference Guide*
  - Refer to the ADC section
- TI Precision Labs - ADCs
- TI Precision Labs: Driving the reference input on a SAR ADC (Video)
- TI Precision Labs: Introduction to analog-to-digital converters (ADCs) (Video)
- TI Precision Labs: SAR ADC input driver design (Video)
- TI e2e: Connecting VDDA to VREFHI
- TI e2e: Topologies for ADC Input Protection
- TI e2e: Why does the ADC Input Voltage drop with sampling?

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  - Sampling a high impedance voltage divider with ADC
- *Understanding Data Converters Application Report*
- *VREFHI Input Driver Design for C2000 MCUs Application Report*

Getting Started Materials

- ADC-PWM Synchronization Using ADC Interrupt
  - NOTE: This is a non-TI (third party) site.
- *Hardware Design Guide for F2800x C2000 Real-Time MCU Series*

Expert Materials

- *A potential firmware mistake may lead to control instability*
- Analog Engineer's Calculator
- *Analog Engineer's Pocket Reference*
- Debugging an integrated ADC in a microcontroller using an oscilloscope
- TI Precision Labs: ADC AC specifications (Video)
- TI Precision Labs: ADC Error sources (Video)
- TI Precision Labs: ADC Noise (Video)
- TI Precision Labs: Analog-to-digital converter (ADC) drive topologies (Video)
- TI Precision Labs: Electrical overstress on data converters (Video)
- TI Precision Labs: High-speed ADC fundamentals (Video)
- TI Precision Labs: SAR & Delta-Sigma: Understanding the Difference (Video)
- TI e2e: ADC Bandwidth Clarification
- TI e2e: ADC Resolution with Oversampling
- TI e2e: ADC configuration for interleaved mode
- TI e2e: Simultaneous Sampling with Single ADC

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20.1.3 Block Diagram

Figure 20-1 shows the block diagram for the ADC core and ADC wrapper.

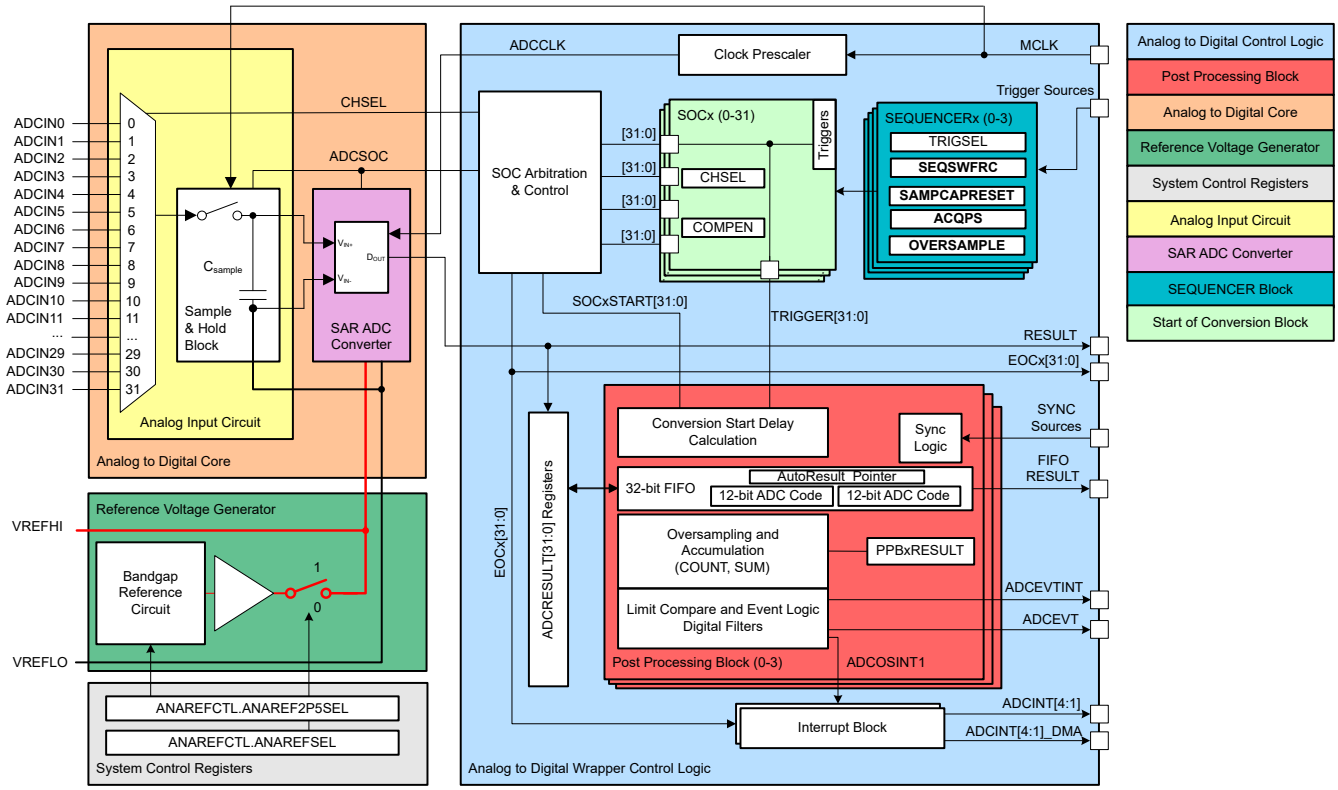


Figure 20-1. ADC Module Block Diagram

Note

- The ADC block diagram reflects the number of ADC channels internally configurable on the device. The actual number of available external ADC inputs varies depending on device part number and package type.

20.1.4 ADC Glossary

ACQPS	**"ACQ**uisition **P**re**S**caler"- A register field in that configures the acquisition window duration.
ADC	**"Analog to Digital Converter"** - A module that converts an analog input voltage into a digital value.
ADCCLK	The internal clock that drives the ADC core conversion logic. ADCCLK is derived from the system clock (MCLK) through a prescaler register. The ADCCLK frequency must not exceed the maximum value specified in the device data sheet.
ADCINx	An analog input channel. Each SOC can be configured to convert any available ADCINx channel. Inputs include external pins and internally routed signals such as PGA_OUT, or the internal gain calibration channel.
ADCINT1–ADCINT4	ADC interrupt channels. Each ADCINT flag can be linked to any SOC's EOC signal. ADCINT1 and ADCINT2 can also be configured to trigger additional SOC conversions through the ADC Trigger Select registers. ADCINT1 can also be selected as a sequencer trigger (ADCSEQxCONFIG.TRIGSEL[16:18]

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ADCRESULT	A 12-bit read-only register that holds the digital output of an SOC conversion. Result registers are indexed per SOC (ADCRESULT0–ADCRESULT15) and represent the digitized input as an unsigned integer from 0 to 4095.
Acquisition window	The time during which the ADC sample capacitor is allowed to charge before the conversion begins. The duration must be at least one ADCCLK cycle and must meet the nanosecond minimum specified in the device data sheet. A longer window improves settling accuracy for high-impedance signal sources.
Conversion phase	The second stage of an ADC conversion, following the sample-and-hold (S+H) phase. During this phase, the ADC digitizes the voltage captured on the sample capacitor. Refer to the device datasheet for the exact conversion time.
DLYSTAMP	"Delay Stamp" - A field in the ADCPPBxSTAMP register that records the number of MCLK cycles between when a SOC was triggered and when the ADC actually began sampling it. Used in multi-loop applications to detect and compensate for sample timing delay caused by sample arbitration.
Early interrupt mode	An interrupt configuration in which the ADC interrupt fires before the conversion result is ready (before EOC). Enabled by clearing ADCCTL1.INTPULSEPOS to 0. The DELAY field in ADCINTCYCLE sets how many MCLK cycles after the end of the S+H window, before EOC the interrupt fires. This allows the CPU/SW to pre-execute ISR overhead.
EOC	"End Of Conversion" - A pulse generated when an SOC conversion completes. EOC can be configured to fire at the end of the acquisition window or at the end of the voltage conversion phase (ADCCTL1.INTPULSEPOS). EOC sets an ADCINT flag and can optionally trigger additional SOC conversions.
FIFO	"First-in First-out" - A result buffer associated with each sequencer (SEQ1–SEQ4). As each SOC in a sequencer completes, its result is pushed into the FIFO via ADCSEQxFIFORESULT. The ADCSEQxFIFOSTATUS register provides SEQFIFOVALID and SEQFIFOPENDREAD bits indicating whether unread data is present.
Gain calibration	A procedure that corrects the ADC's gain error. Factory gain trim values are stored in OTP memory and applied at boot. Additional on-board gain trimming can be performed using the internal calibration channel with a known reference voltage.
Global software trigger	A synchronous trigger that simultaneously starts SOC conversions across multiple ADC instances. On the AM13E23x devices, this is routed through INPUTXBAR[5]. A global software trigger ensures that all targeted ADC modules begin sampling on exactly the same MCLK cycle.
INPUTXBAR	"Input Crossbar" - A hardware interconnect that routes digital signals from external pins and internal peripherals to ADC SOC trigger inputs and other destinations. The ADC supports INPUTXBAR.OUT[5] as a GPIO-based SOC trigger source.
Interrupt overflow	A condition that occurs when an EOC pulse attempts to set an ADCINT flag that is already set and not yet cleared by software. The event is recorded in the ADCINTOVF register. An overflow does not block subsequent interrupts but indicates the ISR is not running fast enough.
LSB	"Least-significant bit" - The smallest measurable step in the 12-bit ADC output. For a reference span of (VREFHI − VREFLO), 1 LSB = (VREFHI − VREFLO) / 4096.
MCLK	"Main Clock" - The primary system clock for the device. MCLK drives the ADC sample-and-hold circuitry, sequencer control logic, and PPB. ADCCLK is derived from MCLK through a configurable prescaler.
Memory crosstalk	A sampling error that occurs when the ADC samples multiple channels in sequence without sufficient acquisition time. The sample capacitor retains charge from the previous conversion, pulling the new result toward the previous channel's voltage. Mitigated by increasing the acquisition window or enabling sample capacitor reset.

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OFFCAL	"Offset Calibration" - A signed field in ADCPPBxOFFCAL that applies a per-channel offset correction to raw ADC results. The PPB adds the OFFCAL value to the raw ADCRESULT and stores the corrected value in the ADCRESULT register. Writing 0 disables offset correction.
OFFREF	"Offset Reference" - A field in ADCPPBxOFFREF that stores a reference value. The PPB subtracts OFFREF from the raw ADCRESULT and stores the signed, sign-extended 32-bit error in ADCPPBxRESULT. Used to compute control error relative to a set point.
OTP memory	"One-time-programmable memory - A non-volatile memory region that stores factory-calibrated gain, offset, and linearity trim values for the ADC and other analog modules. OTP values are loaded into ADC trim registers at boot.
Oversampling	A technique that improves effective resolution or noise performance by sampling the same signal multiple times and averaging the results. Achieved by assigning multiple SOCs to the same channel and trigger, or by using the trigger repeater module with a single trigger source.
PGA_OF	"PGA_OUTPUT_FILTERED" - The RC-filtered output of an on-chip Programmable Gain Amplifier (PGA). PGA_OF has reduced high-frequency noise but lower bandwidth, requiring a longer acquisition window when used as an ADC input.
PGA_OUT	"PGA_OUTPUT" - The unfiltered, full-bandwidth output of an on-chip Programmable Gain Amplifier (PGA). PGA_OUT can be routed directly to an ADC input channel and requires a shorter acquisition window than PGA_OF.
PPB	"Post Processing Block - A hardware block that processes ADC results with zero software overhead. Each ADC module has four PPBs (PPB1–PPB4). Functions include: offset correction, set-point error calculation, high/low limit comparison, zero-crossing detection, oversampling accumulation, and sample delay capture.
PPB limit detection	A PPB function that compares ADCPPBxRESULT against programmed high (LIMITHI) and low (LIMITLO) thresholds. When a threshold is exceeded, the corresponding flag is set in ADCEVTSTAT, and an interrupt or PWM trip event can optionally be generated.
PPB oversampling	A PPB function that hardware-accumulates results from multiple oversampled conversions. The PPB maintains partial sum (PSUM), full sum (SUM), partial count (PCOUNT), and full count (COUNT) registers, reducing software overhead for averaging or decimation.
Resolution	The number of discrete output levels the ADC produces.
S+H	"Sample + Hold" - The first stage of an ADC conversion. The ADC connects the sample capacitor (Ch) to the analog input and allows it to charge to the input voltage. S+H duration equals the acquisition window, configured by ACQPS.
Sample/Hold capacitor (Ch)	The capacitor inside the ADC core that stores the analog input voltage during the sample-and-hold phase. If the acquisition window is too short, the capacitor may not fully charge, contributing to memory crosstalk and conversion error.
Sample capacitor reset	A feature that discharges the sample capacitor to VREFLO or VREFHI/2 after each conversion (configured by ADCSEQxCONFIG.SAMPCAPRESETSEL). Reduces memory crosstalk when sampling multiple different channels in succession. Requires additional acquisition time to allow the capacitor to re-settle.
SEQEND	A register field in ADCSEQCTL that defines the last SOC index of the final sequencer. Combined with SEQSTART values, SEQEND determines the number of SOCs allocated across all four sequencers.
SEQPREEMPT	A two-bit field in ADCSEQCTL that governs how a higher-priority sequencer interrupts a lower-priority sequencer in progress. • 0x: disabled (current sequence completes first). • 10: enabled without restart (aborted sequence is discarded).

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	• 11: enabled with restart (aborted sequence restarts after higher-priority sequence completes).
SEQSTART	A field in ADCSEQxCONFIG that specifies the first SOC index assigned to sequencer x. The sequencer begins converting from SEQSTART and converts subsequent SOCs in ascending order until the end of the sequencer range.
SEQ	"Sequencer" - A hardware block that groups a contiguous range of SOCs and converts them in ascending order when triggered. The device ADC supports four sequencers with fixed priority: SEQ1 > SEQ2 > SEQ3 > SEQ4. Multiple sequencers can share a trigger source.
Single-ended signal mode	The ADC input mode used by the device, in which the analog input voltage is measured relative to VREFLO rather than as a differential pair. Single-ended mode is fixed and not configurable.
SOC	"Start Of Conversion" - A hardware configuration set that defines one ADC conversion. Each SOC specifies the input channel (CHSEL).
TRIGSEL	"Trigger Select" - A field in ADCSEQxCONFIG that selects the hardware trigger source for an SOC. Sources include software trigger, PWM event outputs (ADCSOCx), GPIO via INPUTXBAR, and timer events.
Two's complement	A bit in ADCPPBxCONFIG that, when set, negates the PPB error result before storing it in ADCPPBxRESULT. Used when a bipolar or sign-inverted error representation is needed for control loop calculations.
VREFHI	"Voltage Reference High" - The high-side reference voltage for the ADC. An analog input at or above VREFHI produces the maximum output code. VREFHI can be sourced from the internal on-chip bandgap or from an external pin.
VREFLO	"Voltage Reference Low" - The low-side reference voltage for the ADC. An analog input at or below VREFLO produces the minimum output code (0). VREFLO is typically connected to analog ground (0 V).
Zero-crossing detection	A PPB function that detects when the PPB result transitions through zero. No threshold configuration is required. When a zero-crossing occurs, a flag is set in ADCEVTSTAT and an interrupt or PWM trip can be generated. A result of exactly zero is treated as positive.
Zero offset calibration	A calibration procedure that removes systematic zero-code offset error from the ADC. Factory offset trim values are stored in OTP memory and applied automatically at boot. The user can also perform zero offset calibration using the internal calibration channel.

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20.2 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 20-1 summarizes the basic ADC options and the level of configurability. The subsequent sections discuss these configurations.

Table 20-1. ADC Options and Configuration Levels

Options	Configurability
Clock	Per module(1)
Resolution	Not configurable (12-bit only)
Signal Mode	Not configurable (single-ended only)
Reference Voltage Source	Either external or internal for all modules
Trigger Source	Per SOC(1)
Converted Channel	Per SOC
Acquisition Window Duration	Per SOC(1)
EOC Location	Per module
Burst Mode	Per module(1)
Sample capacitor reset	Per SOC(1)

(1) Writing these values differently to different ADC modules can cause the ADCs to operate asynchronously. See *Ensuring Synchronous Operation* for guidance on when the ADCs are operating synchronously or asynchronously.

20.2.1 ADC Clock Configuration

The base ADC clock is provided directly by the system clock. MCLK is used to generate the ADC acquisition window. The register ADCCTL2 has a PRESCALE field that determines the ADCCLK. ADCCLK is used to clock the converter, and is only active during the conversion phase. At all other times, including during the sample-and-hold window, the ADCCLK signal is gated off.

The ADC core requires approximately 11 ADCCLK cycles to process a voltage into a conversion result. The user must determine the required duration of the acquisition window, see *Choosing an Acquisition Window Duration*.

Note

To determine an appropriate value for ADCCTL2.PRESCALE, see the device data sheet for the maximum allowable ADCCLK frequencies.

20.2.2 Resolution

The resolution of the ADC determines how finely the analog range is quantized into digital values. Each ADC module supports a fixed resolution of 12 bits.

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20.2.3 Voltage Reference

20.2.3.1 External Reference Mode

The ADC module share VREFHI and VREFLO inputs. In external reference mode, these pins are used as a ratiometric reference to determine the ADC conversion input range.

See Section 20.12.6 for information on how to supply the reference voltage.

Note

- On devices with no external VREFHI and VREFLO pin, VREFHI is internally tied to VDDA and VREFLO is internally connected to the device analog ground, VSSA. Internal reference mode is not available for packages lacking VREFHI and VREFLO pins. See the device data sheet for packages with VREFHI and VREFLO pins available.
- See the device data sheet to determine the allowable voltage range for VREFHI and VREFLO.
- The external reference mode requires an external capacitor on the VREFHI pin. See the device data sheet for the specific value required.

20.2.3.2 Internal Reference Mode

In internal reference mode, the device drives a voltage out onto the VREFHI pin. The VREFHI and VREFLO pins then set the ADC conversion range. Internal reference mode is not available for packages without VREFHI and VREFLO pins. See the device data sheet for packages with VREFHI and VREFLO pins available.

The internal reference voltage can be configured to be either 2.5V or 1.65V. When the 1.65V internal reference voltage is selected, the ADC input signal is internally divided by 2 before conversion, which effectively makes the ADC conversion range from VREFLO to 3.3V.

Note

The internal reference mode also requires an external capacitor on the VREFHI pin. See the device data sheet for the specific value required.

20.2.3.3 Selecting Reference Mode

The voltage reference mode must be configured by using either the ADC_setVREF() or the SetVREF() functions, depending on the header files used, provided in the Device SDK. Using either of these functions makes sure that the correct trim is loaded in the ADC trim registers. This function must be called at least once after a device reset. Do not configure the voltage reference mode by directly writing to the associated analog reference voltage control register.

20.2.4 Signal Mode

The ADC supports single-ended signaling.

In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

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20.2.4.1 Expected Conversion Results

Based on a given analog input voltage, the expected digital conversion is given in Table 20-2. Fractional values are truncated.

Table 20-2. Analog to 12-bit Digital Formulas

Analog Input	Digital Result
when ADCINy ≤ VREFLO	ADCRESULTx = 0
when VREFLO < ADCINy < VREFHI	$\text{ADCRESULTx} = 4096 \left(\frac{\text{ADCINy - VREFLO}}{\text{VREFHI - VREFLO}} \right)$
when ADCINy ≥ VREFHI	ADCRESULTx = 4095

20.2.4.2 Interpreting Conversion Results

Based on a given ADC conversion result, the corresponding analog input is given in Table 20-3. This corresponds to the center of the possible range of analog voltages that can produce this conversion result.

Table 20-3. 12-Bit Digital-to-Analog Formulas

Digital Value	Analog Equivalent	
when ADCRESULTy = 0	$\text{ADCINx} \leq \text{VREFLO}$	(15)
when 0 < ADCRESULTy < 4095	$\text{ADCINx} = (\text{VREFHI} - \text{VREFLO}) \left(\frac{\text{ADCRESULTy}}{4096} \right) + \text{VREFLO}$	(16)
when ADCRESULTy = 4095	$\text{ADCINx} \geq \text{VREFHI}$	(17)

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20.3 SOC Principle of Operation

The ADC conversion sequencing is accomplished through configurable start-of-conversions (SOCs). Each SOC is a configuration set defining the single conversion of a single channel. In that set, there are two configurations: the channel to convert and whether or not limit comparison is enabled. Upon receiving the start signal for an SOC, the wrapper makes sure that the specified channel is captured and the limit comparison is performed if enabled.

Multiple SOCs can be configured for the same channel as desired. Configuring multiple SOCs to use the same trigger allows the trigger to generate a sequence of conversions. Configuring multiple SOCs to use the same trigger and channel allows for oversampling.

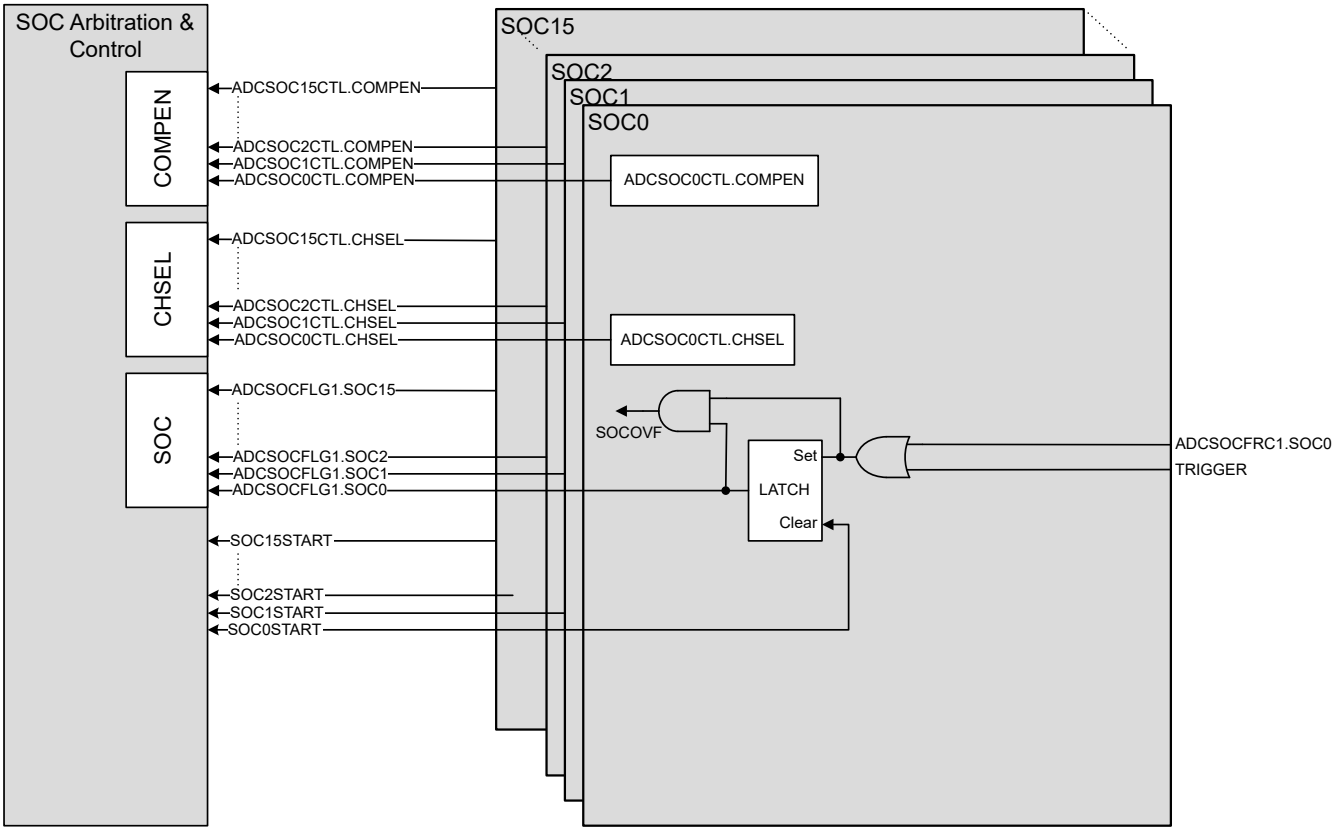


Figure 20-2. SOC Block Diagram

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20.3.1 ADC Sequencer

Sequencer Overview

The ADC supports up to four sequencers, which are used to sequence the order in which ADC channels are converted. Each sequencer is associated with multiple SOCs, and the number of SOCs within a sequencer is configured using the ADCSEQ{#}CONFIG.SEQSTART and ADCSEQ{#+1}CONFIG.SEQSTART-1 or ADCSEQCTL.SEQEND registers. Sequencers are enabled using the ADCSEQ{#}CONFIG.SEQENABLE register.

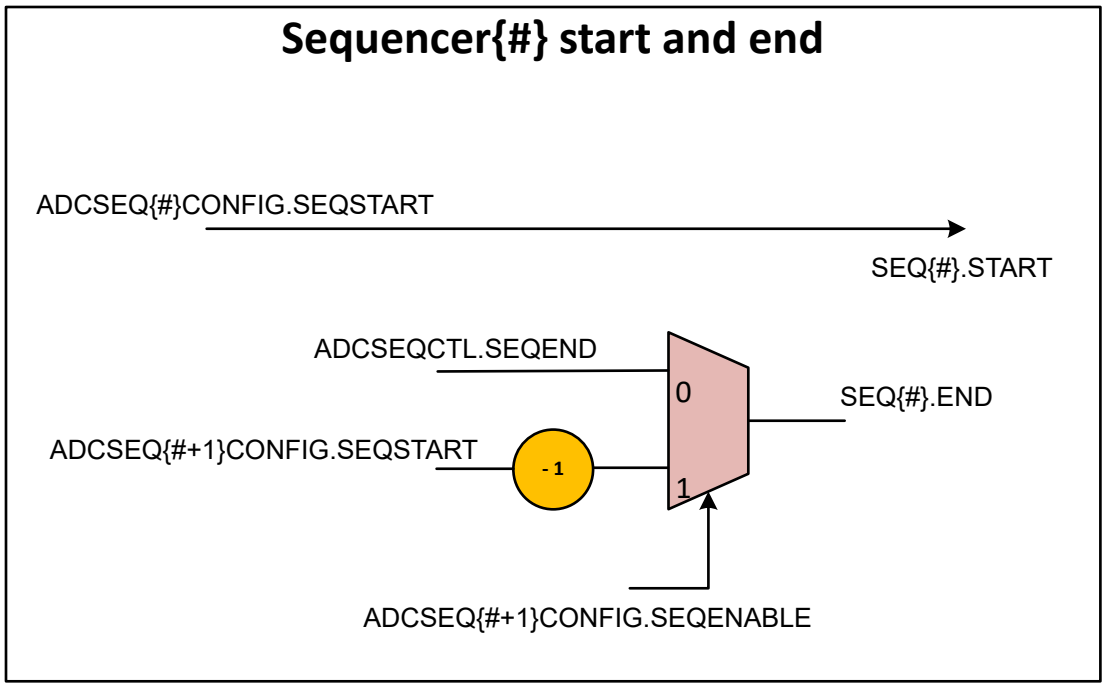


Figure 20-3. Sequencer start and end

Once a trigger is received for a sequencer and the ADC Wrapper is ready for arbitration, the sequencer starts converting in ascending order of SOCs. The first SOC in the sequence to convert is determined by ADCSEQ{#}CONFIG.SEQSTART, followed by subsequent SOCs until the end of the sequencer is reached.

Multiple sequencers can be configured to use the same trigger if desired. If multiple sequencers are triggered at the same time, the conversions within the sequence happens in the order of priority: SEQ1 followed by SEQ2, SEQ3, and SEQ4.

If a trigger for higher priority sequence occurs while a lower priority sequence is ongoing, the higher priority sequence can either be serviced as soon as the ongoing SOC conversion is complete or serviced after the lower priority sequence is complete. This can be configured using ADCSEQCTL.SEQPREEMPT register.

The ADCSEQCTL.SEQPREEMPT register configuration is as follows

- (2'b0x) Pre-empt disabled: The ongoing sequence fully completes before switching to higher priority sequence.
- (2'b10)Pre-empt enabled without restart of aborted SEQ : The ongoing sequence is discarded (after completing any ongoing conversion) and arbitration switches to higher priority sequence. The discarded/ aborted sequence is not be re-started after completing the higher priority sequence.
- (2'b11)Pre-empt enabled with restart of aborted SEQ: The ongoing sequence is discarded (after completing any ongoing conversion) and arbitration switches to the higher priority sequence. The discarded/aborted sequence is re-started from the beginning of the sequence after completing all higher priority sequences.

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Figure 20-4 illustrates the logical representation of sequencer{#} enable and overflow logic, which generates the overflow condition when the new trigger is received while a previous trigger is ongoing or pending.

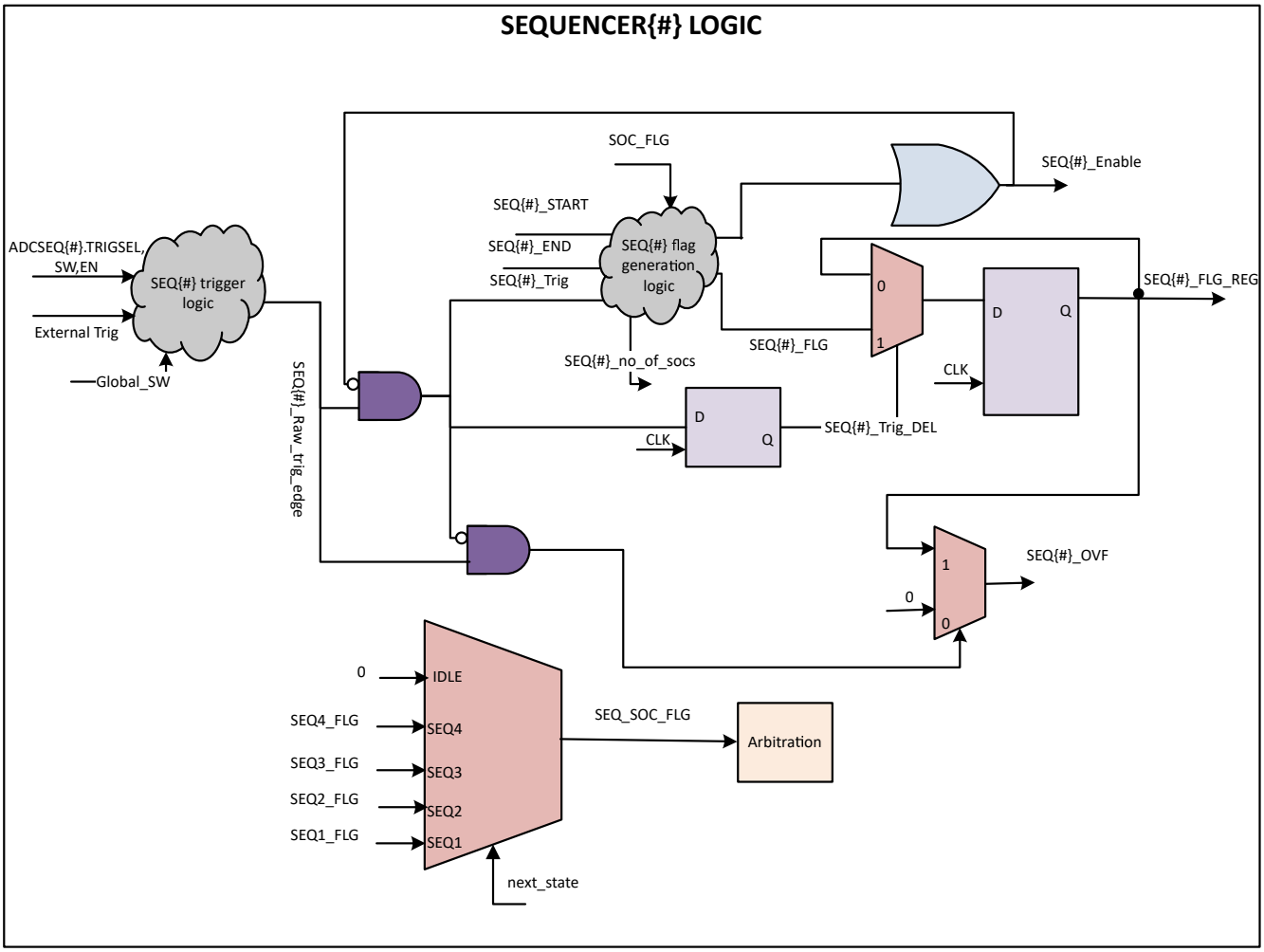


Figure 20-4. Sequencer Enable and Overflow Logic

Figure 20-5 illustrates the logical representation of sequencer{#} restart & discard logic.

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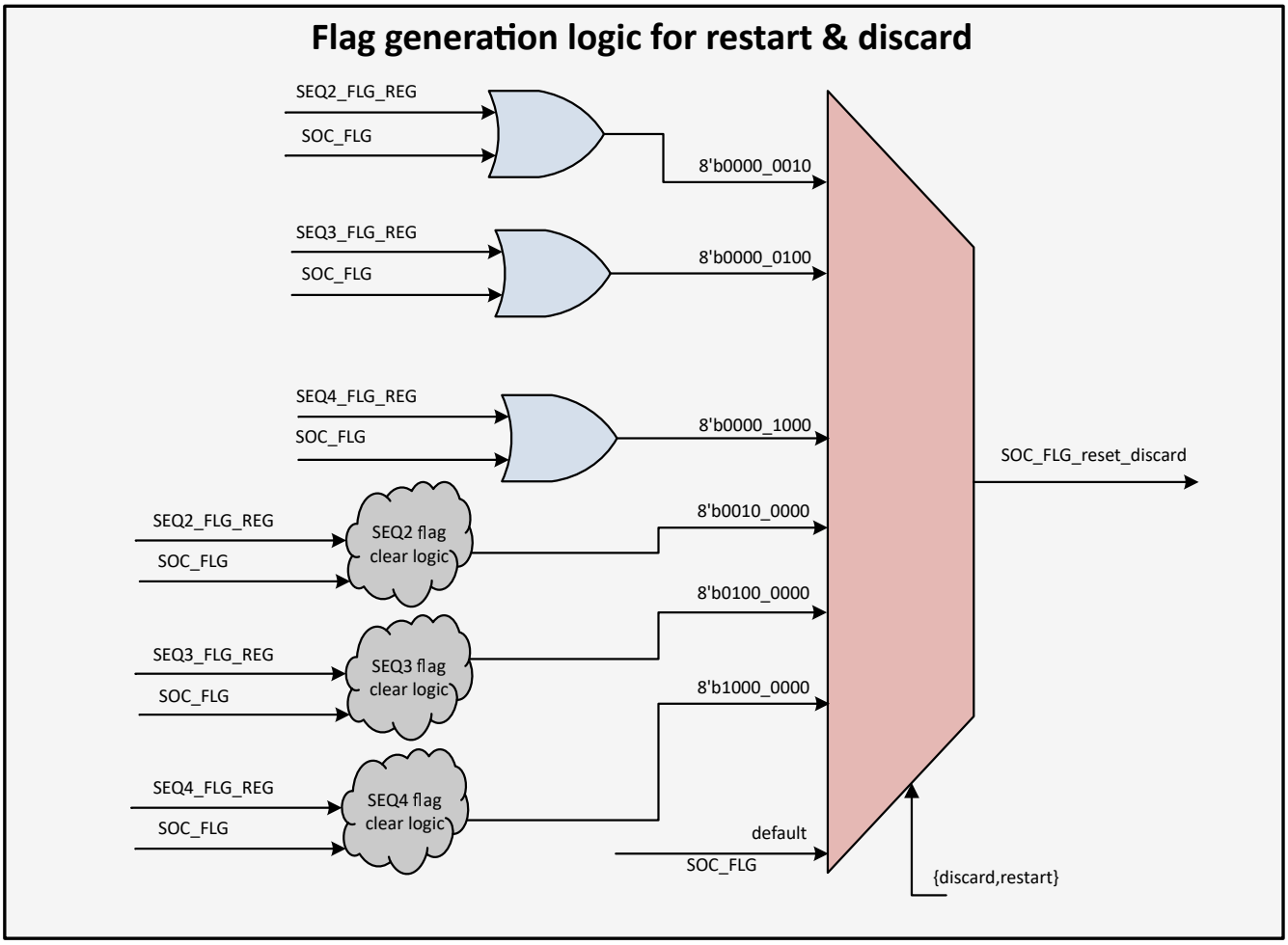


Figure 20-5. Sequencer Pre-empt Restart & Discard Logic

Additionally, oversampling and averaging can be enabled for the SOCs within the sequence using the Post Processing Blocking (PPB) averaging feature. Each sequencer is associated with the corresponding PPB block. PPB{#}LIMIT defines the number of samples per SOCs.

If oversampling is enabled, each SOC is sampled and converted ‘N’ times (N – total number of samples configured) before moving to the next SOC.

Each sequencer is associated with the corresponding ADCPPB{#}TRIPHI and ADCPPB{#}TRIPLO registers. This can be used to compare whether ADCRESULT is within the configured TRIPHI and TRIPLO limits or exceeded either of the limits.

Since the limit comparator settings are common across all SOCs within a Sequencer, limit comparison for a given SOC can be enabled or disabled using the ADCSOC{#}CTL.COMPEN field of the corresponding SOC.

20.3.2 SOC Configuration

Each SOC has a configuration register, ADCSOCxCTL. Within this register, SOCx can be configured for a specific trigger source, channel to convert, and acquisition (sample) window duration.

20.3.3 Trigger Operation

Each SOC can be configured to start on one of many input triggers. The primary trigger select for SEQx is in the ADCSEQxCONFIG.TRIGSEL register, which can select between:

- Disabled (Software only)
- GPIO: INPUTXBAR.OUT[5]

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- ADCSOCA, ADCSOCB, ADCSOCC, or ADCSOCD from each PWM module

In addition, each SOC can also be triggered when the ADCINT1 flag or ADCINT2 flag is set. This is achieved by configuring the ADCINTSOCSEL1 register (for SOC0 to SOC7) or the ADCINTSOCSEL2 register (for SOC8 to SOC15). This can be useful for creating continuous conversions.

Table 20-4. ADC SOC Trigger Selection

ADCSEQxCONFIG.TRIGSEL	Input Signal
0	ADC_SOFTWARE_TRIGGER
1	TIMG4.GEN_EVENT0
2	TIMG12.GEN_EVENT0
3	INPUTXBAR5
4	MCPWM0_SOCA
5	MCPWM0_SOCB
6	MCPWM0_SOCC
7	MCPWM0_SOCD
8	MCPWM1_SOCA
9	MCPWM1_SOCB
10	MCPWM1_SOCC
11	MCPWM1_SOCD
12	MCPWM2_SOCA
13	MCPWM2_SOCB
14	MCPWM2_SOCC
15	MCPWM2_SOCD
16	ADC0_INT1
17	ADC1_INT1
18	ADC2_INT1
19	EPWM0_SOCA
20	EPWM0_SOCB
21	EPWM1_SOCA
22	EPWM1_SOCB
23	EPWM2_SOCA
24	EPWM2_SOCB
25	EPWM3_SOCA
26	EPWM3_SOCB
27	EPWM4_SOCA
28	EPWM4_SOCB
29	EPWM5_SOCA
30	EPWM5_SOCB
31	Reserved

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20.3.3.1 Global Software Trigger

This ADC only supports a synchronous global software trigger through use of the INPUTXBAR5 signal. Synchronous global triggers allow the application to trigger SOCs on multiple ADC instances that are exactly simultaneous in time.

20.3.4 ADC Acquisition (Sample and Hold) Window

External signal sources vary in the ability to drive an analog signal quickly and effectively. To achieve rated resolution, the signal source needs to charge the sampling capacitor in the ADC core to within 0.5 LSBs of the signal voltage. The acquisition window is the amount of time the sampling capacitor is allowed to charge and is configurable per SEQx by the ADCSEQxCONFIG.ACQPS register.

ACQPS is a 8-bit register field that can be set to a value between 0 and 255. The 2 upper bits (ADCSEQxCONFIG.ACQPS[7:6]) configure the base duration and cycle prescalers. The base duration can be set to values of 0, 64, 192, or 448 with corresponding cycle prescalers of 1, 2, 4, and 16 respectively. The lower 6 bits (ADCSEQxCONFIG.ACQPS[5:0]) in the register field configure the additional cycles to be multiplied by the prescaler and added to the base duration.

- ACQPS[7:6] = 00: Acquisition Window = ACQPS[5:0] + 1 [MCLK cycles]
- ACQPS[7:6] = 01: Acquisition Window = 64 + ((ACQPS[5:0] + 1) × 2) [MCLK cycles]
- ACQPS[7:6] = 10: Acquisition Window = 192 + ((ACQPS[5:0] + 1) × 4) [MCLK cycles]
- ACQPS[7:6] = 11: Acquisition Window = 448 + ((ACQPS[5:0] + 1) × 16) [MCLK cycles]

- The acquisition window duration is based on the System Clock (MCLK), not the ADC clock (ADCCLK).
- The selected acquisition window duration must be at least as long as one ADCCLK cycle.
- The data sheet specifies a minimum acquisition window duration (in nanoseconds). The user is responsible for selecting an acquisition window duration that meets this requirement.

20.3.5 Sample Capacitor Reset

In certain systems where the ADC successively samples multiple signal sources, memory crosstalk can occur. Memory crosstalk is the tendency of the ADC conversion to be pulled towards the value of the previous conversion, due to inadequate acquisition/settling time. This happens because the ADC sample capacitor voltage starts near the previously converted voltage, then settles towards the newly applied voltage on the current channel. If the acquisition window is not long enough for the sample capacitor to settle, this can result in some sample error reflected in the ADC conversion.

The 12-bit ADC modules in this device include a sample capacitor reset feature to help mitigate memory crosstalk. When sample capacitor reset is enabled, after every conversion, the sampling capacitor voltage is reset to either the VREFLO or VREFHI/2 voltage, depending on the configuration of the ADCSEQxCONFIG.SAMPCAPRESETSEL bit. This reset takes an extra ADCCLK cycle to complete. The sample capacitor reset function is inactive by default for each SOC. If desired, the application can activate sample capacitor reset by writing 0 to the SAMPCAPRESETDISABLE bit in the ADCSOCxCTL register. When sample capacitor reset is active, overall ADC throughput is slightly decreased due to the extra ADCCLK cycle in the conversion period.

20.3.6 ADC Input Models

For single-ended operation, the ADC input characteristics for values in the single-ended input model (see Figure 20-6) can be found in the device data sheet.

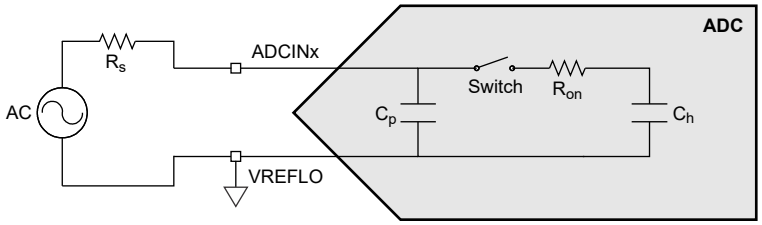


Figure 20-6. Single-Ended Input Model

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These input models must be used along with actual signal source impedance to determine the acquisition window duration. See *Choosing an Acquisition Window Duration* for more information.

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20.3.7 Channel Selection

Each SOC can be configured to convert any of the ADC channels. This behavior is selected for SOCx by the ADCSOCxCTL.CHSEL register. This is summarized in the table below. For the pin location of ADC inputs, refer to the device specific data sheet.

Table 20-5. Channel Selection of Input Pins

Input Mode	CHSEL	Input
Single-Ended	0	ADCIN0
	1	ADCIN1
	2	ADCIN2
	3	ADCIN3
	4	ADCIN4
	5	ADCIN5
	6	ADCIN6
	7	ADCIN7
	8	ADCIN8
	9	ADCIN9
	10	ADCIN10
	11	ADCIN11
	12	ADCIN12
	13	ADCIN13
	14	ADCIN14
	15	ADCIN15
	16	ADCIN16
	17	ADCIN17
	18	ADCIN18
	19	ADCIN19
	20	ADCIN20
	21	ADCIN21
	22	ADCIN22
	23	ADCIN23
	24	ADCIN24
	25	ADCIN25
	26	ADCIN26
	27	ADCIN27
	28	ADCIN28
	29	ADCIN29
	30	ADCIN30
	31	ADCIN31

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20.4 SOC Configuration Examples

The following sections provide some specific examples of how to configure the SOCs to produce some conversions.

20.4.1 Single Conversion from ePWM MCPWM Trigger

To configure ADCA to perform a single conversion on channel ADCIN1 when the ePWMMCPWM timer reaches the period match, a few things are necessary. First, ePWM3MCPWM3 must be configured to generate an SOCA or SOCB, SOCB, SOCC, or SOCD signal (in this statement, SOC refers to a signal in the ePWM module). See the *Enhanced Pulse Width Modulator Module (EPWM)* chapter on how to do this.MCPWM module). See the *Multi-Channel Pulse Width Modulator Module (MCPWM)* chapter on how to do this. Assume that SOCB was chosen.

SOC5 is chosen arbitrarily. Any of the 16 SOCs can be used.

Assuming a 100ns sample window is desired with a MCLK frequency of 200MHz, then the acquisition window duration must be 100ns/6.25ns = 16 cycles. The ACQPS field must be set to 0 in the upper two bits and 16 - 1 in the lower six bits (ACQPS[7:6] = 0, ACQPS[5:0]=15)..

```
AdcaRegs.ADCSEQxCONFIG.bit.CHSEL = 1;      //SEQx converts ADCINA1
AdcaRegs.ADCSEQxCONFIG.bit.ACQPS = 15;     //SEQx uses a sample duration of 16 MCLK cycles
(ACQPS[7:6]=0, ACQPS[5:0]=15)
AdcaRegs.ADCSEQxCONFIG.bit.TRIGSEL = 14;   //SEQx begins conversion on MCPWM3 SOCB
```

As configured, when ePWM3MCPWM3 matches the period and generates the SOCB signal, the ADC begins sampling channel ADCINA1 (SOC5) immediately if the ADC is idle. If the ADC is busy, ADCINA1 begins sampling when SOC5 gains priority. The ADC control logic samples ADCINA1 with the specified acquisition window width of 100ns. Immediately after the acquisition is complete, the ADC converts the voltage to a digital value. When the ADC conversion is complete, the results are available in the ADCRESULT5 register (see Section 20.11 for exact sample, conversion, and result latch timings).

20.4.2 Oversampled Conversion from ePWMMCPWM Trigger

Note

The device has four sequencers (SEQ1–SEQ4). The SOC-based oversampling pattern (chaining multiple SOCs to the same trigger) does not apply. Multiple SOCs can be configured with the same channel and trigger source using the ADCSEQxCONFIG registers, up to the number of available sequencers.

When ePWM3MCPWM3 matches the period and generates the SOCB signal, the ADC begins sampling channel ADCINA1 (SOC5) immediately if the ADC is idle. If the ADC is busy, ADCINA1 begins sampling when SOC5 gains priority. Once the conversion is complete for SOC5, SOC6 begins converting ADCINA1 and the results for SOC5 are placed in the ADCRESULT5 register. All four conversions eventually are completed sequentially, with the results in ADCRESULT5, ADCRESULT6, ADCRESULT7, and ADCRESULT8 for SOC5, SOC6, SOC7, and SOC8, respectively.

20.4.3 Software Triggering of SOCs

At any point, whether or not the SOCs have been configured to accept a specific trigger, a software trigger can set the SOCs to be converted. This is accomplished by writing bits in the ADCSOCFRC1 register.

Software triggering of the previous example without waiting for the CPU1 Timer 2 to generate the trigger can be accomplished by the statement:

```
AdcaRegs.ADCSOCFRC1.all = 0x000F;        //set SOC flags for SOC0 to SOC3
```


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20.5 EOC and Interrupt Operation

Each SOC has a corresponding end-of-conversion (EOC) signal. This EOC signal can be used to trigger an ADC interrupt. The ADC can be configured to generate the EOC pulse at either the end of the acquisition window or at the end of the voltage conversion. This is configured using the bit INTPULSEPOS in the ADCCTL1 register. See Section 20.11 for exact EOC pulse location.

An ADC module has 4 configurable ADC interrupts. These interrupts can be triggered by any of the 16 EOC signals. The flag bit for each ADCINT can be read directly to determine if the associated SOC is complete or the interrupt can be passed on to the NVIC.

It is also possible to generate an ADC interrupt based on a PPB oversampling logic event, such as when the sample count matches the configured limit. There are four oversampling interrupt (OSINT) flags available in each module for this purpose. Any of the ADCINT flags can be configured for an OSINT by configuring the INTxSEL field the corresponding ADCINTSELxNy register.

Note

The ADCCTL1.ADCBSY bit being clear does not indicate that all conversions in a set of SOCs have completed, only that the ADC is ready to process the next conversion. To determine if a sequence of SOCs is complete, link an ADCINT flag to the last SOC in the sequence and monitor that ADCINT flag.

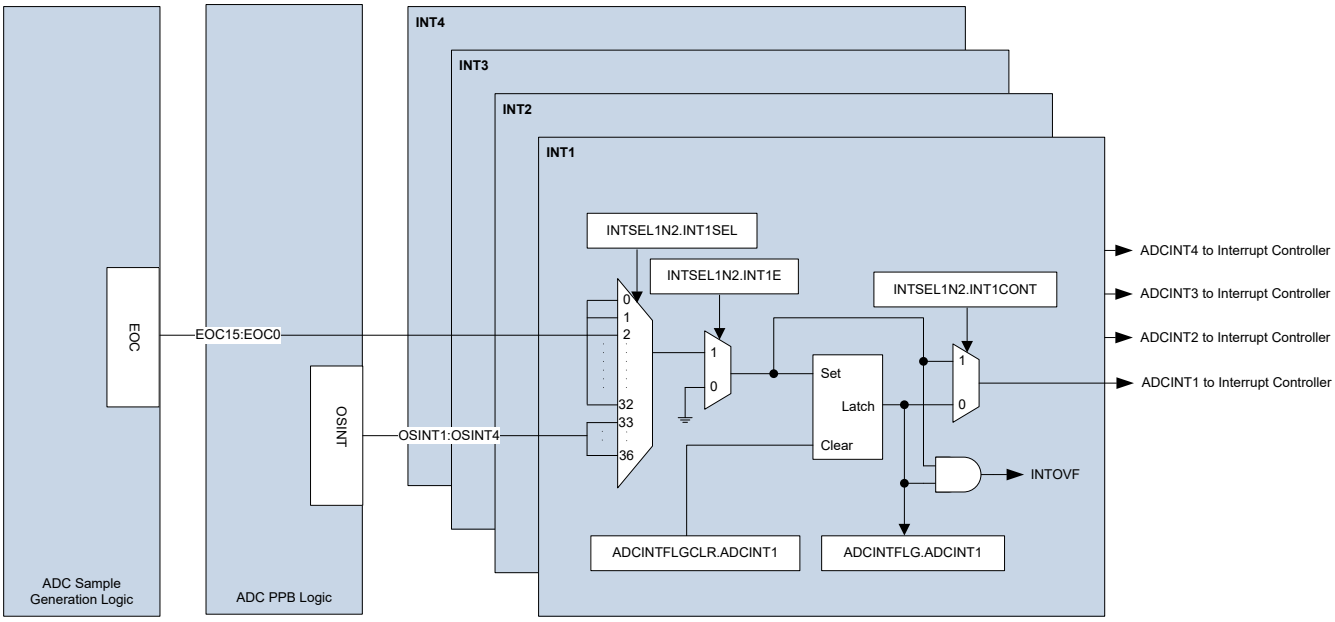


Figure 20-7. ADC End-of-Conversion (EOC) Signal Interrupts

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20.5.1 Interrupt Overflow

If the EOC signal sets a flag in the ADCINTFLG register, but that flag is already set, an interrupt overflow occurs. By default, overflow interrupts are not passed on to the NVIC module. When an overflow occurs on a given flag in the ADCINTFLG register, the corresponding flag in the ADCINTOVF register is set. This overflow flag is only used to detect that an overflow has occurred; the flag does not block further interrupts from propagating to the NVIC module.

When an ADC interrupt overflow occurs, the application must check the appropriate ADCINTOVF flag inside the ISR or in the background loop and take appropriate action when an overflow is detected.

20.5.2 Continue to Interrupt Mode

The INTxCONT bits in the ADCINTSEL1N2 register configures how interrupts are handled when an ADCINTFLG has not yet been cleared from a prior interrupt. This mode is disabled by default and additional overlapping interrupts are not issued to the NVIC. By activating this mode, ADC interrupts always reach the NVIC. If interrupts occur while ADCINTFLG is set, the ADCINTOVF register remains set regardless of the configuration of the INTxCONT bits.

20.5.3 Early Interrupt Configuration Mode

Enabling early interrupt mode can allow the application to enter the ADC interrupt service routine before the ADC results are ready. This allows the application to do any necessary pre-work so that the application can act on the ADC results immediately when the ADC results become available. If the timing of the early interrupt is too early, then the application needs to waste time until the updated ADC results become available. To prevent this situation, the time the ADC interrupt is entered in early interrupt mode is configurable by way of the DELAY field in the ADCINTCYCLE register.

- To use the configurable interrupt time, the ADC must be in early interrupt mode. To achieve this, clear the bit INTPULSEPOS to 0 in ADCCTL1.
- The DELAY value in the ADCINTCYCLE register sets the number of additional MCLK cycles after the falling edge of the SOC pulse before the ADCINT flag is set.
- If the value of DELAY goes beyond EOC, the ADC interrupt is generated along with EOC.
- Writing values to DELAY when INTPULSEPOS is set to 1 does not have any effect on the interrupt generation.

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20.6 Post-Processing Blocks

Each ADC module contains four post-processing blocks (PPB). These blocks can be associated with any of the available RESULT registers. The post-processing blocks have the ability to:

- Remove an offset associated with the ADCIN channel
- Flag a high or low compare limit, with the option to trip a PWM and generate an interrupt
- Record the delay between the associated SOC trigger and when sampling actually begins

Figure 20-8 presents the structure of each PPB. Subsequent sections explain the use of each submodule.

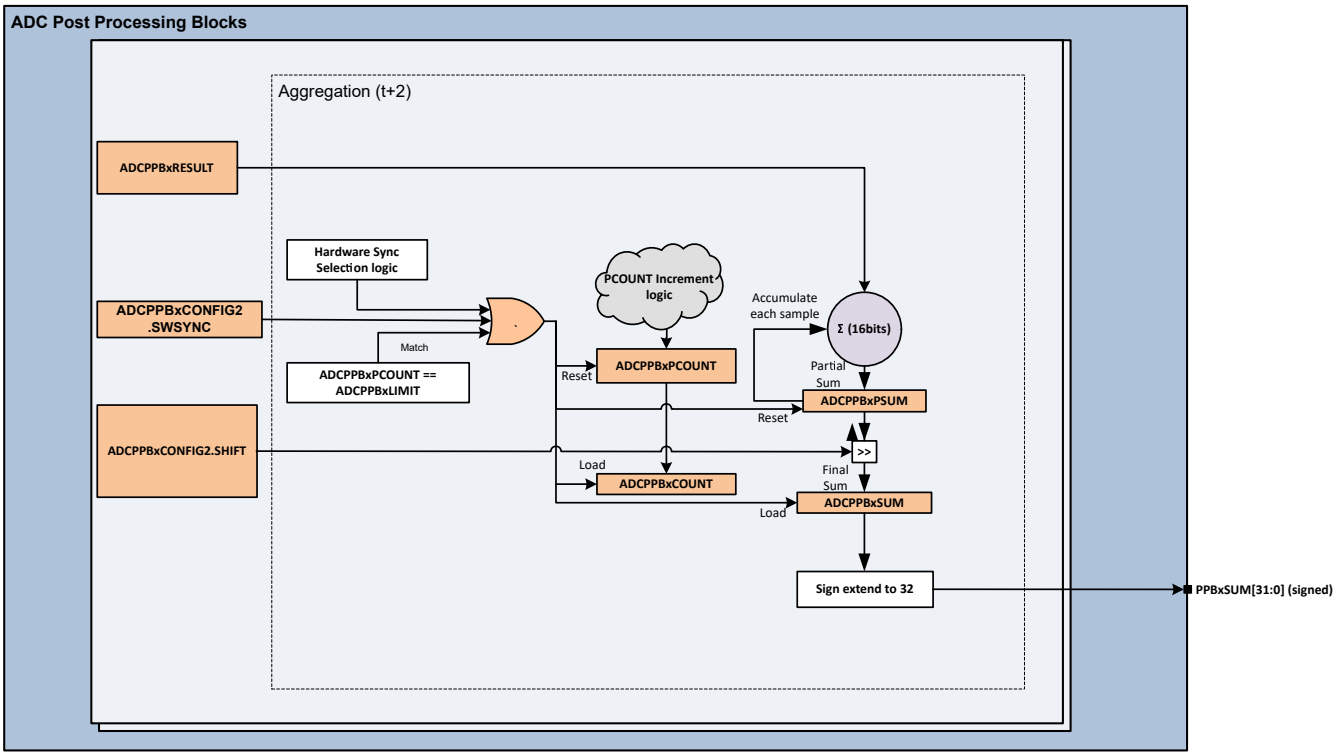


Figure 20-8. ADC Post-Processing Blocks (PPB) Block Diagram

20.6.1 PPB Oversampling

This ADC has built-in support for oversampling in the post-processing block. The oversampling support module exists at the output of the sample correction module, as shown in Figure 20-8. The oversampling module works by accumulating results in partial registers until either the sample count limit defined in the ADCPPBxLIMIT register is reached , an external hardware sync event occurs, or the software forces a sync event by writing to the SWSYNC bit in the ADCPPBxCONFIG2 register.

20.6.1.1 ADC - ADC Sync Input Selection

Table 20-6. ADC Sync Input Selection

ADCPPBxCONFIG2. SYNCINSEL	Input Signal
0	Disable
1	INPUTXBAROUT5
2	INPUTXBAROUT6
3	ECAP0_SYNCOUT
4	ECAP1_SYNCOUT
5	MCPWM0_SYNCPER
6	MCPWM1_SYNCPER

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Table 20-6. ADC Sync Input Selection (continued)

ADCPPBxCONFIG2. SYNCINSEL	Input Signal
7	MCPWM2_SYNCPER
8	Reserved
9	Reserved
10	ECAP2_SYNCOUT
11	EPWM0_SYNCPER
12	EPWM1_SYNCPER
13	EPWM2_SYNCPER
14	EPWM3_SYNCPER
15	EPWM4_SYNCPER
16	EPWM5_SYNCPER
17	ECAT_SYNC0
18	ECAT_SYNC1
19-31	Reserved

20.6.1.2 Accumulation and Average Functions

At the end of each ADC sample conversion, the PPB updates the partial result registers ADCPPBxPSUM with the newly processed conversion result from the ADCPPBxRESULT register, and the partial conversion count register (ADCPPBxPCOUNT) increments by 1. When the partial conversion count equals the limit defined in ADCPPBxLIMIT, or the PPB receives a software sync signal, the PPB takes the following actions:

1. The PPB loads the values of the respective partial result registers into the final result registers ADCPPBxSUM.
2. The PPB loads the partial count in ADCPPBxPCOUNT into the final conversion count register ADCPPBxCOUNT.
3. The partial count register and partial result registers reset to zero.

The PPB can also be configured to generate an oversampling interrupt when there is a hardware or software sync event. To trigger an OSINTx pulse when a sync event occurs, write 1 to the OSINTSEL bit in the ADCPPBxCONFIG2 register.

The PPB can automatically compute the average of the accumulated samples if ADCPPBxLIMIT is set to a power of 2 (x2/x4/x8 samples). To perform automatic averaging over 2^n samples, set the SHIFT field in the ADCPPBxCONFIG2 register to n. When this field is set, the PPB divides the value of ADCPPBxPSUM by 2^n before loading into ADCPPBxSUM.

To compute an average from the accumulated sum when the number of samples is not a power of 2, divide the value of ADCPPBxSUM by the value of ADCPPBxCOUNT using the CPU.

20.6.1.3 Outlier Rejection

The post-processing block enables the application to easily perform outlier rejection, by eliminating the largest and smallest samples during each SOC burst. To eliminate outliers, the following formula can be used in a software routine or ISR:

$$\text{Average} = \frac{(\text{ADCPPBxSUM} - \text{ADCPPBxMAX} - \text{ADCPPBxMIN})}{(\text{ADCPPBxCOUNT} - 2)} \quad (18)$$

20.7 ADC Results

The ADC_LITE_RESULT_REGS registers contain the conversion results and post-processed data from the ADC. Any initiator can read these registers independently without arbitration penalty, providing efficient access to ADC conversion data.

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ADCRESULT Register

The ADCRESULT register stores the conversion result per channel for each start of conversion (SOC). The register width is 12-bit and the data is represented as an unsigned integer.

Note

When oversampling is enabled in the sequencer, the HSADCRESULT register holds the final accumulated SUM instead of the single conversion result.

PPBRESULT Register

The PPBRESULT register stores the post-processed result from the post-processing block (PPB). Refer to Section 20.6 for detailed information on post-processing operations. The data is represented as a signed number with the most significant bit (MSB) indicating the sign.

PPBSUM Register

The PPBSUM register stores the final accumulated sum from the post-processing block (PPB). When SHIFT is enabled, this register stores the final result after accumulation and shift operation. The data is represented as a signed number. The register size depends on the ADC resolution and the number of samples that can be accumulated.

For a 12-bit ADC supporting up to 8x oversampling, a 16-bit register is sufficient to store the accumulated result

Table 20-7. Register Width Summary

Register	Register Bit Width
ADCRESULT	12-bit
PPBRESULT	13-bit
PPBSUM	16-bit (8x oversampling)

20.7.1 FIFO Operation

The ADC provides a dedicated first-in, first-out (FIFO) interface for sequential reading of conversion results from all start-of-conversion (SOC) events associated with each sequencer. In addition to the standard ADCRESULT, PPBRESULT, and PPBSUM registers, ADCRESULT and PPBSUM results are also mapped to a FIFO location per sequencer. The FIFO mechanism enables efficient batch reading of multiple conversion results without requiring individual register accesses for each SOC.

Overview

The ADC FIFO architecture provides one dedicated address location per sequencer for reading conversion results in sequential order. Each sequencer supports a single independent FIFO, allowing parallel result retrieval across multiple sequencers. The FIFO read interface simplifies firmware implementation by automatically advancing through results with each read operation, eliminating the need for manual result register indexing.

Register Descriptions

ADCSEQ{#}FIFORESULT Register

The`ADCSEQ{#}FIFORESULT`register provides the primary interface for reading ADC conversion results from the FIFO associated with sequencer {#} (where {#} ranges from 1 to 4). Each read operation from this register returns a 32-bit value containing conversion results for two consecutive SOCs. The lower 16 bits [15:0] contain the result from the first SOC in the pair. The upper 16 bits [31:16] contain the result from the second SOC in the pair.

The register automatically advances the internal FIFO read pointer with each access, enabling sequential retrieval of all results associated with the sequencer without additional pointer management.

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ADCSEQ{#}FIFOSTATUS Register

The ADCSEQ{#}FIFOSTATUS register provides status information for the FIFO associated with sequencer {#}. This register contains the following status fields:

- FIFO valid: Indicates whether valid conversion results are available in the FIFO for reading
- FIFO read pointer: Provides the current position within the FIFO, indicating which result pair the next read operation returns

Check the FIFO valid status field before reading from ADCSEQ{#}FIFORESULT to confirm that valid data is available.

FIFO Read Behavior

Each read from ADCSEQ{#}FIFORESULT returns a 32-bit value containing results for exactly 2 consecutive SOCs, formatted as: {SOC(N+1)RESULT[15:0], SOC(N)RESULT[15:0]} where SOC(N) and SOC(N+1) represent consecutive SOCs assigned to the sequencer.

Sequential reads from the same ADCSEQ{#}FIFORESULT register automatically advance through all SOCs associated with that sequencer. The FIFO read pointer increments after each access, and subsequent reads return the next pair of results in sequence.

Odd-SOC Edge Case

NOTE: If an odd number of SOCs are associated with a sequencer, the final FIFO read contains valid result data in the lower 16 bits [15:0] and padding zeros (16'h0) in the upper 16 bits [31:16]. The FIFO always returns results in pairs, and the final SOC has no subsequent SOC to pair with.

FIFO Operation Example

The following example demonstrates FIFO operation across all four sequencers with varying numbers of associated SOCs:

Sequencer Configuration	Read Number	FIFO Result Format {Upper[31:16], Lower[15:0]}
SEQ1: SOC0 to SOC5 (6 SOCs)	First Read	{SOC1RESULT, SOC0RESULT}
	Second Read	{SOC3RESULT, SOC2RESULT}
	Third Read	{SOC5RESULT, SOC4RESULT}
SEQ2: SOC6 to SOC8 (3 SOCs - Odd)	First Read	{SOC7RESULT, SOC6RESULT}
	Second Read	{16'h0, SOC8RESULT}
SEQ3: SOC9 to SOC10 (2 SOCs)	First Read	{SOC10RESULT, SOC9RESULT}
SEQ4: SOC11 to SOC15 (5 SOCs - Odd)	First Read	{SOC12RESULT, SOC11RESULT}
	Second Read	{SOC14RESULT, SOC13RESULT}
	Third Read	{16'h0, SOC15RESULT}

In this example, SEQ2 and SEQ4 demonstrate the odd-SOC edge case. SEQ2 has 3 SOCs (SOC6, SOC7, SOC8), resulting in two FIFO reads where the second read contains only SOC8RESULT with padding in the upper bits. Similarly, SEQ4 has 5 SOCs (SOC11 through SOC15), requiring three reads with the final read containing only SOC15RESULT and padding.

FIFO Access Sequence

To read all conversion results from a sequencer FIFO:

- Check the FIFO valid status field in ADCSEQ{#}FIFOSTATUS to confirm that results are available
- Read from ADCSEQ{#}FIFORESULT to retrieve the first result pair

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- Extract SOC(N)RESULT from bits [15:0] and SOC(N+1)RESULT from bits [31:16]
- Repeat steps 2 and 3 until all results for the sequencer have been read
- For sequencers with odd SOC counts, the final read has 16'h0 in bits [31:16]

The FIFO read pointer automatically manages sequencing, eliminating the need for firmware to track which SOC result pair each read returns.

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20.8 Opens/Shorts Detection Circuit (OSDETECT)

The opens/shorts detection circuit (OSDETECT) can be used to detect pin faults in the system. The circuit connects to the ADC input after the channel select multiplexer but before the S+H circuit as shown in Figure 20-9.

Note

- The divider resistance tolerances can vary widely; hence, this feature must not be used to check for conversion accuracy.
- See the data sheet for implementation and availability of analog input channels.
- Due to high drive impedance, a S+H duration much longer than the ADC minimum is needed.

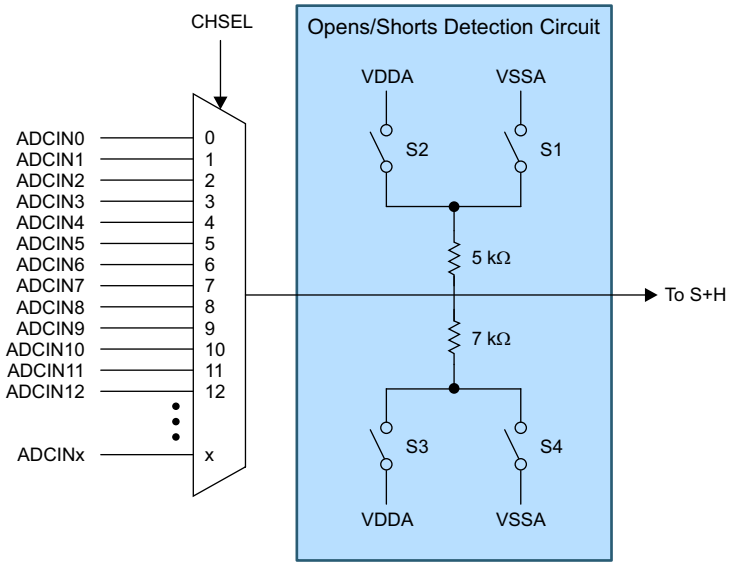


Figure 20-9. Opens/Shorts Detection Circuit

The circuit can be operated by writing a value to the DETECTCFG field in the ADCOSDETECT register. This causes the circuit to source a voltage onto the input during the S+H phase of any conversion. The voltage and drive strength of the OSDETECT circuit for different DETECTCFG settings is given in Table 20-8.

Table 20-8. DETECTCFG Settings

ADCOSDETECT. DETECTCFG	Source Voltage	S4	S3	S2	S1	Drive Impedance
0	Off	Open	Open	Open	Open	Open
1	Zero Scale	Closed	Open	Open	Closed	5K || 7K
2	Full Scale	Open	Closed	Closed	Open	5K || 7K
3	5/12 VDDA	Open	Closed	Open	Closed	5K || 7K
4	7/12 VDDA	Closed	Open	Closed	Open	5K || 7K
5	Zero Scale	Open	Open	Open	Closed	5K
6	Full Scale	Open	Open	Closed	Open	5K
7	Zero Scale	Closed	Open	Open	Open	7K

20.8.1 Open Short Detection Implementation

A representative circuit with the Open-short Detection (OSDETECT) implementation consists of the signal source with series resistance R_S, shunt capacitor C_P, the equivalent OSDETECT resistance $R_{OSDETECT}$ and

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voltage $V_{OSDETECT}$ is shown in Figure 20-10 and can be used as a basis to calculate the signal level going in to the sampling capacitor. $R_{OSDETECT}$ and $V_{OSDETECT}$ are the equivalent input resistance and voltage source contributed by the OSDETECT circuit with values shown in Table 20-8 for the different configuration settings. Refer to Figure 20-10 when deriving the input signal to S/H if signal source V_S is driving while the OSDETECT feature is enabled.

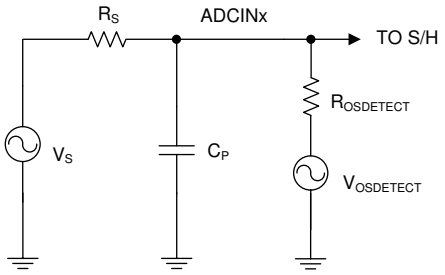


Figure 20-10. Input Circuit Equivalent with OSDETECT Enabled

The input impedance R_S and C_P are integral parts of the signal source or can have been implemented in the design to precondition the signal or to control signal settling time to meet S/H requirements. The input path has to be considered when using the OSDETECT feature, as this affects the conversion results. For instance, driving an input signal when this feature is enabled connects signal V_S to the OSDETECT circuit through R_S and affects the ADC results. Larger C_P values (in the order greater than hundreds of pF) require using higher ACQPS to make sure the signal at the input has settled prior to conversion.

To enable the circuit:

1. Configure the ADC for conversion (for example, channel, SOC, ACQPS, prescaler, trigger, and so on).
2. Set up the ADCOSDETECT register for the desired voltage divider connection as shown in Table 20-8.
3. Initiate a conversion and inspect the conversion result.

Interpret the results based on what is driving on the input side and what are the values of R_S and C_P. If the V_S signal can be disconnected from the input pin, the circuit can be used to detect open and shorted input pins as described in the following sections.

20.8.2 Detecting an Open Input Pin

By cycling through the various OSDETECT settings, the input signal is pulled towards the sourced voltages. An input with good drive strength (pin not open) is minimally affected. However, if the pin is open, the sampled voltages is close to the source voltages specified in Table 20-8.

20.8.3 Detecting a Shorted Input Pin

By cycling through the various OSDETECT settings, the input signal is pulled towards the sourced voltages. An input with finite drive strength (pin not shorted) is pulled toward each sourced voltage. However, if the pin is shorted, the signal remains at the same voltage.

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20.9 Power-Up Sequence

Upon device power-up or system level reset, the ADC is powered down and disabled. When powering up the ADC, the following sequence must be used:

1. Set the desired ADC clock divider in the PRESCALE field of ADCCTL2.
2. Power up the ADC by setting the ADCPWDNZ bit in ADCCTL1.
3. Allow a delay before sampling. See the data sheet for the necessary time.

Only one delay is necessary as long as the delay occurs after the ADC has begun powering up.

20.10 ADC Calibration

During the fabrication and test process, Texas Instruments calibrates the gain, offset, and linearity of the ADCs. These trim settings are stored in TI reserved OTP memory, and are loaded automatically by the boot ROM before application code executes.

- The boot ROM automatically executes the calibration routine before application code runs, copying factory ADC trim values from OTP memory to the ADCINLTRIM and ADCOFFTRIM registers. No explicit call to Device_cal() is required in the standard MCU+ SDK flow. For bare-metal applications that bypass the boot ROM, the OTP trim values must be manually copied to the ADC trim registers (ADCINLTRIM1–ADCINLTRIM4 and ADCOFFTRIM) before ADC operation. Refer to the MCU+ SDK for an example of manual trim register initialization.

Until the appropriate factory trim is loaded, the ADC and other analog modules are not specified to operate within the data sheet specifications. Similarly, if trim values other than the factory settings are placed into the trim registers, the ADC (and other modules) is not specified to operate within the data sheet specifications.

The boot ROM calls the calibration functions, so trim values are initially populated without user intervention. If trim registers are cleared by a module reset, the boot ROM calibration routine must be re-applied. In standard MCU+ SDK applications, a warm reset re-runs the boot ROM automatically. For bare-metal applications that bypass the boot ROM, manually re-copy the OTP trim values to the ADC trim registers after any reset that clears them.

20.11 ADC Timings

The process of converting an analog voltage to a digital value is broken down into an S+H phase and a conversion phase. The ADC sample and hold circuits (S+H) are clocked by MCLK while the ADC conversion process is clocked by ADCCLK. ADCCLK is generated by dividing down MCLK based on the PRESCALE field in the ADCCTL2 register.

The S+H duration is the value of the ACQPS field of the SOC being converted, plus one, times the MCLK period. The user must make sure that this duration exceeds both 1 ADCCLK period and the minimum S+H duration specified in the data sheet. The conversion time is approximately 10.5 ADCCLK cycles. See the timing diagrams and tables in Section 20.11.1 for exact timings.

20.11.1 ADC Timing Diagrams

The diagrams below show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the NVIC module).

Table 20-9. ADC Timing Parameter Descriptions

Parameter	Description
t_{SH}	The duration of the S+H window.

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Table 20-9. ADC Timing Parameter Descriptions (continued)

Parameter	Description
	At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) MCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. **Note:** The value on the S+H capacitor is captured approximately 5ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned.
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET MCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR when the sample is ready. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read).
t_{DMA}	The time from the end of the S+H window until a DMA read of the ADC conversion result is triggered.

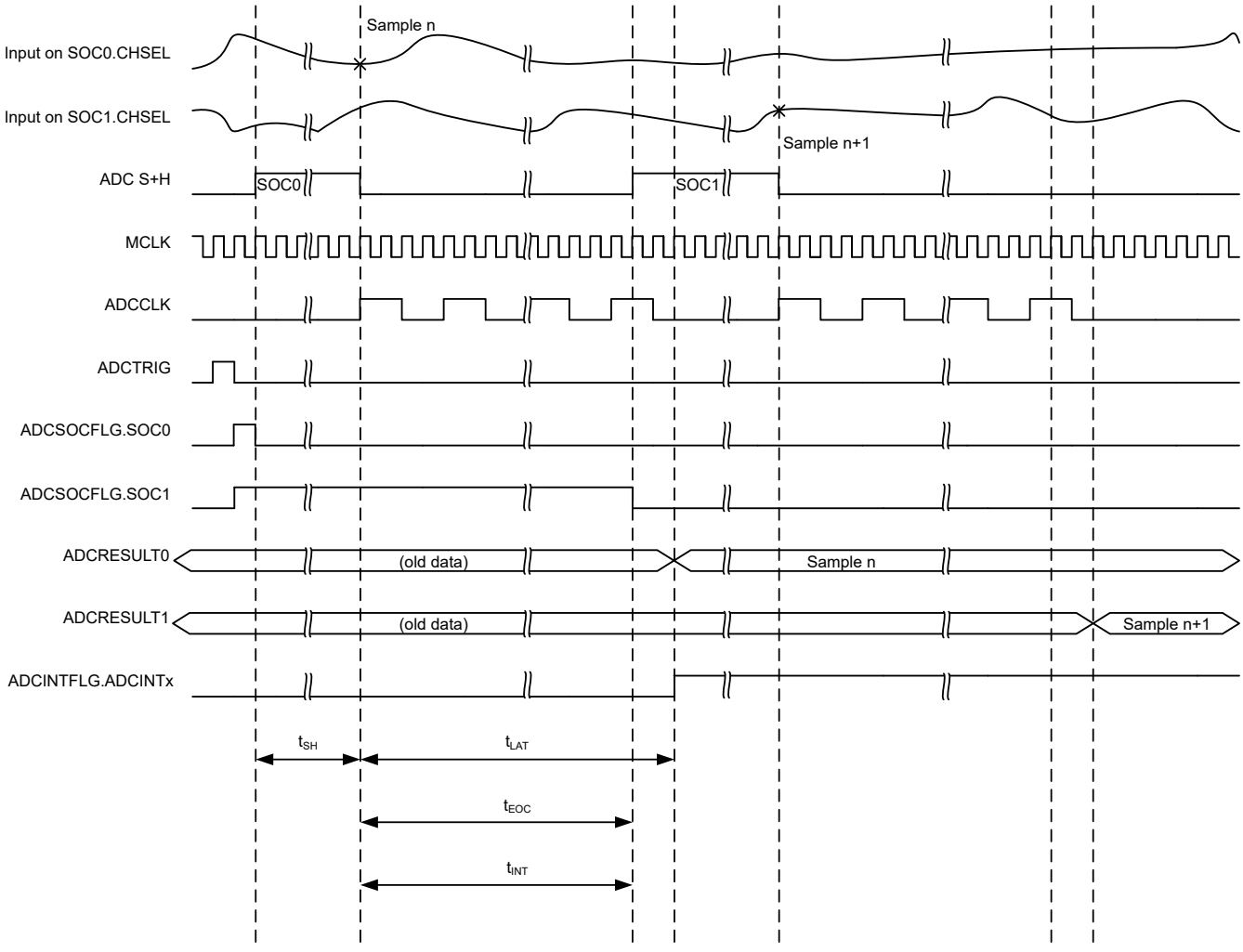


Figure 20-11. ADC Timings for 12-bit Mode in Early Interrupt Mode

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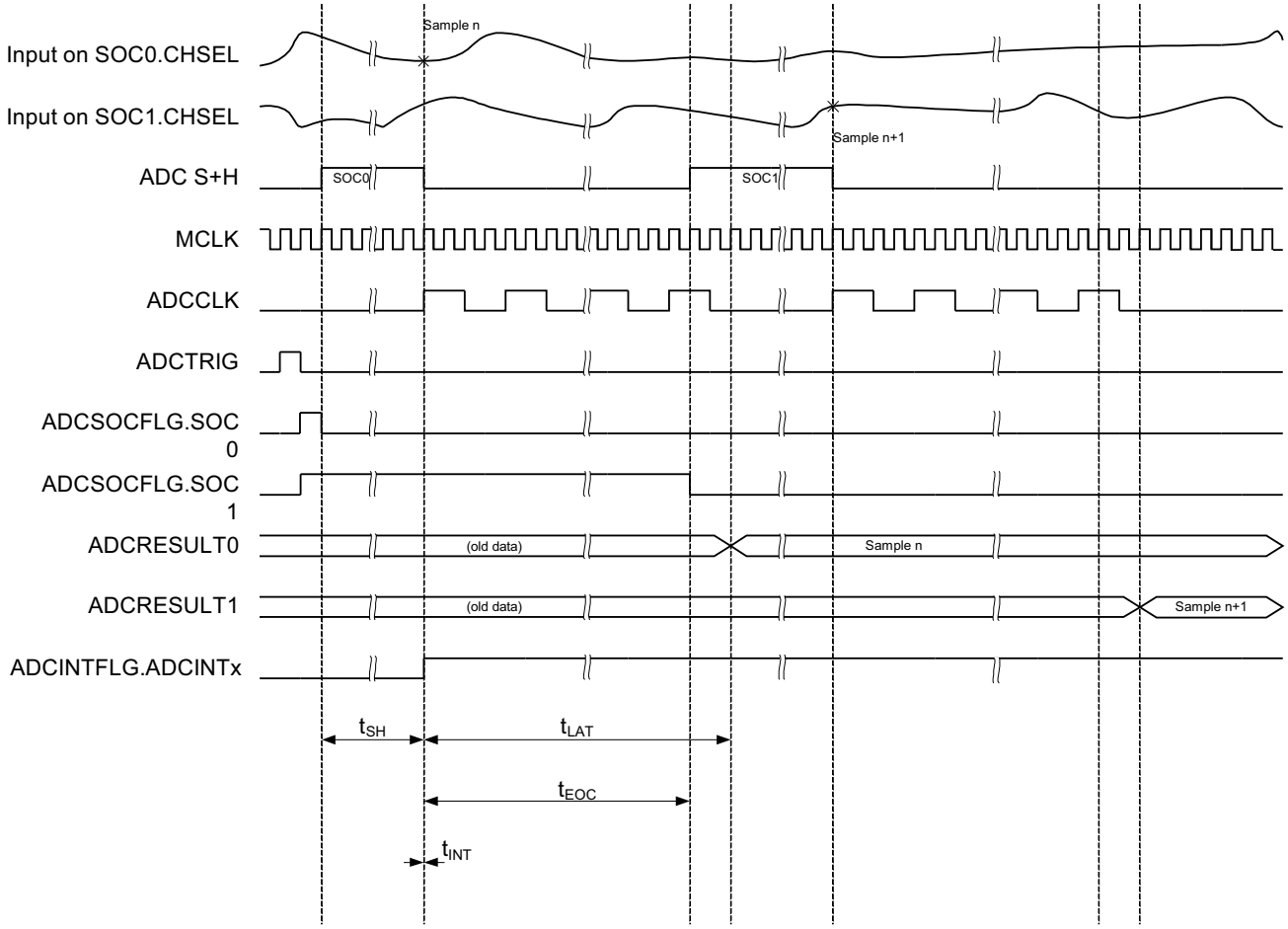


Figure 20-12. ADC Timings for 12-bit Mode in Late Interrupt Mode

Table 20-10. ADC Timings with SAMPCAPRESETSEL = 0

ADCCLK Prescale		MCLK Cycles				
ADCCTL2.PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)	t_{INT} (Late)	t_{DMA}
0	1	12	16	1	12	16
2	2	24	28	1	24	28
4	3	36	40	1	36	40
6	4	48	52	1	48	52
8	5	60	64	1	60	64
10	6	72	76	1	72	76
12	7	84	88	1	84	88
14	8	96	100	1	96	100

Table 20-11. ADC Timings with SAMPCAPRESETSEL = 1

ADCCLK Prescale		MCLK Cycles				
ADCCTL2.PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)	t_{INT} (Late)	t_{DMA}
0	1	11	15	1	11	15
2	2	22	26	1	22	26
4	3	33	37	1	22	37

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Table 20-11. ADC Timings with SAMPCAPRESETSEL = 1 (continued)

ADCCLK Prescale		MCLK Cycles				
ADCCTL2. PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)	t_{INT} (Late)	t_{DMA}
6	4	44	48	1	44	48
8	5	55	59	1	55	59
10	6	66	70	1	66	70
12	7	77	81	1	77	81
14	8	88	92	1	88	92

Note

It is recommended only to configure whole numbered integer prescalers in ADCCTL2.PRESCALE.

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20.11.2 Post-Processing Block Timings

The value of ADCRESULT is always available at time t_{LAT}, as specified in Section 20.11.1 . The value of ADCPPBxRESULT, and the limit and zero-crossing comparisons are available 1 MCLK cycle later, as long as multiple PPB instances do not point to the same SOC. Table 20-12 shows PPB result availability timings when there are no SOCs shared between multiple PPBs. In cases where multiple PPBs point to the same SOC, PPB results become available sequentially, starting with the lowest numbered PPB. The first ADCPPBxRESULT becomes available 1 MCLK cycle after t_{LAT}, and each subsequent ADCPPBxRESULT becomes available 1 MCLK cycle after the previous PPB has completed the limit, in-line, and zero-crossing comparison. The serialized PPB results are therefore spaced 2 or 3 MCLK cycles apart, depending on whether the comparison uses ADCPPBxRESULT or PSUM/SUM respectively. This timing is as shown in Table 20-13. PPB aggregation values (PSUM, SUM, PCOUNT, COUNT) are available 1 cycle after the associated ADCPPBxRESULT becomes available.

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Table 20-12. PPB Result Timings (One PPB per SOC)

Register	Description	Results Available
ADCRESULTy	ADC result	t_{LAT}
ADCPPBxRESULT	PPB result	t_{LAT} + 1 MCLK
ADCPPBxPSUM	Oversampling partial sum	t_{LAT} + 2 MCLK
ADCPPBxSUM	Oversampling sum	t_{LAT} + 2 MCLK
ADCPPBxPCOUNT	Oversampling partial sample count	t_{LAT} + 2 MCLK
ADCPPBxCOUNT	Oversampling sample count	t_{LAT} + 2 MCLK
Comparison	Limit and zero-crossing comparison (if using PPBxRESULT)	t_{LAT} + 2 MCLK
Comparison	Limit and zero-crossing comparison (if using PSUM or SUM)	t_{LAT} + 3 MCLK

Table 20-13. PPB Result Timings (Multiple PPBs Configured to Same SOC)

Register	Description	Results Available
ADCRESULTy	ADC result	t_{LAT}
ADCPPBxRESULT	PPB result	Varies (PPBs process serially)
ADCPPBxPSUM	Oversampling partial sum	ADCPPBxRESULT+ 1 MCLK
ADCPPBxSUM	Oversampling sum	ADCPPBxRESULT+ 1 MCLK
ADCPPBxPSUM	Oversampling partial sum	ADCPPBxRESULT+ 1 MCLK
ADCPPBxSUM	Oversampling sum	ADCPPBxRESULT+ 1 MCLK
Comparison	Limit and zero-crossing comparison (if using PPBxRESULT)	t_{LAT} + 2 MCLK
Comparison	Limit and zero-crossing comparison (if using PSUM or SUM)	t_{LAT} + 3 MCLK

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20.12 Additional Information

The following sections contain additional practical information.

20.12.1 Ensuring Synchronous Operation

For best performance, all ADCs on the device must be operated synchronously. The device data sheet specifies the performance in both synchronous and asynchronous mode for those parameters which differ between the modes of operation.

To make sure of synchronous operation, all ADCs on the device must operate in lockstep. This is accomplished by writing configurations to all ADCs that cause the sampling and conversion phases of all ADCs to be exactly aligned. The easiest way to accomplish this is to write identical values to the SOC configurations for each ADC for trigger select and ACQPS (S+H duration). In addition, synchronous ADCs must also configure identical values for the SOC priority control.

On some products, ADC types can be combined on the device for versatility. Synchronous operation can be restricted when operating different ADC types simultaneously. Consult the device data sheet, if there are restrictions on simultaneous operation of ADCs of different types to understand if ADC performance is impacted.

20.12.1.1 Basic Synchronous Operation

The following example configures two SOCs each on ADCA and with identical trigger select and ACQPS values. This results in synchronous operation between ADCA and . For devices with more than two ADCs, the same principles can be used to synchronize all the ADCs.

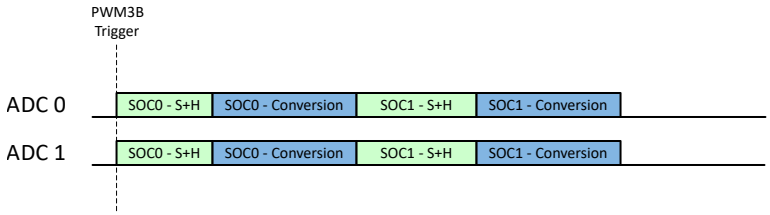


Figure 20-13. Example: Basic Synchronous Operation

Several things can be noted from the details above. First, while the ACQPS values must be the same for SOCs with the same number, different ACQPS values can be used for SOCs with different numbers. Because of this, synchronous operation does not require one global S+H time, but instead only channels sampled simultaneously require identical S+H durations. Another important point from this example is that any channel select value can be used for any SOC. If high-priority SOCs are to be used, the priority must be configured the same on all ADCs.

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20.12.1.2 Synchronous Operation with Multiple Trigger Sources

As long as each set of SOCs has identical trigger select and ACQPS settings, multiple trigger sources can be used while still achieving synchronous operation.

The following example demonstrates synchronous operation between ADCA and ADCB while using three SOCs and two trigger sources. Figure 20-14 demonstrates that any combination of relative trigger timings still results in synchronous operation.

Note

In the diagram below:

- ADC0 and ADC1 can be any two ADC[0:x]
- CPU Timer can be any TIMER_G4/G12[0:x]
- PWM3 SOCB can be any PWM[0:x]_SOCB

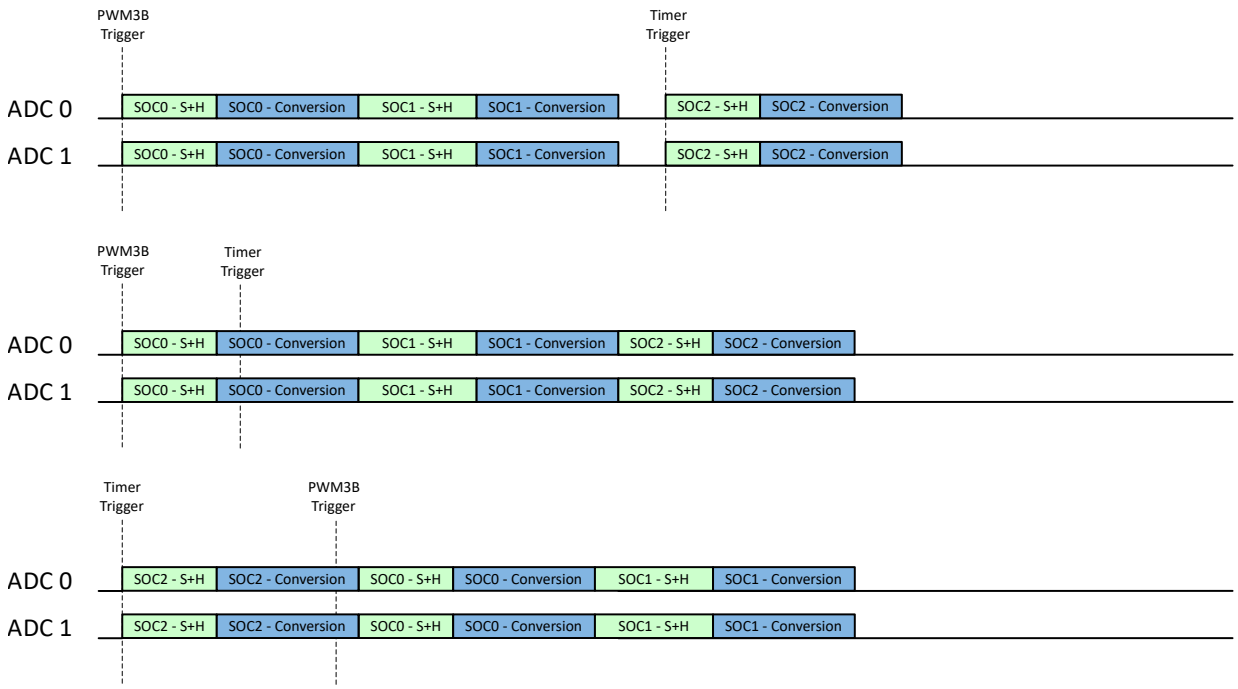


Figure 20-14. Example: Synchronous Operation with Multiple Trigger Sources

Note that any trigger source that can be selected in the TRIGSEL field can be used except for software triggering. There is no way to issue the software triggers for all ADCs simultaneously, so this results in asynchronous operation. ADCINT1 or ADCINT2 can also be used as a trigger when the ADCINTSOCSEL1 and ADCINTSOCSEL2 registers are configured identically for all ADCs and software triggering is not used to start the chain of conversions.

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20.12.1.3 Synchronous Operation with Uneven SOC Numbers

If only one trigger source is used, one ADC can use more SOCs than the other ADCs while still operating synchronously.

Note

In the diagrams below:

- ADCA and ADCB can be any two ADC[0:x]
- CPU Timer can be any RTI[0:x]
- PWM3 SOCB can be any PWM[0:x]_SOCB

Figure 20-15. Example: Synchronous Operation with Uneven SOC Numbers

Note that if the trigger comes again before all SOCs have completed the conversions, ADCB begins converting immediately on SOC0 while ADCA does not start converting SOC0 again until SOC2 is complete. This results in asynchronous operation, so care must be taken to not overflow the trigger.

Figure 20-16. Example: Asynchronous Operation with Uneven SOC Numbers – Trigger Overflow

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20.12.1.4 Non-overlapping Conversions

If conversion timings can be made sure to not overlap by the user, then all the SOCs on all ADCs do not have to be identically configured to achieve performance equivalent to synchronous operation. For example, if the two ADC triggers in a system come from two PWM sources that are always 180-degrees out-of-phase, then SOC0 can be used for both ADCA and ADCB with different trigger sources and different ACQPS values.

Note

In the diagram below:

- ADCA and ADCB can be any two ADC[0:x]
- CPU Timer can be any RTI[0:x]
- PWM3 SOCA can be any PWM[0:x]_SOCA
- PWM3 SOCB can be any PWM[0:x]_SOCB

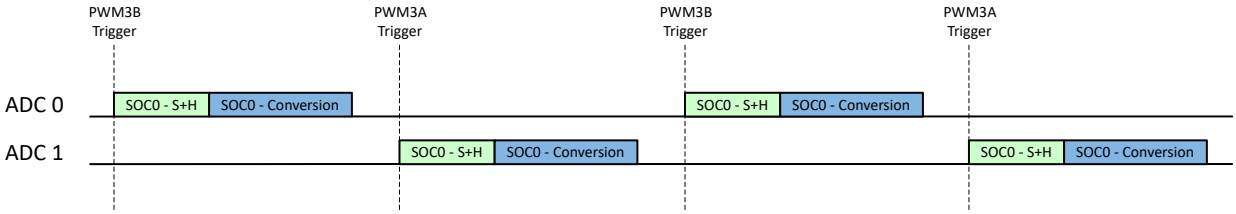


Figure 20-17. Example: Synchronous Equivalent Operation with Non-Overlapping Conversions

20.12.2 Choosing an Acquisition Window Duration

For correct operation, the input signal to the ADC must be allowed adequate time to charge the sample and hold capacitor, Ch. Typically, the S+H duration is chosen such that the sampling capacitor is charged to within ½ LSB or ¼ LSB of the final value, depending on the tolerable settling error.

The best methodology to determine the required settling time is to simulate the ADC and ADC driving circuits to make sure adequate settling performance. See *ADC Input Circuit Evaluation for C2000 MCUs* and *Charge-Sharing Driving Circuits for C2000 ADCs* for additional guidance on ADC signal conditioning circuit design and evaluation.

An approximation of the required settling time can also be determined using an RC settling model. The time constant for the model is given by the equation:

$$\tau = (R_S + R_{on}) \times C_h + R_S \times \left(C_S + C_p\right) \tag{19}$$

And the number of time constants needed is given by the equation:

$$k = ln\left(\frac{2^n}{settling\ error}\right) - ln\left(\frac{C_S + C_P}{CH}\right) \tag{20}$$

So the total S+H time must be set to at least:

$$t = k \cdot \tau \tag{21}$$

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Where the following parameters are provided by the ADC input model in the device data sheet:

- n = ADC resolution (in bits)
- R_{ON} = ADC sampling switch resistance (provided in Ω)
- C_H = ADC sampling capacitor (provided in pF)
- C_p = ADC channel parasitic input capacitance (provided in pF)

And the following parameters are dependent on the application design:

- settling error = tolerable settling error (in LSBs)
- R_s = ADC driving circuit source impedance (typically in Ω or kΩ)
- C_S = capacitance on ADC input pin (typically in pF or nF)

For example, assuming the following parameters:

- n = 12-bits
- R_{ON} = 500Ω
- C_H = 12.5pF
- C_p = 12.7pF
- settling error = ¼ LSB
- R_s = 180Ω
- C_s = 150pF

The time constant is calculated as:

$$\tau = (180\Omega + 500\Omega) \times 12.5pF + 180\Omega \times (150pF + 12.7pF) = 37.8ns \quad (22)$$

And the number of required time constants is:

$$k = ln\left(\frac{2^{12}}{0.25}\right) - ln\left(\frac{150pF + 12.7pF}{12.5pF}\right) = 9.70 - 2.57 = 7.13 \quad (23)$$

So the S+H time must be set to at least: 37.8ns × 7.13 = 270ns

If MCLK = 160MHz , then each MCLK cycle is 6.25ns. S+H duration is 270ns/6.25ns = 43.2 MCLK cycles, so ACQPS for this input is set to at least CEILING(43.2) – 1 = 42.

While this gives a rough estimate of the required acquisition window, a better method is to setup a circuit with the ADC input model, a model of the source impedance/capacitance, and any board parasitics in SPICE (or similar software) and simulate to verify that the sampling capacitor settles to the desired accuracy.

Note

The device data sheet specifies a minimum ADC S+H window duration. Do not use an ACQPS value that gives a duration less than this specification.

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20.12.3 Achieving Simultaneous Sampling

While each ADC does not have dual S+H circuits, achieving simultaneous sampling is accomplished by setting the SOC triggers on two or more ADC modules to use the same trigger source. The following example demonstrates simultaneous sampling on 3 ADCs based on the MCPWM3 event. A0_3 and A2_5 are sampled. An acquisition window of 20 MCLK cycles is used, but different durations are possible.

```
AdcORegs.ADCSOCOCTL.bit.CHSEL = 3;        //SOC0 converts ADC0 Channel 3
AdcORegs.ADCSOCOCTL.bit.ACQPS = 19;       //SOC0 uses sample duration of 20 MCLK cycles
AdcORegs.ADCSOCOCTL.bit.TRIGSEL = 10;     //SOC0 begins conversion on MCPWM3 SOCB
Adc2Regs.ADCSOCOCTL.bit.CHSEL = 5;        //SOC0 converts ADC2 Channel 5
Adc2Regs.ADCSOCOCTL.bit.ACQPS = 19;       //SOC0 uses sample duration of 20 MCLK cycles
Adc2Regs.ADCSOCOCTL.bit.TRIGSEL = 10;     //SOC0 begins conversion on MCPWM3 SOCB
```

When the MCPWM3 trigger is received, all 3 ADCs begin converting in parallel immediately. All results are stored in the ADCRESULT0 register for each ADC. Note that this assumes that all ADCs are idle when the trigger is received. If one or more ADCs is busy, the samples do not happen at exactly the same time.

20.12.4 Result Register Mapping

The ADC results and the ADC PPB results are duplicated for each memory bus controller in the system. Bus controllers include all CPUs, DMAs, and CLAs present on the specific part family and part number. For each bus controller, no access configuration is needed to allow read access to the result registers, and no contention occurs in cases where multiple bus controllers try to read the ADC results simultaneously.

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20.12.5 Internal Temperature Sensor

The internal temperature sensor measures the junction temperature of the device. The output of the sensor can be sampled with the ADC through an internal connection. This can be enabled on channel A0_13 on ADC0 or A2_13 on ADC2 and on the CMP0_HP5 input by setting the ENABLE bit in the TSNSCTL register.

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20.12.6 Designing an External Reference Circuit

Figure 20-18 shows the basic organization of the external voltage reference generation circuitry. For best performance, the externally generated reference voltage must be buffered by a precision op-amp with good bandwidth and low output impedance before being driven into the ADC reference pin. A capacitor between the high and low reference pins must be placed on the PCB as close to the pins as practical to help absorb high-frequency currents. A series resistor (typically <1Ω) in series with this capacitor is sometimes necessary to maintain op-amp stability.

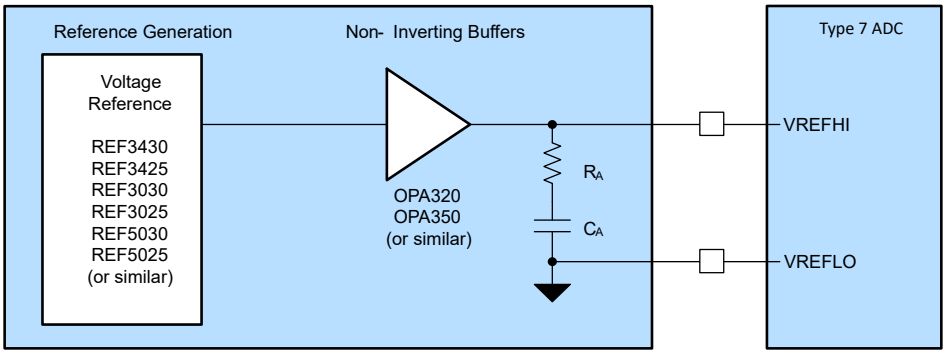


Figure 20-18. ADC Reference System

20.12.7 ADC-DAC Loopback Testing

For system diagnostic or functional safety purposes, the user application can perform a loopback test of the ADC module to verify that the ADC is converting correctly. Using the output of the DAC in the first CMPSS module, the device can be configured to supply a series of known voltages to the input of the converter, and the conversion result verified against expected results. Loopback test mode is enabled by setting the bit corresponding to the ADC module under test in the ADCLOOPBACK register in the analog subsystem module to 1. Figure 20-19 shows the connection between the CMPSS DAC output and the ADC.

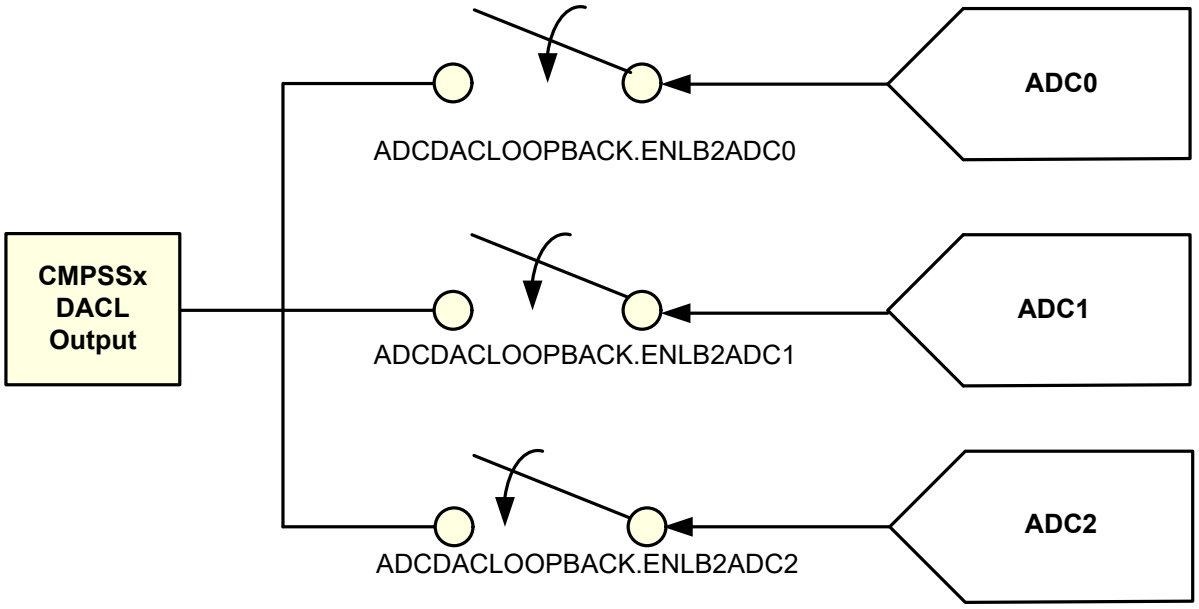


Figure 20-19. CMPSS to ADC Loopback Connection

In ADC loopback test mode, the following special considerations apply:

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- The ADC module always samples the CMPSS1 DACL output, regardless of what channel is selected in the ADCSOCxCTL.CHSEL field.
- The minimum sampling window size (ACQPS) when converting the DAC output is 2.5µs (512 MCLK cycles at 200MHz MCLK).
- The output resolution of the CMPSS DAC is 6 bits. The lower 6 bits of the input DACVAL are discarded.
- ADC loopback test mode affects CMPSS trip voltages. Avoid enabling ADC loopback mode during regular CMPSS operation.

For more information on the CMPSS module and how to configure the CMPSS DAC, see the *Comparator Subsystem (CMPSS)* chapter.

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20.12.8 Internal Test Mode

For diagnostic purposes, the ADC can sample various internal node voltages using a special input selection mux called INTERNALTEST. The INTERNALTEST mux can be sampled on the ADCIN20 input channel of any of the ADC modules. Internal test mode can be used to sample the VDDCORE voltage, VREFLO, VDDA, VSSA, and the CMPSS DAC outputs.

To enable internal test mode, write the desired node selection to the TESTSEL field of the INTERNALTESTCTL analog subsystem register. For details of internal test mux connections to various internal device voltage nodes, refer to the INTERNALTESTCTL register description.

To disable internal test mode, write 0 to the TESTSEL field of the INTERNALTESTCTL register.

When using internal test mode, the following special considerations apply:

- The minimum sampling window size (ACQPS) when converting INTERNALTEST is 2.56µs (512 MCLK cycles at 200MHz MCLK).
- The effective resolution of the CMPSS DAC outputs to INTERNALTEST is 6 bits.

For more information on the CMPSS module and how to configure the CMPSS DAC, see the *Comparator Subsystem (CMPSS)* chapter.

20.12.9 ADC Gain and Offset Calibration

Using a dedicated input channel, gain balancing between multiple ADCs can be performed. By calculating the relative gain error between the ADCs, conversion results can be post-processed in software such that each ADC has the same output for each equivalent input.

To perform gain calibration, configure the ADC SOC to sample channel ADCIN20. On this channel, the voltage sampled by all ADCs when triggered is (VREFHI × 0.9).

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20.12.10 ADC Zero Offset Calibration

ADC offset error is determined and calibrated during factory testing. However, the user still has the option to perform offset calibration if the end application specifically requires this. This section describes how to perform offset calibration using the VREFLO connection (see your device DS for the ADC channel connection to VREFLO) for single-ended operation.

Zero offset error is defined as the difference from 0 that occurs when converting a voltage at VREFLO. The zero offset error can be positive or negative. To correct this error, an adjustment of equal magnitude and opposite polarity is written into the ADCOFFTRIM register. The value contained in this register is applied before the results are available in the ADC result registers. This operation is fully contained within the ADC core, so the timing of the results is not affected, and the full dynamic range of the ADC is maintained for any trim value.

Note

Regardless of the converter resolution, the size of each ADCOFFTRIM step is (VREFHI-VREFLO)/65536.

Use the following procedure to re-calibrate the ADC offset in 12-bit single-ended mode:

1. Set ADCOFFTRIM to +112 steps (0x70). This adds an artificial offset to account for negative offset that can reside in the ADC core.
2. Perform some multiple of 16 conversions on VREFLO (internal connection, see device DS for the ADC channel connected to VREFLO), accumulating the results (for example, 32 × 16 conversions = 512 conversions). Use the maximum value of ACQPS to make sure longer settling time to account for parasitic impedance of internal VREFLO connections.
3. Divide the accumulated result by the multiple of 16 (for example, for 512 conversions, divide by 32).
4. Set ADCOFFTRIM to 112 – result from step 3.

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20.13 ADC Interrupts & Triggers

20.13.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 20-14. CPU Interrupts Triggered by the ADC

NVIC Interrupt Name	Peripheral Instance Name	Register Group	ADC Interrupt Configuration Registers	Description
ADC0_INT1	ADC0	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC0 ADCINT1 interrupt. Single, configurable source condition.
ADC0_INT2	ADC0	N/A	ADCINTSEL.INT2SEL, ADCINTSEL.INT2E, ADCINTFLG.ADCINT2, ADCINTFLGFRC.ADCINT2, ADCINTFLGCLR.ADCINT2	ADC0 ADCINT2 interrupt. Single, configurable source condition.
ADC0_INT3	ADC0	N/A	ADCINTSEL.INT3SEL, ADCINTSEL.INT3E, ADCINTFLG.ADCINT3, ADCINTFLGFRC.ADCINT3, ADCINTFLGCLR.ADCINT3	ADC0 ADCINT3 interrupt. Single, configurable source condition.
ADC0_INT4	ADC0	N/A	ADCINTSEL.INT4SEL, ADCINTSEL.INT4E, ADCINTFLG.ADCINT4, ADCINTFLGFRC.ADCINT4, ADCINTFLGCLR.ADCINT4	ADC0 ADCINT4 interrupt. Single, configurable source condition.
ADC0_EVT	ADC0	N/A	ADCEVTINTSEL, ADCEVTSTAT, ADCEVTCLR	ADC0 Event interrupt. Single, configurable source condition.
ADC1_INT1	ADC1	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC1 ADCINT1 interrupt. Single, configurable source condition.
ADC1_INT2	ADC1	N/A	ADCINTSEL.INT2SEL, ADCINTSEL.INT2E, ADCINTFLG.ADCINT2, ADCINTFLGFRC.ADCINT2, ADCINTFLGCLR.ADCINT2	ADC1 ADCINT2 interrupt. Single, configurable source condition.
ADC1_INT3	ADC1	N/A	ADCINTSEL.INT3SEL, ADCINTSEL.INT3E, ADCINTFLG.ADCINT3, ADCINTFLGFRC.ADCINT3, ADCINTFLGCLR.ADCINT3	ADC1 ADCINT3 interrupt. Single, configurable source condition.
ADC1_INT4	ADC1	N/A	ADCINTSEL.INT4SEL, ADCINTSEL.INT4E, ADCINTFLG.ADCINT4, ADCINTFLGFRC.ADCINT4, ADCINTFLGCLR.ADCINT4	ADC1 ADCINT4 interrupt. Single, configurable source condition.
ADC1_EVT	ADC1	N/A	ADCEVTINTSEL, ADCEVTSTAT, ADCEVTCLR	ADC1 Event interrupt. Single, configurable source condition.

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Table 20-14. CPU Interrupts Triggered by the ADC (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	ADC Interrupt Configuration Registers	Description
ADC2_INT1	ADC2	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC2 ADCINT1 interrupt. Single, configurable source condition.
ADC2_INT2	ADC2	N/A	ADCINTSEL.INT2SEL, ADCINTSEL.INT2E, ADCINTFLG.ADCINT2, ADCINTFLGFRC.ADCINT2, ADCINTFLGCLR.ADCINT2	ADC2 ADCINT2 interrupt. Single, configurable source condition.
ADC2_INT3	ADC2	N/A	ADCINTSEL.INT3SEL, ADCINTSEL.INT3E, ADCINTFLG.ADCINT3, ADCINTFLGFRC.ADCINT3, ADCINTFLGCLR.ADCINT3	ADC2 ADCINT3 interrupt. Single, configurable source condition.
ADC2_INT4	ADC2	N/A	ADCINTSEL.INT4SEL, ADCINTSEL.INT4E, ADCINTFLG.ADCINT4, ADCINTFLGFRC.ADCINT4, ADCINTFLGCLR.ADCINT4	ADC2 ADCINT4 interrupt. Single, configurable source condition.
ADC2_EVT	ADC2	N/A	ADCEVTINTSEL, ADCEVTSTAT, ADCEVTCLR	ADC2 Event interrupt. Single, configurable source condition.

20.13.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 20-15. DMA Triggers from the ADC

Trigger Name	Peripheral Instance Name	Register Group	ADC DMA Configuration Registers	Description
ADC0_DMA_TRIG1	ADC0	N/A	ADCDMAINTSEL.DMAINT1SEL, ADCDMAINTSEL.DMAINT1CONT, ADCDMAINTSEL.DMAINT1E, ADCINTFLGCLR.ADCDMAINT1	ADC0 DMAINT1 trigger. Single, configurable source condition.
ADC0_DMA_TRIG2	ADC0	N/A	ADCDMAINTSEL.DMAINT2SEL, ADCDMAINTSEL.DMAINT2CONT, ADCDMAINTSEL.DMAINT2E, ADCINTFLGCLR.ADCDMAINT2	ADC0 DMAINT2 trigger. Single, configurable source condition.
ADC0_DMA_TRIG3	ADC0	N/A	ADCDMAINTSEL.DMAINT3SEL, ADCDMAINTSEL.DMAINT3CONT, ADCDMAINTSEL.DMAINT3E, ADCINTFLGCLR.ADCDMAINT3	ADC0 DMAINT3 trigger. Single, configurable source condition.
ADC0_DMA_TRIG4	ADC0	N/A	ADCDMAINTSEL.DMAINT4SEL, ADCDMAINTSEL.DMAINT4CONT, ADCDMAINTSEL.DMAINT4E, ADCINTFLGCLR.ADCDMAINT4	ADC0 DMAINT4 trigger. Single, configurable source condition.

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Table 20-15. DMA Triggers from the ADC (continued)

Trigger Name	Peripheral Instance Name	Register Group	ADC DMA Configuration Registers	Description
ADC1_DMA_TRIG1	ADC1	N/A	ADCDMAINTSEL.DMAINT1SEL, ADCDMAINTSEL.DMAINT1CONT, ADCDMAINTSEL.DMAINT1E, ADCINTFLGCLR.ADCDMAINT1	ADC1 DMAINT1 trigger. Single, configurable source condition.
ADC1_DMA_TRIG2	ADC1	N/A	ADCDMAINTSEL.DMAINT2SEL, ADCDMAINTSEL.DMAINT2CONT, ADCDMAINTSEL.DMAINT2E, ADCINTFLGCLR.ADCDMAINT2	ADC1 DMAINT2 trigger. Single, configurable source condition.
ADC1_DMA_TRIG3	ADC1	N/A	ADCDMAINTSEL.DMAINT3SEL, ADCDMAINTSEL.DMAINT3CONT, ADCDMAINTSEL.DMAINT3E, ADCINTFLGCLR.ADCDMAINT3	ADC1 DMAINT3 trigger. Single, configurable source condition.
ADC1_DMA_TRIG4	ADC1	N/A	ADCDMAINTSEL.DMAINT4SEL, ADCDMAINTSEL.DMAINT4CONT, ADCDMAINTSEL.DMAINT4E, ADCINTFLGCLR.ADCDMAINT4	ADC1 DMAINT4 trigger. Single, configurable source condition.
ADC2_DMA_TRIG1	ADC2	N/A	ADCDMAINTSEL.DMAINT1SEL, ADCDMAINTSEL.DMAINT1CONT, ADCDMAINTSEL.DMAINT1E, ADCINTFLGCLR.ADCDMAINT1	ADC2 DMAINT1 trigger. Single, configurable source condition.
ADC2_DMA_TRIG2	ADC2	N/A	ADCDMAINTSEL.DMAINT2SEL, ADCDMAINTSEL.DMAINT2CONT, ADCDMAINTSEL.DMAINT2E, ADCINTFLGCLR.ADCDMAINT2	ADC2 DMAINT2 trigger. Single, configurable source condition.
ADC2_DMA_TRIG3	ADC2	N/A	ADCDMAINTSEL.DMAINT3SEL, ADCDMAINTSEL.DMAINT3CONT, ADCDMAINTSEL.DMAINT3E, ADCINTFLGCLR.ADCDMAINT3	ADC2 DMAINT3 trigger. Single, configurable source condition.
ADC2_DMA_TRIG4	ADC2	N/A	ADCDMAINTSEL.DMAINT4SEL, ADCDMAINTSEL.DMAINT4CONT, ADCDMAINTSEL.DMAINT4E, ADCINTFLGCLR.ADCDMAINT4	ADC2 DMAINT4 trigger. Single, configurable source condition.

20.13.3 ADC Sequencer Triggers

See the Section 20.3.3 section for more details about how to configure triggers for individual ADC sequencers.

Table 20-16. ADC Triggers from the ADC

Trigger Name	Peripheral Instance Name	Register Group	ADC-to-ADC Trigger Configuration Registers	Description
ADC0_INT1	ADC0	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC0 ADCINT1 triggers an ADC sequencer operation. Single, configurable source condition.

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Table 20-16. ADC Triggers from the ADC (continued)

Trigger Name	Peripheral Instance Name	Register Group	ADC-to-ADC Trigger Configuration Registers	Description
ADC1_INT1	ADC1	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC1 ADCINT1 triggers an ADC sequencer operation. Single, configurable source condition.
ADC2_INT1	ADC2	N/A	ADCINTSEL.INT1SEL, ADCINTSEL.INT1E, ADCINTFLG.ADCINT1, ADCINTFLGFRC.ADCINT1, ADCINTFLGCLR.ADCINT1	ADC2 ADCINT1 triggers an ADC sequencer operation. Single, configurable source condition.

20.14 ADC Registers

This Section describes the ADC Registers.

20.14.1 ADC Base Address Table

Table 20-17. ADC Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Adc0Regs	ADC_LITE_REGS	ADC0	0x4000_0000
Adc1Regs	ADC_LITE_REGS	ADC1	0x4000_2000
Adc2Regs	ADC_LITE_REGS	ADC2	0x4000_4000
Adc0ResultRegs	ADC_LITE_RESULT_REGS	ADC0RESULT	0x4000_A000
Adc1ResultRegs	ADC_LITE_RESULT_REGS	ADC1RESULT	0x4000_B000
Adc2ResultRegs	ADC_LITE_RESULT_REGS	ADC2RESULT	0x4000_C000

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20.14.2 ADC_LITE_REGS Registers

Table 20-18 lists the memory-mapped registers for the ADC_LITE_REGS registers. All register offset addresses not listed in Table 20-18 should be considered as reserved locations and the register contents should not be modified.

Table 20-18. ADC_LITE_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control.		Go
814h	STAT	Status Register		Go
1000h	ADCCTL1	ADC Control 1 Register		Go
1004h	ADCCTL2	ADC Control 2 Register		Go
1010h	ADCINTSEL	ADC Interrupt 1, 2, 3 and 4 Selection Register		Go
1014h	ADCDMAINTSEL	ADC DMA Interrupt 1, 2, 3 and 4 Selection Register		Go
1018h	ADCRAWINTFLG	ADC Raw Interrupt Flag Register		Go
101Ch	ADCINTFLG	ADC Interrupt Flag Register		Go
1020h	ADCINTFLGFRC	ADC Interrupt Flag Force Register		Go
1024h	ADCINTFLGCLR	ADC Interrupt Flag Clear Register		Go
1028h	ADCINTOVF	ADC Interrupt Overflow Register		Go
102Ch	ADCINTOVFCLR	ADC Interrupt Overflow Clear Register		Go
103Ch	ADCSOCFLG1	ADC SOC Flag 1 Register		Go
1044h	ADCSOCOVF1	ADC SOC Overflow 1 Register		Go
1048h	ADCSOCOVFCLR1	ADC SOC Overflow Clear 1 Register		Go
104Ch	ADCSOC0CTL	ADC SOC0 Control Register		Go
1050h	ADCSOC1CTL	ADC SOC1 Control Register		Go
1054h	ADCSOC2CTL	ADC SOC2 Control Register		Go
1058h	ADCSOC3CTL	ADC SOC3 Control Register		Go
105Ch	ADCSOC4CTL	ADC SOC4 Control Register		Go
1060h	ADCSOC5CTL	ADC SOC5 Control Register		Go
1064h	ADCSOC6CTL	ADC SOC6 Control Register		Go
1068h	ADCSOC7CTL	ADC SOC7 Control Register		Go
106Ch	ADCSOC8CTL	ADC SOC8 Control Register		Go
1070h	ADCSOC9CTL	ADC SOC9 Control Register		Go
1074h	ADCSOC10CTL	ADC SOC10 Control Register		Go
1078h	ADCSOC11CTL	ADC SOC11 Control Register		Go
107Ch	ADCSOC12CTL	ADC SOC12 Control Register		Go
1080h	ADCSOC13CTL	ADC SOC13 Control Register		Go
1084h	ADCSOC14CTL	ADC SOC14 Control Register		Go
1088h	ADCSOC15CTL	ADC SOC15 Control Register		Go
10CCh	ADCEVTSTAT	ADC Event Status Register		Go
10D0h	ADCEVTCLR	ADC Event Clear Register		Go
10D4h	ADCEVTSEL	ADC Event Selection Register		Go
10D8h	ADCEVTINTSEL	ADC Event Interrupt Selection Register		Go
10E4h	ADCREV	ADC Revision Register		Go
10E8h	ADCOFFTRIM	ADC Offset Trim Register 1		Go
1100h	ADCPPB1CONFIG	ADC PPB1 Config Register		Go
1110h	ADCPPB1TRIPHI	ADC PPB1 Trip High Register		Go

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Table 20-18. ADC_LITE_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
1114h	ADCPPB1TRIPLO	ADC PPB1 Trip Low/Trigger Time Stamp Register		Go
1120h	ADCPPB2CONFIG	ADC PPB2 Config Register		Go
1130h	ADCPPB2TRIPHI	ADC PPB2 Trip High Register		Go
1134h	ADCPPB2TRIPLO	ADC PPB2 Trip Low/Trigger Time Stamp Register		Go
1140h	ADCPPB3CONFIG	ADC PPB3 Config Register		Go
1150h	ADCPPB3TRIPHI	ADC PPB3 Trip High Register		Go
1154h	ADCPPB3TRIPLO	ADC PPB3 Trip Low/Trigger Time Stamp Register		Go
1160h	ADCPPB4CONFIG	ADC PPB4 Config Register		Go
1170h	ADCPPB4TRIPHI	ADC PPB4 Trip High Register		Go
1174h	ADCPPB4TRIPLO	ADC PPB4 Trip Low/Trigger Time Stamp Register		Go
1180h	ADCINTCYCLE	ADC Early Interrupt Generation Cycle		Go
119Ch	ADCREV2	ADC Wrapper Revision Register		Go
1200h	ADCPPB1LIMIT	ADC PPB1Conversion Count Limit Register		Go
1204h	ADCPPB1PCOUNT	ADC PPB1 Partial Conversion Count Register		Go
1208h	ADCPPB1CONFIG2	ADC PPB1 Sum Shift Register		Go
120Ch	ADCPPB1PSUM	ADC PPB1 Partial Sum Register		Go
1240h	ADCPPB2LIMIT	ADC PPB2Conversion Count Limit Register		Go
1244h	ADCPPB2PCOUNT	ADC PPB2 Partial Conversion Count Register		Go
1248h	ADCPPB2CONFIG2	ADC PPB2 Sum Shift Register		Go
124Ch	ADCPPB2PSUM	ADC PPB2 Partial Sum Register		Go
1280h	ADCPPB3LIMIT	ADC PPB3Conversion Count Limit Register		Go
1284h	ADCPPB3PCOUNT	ADC PPB3 Partial Conversion Count Register		Go
1288h	ADCPPB3CONFIG2	ADC PPB3 Sum Shift Register		Go
128Ch	ADCPPB3PSUM	ADC PPB3 Partial Sum Register		Go
12C0h	ADCPPB4LIMIT	ADC PPB4Conversion Count Limit Register		Go
12C4h	ADCPPB4PCOUNT	ADC PPB4 Partial Conversion Count Register		Go
12C8h	ADCPPB4CONFIG2	ADC PPB4 Sum Shift Register		Go
12CCh	ADCPPB4PSUM	ADC PPB4 Partial Sum Register		Go
1320h	ADCSEQCTL	ADC Sequencer common control Register		Go
1324h	ADCSEQ1CONFIG	ADC Sequencer 1 Config register		Go
1328h	ADCSEQ2CONFIG	ADC Sequencer 2 Config register		Go
132Ch	ADCSEQ3CONFIG	ADC Sequencer 3 Config register		Go
1330h	ADCSEQ4CONFIG	ADC Sequencer 4 Config register		Go

Complex bit access types are encoded to fit into small table cells. Table 20-19 shows the codes that are used for access types in this section.

Table 20-19. ADC_LITE_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write

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Table 20-19. ADC_LITE_REGS Access Type Codes (continued)

Access Type	Code	Description
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 20-20 and described in Table 20-20.

Return to the Summary Table.

Register to control the power state.

Figure 20-20. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 20-21. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change. 26h = KEY to allow write access to this register.
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power. [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power. 1h = Enable Power.

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 20-21 and described in Table 20-21.

Return to the Summary Table.

Register to control reset assertion and de-assertion

.

Figure 20-21. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 20-23. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key. B1h = KEY to allow write access to this register.
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register. [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect. 1h = Clear reset sticky bit.
0	RESETASSERT	WK	0h	Assert reset to the peripheral. [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect. 1h = Assert reset.

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 20-22 and described in Table 20-22.

Return to the Summary Table.

Peripheral Enable and Reset Status Register.

Figure 20-22. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKYCLR
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-25. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	

16	RESETSTKYCLR	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register. #br 0h = The peripheral has NOT been reset since the bit was last cleared. #br 1h = The peripheral has been reset since the bit was last cleared.
				0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register.
				1h = The peripheral was reset since the last bit clear.

15-0	RESERVED	R	0h	

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4 ADCCTL1 Register (Offset = 1000h) [Reset = 00000000h]

ADCCTL1 is shown in Figure 20-23 and described in Table 20-23.

Return to the Summary Table.

ADC Control 1 Register.

Figure 20-23. ADCCTL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		ADCBSY	RESERVED	ADCBSYCHN			
R-0h		R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
ADCPWDNZ	RESERVED				INTPULSEPOS	RESERVED	
R/W-0h	R-0h				R/W-0h	R-0h	

Table 20-27. ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel. 1 ADC is busy and cannot sample another channel. Reset type: SYSRST
12	RESERVED	R	0h	Reserved
11-8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when an ADC Start of Conversion (SOC) is generated. When ADCBSY=0: holds the value of the last converted SOC. When ADCBSY=1: reflects the SOC currently being processed. 0h SOC0 is currently processing or was last SOC converted. 1h SOC1 is currently processing or was last SOC converted. 2h SOC2 is currently processing or was last SOC converted. 3h SOC3 is currently processing or was last SOC converted. 4h SOC4 is currently processing or was last SOC converted. 5h SOC5 is currently processing or was last SOC converted. 6h SOC6 is currently processing or was last SOC converted. 7h SOC7 is currently processing or was last SOC converted. 8h SOC8 is currently processing or was last SOC converted. 9h SOC9 is currently processing or was last SOC converted. Ah SOC10 is currently processing or was last SOC converted. Bh SOC11 is currently processing or was last SOC converted. Ch SOC12 is currently processing or was last SOC converted. Dh SOC13 is currently processing or was last SOC converted. Eh SOC14 is currently processing or was last SOC converted. Fh SOC15 is currently processing or was last SOC converted. Reset type: SYSRST

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Table 20-27. ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ADCPWDNZ	R/W	0h	ADC Power Down (active low). This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down. 1 All analog circuitry inside the core is powered up. Reset type: SYSRST
6-3	RESERVED	R	0h	Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion (at the end of the acquisition window) plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register. Reset type: SYSRST
1-0	RESERVED	R	0h	Reserved

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5 ADCCTL2 Register (Offset = 1004h) [Reset = 00000000h]

ADCCTL2 is shown in Figure 20-24 and described in Table 20-24.

Return to the Summary Table.

ADC Control 2 Register

Figure 20-24. ADCCTL2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			RESERVED				RESERVED
R-0h			R-0h				R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		PRESCALE			
R/W-0h	R/W-0h	R-0h		R/W-0h			

Table 20-29. ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 ADCCLK = Input Clock / 1.5 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5 Reset type: SYSRST

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6 ADCINTSEL Register (Offset = 1010h) [Reset = 00000000h]

ADCINTSEL is shown in Figure 20-25 and described in Table 20-25.

Return to the Summary Table.

ADC Interrupt 1, 2, 3 and 4 Selection Register

Figure 20-25. ADCINTSEL Register

31	30	29	28	27	26	25	24
INT4E	INT4CONT	RESERVED		INT4SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
23	22	21	20	19	18	17	16
INT3E	INT3CONT	RESERVED		INT3SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
15	14	13	12	11	10	9	8
INT2E	INT2CONT	RESERVED		INT2SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
7	6	5	4	3	2	1	0
INT1E	INT1CONT	RESERVED		INT1SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			

Table 20-31. ADCINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled Reset type: SYSRST
30	INT4CONT	R/W	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
29-28	RESERVED	R	0h	Reserved
27-24	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 00h EOC0 is trigger for ADCINT4 01h EOC1 is trigger for ADCINT4 02h EOC2 is trigger for ADCINT4 03h EOC3 is trigger for ADCINT4 04h EOC4 is trigger for ADCINT4 05h EOC5 is trigger for ADCINT4 06h EOC6 is trigger for ADCINT4 07h EOC7 is trigger for ADCINT4 08h EOC8 is trigger for ADCINT4 09h EOC9 is trigger for ADCINT4 0Ah EOC10 is trigger for ADCINT4 0Bh EOC11 is trigger for ADCINT4 0Ch EOC12 is trigger for ADCINT4 0Dh EOC13 is trigger for ADCINT4 0Eh EOC14 is trigger for ADCINT4 0Fh EOC15 is trigger for ADCINT4 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the interrupts Reset type: SYSRST

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Table 20-31. ADCINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled Reset type: SYSRST
22	INT3CONT	R/W	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
21-20	RESERVED	R	0h	Reserved
19-16	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 00h EOC0 is trigger for ADCINT3 01h EOC1 is trigger for ADCINT3 02h EOC2 is trigger for ADCINT3 03h EOC3 is trigger for ADCINT3 04h EOC4 is trigger for ADCINT3 05h EOC5 is trigger for ADCINT3 06h EOC6 is trigger for ADCINT3 07h EOC7 is trigger for ADCINT3 08h EOC8 is trigger for ADCINT3 09h EOC9 is trigger for ADCINT3 0Ah EOC10 is trigger for ADCINT3 0Bh EOC11 is trigger for ADCINT3 0Ch EOC12 is trigger for ADCINT3 0Dh EOC13 is trigger for ADCINT3 0Eh EOC14 is trigger for ADCINT3 0Fh EOC15 is trigger for ADCINT3 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the interrupts Reset type: SYSRST
15	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled Reset type: SYSRST
14	INT2CONT	R/W	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
13-12	RESERVED	R	0h	Reserved

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Table 20-31. ADCINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 00h EOC0 is trigger for ADCINT2 01h EOC1 is trigger for ADCINT2 02h EOC2 is trigger for ADCINT2 03h EOC3 is trigger for ADCINT2 04h EOC4 is trigger for ADCINT2 05h EOC5 is trigger for ADCINT2 06h EOC6 is trigger for ADCINT2 07h EOC7 is trigger for ADCINT2 08h EOC8 is trigger for ADCINT2 09h EOC9 is trigger for ADCINT2 0Ah EOC10 is trigger for ADCINT2 0Bh EOC11 is trigger for ADCINT2 0Ch EOC12 is trigger for ADCINT2 0Dh EOC13 is trigger for ADCINT2 0Eh EOC14 is trigger for ADCINT2 0Fh EOC15 is trigger for ADCINT2 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the interrupts Reset type: SYSRST
7	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled Reset type: SYSRST
6	INT1CONT	R/W	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
5-4	RESERVED	R	0h	Reserved
3-0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 00h EOC0 is trigger for ADCINT1 01h EOC1 is trigger for ADCINT1 02h EOC2 is trigger for ADCINT1 03h EOC3 is trigger for ADCINT1 04h EOC4 is trigger for ADCINT1 05h EOC5 is trigger for ADCINT1 06h EOC6 is trigger for ADCINT1 07h EOC7 is trigger for ADCINT1 08h EOC8 is trigger for ADCINT1 09h EOC9 is trigger for ADCINT1 0Ah EOC10 is trigger for ADCINT1 0Bh EOC11 is trigger for ADCINT1 0Ch EOC12 is trigger for ADCINT1 0Dh EOC13 is trigger for ADCINT1 0Eh EOC14 is trigger for ADCINT1 0Fh EOC15 is trigger for ADCINT1 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the interrupts Reset type: SYSRST

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7 ADCDMAINTSEL Register (Offset = 1014h) [Reset = 00000000h]

ADCDMAINTSEL is shown in Figure 20-26 and described in Table 20-26.

Return to the Summary Table.

ADC DMA Interrupt 1, 2, 3 and 4 Selection Register

Figure 20-26. ADCDMAINTSEL Register

31	30	29	28	27	26	25	24
DMAINT4E	DMAINT4CONT	RESERVED		DMAINT4SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
23	22	21	20	19	18	17	16
DMAINT3E	DMAINT3CONT	RESERVED		DMAINT3SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
15	14	13	12	11	10	9	8
DMAINT2E	DMAINT2CONT	RESERVED		DMAINT2SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			
7	6	5	4	3	2	1	0
DMAINT1E	DMAINT1CONT	RESERVED		DMAINT1SEL			
R/W-0h	R/W-0h	R-0h		R/W-0h			

Table 20-33. ADCDMAINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DMAINT4E	R/W	0h	ADCDMAINT4 Interrupt Enable 0 ADCDMAINT4 is disabled 1 ADCDMAINT4 is enabled Reset type: SYSRST
30	DMAINT4CONT	R/W	0h	ADCDMAINT4 Continue to Interrupt Mode 0 No further ADCDMAINT4 pulses are generated until ADCDMAINT4 flag (in ADCDMAINTFLG register) is cleared by user. 1 ADCDMAINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
29-28	RESERVED	R	0h	Reserved
27-24	DMAINT4SEL	R/W	0h	ADCDMAINT4 EOC Source Select 00h EOC0 is trigger for ADCDMAINT4 01h EOC1 is trigger for ADCDMAINT4 02h EOC2 is trigger for ADCDMAINT4 03h EOC3 is trigger for ADCDMAINT4 04h EOC4 is trigger for ADCDMAINT4 05h EOC5 is trigger for ADCDMAINT4 06h EOC6 is trigger for ADCDMAINT4 07h EOC7 is trigger for ADCDMAINT4 08h EOC8 is trigger for ADCDMAINT4 09h EOC9 is trigger for ADCDMAINT4 0Ah EOC10 is trigger for ADCDMAINT4 0Bh EOC11 is trigger for ADCDMAINT4 0Ch EOC12 is trigger for ADCDMAINT4 0Dh EOC13 is trigger for ADCDMAINT4 0Eh EOC14 is trigger for ADCDMAINT4 0Fh EOC15 is trigger for ADCDMAINT4 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the DMA Interrupt. Reset type: SYSRST

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Table 20-33. ADCDMAINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DMAINT3E	R/W	0h	ADCDMAINT3 Interrupt Enable 0 ADCDMAINT3 is disabled 1 ADCDMAINT3 is enabled Reset type: SYSRST
22	DMAINT3CONT	R/W	0h	ADCDMAINT3 Continue to Interrupt Mode 0 No further ADCDMAINT3 pulses are generated until ADCDMAINT3 flag (in ADCDMAINTFLG register) is cleared by user. 1 ADCDMAINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
21-20	RESERVED	R	0h	Reserved
19-16	DMAINT3SEL	R/W	0h	ADCDMAINT3 EOC Source Select 00h EOC0 is trigger for ADCDMAINT3 01h EOC1 is trigger for ADCDMAINT3 02h EOC2 is trigger for ADCDMAINT3 03h EOC3 is trigger for ADCDMAINT3 04h EOC4 is trigger for ADCDMAINT3 05h EOC5 is trigger for ADCDMAINT3 06h EOC6 is trigger for ADCDMAINT3 07h EOC7 is trigger for ADCDMAINT3 08h EOC8 is trigger for ADCDMAINT3 09h EOC9 is trigger for ADCDMAINT3 0Ah EOC10 is trigger for ADCDMAINT3 0Bh EOC11 is trigger for ADCDMAINT3 0Ch EOC12 is trigger for ADCDMAINT3 0Dh EOC13 is trigger for ADCDMAINT3 0Eh EOC14 is trigger for ADCDMAINT3 0Fh EOC15 is trigger for ADCDMAINT3 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the DMA Interrupt. Reset type: SYSRST
15	DMAINT2E	R/W	0h	ADCDMAINT2 Interrupt Enable 0 ADCDMAINT2 is disabled 1 ADCDMAINT2 is enabled Reset type: SYSRST
14	DMAINT2CONT	R/W	0h	ADCDMAINT2 Continue to Interrupt Mode 0 No further ADCDMAINT2 pulses are generated until ADCDMAINT2 flag (in ADCDMAINTFLG register) is cleared by user. 1 ADCDMAINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
13-12	RESERVED	R	0h	Reserved

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Table 20-33. ADCDMAINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	DMAINT2SEL	R/W	0h	ADCDMAINT2 EOC Source Select 00h EOC0 is trigger for ADCDMAINT2 01h EOC1 is trigger for ADCDMAINT2 02h EOC2 is trigger for ADCDMAINT2 03h EOC3 is trigger for ADCDMAINT2 04h EOC4 is trigger for ADCDMAINT2 05h EOC5 is trigger for ADCDMAINT2 06h EOC6 is trigger for ADCDMAINT2 07h EOC7 is trigger for ADCDMAINT2 08h EOC8 is trigger for ADCDMAINT2 09h EOC9 is trigger for ADCDMAINT2 0Ah EOC10 is trigger for ADCDMAINT2 0Bh EOC11 is trigger for ADCDMAINT2 0Ch EOC12 is trigger for ADCDMAINT2 0Dh EOC13 is trigger for ADCDMAINT2 0Eh EOC14 is trigger for ADCDMAINT2 0Fh EOC15 is trigger for ADCDMAINT2 Note : When oversampling is enabled, the end of the last oversampled coversion will trigger the DMA Interrupt. Reset type: SYSRST
7	DMAINT1E	R/W	0h	ADCDMAINT1 Interrupt Enable 0 ADCDMAINT1 is disabled 1 ADCDMAINT1 is enabled Reset type: SYSRST
6	DMAINT1CONT	R/W	0h	ADCDMAINT1 Continue to Interrupt Mode 0 No further ADCDMAINT1 pulses are generated until ADCDMAINT1 flag (in ADCDMAINTFLG register) is cleared by user. 1 ADCDMAINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not. Reset type: SYSRST
5-4	RESERVED	R	0h	Reserved
3-0	DMAINT1SEL	R/W	0h	ADCDMAINT1 EOC Source Select 00h EOC0 is trigger for ADCDMAINT1 01h EOC1 is trigger for ADCDMAINT1 02h EOC2 is trigger for ADCDMAINT1 03h EOC3 is trigger for ADCDMAINT1 04h EOC4 is trigger for ADCDMAINT1 05h EOC5 is trigger for ADCDMAINT1 06h EOC6 is trigger for ADCDMAINT1 07h EOC7 is trigger for ADCDMAINT1 08h EOC8 is trigger for ADCDMAINT1 09h EOC9 is trigger for ADCDMAINT1 0Ah EOC10 is trigger for ADCDMAINT1 0Bh EOC11 is trigger for ADCDMAINT1 0Ch EOC12 is trigger for ADCDMAINT1 0Dh EOC13 is trigger for ADCDMAINT1 0Eh EOC14 is trigger for ADCDMAINT1 0Fh EOC15 is trigger for ADCDMAINT1 Note : When oversampling is enabled, the end of the last oversampled conversion will trigger the DMA Interrupt. Reset type: SYSRST

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8 ADCRAWINTFLG Register (Offset = 1018h) [Reset = 00000000h]

ADCRAWINTFLG is shown in Figure 20-27 and described in Table 20-27.

Return to the Summary Table.

ADC Raw Interrupt Flag Register

Figure 20-27. ADCRAWINTFLG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMARAWINT4	ADCDMARAWINT3	ADCDMARAWINT2	ADCDMARAWINT1
R-0h				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCRAWINT4	ADCRAWINT3	ADCRAWINT2	ADCRAWINT1
R-0h				R-0h	R-0h	R-0h	R-0h

Table 20-35. ADCRAWINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMARAWINT4	R	0h	ADC DMA Raw Interrupt 4 Flag. Reading these flags indicates if the associated ADCDMAINT condition occurred. This flag will be set irrespective of corresponding DMAINTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occurred Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
18	ADCDMARAWINT3	R	0h	ADC DMA Raw Interrupt 3 Flag. Reading these flags indicates if the associated ADCDMAINT condition occurred. This flag will be set irrespective of corresponding DMAINTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occurred Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
17	ADCDMARAWINT2	R	0h	ADC DMA Raw Interrupt 2 Flag. Reading these flags indicates if the associated ADCDMAINT condition occurred. This flag will be set irrespective of corresponding DMAINTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occurred Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST

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Table 20-35. ADCRAWINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ADCDMARAWINT1	R	0h	ADC DMA Raw Interrupt 1 Flag. Reading these flags indicates if the associated ADCDMAINT condition occurred. This flag will be set irrespective of corresponding DMAINTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occurred Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
15-4	RESERVED	R	0h	Reserved
3	ADCRAWINT4	R	0h	ADC RAW Interrupt 4 Flag. Reading these flags indicates if the associated INT condition occurred. This flag will be set irrespective of corresponding INTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occured Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
2	ADCRAWINT3	R	0h	ADC RAW Interrupt 3 Flag. Reading these flags indicates if the associated INT condition occurred. This flag will be set irrespective of corresponding INTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occured Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
1	ADCRAWINT2	R	0h	ADC RAW Interrupt 2 Flag. Reading these flags indicates if the associated INT condition occurred. This flag will be set irrespective of corresponding INTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occured Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST
0	ADCRAWINT1	R	0h	ADC RAW Interrupt 1 Flag. Reading these flags indicates if the associated INT condition occurred. This flag will be set irrespective of corresponding INTE setting 0 Selected EOC/OSINT event did not occur 1 Selected EOC/OSINT event occurred Writing corresponding INTCLR bit in ADCINTFLGCLR register will clear this bit. Reset type: SYSRST

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9 ADCINTFLG Register (Offset = 101Ch) [Reset = 00000000h]

ADCINTFLG is shown in Figure 20-28 and described in Table 20-28.

Return to the Summary Table.

ADC Interrupt Flag Register

Figure 20-28. ADCINTFLG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMAINT4	ADCDMAINT3	ADCDMAINT2	ADCDMAINT1
R-0h				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED				ADCINT4RESULT	ADCINT3RESULT	ADCINT2RESULT	ADCINT1RESULT
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R-0h	R-0h	R-0h	R-0h

Table 20-37. ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMAINT4	R	0h	ADC DMA Interrupt 4 Flag. Reading these flags indicates if the associated ADCDMAINT pulse was generated since the last clear. 0 No ADC DMA interru4pt pulse generated 1 ADC DMA Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (DMAINTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST
18	ADCDMAINT3	R	0h	ADC DMA Interrupt 3 Flag. Reading these flags indicates if the associated ADCDMAINT pulse was generated since the last clear. 0 No ADC DMA Interrupt pulse generated 1 ADC DMA Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (DMAINTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST

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Table 20-37. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	ADCDMAINT2	R	0h	ADC DMA Interrupt 2 Flag. Reading these flags indicates if the associated ADCDMAINT pulse was generated since the last clear. 0 No ADC DMA Interrupt pulse generated 1 ADC DMA Interrupt pulse generated If the ADC DMA Interrupt is placed in continue to Interrupt mode (DMAINTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST
16	ADCDMAINT1	R	0h	ADC DMA Interrupt 1 Flag. Reading these flags indicates if the associated ADCDMAINT pulse was generated since the last clear. 0 No ADC DMA Interrupt pulse generated 1 ADC DMA Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (DMAINTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST
15-12	RESERVED	R	0h	Reserved
11	ADCINT4RESULT	R	0h	ADC Interrupt 4 Results Ready Flag. This flag is set when the conversions results associated with ADCINT4 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early Interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT4 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch. Reset type: SYSRST
10	ADCINT3RESULT	R	0h	ADC Interrupt 3 Results Ready Flag. This flag is set when the conversions results associated with ADCINT3 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early Interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT3 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch. Reset type: SYSRST

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Table 20-37. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ADCINT2RESULT	R	0h	ADC Interrupt 2 Results Ready Flag. This flag is set when the conversions results associated with ADCINT2 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early Interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT2 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch. Reset type: SYSRST
8	ADCINT1RESULT	R	0h	ADC Interrupt 1 Results Ready Flag. This flag is set when the conversions results associated with ADCINT1 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early Interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT1 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch. Reset type: SYSRST
7-4	RESERVED	R	0h	Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC Interrupt pulse generated 1 ADC Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (INTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC Interrupt pulse generated 1 ADC Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (INTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST

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Table 20-37. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC Interrupt pulse generated 1 ADC Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (INTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC Interrupt pulse generated 1 ADC Interrupt pulse generated If the ADC Interrupt is placed in continue to Interrupt mode (INTSEL register) then further Interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further Interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC Interrupt overflow event occurs in the ADCINTOVF register. Reset type: SYSRST

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10 ADCINTFLGFRC Register (Offset = 1020h) [Reset = 00000000h]

ADCINTFLGFRC is shown in Figure 20-29 and described in Table 20-29.

Return to the Summary Table.

ADC Interrupt Flag Force Register

Figure 20-29. ADCINTFLGFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMAINT4	ADCDMAINT3	ADCDMAINT2	ADCDMAINT1
R-0h				R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 20-39. ADCINTFLGFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMAINT4	R-0/W1S	0h	ADC DMA Interrupt 4 Flag Force. Reads return 0. 0 No action 1 Forces ADCDMAINT4 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
18	ADCDMAINT3	R-0/W1S	0h	ADC DMA Interrupt 3 Flag Force. Reads return 0. 0 No action 1 Forces ADCDMAINT3 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
17	ADCDMAINT2	R-0/W1S	0h	ADC DMA Interrupt 2 Flag Force. Reads return 0. 0 No action 1 Forces ADCDMAINT2 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
16	ADCDMAINT1	R-0/W1S	0h	ADC DMA Interrupt 1 Flag Force. Reads return 0. 0 No action 1 Forces ADCDMAINT1 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R-0/W1S	0h	ADC Interrupt 4 Flag Force. Reads return 0. 0 No action 1 Forces ADCINT4 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST

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Table 20-39. ADCINTFLGFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ADCINT3	R-0/W1S	0h	ADC Interrupt 3 Flag Force. Reads return 0. 0 No action 1 Forces ADCINT3 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
1	ADCINT2	R-0/W1S	0h	ADC Interrupt 2 Flag Force. Reads return 0. 0 No action 1 Forces ADCINT2 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST
0	ADCINT1	R-0/W1S	0h	ADC Interrupt 1 Flag Force. Reads return 0. 0 No action 1 Forces ADCINT1 flags in the ADCINTFLG and ADCRAWINTFLG registers. Reset type: SYSRST

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11 ADCINTFLGCLR Register (Offset = 1024h) [Reset = 00000000h]

ADCINTFLGCLR is shown in Figure 20-30 and described in Table 20-30.

Return to the Summary Table.

ADC Interrupt Flag Clear Register

Figure 20-30. ADCINTFLGCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMAINT4	ADCDMAINT3	ADCDMAINT2	ADCDMAINT1
R-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 20-41. ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMAINT4	R-0/W1C	0h	ADC DMA Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears ADDMACINT4 flags in the ADCINTFLG ,ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
18	ADCDMAINT3	R-0/W1C	0h	ADC DMA Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears ADDMACINT3 flags in the ADCINTFLG ,ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
17	ADCDMAINT2	R-0/W1C	0h	ADC DMA Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears ADDMACINT2 flags in the ADCINTFLG ,ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST

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Table 20-41. ADCINTFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ADCDMAINT1	R-0/W1C	0h	ADC DMA Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears ADDMACINT1 flags in the ADCINTFLG ,ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
15-4	RESERVED	R	0h	Reserved
3	ADCINT4	R-0/W1C	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT4 and ADCINT4RESULT flags in the ADCINTFLG,, ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
2	ADCINT3	R-0/W1C	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT3 and ADCINT3RESULT flags in the ADCINTFLG, ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
1	ADCINT2	R-0/W1C	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT2 and ADCINT2RESULT flags in the ADCINTFLG, ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST
0	ADCINT1	R-0/W1C	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT1 and ADCINT1RESULT flags in the ADCINTFLG, ADCRAWINTFLG registers. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set Reset type: SYSRST

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12 ADCINTOVF Register (Offset = 1028h) [Reset = 00000000h]

ADCINTOVF is shown in Figure 20-31 and described in Table 20-31.

Return to the Summary Table.

ADC Interrupt Overflow Register

Figure 20-31. ADCINTOVF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMAINT4OVF	ADCDMAINT3OVF	ADCDMAINT2OVF	ADCDMAINT1OVF
R-0h				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4OVF	ADCINT3OVF	ADCINT2OVF	ADCINT1OVF
R-0h				R-0h	R-0h	R-0h	R-0h

Table 20-43. ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMAINT4OVF	R	0h	ADC DMA Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC DMA Interrupt overflow event detected. 1 ADC DMA Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
18	ADCDMAINT3OVF	R	0h	ADC DMA Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC DMA Interrupt overflow event detected. 1 ADC DMA Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
17	ADCDMAINT2OVF	R	0h	ADC DMA Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC DMA Interrupt overflow event detected. 1 ADC DMA Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST

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Table 20-43. ADCINTOVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	ADCDMAINT1OVF	R	0h	ADC DMA Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC DMA Interrupt overflow event detected. 1 ADC DMA Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
15-4	RESERVED	R	0h	Reserved
3	ADCINT4OVF	R	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC Interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
2	ADCINT3OVF	R	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC Interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
1	ADCINT2OVF	R	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC Interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST
0	ADCINT1OVF	R	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC Interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. Reset type: SYSRST

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13 ADCINTOVFCLR Register (Offset = 102Ch) [Reset = 00000000h]

ADCINTOVFCLR is shown in Figure 20-32 and described in Table 20-32.

Return to the Summary Table.

ADC Interrupt Overflow Clear Register

Figure 20-32. ADCINTOVFCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				ADCDMAINT4OVF	ADCDMAINT3OVF	ADCDMAINT2OVF	ADCDMAINT1OVF
R-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4OVF	ADCINT3OVF	ADCINT2OVF	ADCINT1OVF
R-0h				R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 20-45. ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	ADCDMAINT4OVF	R-0/W1C	0h	ADC DMA Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
18	ADCDMAINT3OVF	R-0/W1C	0h	ADC DMA Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
17	ADCDMAINT2OVF	R-0/W1C	0h	ADC DMA Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
16	ADCDMAINT1OVF	R-0/W1C	0h	ADC DMA Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST

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Table 20-45. ADCINTOVFCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	ADCINT4OVF	R-0/W1C	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
2	ADCINT3OVF	R-0/W1C	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
1	ADCINT2OVF	R-0/W1C	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST
0	ADCINT1OVF	R-0/W1C	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. Reset type: SYSRST

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14 ADCSOCFLG1 Register (Offset = 103Ch) [Reset = 00000000h]

ADCSOCFLG1 is shown in Figure 20-33 and described in Table 20-33.

Return to the Summary Table.

ADC SOC Flag 1 Register

Figure 20-33. ADCSOCFLG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 20-47. ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST

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Table 20-47. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST

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Table 20-47. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST

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Table 20-47. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST

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Table 20-47. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. Reset type: SYSRST

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15 ADCSOCOVF1 Register (Offset = 1044h) [Reset = 00000000h]

ADCSOCOVF1 is shown in Figure 20-34 and described in Table 20-34.

Return to the Summary Table.

ADC SOC Overflow 1 Register

Figure 20-34. ADCSOCOVF1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
SOC15OVF	SOC14OVF	SOC13OVF	SOC12OVF	SOC11OVF	SOC10OVF	SOC9OVF	SOC8OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SOC7OVF	SOC6OVF	SOC5OVF	SOC4OVF	SOC3OVF	SOC2OVF	SOC1OVF	SOC0OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 20-49. ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SOC15OVF	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
14	SOC14OVF	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
13	SOC13OVF	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST

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Table 20-49. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12OVF	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
11	SOC11OVF	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
10	SOC10OVF	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
9	SOC9OVF	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
8	SOC8OVF	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
7	SOC7OVF	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST

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Table 20-49. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SOC6OVF	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
5	SOC5OVF	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
4	SOC4OVF	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
3	SOC3OVF	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
2	SOC2OVF	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST
1	SOC1OVF	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST

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Table 20-49. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SOC0OVF	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. Reset type: SYSRST

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16 ADCSOCOVFCLR1 Register (Offset = 1048h) [Reset = 00000000h]

ADCSOCOVFCLR1 is shown in Figure 20-35 and described in Table 20-35.

Return to the Summary Table.

ADC SOC Overflow Clear 1 Register

Figure 20-35. ADCSOCOVFCLR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
SOC15OVF	SOC14OVF	SOC13OVF	SOC12OVF	SOC11OVF	SOC10OVF	SOC9OVF	SOC8OVF
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
SOC7OVF	SOC6OVF	SOC5OVF	SOC4OVF	SOC3OVF	SOC2OVF	SOC1OVF	SOC0OVF
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 20-51. ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	SOC15OVF	R-0/W1C	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
14	SOC14OVF	R-0/W1C	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
13	SOC13OVF	R-0/W1C	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST

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Table 20-51. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12OVF	R-0/W1C	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
11	SOC11OVF	R-0/W1C	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
10	SOC10OVF	R-0/W1C	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
9	SOC9OVF	R-0/W1C	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
8	SOC8OVF	R-0/W1C	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
7	SOC7OVF	R-0/W1C	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST

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Table 20-51. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SOC6OVF	R-0/W1C	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
5	SOC5OVF	R-0/W1C	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
4	SOC4OVF	R-0/W1C	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
3	SOC3OVF	R-0/W1C	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
2	SOC2OVF	R-0/W1C	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST
1	SOC1OVF	R-0/W1C	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST

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Table 20-51. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SOC0OVF	R-0/W1C	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. Reset type: SYSRST

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17 ADCSOC0CTL Register (Offset = 104Ch) [Reset = 00000000h]

ADCSOC0CTL is shown in Figure 20-36 and described in Table 20-36.

Return to the Summary Table.

ADC SOC0 Control Register

Figure 20-36. ADCSOC0CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-53. ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC0 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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18 ADCSOC1CTL Register (Offset = 1050h) [Reset = 00000000h]

ADCSOC1CTL is shown in Figure 20-37 and described in Table 20-37.

Return to the Summary Table.

ADC SOC1 Control Register

Figure 20-37. ADCSOC1CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-55. ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC1 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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19 ADCSOC2CTL Register (Offset = 1054h) [Reset = 00000000h]

ADCSOC2CTL is shown in Figure 20-38 and described in Table 20-38.

Return to the Summary Table.

ADC SOC2 Control Register

Figure 20-38. ADCSOC2CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-57. ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC2 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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20 ADCSOC3CTL Register (Offset = 1058h) [Reset = 00000000h]

ADCSOC3CTL is shown in Figure 20-39 and described in Table 20-39.

Return to the Summary Table.

ADC SOC3 Control Register

Figure 20-39. ADCSOC3CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-59. ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC3 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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21 ADCSOC4CTL Register (Offset = 105Ch) [Reset = 00000000h]

ADCSOC4CTL is shown in Figure 20-40 and described in Table 20-40.

Return to the Summary Table.

ADC SOC4 Control Register

Figure 20-40. ADCSOC4CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-61. ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC4 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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22 ADCSOC5CTL Register (Offset = 1060h) [Reset = 00000000h]

ADCSOC5CTL is shown in Figure 20-41 and described in Table 20-41.

Return to the Summary Table.

ADC SOC5 Control Register

Figure 20-41. ADCSOC5CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-63. ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC5 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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23 ADCSOC6CTL Register (Offset = 1064h) [Reset = 00000000h]

ADCSOC6CTL is shown in Figure 20-42 and described in Table 20-42.

Return to the Summary Table.

ADC SOC6 Control Register

Figure 20-42. ADCSOC6CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-65. ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC6 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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24 ADCSOC7CTL Register (Offset = 1068h) [Reset = 00000000h]

ADCSOC7CTL is shown in Figure 20-43 and described in Table 20-43.

Return to the Summary Table.

ADC SOC7 Control Register

Figure 20-43. ADCSOC7CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-67. ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC7 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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25 ADCSOC8CTL Register (Offset = 106Ch) [Reset = 00000000h]

ADCSOC8CTL is shown in Figure 20-44 and described in Table 20-44.

Return to the Summary Table.

ADC SOC8 Control Register

Figure 20-44. ADCSOC8CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-69. ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC8 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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26 ADCSOC9CTL Register (Offset = 1070h) [Reset = 00000000h]

ADCSOC9CTL is shown in Figure 20-45 and described in Table 20-45.

Return to the Summary Table.

ADC SOC9 Control Register

Figure 20-45. ADCSOC9CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-71. ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC9 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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27 ADCSOC10CTL Register (Offset = 1074h) [Reset = 00000000h]

ADCSOC10CTL is shown in Figure 20-46 and described in Table 20-46.

Return to the Summary Table.

ADC SOC10 Control Register

Figure 20-46. ADCSOC10CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-73. ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC10 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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28 ADCSOC11CTL Register (Offset = 1078h) [Reset = 00000000h]

ADCSOC11CTL is shown in Figure 20-47 and described in Table 20-47.

Return to the Summary Table.

ADC SOC11 Control Register

Figure 20-47. ADCSOC11CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-75. ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC11 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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29 ADCSOC12CTL Register (Offset = 107Ch) [Reset = 00000000h]

ADCSOC12CTL is shown in Figure 20-48 and described in Table 20-48.

Return to the Summary Table.

ADC SOC12 Control Register

Figure 20-48. ADCSOC12CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-77. ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC12 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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30 ADCSOC13CTL Register (Offset = 1080h) [Reset = 00000000h]

ADCSOC13CTL is shown in Figure 20-49 and described in Table 20-49.

Return to the Summary Table.

ADC SOC13 Control Register

Figure 20-49. ADCSOC13CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-79. ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC13 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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31 ADCSOC14CTL Register (Offset = 1084h) [Reset = 00000000h]

ADCSOC14CTL is shown in Figure 20-50 and described in Table 20-50.

Return to the Summary Table.

ADC SOC14 Control Register

Figure 20-50. ADCSOC14CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-81. ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC14 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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32 ADCSOC15CTL Register (Offset = 1088h) [Reset = 00000000h]

ADCSOC15CTL is shown in Figure 20-51 and described in Table 20-51.

Return to the Summary Table.

ADC SOC15 Control Register

Figure 20-51. ADCSOC15CTL Register

31	30	29	28	27	26	25	24
RESERVED						COMPEN	RESERVED
R-0h						R/W-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED				CHSEL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CHSEL	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20-83. ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	COMPEN	R/W	0h	SOC15 Threshold comparator enable. Reset type: SYSRST
24-20	RESERVED	R	0h	Reserved
19-15	CHSEL	R/W	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Reset type: SYSRST
14-0	RESERVED	R	0h	Reserved

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33 ADCEVTSTAT Register (Offset = 10CCh) [Reset = 00000000h]

ADCEVTSTAT is shown in Figure 20-52 and described in Table 20-52.

Return to the Summary Table.

ADC Event Status Register

Figure 20-52. ADCEVTSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PPB4INLIMIT	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	PPB3INLIMIT	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PPB2INLIMIT	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	PPB1INLIMIT	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 20-85. ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PPB4INLIMIT	R	0h	Post Processing Block 4 Within trip limit Flag. When set indicates a digital compare within limit event has occurred. This will be set when the PPB result is either in between or equal to the TRIPHI and TRIPLO thresholds. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
14	PPB4ZERO	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADC PPB4RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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Table 20-85. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
11	PPB3INLIMIT	R	0h	Post Processing Block 3 Within trip limit Flag. When set indicates a digital compare within limit event has occurred. This will be set when the PPB result is either in between or equal to the TRIPHI and TRIPLO thresholds. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
10	PPB3ZERO	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADC PPB3RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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Table 20-85. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PPB2INLIMIT	R	0h	Post Processing Block 2 Within trip limit Flag. When set indicates a digital compare within limit event has occurred. This will be set when the PPB result is either in between or equal to the TRIPHI and TRIPLO thresholds. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
6	PPB2ZERO	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADC PPB2RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
3	PPB1INLIMIT	R	0h	Post Processing Block 1 Within trip limit Flag. When set indicates a digital compare within limit event has occurred. This will be set when the PPB result is either in between or equal to the TRIPHI and TRIPLO thresholds. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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Table 20-85. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PPB1ZERO	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADC PPB1RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the Interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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34 ADCEVTCLR Register (Offset = 10D0h) [Reset = 00000000h]

ADCEVTCLR is shown in Figure 20-53 and described in Table 20-53.

Return to the Summary Table.

ADC Event Clear Register

Figure 20-53. ADCEVTCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PPB4INLIMIT	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	PPB3INLIMIT	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h
7	6	5	4	3	2	1	0
PPB2INLIMIT	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	PPB1INLIMIT	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 20-87. ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PPB4INLIMIT	R-0/W1C	0h	Post Processing Block 4 Within trip limit flag Clear, Clears the corresponding within trip limit flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
14	PPB4ZERO	R-0/W1C	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
13	PPB4TRIPLO	R-0/W1C	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
12	PPB4TRIPHI	R-0/W1C	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
11	PPB3INLIMIT	R-0/W1C	0h	Post Processing Block 3 Within trip limit flag Clear, Clears the corresponding within trip limit flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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Table 20-87. ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PPB3ZERO	R-0/W1C	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
9	PPB3TRIPLO	R-0/W1C	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
8	PPB3TRIPHI	R-0/W1C	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
7	PPB2INLIMIT	R-0/W1C	0h	Post Processing Block 2 Within trip limit flag Clear, Clears the corresponding within trip limit flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
6	PPB2ZERO	R-0/W1C	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
5	PPB2TRIPLO	R-0/W1C	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
4	PPB2TRIPHI	R-0/W1C	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
3	PPB1INLIMIT	R-0/W1C	0h	Post Processing Block 1 Within trip limit flag Clear, Clears the corresponding within trip limit flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
2	PPB1ZERO	R-0/W1C	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST
1	PPB1TRIPLO	R-0/W1C	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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Table 20-87. ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PPB1TRIPHI	R-0/W1C	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority Reset type: SYSRST

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35 ADCEVTSEL Register (Offset = 10D4h) [Reset = 00000000h]

ADCEVTSEL is shown in Figure 20-54 and described in Table 20-54.

Return to the Summary Table.

ADC Event Selection Register

Figure 20-54. ADCEVTSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PPB4INLIMIT	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	PPB3INLIMIT	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PPB2INLIMIT	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	PPB1INLIMIT	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 20-89. ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PPB4INLIMIT	R/W	0h	Post Processing Block 4 Within trip limit event enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
11	PPB3INLIMIT	R/W	0h	Post Processing Block 3 Within trip limit event enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST

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Table 20-89. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
7	PPB2INLIMIT	R/W	0h	Post Processing Block 2 Within trip limit event enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
3	PPB1INLIMIT	R/W	0h	Post Processing Block 1 Within trip limit event enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST

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Table 20-89. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. Reset type: SYSRST

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36 ADCEVTINTSEL Register (Offset = 10D8h) [Reset = 00000000h]

ADCEVTINTSEL is shown in Figure 20-55 and described in Table 20-55.

Return to the Summary Table.

ADC Event Interrupt Selection Register

Figure 20-55. ADCEVTINTSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PPB4INLIMIT	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	PPB3INLIMIT	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PPB2INLIMIT	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	PPB1INLIMIT	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 20-91. ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	PPB4INLIMIT	R/W	0h	Post Processing Block 4 Within trip limit Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
11	PPB3INLIMIT	R/W	0h	Post Processing Block 3 Within trip limit Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST

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Table 20-91. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
7	PPB2INLIMIT	R/W	0h	Post Processing Block 2 Within trip limit Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
3	PPB1INLIMIT	R/W	0h	Post Processing Block 1 Within trip limit Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST

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Table 20-91. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event Interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. Reset type: SYSRST

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37 ADCREV Register (Offset = 10E4h) [Reset = 00000006h]

ADCREV is shown in Figure 20-56 and described in Table 20-56.

Return to the Summary Table.

ADC Revision Register

Figure 20-56. ADCREV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																								TYPE							
R-0h																								R-6h							

Table 20-93. ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	REV	R	0h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h. Reset type: SYSRST
7-0	TYPE	R	6h	ADC Type. Always set to 6 for this HSADC-12b. Reset type: SYSRST

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38 ADCOFFTRIM Register (Offset = 10E8h) [Reset = 00000000h]

ADCOFFTRIM is shown in Figure 20-57 and described in Table 20-57.

Return to the Summary Table.

ADC Offset Trim Register 1

Figure 20-57. ADCOFFTRIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								OFFTRIM							
R-0h																								R/W-0h							

Table 20-95. ADCOFFTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	OFFTRIM	R/W	0h	ADC Offset Trim Adjusts the conversion results of the converter up or down to account for offset error in the ADC. A factory trim setting will be loaded during device boot. Offset can be corrected in the range of +7 to -8 LSBs. Value is 16*Offset in 8-bit 2's complement: 7 LSB (16*7) = 112 6 LSB (16*6) = 96 5 LSB (16*5) = 80 4 LSB (16*4) = 64 3 LSB (16*3) = 48 2 LSB (16*2) = 32 1 LSB (16*1) = 16 0 LSB (16*0) = 0 -1 LSB (16*(-1)) = 240 : : -7LSB(16*(-7)) = 144 Reset type: POR

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39 ADCPPB1CONFIG Register (Offset = 1100h) [Reset = 00000000h]

ADCPPB1CONFIG is shown in Figure 20-58 and described in Table 20-58.

Return to the Summary Table.

ADC PPB1 Config Register

Figure 20-58. ADCPPB1CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	CBCEN	RESERVED				
R/W-0h	R-0h	R/W-0h	R-0h				

Table 20-97. ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R	0h	Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present. Reset type: SYSRST
4-0	RESERVED	R	0h	Reserved

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40 ADCPPB1TRIPHI Register (Offset = 1110h) [Reset = 00000000h]

ADCPPB1TRIPHI is shown in Figure 20-59 and described in Table 20-59.

Return to the Summary Table.

ADC PPB1 Trip High Register

Figure 20-59. ADCPPB1TRIPHI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITHI															
R-0h																R/W-0h															

Table 20-99. ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITHI	R/W	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPHI[15:13] will be ignored Reset type: SYSRST

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41 ADCPPB1TRIPLO Register (Offset = 1114h) [Reset = 00000000h]

ADCPPB1TRIPLO is shown in Figure 20-60 and described in Table 20-60.

Return to the Summary Table.

ADC PPB1 Trip Low/Trigger Time Stamp Register

Figure 20-60. ADCPPB1TRIPLO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITLO															
R-0h																R/W-0h															

Table 20-101. ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip High Low Limit. This value sets the digital comparator trip low limit if ADC PPB1TRIPLO.LIMITLO2EN = 1. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPLO[15:13] will be ignored. Reset type: SYSRST

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42 ADCPPB2CONFIG Register (Offset = 1120h) [Reset = 00000000h]

ADCPPB2CONFIG is shown in Figure 20-61 and described in Table 20-61.

Return to the Summary Table.

ADC PPB2 Config Register

Figure 20-61. ADCPPB2CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	CBCEN	RESERVED				
R/W-0h	R-0h	R/W-0h	R-0h				

Table 20-103. ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R	0h	Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present. Reset type: SYSRST
4-0	RESERVED	R	0h	Reserved

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43 ADCPPB2TRIPHI Register (Offset = 1130h) [Reset = 00000000h]

ADCPPB2TRIPHI is shown in Figure 20-62 and described in Table 20-62.

Return to the Summary Table.

ADC PPB2 Trip High Register

Figure 20-62. ADCPPB2TRIPHI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITHI															
R-0h																R/W-0h															

Table 20-105. ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITHI	R/W	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPHI[15:13] will be ignored Reset type: SYSRST

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44 ADCPPB2TRIPLO Register (Offset = 1134h) [Reset = 00000000h]

ADCPPB2TRIPLO is shown in Figure 20-63 and described in Table 20-63.

Return to the Summary Table.

ADC PPB2 Trip Low/Trigger Time Stamp Register

Figure 20-63. ADCPPB2TRIPLO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITLO															
R-0h																R/W-0h															

Table 20-107. ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip High Low Limit. This value sets the digital comparator trip low limit if ADC PPB2TRIPLO.LIMITLO2EN = 1. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPLO[15:13] will be ignored in 12 bit mode Reset type: SYSRST

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45 ADCPPB3CONFIG Register (Offset = 1140h) [Reset = 00000000h]

ADCPPB3CONFIG is shown in Figure 20-64 and described in Table 20-64.

Return to the Summary Table.

ADC PPB3 Config Register

Figure 20-64. ADCPPB3CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	CBCEN	RESERVED				
R/W-0h	R-0h	R/W-0h	R-0h				

Table 20-109. ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R	0h	Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present. Reset type: SYSRST
4-0	RESERVED	R	0h	Reserved

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46 ADCPPB3TRIPHI Register (Offset = 1150h) [Reset = 00000000h]

ADCPPB3TRIPHI is shown in Figure 20-65 and described in Table 20-65.

Return to the Summary Table.

ADC PPB3 Trip High Register

Figure 20-65. ADCPPB3TRIPHI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITHI															
R-0h																R/W-0h															

Table 20-111. ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITHI	R/W	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPHI[15:13] will be ignored Reset type: SYSRST

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47 ADCPPB3TRIPLO Register (Offset = 1154h) [Reset = 00000000h]

ADCPPB3TRIPLO is shown in Figure 20-66 and described in Table 20-66.

Return to the Summary Table.

ADC PPB3 Trip Low/Trigger Time Stamp Register

Figure 20-66. ADCPPB3TRIPLO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITLO															
R-0h																R/W-0h															

Table 20-113. ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip High Low Limit. This value sets the digital comparator trip low limit if ADC PPB3TRIPLO.LIMITLO2EN = 1. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPLO[15:13] will be ignored in 12 bit mode Reset type: SYSRST

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48 ADCPPB4CONFIG Register (Offset = 1160h) [Reset = 00000000h]

ADCPPB4CONFIG is shown in Figure 20-67 and described in Table 20-67.

Return to the Summary Table.

ADC PPB4 Config Register

Figure 20-67. ADCPPB4CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	CBCEN	RESERVED				
R/W-0h	R-0h	R/W-0h	R-0h				

Table 20-115. ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R	0h	Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present. Reset type: SYSRST
4-0	RESERVED	R	0h	Reserved

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49 ADCPPB4TRIPHI Register (Offset = 1170h) [Reset = 00000000h]

ADCPPB4TRIPHI is shown in Figure 20-68 and described in Table 20-68.

Return to the Summary Table.

ADC PPB4 Trip High Register

Figure 20-68. ADCPPB4TRIPHI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITHI															
R-0h																R/W-0h															

Table 20-117. ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITHI	R/W	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPHI[15:13] will be ignored Reset type: SYSRST

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50 ADCPPB4TRIPLO Register (Offset = 1174h) [Reset = 00000000h]

ADCPPB4TRIPLO is shown in Figure 20-69 and described in Table 20-69.

Return to the Summary Table.

ADC PPB4 Trip Low/Trigger Time Stamp Register

Figure 20-69. ADCPPB4TRIPLO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																LIMITLO															
R-0h																R/W-0h															

Table 20-119. ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip High Low Limit. This value sets the digital comparator trip low limit if ADC PPB4TRIPLO.LIMITLO2EN = 1. When comparing to an ADC PPBxRESULT register, the upper bits will be ignored: - TRIPLO[15:13] will be ignored in 12 bit mode Reset type: SYSRST

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51 ADCINTCYCLE Register (Offset = 1180h) [Reset = 00000000h]

ADCINTCYCLE is shown in Figure 20-70 and described in Table 20-70.

Return to the Summary Table.

ADC Early Interrupt Generation Cycle

Figure 20-70. ADCINTCYCLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DELAY					
R-0h																										R/W-0h					

Table 20-121. ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DELAY	R/W	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the Interrupt to be generated. Reset type: SYSRST

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52 ADCREV2 Register (Offset = 119Ch) [Reset = 00000006h]

ADCREV2 is shown in Figure 20-71 and described in Table 20-71.

Return to the Summary Table.

ADC Wrapper Revision Register

Figure 20-71. ADCREV2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRAPPERREV															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRAPPERREV								WRAPPERTYPE							
R-0h								R-6h							

Table 20-123. ADCREV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	WRAPPERREV	R	0h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h. Reset type: SYSRST
7-0	WRAPPERTYPE	R	6h	ADC Wrapper Type. Always set to 6 for this ADC. Reset type: SYSRST

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53 ADCPPB1LIMIT Register (Offset = 1200h) [Reset = 00000000h]

ADCPPB1LIMIT is shown in Figure 20-72 and described in Table 20-72.

Return to the Summary Table.

ADC PPB1Conversion Count Limit Register

Figure 20-72. ADCPPB1LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LIMIT	
R-0h														R/W-0h	

Table 20-125. ADCPPB1LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LIMIT	R/W	0h	Post Processing Block 1 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. 0 = No - accumulation 1 = 2 conversions are accumulated 2 = 4 conversions are accumulated 3 = 8 conversions are accumulated Reset type: SYSRST

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54 ADCPPB1PCOUNT Register (Offset = 1204h) [Reset = 00000000h]

ADCPPB1PCOUNT is shown in Figure 20-73 and described in Table 20-73.

Return to the Summary Table.

ADC PPB1 Partial Conversion Count Register

Figure 20-73. ADCPPB1PCOUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PCOUNT		
R-0h													R-0h		

Table 20-127. ADCPPB1PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	PCOUNT	R	0h	Post Processing Block 1 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADC PPB1PSUM this register is incremented by 1. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB1RESULT timing information). Reset type: SYSRST

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55 ADCPPB1CONFIG2 Register (Offset = 1208h) [Reset = 00000000h]

ADCPPB1CONFIG2 is shown in Figure 20-74 and described in Table 20-74.

Return to the Summary Table.

ADC PPB1 Sum Shift Register

Figure 20-74. ADCPPB1CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
COMPSEL	RESERVED		RESERVED	SWSYNC	RESERVED		SYNCINSEL
R/W-0h	R-0h		R/W-0h	R-0/W1S-0h	R-0h		R/W-0h
7	6	5	4	3	2	1	0
SYNCINSEL				RESERVED	SHIFT		
R/W-0h				R-0h	R/W-0h		

Table 20-129. ADCPPB1CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	COMPSEL	R/W	0h	Post Processing Block 1 Compare Source Select. This field determines whether ADC PPB1RESULT or ADC PPB1SUM is used for the threshold compare. 0 = ADC PPB1RESULT is used for compare logic 1 = ADC PPB1SUM is used for compare logic Reset type: SYSRST
14-13	RESERVED	R	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	SWSYNC	R-0/W1S	0h	PPB 1 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. Reset type: SYSRST
10-9	RESERVED	R	0h	Reserved
8-4	SYNCINSEL	R/W	0h	PPB 1 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details Reset type: SYSRST
3	RESERVED	R	0h	Reserved

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Table 20-129. ADCPPB1CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SHIFT	R/W	0h	Post Processing Block 1 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM >> 1 2 : SUM = PSUM >> 2 ... 7 : SUM = PSUM >> 7 Reset type: SYSRST

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56 ADCPPB1PSUM Register (Offset = 120Ch) [Reset = 00000000h]

ADCPPB1PSUM is shown in Figure 20-75 and described in Table 20-75.

Return to the Summary Table.

ADC PPB1 Partial Sum Register

Figure 20-75. ADCPPB1PSUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PSUM															
R-0h																R-0h															

Table 20-131. ADCPPB1PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	PSUM	R	0h	Post Processing Block 1 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADC PPB1RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for detailed timing information). Reset type: SYSRST

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57 ADCPPB2LIMIT Register (Offset = 1240h) [Reset = 00000000h]

ADCPPB2LIMIT is shown in Figure 20-76 and described in Table 20-76.

Return to the Summary Table.

ADC PPB2Conversion Count Limit Register

Figure 20-76. ADCPPB2LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LIMIT	
R-0h														R/W-0h	

Table 20-133. ADCPPB2LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LIMIT	R/W	0h	Post Processing Block 2 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. 0 = No - accumulation 1 = 2 conversions are accumulated 2 = 4 conversions are accumulated 3 = 8 conversions are accumulated Reset type: SYSRST

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58 ADCPPB2PCOUNT Register (Offset = 1244h) [Reset = 00000000h]

ADCPPB2PCOUNT is shown in Figure 20-77 and described in Table 20-77.

Return to the Summary Table.

ADC PPB2 Partial Conversion Count Register

Figure 20-77. ADCPPB2PCOUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PCOUNT		
R-0h													R-0h		

Table 20-135. ADCPPB2PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	PCOUNT	R	0h	Post Processing Block 2 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADC PPB2PSUM this register is incremented by 1. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB2RESULT timing information). Reset type: SYSRST

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59 ADCPPB2CONFIG2 Register (Offset = 1248h) [Reset = 00000000h]

ADCPPB2CONFIG2 is shown in Figure 20-78 and described in Table 20-78.

Return to the Summary Table.

ADC PPB2 Sum Shift Register

Figure 20-78. ADCPPB2CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
COMPSEL	RESERVED		RESERVED	SWSYNC	RESERVED		SYNCINSEL
R/W-0h	R-0h		R/W-0h	R-0/W1S-0h	R-0h		R/W-0h
7	6	5	4	3	2	1	0
SYNCINSEL				RESERVED	SHIFT		
R/W-0h				R-0h	R/W-0h		

Table 20-137. ADCPPB2CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	COMPSEL	R/W	0h	Post Processing Block 2 Compare Source Select. This field determines whether ADC PPB2RESULT or ADC PPB2SUM is used for the threshold compare. 0 = ADC PPB2RESULT is used for compare logic 1 = ADC PPB2SUM is used for compare logic Reset type: SYSRST
14-13	RESERVED	R	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	SWSYNC	R-0/W1S	0h	PPB 2 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. Reset type: SYSRST
10-9	RESERVED	R	0h	Reserved
8-4	SYNCINSEL	R/W	0h	PPB 2 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details Reset type: SYSRST
3	RESERVED	R	0h	Reserved

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Table 20-137. ADCPPB2CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SHIFT	R/W	0h	Post Processing Block 2 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM >> 1 2 : SUM = PSUM >> 2 ... 7 : SUM = PSUM >> 7 Reset type: SYSRST

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60 ADCPPB2PSUM Register (Offset = 124Ch) [Reset = 00000000h]

ADCPPB2PSUM is shown in Figure 20-79 and described in Table 20-79.

Return to the Summary Table.

ADC PPB2 Partial Sum Register

Figure 20-79. ADCPPB2PSUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PSUM															
R-0h																R-0h															

Table 20-139. ADCPPB2PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	PSUM	R	0h	Post Processing Block 2 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADC PPB2RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for detailed timing information). Reset type: SYSRST

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61 ADCPPB3LIMIT Register (Offset = 1280h) [Reset = 00000000h]

ADCPPB3LIMIT is shown in Figure 20-80 and described in Table 20-80.

Return to the Summary Table.

ADC PPB3Conversion Count Limit Register

Figure 20-80. ADCPPB3LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LIMIT	
R-0h														R/W-0h	

Table 20-141. ADCPPB3LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LIMIT	R/W	0h	Post Processing Block 3 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. 0 = No - accumulation 1 = 2 conversions are accumulated 2 = 4 conversions are accumulated 3 = 8 conversions are accumulated Reset type: SYSRST

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62 ADCPPB3PCOUNT Register (Offset = 1284h) [Reset = 00000000h]

ADCPPB3PCOUNT is shown in Figure 20-81 and described in Table 20-81.

Return to the Summary Table.

ADC PPB3 Partial Conversion Count Register

Figure 20-81. ADCPPB3PCOUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PCOUNT		
R-0h													R-0h		

Table 20-143. ADCPPB3PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	PCOUNT	R	0h	Post Processing Block 3 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADC PPB3PSUM this register is incremented by 1. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB3RESULT timing information). Reset type: SYSRST

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63 ADCPPB3CONFIG2 Register (Offset = 1288h) [Reset = 00000000h]

ADCPPB3CONFIG2 is shown in Figure 20-82 and described in Table 20-82.

Return to the Summary Table.

ADC PPB3 Sum Shift Register

Figure 20-82. ADCPPB3CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
COMPSEL	RESERVED		RESERVED	SWSYNC	RESERVED		SYNCINSEL
R/W-0h	R-0h		R/W-0h	R-0/W1S-0h	R-0h		R/W-0h
7	6	5	4	3	2	1	0
SYNCINSEL				RESERVED	SHIFT		
R/W-0h				R-0h	R/W-0h		

Table 20-145. ADCPPB3CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	COMPSEL	R/W	0h	Post Processing Block 3 Compare Source Select. This field determines whether ADC PPB3RESULT or ADC PPB3SUM is used for the threshold compare. 0 = ADC PPB3RESULT is used for compare logic 1 = ADC PPB3SUM is used for compare logic Reset type: SYSRST
14-13	RESERVED	R	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	SWSYNC	R-0/W1S	0h	PPB 3 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. Reset type: SYSRST
10-9	RESERVED	R	0h	Reserved
8-4	SYNCINSEL	R/W	0h	PPB 3 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details Reset type: SYSRST
3	RESERVED	R	0h	Reserved

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Table 20-145. ADCPPB3CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SHIFT	R/W	0h	Post Processing Block 3 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM >> 1 2 : SUM = PSUM >> 2 ... 7 : SUM = PSUM >> 7 Reset type: SYSRST

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64 ADCPPB3PSUM Register (Offset = 128Ch) [Reset = 00000000h]

ADCPPB3PSUM is shown in Figure 20-83 and described in Table 20-83.

Return to the Summary Table.

ADC PPB3 Partial Sum Register

Figure 20-83. ADCPPB3PSUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PSUM															
R-0h																R-0h															

Table 20-147. ADCPPB3PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	PSUM	R	0h	Post Processing Block 3 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADC PPB3RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for detailed timing information). Reset type: SYSRST

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65 ADCPPB4LIMIT Register (Offset = 12C0h) [Reset = 00000000h]

ADCPPB4LIMIT is shown in Figure 20-84 and described in Table 20-84.

Return to the Summary Table.

ADC PPB4Conversion Count Limit Register

Figure 20-84. ADCPPB4LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LIMIT	
R-0h														R/W-0h	

Table 20-149. ADCPPB4LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LIMIT	R/W	0h	Post Processing Block 4 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. 0 = No - accumulation 1 = 2 conversions are accumulated 2 = 4 conversions are accumulated 3 = 8 conversions are accumulated Reset type: SYSRST

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66 ADCPPB4PCOUNT Register (Offset = 12C4h) [Reset = 00000000h]

ADCPPB4PCOUNT is shown in Figure 20-85 and described in Table 20-85.

Return to the Summary Table.

ADC PPB4 Partial Conversion Count Register

Figure 20-85. ADCPPB4PCOUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													PCOUNT		
R-0h													R-0h		

Table 20-151. ADCPPB4PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	PCOUNT	R	0h	Post Processing Block 4 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADC PPB4PSUM this register is incremented by 1. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB4RESULT timing information). Reset type: SYSRST

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67 ADCPPB4CONFIG2 Register (Offset = 12C8h) [Reset = 00000000h]

ADCPPB4CONFIG2 is shown in Figure 20-86 and described in Table 20-86.

Return to the Summary Table.

ADC PPB4 Sum Shift Register

Figure 20-86. ADCPPB4CONFIG2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
COMPSEL	RESERVED		RESERVED	SWSYNC	RESERVED		SYNCINSEL
R/W-0h	R-0h		R/W-0h	R-0/W1S-0h	R-0h		R/W-0h
7	6	5	4	3	2	1	0
SYNCINSEL				RESERVED	SHIFT		
R/W-0h				R-0h	R/W-0h		

Table 20-153. ADCPPB4CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	COMPSEL	R/W	0h	Post Processing Block 4 Compare Source Select. This field determines whether ADC PPB4RESULT or ADC PPB4SUM is used for the threshold compare. 0 = ADC PPB4RESULT is used for compare logic 1 = ADC PPB4SUM is used for compare logic Reset type: SYSRST
14-13	RESERVED	R	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	SWSYNC	R-0/W1S	0h	PPB 4 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. Reset type: SYSRST
10-9	RESERVED	R	0h	Reserved
8-4	SYNCINSEL	R/W	0h	PPB 4 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details Reset type: SYSRST
3	RESERVED	R	0h	Reserved

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Table 20-153. ADCPPB4CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	SHIFT	R/W	0h	Post Processing Block 4 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM >> 1 2 : SUM = PSUM >> 2 ... 7 : SUM = PSUM >> 7 Reset type: SYSRST

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68 ADCPPB4PSUM Register (Offset = 12CCh) [Reset = 00000000h]

ADCPPB4PSUM is shown in Figure 20-87 and described in Table 20-87.

Return to the Summary Table.

ADC PPB4 Partial Sum Register

Figure 20-87. ADCPPB4PSUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																PSUM															
R-0h																R-0h															

Table 20-155. ADCPPB4PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	PSUM	R	0h	Post Processing Block 4 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADC PPB4RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs (PCOUNT = LIMIT) or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADC PPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for detailed timing information). Reset type: SYSRST

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69 ADCSEQCTL Register (Offset = 1320h) [Reset = 00000000h]

ADCSEQCTL is shown in Figure 20-88 and described in Table 20-88.

Return to the Summary Table.

ADC Sequencer common control Register

Figure 20-88. ADCSEQCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						SEQPREEMPT	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				SEQEND			
R-0h				R/W-0h			

Table 20-157. ADCSEQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	SEQPREEMPT	R/W	0h	SoC Sequence PREEMPT 0X: Pre-empt disabled 10: Pre-empt enabled and will not restart aborted Sequence 11: Pre-empt enabled and will restart aborted Sequence Reset type: SYSRST
15-4	RESERVED	R	0h	Reserved
3-0	SEQEND	R/W	0h	END SOC of last enabled sequence Reset type: SYSRST

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70 ADCSEQ1CONFIG Register (Offset = 1324h) [Reset = 00000200h]

ADCSEQ1CONFIG is shown in Figure 20-89 and described in Table 20-89.

Return to the Summary Table.

ADC Sequencer 1 Config register

Figure 20-89. ADCSEQ1CONFIG Register

31	30	29	28	27	26	25	24
SEQENABLE	SEQSWFRC	RESERVED					TRIGSEL
R/W-0h	R-0/W1S-0h	R-0h					R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	SEQSTART		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
SEQSTART	RESERVED				SAMPCAPRESETSEL	SAMPCAPRESETDISABLE	RESERVED
R/W-0h	R-0h				R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

Table 20-159. ADCSEQ1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEQENABLE	R/W	0h	SEQ1Enable Indicates whether the Sequence1 is enabled or not Reset type: SYSRST
30	SEQSWFRC	R-0/W1S	0h	Write 1 to force a trigger to Sequencer 1 regardless of the value of Hardware TRIGGER. Always reads 0. Reset type: SYSRST
29-25	RESERVED	R	0h	Reserved
24-20	TRIGSEL	R/W	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 0h ADCTRIG0 - Software only 1h - 31h Hardware triggers Reset type: SYSRST
19	RESERVED	R	0h	Reserved
18-15	SEQSTART	R/W	0h	Beginning SOC of SEQ1 Reset type: SYSRST
14-11	RESERVED	R	0h	Reserved
10	SAMPCAPRESETSEL	R/W	0h	SOC1 Sample Cap Reset Select : Resets sample cap after conversion to either vrefhi/2 or vreflo 0 - The sample cap is reset to Vreflo after each conversion 1 - The sample cap is reset to Vrefhi/2 after each conversion Reset type: SYSRST

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Table 20-159. ADCSEQ1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SAMPCAPRESETDISABLE	R/W	1h	SOC1 Sample Cap Reset enable : Resets sample cap after conversion. 0 - The sample cap is reset after each conversion 1 - The sample cap is not reset after each conversion Reset type: SYSRST
8	RESERVED	R	0h	Reserved
7-0	ACQPS	R/W	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for each SOC in this Seqeunce. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. S+H window values is defined based on a combonation of ACQPS[7:6] and ACQPS[5:0] values If ACQPS[7:6] value is "00" S+H window = ACQPS[5:0] + 1 sysclk cycles "01" S+H window = 64 + ((ACQPS[5:0] +1) * 2) sysclk cycles "10" S+H window = 192 + ((ACQPS[5:0] +1) * 4) sysclk cycles "11" S+H window = 448 + ((ACQPS[5:0] +1) * 16) sysclk cycles Reset type: SYSRST

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71 ADCSEQ2CONFIG Register (Offset = 1328h) [Reset = 00000200h]

ADCSEQ2CONFIG is shown in Figure 20-90 and described in Table 20-90.

Return to the Summary Table.

ADC Sequencer 2 Config register

Figure 20-90. ADCSEQ2CONFIG Register

31	30	29	28	27	26	25	24
SEQENABLE	SEQSWFRC	RESERVED					TRIGSEL
R/W-0h	R-0/W1S-0h	R-0h					R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	SEQSTART		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
SEQSTART	RESERVED				SAMPCAPRESETSEL	SAMPCAPRESETDISABLE	RESERVED
R/W-0h	R-0h				R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

Table 20-161. ADCSEQ2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEQENABLE	R/W	0h	SEQ2Enable Indicates whether the Sequence2 is enabled or not Reset type: SYSRST
30	SEQSWFRC	R-0/W1S	0h	Write 1 to force a trigger to Sequencer 2 regardless of the value of Hardware TRIGGER. Always reads 0. Reset type: SYSRST
29-25	RESERVED	R	0h	Reserved
24-20	TRIGSEL	R/W	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 0h ADCTRIG0 - Software only 1h - 31h Hardware triggers Reset type: SYSRST
19	RESERVED	R	0h	Reserved
18-15	SEQSTART	R/W	0h	Beginning SOC of SEQ2 Reset type: SYSRST
14-11	RESERVED	R	0h	Reserved
10	SAMPCAPRESETSEL	R/W	0h	SOC2 Sample Cap Reset Select : Resets sample cap after conversion to either vrefhi/2 or vreflo 0 - The sample cap is reset to Vreflo after each conversion 1 - The sample cap is reset to Vrefhi/2 after each conversion Reset type: SYSRST

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Table 20-161. ADCSEQ2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SAMPCAPRESETDISABLE	R/W	1h	SOC2 Sample Cap Reset enable : Resets sample cap after conversion. 0 - The sample cap is reset after each conversion 1 - The sample cap is not reset after each conversion Reset type: SYSRST
8	RESERVED	R	0h	Reserved
7-0	ACQPS	R/W	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for each SOC in this Seqeunce. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. S+H window values is defined based on a combonation of ACQPS[7:6] and ACQPS[5:0] values If ACQPS[7:6] value is "00" S+H window = ACQPS[5:0] + 1 sysclk cycles "01" S+H window = 64 + ((ACQPS[5:0] +1) * 2) sysclk cycles "10" S+H window = 192 + ((ACQPS[5:0] +1) * 4) sysclk cycles "11" S+H window = 448 + ((ACQPS[5:0] +1) * 16) sysclk cycles Reset type: SYSRST

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72 ADCSEQ3CONFIG Register (Offset = 132Ch) [Reset = 00000200h]

ADCSEQ3CONFIG is shown in Figure 20-91 and described in Table 20-91.

Return to the Summary Table.

ADC Sequencer 3 Config register

Figure 20-91. ADCSEQ3CONFIG Register

31	30	29	28	27	26	25	24
SEQENABLE	SEQSWFRC	RESERVED					TRIGSEL
R/W-0h	R-0/W1S-0h	R-0h					R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	SEQSTART		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
SEQSTART	RESERVED				SAMPCAPRESETSEL	SAMPCAPRESETDISABLE	RESERVED
R/W-0h	R-0h				R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

Table 20-163. ADCSEQ3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEQENABLE	R/W	0h	SEQ3Enable Indicates whether the Sequence3 is enabled or not Reset type: SYSRST
30	SEQSWFRC	R-0/W1S	0h	Write 1 to force a trigger to Sequencer 3 regardless of the value of Hardware TRIGGER. Always reads 0. Reset type: SYSRST
29-25	RESERVED	R	0h	Reserved
24-20	TRIGSEL	R/W	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 0h ADCTRIG0 - Software only 1h - 31h Hardware triggers Reset type: SYSRST
19	RESERVED	R	0h	Reserved
18-15	SEQSTART	R/W	0h	Beginning SOC of SEQ3 Reset type: SYSRST
14-11	RESERVED	R	0h	Reserved
10	SAMPCAPRESETSEL	R/W	0h	SOC3 Sample Cap Reset Select : Resets sample cap after conversion to either vrefhi/2 or vreflo 0 - The sample cap is reset to Vreflo after each conversion 1 - The sample cap is reset to Vrefhi/2 after each conversion Reset type: SYSRST

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Table 20-163. ADCSEQ3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SAMPCAPRESETDISABLE	R/W	1h	SOC3 Sample Cap Reset enable : Resets sample cap after conversion. 0 - The sample cap is reset after each conversion 1 - The sample cap is not reset after each conversion Reset type: SYSRST
8	RESERVED	R	0h	Reserved
7-0	ACQPS	R/W	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for each SOC in this Seqeunce. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. S+H window values is defined based on a combonation of ACQPS[7:6] and ACQPS[5:0] values If ACQPS[7:6] value is "00" S+H window = ACQPS[5:0] + 1 sysclk cycles "01" S+H window = 64 + ((ACQPS[5:0] +1) * 2) sysclk cycles "10" S+H window = 192 + ((ACQPS[5:0] +1) * 4) sysclk cycles "11" S+H window = 448 + ((ACQPS[5:0] +1) * 16) sysclk cycles Reset type: SYSRST

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73 ADCSEQ4CONFIG Register (Offset = 1330h) [Reset = 00000200h]

ADCSEQ4CONFIG is shown in Figure 20-92 and described in Table 20-92.

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ADC Sequencer 4 Config register

Figure 20-92. ADCSEQ4CONFIG Register

31	30	29	28	27	26	25	24
SEQENABLE	SEQSWFRC	RESERVED					TRIGSEL
R/W-0h	R-0/W1S-0h	R-0h					R/W-0h
23	22	21	20	19	18	17	16
TRIGSEL				RESERVED	SEQSTART		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
SEQSTART	RESERVED				SAMPCAPRESETSEL	SAMPCAPRESETDISABLE	RESERVED
R/W-0h	R-0h				R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
ACQPS							
R/W-0h							

Table 20-165. ADCSEQ4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SEQENABLE	R/W	0h	SEQ4Enable Indicates whether the Sequence4 is enabled or not Reset type: SYSRST
30	SEQSWFRC	R-0/W1S	0h	Write 1 to force a trigger to Sequencer 4 regardless of the value of Hardware TRIGGER. Always reads 0. Reset type: SYSRST
29-25	RESERVED	R	0h	Reserved
24-20	TRIGSEL	R/W	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 0h ADCTRIG0 - Software only 1h - 31h Hardware triggers Reset type: SYSRST
19	RESERVED	R	0h	Reserved
18-15	SEQSTART	R/W	0h	Beginning SOC of SEQ4 Reset type: SYSRST
14-11	RESERVED	R	0h	Reserved
10	SAMPCAPRESETSEL	R/W	0h	SOC4 Sample Cap Reset Select : Resets sample cap after conversion to either vrefhi/2 or vreflo 0 - The sample cap is reset to Vreflo after each conversion 1 - The sample cap is reset to Vrefhi/2 after each conversion Reset type: SYSRST

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Table 20-165. ADCSEQ4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SAMPCAPRESETDISABLE	R/W	1h	SOC4 Sample Cap Reset enable : Resets sample cap after conversion. 0 - The sample cap is reset after each conversion 1 - The sample cap is not reset after each conversion Reset type: SYSRST
8	RESERVED	R	0h	Reserved
7-0	ACQPS	R/W	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for each SOC in this Seqeunce. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. S+H window values is defined based on a combonation of ACQPS[7:6] and ACQPS[5:0] values If ACQPS[7:6] value is "00" S+H window = ACQPS[5:0] + 1 sysclk cycles "01" S+H window = 64 + ((ACQPS[5:0] +1) * 2) sysclk cycles "10" S+H window = 192 + ((ACQPS[5:0] +1) * 4) sysclk cycles "11" S+H window = 448 + ((ACQPS[5:0] +1) * 16) sysclk cycles Reset type: SYSRST

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20.14.3 ADC_LITE_RESULT_REGS Registers

Table 20-93 lists the memory-mapped registers for the ADC_LITE_RESULT_REGS registers. All register offset addresses not listed in Table 20-93 should be considered as reserved locations and the register contents should not be modified.

Table 20-166. ADC_LITE_RESULT_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	ADCRESULT0	ADC Result 0 Register		Go
2h	ADCRESULT1	ADC Result 1 Register		Go
4h	ADCRESULT2	ADC Result 2 Register		Go
6h	ADCRESULT3	ADC Result 3 Register		Go
8h	ADCRESULT4	ADC Result 4 Register		Go
Ah	ADCRESULT5	ADC Result 5 Register		Go
Ch	ADCRESULT6	ADC Result 6 Register		Go
Eh	ADCRESULT7	ADC Result 7 Register		Go
10h	ADCRESULT8	ADC Result 8 Register		Go
12h	ADCRESULT9	ADC Result 9 Register		Go
14h	ADCRESULT10	ADC Result 10 Register		Go
16h	ADCRESULT11	ADC Result 11 Register		Go
18h	ADCRESULT12	ADC Result 12 Register		Go
1Ah	ADCRESULT13	ADC Result 13 Register		Go
1Ch	ADCRESULT14	ADC Result 14 Register		Go
1Eh	ADCRESULT15	ADC Result 15 Register		Go
40h	ADCPPB1RESULT	ADC Post Processing Block 1 Result Register		Go
44h	ADCPPB2RESULT	ADC Post Processing Block 2 Result Register		Go
48h	ADCPPB3RESULT	ADC Post Processing Block 3 Result Register		Go
4Ch	ADCPPB4RESULT	ADC Post Processing Block 4 Result Register		Go
50h	ADCPPB1SUM	ADC PPB 1 Final Sum Result Register		Go
54h	ADCPPB1COUNT	ADC PPB1 Final Conversion Count Register		Go
58h	ADCPPB2SUM	ADC PPB 2 Final Sum Result Register		Go
5Ch	ADCPPB2COUNT	ADC PPB2 Final Conversion Count Register		Go
60h	ADCPPB3SUM	ADC PPB 3 Final Sum Result Register		Go
64h	ADCPPB3COUNT	ADC PPB3 Final Conversion Count Register		Go
68h	ADCPPB4SUM	ADC PPB 4 Final Sum Result Register		Go
6Ch	ADCPPB4COUNT	ADC PPB4 Final Conversion Count Register		Go
C0h	ADCSEQ1FIFORESULT	ADC Sequence 1 FIFO Result Register		Go
C4h	ADCSEQ2FIFORESULT	ADC Sequence 2 FIFO Result Register		Go
C8h	ADCSEQ3FIFORESULT	ADC Sequence 3 FIFO Result Register		Go
CCh	ADCSEQ4FIFORESULT	ADC Sequence 4 FIFO Result Register		Go
D0h	ADCSEQ1FIFOSTATUS	ADC Sequence 1 FIFO Status		Go
D4h	ADCSEQ2FIFOSTATUS	ADC Sequence 2 FIFO Status		Go
D8h	ADCSEQ3FIFOSTATUS	ADC Sequence 3 FIFO Status		Go
DCh	ADCSEQ4FIFOSTATUS	ADC Sequence 4 FIFO Status		Go

Complex bit access types are encoded to fit into small table cells. Table 20-94 shows the codes that are used for access types in this section.

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Table 20-167. ADC_LITE_RESULT_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 ADCRESULT0 Register (Offset = 0h) [Reset = 0000h]

ADCRESULT0 is shown in Figure 20-93 and described in Table 20-95.

Return to the Summary Table.

ADC Result 0 Register

Figure 20-93. ADCRESULT0 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-169. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 0 12-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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2 ADCRESULT1 Register (Offset = 2h) [Reset = 0000h]

ADCRESULT1 is shown in Figure 20-94 and described in Table 20-96.

Return to the Summary Table.

ADC Result 1 Register

Figure 20-94. ADCRESULT1 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-171. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 1 12-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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3 ADCRESULT2 Register (Offset = 4h) [Reset = 0000h]

ADCRESULT2 is shown in Figure 20-95 and described in Table 20-97.

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ADC Result 2 Register

Figure 20-95. ADCRESULT2 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-173. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 2 12-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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4 ADCRESULT3 Register (Offset = 6h) [Reset = 0000h]

ADCRESULT3 is shown in Figure 20-96 and described in Table 20-98.

Return to the Summary Table.

ADC Result 3 Register

Figure 20-96. ADCRESULT3 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-175. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 3 12-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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5 ADCRESULT4 Register (Offset = 8h) [Reset = 0000h]

ADCRESULT4 is shown in Figure 20-97 and described in Table 20-99.

Return to the Summary Table.

ADC Result 4 Register

Figure 20-97. ADCRESULT4 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-177. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 4 12-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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6 ADCRESULT5 Register (Offset = Ah) [Reset = 0000h]

ADCRESULT5 is shown in Figure 20-98 and described in Table 20-100.

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ADC Result 5 Register

Figure 20-98. ADCRESULT5 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-179. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 5 12-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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7 ADCRESULT6 Register (Offset = Ch) [Reset = 0000h]

ADCRESULT6 is shown in Figure 20-99 and described in Table 20-101.

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ADC Result 6 Register

Figure 20-99. ADCRESULT6 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-181. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 6 12-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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8 ADCRESULT7 Register (Offset = Eh) [Reset = 0000h]

ADCRESULT7 is shown in Figure 20-100 and described in Table 20-102.

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ADC Result 7 Register

Figure 20-100. ADCRESULT7 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-183. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 7 12-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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9 ADCRESULT8 Register (Offset = 10h) [Reset = 0000h]

ADCRESULT8 is shown in Figure 20-101 and described in Table 20-103.

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ADC Result 8 Register

Figure 20-101. ADCRESULT8 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-185. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 8 12-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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10 ADCRESULT9 Register (Offset = 12h) [Reset = 0000h]

ADCRESULT9 is shown in Figure 20-102 and described in Table 20-104.

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ADC Result 9 Register

Figure 20-102. ADCRESULT9 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-187. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 9 12-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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11 ADCRESULT10 Register (Offset = 14h) [Reset = 0000h]

ADCRESULT10 is shown in Figure 20-103 and described in Table 20-105.

Return to the Summary Table.

ADC Result 10 Register

Figure 20-103. ADCRESULT10 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-189. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 10 12-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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12 ADCRESULT11 Register (Offset = 16h) [Reset = 0000h]

ADCRESULT11 is shown in Figure 20-104 and described in Table 20-106.

Return to the Summary Table.

ADC Result 11 Register

Figure 20-104. ADCRESULT11 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-191. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 11 12-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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13 ADCRESULT12 Register (Offset = 18h) [Reset = 0000h]

ADCRESULT12 is shown in Figure 20-105 and described in Table 20-107.

Return to the Summary Table.

ADC Result 12 Register

Figure 20-105. ADCRESULT12 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-193. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 12 12-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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14 ADCRESULT13 Register (Offset = 1Ah) [Reset = 0000h]

ADCRESULT13 is shown in Figure 20-106 and described in Table 20-108.

Return to the Summary Table.

ADC Result 13 Register

Figure 20-106. ADCRESULT13 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-195. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 13 12-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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15 ADCRESULT14 Register (Offset = 1Ch) [Reset = 0000h]

ADCRESULT14 is shown in Figure 20-107 and described in Table 20-109.

Return to the Summary Table.

ADC Result 14 Register

Figure 20-107. ADCRESULT14 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-197. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 14 12-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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16 ADCRESULT15 Register (Offset = 1Eh) [Reset = 0000h]

ADCRESULT15 is shown in Figure 20-108 and described in Table 20-110.

Return to the Summary Table.

ADC Result 15 Register

Figure 20-108. ADCRESULT15 Register

15	14	13	12	11	10	9	8
RESULT							
R-0h							
7	6	5	4	3	2	1	0
RESULT							
R-0h							

Table 20-199. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESULT	R	0h	ADC Result 15 12-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field. If oversampling is enabled, Final SUM (After any Shift if enabled) will be stored in this register after completing the specified number of samples. Reset type: SYSRST

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17 ADCPPB1RESULT Register (Offset = 40h) [Reset = 00000000h]

ADCPPB1RESULT is shown in Figure 20-109 and described in Table 20-111.

Return to the Summary Table.

ADC Post Processing Block 1 Result Register

Figure 20-109. ADCPPB1RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																			PPBRESULT												
R-0h																			R-0h											

Table 20-201. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 12. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. Reset type: SYSRST
12-0	PPBRESULT	R	0h	ADC Post Processing Block Result 1 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for more detailed timing information). If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0. Reset type: SYSRST

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18 ADCPPB2RESULT Register (Offset = 44h) [Reset = 00000000h]

ADCPPB2RESULT is shown in Figure 20-110 and described in Table 20-112.

Return to the Summary Table.

ADC Post Processing Block 2 Result Register

Figure 20-110. ADCPPB2RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																			PPBRESULT												
R-0h																			R-0h											

Table 20-203. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 12. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. Reset type: SYSRST
12-0	PPBRESULT	R	0h	ADC Post Processing Block Result 2 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for more detailed timing information). If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0. Reset type: SYSRST

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19 ADCPPB3RESULT Register (Offset = 48h) [Reset = 00000000h]

ADCPPB3RESULT is shown in Figure 20-111 and described in Table 20-113.

Return to the Summary Table.

ADC Post Processing Block 3 Result Register

Figure 20-111. ADCPPB3RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																			PPBRESULT												
R-0h																			R-0h											

Table 20-205. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 12. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. Reset type: SYSRST
12-0	PPBRESULT	R	0h	ADC Post Processing Block Result 3 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for more detailed timing information). If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0. Reset type: SYSRST

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20 ADCPPB4RESULT Register (Offset = 4Ch) [Reset = 00000000h]

ADCPPB4RESULT is shown in Figure 20-112 and described in Table 20-114.

Return to the Summary Table.

ADC Post Processing Block 4 Result Register

Figure 20-112. ADCPPB4RESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																			PPBRESULT												
R-0h																			R-0h											

Table 20-207. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 12. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. Reset type: SYSRST
12-0	PPBRESULT	R	0h	ADC Post Processing Block Result 4 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results (in order from lowest numbered PPB to highest) will each become available every 2-3 SYSCLK cycles (refer to the TRM for more detailed timing information). If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0. Reset type: SYSRST

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21 ADCPPB1SUM Register (Offset = 50h) [Reset = 00000000h]

ADCPPB1SUM is shown in Figure 20-113 and described in Table 20-115.

Return to the Summary Table.

ADC PPB 1 Final Sum Result Register

Figure 20-113. ADCPPB1SUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																SUM															
R-0h																R-0h															

Table 20-209. ADCPPB1SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	SUM	R	0h	Post Processing Block 1 Oversampling Final Sum. When either a count-match event occurs (PCOUNT = LIMIT) or PPB1 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADC PPB1RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB1RESULT timing information). Reset type: SYSRST

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22 ADCPPB1COUNT Register (Offset = 54h) [Reset = 0000h]

ADCPPB1COUNT is shown in Figure 20-114 and described in Table 20-116.

Return to the Summary Table.

ADC PPB1 Final Conversion Count Register

Figure 20-114. ADCPPB1COUNT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				COUNT			
R-0h				R-0h			

Table 20-211. ADCPPB1COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	COUNT	R	0h	Post Processing Block 1 Oversampling Final Count. When either a count-match event occurs (PCOUNT = LIMIT) or PPB1 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADC PPB1RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB1RESULT timing information). Reset type: SYSRST

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23 ADCPPB2SUM Register (Offset = 58h) [Reset = 00000000h]

ADCPPB2SUM is shown in Figure 20-115 and described in Table 20-117.

Return to the Summary Table.

ADC PPB 2 Final Sum Result Register

Figure 20-115. ADCPPB2SUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																SUM															
R-0h																R-0h															

Table 20-213. ADCPPB2SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	SUM	R	0h	Post Processing Block 2 Oversampling Final Sum. When either a count-match event occurs (PCOUNT = LIMIT) or PPB2 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADC PPB2RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB2RESULT timing information). Reset type: SYSRST

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24 ADCPPB2COUNT Register (Offset = 5Ch) [Reset = 0000h]

ADCPPB2COUNT is shown in Figure 20-116 and described in Table 20-118.

Return to the Summary Table.

ADC PPB2 Final Conversion Count Register

Figure 20-116. ADCPPB2COUNT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				COUNT			
R-0h				R-0h			

Table 20-215. ADCPPB2COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	COUNT	R	0h	Post Processing Block 2 Oversampling Final Count. When either a count-match event occurs (PCOUNT = LIMIT) or PPB2 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADC PPB2RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB2RESULT timing information). Reset type: SYSRST

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25 ADCPPB3SUM Register (Offset = 60h) [Reset = 00000000h]

ADCPPB3SUM is shown in Figure 20-117 and described in Table 20-119.

Return to the Summary Table.

ADC PPB 3 Final Sum Result Register

Figure 20-117. ADCPPB3SUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																SUM															
R-0h																R-0h															

Table 20-217. ADCPPB3SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	SUM	R	0h	Post Processing Block 3 Oversampling Final Sum. When either a count-match event occurs (PCOUNT = LIMIT) or PPB3 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADC PPB3RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB3RESULT timing information). Reset type: SYSRST

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26 ADCPPB3COUNT Register (Offset = 64h) [Reset = 0000h]

ADCPPB3COUNT is shown in Figure 20-118 and described in Table 20-120.

Return to the Summary Table.

ADC PPB3 Final Conversion Count Register

Figure 20-118. ADCPPB3COUNT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				COUNT			
R-0h				R-0h			

Table 20-219. ADCPPB3COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	COUNT	R	0h	Post Processing Block 3 Oversampling Final Count. When either a count-match event occurs (PCOUNT = LIMIT) or PPB3 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADC PPB3RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB3RESULT timing information). Reset type: SYSRST

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27 ADCPPB4SUM Register (Offset = 68h) [Reset = 00000000h]

ADCPPB4SUM is shown in Figure 20-119 and described in Table 20-121.

Return to the Summary Table.

ADC PPB 4 Final Sum Result Register

Figure 20-119. ADCPPB4SUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIGN																SUM															
R-0h																R-0h															

Table 20-221. ADCPPB4SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 15. Reset type: SYSRST
15-0	SUM	R	0h	Post Processing Block 4 Oversampling Final Sum. When either a count-match event occurs (PCOUNT = LIMIT) or PPB4 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADC PPB4RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB4RESULT timing information). Reset type: SYSRST

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28 ADCPPB4COUNT Register (Offset = 6Ch) [Reset = 0000h]

ADCPPB4COUNT is shown in Figure 20-120 and described in Table 20-122.

Return to the Summary Table.

ADC PPB4 Final Conversion Count Register

Figure 20-120. ADCPPB4COUNT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				COUNT			
R-0h				R-0h			

Table 20-223. ADCPPB4COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	COUNT	R	0h	Post Processing Block 4 Oversampling Final Count. When either a count-match event occurs (PCOUNT = LIMIT) or PPB4 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADC PPB4RESULT is available (only in case of a count-match event). This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC (refer to the ADC PPB4RESULT timing information). Reset type: SYSRST

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29 ADCSEQ1FIFORESULT Register (Offset = C0h) [Reset = 00000000h]

ADCSEQ1FIFORESULT is shown in Figure 20-121 and described in Table 20-123.

Return to the Summary Table.

ADC Sequence 1 FIFO Result Register

Figure 20-121. ADCSEQ1FIFORESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQFIFORESULT																															
R-0h																															

Table 20-225. ADCSEQ1FIFORESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEQFIFORESULT	R	0h	Sequencer 1 Result in FIFO mode Reset type: SYSRST

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30 ADCSEQ2FIFORESULT Register (Offset = C4h) [Reset = 00000000h]

ADCSEQ2FIFORESULT is shown in Figure 20-122 and described in Table 20-124.

Return to the Summary Table.

ADC Sequence 2 FIFO Result Register

Figure 20-122. ADCSEQ2FIFORESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQFIFORESULT																															
R-0h																															

Table 20-227. ADCSEQ2FIFORESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEQFIFORESULT	R	0h	Sequencer 2 Result in FIFO mode Reset type: SYSRST

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31 ADCSEQ3FIFORESULT Register (Offset = C8h) [Reset = 00000000h]

ADCSEQ3FIFORESULT is shown in Figure 20-123 and described in Table 20-125.

Return to the Summary Table.

ADC Sequence 3 FIFO Result Register

Figure 20-123. ADCSEQ3FIFORESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQFIFORESULT																															
R-0h																															

Table 20-229. ADCSEQ3FIFORESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEQFIFORESULT	R	0h	Sequencer 3 Result in FIFO mode Reset type: SYSRST

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32 ADCSEQ4FIFORESULT Register (Offset = CCh) [Reset = 00000000h]

ADCSEQ4FIFORESULT is shown in Figure 20-124 and described in Table 20-126.

Return to the Summary Table.

ADC Sequence 4 FIFO Result Register

Figure 20-124. ADCSEQ4FIFORESULT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQFIFORESULT																															
R-0h																															

Table 20-231. ADCSEQ4FIFORESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEQFIFORESULT	R	0h	Sequencer 4 Result in FIFO mode Reset type: SYSRST

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33 ADCSEQ1FIFOSTATUS Register (Offset = D0h) [Reset = 00000000h]

ADCSEQ1FIFOSTATUS is shown in Figure 20-125 and described in Table 20-127.

Return to the Summary Table.

ADC Sequence 1 FIFO Status

Figure 20-125. ADCSEQ1FIFOSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			SEQFIFOPENDREAD				SEQFIFOVALID
R-0h			R-0h				R-0h

Table 20-233. ADCSEQ1FIFOSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-1	SEQFIFOPENDREAD	R	0h	Sequencer 1 FIFO pending reads Note: 1. This field is only updated when after the last byte of ADCSEQ1FIFORESULT is read. 2. The Pending read information will not be updated for debug reads. 3. Once all the data in the FIFO has been read, FIFO will wrap back. Subsequent reads will read from the beginning of the FIFO. Reset type: SYSRST
0	SEQFIFOVALID	R	0h	Sequencer 1 FIFO Valid 0 - All Conversions associated with the current Sequencer are NOT complete. 1 - Conversion from all the SOCs associated with the Sequencer are complete and result is available to be read. Reset type: SYSRST

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34 ADCSEQ2FIFOSTATUS Register (Offset = D4h) [Reset = 00000000h]

ADCSEQ2FIFOSTATUS is shown in Figure 20-126 and described in Table 20-128.

Return to the Summary Table.

ADC Sequence 2 FIFO Status

Figure 20-126. ADCSEQ2FIFOSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			SEQFIFOPENDREAD				SEQFIFOVALID
R-0h			R-0h				R-0h

Table 20-235. ADCSEQ2FIFOSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-1	SEQFIFOPENDREAD	R	0h	Sequencer 2 FIFO pending reads Note: 1. This field is only updated when after the last byte of ADCSEQ2FIFORESULT is read. 2. The Pending read information will not be updated for debug reads. 3. Once all the data in the FIFO has been read, FIFO will wrap back. Subsequent reads will read from the beginning of the FIFO. Reset type: SYSRST
0	SEQFIFOVALID	R	0h	Sequencer 2 FIFO Valid 0 - All Conversions associated with the current Sequencer are NOT complete. 1 - Conversion from all the SOCs associated with the Sequencer are complete and result is available to be read. Reset type: SYSRST

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35 ADCSEQ3FIFOSTATUS Register (Offset = D8h) [Reset = 00000000h]

ADCSEQ3FIFOSTATUS is shown in Figure 20-127 and described in Table 20-129.

Return to the Summary Table.

ADC Sequence 3 FIFO Status

Figure 20-127. ADCSEQ3FIFOSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			SEQFIFOPENDREAD				SEQFIFOVALID
R-0h			R-0h				R-0h

Table 20-237. ADCSEQ3FIFOSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-1	SEQFIFOPENDREAD	R	0h	Sequencer 3 FIFO pending reads Note: 1. This field is only updated when after the last byte of ADCSEQ3FIFORESULT is read. 2. The Pending read information will not be updated for debug reads. 3. Once all the data in the FIFO has been read, FIFO will wrap back. Subsequent reads will read from the beginning of the FIFO. Reset type: SYSRST
0	SEQFIFOVALID	R	0h	Sequencer 3 FIFO Valid 0 - All Conversions associated with the current Sequencer are NOT complete. 1 - Conversion from all the SOCs associated with the Sequencer are complete and result is available to be read. Reset type: SYSRST

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36 ADCSEQ4FIFOSTATUS Register (Offset = DCh) [Reset = 00000000h]

ADCSEQ4FIFOSTATUS is shown in Figure 20-128 and described in Table 20-130.

Return to the Summary Table.

ADC Sequence 4 FIFO Status

Figure 20-128. ADCSEQ4FIFOSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			SEQFIFOPENDREAD				SEQFIFOVALID
R-0h			R-0h				R-0h

Table 20-239. ADCSEQ4FIFOSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-1	SEQFIFOPENDREAD	R	0h	Sequencer 4 FIFO pending reads Note: 1. This field is only updated when after the last byte of ADCSEQ4FIFORESULT is read. 2. The Pending read information will not be updated for debug reads. 3. Once all the data in the FIFO has been read, FIFO will wrap back. Subsequent reads will read from the beginning of the FIFO. Reset type: SYSRST
0	SEQFIFOVALID	R	0h	Sequencer 4 FIFO Valid 0 - All Conversions associated with the current Sequencer are NOT complete. 1 - Conversion from all the SOCs associated with the Sequencer are complete and result is available to be read. Reset type: SYSRST

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Chapter 21

Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power, power factor correction, voltage trip monitoring, and so forth.

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21.5 Using the CMPSS 1327
21.6 CMPSS DAC Output 1329
21.7 CMPSS Registers 1330

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21.1 Introduction

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, and two digital filters. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from or by the PGA (see the *Analog Subsystem* chapter for mux options available to the CMPSS).. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required.

21.1.1 Features

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs (These DAC instances are 12-bit with a lower effective resolution as described in the data sheet)
- Two digital filters, max filter clock prescale = 2^{16}
- Ability to synchronize submodules with MCPWMSYNCPER
- Ability to synchronize output with MCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- VDDA is the DAC reference voltage
- Option to use the low comparator DAC output on an external pin (select instances only, mutually exclusive with use of comparator functionality)

21.1.2 CMPSS Related Collateral

Foundational Materials

- *Real-Time Control Reference Guide*
  - Refer to the Comparator section

Expert Materials

- *Peak Current Mode Controlled PSFB Converter Reference Design Using C2000™ Real-time MCU*
- *Understanding and Applying Current-Mode Control Theory Application Report*

21.1.3 CMPSS Block Diagram

The block diagram for the CMPSS is shown below.

- CTRIPx (x= "H" or "L") signals are connected to the PWM X-BAR for PWM trip response.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter for more details on the Output X-BAR mux configuration.
- CMP3_LITE_DACL is the low comparator DAC output that is available only in the CMPSS3 module. To enable this DAC output, set the CMPSSCTL.CMP3LDACOUTEN register field in SYSCTL.
- CMP4_LITE_DACL is the low comparator DAC output that is available only in the CMPSS4 module. To enable this DAC output, set the CMPSSCTL.CMP4LDACOUTEN register field in SYSCTL.

Note

Enabling the CMP[3:4]_LITE_DACLCMP3_LITE_DACL to a pin disables the functionality to the associated COMPL in CMPSS. In this case, the inverting input of the COMPL must come from the CMPx_LN input pin. All other functions of the CMPSS module are retained.

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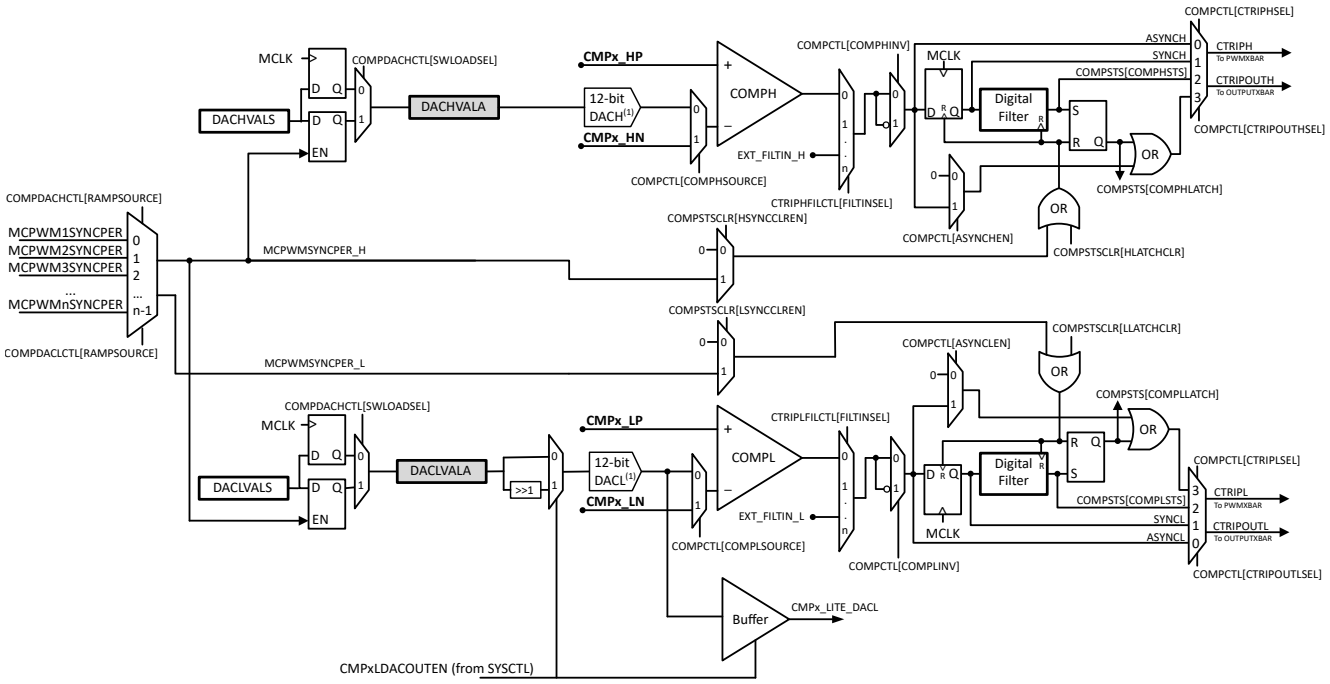


Figure 21-1. CMPSS_LITE Module Block Diagram

21.2 Comparator

The comparator generates a high digital output when the voltage on the positive input is greater than the voltage on the negative input, and a low digital output when the voltage on the positive input is less than the voltage on the negative input. The comparator is illustrated in Figure 21-2.

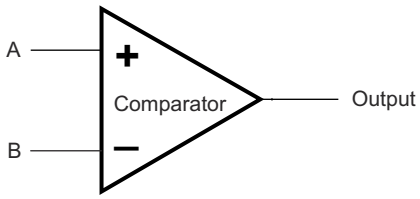


Figure 21-2. Comparator Block Diagram

Voltages	Output
Voltage A > Voltage B	1
Voltage A < Voltage B	0

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21.3 Reference DAC

Each 12-bit reference DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not useable, including the high DAC, both comparators, and the digital filters.

Two sets of DACxVAL registers, DACxVALA and DACxVALS, are present for each reference 12-bit DAC. DACxVALA is a read-only register that actively controls the reference 12-bit DAC value. DACxVALS is a writable shadow register that loads into DACxVALA either immediately or synchronized with the next MCPWMSYNCPER event.

The operating range of the reference 12-bit DAC is bounded by DACREF and VSSA. The reference 12-bit DAC is illustrated in Figure 21-3.

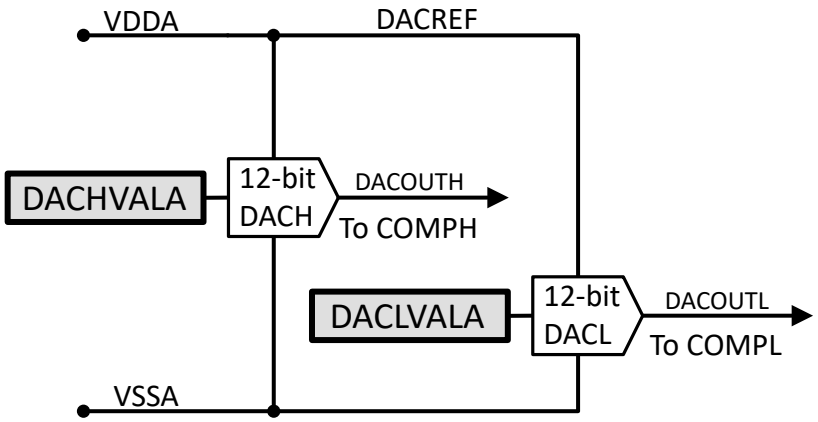


Figure 21-3. Reference DAC Block Diagram

The output of the reference 12-bit DAC can be calculated as:

$$DACOUT = \frac{(1 + DACVALA)*DACREF}{4096} \quad (24)$$

Note

- In the situations where both the DACH and DACL are driving the high and low comparators, a trip on one comparator can temporarily disturb the DAC output of the other comparator. The amount and length of time of this disturbance is specified in the device data sheet as “CMPSS DAC Output Disturbance” and “CMPSS DAC Disturbance Time”, respectively.

  Users must carefully design the system so that if the input signal crosses either DACH or DACL and trips the associated comparator, the input signal stays more than a “*CMPSS DAC output disturbance*” away from the other comparator trip point for the minimum length of “*CMPSS DAC disturbance time*”.
- If the user is not using DACL, the DACLVALS register must be set to 0 to avoid COMPL from affecting and tripping DACH. In this case, there is no limitation on the DACHVALS setting. Similarly, when not using DACH, the user must set DACHVALS to the maximum value.
- The CMPSS instance can be enabled before programming the reference DAC values.

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21.4 Digital Filter

The digital filter works on a window of FIFO samples (SAMPWIN) taken from the input. The filter output resolves to the majority value of the sample window, where majority is defined by the threshold (THRESH) value. If the majority threshold is not satisfied, the filter output remains unchanged.

For proper operation, the value of THRESH must be greater than SAMPWIN / 2 and less than or equal to SAMPWIN.

A prescale function (CLKPRESCALE) determines the filter sampling rate, where the filter FIFO captures one sample every prescaled system clock cycle. Old data from the FIFO is discarded.

Note that for SAMPWIN, THRESH, and CLKPRESCALE, the internal number used by the digital filter is + 1 in all cases. In essence, samples = SAMPWIN + 1, threshold = THRESH + 1 and prescale = CLKPRESCALE + 1.

A conceptual model of the digital filter is shown in Figure 21-4.

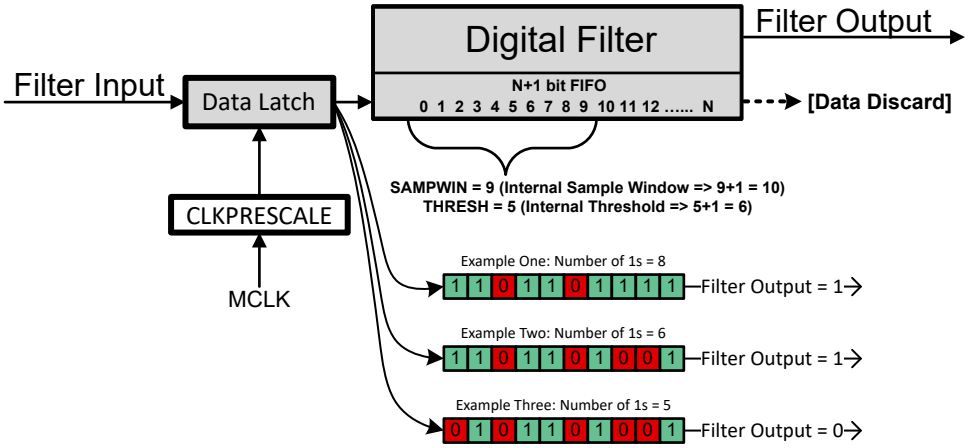


Figure 21-4. Digital Filter Behavior

Equivalent C code of the filter implementation is:

```
if (FILTER_OUTPUT == 0) {
    if (Num_1s_in_SAMPWIN >= THRESH) {
        FILTER_OUTPUT = 1;
    }
}
else {
    if (Num_0s_in_SAMPWIN >= THRESH) {
        FILTER_OUTPUT = 0;
    }
}
```


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21.4.1 Filter Initialization Sequence

For proper operation of the digital filter, the following initialization sequence is recommended:

1. Configure and enable the comparator for operation.
2. Configure the digital filter parameters for operation:
   - Set SAMPWIN for the number of samples to monitor in the FIFO window.
   - Set THRESH for the threshold required for majority qualification.
   - Set CLKPRESCALE for the digital filter clock prescale value.
3. Initialize the sample values in the digital FIFO window by setting FILINIT.
4. Clear COMPSTS latch using COMPSTSCLR, if the latched path is desired.
5. Configure the CTRIP and CTRIPOUT signal paths.
6. If desired, configure the destination module, for example, MCPWM, GPIO, and so on to accept the filtered signals.

21.5 Using the CMPSS

21.5.1 LATCHCLR, and MCPWMSYNCPER Signals

The LATCHCLR signal holds the digital filter, synchronization block, and the latch output in reset (0) after the required delays. The LATCHCLR signal is activated in software using xLATCHCLR (x = H or L). The LATCHCLR signal can also be activated by MCPWMSYNCPER when xSYNCCLREN (x = H or L) is set. If a longer LATCHCLR signal is required, the EPWMBLANK signal can be used to extend the LATCHCLR signal by setting BLANKEN.

MCPWMxSYNCPER comes from the Time-Base submodule of the MCPWM, respectively. For a detailed description of how these two signals are generated, refer to the Time Base Counter Synchronization subsection in the *Multi-Channel Pulse Width Modulator (MCPWM)* chapter.

The MCPWMxSYNCPER signal that loads DACxVALA when COMPDACCTL[SWLOADSEL] = 1 is a level trigger load. If TBCTR and TBPRD of the MCPWM are both 0, MCPWMSYNCPER is held at level high and DACxVALA is loaded immediately from DACxVALS irrespective of the value of COMPDACCTL[SWLOADSEL]. Due to this, configure the MCPWM first before setting COMPDACCTL[SWLOADSEL] to 1.

Note

The name of the sync signal that the CMPSS receives from the MCPWM is referred to as MCPWMSYNCPER, PWMSYNCPER, and MCPWMxSYNCPER interchangeably in this document.

21.5.2 Synchronizer, Digital Filter, and Latch Delays

The synchronization block adds 1-2 MCLK cycle delays. If the digital filter is bypassed (all filter settings are 0), the digital filter adds 2 MCLK cycle delays. The latch adds 1 MCLK cycle delay.

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21.5.3 Calibrating the CMPSS

The CMPSS has two sources of offset errors: comparator offset error and compdac offset error. In the data sheet, the comparator offset error is referred to as ***Input referred offset error*** and compdac offset error is referred to as ***Static offset error***. See the device data sheet for the values.

If both inputs of the comparator are driven from a pin, only the comparator offset error applies. However if the inverting input of the comparator is driven from the compdac, then only the compdac offset error applies. This is because the compdac offset error includes comparator offset error.

Due to the offset errors, the CMPSS must be calibrated to make sure trips happen at the expected levels. The following flow outlines how the calibration can be performed if the inverting input of the comparator is driven from the compdac.

Notes before calibration:

1. A static DC signal is required on the non-inverting input of the comparator.
2. Hysteresis can be disabled for calibration and can be re-enabled after calibration is complete.
3. A noisy input can make calibration difficult, so use the latch with non-zero filter settings depending on how noisy is the signal on the non-inverting input.

This approach sweeps down the compdac:

1. Set the starting compdac value to max, 0xFFF.
   - Optional: Instead of setting the starting compdac value to maximum, set to ***Vtarget*** + ***Static offset error*** + ***Margin***. Where ***Vtarget*** is the approximate DC voltage on the non-inverting input, ***Static offset error*** is the compdac offset error specification and ***Margin*** is some amount of guard band. This can lead to a faster calibration but only works if ***Vtarget*** is known. Alternatively, if ***Vtarget*** is unknown, the ADC can be used to convert ***Vtarget***.
2. Decrement compdac value by 1.
3. Wait for compdac to settle.
4. Clear latch.
5. Wait for possible latch set.
6. If latch is set, trip code is found exit.
   - Optional: The trip code can be double checked by:
     a. Increasing compdac value by 1.
     b. Clear latch.
     c. Wait for possible latch set.
     d. Latch can be unset.
7. If latch is unset, go back to step 2 and repeat.

It is also possible to calibrate the CMPSS, if both inputs of the comparator are driven from a pin. For this case, the flow stays the same but the voltage on the inverting pin of the comparator is swept externally.

21.5.4 Enabling and Disabling the CMPSS Clock

If the clock to the CMPSS module is disabled while the comparator is active, the following behavior can be expected:

- The comparator remains unaffected and continues to trip from voltages on the inputs.
- If the reference 12-bit DAC is driving the negative input of the comparator, the voltage on the negative input remains static and unaffected but DACxVALA can no longer be updated from the ramp generator or DACxVALS.
- The ramp generator, synchronize block and digital filter freeze on the current states.

Enabling the clock to the CMPSS restores the clock to the state before the clock was disabled.

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21.6 CMPSS DAC Output

Select instances of the CMPSS_LITE module can optionally route the low DAC output to an external pin to be used as an external DAC. This is subject to the following constraints:

- This is available only on select instances; consult the device data sheet to determine if the CMPSS DAC has been pinned out for a particular instance.
- In this case, the DAC output is not available to the COMPL inside the CMPSS module. The negative input to COMPL must be driven from the device pin in this case, if used. All other CMPSS module functionality, including the COMPH DAC source, is usable in this case.
- See the device data sheet for effective resolution of the CMPSS DAC output.

Note

The CMPSS low DAC output does not necessarily appear on the same pins that are available for low comparator input. Consult the pinout of the device data sheet to determine which pin the CMPSS output DAC is available on.

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21.7 CMPSS Registers

This Section describes the CMPSS Registers.

21.7.1 CMPSS Base Address Table

Table 21-1. CMPSS Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Cmpss0Regs	CMPSS_LITE_REGS	CMPSS0	0x4046_0000
Cmpss1Regs	CMPSS_LITE_REGS	CMPSS1	0x4046_1000
Cmpss2Regs	CMPSS_LITE_REGS	CMPSS2	0x4046_2000
Cmpss3Regs	CMPSS_LITE_REGS	CMPSS3	0x4046_3000

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21.7.2 CMPSS_LITE_REGS Registers

Table 21-2 lists the memory-mapped registers for the CMPSS_LITE_REGS registers. All register offset addresses not listed in Table 21-2 should be considered as reserved locations and the register contents should not be modified.

Table 21-2. CMPSS_LITE_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	COMPCTL	CMPSS Comparator Control Register		Go
2h	COMPHYSCTL	CMPSS Comparator Hysteresis Control Register		Go
4h	COMPSTS	CMPSS Comparator Status Register		Go
6h	COMPSTSCLR	CMPSS Comparator Status Clear Register		Go
8h	COMPDACHCTL	CMPSS High DAC Control Register		Go
Ch	DACHVALS	CMPSS High DAC Value Shadow Register		Go
Eh	DACHVALA	CMPSS High DAC Value Active Register		Go
24h	DACLVALS	CMPSS Low DAC Value Shadow Register		Go
26h	DACLVALA	CMPSS Low DAC Value Active Register		Go
2Ch	CTRIPLFILCTL	CTRIPL Filter Control Register		Go
2Eh	CTRIPLFILCLKCTL	CTRIPL Filter Clock Control Register		Go
30h	CTRIPHFILCTL	CTRIPH Filter Control Register		Go
32h	CTRIPHFILCLKCTL	CTRIPH Filter Clock Control Register		Go
34h	COMPLOCK	CMPSS Lock Register		Go
48h	COMPDACLCTL	CMPSS Low DAC Control Register		Go
6Eh	CTRIPLFILCLKCTL2	CTRIPL Filter Clock Control Register 2		Go
72h	CTRIPHFILCLKCTL2	CTRIPH Filter Clock Control Register 2		Go

Complex bit access types are encoded to fit into small table cells. Table 21-3 shows the codes that are used for access types in this section.

Table 21-3. CMPSS_LITE_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value

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1 COMPCTL Register (Offset = 0h) [Reset = 0000h]

COMPCTL is shown in Figure 21-5 and described in Table 21-4.

Return to the Summary Table.

CMPSS Comparator Control Register

Figure 21-5. COMPCTL Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	COMPLSOURCE
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	COMPHSOURCE
R-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h

Table 21-5. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled Reset type: SYSRSn
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset type: SYSRSn
13-12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL Reset type: SYSRSn
11-10	CTRIPLSEL	R/W	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL Reset type: SYSRSn
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset type: SYSRSn
8	COMPLSOURCE	R/W	0h	Low comparator input source. 0 Inverting input of comparator driven by internal DAC 1 Inverting input of comparator driven through external pin Reset type: SYSRSn
7	RESERVED	R	0h	Reserved

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Table 21-5. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ASYNCHEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output Reset type: SYSRSn
5-4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH Reset type: SYSRSn
3-2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH Reset type: SYSRSn
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted Reset type: SYSRSn
0	COMPHSOURCE	R/W	0h	High comparator input source. 0 Inverting input of comparator driven by internal DAC 1 Inverting input of comparator driven through external pin Reset type: SYSRSn

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2 COMPHYSCTL Register (Offset = 2h) [Reset = 0000h]

COMPHYSCTL is shown in Figure 21-6 and described in Table 21-5.

Return to the Summary Table.

CMPSS Comparator Hysteresis Control Register

Figure 21-6. COMPHYSCTL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				COMPHYS			
R-0h				R/W-0h			

Table 21-7. COMPHYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	COMPHYS	R/W	0h	Comparator hysteresis. Sets the amount of hysteresis on the comparator inputs. 0 None 1 Set to typical hysteresis 2 Set to 2x of typical hysteresis 3 Set to 3x of typical hysteresis 4 Set to 4x of typical hysteresis others : undefined Reset type: SYSRSn

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3 COMPSTS Register (Offset = 4h) [Reset = 0000h]

COMPSTS is shown in Figure 21-7 and described in Table 21-6.

Return to the Summary Table.

CMPSS Comparator Status Register

Figure 21-7. COMPSTS Register

15	14	13	12	11	10	9	8
RESERVED						COMPLLATCH	COMPLSTS
R-0h						R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED						COMPHLATCH	COMPHSTS
R-0h						R-0h	R-0h

Table 21-9. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	COMPLLATCH	R	0h	Latched value of low comparator digital filter output Reset type: SYSRSn
8	COMPLSTS	R	0h	Low comparator digital filter output Reset type: SYSRSn
7-2	RESERVED	R	0h	Reserved
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output Reset type: SYSRSn
0	COMPHSTS	R	0h	High comparator digital filter output Reset type: SYSRSn

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4 COMPSTSCLR Register (Offset = 6h) [Reset = 0000h]

COMPSTSCLR is shown in Figure 21-8 and described in Table 21-7.

Return to the Summary Table.

CMPSS Comparator Status Clear Register

Figure 21-8. COMPSTSCLR Register

15	14	13	12	11	10	9	8
RESERVED					LSYNCCLREN	LLATCHCLR	RESERVED
R-0h					R/W-0h	R-0/W1S-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED					HSYNCCLREN	HLATCHCLR	RESERVED
R-0h					R/W-0h	R-0/W1S-0h	R-0h

Table 21-11. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	LSYNCCLREN	R/W	0h	Low comparator latch PWMSYNCPER clear. Enable PWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 PWMSYNCPER will not reset latch 1 PWMSYNCPER will reset latch Reset type: SYSRSn
9	LLATCHCLR	R-0/W1S	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH] Reset type: SYSRSn
8-3	RESERVED	R	0h	Reserved
2	HSYNCCLREN	R/W	0h	High comparator latch PWMSYNCPER clear. Enable PWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 PWMSYNCPER will not reset latch 1 PWMSYNCPER will reset latch Reset type: SYSRSn
1	HLATCHCLR	R-0/W1S	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH] Reset type: SYSRSn
0	RESERVED	R	0h	Reserved

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5 COMPDACHCTL Register (Offset = 8h) [Reset = 0000h]

COMPDACHCTL is shown in Figure 21-9 and described in Table 21-8.

Return to the Summary Table.

CMPSS High DAC Control Register

Figure 21-9. COMPDACHCTL Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	RESERVED	RESERVED			
R/W-0h		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
SWLOADSEL	RESERVED	RESERVED	RAMPSOURCE				RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h

Table 21-13. COMPDACHCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	0h	Reserved
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or MCPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on MCPWMSYNCPER Reset type: SYSRSn
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4-1	RAMPSOURCE	R/W	0h	MCPWMSYNCPER source select. Determines which MCPWMnSYNCPER signal is used within the COMPH Where n represents the maximum number of MCPWMSYNCPER signals available on the device: 0 MCPWM1SYNCPER 1 MCPWM2SYNCPER 2 MCPWM3SYNCPER ... n-1 MCPWMnSYNCPER Reset type: SYSRSn
0	RESERVED	R/W	0h	Reserved

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6 DACHVALS Register (Offset = Ch) [Reset = 0000h]

DACHVALS is shown in Figure 21-10 and described in Table 21-9.

Return to the Summary Table.

CMPSS High DAC Value Shadow Register

Figure 21-10. DACHVALS Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W-0h							

Table 21-15. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset type: SYSRSn

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7 DACHVALA Register (Offset = Eh) [Reset = 0000h]

DACHVALA is shown in Figure 21-11 and described in Table 21-10.

Return to the Summary Table.

CMPSS High DAC Value Active Register

Figure 21-11. DACHVALA Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
R-0h				R-0h			
7	6	5	4	3	2	1	0
DACVAL							
R-0h							

Table 21-17. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC. Reset type: SYSRSn

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8 DACLVALS Register (Offset = 24h) [Reset = 0000h]

DACLVALS is shown in Figure 21-12 and described in Table 21-11.

Return to the Summary Table.

CMPSS Low DAC Value Shadow Register

Figure 21-12. DACLVALS Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
DACVAL							
R/W-0h							

Table 21-19. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. Reset type: SYSRSn

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9 DACLVALA Register (Offset = 26h) [Reset = 0000h]

DACLVALA is shown in Figure 21-13 and described in Table 21-12.

Return to the Summary Table.

CMPSS Low DAC Value Active Register

Figure 21-13. DACLVALA Register

15	14	13	12	11	10	9	8
RESERVED				DACVAL			
R-0h				R-0h			
7	6	5	4	3	2	1	0
DACVAL							
R-0h							

Table 21-21. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC. Reset type: SYSRSn

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10 CTRIPLFILCTL Register (Offset = 2Ch) [Reset = 0000h]

CTRIPLFILCTL is shown in Figure 21-14 and described in Table 21-13.

Return to the Summary Table.

CTRIPL Filter Control Register

Figure 21-14. CTRIPLFILCTL Register

15	14	13	12	11	10	9	8
FILINIT	THRESH						SAMPWIN
R-0/W1S-0h	R/W-0h						R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN						FILTINSEL	
R/W-0h						R/W-0h	

Table 21-23. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset type: SYSRSn
8-3	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
2-0	FILTINSEL	R/W	0h	Low filter Input Mux Select Bit 0 Selects the COMPL output as the filter input 1 Selects the external signal EXT_FILTIN_L[1] as the filter input 2 Selects the external signal EXT_FILTIN_L[2] as the filter input ... ... 7 Selects the external signal EXT_FILTIN_L[7] as the filter input Reset type: SYSRSn

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11 CTRIPLFILCLKCTL Register (Offset = 2Eh) [Reset = 0000h]

CTRIPLFILCLKCTL is shown in Figure 21-15 and described in Table 21-14.

Return to the Summary Table.

CTRIPL Filter Clock Control Register

Figure 21-15. CTRIPLFILCLKCTL Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W-0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 21-25. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset type: SYSRSn

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12 CTRIPHFILCTL Register (Offset = 30h) [Reset = 0000h]

CTRIPHFILCTL is shown in Figure 21-16 and described in Table 21-15.

Return to the Summary Table.

CTRIPH Filter Control Register

Figure 21-16. CTRIPHFILCTL Register

15	14	13	12	11	10	9	8
FILINIT	THRESH						SAMPWIN
R-0/W1S-0h	R/W-0h						R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN						FILTINSEL	
R/W-0h						R/W-0h	

Table 21-27. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. Reset type: SYSRSn
8-3	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
2-0	FILTINSEL	R/W	0h	High filter Input Mux Select Bit 0 Selects the COMPL output as the filter input 1 Selects the external signal EXT_FILTIN_H[1] as the filter input 2 Selects the external signal EXT_FILTIN_H[2] as the filter input ... ... 7 Selects the external signal EXT_FILTIN_H[7] as the filter input Reset type: SYSRSn

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13 CTRIPHFILCLKCTL Register (Offset = 32h) [Reset = 0000h]

CTRIPHFILCLKCTL is shown in Figure 21-17 and described in Table 21-16.

Return to the Summary Table.

CTRIPH Filter Clock Control Register

Figure 21-17. CTRIPHFILCLKCTL Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W-0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 21-29. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. Reset type: SYSRSn

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14 COMPLOCK Register (Offset = 34h) [Reset = 0000h]

COMPLOCK is shown in Figure 21-18 and described in Table 21-17.

Return to the Summary Table.

CMPSS Lock Register

Figure 21-18. COMPLOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	CTRIP	DACCTL	COMPHYSCTL	COMPCTL
R-0h			R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h	R/WSonce-0h

Table 21-31. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R/WSonce	0h	Reserved
3	CTRIP	R/WSonce	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL* registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL* registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL* registers are locked. Only a system reset can clear this bit. Reset type: SYSRSn
2	DACCTL	R/WSonce	0h	Lock write-access to the COMPDAC*CTL* register(s). 0 COMPDAC*CTL* register(s) not locked. Write 0 to this bit has no effect. 1 COMPDAC*CTL* register(s) locked. Only a system reset can clear this bit. Reset type: SYSRSn
1	COMPHYSCTL	R/WSonce	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn
0	COMPCTL	R/WSonce	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn

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15 COMPDACLCTL Register (Offset = 48h) [Reset = 0000h]

COMPDACLCTL is shown in Figure 21-19 and described in Table 21-18.

Return to the Summary Table.

CMPSS Low DAC Control Register

Figure 21-19. COMPDACLCTL Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	RESERVED	RESERVED			
R-0h		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RAMPSOURCE				RESERVED
R-0h	R/W-0h	R-0h	R/W-0h				R/W-0h

Table 21-33. COMPDACLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R	0h	Reserved
4-1	RAMPSOURCE	R/W	0h	MCPWMSYNCPER source select. Determines which MCPWMnSYNCPER signal is used within the COMPL Where n represents the maximum number of MCPWMSYNCPER signals available on the device: 0 MCPWM1SYNCPER 1 MCPWM2SYNCPER 2 MCPWM3SYNCPER ... n-1 MCPWMnSYNCPER Reset type: SYSRSn
0	RESERVED	R/W	0h	Reserved

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16 CTRIPLFILCLKCTL2 Register (Offset = 6Eh) [Reset = 0000h]

CTRIPLFILCLKCTL2 is shown in Figure 21-20 and described in Table 21-19.

Return to the Summary Table.

CTRIPL Filter Clock Control Register 2

Figure 21-20. CTRIPLFILCLKCTL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CLKPRESCALEU							
R/W-0h							

Table 21-35. CTRIPLFILCLKCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	CLKPRESCALEU	R/W	0h	COMP Low filter sample clock prescale Upper Bits. The effective prescale value is (CLKPRESCALEH:CLKPRESCALE)+1 Reset type: SYSRSn

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17 CTRIPHFILCLKCTL2 Register (Offset = 72h) [Reset = 0000h]

CTRIPHFILCLKCTL2 is shown in Figure 21-21 and described in Table 21-20.

Return to the Summary Table.

CTRIPH Filter Clock Control Register 2

Figure 21-21. CTRIPHFILCLKCTL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CLKPRESCALEU							
R/W-0h							

Table 21-37. CTRIPHFILCLKCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	CLKPRESCALEU	R/W	0h	COMP High filter sample clock prescale Upper Bits. The effective prescale value is (CLKPRESCALEH:CLKPRESCALE)+1 Reset type: SYSRSn

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Chapter 22

Programmable Gain Amplifier (PGA)

The Programmable Gain Amplifier (PGA) is used to amplify an input voltage for the purpose of increasing the dynamic range of the downstream ADC and CMPSS modules.

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22.1 Programmable Gain Amplifier (PGA) Overview

The integrated PGA helps to reduce cost and design effort for many control applications that traditionally require external, standalone amplifiers. On-chip integration makes sure that the PGA is compatible with the downstream analog-to-digital converter (ADC) and comparator subsystem (CMPSS) modules. Software selectable gain, filter settings, and different operational modes make the PGA adaptable to various performance needs.

22.1.1 Features

Features available to PGA modules are:

- Rail to rail input and output voltage within VDDA and VSSA range
- Programmable gain modes including unity gain and other values from x2 to x64
- Standalone gain mode using off-chip passive components
- Post-gain filtering using on-chip resistors
- Differential input support
- Hardware assisted chopping for offset reduction
- Support for Kelvin ground connections using PGA_INM pins
- 4-to-1 mux on positive input pins
- 4-to-1 mux on negative input pins

22.1.2 Block Diagram

Figure 22-1 shows the block diagram of the PGA. The active component in the PGA is an embedded operational amplifier (op-amp) that is configurable as a non-inverting or inverting amplifier with internal feedback resistors. These internal feedback resistor values are paired to produce software selectable voltage gains.

Six PGA signals are available at the device pins:

- PGA_INP0 through PGA_INP8 are multiplexed to get the positive input to the PGA op-amp.
- PGA_INM0 through PGA_INM3 are multiplexed to get the negative input to the PGA op-amp.
- PGA_OUT supports op-amp output filtering with RC components. The filtered signal is available for sampling and monitoring by on-chip ADC and CMPSS modules.

Note

PGA_OUT_INT is an internal signal at the op-amp output, which is available for sampling and monitoring by the internal ADC and CMPSS modules.

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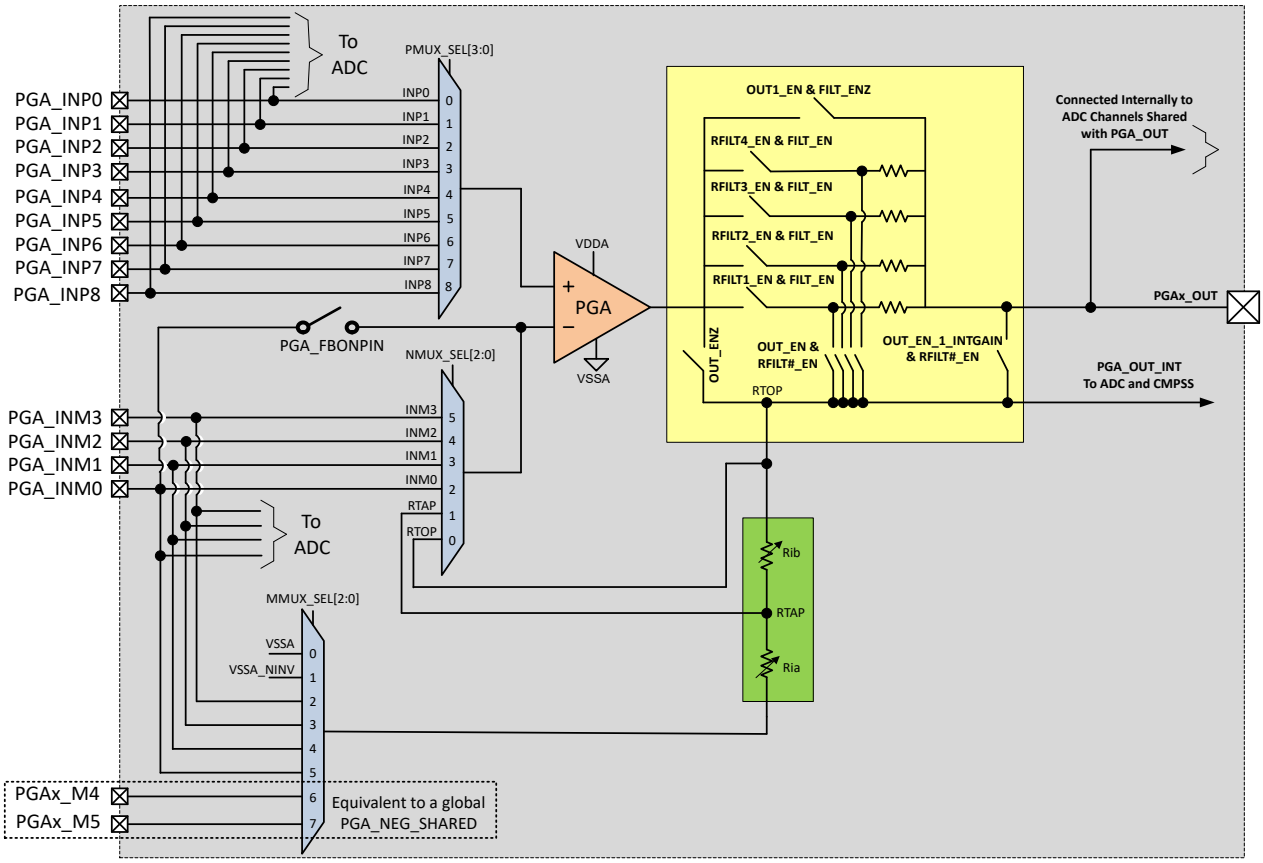


Figure 22-1. PGA Block Diagram

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22.2 Linear Output Range

The absolute output range of the PGA is bounded by the analog VDDA and VSSA supplies – the PGA cannot produce output voltages greater than VDDA or less than VSSA.

Although the PGA can produce full-scale output across the absolute voltage range of VSSA to VDDA, the amplifier output is only linear within a subset of the absolute range. This reduced range is referred to as the linear output range.

The PGA performance specifications in the device data sheet only apply to the linear output range. For best performance, the input signal can be conditioned in such a way that the PGA stays within the linear output range during normal system operation.

Note

The voltage input range required to operate the PGA in the linear output range is unique for each gain mode. See the device data sheet for the linear output range.

22.3 Gain Values

Gain values of PGA are software-selectable using the PGACTL[GAIN] register field. The gain of the PGA in the subtractor and non-inverting modes is determined by a preset ratio between resistors R_{ia} and R_{ib}.

The target values for the gain resistors for subtractor and non-inverting modes are shown in Table 22-1.

Table 22-1. Different Gain Values and Corresponding Resistor Values

PGACTL[GAIN]	Non-inverting Gain	Inverting Gain	R_{ia}	R_{ib}
000	1	NA	256K	0(1)
001	2	-1	16K	16K
010	4	-3	8K	24K
011	8	-7	8K	56K
100	16	-15	8K	120K
101	32	-31	8K	248K
110	64	-63	4K	252K

(1) These values are nominal; tolerance is specified in electrical spec table given in the device data sheet.

Note

Changing the gain mode during normal operation is allowed, but a minimum configuration settling time can be observed when doing so. See the device data sheet for the gain switch settling time.

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22.4 Modes of Operation

PGA can support four different operational modes based on the values in MUXSEL register, which are given in Table 22-2:

1. Buffer mode: PGA works in unity gain mode.
2. Standalone mode: PGA operates as a conventional op-amp.
3. Non-inverting mode: PGA works as a non-inverting op-amp.
4. Subtractor mode: PGA output voltage equals to the subtraction of the two inputs.

Table 22-2. Modes of Operation

Mode	MUXSEL[PMUXSEL]	MUXSEL[NMUXSEL]	MUXSEL[MMUXSEL]
Buffer mode	0	0	0
Standalone mode	0	2	0
Non-inverting mode	0	1	1
Subtractor mode	0	1	2 or 3

22.4.1 Buffer Mode

In this mode, PGA provides a high input impedance, low output impedance, and a voltage gain of approximately one. The block diagram of PGA in this mode is shown in Figure 22-2. This mode is also known as voltage follower, or unity gain mode. Even though this mode does not provide any voltage amplification, this mode is extremely useful because this mode prevents one stage's input impedance from loading the prior stage's output impedance. Not only does buffer mode isolate the load from the signal source, but also offers impedance matching between different parts of a circuit. The buffer op-amp also has a low output impedance that can drive a load without being affected by the load's impedance. Moreover, the low output impedance helps to maintain the signal voltage across the load, preventing voltage drops that can affect the performance of the circuit.

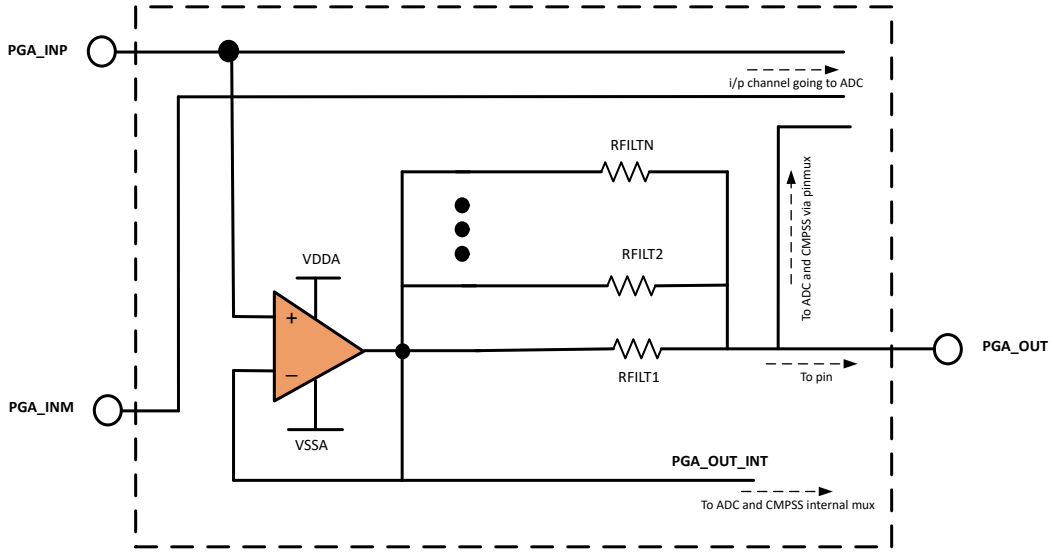


Figure 22-2. Buffer Mode

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22.4.2 Standalone Mode

In this mode, a standalone operational amplifier is available that can support a number of analog applications using a minimum number of external components. Figure 22-3 Shows the block diagram of PGA in this mode. In this mode, the output voltage is determined by the external resistors connected to the inverting and non-inverting pins, as well as the feedback circuitry connected to the output.

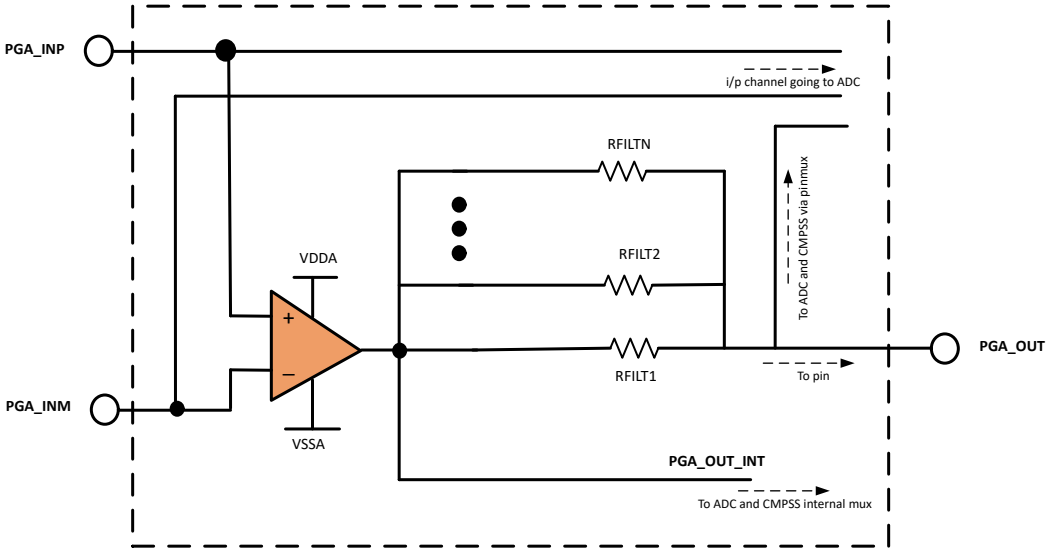


Figure 22-3. Standalone Mode

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22.4.3 Non-inverting Mode

In non-inverting mode, the input voltage signal is applied directly to the non-inverting pin PGA_INP and generates an amplified output signal that is proportional and in phase with the input signal. The block diagram of PGA in this mode is illustrated in Figure 22-4. Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting input terminal by way of a voltage divider network R_{ia} – R_{ib}. The voltage gain in this mode can be calculated using Equation 25:

$$V_{PGA_OUT} = \left(1 + \frac{R_{ib}}{R_{ia}}\right) V_{PGA_INP} \quad (25)$$

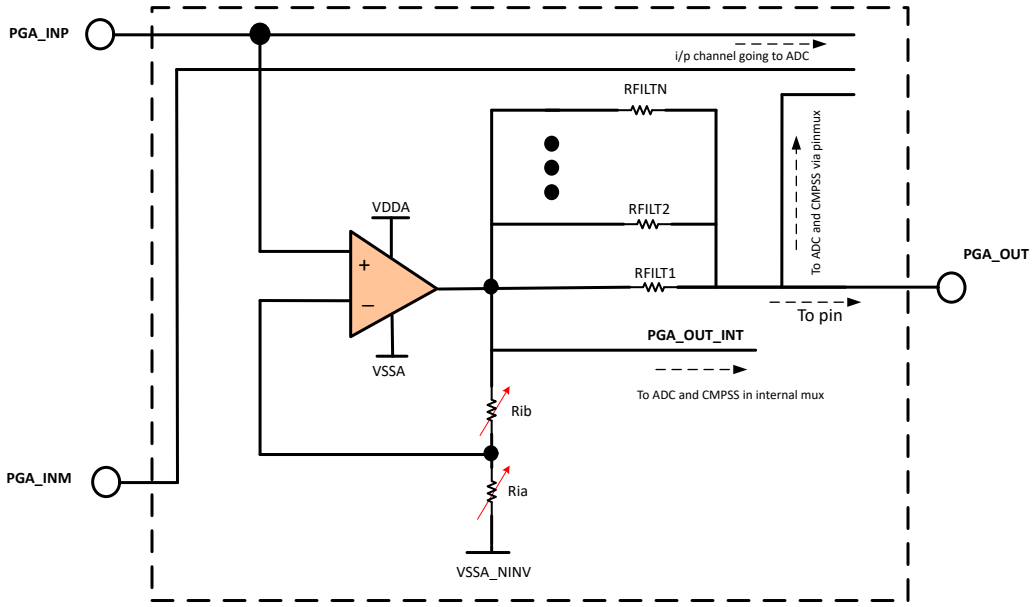


Figure 22-4. Non-inverting Mode

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22.4.4 Subtractor Mode

In subtractor mode, the subtraction of the two input voltages is possible. Superposition is used to calculate the output voltage resulting from each input voltage, and then the two output voltages are subtracted to arrive at the final output voltage. The block diagram of PGA in this mode is demonstrated in Figure 22-5. The voltage gain can be derived as:

$$V_{PGA_OUT} = \left(1 + \frac{R_{ib}}{R_{ia}}\right)V_{PGA_INP} - \left(\frac{R_{ib}}{R_{ia}}\right)V_{PGA_INM} \quad (26)$$

The differential signal is multiplied by the stage gain, so the subtractor mode name is a good choice for the circuit. If a voltage divider circuit with similar values of R_{ia}-R_{ib} is added to the non-inverting pin, this mode only amplifies the differential portion of the input signal; therefore, this mode rejects the common-mode portion of the input signal.

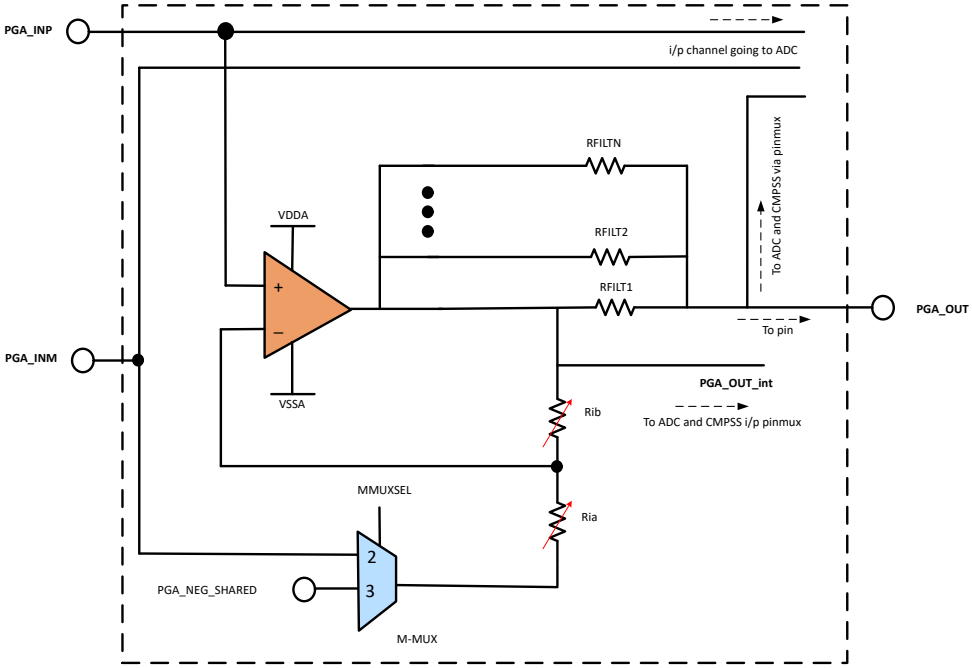


Figure 22-5. Subtractor Mode

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22.5 External Filtering

To remove any unwanted high-frequency noise, two types of low-pass filter can be implemented using internal resistors of PGA module:

1. Low-pass filter using internal filter resistors R_{FILT} and external capacitor
2. Low-pass filter using internal gain resistors R_{ib} and external capacitor

22.5.1 Low-Pass Filter Using Internal Filter Resistor and External Capacitor

The PGA output can be routed to a pin through an embedded series resistor for the purpose of low-pass filtering the amplified signal. The filter resistance is software selectable using the PGACTL[FILT_RES_SEL] register field. The default selection of PGACTL[FILT_RES_SEL] = 0 disables the filter path.

The cutoff frequency can be estimated using the standard low-pass RC given by:

$$f_{cutoff} = \frac{1}{2\pi R_{FILT} C_{FILTER}} \quad (27)$$

Each gain mode requires a minimum amount of series resistance when filtering is enabled. The values are shown in Table 22-3. Also, the external capacitor value C_{FILTER} influences the ADC sampling performance. See Section 22.10.2.2 for more information.

Table 22-3. Minimum Filter Resistance

PGACTL[GAIN]	Minimum R_{FILT} Required PGACTL[FILT_RES_SEL]
0	50Ω
1	50Ω
2	50Ω
3	100Ω
4	100Ω
5	200Ω
6	400Ω

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22.5.2 Single Pole Low-Pass Filter Using Internal Gain Resistor and External Capacitor

Some applications cannot tolerate having an RC network at the output of the amplifier. Amplifier output current flowing through the filter resistor creates a voltage offset that introduces output error. In this case, one can opt to filter the noise spikes by placing a feedback capacitor across the feedback loop. In fact, a simple single-pole low pass filter can be implemented by placing an external capacitance between PGA_INM and PGA_OUT in internal gain mode, which is shown in Figure 22-6.

This form of very simple filter is normally used in instances where a small amount of roll off is required. PGA feedback node RTAP can be brought on pin PGA_INM for external filtering by selecting PMUXSEL = 00, NMUXSEL = 01, and MMUXSEL = 01. Also, to enable this mode, PGA_FB_ON_PIN input/register needs to be set to 1.

The cutoff frequency for this type of filter can be calculated very easily by working out the frequency at which the reactance of the capacitor equals the resistance of the resistor R_{ib}, which is defined by Equation 28:

$$f_{cutoff} = \frac{1}{2\pi R_{ib} C_{Ext}} \tag{28}$$

The gain for this op amp circuit can be calculated in the normal way ignoring the effect of the capacitor:

$$Gain = \left(1 + \frac{R_{ib}}{R_{ia}}\right) \tag{29}$$

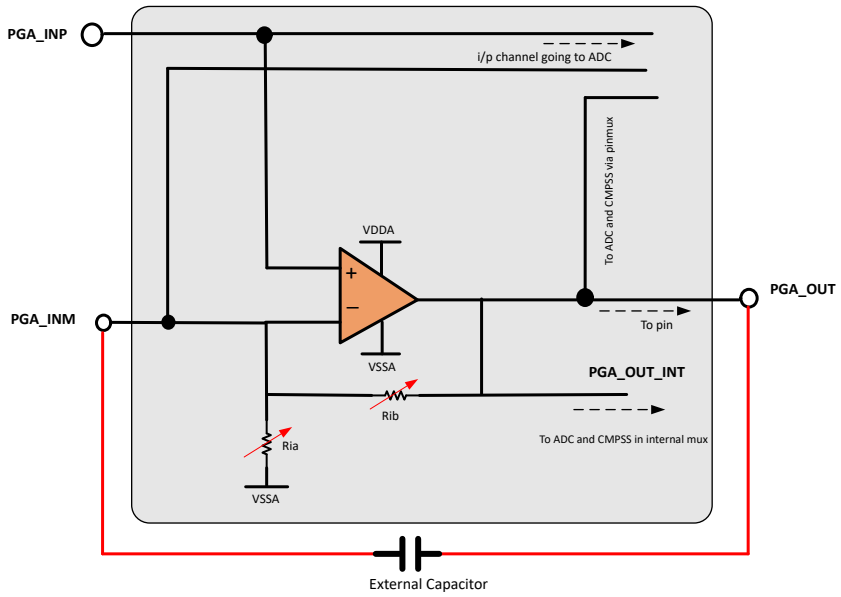


Figure 22-6. Low-Pass Filter Using External Capacitor

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22.6 Error Calibration

Op-Amp error calibration is the process of adjusting the Op-Amp parameters to minimize or eliminate errors. Calibration can be done using different methods, depending on the type of error and the Op-Amp configuration. To reduce inherent offset, factory-generated values are written to the trim registers by calling the Device_cal() function that is located in TI reserved OTP.

22.6.1 Offset Error

This error occurs due to mismatches in the Op-Amp input terminals. The offset error appears as a constant DC offset across the PGA output range, see Figure 22-7. The built-in Device_cal() function reduces the offset error so that the error falls within the data sheet specifications.

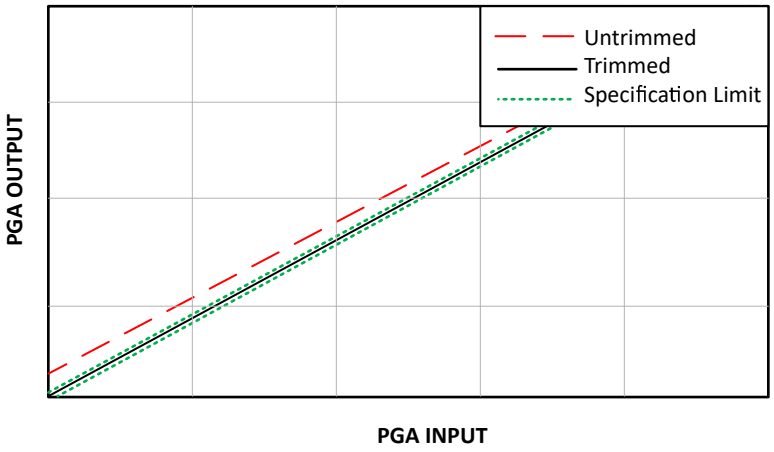


Figure 22-7. PGA Offset Trim

22.6.2 Gain Error

This error occurs due to mismatches in the Op-Amp gain. After the offset error has been removed, the remaining error, the gain error appears as a scaled error that increases in magnitude with increasing PGA output voltage, see Figure 22-8. The hardware trim targets the gain performance so that the hardware trim falls within the data sheet specifications.

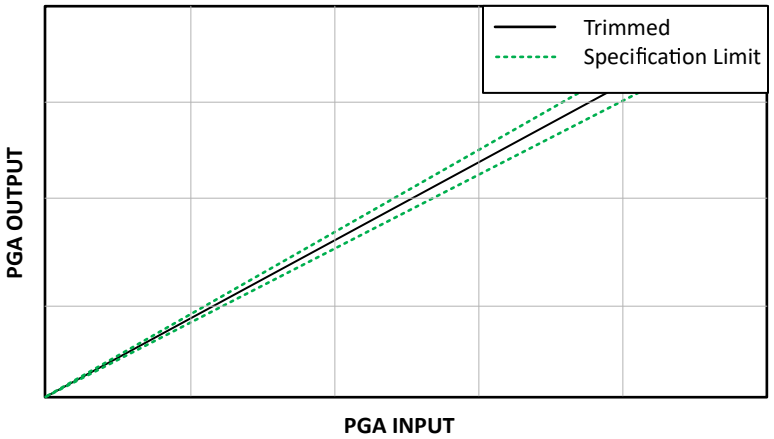


Figure 22-8. PGA Gain Error

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22.7 Chopping Feature

The PGA supports chopping feature, which is a continuous-time modulation technique in which the signal and offset are modulated to different frequencies. The motivation behind adding this feature is primarily to reduce input referred offset to a very small number (in micro volt order). Not only chopping is dynamic technique that continuously reduces offset, but also this technique removes low frequency 1/f noise as well as offset drift over temperature or time.

The chopping feature is demonstrated in Figure 22-9. In broad terms, an input voltage first passes through a chopper driven by a clock at frequency f_{ch}; so, the voltage is converted to a square-wave voltage. Then, the modulated signal along with the offset are amplified by the fully differential amplifier. The second chopper then demodulates the amplified input signal back to DC, while the offset is shifted to the frequency of the clock f_{ch} harmonics. The DC offset can be filtered out by a low-pass filter.

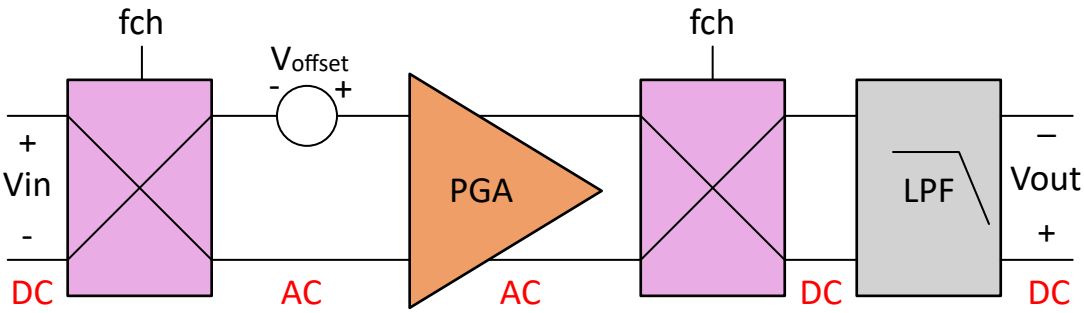


Figure 22-9. General Chopping Technique

This device supports ADC-assisted method. In this method, the chopping control signal comes from the on-chip ADC module. Moreover, Start of Conversion (SOC) in the ADC module can be used to implement chopping. In this method, PGA output is sampled by the on-chip ADC module. Note that the ADC-assisted method relies on ADC module for filtering the output instead of using external low-pass filter. To remove the offset, an average of the output signal can be taken in ADC module. This functionality is provided in post-processing block in ADC module. The ADC-assisted chopping stands out from purely analog chopping methods due to the ability to offer higher accuracy and precision.

Figure 22-10 shows the general diagram of ADC-assisted chopping mode, in which a logic block is used to generate the necessary signal to handle chopping. To configure the ADC-assisted chopping, write to the PGA_CHOP field in the MUXSEL register. To configure control signal for ADC-assisted chopping, write to the CHOP_EXTCTRL field in the PGACTL register.

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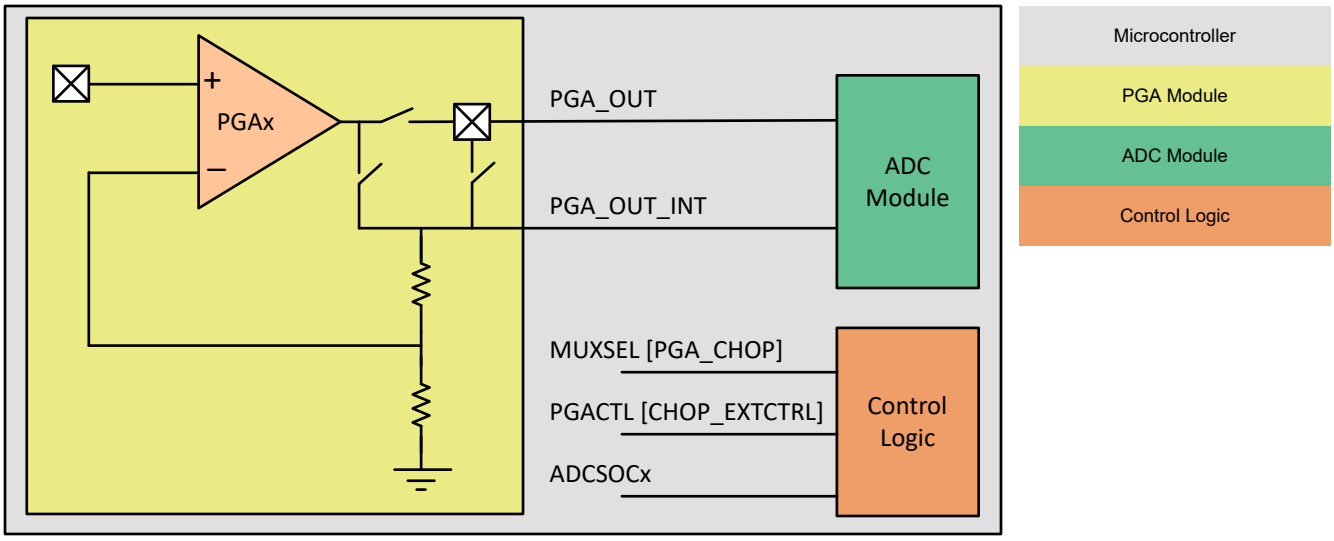


Figure 22-10. ADC-Assisted Chopping Block Diagram

For the PGA, the ADC assisted chopping feature is supported when the ADC is connected to the PGA_OUT_INT of the PGA. The table below shows the connectivity between the PGA and ADC modules.

Table 22-4. PGA and ADC Connection

Internal PGA Out Signal	ADC Connection
PGA0_OUT_INT	ADC0_IN31
PGA1_OUT_INT	ADC1_IN31
PGA2_OUT_INT	ADC2_IN31

22.8 Enabling and Disabling the PGA Clock

If the clock to the PGA is disabled while the PGA is outputting a voltage, the output voltage remains unaffected but the PGA registers are no longer updated with register writes. Enabling the clock resumes register writes.

22.9 Lock Register

The PGALOCK register provides the ability to block writes to certain PGA configuration registers. Locking register writes can prevent spurious or malicious code from modifying critical register settings. Once a register has been locked using the PGALOCK register, only a module-level or device-level reset can restore write functionality.

22.10 Analog Front-End Integration

The PGAs operate together with the other embedded analog modules (ADC, CMPSS) creating an analog front-end system.

22.10.1 Buffered DAC

Buffered DACs are commonly used in a variety of applications such as dc-coupled applications,in which the drive amplifier must provide the required gain and offset voltage, to match the signal to the input voltage range of the ADC. As a best practice, the PGA input signal is conditioned so that the PGA output is centered within the linear range. The input signal requires some combination of offset and attenuation to achieve this goal. For example, an external resistor divider can attenuate the input signal while the embedded buffered DAC can provide a positive voltage offset, see Figure 22-11.

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Note

While this device does not have a dedicated Buffered DAC module, the same functionality can be implemented with CMPSS DACL Output signal.

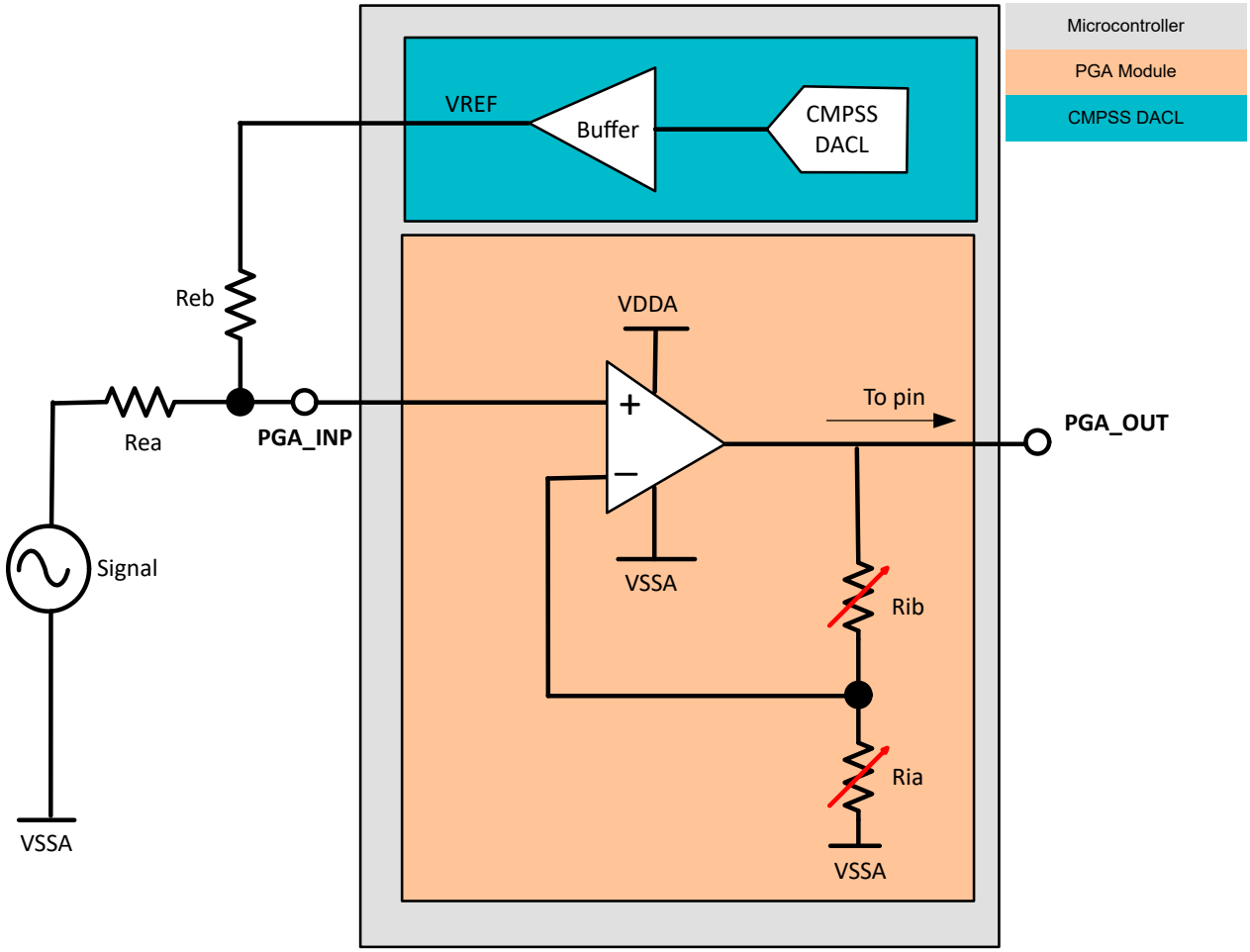


Figure 22-11. Level Shifting Using Internal DAC

With the topology shown in Figure 22-11, the voltage seen at the PGA_INP pin can be calculated as:

$$V_{PGA_OUT} = \frac{R_{ib} + R_{ia}}{R_{ia}}\left(\frac{R_{eb}}{R_{ea} + R_{eb}}V_{signal} + \frac{R_{ea}}{R_{ea} + R_{eb}}V_{REF}\right) \quad (30)$$

Supplying a V_{DAC_OUT} of 1.65V transforms a bipolar V_{SIGNAL} range of -0.5V to +0.5V into a V_{PGA_INP} range of 0.22V to 0.88V, which is an excellent choice for the 3× gain mode.

22.10.2 Analog-to-Digital Converter (ADC)

In the simplest application, the PGA amplifies small input signals to increase the ADC dynamic range. The PGA also provides the additional benefit of buffering input signals from the ADC sample and hold capacitor, which further reduces sampling error.

Both the filtered and unfiltered PGA output paths are available for ADC sampling. Minimum ADC acquisition windows are recommended when sampling the PGA paths.

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22.10.2.1 Unfiltered Acquisition Window

The device data sheet provides a minimum estimated ADC acquisition window for sampling the PGA_OUT signal with one ADC. This estimated value can provide sampling accuracy close to the specified performance parameters of the ADC. A longer acquisition window can be used for better performance.

22.10.2.2 Filtered Acquisition Window

The minimum ADC acquisition window for sampling the PGA_OF filtered signal with one ADC varies based on the values of R_{FILTER} and C_{FILTER}. To make sure of good performance, choose a C_{FILTER} capacitor that is large enough to satisfy most of the ADC sample and hold capacitor (Ch) charge requirements. The C_{FILTER} value can be sized based on the acceptable amount of ADC sampling error (LSB_{Err}):

$$C_{FILTER} = \frac{C_h \times 4096}{LSB_{Err}} \quad (31)$$

22.10.3 Comparator Subsystem (CMPSS)

The PGA output can be monitored by a CMPSS module for trips above or below a reference voltage. Up to two independent reference thresholds per CMPSS can be used for trip detection.

Both the filtered and unfiltered PGA output paths are available for CMPSS trip monitoring.

22.10.4 PGA_NEG_SHARED Feature

This feature allows sharing PGA_INM pin across three available PGA modules, which helps to save two pins for applications where multiple PGAs are required, but the PGA modules all can have a common negative sense point. To enable this feature, MMUXSEL and NMUXSEL must be set to 3 and 1, respectively. As you can see in Figure 22-12, PGA_NEG_SHARED is shared among three PGA modules internally so that the user can employ there PGA modules with only one inverting pin. In three-phase current measurement, three modules of PGA can be employed to monitor the shunt current by using only four pins. The schematic of three-phase current sensing is shown in Figure 22-13.

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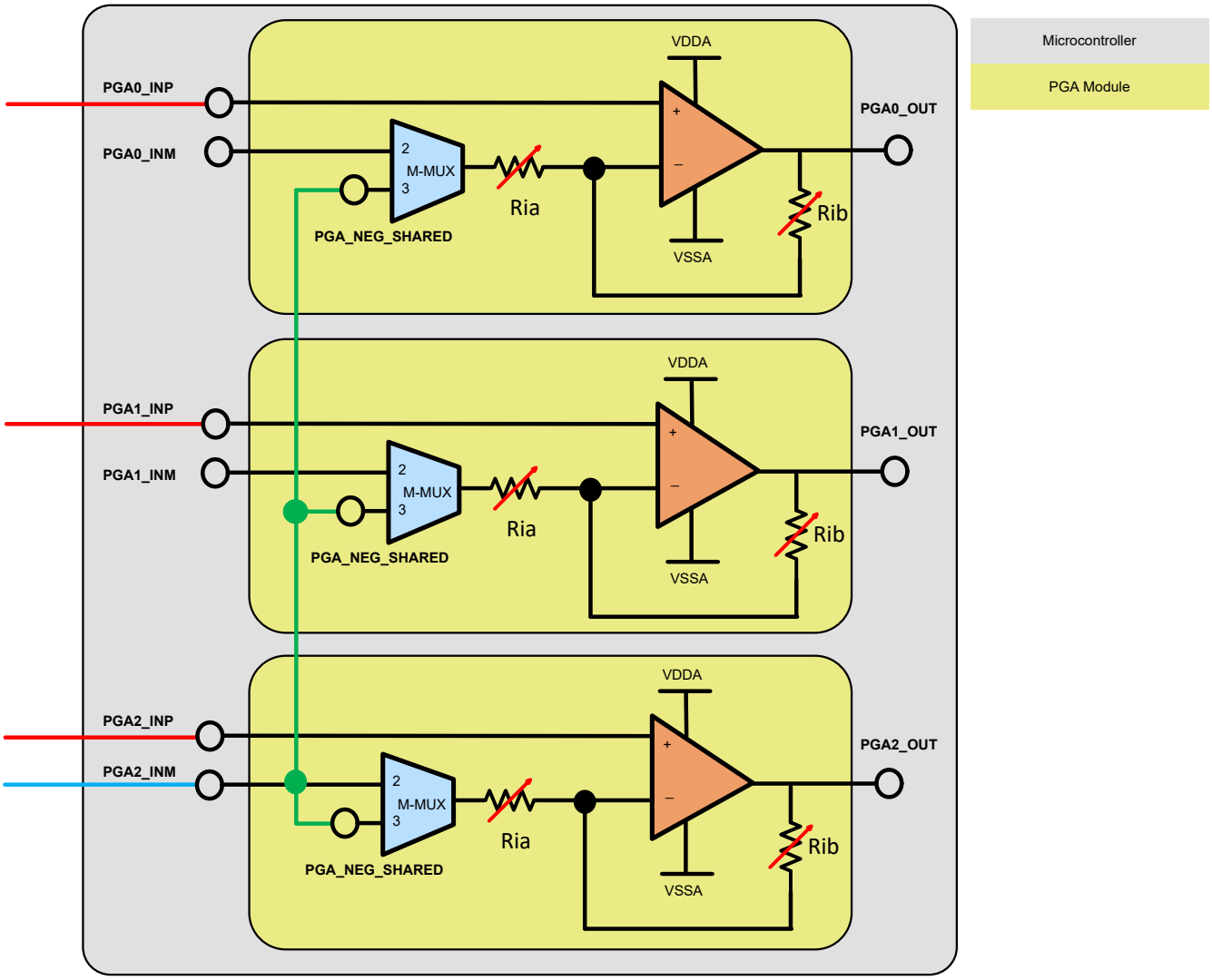


Figure 22-12. Sharing PGA_NEG Pin Between PGA Modules

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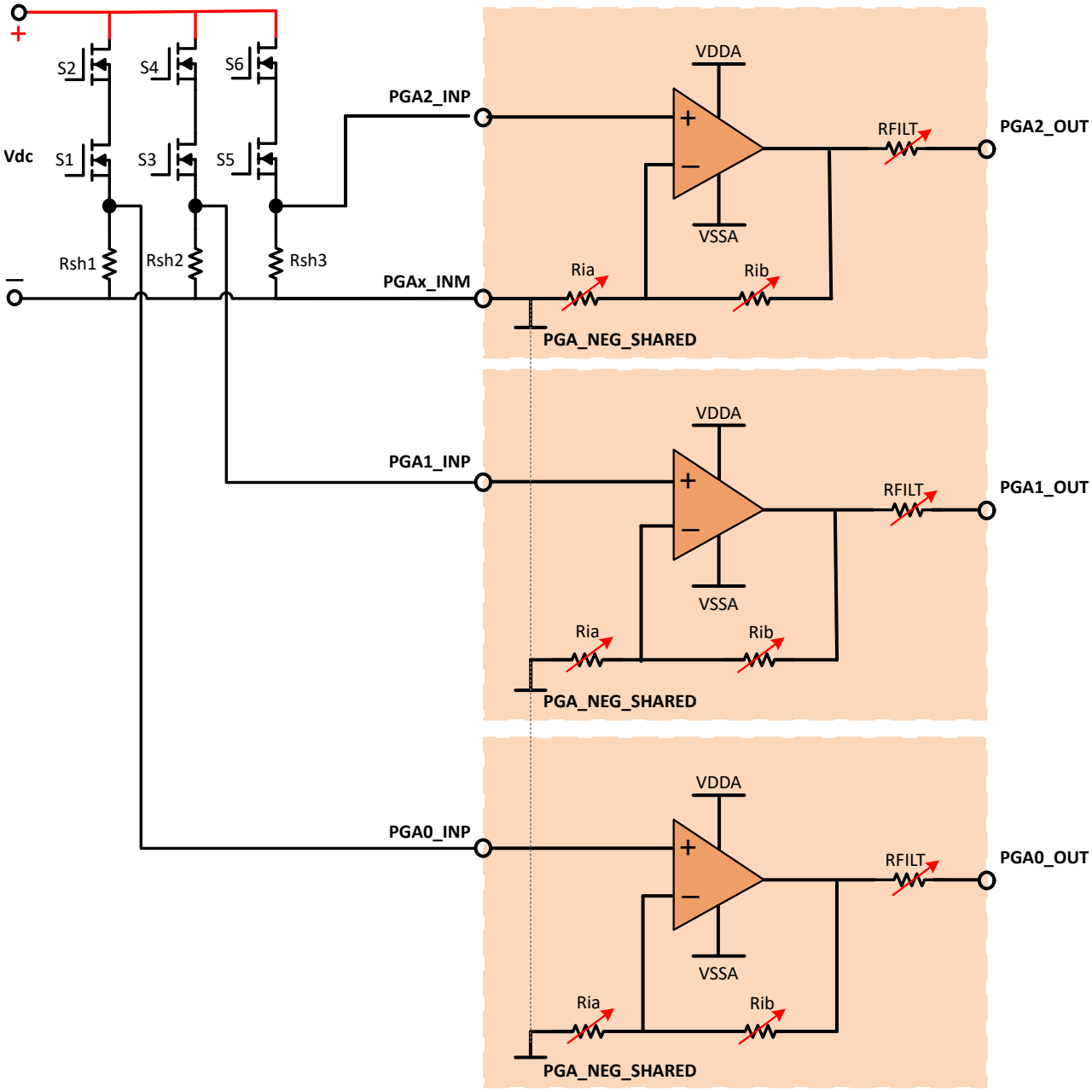


Figure 22-13. Three-phase Current Sensing Using PGA_NEG_SHARED Feature

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22.10.5 Alternate Functions

Each PGA has up to three device terminals for operation: non-inverting pin PGA_INP, inverting pin PGA_INM, and output pin PGA_OUT, see Figure 22-14. Alternate paths at the device level allow the input and output filter terminals to take on alternate functions. This can be especially valuable, if the respective PGA resource is not used for an application. See *Analog Subsystem* for more information.

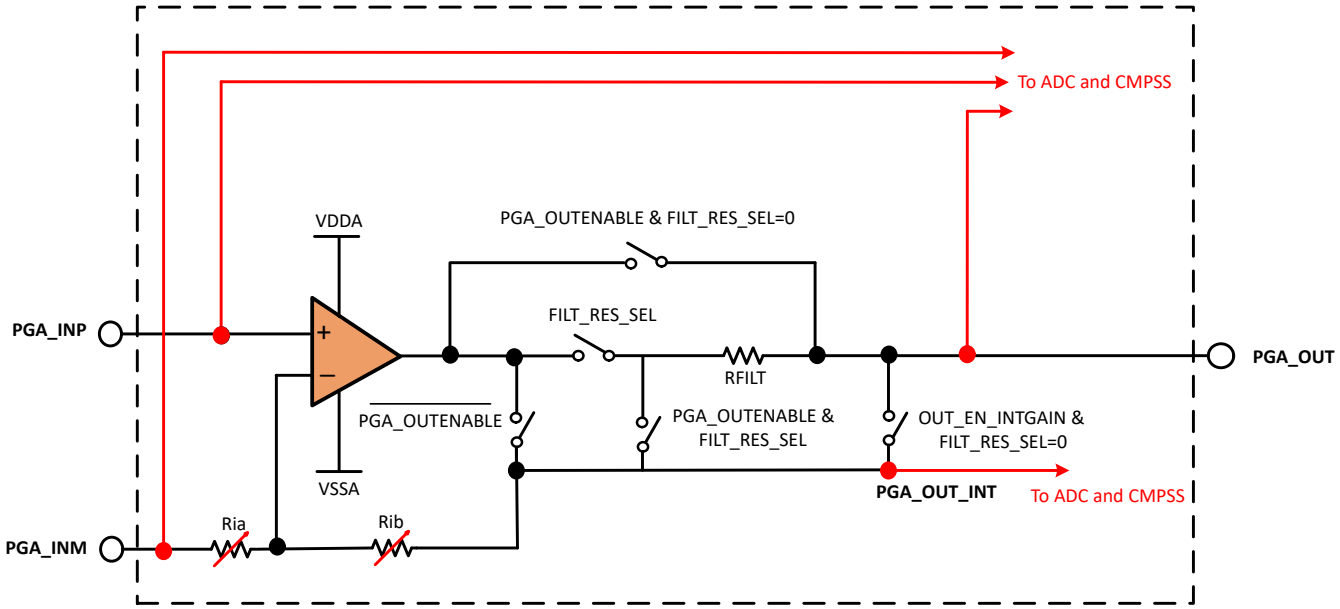


Figure 22-14. PGA Pin Alternate Functions

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22.11 Examples

22.11.1 Non-Inverting Amplifier Using Non-Inverting Mode

Given a small positive signal, the PGA can be used to amplify the signal to increase the dynamic range of ADC sampling and comparator trip monitoring. For example, an input signal with a valid range between 0.25V to 0.75V can be amplified in 4× mode to produce an output signal between 1V to 3V.

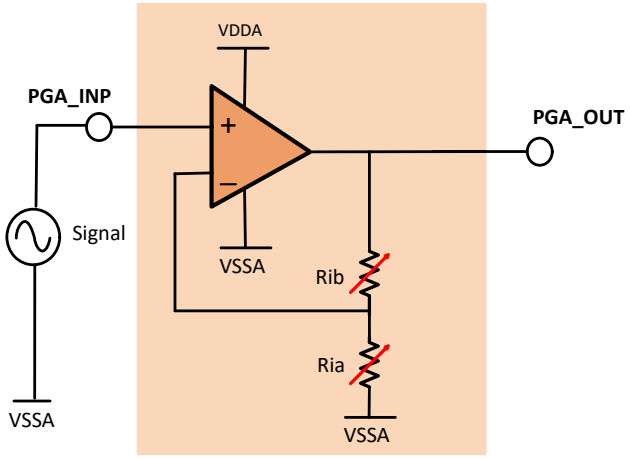


Figure 22-15. Signal Conditioning Using Non-inverting Mode

The amplified output voltage is calculated as:

$$V_{PGA_OUT} = \left(1 + \frac{R_{ib}}{R_{ib}}\right) V_{Signal} \quad (32)$$

22.11.2 Buffer Mode

Assume that there is an analog sensor that gives a 0 to 12V range signal. To sample the signal using the ADC, a voltage divider along with a unity-gain op-amp is required. In the circuit shown in Figure 22-16, the voltage divider (36kΩ and 100kΩ) brings the 12V sensor voltage down to something less than 3.3V. The 100Ω filter resistor and 1nF capacitor form a low-pass filter with a cut-off frequency of 1.5MHz.

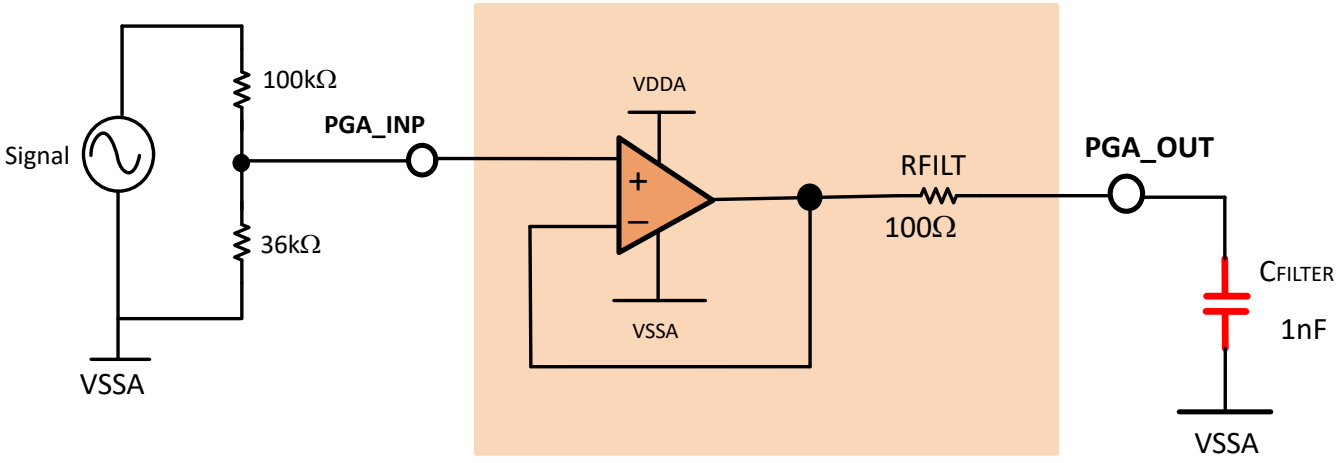


Figure 22-16. Buffer Mode Example

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22.11.3 Low-Side Current Sensing

Low-side current sensing connects the sensing resistor between the load and ground. To not adversely affect current flow, the current resistors have a small value that produces a proportionally small voltage across them. The small voltage across the shunt resistor must usually be boosted from tens or hundreds of millivolts to tenths of a volt or volts for upstream conversion by an analog-to-digital converter (ADC). This task can be performed by PGA. Figure 22-17 shows the low-side current sensing using PGA.

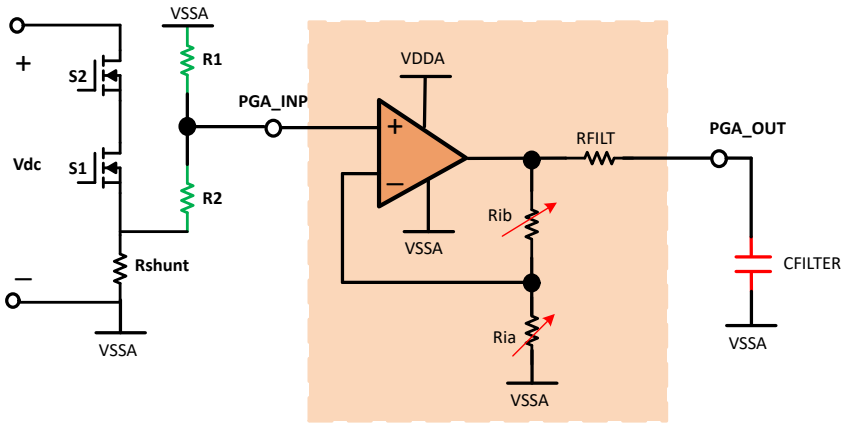


Figure 22-17. PGA Shunt Current Example

In this circuit, the amplifier gain is set by the ratio of R_{ib} divided by R_{ia}. If the divider resistors R_1=R_{ib} and R_2=R_{ia}, then the amplified voltage can be calculated by:

$$V_{PGA_OUT} = \frac{R_{ib}}{R_{ia}}\left(R_{shunt}I_{load}\right) \quad (33)$$

If low-pass filtering is desired, an external capacitor in conjunction with internal filter resistors R_{FILT} can be used. The filter cutoff frequency is estimated using:

$$f_{cutoff} = \frac{1}{2\pi R_{FILT}C_{FILTER}} \quad (34)$$

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22.11.4 Bidirectional Current Sensing

The PGA senses current flow through a sense resistor in both directions, demonstrated in Figure 22-18. The bidirectional current-sensing capability is achieved by applying a positive voltage at the non-inverting pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The output voltage of the PGA is given by:

$$V_{PGA_OUT} = \frac{R_{ib}}{R_{ia}}(R_{sense}I_{load}) + V_{REF} \quad (35)$$

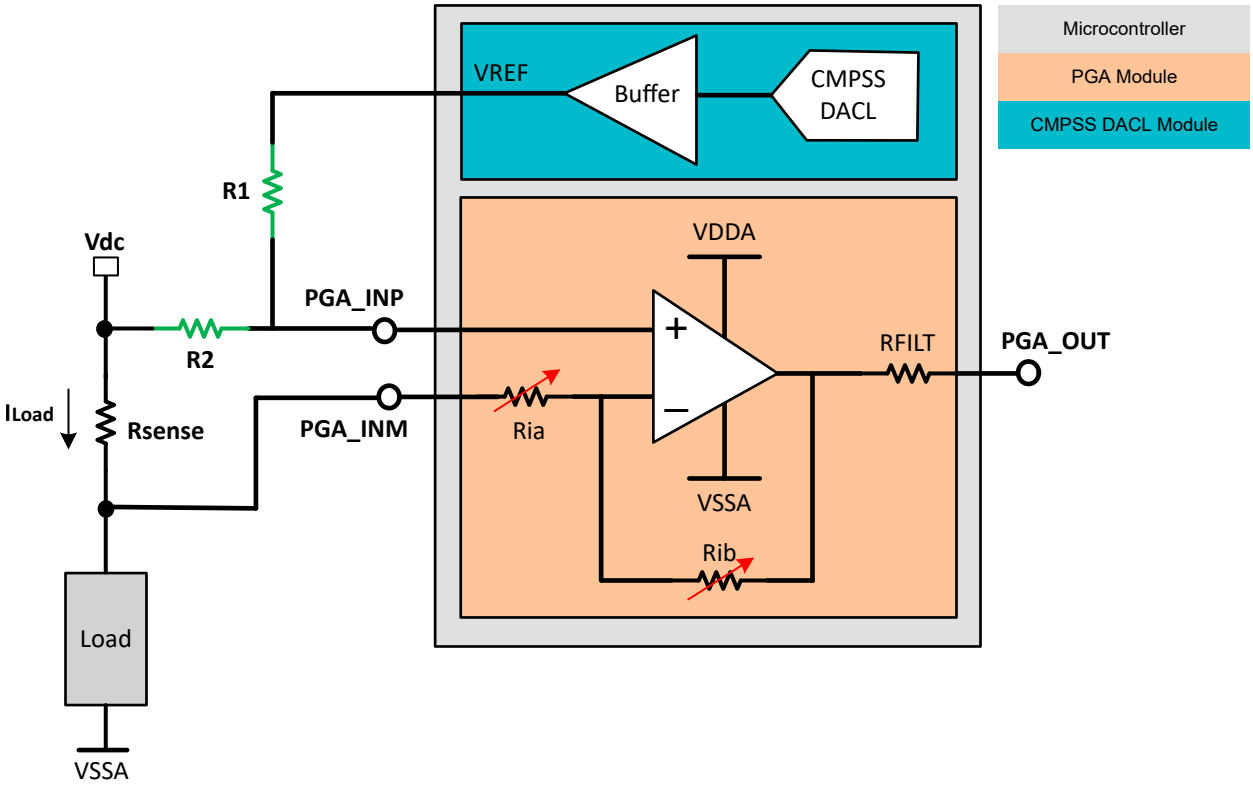


Figure 22-18. Bidirectional Current Sensing

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22.12 PGA Registers

This Section describes the PGA Registers.

22.12.1 PGA Base Address Table

Table 22-5. PGA Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Pga0Regs	PGA_REGS	PGA0	0x400F_C000
Pga1Regs	PGA_REGS	PGA1	0x400F_D000
Pga2Regs	PGA_REGS	PGA2	0x400F_E000

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22.12.2 PGA_REGS Registers

Table 22-6 lists the memory-mapped registers for the PGA_REGS registers. All register offset addresses not listed in Table 22-6 should be considered as reserved locations and the register contents should not be modified.

Table 22-6. PGA_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	PGACTL	PGA Control Register		Go
4h	MUXSEL	Mux Selection Register		Go
10h	PGATYPE	PGA Type Register		Go
14h	PGALOCK	PGA Lock Register		Go

Complex bit access types are encoded to fit into small table cells. Table 22-7 shows the codes that are used for access types in this section.

Table 22-7. PGA_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 PGACTL Register (Offset = 0h) [Reset = 0000h]

PGACTL is shown in Figure 22-19 and described in Table 22-8.

Return to the Summary Table.

PGA Control Register

Figure 22-19. PGACTL Register

15	14	13	12	11	10	9	8
CHOP_EXTCTRL	RESERVED					PGA_OUTEN_INTGAIN	PGA_OUTENABLE
R/W-0h	R-0h					R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
GAIN			RESERVED	FILT_RES_SEL			PGAEN
R/W-0h			R-0h	R/W-0h			R/W-0h

Table 22-9. PGACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CHOP_EXTCTRL	R/W	0h	CHOP Signal Control Control dependent on the state of the PGA_CHOP field in the MUXSEL regsiter. If PGA_CHOP = 2, then this is a read only bit. If PGA_CHOP = 3, then this bit can be written by SW to control the chopping signal to the PGA Reset type: SYSRSn 0h (R/W) = Chop control signal is 0 1h (R/W) = Chop control signal is 1
14-10	RESERVED	R	0h	Reserved
9	PGA_OUTEN_INTGAIN	R/W	0h	PGA Internal Gain on Pin 0 PGA internal gain path comes to a pin 1 PGA internal gain path does not come to a pin Reset type: SYSRSn
8	PGA_OUTENABLE	R/W	0h	PGA Output Enable 0 PGA Output does not come to a pin 1 PGA Output does come to a pin Reset type: SYSRSn
7-5	GAIN	R/W	0h	PGA Gain programming-1-64 000 x 1 001 x 2/-1 010 x 4/-3 011 x 8/-7 100 x 16/-15 101 x 32/-31 110 x 64/-63 111 reserved Reset type: SYSRSn
4	RESERVED	R	0h	Reserved

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Table 22-9. PGACTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	FILT_RES_SEL	R/W	0h	Filter Resistor Select 000 Filter Disabled 001 50 010 100 011 200 100 400 101 800 110 Filter Disabled 111 Filter Disabled Reset type: SYSRSn
0	PGAEN	R/W	0h	PGA Enable. 0 PGA is disabled and powered down. 1 PGA is enabled. Reset type: SYSRSn

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2 MUXSEL Register (Offset = 4h) [Reset = 0000h]

MUXSEL is shown in Figure 22-20 and described in Table 22-9.

Return to the Summary Table.

Mux Selection Register

Figure 22-20. MUXSEL Register

15	14	13	12	11	10	9	8
RESERVED	PGA_CHOP		PGA_FBONPIN	RESERVED	MMUXSEL		
R-0h	R/W-0h		R/W-0h	R-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	NMUXSEL			PMUXSEL			
R-0h	R/W-0h			R/W-0h			

Table 22-11. MUXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-13	PGA_CHOP	R/W	0h	PGA Output Chopping Control 00 Chopping Disabled 01 Reserved 10 ADC assisted chop (using ADCSOC as ctrl) 11 ADC assisted chop (using PGA_CHOP_EXTCTRL register) Reset type: SYSRSn 0h (R/W) = PGA Chopping disabled 1h (R/W) = Reserved 2h (R/W) = ADC SOC signal will automatically change the state of CHOP_EXTCTRL bit in PGACTL register after each sample 3h (R/W) = CHOP_EXTCTRL bit must manually be written by SW to change the its state
12	PGA_FBONPIN	R/W	0h	PGA Feedback to Negative Input Connection 0 PGA_INM0 and Inverting Input are not connected 1 PGA_INM0 and Inverting Input are connected Reset type: SYSRSn
11	RESERVED	R	0h	Reserved
10-8	MMUXSEL	R/W	0h	PGA M Mux Select Select which signal is connected to the RBOT node of the PGA feedback resistor path Reset type: SYSRSn 0h (R/W) = Stand alone op-amp or G=1 mode select 1h (R/W) = Non-inverting gain mode select, feedback resistors have a path to VSSA 2h (R/W) = Inverting gain mode select, feedback resistors have a path to local PGA_INM0 pin 3h (R/W) = Inverting gain mode select, feedback resistors have a path to local PGA_INM1 pin 4h (R/W) = Inverting gain mode select, feedback resistors have a path to local PGA_INM2 pin 5h (R/W) = Inverting gain mode select, feedback resistors have a path to local PGA_INM3 pin 6h (R/W) = Inverting gain mode select, feedback resistors have a path to global PGA_INMx pin 7h (R/W) = Inverting gain mode select, feedback resistors have a path to global PGA_INMx pin
7	RESERVED	R	0h	Reserved

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Table 22-11. MUXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	NMUXSEL	R/W	0h	PGA Negative Input Mux Select Select which signal is routed to the inverting input of the PGA Reset type: SYSRSn 0h (R/W) = Top of the feedback resistor path selected 1h (R/W) = Tap point in the feedback resistor path selected 2h (R/W) = INM0 selected as inverting input 3h (R/W) = INM1 selected as inverting input 4h (R/W) = INM2 selected as inverting input 5h (R/W) = INM3 selected as inverting input 6h (R/W) = Reserved 7h (R/W) = Reserved
3-0	PMUXSEL	R/W	0h	PGA Positive Input Mux Select Select which signal is routed to the non-inverting input of the PGA Reset type: SYSRSn 0h (R/W) = INP0 selected as non-inverting input 1h (R/W) = INP1 selected as non-inverting input 2h (R/W) = INP2 selected as non-inverting input 3h (R/W) = INP3 selected as non-inverting input 4h (R/W) = INP4 selected as non-inverting input 5h (R/W) = INP5 selected as non-inverting input 6h (R/W) = INP6 selected as non-inverting input 7h (R/W) = INP7 selected as non-inverting input 8h (R/W) = INP8 selected as non-inverting input 9h (R/W) = Reserved Ah (R/W) = Reserved Bh (R/W) = Reserved Ch (R/W) = Reserved Dh (R/W) = Reserved Eh (R/W) = Reserved Fh (R/W) = Reserved

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3 PGATYPE Register (Offset = 10h) [Reset = 0201h]

PGATYPE is shown in Figure 22-21 and described in Table 22-10.

Return to the Summary Table.

PGA Type Register

Figure 22-21. PGATYPE Register

15	14	13	12	11	10	9	8
TYPE							
R-2h							
7	6	5	4	3	2	1	0
REV							
R-1h							

Table 22-13. PGATYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TYPE	R	2h	PGA Type. Reset type: SYSRSn
7-0	REV	R	1h	PGA Revision. Reset type: SYSRSn

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4 PGALOCK Register (Offset = 14h) [Reset = 0000h]

PGALOCK is shown in Figure 22-22 and described in Table 22-11.

Return to the Summary Table.

PGA Lock Register

Figure 22-22. PGALOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	PGATMCTL	RESERVED	MUXSEL	PGACTL
WSonce-0h	R-0h	R-0h	R-0h	WSonce-0h	WSonce-0h	WSonce-0h	WSonce-0h

Table 22-15. PGALOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RESERVED	WSonce	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	PGATMCTL	WSonce	0h	0 Writes to PGATMCTL are enabled. 1 Writes to PGATMCTL are disabled. Reset type: SYSRSn
2	RESERVED	WSonce	0h	Reserved
1	MUXSEL	WSonce	0h	0 Writes to MUXSEL are enabled. 1 Writes to MUXSEL are disabled. Reset type: SYSRSn
0	PGACTL	WSonce	0h	0 Writes to PGACTL are enabled. 1 Writes to PGACTL are disabled. Reset type: SYSRSn

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Chapter 23

Enhanced Capture (eCAP)

This chapter describes the enhanced capture (eCAP) module, which is used in systems where accurate timing of external events is important.

23.1 Introduction 1380
23.2 Description 1380
23.3 Configuring Device Pins for the eCAP 1380
23.4 Capture and APWM Operating Mode 1383
23.5 Capture Mode Description 1386
23.6 Application of the eCAP Module 1396
23.7 Application of the APWM Mode 1400
23.8 ECAP Interrupts & Triggers 1400
23.9 ECAP Registers 1403

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23.1 Introduction

23.1.1 ECAP Features

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register:
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

23.2 Description

The eCAP module represents one complete capture channel that can be instantiated multiple times, depending on the target device. In the context of this guide, one eCAP channel has the following independent key resources:

- Capture inputs can be connected using the Input X-BAR
- 128:1 input multiplexer
- Output X-BAR is used to configure output in APWM mode
- 32-bit time base (counter)
- 4 × 32-bit time-stamp capture registers (CAP1-CAP4)
- Four-stage sequencer (modulo4 counter) that is synchronized to external events, eCAP pin rising/falling edges.
- Modulo counter status register (MODCNTRSTS) to indicate sequencer state
- Independent edge polarity (rising/falling edge) selection for all four events
- Input capture signal prescaling (from 2-62 or bypass)
- One-shot compare register (two bits) to freeze captures after 1-4 time-stamp events
- Control for continuous time-stamp captures using a four-deep circular buffer (CAP1-CAP4) scheme
- Ability to reset event filter, modulo counter, and interrupt flags
- Interrupt capabilities on any of the four capture events

23.3 Configuring Device Pins for the eCAP

The Input X-BAR connects the device pins to the module as input. Any GPIO on the device can be configured as an input. A 128:1 input multiplexer must also be configured (see Figure 23-3). This multiplexer can select a variety of inputs by configuring ECCTL0.INPUTSEL.

Note

Note ECAPxIN has to be at least 2 × MCLK-cycles wide to be properly captured by the eCAP module; otherwise, the input pulse can get missed from sampling by the MCLK.

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Table 23-1. eCAP Input Selection

Input Signal	ECAP0 INDEX	ECAP1 INDEX	ECAP2 INDEX
INPUTXBAR1	0	0	0
INPUTXBAR2	1	1	1
INPUTXBAR3	2	2	2
INPUTXBAR4	3	3	3
INPUTXBAR5	4	4	4
INPUTXBAR6	5	5	5
INPUTXBAR7	6	6	6
INPUTXBAR8	7	7	7
INPUTXBAR9	8	8	8
INPUTXBAR10	9	9	9
INPUTXBAR11	10	10	10
INPUTXBAR12	11	11	11
INPUTXBAR13	12	12	12
INPUTXBAR14	13	13	13
INPUTXBAR15	14	14	14
INPUTXBAR16	15	15	15
MCAN0_INT0	16	16	16
OUTPUTXBAR1	17	17	17
OUTPUTXBAR2	18	18	18
OUTPUTXBAR3	19	19	19
OUTPUTXBAR4	20	20	20
OUTPUTXBAR5	21	21	21
OUTPUTXBAR6	22	22	22
OUTPUTXBAR7	23	23	23
OUTPUTXBAR8	24	24	24
MCAN1_INT0	25	25	25
Reserved	26	26	26
Reserved	27	27	27
Reserved	28	28	28
ADC0EVT1	29	29	29
ADC0EVT2	30	30	30
ADC0EVT3	31	31	31
ADC0EVT4	32	32	32
ADC1EVT1	33	33	33
ADC1EVT2	34	34	34
ADC1EVT3	35	35	35
ADC1EVT4	36	36	36
ADC2EVT1	37	37	37
ADC2EVT2	38	38	38
ADC2EVT3	39	39	39
ADC2EVT4	40	40	40
CMPSS0_CTRIPL	41	41	41
CMPSS1_CTRIPL	42	42	42
CMPSS2_CTRIPL	43	43	43
CMPSS3_CTRIPL	44	44	44

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Table 23-1. eCAP Input Selection (continued)

Input Signal	ECAP0 INDEX	ECAP1 INDEX	ECAP2 INDEX
CMPSS0_CTRIPH	45	45	45
CMPSS1_CTRIPH	46	46	46
CMPSS2_CTRIPH	47	47	47
CMPSS3_CTRIPH	48	48	48
CMPSS0_CTRIPH_OR_CTRIPL	49	49	49
CMPSS1_CTRIPH_OR_CTRIPL	50	50	50
CMPSS2_CTRIPH_OR_CTRIPL	51	51	51
CMPSS3_CTRIPH_OR_CTRIPL	52	52	52
INPUTXBAR7	53	Reserved	Reserved
INPUTXBAR8	Reserved	53	Reserved
INPUTXBAR9	Reserved	Reserved	53
FSIRX_MEASURE	54	54	54
FSIRX_MEASURE_RISE	55	55	55
FSIRX_MEASURE_FALL	56	56	56
SDFLT1_COMPL	57	57	57
SDFLT2_COMPL	58	58	58
SDFLT3_COMPL	59	59	59
SDFLT4_COMPL	60	60	60
SDFLT1_COMPZ	61	61	61
SDFLT2_COMPZ	62	62	62
SDFLT3_COMPZ	63	63	63
SDFLT4_COMPZ	64	64	64
SDFLT1_COMPH	65	65	65
SDFLT2_COMPH	66	66	66
SDFLT3_COMPH	67	67	67
SDFLT4_COMPH	68	68	68
SDFLT1_COMPH_OR_COMPL	69	69	69
SDFLT2_COMPH_OR_COMPL	70	70	70
SDFLT3_COMPH_OR_COMPL	71	71	71
SDFLT4_COMPH_OR_COMPL	72	72	72
ECAT_SYNC0	73	73	73
ECAT_SYNC1	74	74	74
GPIO_PA8	75	75	75
GPIO_PA9	76	76	76
GPIO_PA22	77	77	77
GPIO_PA23	78	78	78
Reserved	79-127	79-127	79-127

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23.4 Capture and APWM Operating Mode

Use the eCAP module resources to implement a single-channel PWM generator (with 32-bit capabilities) when the eCAP module is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms. The CAP1 and CAP2 registers become the active period and compare registers, respectively, while CAP3 and CAP4 registers become the period and compare shadow registers, respectively. Figure 23-1 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

Figure 23-2 further descries the output of the eCAP in APWM mode based on the CMP and PRD values.

Note

A single pin is shared between CAP and APWM functions. In capture mode, the pin is an input; in APWM mode, the pin is an output.

Note

In APWM mode, writing any value to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.

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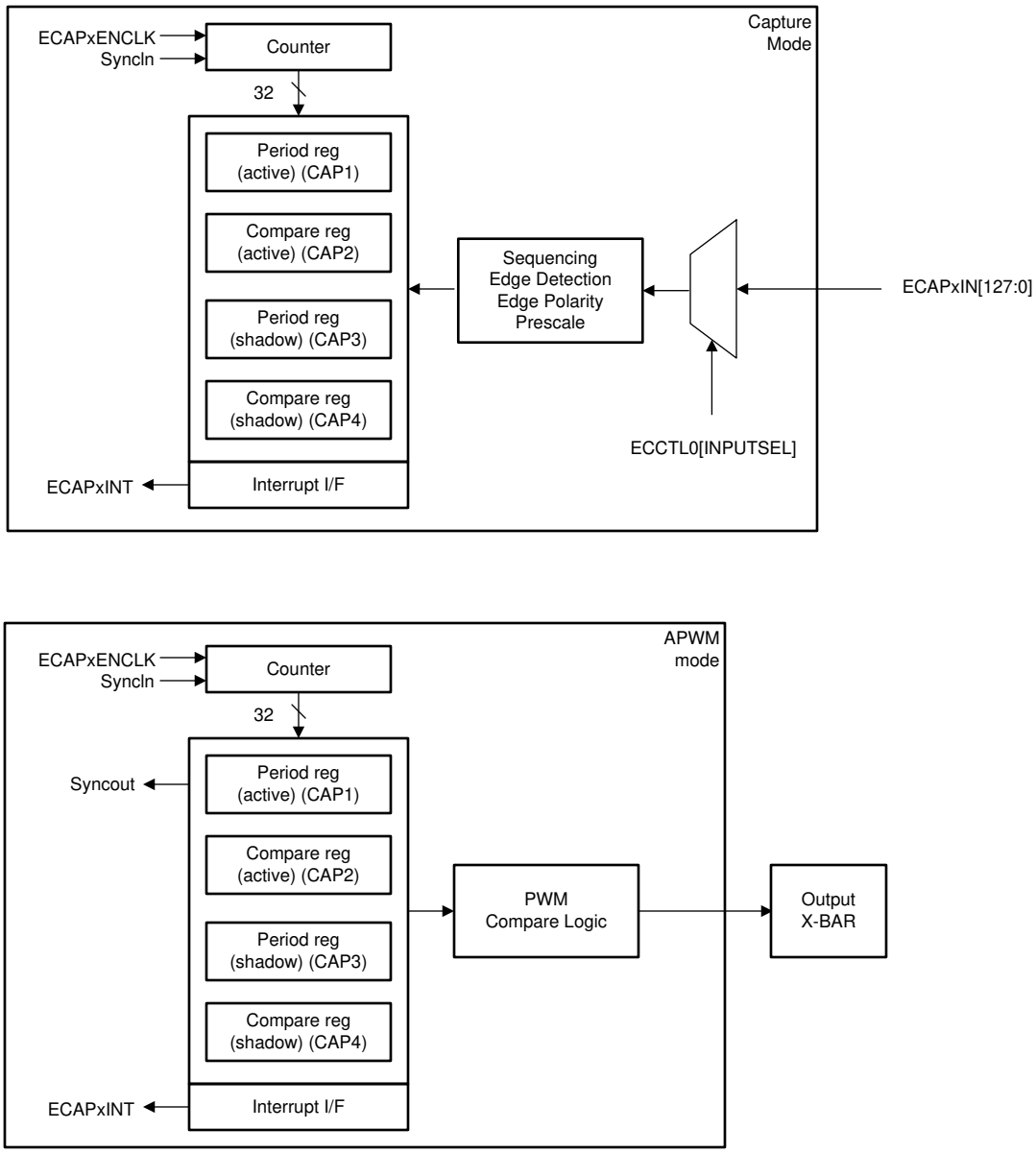


Figure 23-1. Capture and APWM Modes of Operation

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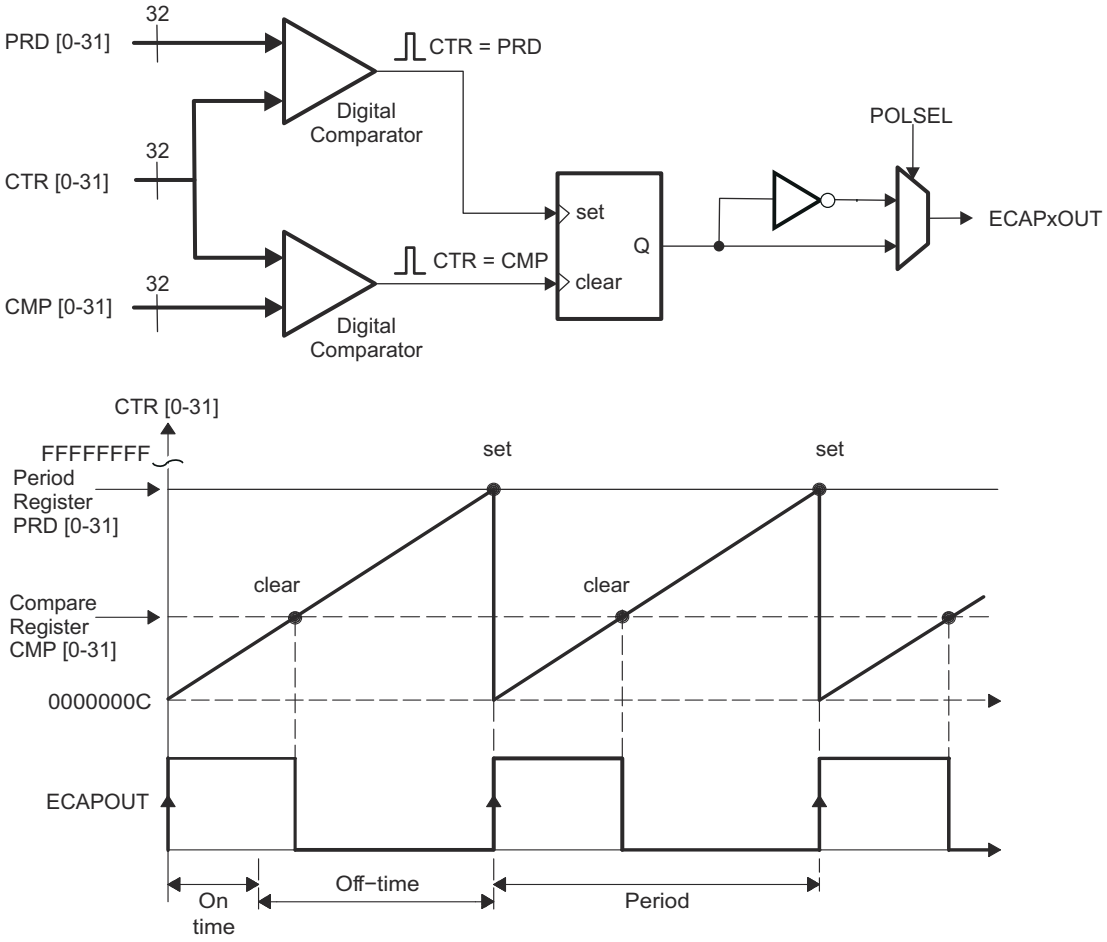


Figure 23-2. Counter Compare and PRD Effects on the eCAP Output in APWM Mode

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23.5 Capture Mode Description

Figure 23-3 shows the various components that implement the capture function.

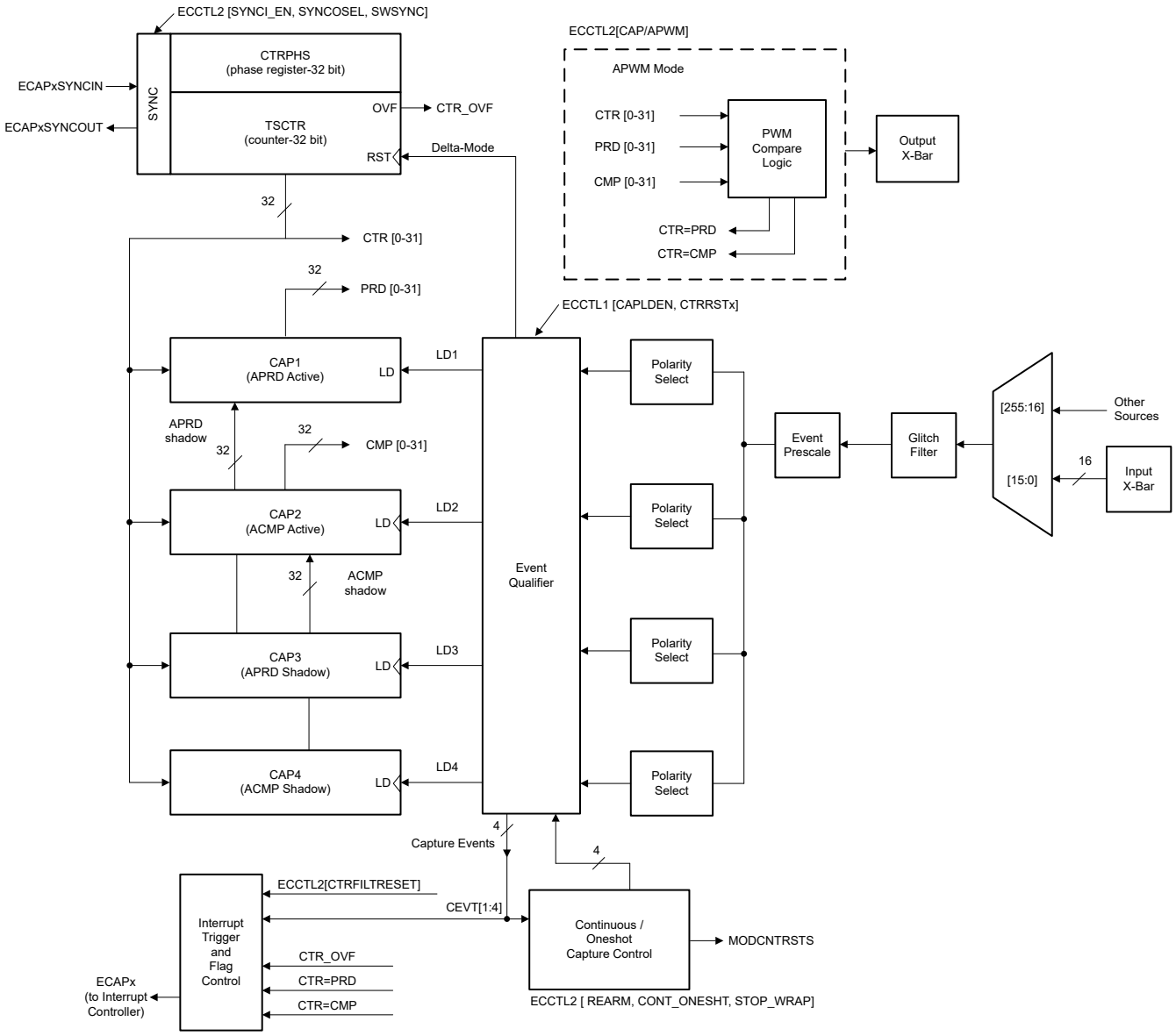
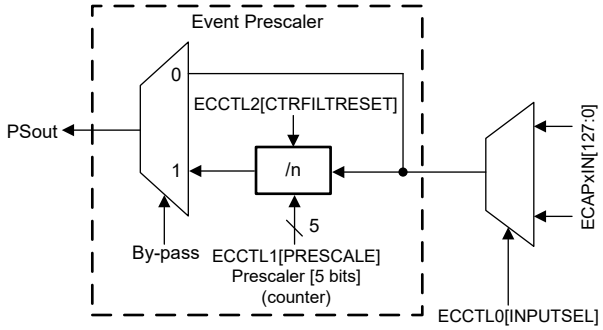


Figure 23-3. eCAP Block Diagram

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23.5.1 Event Prescaler

An input capture signal (pulse train) can be prescaled by N = 2-62 (in multiples of 2) or can bypass the prescaler. This is useful when very high frequency signals are used as inputs. Figure 23-4 shows a functional diagram and Figure 23-5 shows the operation of the prescale function. The event prescaler can be reset by setting the ECCTL2.CTRFILTRESET register bit.



Note

When a prescale value of 1 is chosen (ECCTL1[13:9] = 0,0,0,0,0), the input capture signal bypasses the prescale logic completely.

Note

The first Rise edge after Prescale configuration change is not passed to Capture logic, prescaler value takes into effect on the second rising edge after the configuration.

Figure 23-4. Event Prescale Control

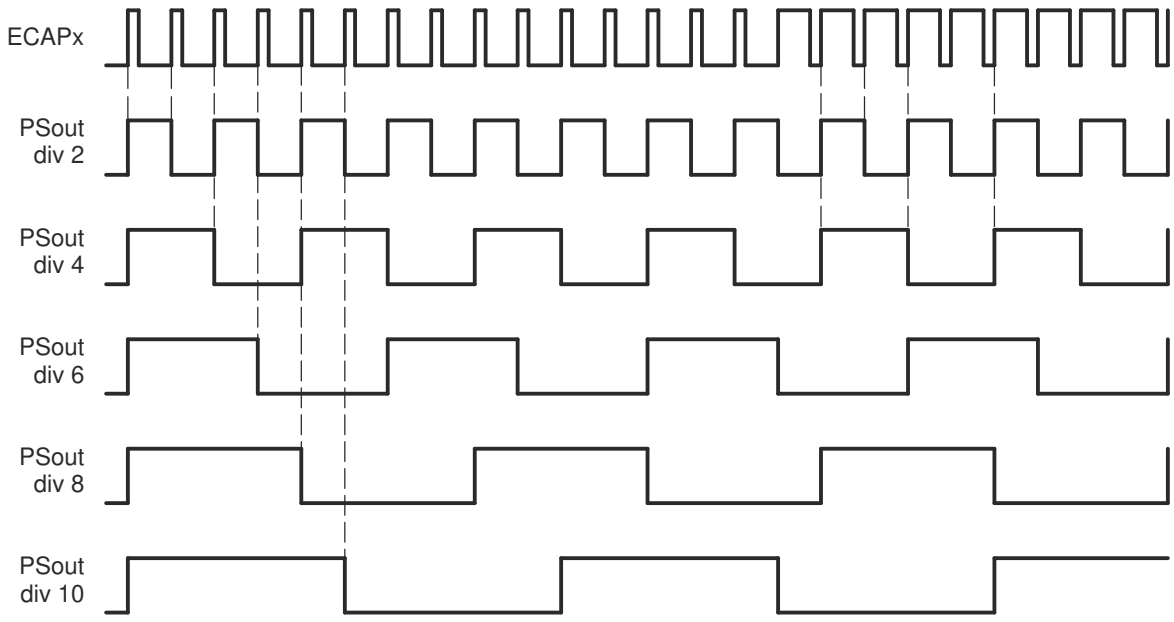


Figure 23-5. Prescale Function Waveforms

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23.5.2 Edge Polarity Select and Qualifier

Functionality and features include:

- Four independent edge polarity (rising edge/falling edge) selection muxes are used, one for each capture event.
- Each edge (up to 4) is event qualified by the Modulo4 sequencer.
- The edge event is gated to the respective CAPx register by the Mod4 counter. The CAPx register is loaded on the falling edge.

23.5.3 Continuous/One-Shot Control

Operation of eCAP in Continuous/One-Shot mode:

- The Mod4 (2-bit) counter is incremented using edge qualified events (CEVT1-CEVT4).
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- During one-shot operation, a 2-bit stop register (STOP_WRAP) is used to compare the Mod4 counter output, and when equal, stops the Mod4 counter and inhibits further loads of the CAP1-CAP4 registers. In this mode, if TSCCTR counter is configured to reset on capture event (CEVTx) by configuring ECCTL1.CTRRSTx bit, the operation still keeps resetting the TSCCTR counter on capture event (CEVTx) after the STOP_WRAP value is reached and re-arm (REARM) has not occurred.

The continuous/one-shot block controls the start, stop and reset (zero) functions of the Mod4 counter, using a mono-shot type of action that can be triggered by the stop-value comparator and re-armed using software control.

Once armed, the eCAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of CAP1-4 registers (time stamps).

Re-arming prepares the eCAP module for another capture sequence. Also, re-arming clears (to zero) the Mod4 counter and permits loading of CAP1-4 registers again, providing the CAPLDEN bit is set.

In continuous mode, the Mod4 counter continues to run (0->1->2->3->0, the one-shot action is ignored, and capture values continue to be written to CAP1-4 in a circular buffer sequence.

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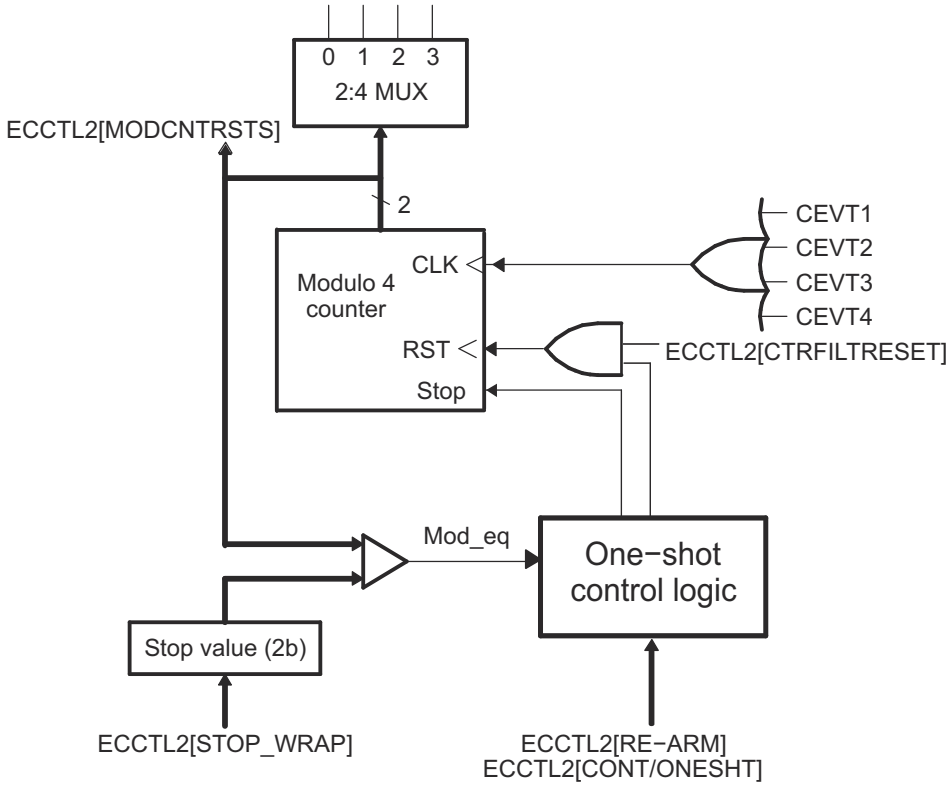


Figure 23-6. Details of the Continuous/One-shot Block

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23.5.4 32-Bit Counter and Phase Control

This counter provides the time-base for event captures, and is clocked using the system clock.

A phase register is provided to achieve synchronization with other counters using a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then the counter value is reset to 0 by any of the LD1-LD4 signals.

23.5.5 CAP1-CAP4 Registers

These 32-bit registers are supplied by the 32-bit counter timer bus, CTR[0-31], and are loaded (capture a time-stamp) when the respective LD inputs are strobed.

Control bit CAPLDEN can inhibit loading of the capture registers. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, StopValue = Mod4.

CAP1 and CAP2 registers become the active period and compare registers, respectively, in APWM mode.

CAP3 and CAP4 registers become the respective shadow registers (APRD and ACMP) for CAP1 and CAP2 during APWM operation.

23.5.6 eCAP Sync Selection

eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from eCAP, X-Bar, or PWM modules. The SWSYNC of the eCAP module is logically ORed with the SYNC signal as shown in Figure 23-7. The SYNC signal is defined by the selection of ECAPSYNCINSEL.SEL as shown in Figure 23-8. To select a mux source for EXTSYNCOUT, configure the SYNCSELECT register from the SYNC_SOC_REGS defined in the *Crossbar (X-BAR)* chapter of this document. The below table specifies the sources for the eCAP Sync options in the ECAPSYNCINSEL.SEL register field.

Table 23-2. PWM and eCAP SYNC Selection

PWM*.SYNCINSEL ECAP*.SYNCINSEL	Input Signal
0	Disable
1	Reserved
2	Reserved
3	ECAP0_SYNCOUT
4	ECAP1_SYNCOUT
5	MCPWM0_SYNCOUT
6	MCPWM1_SYNCOUT
7	MCPWM2_SYNCOUT
8	Reserved
9	Reserved
10	ECAP2_SYNCOUT
11	EPWM0_SYNCOUT
12	EPWM1_SYNCOUT
13	EPWM2_SYNCOUT
14	EPWM3_SYNCOUT
15	EPWM4_SYNCOUT
16	EPWM5_SYNCOUT

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Table 23-2. PWM and eCAP SYNC Selection (continued)

PWM*.SYNCINSEL ECAP*.SYNCINSEL	Input Signal
17	ECAT_SYNC0
18	ECAT_SYNC1
19	FSIRX_TRIG1
20	INPUTXBAROUT5
21	INPUTXBAROUT6
22-31	Reserved

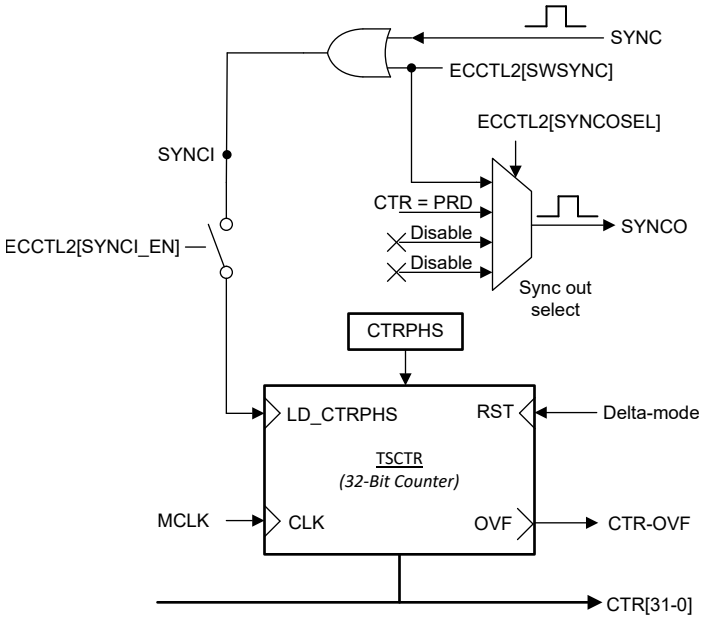


Figure 23-7. ECAP Counter and Synchronization Block

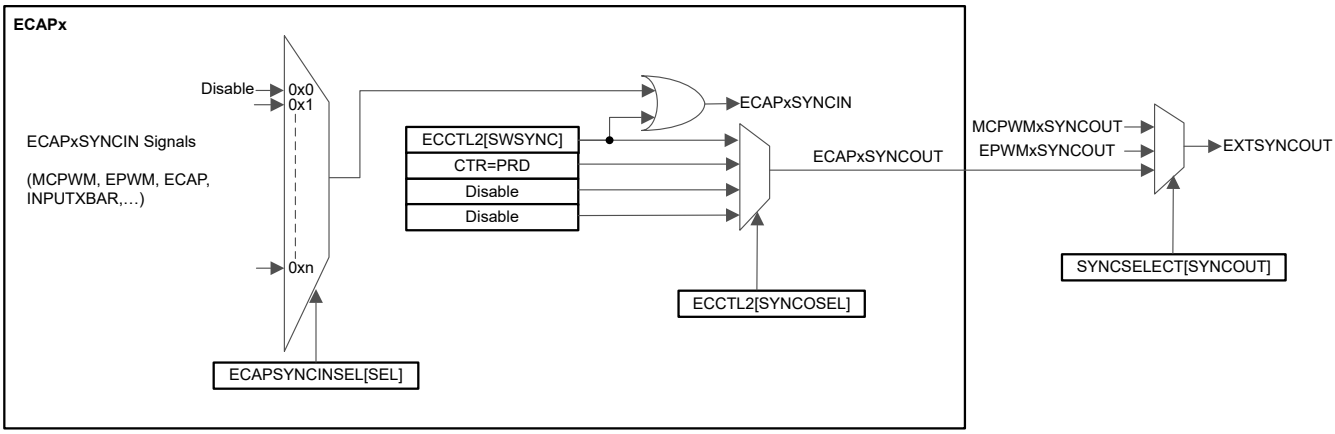


Figure 23-8. eCAP Synchronization Scheme

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23.5.6.1 Example 1 - Using SWSYNC with ECAP Module

Implement the following steps to use SWSYNC with ECAP1 and ECAP2.

- Configure ECAP[1..2].ECAPSYNCINSEL.SEL = 0x0 to disable external SYNCIN coming to eCAP1.
- Configure ECAP[1..2].ECCTL2.SWSYNC = 0x1, to force Software Synchronization of the TSCTR counter.

To use SWSYNC with other eCAP modules, make sure that the previous eCAP chain is not generating a SYNCOUT signal that interferes with the software synchronization.

23.5.7 eCAP Synchronization

eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from ePWMMCPWM. The SWSYNC of the eCAP module is logical ORed with the SYNC signal as shown in Figure 23-9. The SYNC signal is defined by the selection of ECAPxSYNCINSEL[SEL] as shown in Figure 23-10.

Note

ECAPxSYNCOUT going to the ECAPSYNCIN multiplexer is disabled. For example, ECAP1SYNCOUT cannot be a sync in to ECAP1, but ECAP1SYNCOUT can be a sync in to ECAP2, ECAP3, and so on.

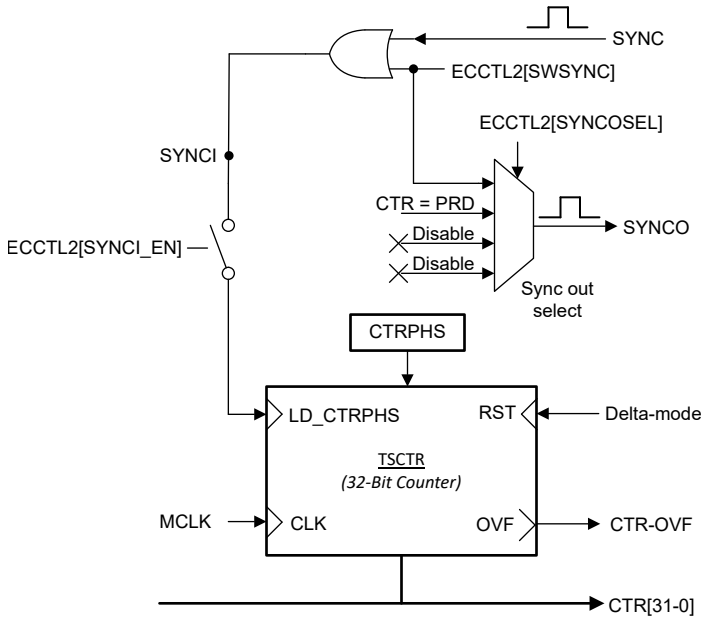


Figure 23-9. ECAP Counter and Synchronization Block

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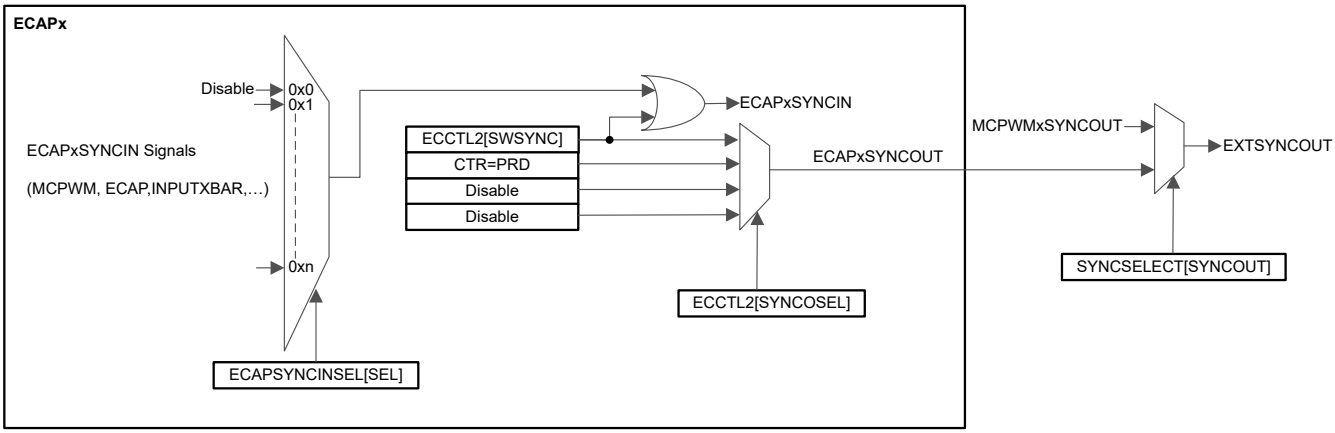


Figure 23-10. eCAP Synchronization Scheme

23.5.8 Shadow Load and Lockout Control

In capture mode, this logic inhibits (locks out) any shadow loading of CAP1 or CAP2 from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate - APRD or ACMP are transferred to CAP1 or CAP2 immediately upon writing a new value.
- On period equal, CTR[31:0] = PRD[31:0].

23.5.9 APWM Mode Operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison by way of 2 digital (32-bit) comparators.
- When CAP1/2 registers are not used in capture mode, the contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved using shadow registers APRD and ACMP (CAP3/4). The shadow register contents are transferred over to CAP1/2 registers, either immediately upon a write, or on a CTR = PRD trigger.
- In APWM mode, writing to CAP1/CAP2 active registers also writes the same value to the corresponding shadow registers CAP3/CAP4. This emulates immediate mode. Writing to the shadow registers CAP3/CAP4 invokes the shadow mode.
- During initialization, write to the active registers for both period and compare. This automatically copies the initial values into the shadow values. For subsequent compare updates during run-time, use the shadow registers.

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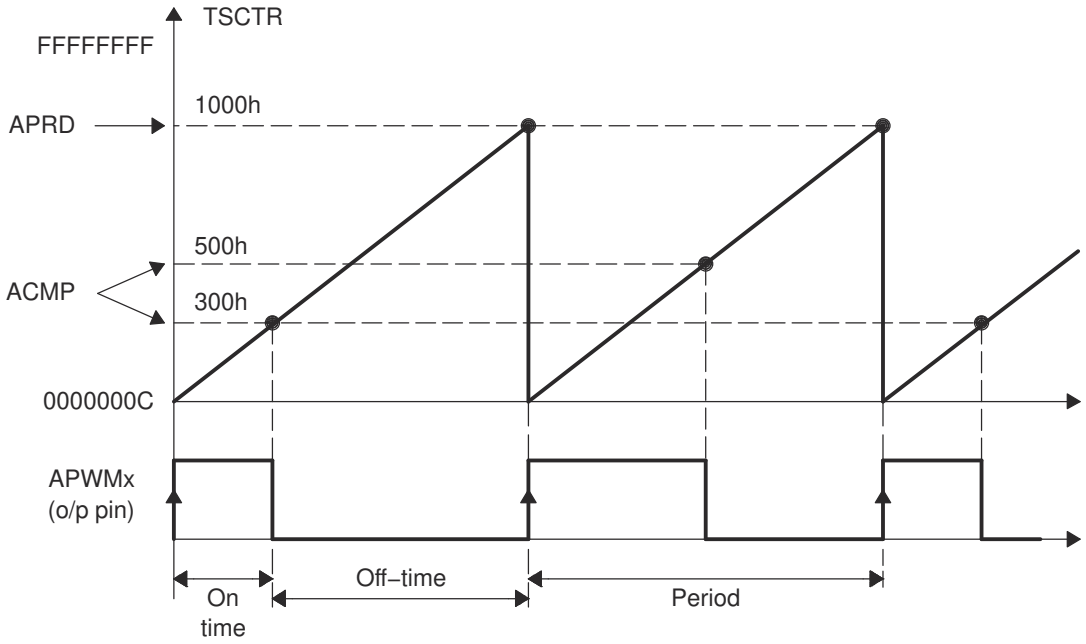


Figure 23-11. PWM Waveform Details Of APWM Mode Operation

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The behavior of APWM active high mode (APWMPOL == 0) is as follows:

```
CMP = 0x00000000, output low for duration of period (0% duty)
```

```
CMP = 0x00000001, output high 1 cycle
```

```
CMP = 0x00000002, output high 2 cycles
```

```
CMP = PERIOD, output high except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output high for complete period (100% duty)
```

```
CMP > PERIOD+1, output high for complete period
```

The behavior of APWM active low mode (APWMPOL == 1) is as follows:

```
CMP = 0x00000000, output high for duration of period (0% duty)
```

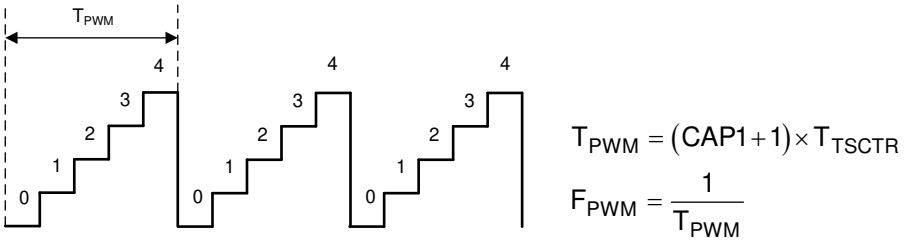
```
CMP = 0x00000001, output low 1 cycle
```

```
CMP = 0x00000002, output low 2 cycles
```

```
CMP = PERIOD, output low except for 1 cycle (<100% duty)
```

```
CMP = PERIOD+1, output low for complete period (100% duty)
```

```
CMP > PERIOD+1, output low for complete period
```



$$T_{PWM} = (CAP1 + 1) \times T_{TSCTR}$$

$$F_{PWM} = \frac{1}{T_{PWM}}$$

Figure 23-12. Time-Base Frequency and Period Calculation

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23.6 Application of the eCAP Module

The following sections provide applications examples to show how to operate the eCAP module.

23.6.1 Example 1 - Absolute Time-Stamp Operation Rising-Edge Trigger

Figure 23-13 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCTR counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCTR contents (time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCTR reaches FFFFFFFF (maximum value), the Mod4 counter wraps around to 00000000 (not shown in Figure 23-13), if this occurs, the CTROVF (counter overflow) flag is set, and an interrupt (if enabled) occurs. Captured Time-stamps are valid at the point indicated by the diagram (after the fourth event); hence, event CEVT4 can conveniently be used to trigger an interrupt and the CPU can read data from the CAPx registers.

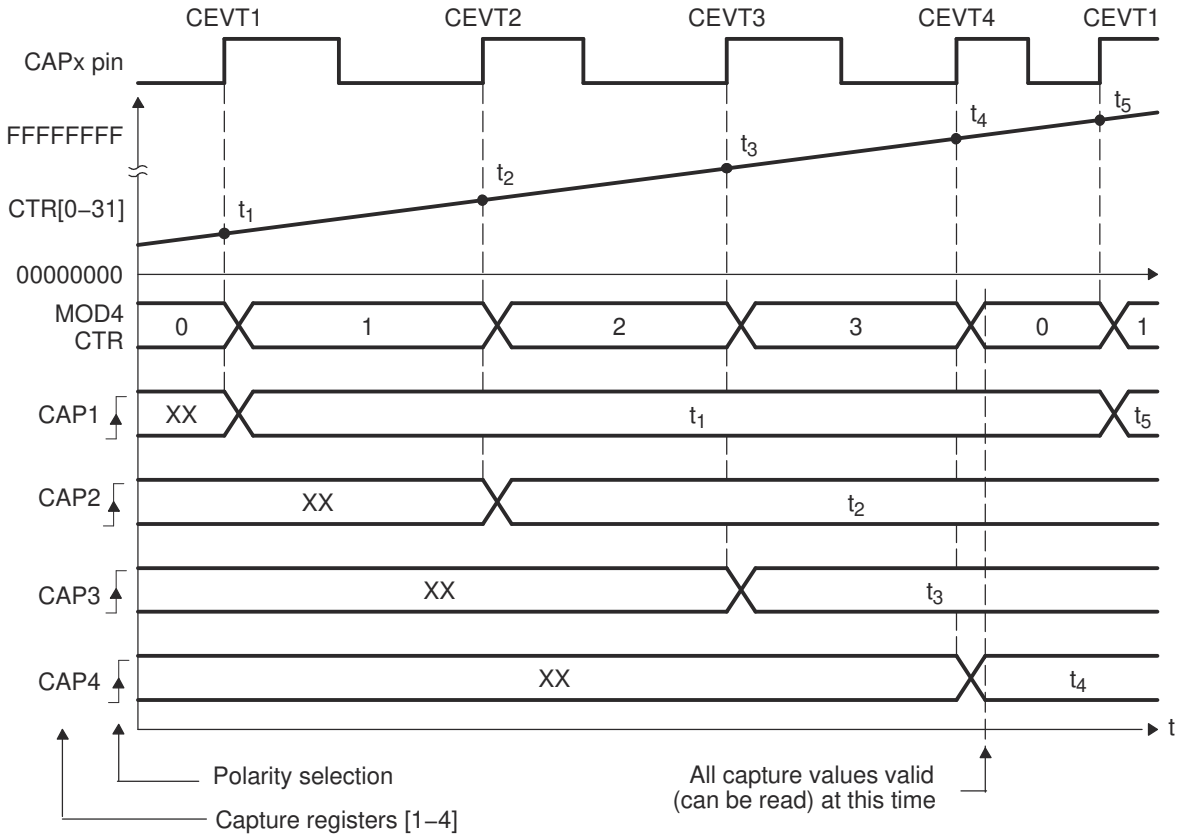


Figure 23-13. Capture Sequence for Absolute Time-stamp and Rising-Edge Detect

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23.6.2 Example 2 - Absolute Time-Stamp Operation Rising- and Falling-Edge Trigger

In Figure 23-14, the eCAP operating mode is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information, that is: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, …and so on. Duty Cycle1 (on-time %) = ($t_2 - t_1$) / Period1 x 100%, and so on. Duty Cycle1 (off-time %) = ($t_3 - t_2$) / Period1 x 100%, and so on.

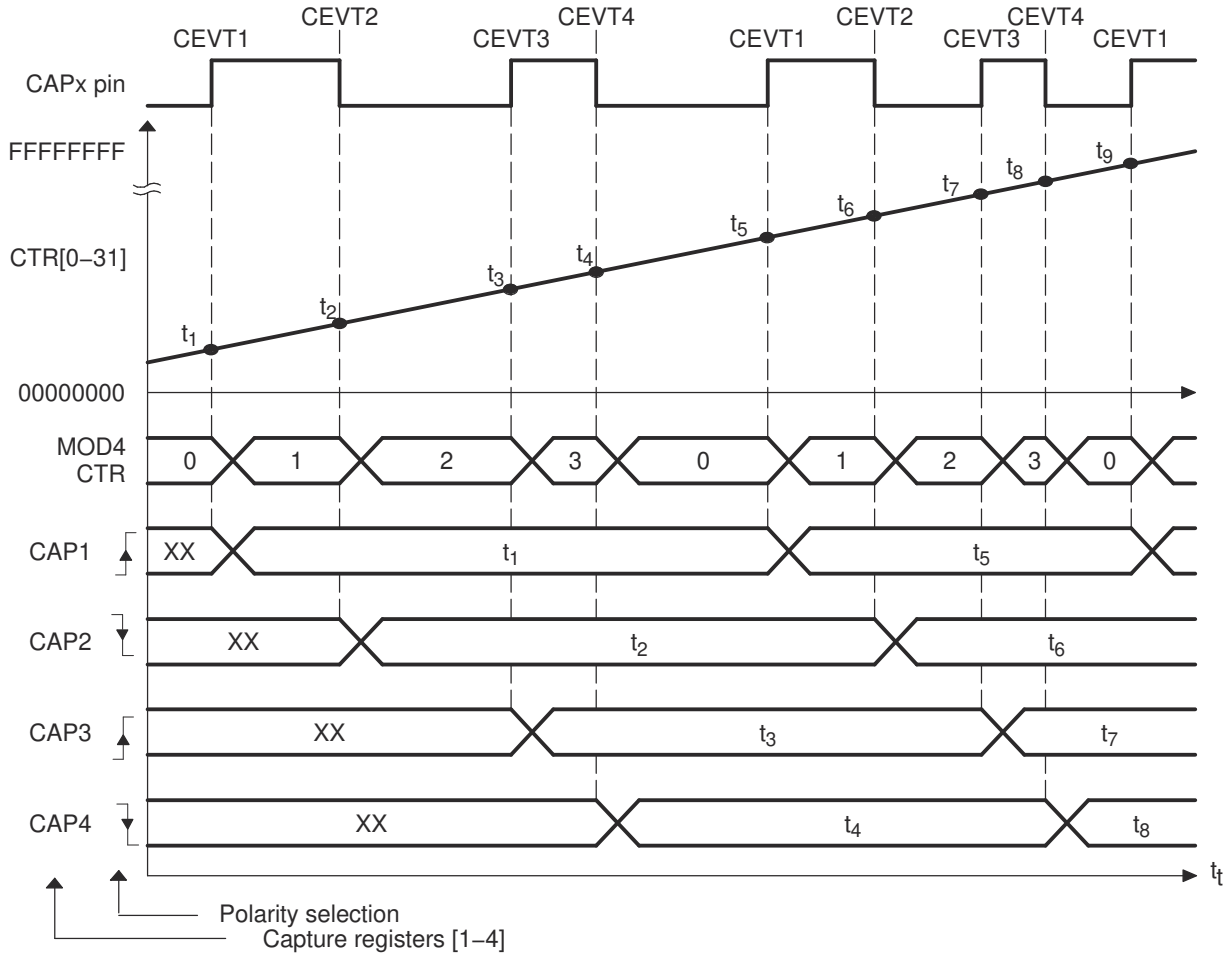


Figure 23-14. Capture Sequence for Absolute Time-stamp with Rising- and Falling-Edge Detect

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23.6.3 Example 3 - Time Difference (Delta) Operation Rising-Edge Trigger

Figure 23-15 shows how the eCAP module can be used to collect delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCTR counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCTR is reset back to zero on every valid event. Here capture events are qualified as rising edge only. On an event, TSCTR contents (Time-Stamp) is captured first, and then TSCTR is reset to zero. The Mod4 counter then increments to the next state. If TSCTR reaches FFFFFFFF (maximum value), before the next event, the Mod4 counter wraps around to 00000000 and continues, a CNTOVF (counter overflow) flag is set, and an interrupt (if enabled) occurs. The advantage of Delta-time mode is that the CAPx contents directly give timing data without the need for CPU calculations, that is, Period1 = T_1, Period2 = T_2, and so on. As shown in Figure 23-15, the CEVT1 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

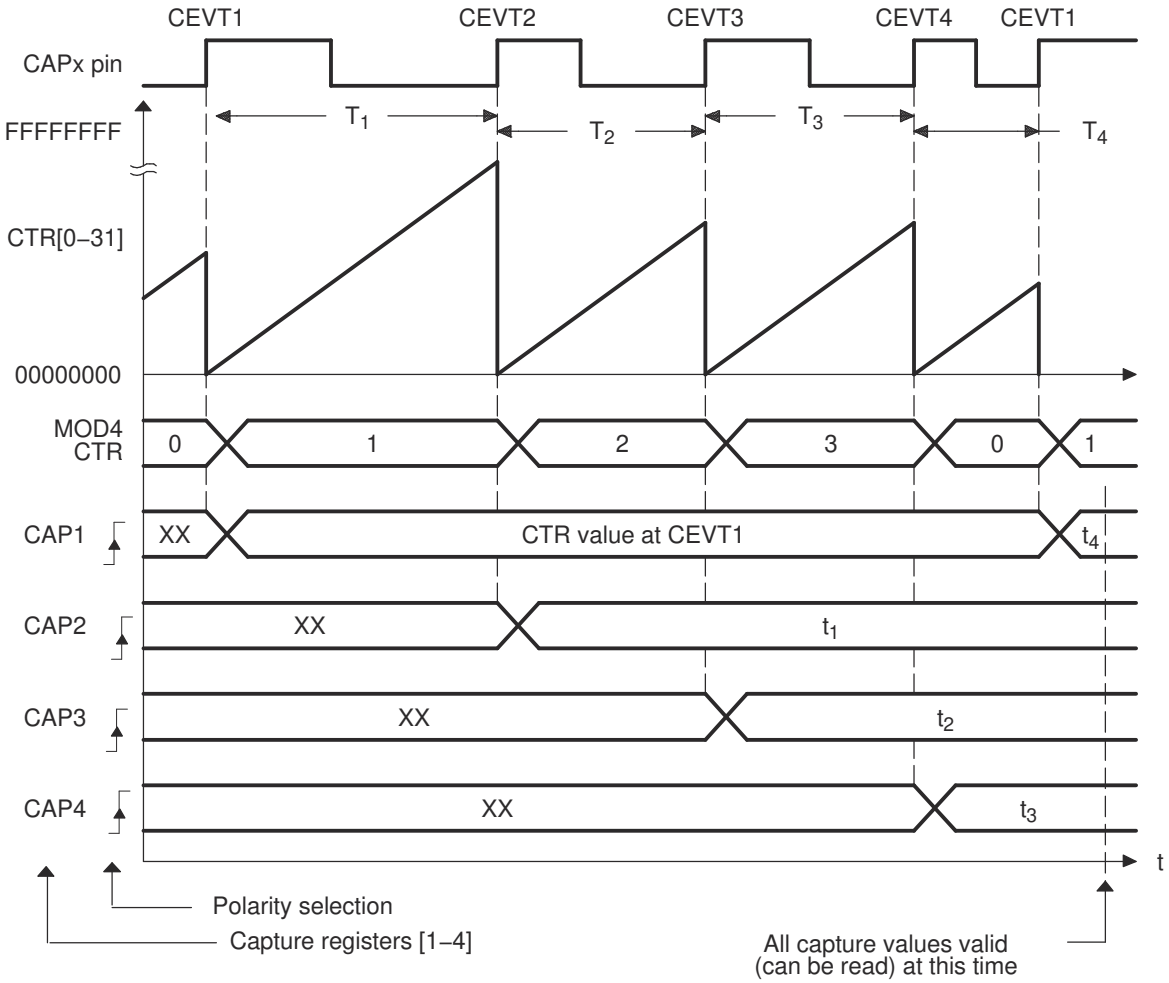


Figure 23-15. Capture Sequence for Delta Mode Time-stamp and Rising Edge Detect

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23.6.4 Example 4 - Time Difference (Delta) Operation Rising- and Falling-Edge Trigger

In Figure 23-16, the eCAP operating mode is almost the same as in previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information, that is: Period1 = T_1+T_2, Period2 = T_3+T_4, and so on. Duty Cycle1 (on-time %) = T_1 / Period1 x 100%, Duty Cycle1 (off-time %) = T_2 / Period1 x 100%, and so on.

During initialization, write to the active registers for both period and compare. This action automatically copies the init values into the shadow values. For subsequent compare updates during run-time, the shadow registers must be used.

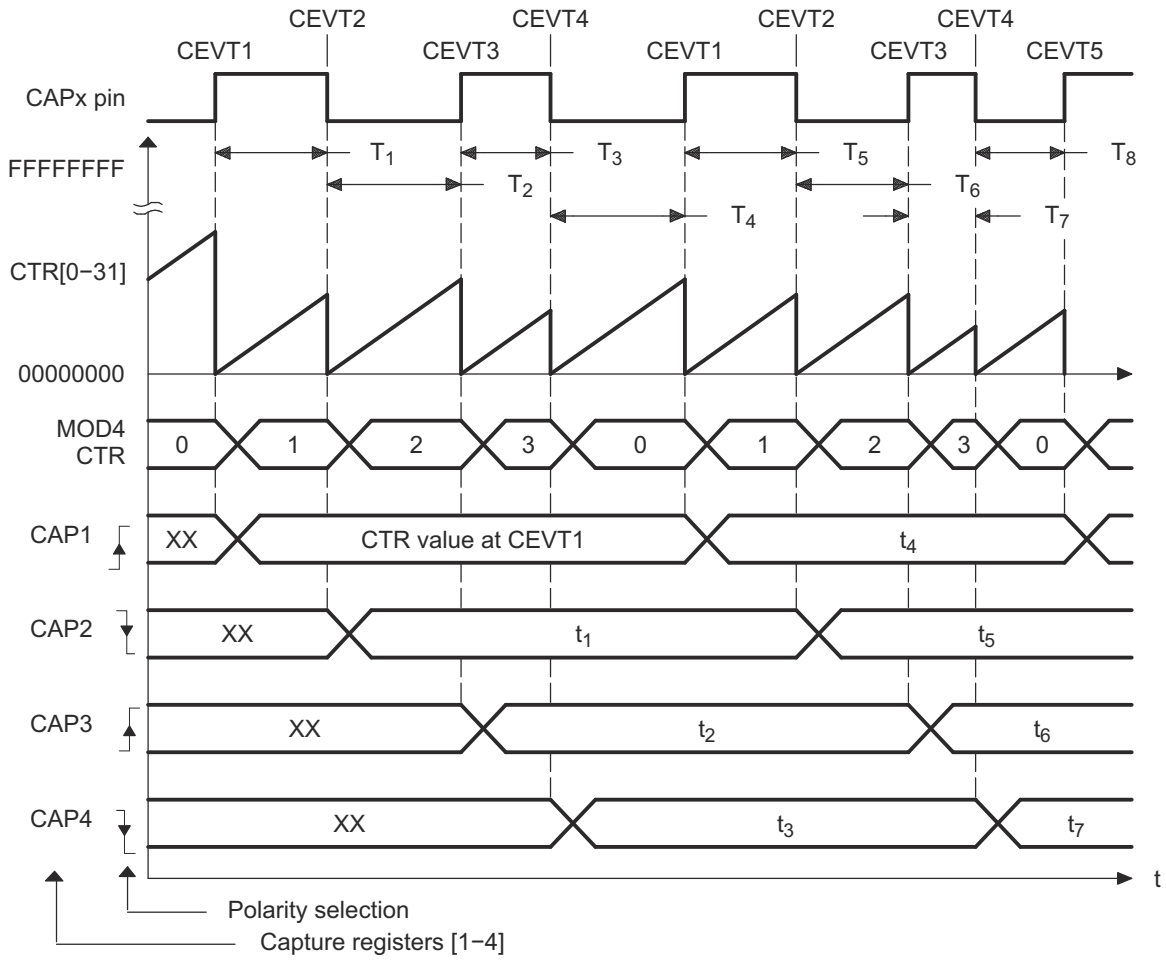


Figure 23-16. Capture Sequence for Delta Mode Time-stamp with Rising- and Falling-Edge Detect

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23.7 Application of the APWM Mode

In this example, the eCAP module is configured to operate as a PWM generator. Here, a very simple single-channel PWM waveform is generated from the APWMx output pin. The PWM polarity is active high, which means that the compare value (CAP2 reg is now a compare register) represents the on-time (high level) of the period. Alternatively, if the APWMPOL bit is configured for active low, then the compare value represents the off-time.

23.7.1 Example 1 - Simple PWM Generation (Independent Channels)

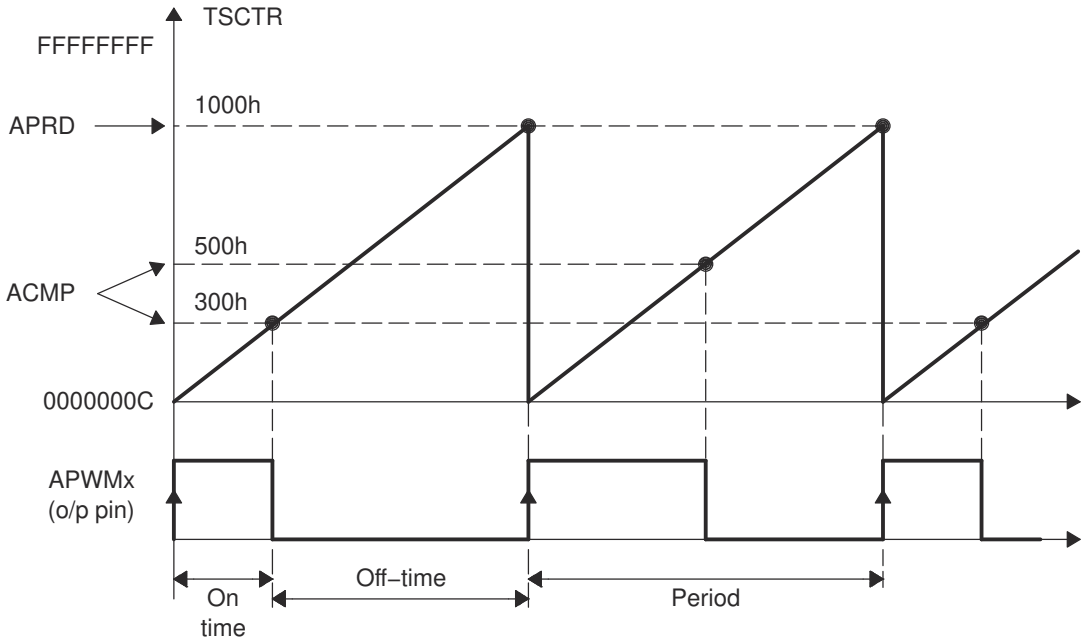


Figure 23-17. PWM Waveform Details of APWM Mode Operation

23.8 ECAP Interrupts & Triggers

23.8.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 23-4. CPU Interrupts Triggered by ECAP

NVIC Interrupt Name	Peripheral Instance Name	Register Group	ECAP Interrupt Configuration Registers	Description
ECAP0	ECAP0	N/A	ECEINT, ECEFLG, ECCLR, ECFRC	ECAP0 interrupt. Multiple OR'd, configurable source conditions.
ECAP1	ECAP1	N/A	ECEINT, ECEFLG, ECCLR, ECFRC	ECAP1 interrupt. Multiple OR'd, configurable source conditions.
ECAP2	ECAP2	N/A	ECEINT, ECEFLG, ECCLR, ECFRC	ECAP2 interrupt. Multiple OR'd, configurable source conditions.

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23.8.1.1 Interrupt Control

Operation and features of the eCAP interrupt control include (see Figure 23-18):

- An interrupt can be generated on capture events (CEVT1-CEVT4, CTROVF) or APWM events (CTR = PRD, CTR = CMP).
- A counter overflow event (FFFFFFFF->00000000) is also provided as an interrupt source (CTROVF).
- The capture events are edge and sequencer-qualified (ordered in time) by the polarity select and Mod4 gating, respectively.
- One of these events can be selected as the interrupt source (from the eCAPx module) going to the Interrupt Controller.
- Seven interrupt events (CEVT1, CEVT2, CEVT3, CEVT4, CNTOVF, CTR=PRD, CTR=CMP) can be generated.
- The interrupt enable register (ECEINT) is used to enable/disable individual interrupt event sources. The interrupt flag register (ECFLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is generated to the interrupt controller only if any of the interrupt events are enabled, the flag bit is 1, and the INT flag bit is 0. The interrupt service routine must clear the global interrupt flag bit and the serviced event using the interrupt clear register (ECCLR) before any other interrupt pulses are generated. All interrupt flags are cleared upon an event filter reset by writing a 1 to ECCTL2[CLRFILTRESET]. To force an interrupt event, use the interrupt force register (ECFRC). Forced interrupts can be used for test purposes.

Note

The CEVT1, CEVT2, CEVT3, CEVT4 flags are only active in capture mode (ECCTL2[CAP/APWM == 0]). The CTR=PRD, CTR=CMP flags are only valid in APWM mode (ECCTL2[CAP/APWM == 1]). CNTOVF flag is valid in both modes.

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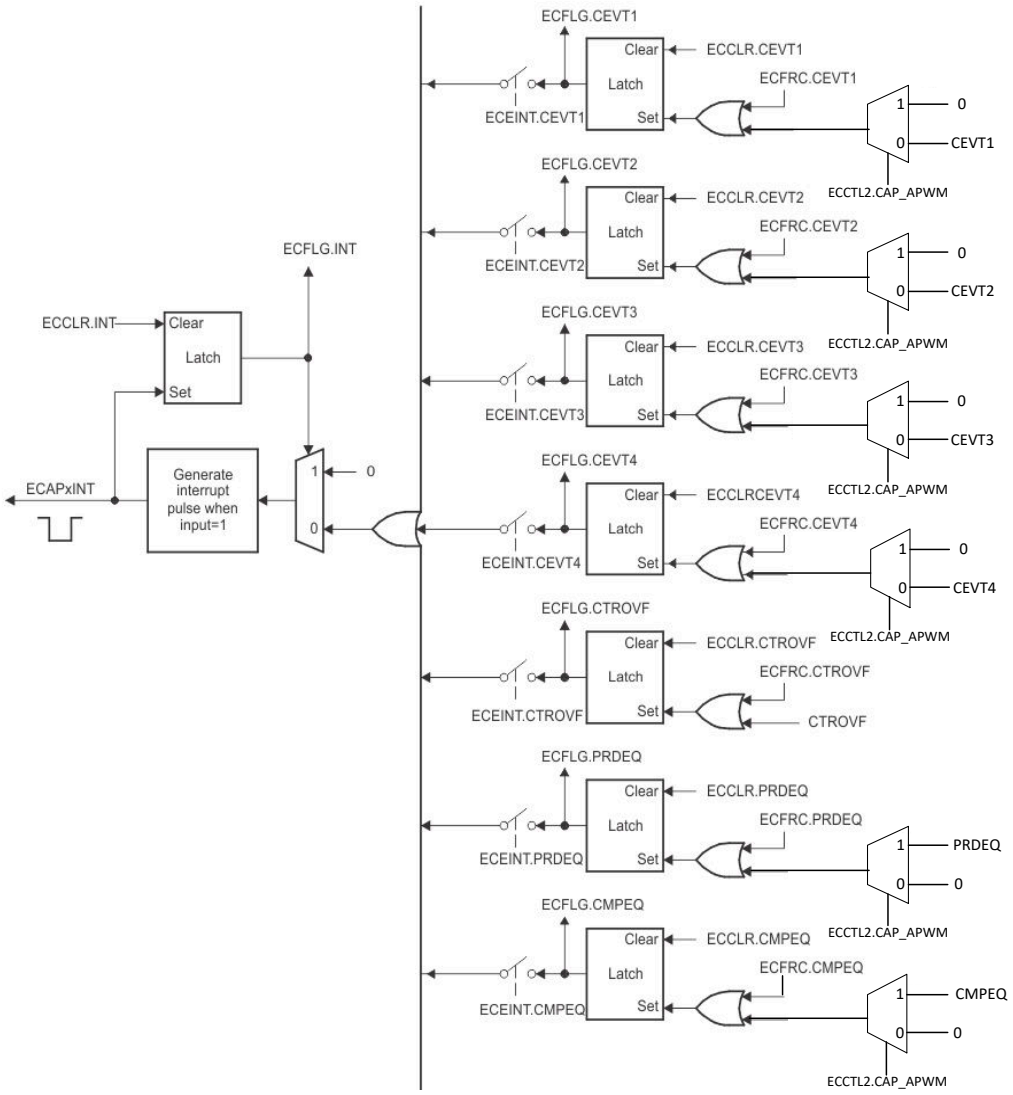


Figure 23-18. Interrupts in eCAP Module

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23.8.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 23-5. DMA Triggers from the ECAP

Trigger Name	Peripheral Instance Name	Register Group	ECAP DMA Configuration Registers	Description
ECAP0DMA	ECAP0	N/A	DMAEVTSEL	ECAP0 DMA trigger. Single, configurable source condition.
ECAP1DMA	ECAP1	N/A	DMAEVTSEL	ECAP1 DMA trigger. Single, configurable source condition.
ECAP2DMA	ECAP2	N/A	DMAEVTSEL	ECAP2 DMA trigger. Single, configurable source condition.

23.9 ECAP Registers

This Section describes the ECAP Registers.

23.9.1 ECAP Base Address Table

Table 23-6. ECAP Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
ECap0Regs	ECAP_REGS	ECAP0	0x4044_0000
ECap1Regs	ECAP_REGS	ECAP1	0x4044_1000
ECap2Regs	ECAP_REGS	ECAP2	0x4044_2000

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23.9.2 ECAP_REGS Registers

Table 23-7 lists the memory-mapped registers for the ECAP_REGS registers. All register offset addresses not listed in Table 23-7 should be considered as reserved locations and the register contents should not be modified.

Table 23-7. ECAP_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	TSCTR	Time-Stamp Counter		Go
4h	CTRPHS	Counter Phase Offset Value Register		Go
8h	CAP1	Capture 1 Register		Go
Ch	CAP2	Capture 2 Register		Go
10h	CAP3	Capture 3 Register		Go
14h	CAP4	Capture 4 Register		Go
24h	ECCTL0	Capture Control Register 0		Go
28h	ECCTL1	Capture Control Register 1		Go
2Ah	ECCTL2	Capture Control Register 2		Go
2Ch	ECEINT	Capture Interrupt Enable Register		Go
2Eh	ECFLG	Capture Interrupt Flag Register		Go
30h	ECCLR	Capture Interrupt Clear Register		Go
32h	ECFRC	Capture Interrupt Force Register		Go
3Ch	ECAPSYNCINSEL	SYNC source select register		Go

Complex bit access types are encoded to fit into small table cells. Table 23-8 shows the codes that are used for access types in this section.

Table 23-8. ECAP_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

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1 TSCTR Register (Offset = 0h) [Reset = 00000000h]

TSCTR is shown in Figure 23-19 and described in Table 23-9.

Return to the Summary Table.

Time-Stamp Counter

Figure 23-19. TSCTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCTR																															
R/W-0h																															

Table 23-10. TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCTR	R/W	0h	Active 32-bit counter register that is used as the capture time-base HR mode : 1) This register reads HRCOUNTER value and is not writable 2) can be reset using CTRFILTRESET 3) Its not synchronized to SYSCLK domain so reads may not be accurate Reset type: SYSRSn

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2 CTRPHS Register (Offset = 4h) [Reset = 00000000h]

CTRPHS is shown in Figure 23-20 and described in Table 23-10.

Return to the Summary Table.

Counter Phase Offset Value Register

Figure 23-20. CTRPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTRPHS																															
R/W-0h																															

Table 23-12. CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CTRPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and PWM time-bases. This register is not applicable in HR mode. Reset type: SYSRSn

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3 CAP1 Register (Offset = 8h) [Reset = 00000000h]

CAP1 is shown in Figure 23-21 and described in Table 23-11.

Return to the Summary Table.

Capture 1 Register

Figure 23-21. CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

Table 23-14. CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by: - Time-Stamp counter value (TSCTR) during a capture event - Software - may be useful for test purposes or initialization - ARPD shadow register (CAP3) when used in APWM mode Reset type: SYSRSn

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4 CAP2 Register (Offset = Ch) [Reset = 00000000h]

CAP2 is shown in Figure 23-22 and described in Table 23-12.

Return to the Summary Table.

Capture 2 Register

Figure 23-22. CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

Table 23-16. CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by: - Time-Stamp (counter value) during a capture event - Software - may be useful for test purposes - ACMP shadow register (CAP4) when used in APWM mode Reset type: SYSRSn

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5 CAP3 Register (Offset = 10h) [Reset = 00000000h]

CAP3 is shown in Figure 23-23 and described in Table 23-13.

Return to the Summary Table.

Capture 3 Register

Figure 23-23. CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3																															
R/W-0h																															

Table 23-18. CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. You can update the PWM period value through this register. CAP3 (APRD) shadows CAP1 in this mode. Reset type: SYSRSn

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6 CAP4 Register (Offset = 14h) [Reset = 00000000h]

CAP4 is shown in Figure 23-24 and described in Table 23-14.

Return to the Summary Table.

Capture 4 Register

Figure 23-24. CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

Table 23-20. CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. You can update the PWM compare value via this register. CAP4 (ACMP) shadows CAP2 in this mode. Reset type: SYSRSn

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7 ECCTL0 Register (Offset = 24h) [Reset = 0000007Fh]

ECCTL0 is shown in Figure 23-25 and described in Table 23-15.

Return to the Summary Table.

Capture Control Register 0

Figure 23-25. ECCTL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									INPUTSEL						
R-0-0h									R/W-7Fh						

Table 23-22. ECCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R-0	0h	Reserved
6-0	INPUTSEL	R/W	7Fh	Capture input source select bits 0000000 capture input is ECAPxINPUT[0] 0000001 capture input is ECAPxINPUT[1] 0000010 capture input is ECAPxINPUT[2] ... 1111111 capture input is ECAPxINPUT[127] Reset type: CPU1.SYSRSn

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8 ECCTL1 Register (Offset = 28h) [Reset = 0000h]

ECCTL1 is shown in Figure 23-26 and described in Table 23-16.

Return to the Summary Table.

Capture Control Register 1

Figure 23-26. ECCTL1 Register

15	14	13	12	11	10	9	8
FREE_SOFT		PRESCALE					CAPLDEN
R/W-0h		R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 23-24. ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Control Reset type: SYSRSn 0h (R/W) = TSCTR counter stops immediately on emulation suspend 1h (R/W) = TSCTR counter runs until = 0 2h (R/W) = TSCTR counter is unaffected by emulation suspend (Run Free) 3h (R/W) = TSCTR counter is unaffected by emulation suspend (Run Free)
13-9	PRESCALE	R/W	0h	Event Filter prescale select Reset type: SYSRSn 0h (R/W) = Divide by 1 (i.e,. no prescale, by-pass the prescaler) 1h (R/W) = Divide by 2 2h (R/W) = Divide by 4 3h (R/W) = Divide by 6 4h (R/W) = Divide by 8 5h (R/W) = Divide by 10 1Eh (R/W) = Divide by 60 1Fh (R/W) = Divide by 62
8	CAPLDEN	R/W	0h	Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated. Reset type: SYSRSn 0h (R/W) = Disable CAP1-4 register loads at capture event time. 1h (R/W) = Enable CAP1-4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 Reset type: SYSRSn 0h (R/W) = Do not reset counter on Capture Event 4 (absolute time stamp operation) 1h (R/W) = Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select Reset type: SYSRSn 0h (R/W) = Capture Event 4 triggered on a rising edge (RE) 1h (R/W) = Capture Event 4 triggered on a falling edge (FE)

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Table 23-24. ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 Reset type: SYSRSn 0h (R/W) = Do not reset counter on Capture Event 3 (absolute time stamp) 1h (R/W) = Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select Reset type: SYSRSn 0h (R/W) = Capture Event 3 triggered on a rising edge (RE) 1h (R/W) = Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 Reset type: SYSRSn 0h (R/W) = Do not reset counter on Capture Event 2 (absolute time stamp) 1h (R/W) = Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select Reset type: SYSRSn 0h (R/W) = Capture Event 2 triggered on a rising edge (RE) 1h (R/W) = Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 Reset type: SYSRSn 0h (R/W) = Do not reset counter on Capture Event 1 (absolute time stamp) 1h (R/W) = Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select Reset type: SYSRSn 0h (R/W) = Capture Event 1 triggered on a rising edge (RE) 1h (R/W) = Capture Event 1 triggered on a falling edge (FE)

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9 ECCTL2 Register (Offset = 2Ah) [Reset = 0006h]

ECCTL2 is shown in Figure 23-27 and described in Table 23-17.

Return to the Summary Table.

Capture Control Register 2

Figure 23-27. ECCTL2 Register

15	14	13	12	11	10	9	8
MODCNTRSTS		DMAEVTSEL		CTRFILTRESET	APWMPOL	CAP_APWM	SWSYNC
R-0h		R/W-0h		R-0/W1C-0h	R/W-0h	R/W-0h	R-0/W1S-0h
7	6	5	4	3	2	1	0
SYNCO_SEL		SYNCI_EN	TSCTRSTOP	REARM	STOP_WRAP		CONT_ONESHT
R/W-0h		R/W-0h	R/W-0h	R-0/W1S-0h	R/W-3h		R/W-0h

Table 23-26. ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	MODCNTRSTS	R	0h	This bit field reads current status on modulo counter 00b (R) = CAP1 register gets loaded on next capture event. 01b (R) = CAP2 register gets loaded on next capture event. 10b (R) = CAP3 register gets loaded on next capture event. 11b (R) = CAP4 register gets loaded on next capture event. Reset type: CPU1.SYSRSn
13-12	DMAEVTSEL	R/W	0h	DMA event select 00b (R/W) = DMA interrupt source is CEVT1 01b (R/W) = DMA interrupt source is CEVT2 10b (R/W) = DMA interrupt source is CEVT3 11b (R/W) = DMA interrupt source is CEVT4 Note: ECCTL1.CAPLDEN also needs to be set to '1' for ECAPxDMA_INT to be generated Reset type: CPU1.SYSRSn
11	CTRFILTRESET	R-0/W1C	0h	Reset Bit 0h (R) = No effect 1h (W) = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured. Reset type: CPU1.SYSRSn
10	APWMPOL	R/W	0h	APWM output polarity select. This is applicable only in APWM operating mode. Reset type: SYSRSn 0h (R/W) = Output is active high (Compare value defines high time) 1h (R/W) = Output is active low (Compare value defines low time)

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Table 23-26. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CAP_APWM	R/W	0h	CAP/APWM operating mode select Reset type: SYSRSn 0h (R/W) = ECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input 1h (R/W) = ECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output
8	SWSYNC	R-0/W1S	0h	Software-forced Counter (TSCTR) Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event. Reset type: SYSRSn 0h (R/W) = Writing a zero has no effect. Reading always returns a zero 1h (R/W) = Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero.
7-6	SYNCO_SEL	R/W	0h	Sync-Out Select Reset type: SYSRSn 0h (R/W) = sync out signal is SWSYNC 1h (R/W) = Select CTR = PRD event to be the sync-out signal. Note: Selection CTR = PRD is meaningful only in APWM mode 2h (R/W) = Disable sync out signal 3h (R/W) = Disable sync out signal
5	SYNCI_EN	R/W	0h	Counter (TSCTR) Sync-In select mode Reset type: SYSRSn 0h (R/W) = Disable sync-in option 1h (R/W) = Enable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	R/W	0h	Time Stamp (TSCTR) Counter Stop (freeze) Control Reset type: SYSRSn 0h (R/W) = TSCTR stopped 1h (R/W) = TSCTR free-running
3	REARM	R-0/W1S	0h	Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode Reset type: SYSRSn 0h (R/W) = Has no effect (reading always returns a 0) 1h (R/W) = Arms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads

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Table 23-26. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	STOP_WRAP	R/W	3h	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1-4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped (frozen) - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. Reset type: SYSRSn 0h (R/W) = Stop after Capture Event 1 in one-shot mode Wrap after Capture Event 1 in continuous mode. 1h (R/W) = Stop after Capture Event 2 in one-shot mode Wrap after Capture Event 2 in continuous mode. 2h (R/W) = Stop after Capture Event 3 in one-shot mode Wrap after Capture Event 3 in continuous mode. 3h (R/W) = Stop after Capture Event 4 in one-shot mode Wrap after Capture Event 4 in continuous mode.
0	CONT_ONESHT	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode) Reset type: SYSRSn 0h (R/W) = Operate in continuous mode 1h (R/W) = Operate in one-Shot mode

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10 ECEINT Register (Offset = 2Ch) [Reset = 0000h]

ECEINT is shown in Figure 23-28 and described in Table 23-18.

Return to the Summary Table.

The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows:
- Disable global interrupts
- Stop eCAP counter
- Disable eCAP interrupts
- Configure peripheral registers
- Clear spurious eCAP interrupt flags
- Enable eCAP interrupts
- Start eCAP counter
- Enable global interrupts

Figure 23-28. ECEINT Register

15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0h							R/W-0h
7	6	5	4	3	2	1	0
CTR_EQ_CMP	CTR_EQ_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 23-28. ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	CTR_EQ_CMP	R/W	0h	Counter Equal Compare Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Compare Equal as an Interrupt source 1h (R/W) = Enable Compare Equal as an Interrupt source
6	CTR_EQ_PRD	R/W	0h	Counter Equal Period Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Period Equal as an Interrupt source 1h (R/W) = Enable Period Equal as an Interrupt source
5	CTROVF	R/W	0h	Counter Overflow Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disabled counter Overflow as an Interrupt source 1h (R/W) = Enable counter Overflow as an Interrupt source
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Capture Event 4 as an Interrupt source 1h (R/W) = Capture Event 4 Interrupt Enable
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Capture Event 3 as an Interrupt source 1h (R/W) = Enable Capture Event 3 as an Interrupt source

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Table 23-28. ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Capture Event 2 as an Interrupt source 1h (R/W) = Enable Capture Event 2 as an Interrupt source
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable Reset type: SYSRSn 0h (R/W) = Disable Capture Event 1 as an Interrupt source 1h (R/W) = Enable Capture Event 1 as an Interrupt source
0	RESERVED	R	0h	Reserved

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11 ECFLG Register (Offset = 2Eh) [Reset = 0000h]

ECFLG is shown in Figure 23-29 and described in Table 23-19.

Return to the Summary Table.

Capture Interrupt Flag Register

Figure 23-29. ECFLG Register

15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0h							R-0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 23-30. ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	CTR_CMP	R	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR_PRD	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) reached the period register value (APRD) and was reset.
5	CTROVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the counter (TSCTR) has made the transition from FFFFFFFF to 00000000
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the fourth event occurred at ECAPx pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the third event occurred at ECAPx pin.
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the second event occurred at ECAPx pin.

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Table 23-30. ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates the first event occurred at ECAPx pin.
0	INT	R	0h	Global Interrupt Status Flag Reset type: SYSRSn 0h (R/W) = Indicates no event occurred 1h (R/W) = Indicates that an interrupt was generated.

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12 ECCLR Register (Offset = 30h) [Reset = 0000h]

ECCLR is shown in Figure 23-30 and described in Table 23-20.

Return to the Summary Table.

Capture Interrupt Clear Register

Figure 23-30. ECCLR Register

15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0h							R-0/W1C-0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 23-32. ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R-0/W1C	0h	Reserved
7	CTR_CMP	R-0/W1C	0h	Counter Equal Compare Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTR=CMP flag.
6	CTR_PRD	R-0/W1C	0h	Counter Equal Period Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTR=PRD flag.
5	CTROVF	R-0/W1C	0h	Counter Overflow Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CTROVF flag.
4	CEVT4	R-0/W1C	0h	Capture Event 4 Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT4 flag.
3	CEVT3	R-0/W1C	0h	Capture Event 3 Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT3 flag.
2	CEVT2	R-0/W1C	0h	Capture Event 2 Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT2 flag.
1	CEVT1	R-0/W1C	0h	Capture Event 1 Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the CEVT1 flag.

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Table 23-32. ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R-0/W1C	0h	ECAP Global Interrupt Status Clear Reset type: SYSRSn 0h (R/W) = Writing a 0 has no effect. Always reads back a 0 1h (R/W) = Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1

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13 ECFRC Register (Offset = 32h) [Reset = 0000h]

ECFRC is shown in Figure 23-31 and described in Table 23-21.

Return to the Summary Table.

Capture Interrupt Force Register

Figure 23-31. ECFRC Register

15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0h							R-0/W1S-0h
7	6	5	4	3	2	1	0
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0h

Table 23-34. ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R-0/W1S	0h	Reserved
7	CTR_CMP	R-0/W1S	0h	Force Counter Equal Compare Interrupt. This event is only active in APWM mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CTR_CMP flag.
6	CTR_PRD	R-0/W1S	0h	Force Counter Equal Period Interrupt. This event is only active in APWM mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CTR_PRD flag.
5	CTROVF	R-0/W1S	0h	Force Counter Overflow Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 to this bit sets the CTROVF flag.
4	CEVT4	R-0/W1S	0h	Force Capture Event 4. This event is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT4 flag.
3	CEVT3	R-0/W1S	0h	Force Capture Event 3. This event is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT3 flag.
2	CEVT2	R-0/W1S	0h	Force Capture Event 2. This event is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Writing a 1 sets the CEVT2 flag.
1	CEVT1	R-0/W1S	0h	Force Capture Event 1. This event is only active in CAP mode. Reset type: SYSRSn 0h (R/W) = No effect. Always reads back a 0. 1h (R/W) = Sets the CEVT1 flag.

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Table 23-34. ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0h	Reserved

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14 ECAPSYNCINSEL Register (Offset = 3Ch) [Reset = 00000001h]

ECAPSYNCINSEL is shown in Figure 23-32 and described in Table 23-22.

Return to the Summary Table.

SYNC source select register

Figure 23-32. ECAPSYNCINSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											SEL					
R-0h																											R/W-1h					

Table 23-36. ECAPSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	SEL	R/W	1h	These bits determines the source of SYNCIN signal. 0x0 : Disabled using SOC tieoff. 0x1-0x7F : Refer to MCPWM SYNCIN sources in MCPWM TRM chapter. Reset type: SYSRSn

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Chapter 24

Enhanced Quadrature Encoder Pulse (eQEP)

The enhanced quadrature encoder pulse (eQEP) module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine for use in a high-performance motion and position-control system.

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24.1 Introduction

An incremental encoder disk is patterned with a track of slots along the periphery, as shown in Figure 24-1. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark and light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position, and zero reference

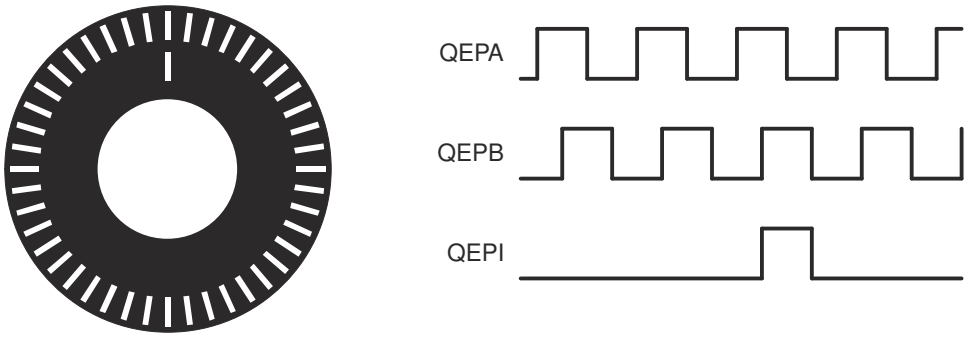
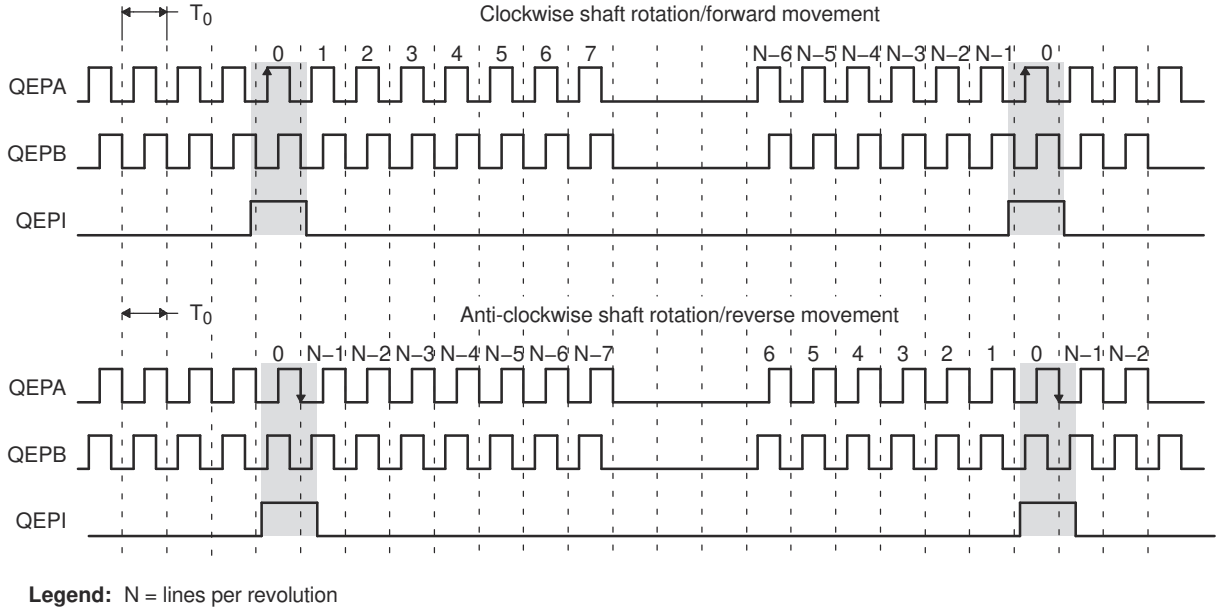


Figure 24-1. Optical Encoder Disk

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is detected with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90° out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and conversely, as shown in Figure 24-2.



Legend: N = lines per revolution

Figure 24-2. QEP Encoder Output Signal for Forward/Reverse Movement

The encoder wheel typically makes one revolution for every revolution of the motor, or the wheel can be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder

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directly coupled to a motor running at 5000 revolutions-per-minute (rpm) results in a frequency of 166.6kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

Quadrature encoders from different manufacturers come with two forms of index pulse (gated index pulse or ungated index pulse) as shown in Figure 24-3. A nonstandard form of index pulse is ungated. In the ungated configuration, the index edges are not necessarily coincident with A and B signals. The gated index pulse is aligned to any of the four quadrature edges and width of the index pulse and can be equal to a quarter, half, or full period of the quadrature signal.

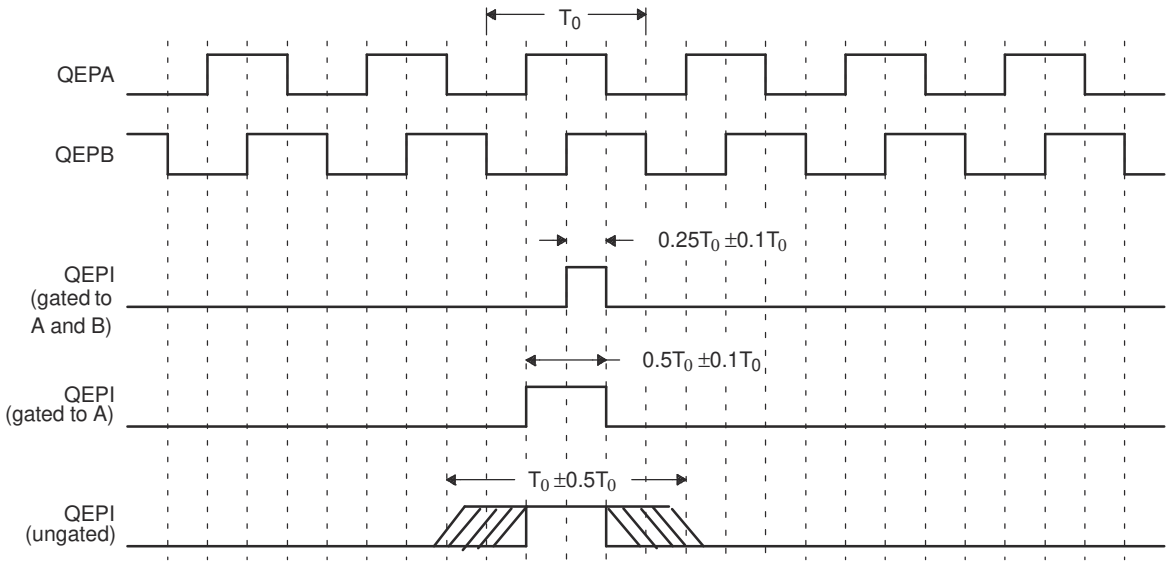


Figure 24-3. Index Pulse Example

Some typical applications of shaft encoders include robotics and computer input in the form of a mouse. Inside your mouse you can see where the mouse ball spins a pair of axles (a left/right, and an up/down axle). These axles are connected to optical shaft encoders that effectively tell the computer how fast and in what direction the mouse is moving.

General Issues: Estimating velocity from a digital position sensor is a cost-effective strategy in motor control. Two different first order approximations for velocity can be written as:

$$v(k) \approx \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad (36)$$

$$v(k) \approx \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (37)$$

where:

- v(k) = Velocity at time instant k
- x(k) = Position at time instant k
- x(k-1) = Position at time instant k-1
- T = Fixed unit time or inverse of velocity calculation rate
- ΔX = Incremental position movement in unit time
- t(k) = Time instant "k"
- t(k-1) = Time instant "k-1"
- X = Fixed unit position
- ΔT = Incremental time elapsed for unit position movement

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Equation 36 is the conventional approach to velocity estimation and requires a time base to provide a unit time event for velocity calculation. Unit time is basically the inverse of the velocity calculation rate.

The encoder count (position) is read once during each unit time event. The quantity [x(k) - x(k-1)] is formed by subtracting the previous reading from the current reading. Then the velocity estimate is computed by multiplying by the known constant 1/T (where T is the constant time between unit time events and is known in advance).

Estimation based on Equation 36 has an inherent accuracy limit directly related to the resolution of the position sensor and the unit time period T. For example, consider a 500 line-per-revolution quadrature encoder with a velocity calculation rate of 400Hz. When used for position, the quadrature encoder gives a four-fold increase in resolution; in this case, 2000 counts-per-revolution. The minimum rotation that can be detected is, therefore, 0.0005 revolutions, which gives a velocity resolution of 12rpm when sampled at 400Hz. While this resolution can be satisfactory at moderate or high speeds, for example 1% error at 1200rpm, this resolution clearly proves inadequate at low speeds. In fact, at speeds below 12rpm, the speed estimate is erroneously zero much of the time.

At low speed, Equation 37 provides a more accurate approach. This method requires a position sensor that outputs a fixed interval pulse train, such as the aforementioned quadrature encoder. The width of each pulse is defined by motor speed for a given sensor resolution. Equation 37 can be used to calculate motor speed by measuring the elapsed time between successive quadrature pulse edges. However, this method suffers from the opposite limitation, as does Equation 36. A combination of relatively large motor speeds and high sensor resolution makes the time interval ΔT small, and thus more greatly influenced by the timer resolution. This can introduce considerable error into high-speed estimates.

For systems with a large speed range (that is, speed estimation is needed at both low and high speeds), one approach is to use Equation 37 at low speed and have the DSP software switch over to Equation 36 when the motor speed rises above some specified threshold.

24.1.1 EQEP Related Collateral

Foundational Materials

- Interfacing with Quadrature Encoders (Video)
- *Real-Time Control Reference Guide*
  - Refer to the Encoders section

24.2 Configuring Device Pins

There are no dedicated pinmux mode options to connect EQEP signals to the device pins. Instead, any GPIO can be used configured to supply the EQEP inputs via the Input XBAR.

See the Crossbar (XBAR) chapter for more details on the INPUTXBAR mux and settings.

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24.3 Description

This section provides the eQEP inputs, memory map, and functional description.

24.3.1 EQEP Inputs

The eQEP inputs include two pins for quadrature-clock mode or direction-count mode, an index (or 0 marker), and a strobe input. The eQEP module requires that the QEPA, QEPB, and QEPI inputs are synchronized to MCLK prior to entering the module.

- **QEPA/XCLK and QEPB/XDIR:** These two pins can be used in quadrature-clock mode or direction-count mode.
  - Quadrature-clock Mode: The eQEP encoders provide two square wave signals (A and B) 90 electrical degrees out of phase. This phase relationship is used to determine the direction of rotation of the input shaft and number of eQEP pulses from the index position to derive the relative position information. For forward or clockwise rotation, QEPA signal leads QEPB signal and conversely. The quadrature decoder uses these two inputs to generate quadrature-clock and direction signals.
  - Direction-count Mode: In direction-count mode, direction and clock signals are provided directly from the external source. Some position encoders have this type of output instead of quadrature output. The QEPA pin provides the clock input and the QEPB pin provides the direction input.
- **QEPI: Index or Zero Marker:** The eQEP encoder uses an index signal to assign an absolute start position from which position information is incrementally encoded using quadrature pulses. This pin is connected to the index output of the eQEP encoder to optionally reset the position counter for each revolution. This signal can be used to initialize or latch the position counter on the occurrence of a desired event on the index pin.
- **QEPS: Strobe Input:** This general-purpose strobe signal can initialize or latch the position counter on the occurrence of a desired event on the strobe pin. This signal is typically connected to a sensor or limit switch to notify that the motor has reached a defined position.

Input signals to the eQEP (QEPA, QEPB, QEPI and QEPS) can come from multiple sources; that is, device pin, CMPSSx, Input X-BAR, or PWMXBARx. One typical use case is if SinCos transducers are used in the motor control system to estimate the position of motor shaft and Index signal is coming from traditional rotary encoder, source of the eQEP signals (QEPA, QEPB and QEPI) can be configured as output of CMPSSx that decodes the Sin, Cos, and Index signals. Figure 24-4 illustrates this.

Selection of the source of Input signals (QEPA, QEPB, and QEPI) is user-configurable through the QEPSRCSEL register as shown in Table 24-1.

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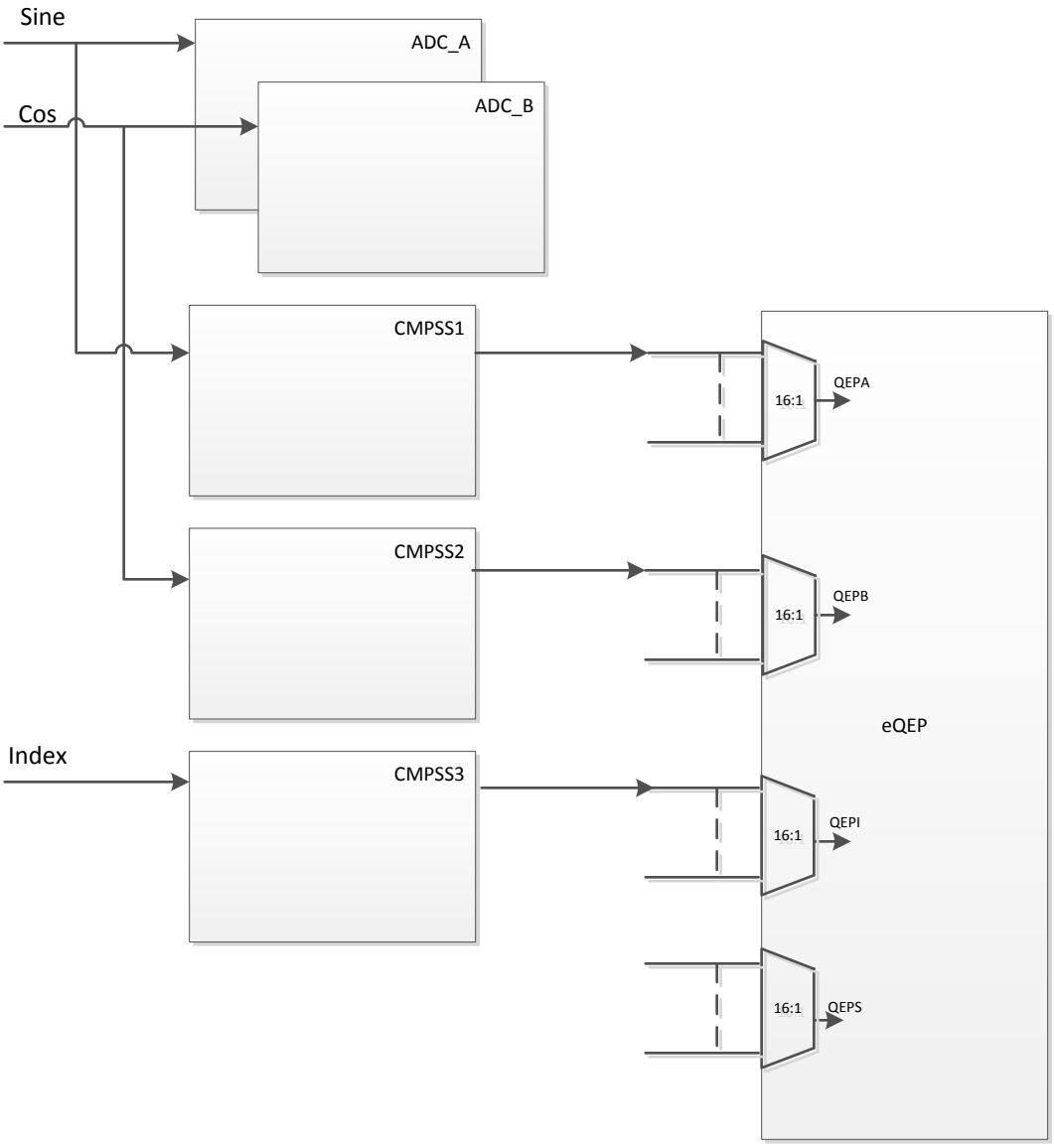


Figure 24-4. Using eQEP to Decode Signals from SinCos Transducer

Table 24-1. eQEP Input Source Select Table

QEPASEL, QEPBSEL, QEPISEL, QEPSSEL	Input Signal
0	INPUTXBAR
1	CMPSS0_CTRIPH
2	CMPSS1_CTRIPH
3	CMPSS2_CTRIPH
4	CMPSS3_CTRIPH
5	PWMXBAR1
6	PWMXBAR2
7	PWMXBAR3
8	PWMXBAR4
9	PWMXBAR5

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Table 24-1. eQEP Input Source Select Table (continued)

QEPASEL, QEPBSEL, QEPISEL, QEPSSEL	Input Signal
10	PWMXBAR6
11	PWMXBAR7
12	PWMXBAR8
13	Reserved
14	Reserved
15	Reserved

Note

Configuration of QEPSRCSEL register to select the source of QEPA, QEPB, and QEPI signals can lead to unexpected transition on these signals, which can cause an undesirable outcome if eQEP is already running. Make sure that the eQEP is disabled before configuring the QEPSRCSEL register for input signals.

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24.3.2 Functional Description

The eQEP peripheral contains the following major functional units (as shown in Figure 24-5):

- Programmable input qualification for each pin (part of the Input X-BAR)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

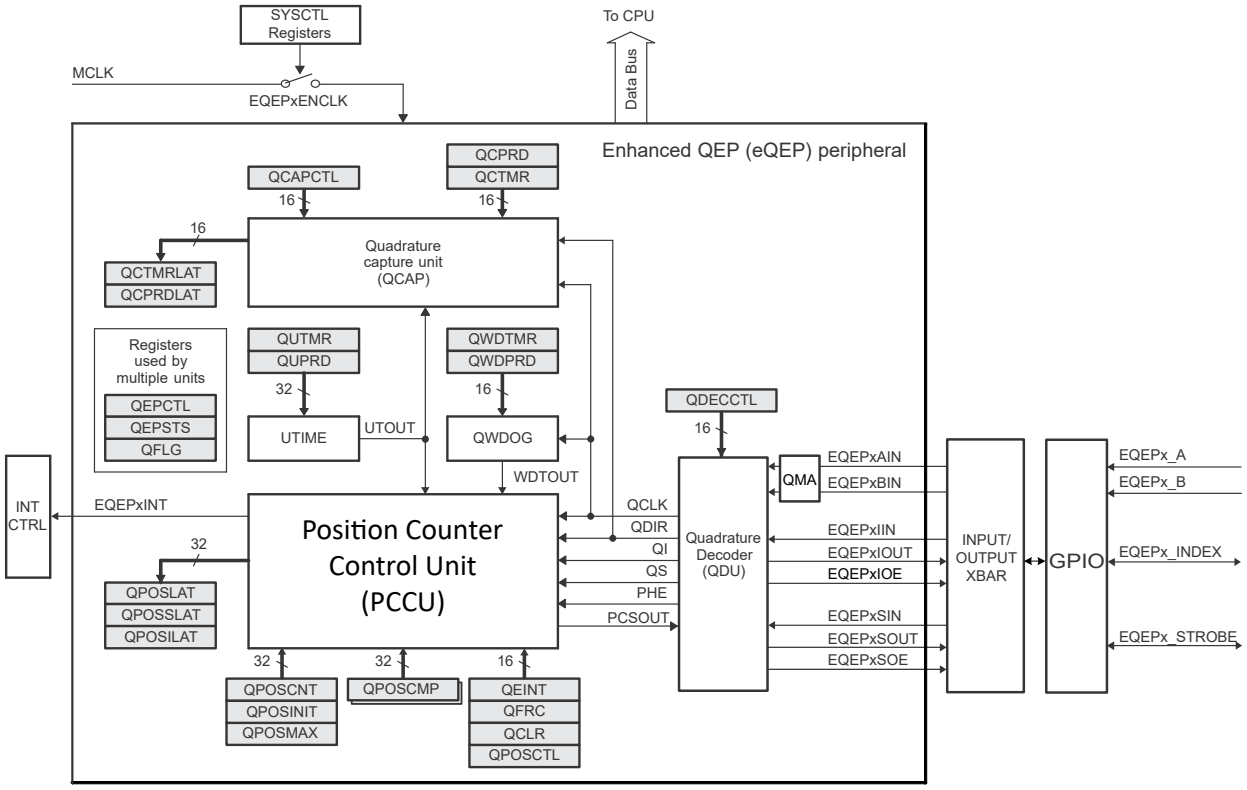


Figure 24-5. Functional Block Diagram of the eQEP Peripheral

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24.4 Quadrature Decoder Unit (QDU)

Figure 24-6 shows a functional block diagram of the QDU.

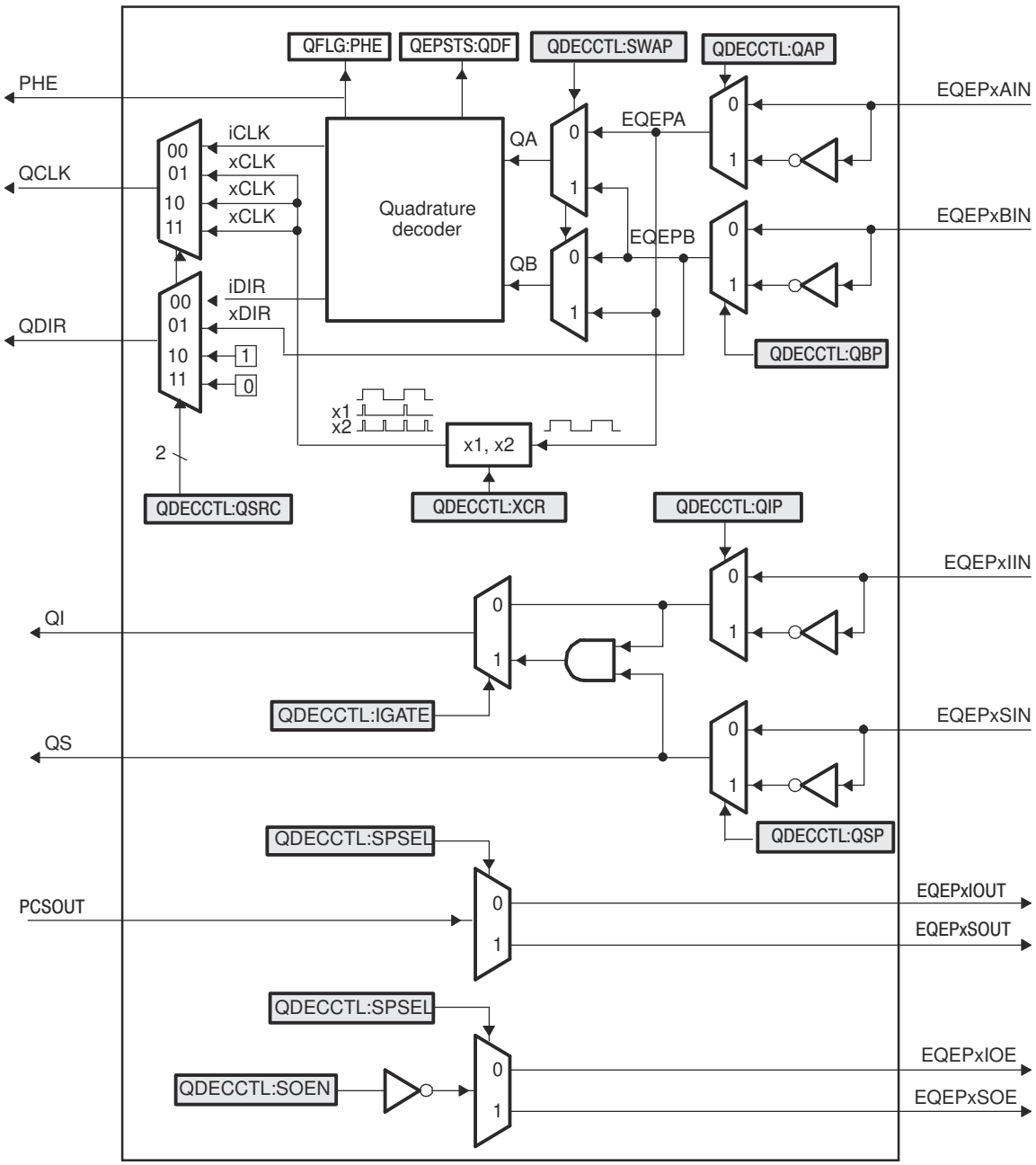


Figure 24-6. Functional Block Diagram of Decoder Unit

24.4.1 Position Counter Input Modes

Clock and direction input to the position counter is selected using QDECCTL[QSRC] bits, based on interface input requirement as follows:

- Quadrature-count mode
- Direction-count mode
- UP-count mode
- DOWN-count mode

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24.4.1.1 Quadrature Count Mode

The quadrature decoder generates the direction and clock to the position counter in quadrature count mode.

Direction Decoding

The direction decoding logic of the eQEP circuit determines which one of the sequences (QEPA, QEPB) is the leading sequence and accordingly updates the direction information in the QEPSTS[QDF] bit. Table 24-2 and Figure 24-7 show the direction decoding logic in truth table and state machine form. Both edges of the QEPA and QEPB signals are sensed to generate count pulses for the position counter. Therefore, the frequency of the clock generated by the eQEP logic is four times that of each input sequence. Figure 24-8 shows the direction decoding and clock generation from the eQEP input signals.

Table 24-2. Quadrature Decoder Truth Table

Previous Edge	Present Edge	QDIR	QPOSCNT
QA↑	QB↑	UP	Increment
	QB↓	DOWN	Decrement
	QA↓	TOGGLE	Increment or Decrement
QA↓	QB↓	UP	Increment
	QB↑	DOWN	Decrement
	QA↑	TOGGLE	Increment or Decrement
QB↑	QA↑	DOWN	Decrement
	QA↓	UP	Increment
	QB↓	TOGGLE	Increment or Decrement
QB↓	QA↓	DOWN	Decrement
	QA↑	UP	Increment
	QB↑	TOGGLE	Increment or Decrement

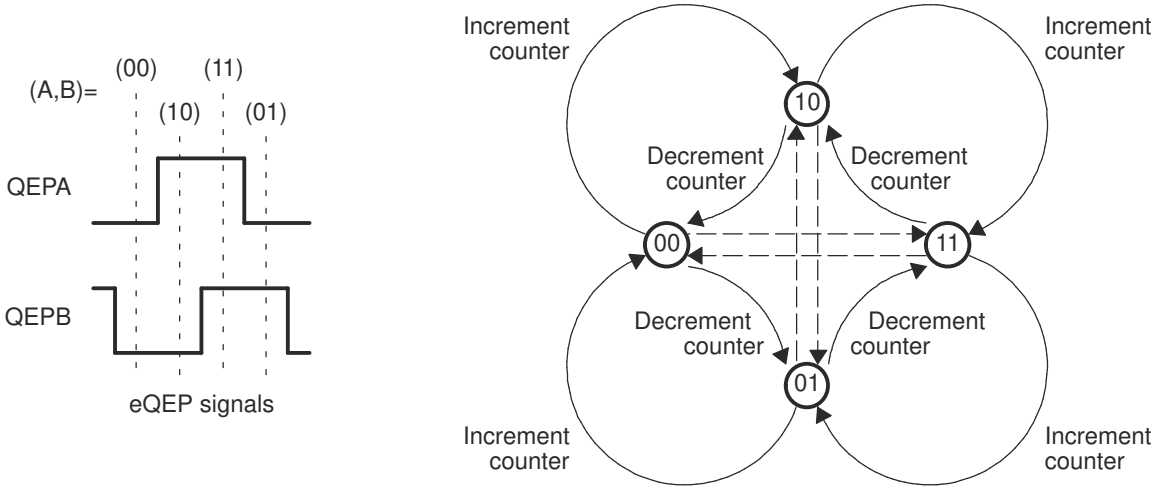


Figure 24-7. Quadrature Decoder State Machine

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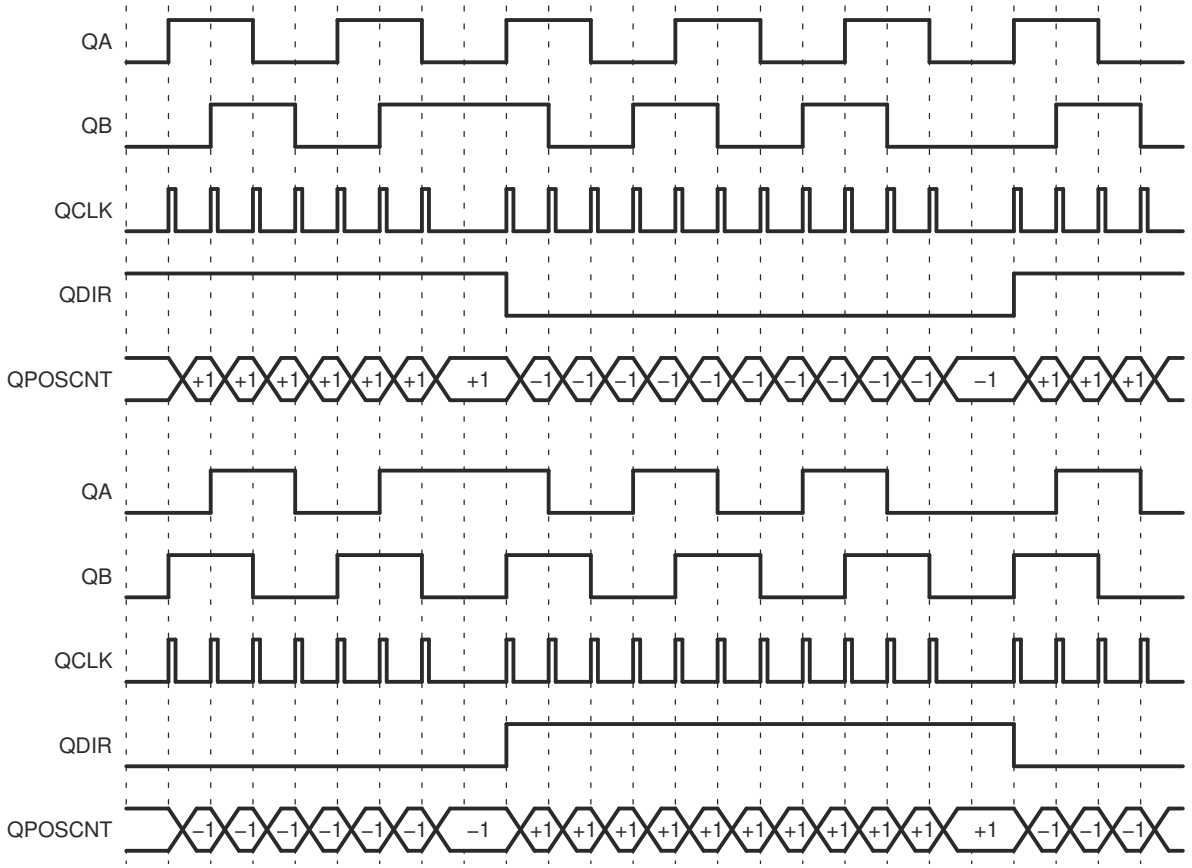


Figure 24-8. Quadrature-clock and Direction Decoding

Phase Error Flag In normal operating conditions, quadrature inputs QEPA and QEPB is 90 degrees out of phase. The phase error flag (PHE) is set in the QFLG register and the QPOSCNT value can be incorrect and offset by multiples of 1 or 3. That is, when edge transition is detected simultaneously on the QEPA and QEPB signals to optionally generate interrupts. State transitions marked by dashed lines in Figure 24-7 are invalid transitions that generate a phase error.

Count Multiplication The eQEP position counter provides 4x times the resolution of an input clock by generating a quadrature-clock (QCLK) on the rising/falling edges of both eQEP input clocks (QEPA and QEPB) as shown in Figure 24-8.

Reverse Count In normal quadrature count operation, QEPA input is applied to the QA input of the quadrature decoder and the QEPB input is applied to the QB input of the quadrature decoder. Reverse counting is enabled by setting the SWAP bit in the QDECCTL register. This swaps the input to the quadrature decoder; thereby, reversing the counting direction.

24.4.1.2 Direction-Count Mode

Some position encoders provide direction and clock outputs, instead of quadrature outputs. In such cases, direction-count mode can be used. The QEPA input provides the clock for the position counter and the QEPB input has the direction information. The position counter is incremented on every rising edge of a QEPA input when the direction input is high, and decremented when the direction input is low.

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24.4.1.3 Up-Count Mode

The counter direction signal is hard-wired for up-count and the position counter is used to measure the frequency of the QEPA input. Clearing the QDECCTL[XCR] bit enables clock generation to the position counter on both edges of the QEPA input; thereby, increasing the measurement resolution by a factor of 2x. In up-count mode, we recommend that the application not configure QEPB as a GPIO mux option, or make sure that a signal edge is not generated on the QEPB input.

24.4.1.4 Down-Count Mode

The counter direction signal is hardwired for a down-count and the position counter is used to measure the frequency of the QEPA input. Clearing the QDECCTL[XCR] bit enables clock generation to the position counter on both edges of a QEPA input, thereby increasing the measurement resolution by a factor of 2x. In down-count mode, the application must not configure QEPB as a GPIO mux option or make sure that a signal edge is not generated on the QEPB input.

24.4.2 eQEP Input Polarity Selection

Each eQEP input can be inverted using QDECCTL[8:5] control bits. As an example, setting the QDECCTL[QIP] bit inverts the index input.

24.4.3 Position-Compare Sync Output

The enhanced eQEP peripheral includes a position-compare unit that is used to generate the position-compare sync signal on compare match between the position-counter register (QPOSCNT) and the position- compare register (QPOSCMP). This sync signal can be output using an index pin or strobe pin of the EQEP peripheral.

Setting the QDECCTL[SOEN] bit enables the position-compare sync output and the QDECCTL[SPSEL] bit selects either an eQEP index pin or an eQEP strobe pin.

24.5 Position Counter and Control Unit (PCCU)

The position-counter and control unit provides two configuration registers (QEPCTL and QPOSCTL) for setting up position-counter operational modes, position-counter initialization/latch modes and position-compare logic for sync signal generation.

24.5.1 Position Counter Operating Modes

Position-counter data can be captured in different manners. In some systems, the position counter is accumulated continuously for multiple revolutions and the position-counter value provides the position information with respect to the known reference. An example of this is the quadrature encoder mounted on the motor controlling the print head in the printer. Here the position counter is reset by moving the print head to the home position and then the position counter provides absolute position information with respect to home position.

In other systems, the position counter is reset on every revolution using index pulse, and the position counter provides a rotor angle with respect to the index pulse position.

The position counter can be configured to operate in following four modes

- Position-Counter Reset on Index Event
- Position-Counter Reset on Maximum Position
- Position-Counter Reset on the first Index Event
- Position-Counter Reset on Unit Time Out Event (Frequency Measurement)

In all the above operating modes, the position counter is reset to 0 on overflow and to the QPOSMAX register value on underflow. Overflow occurs when the position counter counts up after the QPOSMAX value. Underflow occurs when the position counter counts down after 0. The Interrupt flag is set to indicate overflow/underflow in QFLG register.

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24.5.1.1 Position Counter Reset on Index Event (QEPCTL[PCRM] = 00)

If the index event occurs during the forward movement, then the position counter is reset to 0 on the next eQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the QPOSMAX register on the next eQEP clock.

The first index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and direction on the first index event marker (QEPSTS[FIDF]) in QEPSTS registers, the eQEP peripheral also remembers the quadrature edge on the first index marker so that same relative quadrature transition is used for index event reset operation.

For example, if the first reset operation occurs on the falling edge of QEPB during the forward direction, then all the subsequent reset must be aligned with the falling edge of QEPB for the forward rotation and on the rising edge of QEPB for the reverse rotation as shown in Figure 24-9.

The position-counter value is latched to the QPOSILAT register and direction information is recorded in the QEPSTS[QDLF] bit on every index event marker. The position-counter error flag (QEPSTS[PCEF]) and error interrupt flag (QFLG[PCE]) are set if the latched value is not equal to 0 or QPOSMAX. The position-counter error flag (QEPSTS[PCEF]) is updated on every index event marker and an interrupt flag (QFLG[PCE]) is set on error that can be cleared only through software.

The index event latch configuration QEPCTL[IEL] must be configured to 00 or 11 when PRCM = 0 and the position counter error flag/interrupt flag are generated only in index event reset mode. The position counter value is latched into the IPOSLAT register on every index marker.

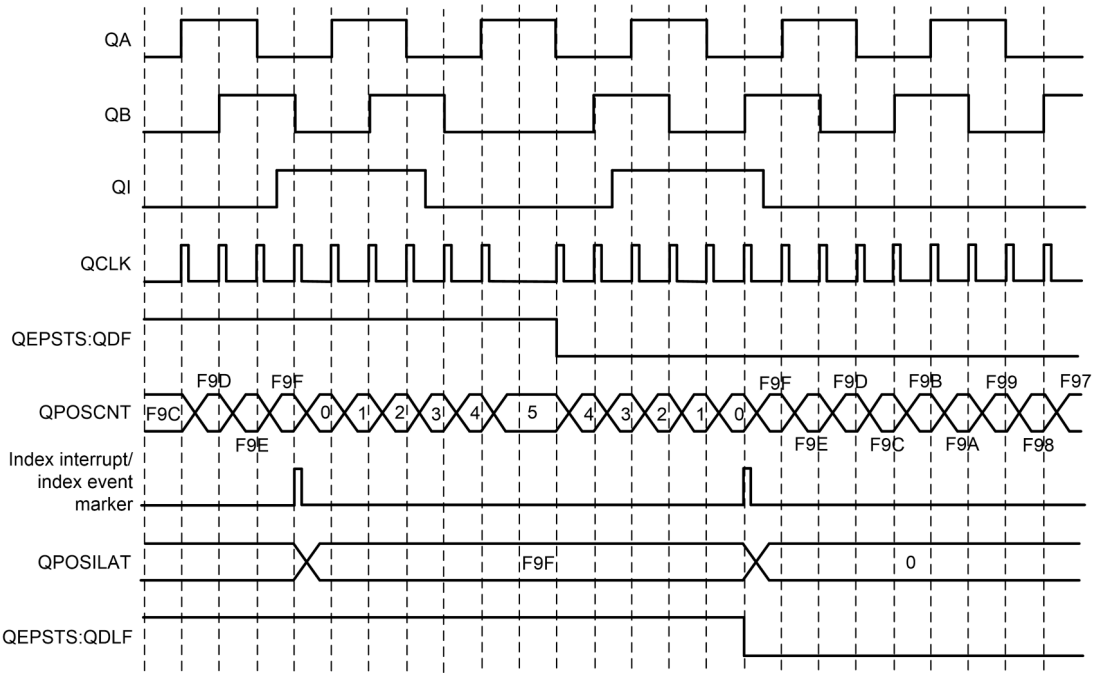


Figure 24-9. Position Counter Reset by Index Pulse for 1000-Line Encoder (QPOSMAX = 3999 or 0xF9F)

Note

In case of a boundary condition where the time period between the Index Event and the previous QCLK edge is less than MCLK period, then QPOSCNT gets reset to zero or QPOSMAX in the same MCLK cycle and does not wait for the next QCLK edge to occur.

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24.5.1.2 Position Counter Reset on Maximum Position (QEPCTL[PCRM] = 01)

If the position counter is equal to QPOSMAX, then the position counter is reset to 0 on the next eQEP clock for forward movement and position counter overflow flag is set. If the position counter is equal to ZERO, then the position counter is reset to QPOSMAX on the next QEP clock for reverse movement and position-counter underflow flag is set. Figure 24-10 shows the position-counter reset operation in this mode.

The first index marker fields (QEPSTS[FIDF] and QEPSTS[FIMF]) are not applicable in this mode.

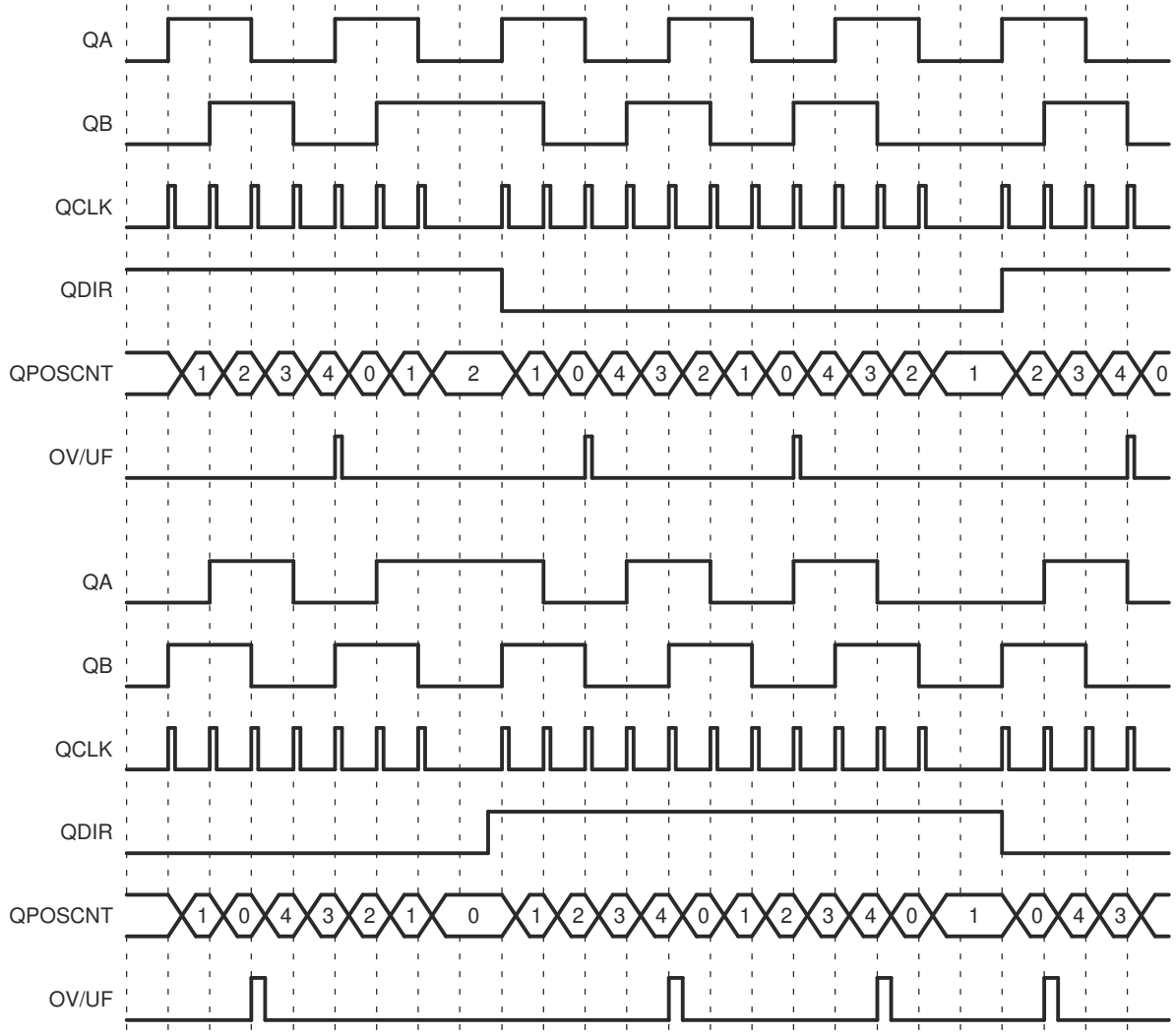


Figure 24-10. Position Counter Underflow/Overflow (QPOSMAX = 4)

24.5.1.3 Position Counter Reset on the First Index Event (QEPCTL[PCRM] = 10)

If the index event occurs during forward movement, then the position counter is reset to 0 on the next eQEP clock. If the index event occurs during the reverse movement, then the position counter is reset to the value in the QPOSMAX register on the next eQEP clock. Note that this is done only on the first occurrence and subsequently the position-counter value is not reset on an index event; rather, the position-counter value is reset based on the maximum position as described in Section 24.5.1.2 .

The first index marker fields (QEPSTS[FIDF] and QEPSTS[FIMF]) are not applicable in this mode.

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24.5.1.4 Position Counter Reset on Unit Time-out Event (QEPCTL[PCRM] = 11)

In this mode, QPOSCNT is set to 0 or QPOMAX, depending on the direction mode selected by QDECCTL[QSRC] bits on a unit time event. This is useful for frequency measurement.

24.5.2 Position Counter Latch

The eQEP index and strobe input can be configured to latch the position counter (QPOSCNT) into QPOSILAT and QPOSSLAT, respectively, on occurrence of a definite event on these pins.

24.5.2.1 Index Event Latch

In some applications, it is not desirable to reset the position counter on every index event and instead it can be required to operate the position counter in full 32-bit mode (QEPCTL[PCRM] = 01 and QEPCTL[PCRM] = 10 modes).

In such cases, the eQEP position counter can be configured to latch on the following events and direction information is recorded in the QEPSTS[QDLF] bit on every index event marker.

- Latch on Rising edge (QEPCTL[IEL] = 01)
- Latch on Falling edge (QEPCTL[IEL] = 10)
- Latch on Index Event Marker (QEPCTL[IEL] = 11)

This is particularly useful as an error checking mechanism to check if the position counter accumulated the correct number of counts between index events. As an example, the 1000-line encoder must count 4000 times when moving in the same direction between the index events.

The index event latch interrupt flag (QFLG[IEL]) is set when the position counter is latched to the QPOSILAT register. The index event latch configuration bits (QEPCTL[IEL]) are ignored when QEPCTL[PCRM] = 00.

Latch on Rising Edge (QEPCTL[IEL] = 01)	The position-counter value (QPOSCNT) is latched to the QPOSILAT register on every rising edge of an index input.
Latch on Falling Edge (QEPCTL[IEL] = 10)	The position-counter value (QPOSCNT) is latched to the QPOSILAT register on every falling edge of index input.
Latch on Index Event Marker/Software Index Marker (QEPCTL[IEL] = 11	The first index marker is defined as the quadrature edge following the first index edge. The eQEP peripheral records the occurrence of the first index marker (QEPSTS[FIMF]) and the direction on the first index event marker (QEPSTS[FIDF]) in the QEPSTS registers. The eQEP peripheral also remembers the quadrature edge on the first index marker so that the same relative quadrature transition is used for latching the position counter (QEPCTL[IEL] = 11).

Figure 24-11 shows the position counter latch using an index event marker.

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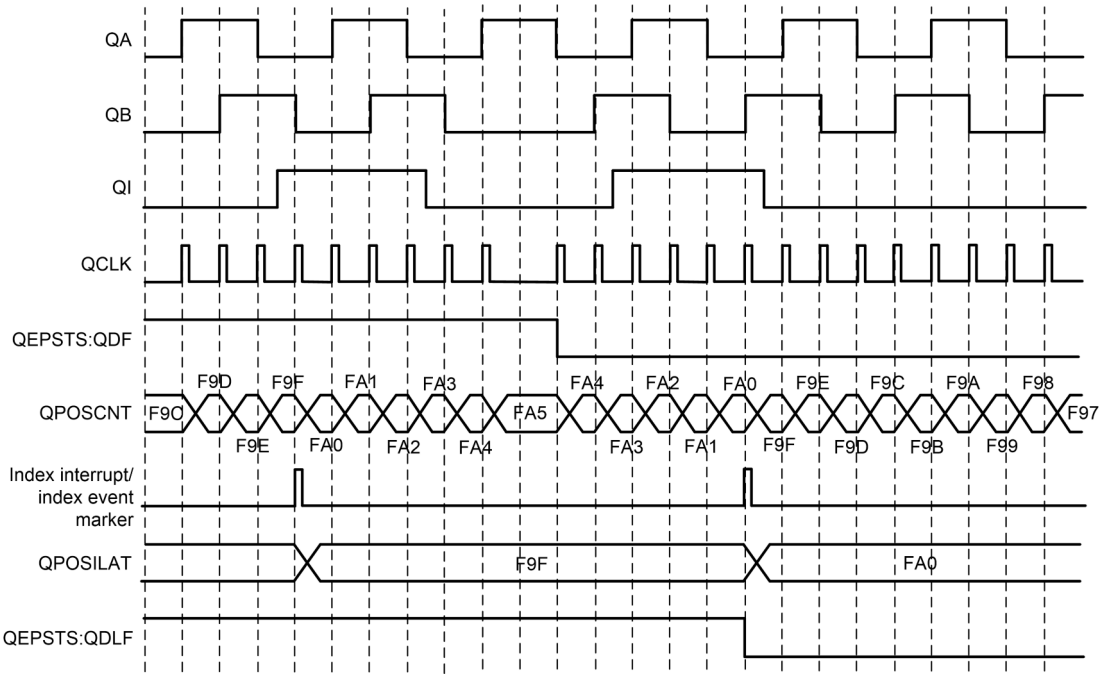


Figure 24-11. Software Index Marker for 1000-line Encoder (QEPCTL[IEL] = 1)

24.5.2.2 Strobe Event Latch

The position-counter value is latched to the QPOSSLAT register on the rising edge of the strobe input by clearing the QEPCTL[SEL] bit.

If the QEPCTL[SEL] bit is set, then the position-counter value is latched to the QPOSSLAT register on the rising edge of the strobe input for forward direction, and on the falling edge of the strobe input for reverse direction as shown in Figure 24-12.

The strobe event latch interrupt flag (QFLG[SEL) is set when the position counter is latched to the QPOSSLAT register.

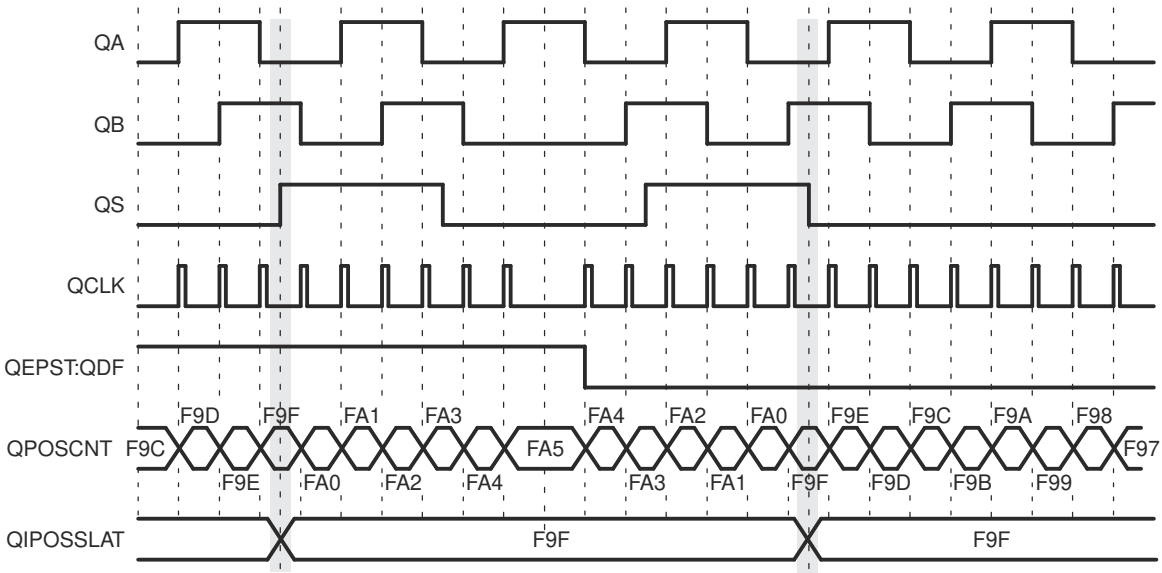


Figure 24-12. Strobe Event Latch (QEPCTL[SEL] = 1)

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There is an added feature on Type 2.0 eQEP where position-counter value can also be latched on ADCSOCA and ADCSOSCB events by configuring the register QEPSTROBESEL.STROBESEL as shown in Figure 24-13. To use the ADCSOCA/B events for the QS signal, configuration of the QEPSRCSEL.QEPSSEL to be non-zero is needed..

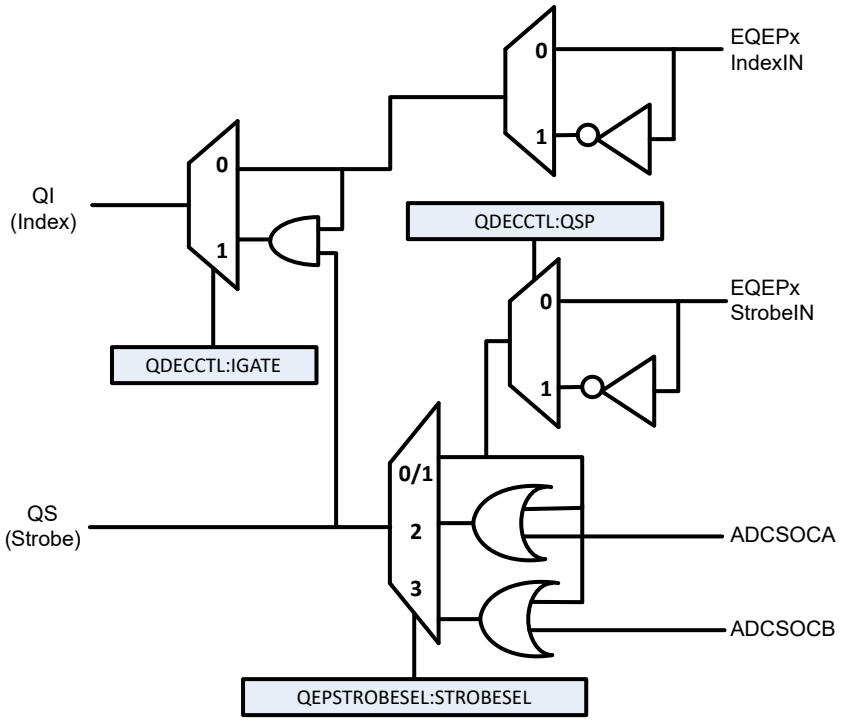


Figure 24-13. Latching Position Counter on ADCSOCA/ADCSOCB Event

24.5.3 Position Counter Initialization

The position counter can be initialized using the following events:

- Index event
- Strobe event
- Software initialization

Index Event Initialization (IEI)	The QEPI index input can be used to trigger the initialization of the position counter at the rising or falling edge of the index input. If the QEPCTL[IEI] bits are 10, then the position counter (QPOSCNT) is initialized with a value in the QPOSINIT register on the rising edge of index input. Conversely, if the QEPCTL[IEI] bits are 11, initialization is on the falling edge of the index input.
Strobe Event Initialization (SEI)	If the QEPCTL[SEI] bits are 10, then the position counter is initialized with a value in the QPOSINIT register on the rising edge of strobe input. If QEPCTL[SEL] bits are 11, then the position counter is initialized with a value in the QPOSINIT register on the rising edge of strobe input for forward direction and on the falling edge of strobe input for reverse direction.
Software Initialization (SWI)	The position counter can be initialized in software by writing a 1 to the QEPCTL[SWI] bit. This bit is not automatically cleared. While the bit is still set, if a 1 is written to the bit again, the position counter is re-initialized.

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24.5.4 eQEP Position-compare Unit

The eQEP peripheral includes a position-compare unit that is used to generate a sync output and interrupt on a position-compare match. Figure 24-14 shows a diagram. The position-compare (QPOSCMP) register is shadowed and shadow mode can be enabled or disabled using the QPOSCTL[PSSHDW] bit. If the shadow mode is not enabled, the CPU writes directly to the active position compare register.

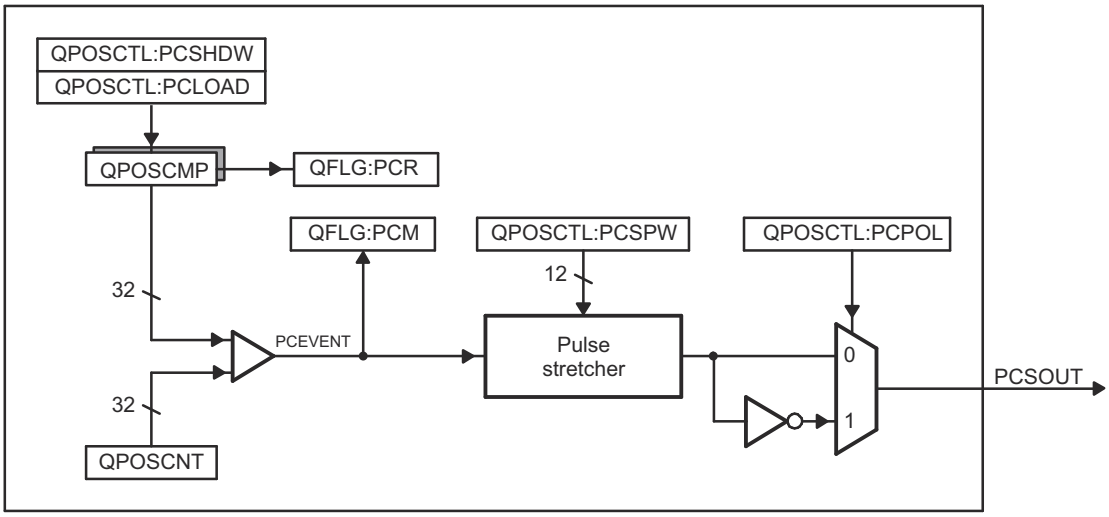


Figure 24-14. eQEP Position-compare Unit

In shadow mode, you can configure the position-compare unit (QPOSCTL[PCLOAD]) to load the shadow register value into the active register on the following events, and to generate the position-compare ready (QFLG[PCR]) interrupt after loading.

- Load on compare match
- Load on position-counter zero event

The position-compare match (QFLG[PCM]) is set when the position-counter value (QPOSCNT) matches with the active position-compare register (QPOSCMP) and the position-compare sync output of the programmable pulse width is generated on compare-match to trigger an external device.

For example, if QPOSCMP = 2, the position-compare unit generates a position-compare event on 1 to 2 transitions of the eQEP position counter for forward counting direction and on 3 to 2 transitions of the eQEP position counter for reverse counting direction (see Figure 24-15).

See the register section for the layout of the eQEP Position-Compare Control Register (QPOSCTL) and description of the QPOSCTL bit fields.

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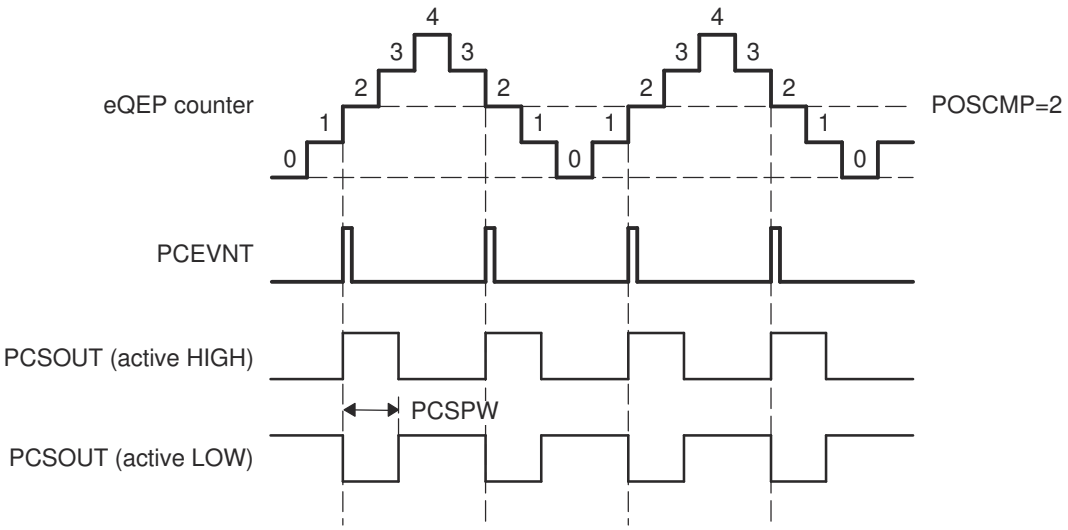


Figure 24-15. eQEP Position-compare Event Generation Points

The pulse stretcher logic in the position-compare unit generates a programmable position-compare sync pulse output on the position-compare match. In the event of a new position-compare match while a previous position-compare pulse is still active, then the pulse stretcher generates a pulse of specified duration from the new position-compare event as shown in Figure 24-16.

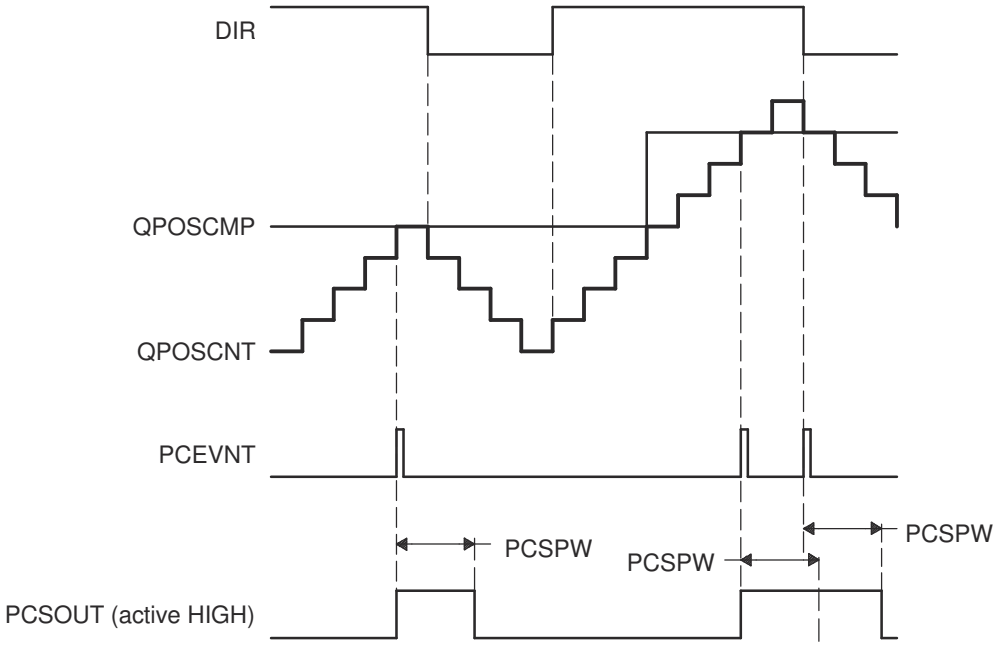


Figure 24-16. eQEP Position-compare Sync Output Pulse Stretcher

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24.6 eQEP Edge Capture Unit

The eQEP peripheral includes an integrated edge capture unit to measure the elapsed time between the unit position events as shown in Figure 24-17. This feature is typically used for low-speed measurement using the following formula:

$$v(k) = \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T} \quad (38)$$

where:

- X = Unit position is defined by integer multiple of quadrature edges (see Figure 24-18)
- ΔT = Elapsed time between unit position events
- v(k) = Velocity at time instant "k"

The eQEP capture timer (QCTMR) runs from prescaled MCLK and the prescaler is programmed by the QCAPCTL[CCPS] bits. The capture timer (QCTMR) value is latched into the capture period register (QCPRD) on every unit position event and then the capture timer is reset, a flag is set in QEPSTS:UPEVNT to indicate that new value is latched into the QCPRD register. Software can check this status flag before reading the period register for low speed measurement, and clear the flag by writing 1.

Time measurement (ΔT) between unit position events is correct if the following conditions are met:

- No more than 65,535 counts have occurred between unit position events.
- No direction change between unit position events.

If the QEP capture timer overflows between unit position events, then the timer sets the QEP capture overflow flag (QEPSTS[COEF]) in the status register.

Note

The QCPRDLAT register is not set to 0xFFFF if the QEPSTS[COEF] bit gets set.

If direction change occurs between the unit position events, then the direction error flag (QEPSTS[CDEF]) is set in the status register and the QCPRDLAT register is set to 0xFFFF.

The Capture Timer (QCTMR) and Capture Period register (QCPRD) can be configured to latch on the following events:

- CPU read of QPOSCNT register
- Unit time-out event

If the QEPCTL[QCLM] bit is cleared, then the capture timer and capture period values are latched into the QCTMRLAT and QCPRDLAT registers, respectively, when the CPU reads the position counter (QPOSCNT).

If the QEPCTL[QCLM] bit is set, then the position counter, capture timer, and capture period values are latched into the QPOSLAT, QCTMRLAT and QCPRDLAT registers, respectively, on unit time out.

Figure 24-19 shows the capture unit operation along with the position counter.

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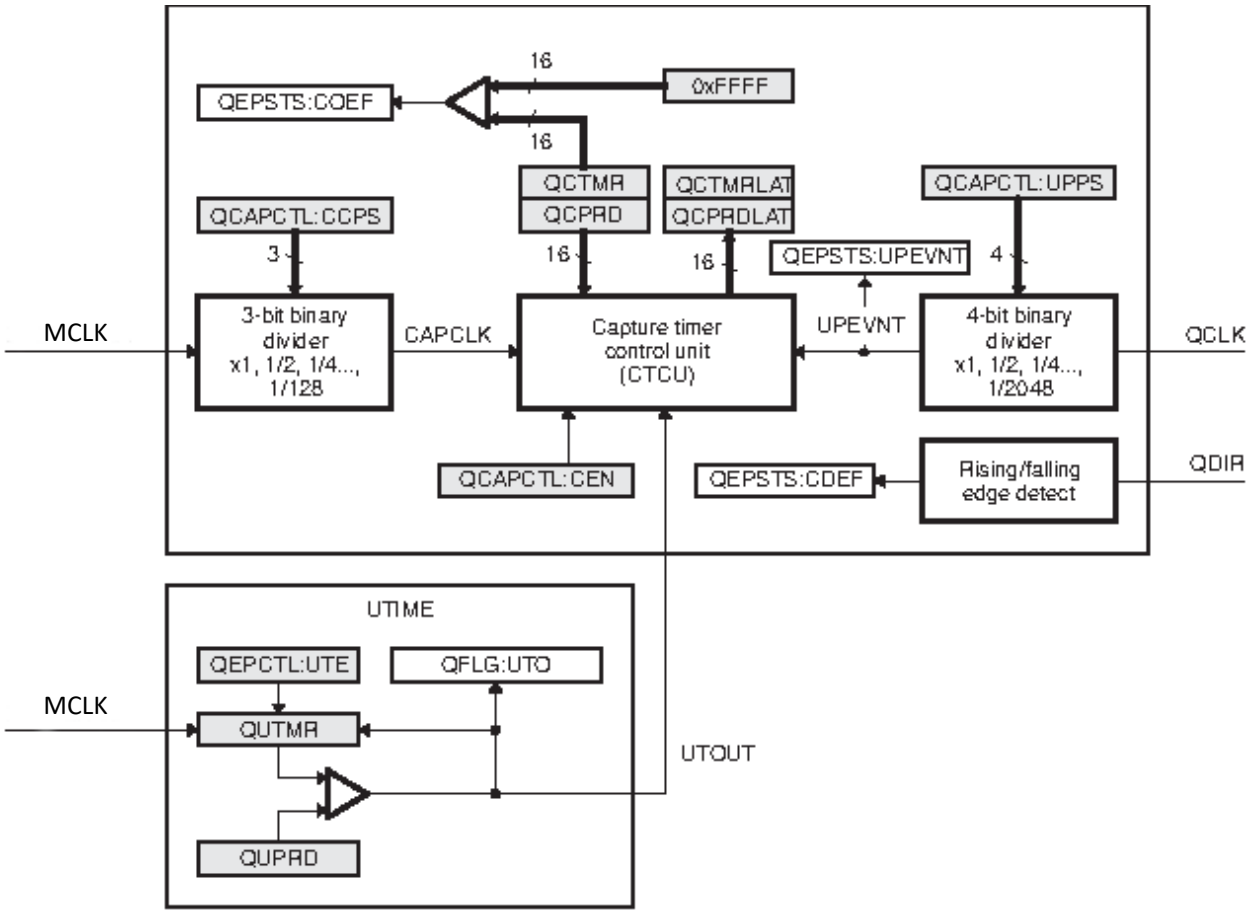
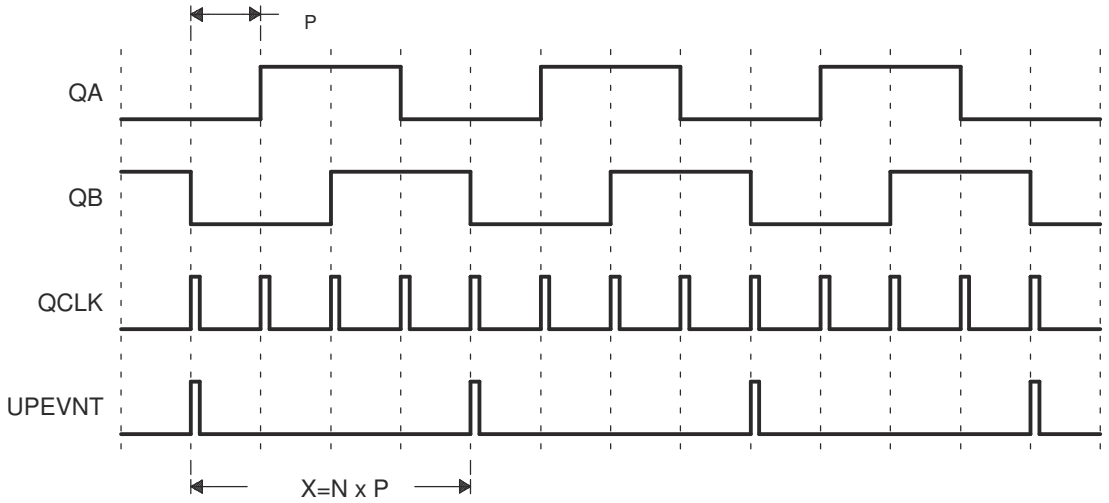


Figure 24-17. eQEP Edge Capture Unit

CAUTION

The QCAPCTL[UPPS] prescaler cannot be modified dynamically (such as switching the unit event prescaler from QCLK/4 to QCLK/8). Doing so can result in undefined behavior. The QCAPCTL[CPPS] prescaler can be modified dynamically (such as switching CAPCLK prescaling mode from MCLK/4 to MCLK/8) only after the capture unit is disabled.

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Note

N = Number of quadrature periods selected using QCAPCTL[UPPS] bits

Figure 24-18. Unit Position Event for Low Speed Measurement (QCAPCTL[UPPS] = 0010)

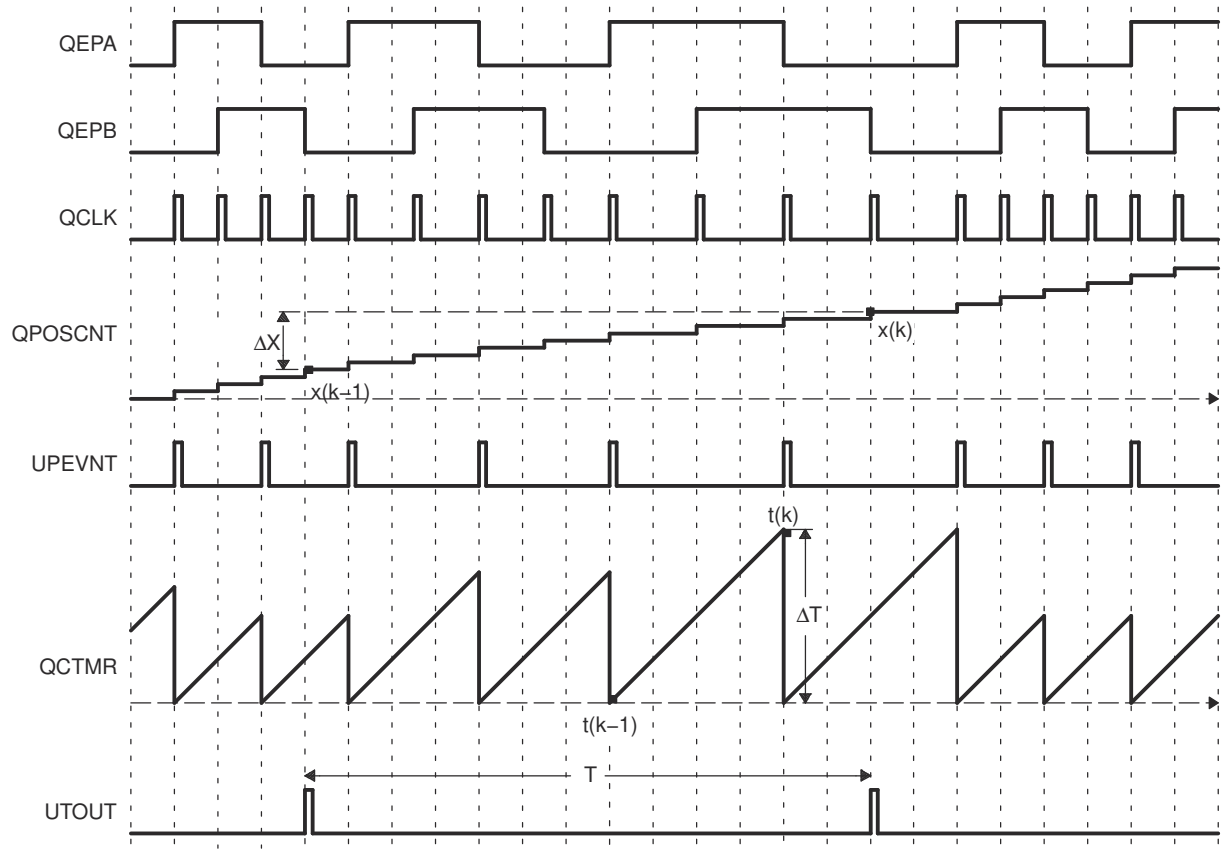


Figure 24-19. eQEP Edge Capture Unit - Timing Details

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Velocity calculation equation:

$$v(k) = \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} \quad (39)$$

where:

- v(k) = Velocity at time instant k
- x(k) = Position at time instant k
- x(k-1) = Position at time instant k-1
- T = Fixed unit time or inverse of velocity calculation rate
- ΔX = Incremental position movement in unit time
- X = Fixed unit position
- ΔT = Incremental time elapsed for unit position movement
- t(k) = Time instant "k"
- t(k-1) = Time instant "k-1"

Unit time (T) and unit period (X) are configured using the QUPRD and QCAPCTL[UPPS] registers. Incremental position output and incremental time output is available in the QPOSLAT and QCPRDLAT registers.

Parameter	Relevant Register to Configure or Read the Information
T	Unit Period Register (QUPRD)
ΔX	Incremental Position = QPOSLAT(k) - QPOSLAT(K-1)
X	Fixed-unit position defined by sensor resolution and QCAPCTL[UPPS] bits
ΔT	Capture Period Latch (QCPRDLAT)

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24.7 eQEP Watchdog

The eQEP peripheral contains a 16-bit watchdog timer (Figure 24-20) that monitors the quadrature clock to indicate proper operation of the motion-control system. The eQEP watchdog timer is clocked from MCLK/64 and the quadrature clock event (pulse) resets the watchdog timer. If no quadrature clock event is detected until a period match (QWDPRD = QWDTMR), then the watchdog timer times out and the watchdog interrupt flag is set (QFLG[WTO]). The time-out value is programmable through the watchdog period register (QWDPRD).

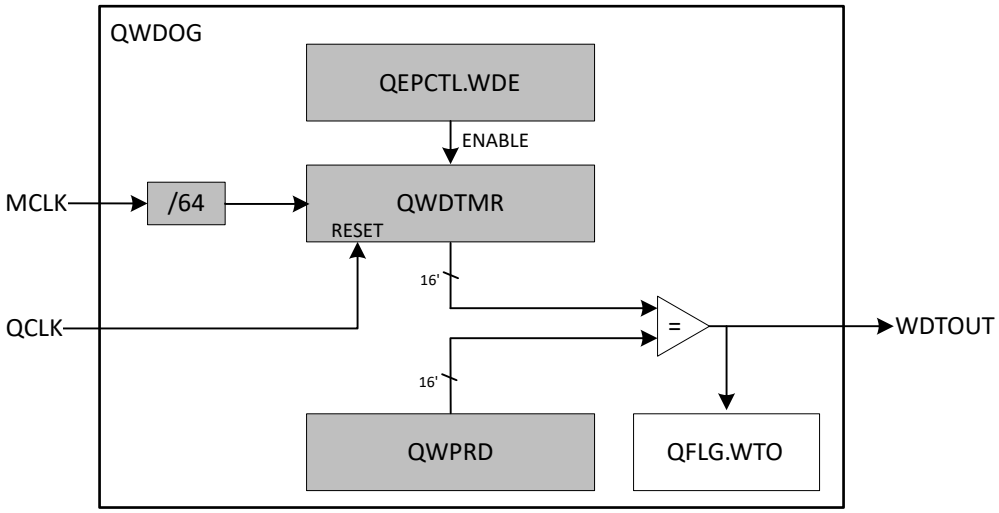


Figure 24-20. eQEP Watchdog Timer

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24.8 eQEP Unit Timer Base

The eQEP peripheral includes a 32-bit timer (QUTMR) that is clocked by MCLK to generate periodic interrupts for velocity calculations, see Figure 24-21. Whenever the unit timer (QUTMR) matches the unit period register (QUPRD), the eQEP peripheral resets the unit timer (QUTMR) and also generates the unit time out interrupt flag (QFLG[UTO]). The unit timer gets reset whenever timer value equals to configured period value.

The eQEP peripheral can be configured to latch the position counter, capture timer, and capture period values on a unit time out event so that latched values are used for velocity calculation as described in Section 24.6 .

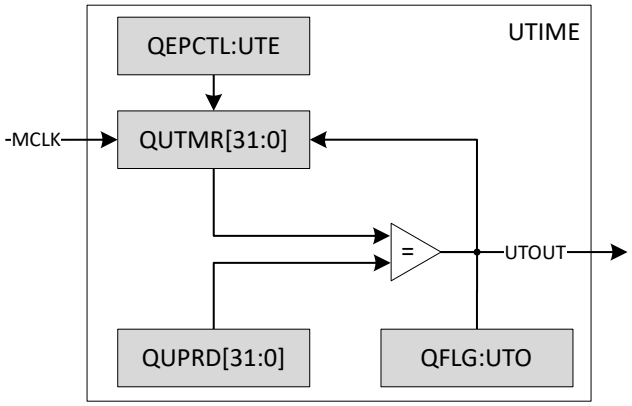


Figure 24-21. eQEP Unit Timer Base

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24.9 QMA Module

The QEP Mode Adapter (QMA) is designed to extend the eQEP module capabilities to support the additional modes described. Figure 24-22 depicts how the QMA module is integrated into to the eQEP module.

At reset, by default QMA logic is bypassed and the EQEPA and EQEPB inputs from the pins go directly into the eQEP module. When QMA module is enabled by configuring the QMACTRL[MODE] register, the EQEPA and EQEPB input are processed by this module and modified version of EQEPA and EQEPB signals are sent to the eQEP module. The QMA module requires the eQEP module to be configured in the Direction-Count mode and generates a clock signal on EQEPA input and direction signal on EQEPB input as needed for the proper operation of the intended mode.

- The xCLKMOD block inside the QMA module looks at the transitions on external EQEPA and EQEPB signals to generate the clock signal on the EQEPA input to the eQEP module.
- The xDIRMOD block inside the QMA module looks at the transitions on external EQEPA and EQEPB signals to generate the direction signal on the EQEPB input to the eQEP module.

The QMA module has error detection logic to detect illegal transitions on EQEPA and EQEPB input signals. The QMA module's error and interrupt are integrated inside the eQEP module as described in Section 24.10.1.1 .

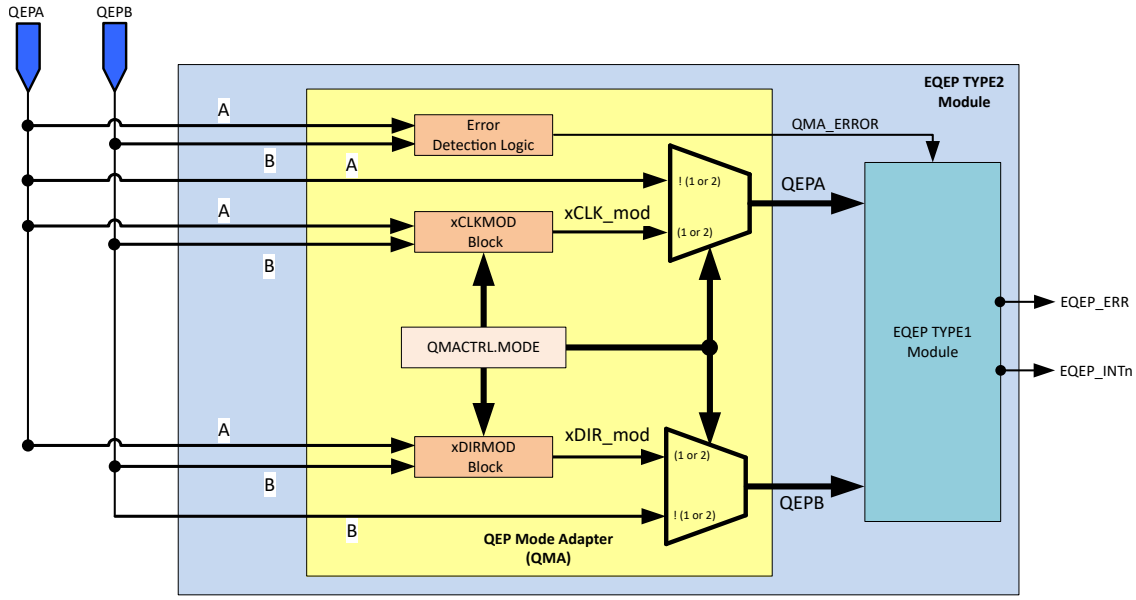


Figure 24-22. QMA Module Block Diagram

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24.9.1 Modes of Operation

The QMA module can be operated in the following modes by configuring the QMACTRL register:

- QMA Mode-1 (QMACTRL[MODE] = 1)
- QMA Mode-2 (QMACTRL[MODE] = 2)

24.9.1.1 QMA Mode-1 (QMACTRL[MODE] = 1)

This mode is used when the default state of EQEPA and EQEPB inputs is high. In this mode, outputs of QMA correspond to the following as shown in Figure 24-23:

- EQEPA Output of QMA is the AND of EQEPA and EQEPB inputs coming from the pin
- EQEPB Output of QMA is the direction signal generated by QMA based on EQEPA and EQEPB inputs

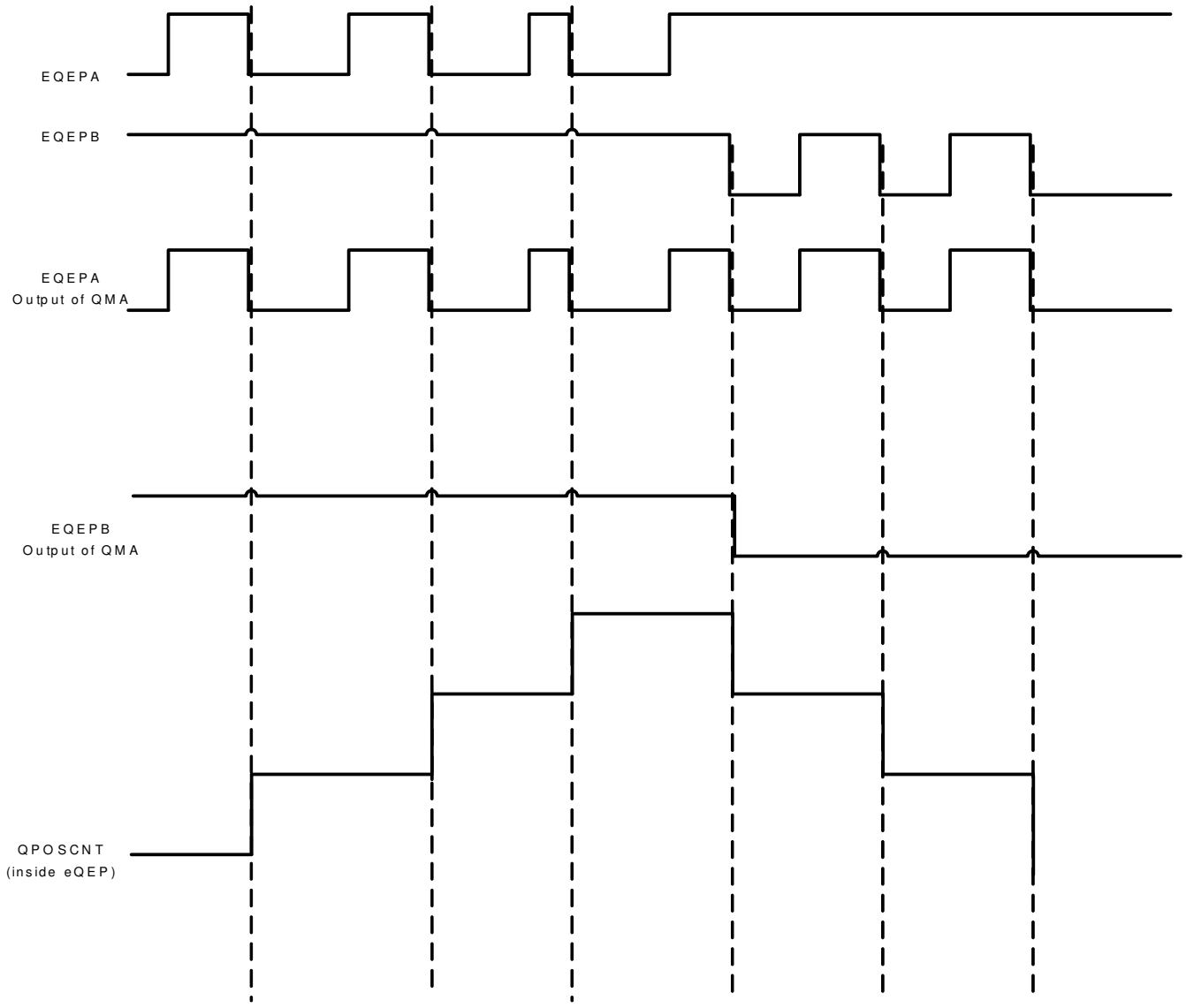


Figure 24-23. QMA Mode-1

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24.9.1.2 QMA Mode-2 (QMACTRL[MODE] = 2)

This mode is used when the default state of EQEPA and EQEPB inputs is low. In this mode, outputs of QMA correspond to the following as shown in Figure 24-24:

- EQEPA Output of QMA is the OR of EQEPA and EQEPB inputs coming from the pin
- EQEPB Output of QMA is the direction signal generated by QMA based on EQEPA and EQEPB inputs

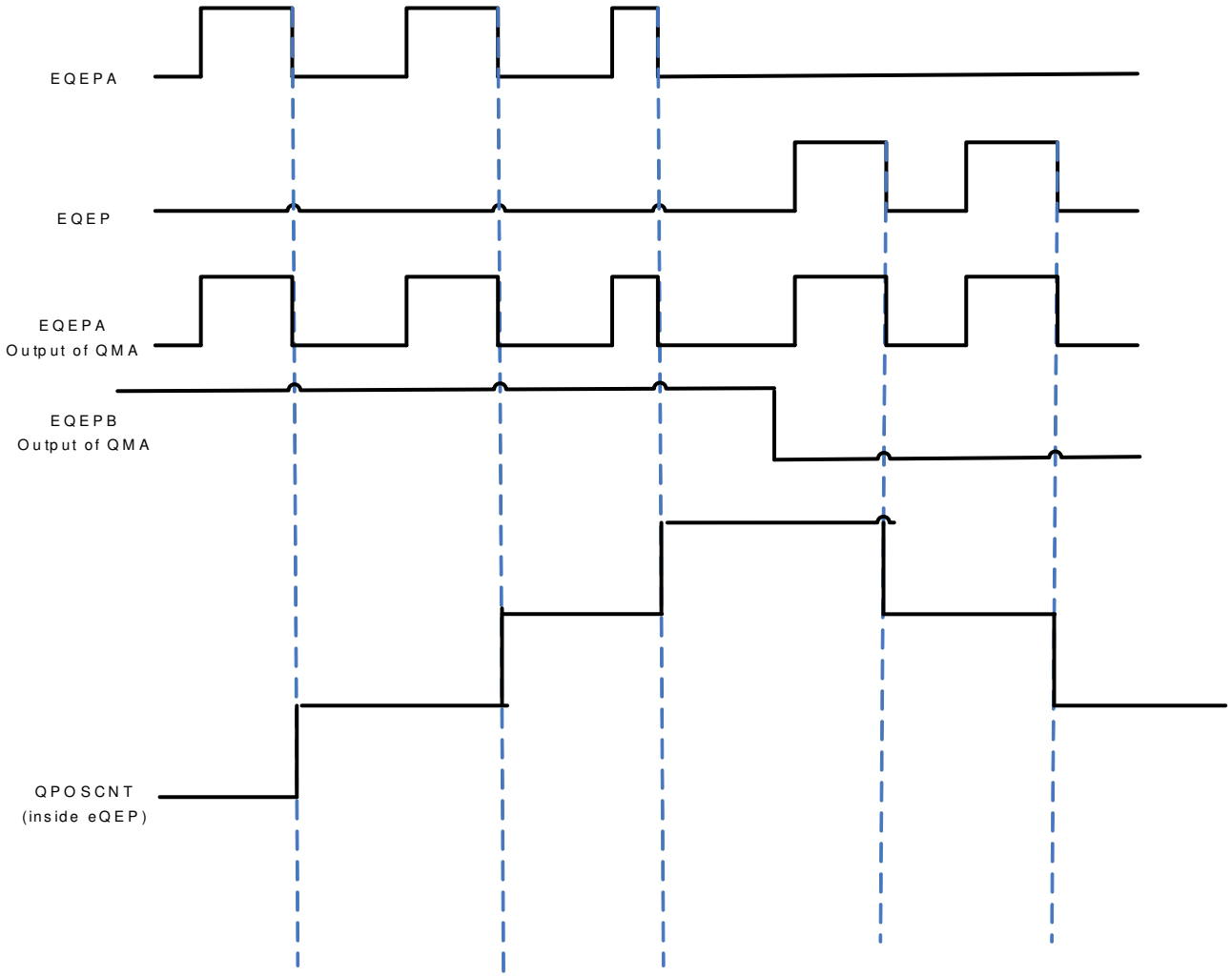


Figure 24-24. QMA Mode-2

24.9.2 Interrupt and Error Generation

The error detection logic detects illegal transitions on EQEPA and EQEPB signals and generates an error signal. This error signal can be used to generate eQEP interrupt and error output. Refer to Section 24.10.1.1 for details.

24.10 EQEP Interrupts &Triggers

24.10.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

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Table 24-3. CPU Interrupts Triggered by EQEP

NVIC Interrupt Name	Peripheral Instance Name	Register Group	EQEP Interrupt Configuration Registers	Description
EQEP0	EQEP0	N/A	QEINT, QFLG, QFRC, QCLR	EQEP0 interrupt. Multiple OR'd, configurable source condition.
EQEP1	EQEP1	N/A	QEINT, QFLG, QFRC, QCLR	EQEP1 interrupt. Multiple OR'd, configurable source condition.
EQEP2	EQEP2	N/A	QEINT, QFLG, QFRC, QCLR	EQEP2 interrupt. Multiple OR'd, configurable source condition.

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24.10.1.1 eQEP Interrupt Structure

Figure 24-25 shows how the interrupt mechanism works in the eQEP module.

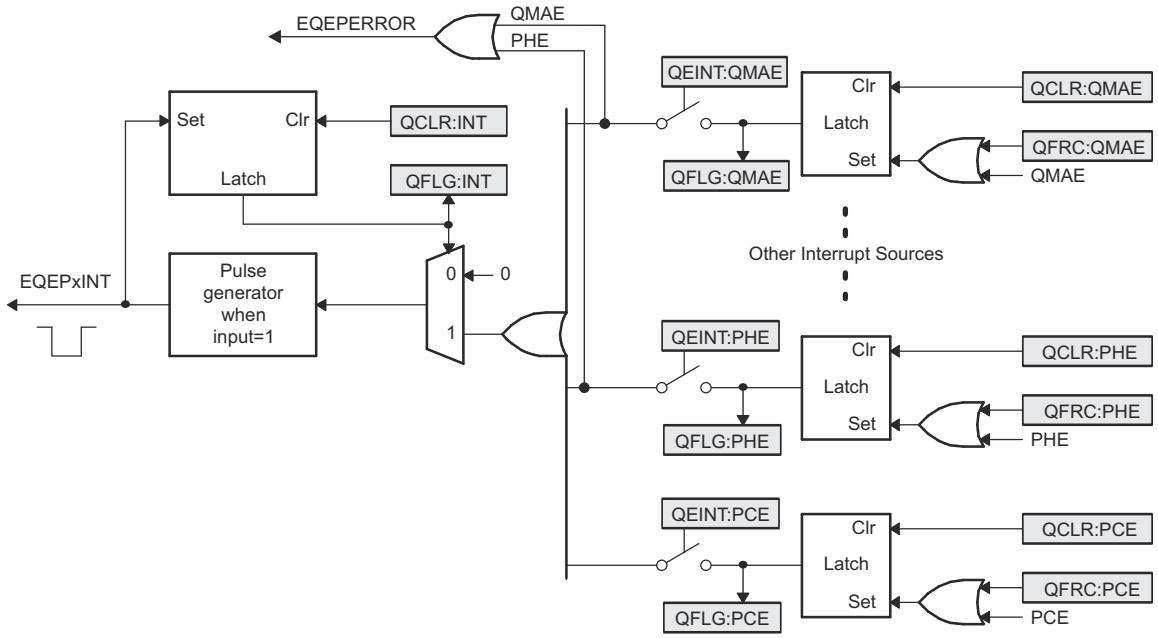


Figure 24-25. eQEP Interrupt Generation

Eleven interrupt events (PCE, PHE, QDC, WTO, PCU, PCO, PCR, PCM, SEL, IEL, and UTO) can be generated. The interrupt control register (QEINT) is used to enable/disable individual interrupt event sources. The interrupt flag register (QFLG) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT).

A pulse interrupt is generated to the NVIC when the following conditions are met:

1. Interrupt is enabled for eQEP event inside QEINT register
2. Interrupt flag for eQEP event inside QFLG register is set, and
3. Global interrupt status flag bit QFLG[INT] had been cleared for previously generated interrupt event. The interrupt service routine needs to clear the global interrupt flag bit and the serviced event, by way of the interrupt clear register (QCLR), before any other interrupt pulses are generated. If either flags inside the QFLG register are not cleared, further interrupt events do not generate an additional interrupt."
4. You can force an interrupt event by way of the interrupt force register (QFRC), which is useful for test/debug purposes.

24.11 Software

24.11.1 EQEP Examples

NOTE: These examples are located in the device SDK installation at the following location: {SDK_VERSION#}/driverlib/{DEVICE_GPN}/examples/{CORE_IF_MULTICORE}/eqep

24.11.1.1 Frequency Measurement Using eQEP

FILE: eqep_ex1_freq_cal.c

This example calculates the frequency of an input signal using the eQEP module. MCPWM1A is configured to generate this input signal with a frequency of 5kHz. There is an interrupt once every period with a call to the frequency calculation function. This example uses the IQMath library to simplify high-precision calculations.

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In addition to the main example file, the following files must be included in this project:
- *eqep_ex1_calculation.c* - contains frequency calculation function
- *eqep_ex1_calculation.h* - includes initialization values for frequency structure

The configuration for this example is as follows:
- Maximum frequency is configured to 10KHz (baseFreq)
- Minimum frequency is assumed at 50Hz for capture pre-scalar selection

SPEED_FR: High Frequency Measurement is obtained by counting the external input pulses for 10ms (unit timer set to 100Hz). \[SPEED_FR = \frac{Count\ Delta}{10ms} \]

SPEED_PR: Low Frequency Measurement is obtained by measuring time period of input edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled MCLK.

Note that the pre-scaler for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user stops the timer.

For more information about the frequency calculation see the comments at the beginning of eqep_ex1_calculation.c and the XLS file provided with the project, eqep_ex1_calculation.xls.

External Connections
- Connect GPIO6/eQEP1A to GPIO0/MCPWM1A

Watch Variables
- *freq.freqHzFR* - Frequency measurement using position counter/unit time out
- *freq.freqHzPR* - Frequency measurement using capture unit

24.11.1.2 Position and Speed Measurement Using eQEP

FILE: eqep_ex2_pos_speed.c

This example provides position and speed measurement using the capture unit and speed measurement using unit time out of the eQEP module. MCPWM1 and a GPIO are configured to generate simulated eQEP signals. The MCPWM module interrupts once every period and calls the position/speed calculation function. This example uses the IQMath library to simplify high-precision calculations.

In addition to the main example file, the following files must be included in this project:
- *eqep_ex2_calculation.c* - contains position/speed calculation function
- *eqep_ex2_calculation.h* - includes initialization values for position/speed structure

The configuration for this example is as follows:
- Maximum speed is configured to 6000rpm (baseRPM)
- Minimum speed is assumed at 10rpm for capture pre-scalar selection
- Pole pair is configured to 2 (polePairs)
- Encoder resolution is configured to 4000 counts/revolution (mechScaler)
- Which means: 4000 / 4 = 1000 line/revolution quadrature encoder (simulated by MCPWM1)
- MCPWM1 (simulating QEP encoder signals) is configured for a 5kHz frequency or 300 rpm (= 4 * 5000 cnts/sec * 60 sec/min) / 4000 cnts/rev)

SPEEDRPM_FR: High Speed Measurement is obtained by counting the QEP input pulses for 10ms (unit timer set to 100Hz).

SPEEDRPM_FR = (Position Delta / 10ms) * 60 rpm

SPEEDRPM_PR: Low Speed Measurement is obtained by measuring time period of QEP edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled MCLK .

Note that the pre-scaler for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user ends the program.

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For more information about the position/speed calculation see the comments at the beginning of eqep_ex2_calculation.c and the XLS file provided with the project, eqep_ex2_calculation.xls.

External Connections

- Connect GPIO6/eQEP1A to GPIO0/MCPWM1A (simulates eQEP Phase A signal)
- Connect GPIO7/eQEP1B to GPIO1/MCPWM1B (simulates eQEP Phase B signal)
- Connect GPIO43/eQEP1I to GPIO2 (simulates eQEP Index Signal)

Watch Variables

- *posSpeed.speedRPMFR* - Speed meas. in rpm using QEP position counter
- *posSpeed.speedRPMPR* - Speed meas. in rpm using capture unit
- *posSpeed.thetaMech* - Motor mechanical angle (Q15)
- *posSpeed.thetaElec* - Motor electrical angle (Q15)

24.11.1.3 PWM Frequency Measurement using EQEP via XBAR connection

FILE: eqep_ex3_epwm_xbar.c

This example calculates the frequency of a PWM signal using the eQEP module. PWM1A is configured to generate this input signal with a frequency of 5kHz. This PWM signal is connected to input of eQEP using Input XBAR and PWM XBAR. The MCPWMEPWM module interrupts once every period and calls the frequency calculation function. This example uses the IQMath library to simplify high-precision calculations.

In addition to the main example file, the following files must be included in this project:

- *eqep_ex1_calculation.c* - contains frequency calculation function
- *eqep_ex1_calculation.h* - includes initialization values for frequency structure

The configuration for this example is as follows

- Maximum frequency is configured to 10KHz (baseFreq)
- Minimum frequency is assumed at 50Hz for capture pre-scalar selection
- GPIO0 is connected to output of INPUT_XBAR1
- INPUT_XBAR1 is connected to output of PWMXBAR at TRIP4
- eQEPA source is configured as PWMXBAR.1 output (TRIP4)

SPEED_FR: High Frequency Measurement is obtained by counting the external input pulses for 10ms (unit timer set to 100Hz). \[SPEED_FR = \frac{Count\ Delta}{10ms} \]

SPEED_PR: Low Frequency Measurement is obtained by measuring time period of input edges. Time measurement is averaged over 64 edges for better results and the capture unit performs the time measurement using pre-scaled MCLK .

Note that the pre-scaler for capture unit clock is selected such that the capture timer does not overflow at the required minimum frequency. This example runs indefinitely until the user stops the program.

For more information about the frequency calculation see the comments at the beginning of eqep_ex1_calculation.c and the XLS file provided with the project, eqep_ex1_calculation.xls.

Watch Variables

- *freq.freqHzFR* - Frequency measurement using position counter/unit time out
- *freq.freqHzPR* - Frequency measurement using capture unit

24.11.1.4 Frequency Measurement Using eQEP via unit timeout interrupt

FILE: eqep_ex4_freq_cal_interrupt.c

This example will calculate the frequency of an input signal using the eQEP module. MCPWM1A is configured to generate this input signal with a frequency of 5kHz. EQEP unit timeout is set which generates an interrupt every *UNIT_PERIOD* microseconds and frequency calculation occurs continuously.

The configuration for this example is as follows:

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- PWM frequency is specified as 5000Hz
- UNIT_PERIOD is specified as 10000µs
- Min frequency is (1 / (2*10ms)), that is, 50Hz
- Highest frequency can be (2^32) / ((2*10ms))
- Resolution of frequency measurement is 50Hz

freq : Frequency Measurement is obtained by counting the external input pulses for UNIT_PERIOD (unit timer set to 10ms).

External Connections for Control Card
- Connect GPIO6/eQEP1A to GPIO0/MCPWM1A

Watch Variables
- *freq* - Frequency measurement using position counter/unit time out
- *pass* - If measured frequency matches with PWM frequency then pass = 1 else 0

24.11.1.5 Motor speed and direction measurement using eQEP via unit timeout interrupt

FILE: eqep_ex5_speed_dir_motor.c

This example can be used to sense the speed and direction of motor using eQEP in quadrature encoder mode. MCPWM1A is configured to simulate motor encoder signals with frequency of 5kHz on both A and B pins with 90 degree phase shift (so as to run this example without motor). EQEP unit timeout is set which will generate an interrupt every *UNIT_PERIOD* microseconds and speed calculation occurs continuously based on the direction of motor

The configuration for this example is as follows
- PWM frequency is specified as 5000Hz
- UNIT_PERIOD is specified as 10000µs
- Simulated quadrature signal frequency is 20000Hz (4 * 5000)
- Encoder holes assumed as 1000
- Thus Simulated motor speed is 300rpm (5000 * (60 / 1000))

freq : Simulated quadrature signal frequency measured by counting the external input pulses for UNIT_PERIOD (unit timer set to 10ms). *speed* : Measure motor speed in rpm *dir* : Indicates clockwise (1) or anticlockwise (-1)

External Connections (if motor encoder signals are simulated by MCPWM)
With motor
- Comment in "MOTOR" in includes
- Connect GPIO6/eQEP1A to GPIO0/MCPWM1A (simulates eQEP Phase A signal)
- Connect GPIO7/eQEP1B to GPIO1/MCPWM1B (simulates eQEP Phase B signal)

Watch Variables
- *freq* : Simulated motor frequency measurement is obtained by counting the external input pulses for UNIT_PERIOD (unit timer set to 10ms).
- *speed* : Measure motor speed in rpm
- *dir* : Indicates clockwise (1) or anticlockwise (-1)
- *pass* - If measured quadrature frequency matches with input quadrature frequency (4 * PWM frequency) then pass = 1 else fail = 1 (** only when "MOTOR" is commented out)

24.12 EQEP Registers

This Section describes the EQEP Registers.

24.12.1 EQEP Base Address Table

Table 24-4. EQEP Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
EQep0Regs	EQEP_REGS	EQEP0	0x4044_8000

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Table 24-4. EQEP Base Address Table (continued)

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
EQep1Regs	EQEP_REGS	EQEP1	0x4044_9000

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24.12.2 EQEP_REGS Registers

Table 24-5 lists the memory-mapped registers for the EQEP_REGS registers. All register offset addresses not listed in Table 24-5 should be considered as reserved locations and the register contents should not be modified.

Table 24-5. EQEP_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	QPOSCNT	Position Counter		Go
4h	QPOSINIT	Position Counter Init		Go
8h	QPOSMAX	Maximum Position Count		Go
Ch	QPOSCMP	Position Compare		Go
10h	QPOSILAT	Index Position Latch		Go
14h	QPOSSLAT	Strobe Position Latch		Go
18h	QPOSLAT	Position Latch		Go
1Ch	QUTMR	QEP Unit Timer		Go
20h	QUPRD	QEP Unit Period		Go
24h	QWDTMR	QEP Watchdog Timer		Go
26h	QWDPRD	QEP Watchdog Period		Go
28h	QDECCTL	Quadrature Decoder Control		Go
2Ah	QEPCTL	QEP Control		Go
2Ch	QCAPCTL	Qaudrature Capture Control		Go
2Eh	QPOSCTL	Position Compare Control		Go
30h	QEINT	QEP Interrupt Control		Go
32h	QFLG	QEP Interrupt Flag		Go
34h	QCLR	QEP Interrupt Clear		Go
36h	QFRC	QEP Interrupt Force		Go
38h	QEPSTS	QEP Status		Go
3Ah	QCTMR	QEP Capture Timer		Go
3Ch	QCPRD	QEP Capture Period		Go
3Eh	QCTMRLAT	QEP Capture Latch		Go
40h	QCPRDLAT	QEP Capture Period Latch		Go
60h	REV	QEP Revision Number		Go
64h	QEPSTROBESEL	QEP Strobe select register		Go
68h	QMACTRL	QMA Control register		Go
6Ch	QEPSRCSEL	QEP Source Select Register		Go

Complex bit access types are encoded to fit into small table cells. Table 24-6 shows the codes that are used for access types in this section.

Table 24-6. EQEP_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear

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Table 24-6. EQEP_REGS Access Type Codes (continued)

Access Type	Code	Description
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 QPOSCNT Register (Offset = 0h) [Reset = 00000000h]

QPOSCNT is shown in Figure 24-26 and described in Table 24-7.

Return to the Summary Table.

Position Counter

Figure 24-26. QPOSCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCNT																															
R/W-0h																															

Table 24-8. QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSCNT	R/W	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Note: It is recommended to only write to the position counter register (QPOSCNT) during initialization, i.e. when the eQEP position counter is disabled (QPEN bit of QEPCTL is zero). Once the position counter is enabled (QPEN bit is one), writing to the eQEP position counter register (QPOSCNT) may cause unexpected results. Reset type: SYSRSn

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2 QPOSINIT Register (Offset = 4h) [Reset = 00000000h]

QPOSINIT is shown in Figure 24-27 and described in Table 24-8.

Return to the Summary Table.

Position Counter Init

Figure 24-27. QPOSINIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSINIT																															
R/W-0h																															

Table 24-10. QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSINIT	R/W	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes. Reset type: SYSRSn

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3 QPOSMAX Register (Offset = 8h) [Reset = 00000000h]

QPOSMAX is shown in Figure 24-28 and described in Table 24-9.

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Maximum Position Count

Figure 24-28. QPOSMAX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSMAX																															
R/W-0h																															

Table 24-12. QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes. Reset type: SYSRSn

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4 QPOSCMP Register (Offset = Ch) [Reset = 00000000h]

QPOSCMP is shown in Figure 24-29 and described in Table 24-10.

Return to the Summary Table.

Position Compare

Figure 24-29. QPOSCMP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSCMP																															
R/W-0h																															

Table 24-14. QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSCMP	R/W	0h	Position Compare The position-compare value in this register is compared with the position counter (QPOSCNT) to generate sync output and/or interrupt on compare match. Writes to this register should always be full 32-bit writes. Reset type: SYSRSn

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5 QPOSILAT Register (Offset = 10h) [Reset = 00000000h]

QPOSILAT is shown in Figure 24-30 and described in Table 24-11.

Return to the Summary Table.

Index Position Latch

Figure 24-30. QPOSILAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSILAT																															
R-0h																															

Table 24-16. QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits. Reset type: SYSRSn

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6 QPOSSLAT Register (Offset = 14h) [Reset = 00000000h]

QPOSSLAT is shown in Figure 24-31 and described in Table 24-12.

Return to the Summary Table.

Strobe Position Latch

Figure 24-31. QPOSSLAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSSLAT																															
R-0h																															

Table 24-18. QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSSLAT	R	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits. Reset type: SYSRSn

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7 QPOSLAT Register (Offset = 18h) [Reset = 00000000h]

QPOSLAT is shown in Figure 24-32 and described in Table 24-13.

Return to the Summary Table.

Position Latch

Figure 24-32. QPOSLAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QPOSLAT																															
R-0h																															

Table 24-20. QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on a unit time out event. Reset type: SYSRSn

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8 QUTMR Register (Offset = 1Ch) [Reset = 00000000h]

QUTMR is shown in Figure 24-33 and described in Table 24-14.

Return to the Summary Table.

QEP Unit Timer

Figure 24-33. QUTMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUTMR																															
R/W-0h																															

Table 24-22. QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QUTMR	R/W	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated. Writes to this register should always be full 32-bit writes. Reset type: SYSRSn

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9 QUPRD Register (Offset = 20h) [Reset = 00000000h]

QUPRD is shown in Figure 24-34 and described in Table 24-15.

Return to the Summary Table.

QEP Unit Period

Figure 24-34. QUPRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUPRD																															
R/W-0h																															

Table 24-24. QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	QUPRD	R/W	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes. Reset type: SYSRSn

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10 QWDTMR Register (Offset = 24h) [Reset = 0000h]

QWDTMR is shown in Figure 24-35 and described in Table 24-16.

Return to the Summary Table.

QEP Watchdog Timer

Figure 24-35. QWDTMR Register

15	14	13	12	11	10	9	8
QWDTMR							
R/W-0h							
7	6	5	4	3	2	1	0
QWDTMR							
R/W-0h							

Table 24-26. QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QWDTMR	R/W	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion. Reset type: SYSRSn

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11 QWDPRD Register (Offset = 26h) [Reset = 0000h]

QWDPRD is shown in Figure 24-36 and described in Table 24-17.

Return to the Summary Table.

QEP Watchdog Period

Figure 24-36. QWDPRD Register

15	14	13	12	11	10	9	8
QWDPRD							
R/W-0h							
7	6	5	4	3	2	1	0
QWDPRD							
R/W-0h							

Table 24-28. QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QWDPRD	R/W	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated. Reset type: SYSRSn

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12 QDECCTL Register (Offset = 28h) [Reset = 0000h]

QDECCTL is shown in Figure 24-37 and described in Table 24-18.

Return to the Summary Table.

Quadrature Decoder Control

Figure 24-37. QDECCTL Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
QBP	QIP	QSP	RESERVED				QIDIRE
R/W-0h	R/W-0h	R/W-0h	R-0h				R/W-0h

Table 24-30. QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	QSRC	R/W	0h	Position-counter source selection Reset type: SYSRSn 0h (R/W) = Quadrature count mode (QCLK = iCLK, QDIR = iDIR) 1h (R/W) = Direction-count mode (QCLK = xCLK, QDIR = xDIR) 2h (R/W) = UP count mode for frequency measurement (QCLK = xCLK, QDIR = 1) 3h (R/W) = DOWN count mode for frequency measurement (QCLK = xCLK, QDIR = 0)
13	SOEN	R/W	0h	Sync output-enable Reset type: SYSRSn 0h (R/W) = Disable position-compare sync output 1h (R/W) = Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection Reset type: SYSRSn 0h (R/W) = Index pin is used for sync output 1h (R/W) = Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate Reset type: SYSRSn 0h (R/W) = 2x resolution: Count the rising/falling edge 1h (R/W) = 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter Reset type: SYSRSn 0h (R/W) = Quadrature-clock inputs are not swapped 1h (R/W) = Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option Reset type: SYSRSn 0h (R/W) = Disable gating of Index pulse 1h (R/W) = Gate the index pin with strobe
8	QAP	R/W	0h	QEPA input polarity Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Negates QEPA input

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Table 24-30. QDECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	QBP	R/W	0h	QEPB input polarity Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Negates QEPB input
6	QIP	R/W	0h	QEPI input polarity Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Negates QEPI input
5	QSP	R/W	0h	QEPS input polarity Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Negates QEPS input
4-1	RESERVED	R	0h	Reserved
0	QIDIRE	R/W	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled: On QEPI direction change, the incoming posedge of QA can erroneously update/reset the position counter of the eQEP. This bit only needs to be enabled if the application requires a direction change occurring at the same time as an incoming QEPI signal, or when erroneous PC resets are observed. Reset type: SYSRSn

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13 QEPCTL Register (Offset = 2Ah) [Reset = 0000h]

QEPCTL is shown in Figure 24-38 and described in Table 24-19.

Return to the Summary Table.

QEP Control

Figure 24-38. QEPCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 24-32. QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation mode Reset type: SYSRSn 0h (R/W) = QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 1h (R/W) = QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 2h (R/W) = QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 3h (R/W) = Same as FREE_SOFT_2
13-12	PCRM	R/W	0h	Postion counter reset Reset type: SYSRSn 0h (R/W) = Position counter reset on an index event 1h (R/W) = Position counter reset on the maximum position 2h (R/W) = Position counter reset on the first index event 3h (R/W) = Position counter reset on a unit time event

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Table 24-32. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	SEI	R/W	0h	Strobe event initialization of position counter Reset type: SYSRSn 0h (R/W) = Does nothing (action disabled) 1h (R/W) = Does nothing (action disabled) 2h (R/W) = Initializes the position counter on rising edge of the QEPS signal 3h (R/W) = Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9-8	IEI	R/W	0h	Index event init of position count Reset type: SYSRSn 0h (R/W) = Do nothing (action disabled) 1h (R/W) = Do nothing (action disabled) 2h (R/W) = Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 3h (R/W) = Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)
7	SWI	R/W	0h	Software init position counter Reset type: SYSRSn 0h (R/W) = Do nothing (action disabled) 1h (R/W) = Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	R/W	0h	Strobe event latch of position counter Reset type: SYSRSn 0h (R/W) = The position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1h (R/W) = Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5-4	IEL	R/W	0h	Index event latch of position counter (software index marker) Reset type: SYSRSn 0h (R/W) = Reserved 1h (R/W) = Latches position counter on rising edge of the index signal 2h (R/W) = Latches position counter on falling edge of the index signal 3h (R/W) = Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.
3	QPEN	R/W	0h	Quadrature position counter enable/software reset Reset type: SYSRSn 0h (R/W) = Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLG register do not get reset or cleared and show the actual state of that flag. 1h (R/W) = eQEP position counter is enabled

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Table 24-32. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	QCLM	R/W	0h	QEP capture latch mode Reset type: SYSRSn 0h (R/W) = Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1h (R/W) = Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	R/W	0h	QEP unit timer enable Reset type: SYSRSn 0h (R/W) = Disable eQEP unit timer 1h (R/W) = Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable Reset type: SYSRSn 0h (R/W) = Disable the eQEP watchdog timer 1h (R/W) = Enable the eQEP watchdog timer

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14 QCAPCTL Register (Offset = 2Ch) [Reset = 0000h]

QCAPCTL is shown in Figure 24-39 and described in Table 24-20.

Return to the Summary Table.

Qaudrature Capture Control

Figure 24-39. QCAPCTL Register

15	14	13	12	11	10	9	8
CEN	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED	CCPS			UPPS			
R-0h	R/W-0h			R/W-0h			

Table 24-34. QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture Reset type: SYSRSn 0h (R/W) = eQEP capture unit is disabled 1h (R/W) = eQEP capture unit is enabled
14-7	RESERVED	R	0h	Reserved
6-4	CCPS	R/W	0h	eQEP capture timer clock prescaler Reset type: SYSRSn 0h (R/W) = CAPCLK = SYSCLKOUT/1 1h (R/W) = CAPCLK = SYSCLKOUT/2 2h (R/W) = CAPCLK = SYSCLKOUT/4 3h (R/W) = CAPCLK = SYSCLKOUT/8 4h (R/W) = CAPCLK = SYSCLKOUT/16 5h (R/W) = CAPCLK = SYSCLKOUT/32 6h (R/W) = CAPCLK = SYSCLKOUT/64 7h (R/W) = CAPCLK = SYSCLKOUT/128
3-0	UPPS	R/W	0h	Unit position event prescaler Reset type: SYSRSn 0h (R/W) = UPEVNT = QCLK/1 1h (R/W) = UPEVNT = QCLK/2 2h (R/W) = UPEVNT = QCLK/4 3h (R/W) = UPEVNT = QCLK/8 4h (R/W) = UPEVNT = QCLK/16 5h (R/W) = UPEVNT = QCLK/32 6h (R/W) = UPEVNT = QCLK/64 7h (R/W) = UPEVNT = QCLK/128 8h (R/W) = UPEVNT = QCLK/256 9h (R/W) = UPEVNT = QCLK/512 Ah (R/W) = UPEVNT = QCLK/1024 Bh (R/W) = UPEVNT = QCLK/2048 Ch (R/W) = Reserved Dh (R/W) = Reserved Eh (R/W) = Reserved Fh (R/W) = Reserved

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15 QPOSCTL Register (Offset = 2Eh) [Reset = 0000h]

QPOSCTL is shown in Figure 24-40 and described in Table 24-21.

Return to the Summary Table.

Position Compare Control

Figure 24-40. QPOSCTL Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PCSPW							
R/W-0h							

Table 24-36. QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	R/W	0h	Position compare of shadow enable Reset type: SYSRSn 0h (R/W) = Shadow disabled, load Immediate 1h (R/W) = Shadow enabled
14	PCLOAD	R/W	0h	Position compare of shadow load Reset type: SYSRSn 0h (R/W) = Load on QPOSCNT = 0 1h (R/W) = Load when QPOSCNT = QPOSCMP
13	PCPOL	R/W	0h	Polarity of sync output Reset type: SYSRSn 0h (R/W) = Active HIGH pulse output 1h (R/W) = Active LOW pulse output
12	PCE	R/W	0h	Position compare enable/disable Reset type: SYSRSn 0h (R/W) = Disable position compare unit 1h (R/W) = Enable position compare unit
11-0	PCSPW	R/W	0h	Select-position-compare sync output pulse width Reset type: SYSRSn 0h (R/W) = 1 * 4 * SYSCLKOUT cycles 1h (R/W) = 2 * 4 * SYSCLKOUT cycles FFFh (R/W) = 4096 * 4 * SYSCLKOUT cycles

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16 QEINT Register (Offset = 30h) [Reset = 0000h]

QEINT is shown in Figure 24-41 and described in Table 24-22.

Return to the Summary Table.

QEP Interrupt Control

Figure 24-41. QEINT Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 24-38. QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	QMAE	R/W	0h	QMA Error Interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
11	UTO	R/W	0h	Unit time out interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
6	PCO	R/W	0h	Position counter overflow interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled

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Table 24-38. QEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PCU	R/W	0h	Position counter underflow interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
4	WTO	R/W	0h	Watchdog time out interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
3	QDC	R/W	0h	Quadrature direction change interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
2	QPE	R/W	0h	Quadrature phase error interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
1	PCE	R/W	0h	Position counter error interrupt enable Reset type: SYSRSn 0h (R/W) = Interrupt is disabled 1h (R/W) = Interrupt is enabled
0	RESERVED	R	0h	Reserved

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17 QFLG Register (Offset = 32h) [Reset = 0000h]

QFLG is shown in Figure 24-42 and described in Table 24-23.

Return to the Summary Table.

QEP Interrupt Flag

Figure 24-42. QFLG Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 24-40. QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	QMAE	R	0h	QMA Error interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
11	UTO	R	0h	Unit time out interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Set by eQEP unit timer period match
10	IEL	R	0h	Index event latch interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	R	0h	Strobe event latch interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	R	0h	eQEP compare match event interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set on position-compare match
7	PCR	R	0h	Position-compare ready interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set after transferring the shadow register value to the active position compare register
6	PCO	R	0h	Position counter overflow interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set on position counter overflow.

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Table 24-40. QFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PCU	R	0h	Position counter underflow interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = This bit is set on position counter underflow.
4	WTO	R	0h	Watchdog timeout interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Set by watchdog timeout
3	QDC	R	0h	Quadrature direction change interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated
2	PHE	R	0h	Quadrature phase error interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Set on simultaneous transition of QEPA and QEPB
1	PCE	R	0h	Position counter error interrupt flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Position counter error
0	INT	R	0h	Global interrupt status flag Reset type: SYSRSn 0h (R/W) = No interrupt generated 1h (R/W) = Interrupt was generated

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18 QCLR Register (Offset = 34h) [Reset = 0000h]

QCLR is shown in Figure 24-43 and described in Table 24-24.

Return to the Summary Table.

QEP Interrupt Clear

Figure 24-43. QCLR Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
R-0h			R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 24-42. QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	QMAE	R-0/W1S	0h	Clear QMA Error interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
11	UTO	R-0/W1S	0h	Clear unit time out interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
10	IEL	R-0/W1S	0h	Clear index event latch interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
9	SEL	R-0/W1S	0h	Clear strobe event latch interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
8	PCM	R-0/W1S	0h	Clear eQEP compare match event interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
7	PCR	R-0/W1S	0h	Clear position-compare ready interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
6	PCO	R-0/W1S	0h	Clear position counter overflow interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag

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Table 24-42. QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PCU	R-0/W1S	0h	Clear position counter underflow interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
4	WTO	R-0/W1S	0h	Clear watchdog timeout interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
3	QDC	R-0/W1S	0h	Clear quadrature direction change interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
2	PHE	R-0/W1S	0h	Clear quadrature phase error interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
1	PCE	R-0/W1S	0h	Clear position counter error interrupt flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag
0	INT	R-0/W1S	0h	Global interrupt clear flag Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Clears the interrupt flag

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19 QFRC Register (Offset = 36h) [Reset = 0000h]

QFRC is shown in Figure 24-44 and described in Table 24-25.

Return to the Summary Table.

QEP Interrupt Force

Figure 24-44. QFRC Register

15	14	13	12	11	10	9	8
RESERVED			QMAE	UTO	IEL	SEL	PCM
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 24-44. QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	QMAE	R/W	0h	Force QMA error interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
11	UTO	R/W	0h	Force unit time out interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
10	IEL	R/W	0h	Force index event latch interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
9	SEL	R/W	0h	Force strobe event latch interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
8	PCM	R/W	0h	Force position-compare match interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
7	PCR	R/W	0h	Force position-compare ready interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
6	PCO	R/W	0h	Force position counter overflow interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt

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Table 24-44. QFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PCU	R/W	0h	Force position counter underflow interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
4	WTO	R/W	0h	Force watchdog time out interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
3	QDC	R/W	0h	Force quadrature direction change interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
2	PHE	R/W	0h	Force quadrature phase error interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
1	PCE	R/W	0h	Force position counter error interrupt Reset type: SYSRSn 0h (R/W) = No effect 1h (R/W) = Force the interrupt
0	RESERVED	R	0h	Reserved

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20 QEPSTS Register (Offset = 38h) [Reset = 0000h]

QEPSTS is shown in Figure 24-45 and described in Table 24-26.

Return to the Summary Table.

QEP Status

Figure 24-45. QEPSTS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W1C-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h

Table 24-46. QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	UPEVNT	R/W1C	0h	Unit position event flag Reset type: SYSRSn 0h (R/W) = No unit position event detected 1h (R/W) = Unit position event detected. Write 1 to clear
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Reset type: SYSRSn 0h (R/W) = Counter-clockwise rotation (or reverse movement) on the first index event 1h (R/W) = Clockwise rotation (or forward movement) on the first index event
5	QDF	R	0h	Quadrature direction flag Reset type: SYSRSn 0h (R/W) = Counter-clockwise rotation (or reverse movement) 1h (R/W) = Clockwise rotation (or forward movement)
4	QDLF	R	0h	eQEP direction latch flag Reset type: SYSRSn 0h (R/W) = Counter-clockwise rotation (or reverse movement) on index event marker 1h (R/W) = Clockwise rotation (or forward movement) on index event marker
3	COEF	R/W1C	0h	Capture overflow error flag Reset type: SYSRSn 0h (R/W) = Overflow has not occurred. 1h (R/W) = Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	R/W1C	0h	Capture direction error flag Reset type: SYSRSn 0h (R/W) = Capture direction error has not occurred. 1h (R/W) = Direction change occurred between the capture position event. This bit is cleared by writing a '1'.

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Table 24-46. QEPSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FIMF	R/W1C	0h	First index marker flag Reset type: SYSRSn 0h (R/W) = First index pulse has not occurred. 1h (R/W) = Set by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Reset type: SYSRSn 0h (R/W) = No error occurred during the last index transition 1h (R/W) = Position counter error

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21 QCTMR Register (Offset = 3Ah) [Reset = 0000h]

QCTMR is shown in Figure 24-46 and described in Table 24-27.

Return to the Summary Table.

QEP Capture Timer

Figure 24-46. QCTMR Register

15	14	13	12	11	10	9	8
QCTMR							
R/W-0h							
7	6	5	4	3	2	1	0
QCTMR							
R/W-0h							

Table 24-48. QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCTMR	R/W	0h	This register provides time base for edge capture unit. Reset type: SYSRSn

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22 QCPRD Register (Offset = 3Ch) [Reset = 0000h]

QCPRD is shown in Figure 24-47 and described in Table 24-28.

Return to the Summary Table.

QEP Capture Period

Figure 24-47. QCPRD Register

15	14	13	12	11	10	9	8
QCPRD							
R/W-0h							
7	6	5	4	3	2	1	0
QCPRD							
R/W-0h							

Table 24-50. QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events Reset type: SYSRSn

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23 QCTMRLAT Register (Offset = 3Eh) [Reset = 0000h]

QCTMRLAT is shown in Figure 24-48 and described in Table 24-29.

Return to the Summary Table.

QEP Capture Latch

Figure 24-48. QCTMRLAT Register

15	14	13	12	11	10	9	8
QCTMRLAT							
R-0h							
7	6	5	4	3	2	1	0
QCTMRLAT							
R-0h							

Table 24-52. QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter. Reset type: SYSRSn

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24 QCPRDLAT Register (Offset = 40h) [Reset = 0000h]

QCPRDLAT is shown in Figure 24-49 and described in Table 24-30.

Return to the Summary Table.

QEP Capture Period Latch

Figure 24-49. QCPRDLAT Register

15	14	13	12	11	10	9	8
QCPRDLAT							
R-0h							
7	6	5	4	3	2	1	0
QCPRDLAT							
R-0h							

Table 24-54. QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	QCPRDLAT	R	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter. Reset type: SYSRSn

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25 REV Register (Offset = 60h) [Reset = 00000009h]

REV is shown in Figure 24-50 and described in Table 24-31.

Return to the Summary Table.

QEP Revision Number

Figure 24-50. REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MINOR			MAJOR		
R-0-0h										R-1h			R-1h		

Table 24-56. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5-3	MINOR	R	1h	This field specifies the Minor Revision number for the eQEP IP. Reset type: N/A
2-0	MAJOR	R	1h	This field specifies the Major Revision number for the eQEP IP. Reset type: N/A

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26 QEPSTROBESEL Register (Offset = 64h) [Reset = 00000000h]

QEPSTROBESEL is shown in Figure 24-51 and described in Table 24-32.

Return to the Summary Table.

QEP Strobe select register

Figure 24-51. QEPSTROBESEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						STROBESEL	
R-0-0h						R/W-0h	

Table 24-58. QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1-0	STROBESEL	R/W	0h	Strobe source select: Reset type: SYSRSn 0h (R/W) = QEP Strobe after polarity mux 1h (R/W) = QEP Strobe after polarity mux 2h (R/W) = QEP Strobe after polarity mux ORed with ADCSOCA 3h (R/W) = QEP Strobe after polarity mux ORed with ADCSOCB

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27 QMACTRL Register (Offset = 68h) [Reset = 00000000h]

QMACTRL is shown in Figure 24-52 and described in Table 24-33.

Return to the Summary Table.

QMA Control register

Figure 24-52. QMACTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MODE		
R-0-0h													R/W-0h		

Table 24-60. QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R-0	0h	Reserved
2-0	MODE	R/W	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed (reserved) 1xx : QMA Module is bypassed (reserved) Reset type: SYSRSn

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28 QEPSRCSEL Register (Offset = 6Ch) [Reset = 00000000h]

QEPSRCSEL is shown in Figure 24-53 and described in Table 24-34.

Return to the Summary Table.

QEP Source Select Register

Figure 24-53. QEPSRCSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEPSSEL				QEPISEL				QEPBSEL				QEPASEL			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

Table 24-62. QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-12	QEPSSEL	R/W	0h	QEP Strobe source select: 0x0: From device Pins (Default). Others: Tied to zero. Reset type: SYSRSn
11-8	QEPISEL	R/W	0h	QEP Index source select: 0x0: Device Pin (Default) 0x1 to 0x1F : Refer to EQEP chaper of TRM Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset type: SYSRSn
7-4	QEPBSEL	R/W	0h	QEPB source select: 0x0: Device Pin (Default) 0x1 to 0x1F : Refer to EQEP chaper of TRM Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset type: SYSRSn
3-0	QEPASEL	R/W	0h	QEPA source select: 0x0: Device Pin (Default) 0x1 to 0x1F : Refer to EQEP chaper of TRM Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. Reset type: SYSRSn

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Chapter 25

Enhanced Pulse Width Modulator (ePWM)

The enhanced pulse width modulator (ePWM) peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. These systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The ePWM peripheral can also perform a digital-to-analog (DAC) function, where the duty cycle is equivalent to a DAC analog value; it is sometimes referred to as a power DAC.

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25.1 Introduction

This chapter includes an overview and information about each submodule:

- Time Base (TB) Submodule
- Counter Compare (CC) Submodule
- Action Qualifier (AQ) Submodule
- Dead-Band Generator (DB) Submodule
- PWM Chopper (PC) Submodule
- Trip Zone (TZ) Submodule
- Event Trigger (ET) Submodule
- Digital Compare (DC) Submodule

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention and must be highly programmable and very flexible while being easy to understand and use. The ePWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the ePWM is built up from smaller single channel submodules with separate resources that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand the operation quickly.

In this document, the letter x within a signal or submodule name is used to indicate a generic ePWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the ePWMx instance. Thus, EPWM1A and EPWM1B belong to ePWM1 and likewise EPWM4A and EPWM4B belong to ePWM4.

25.1.1 EPWM Related Collateral

Foundational Materials

- *Real-Time Control Reference Guide*
  - Refer to the PWM section

Getting Started Materials

- *C2000 ePWM Developer's Guide Application Report*
- Enhanced Pulse Width Modulator (ePWM) Training for C2000 MCUs (Video)
- *Flexible PWMs Enable Multi-Axis Drives, Multi-Level Inverters Application Report*
- Getting Started with the C2000 ePWM Module (Video)
- *Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Control Application Report*
  - Chapters 1 to 6 are Fundamental material, derivations, and explanations that are useful for learning about how PWM can be used to implement a DAC. Subsequent chapters are Getting Started and Expert material for implementing in a system.
- *Using the Enhanced Pulse Width Modulator (ePWM) Module Application Report*

Expert Materials

- *CRM/ZVS PFC Implementation Based on C2000 Type-4 PWM Module Application Report*
- *Leverage New Type ePWM Features for Multiple Phase Control Application Report*

Note

The AM13E232x ePWM module is the same peripheral as the C2000 Type 4 ePWM module. While many of the above application reports refer to the C2000™ Family MCUs, many of the ePWM peripheral level configuration concepts can be applied to the AM13E232x ePWM.

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25.1.2 Submodule Overview

The ePWM module represents one complete PWM channel composed of two PWM outputs: EPWMxA and EPWMxB. Multiple ePWM modules are instanced within a device as shown in . Each ePWM instance is identical with one exception. Some or all ePWM instances include a hardware extension that allows more precise control of the PWM outputs. This extension is the high-resolution pulse width modulator (HRPWM) and is described in Figure 25-1. See the device data sheet to determine which ePWM instances include this feature. Each ePWM module is indicated by a numerical value starting with 1. For example, ePWM1 is the first instance and ePWM3 is the third instance in the system and ePWMx indicates any instance.

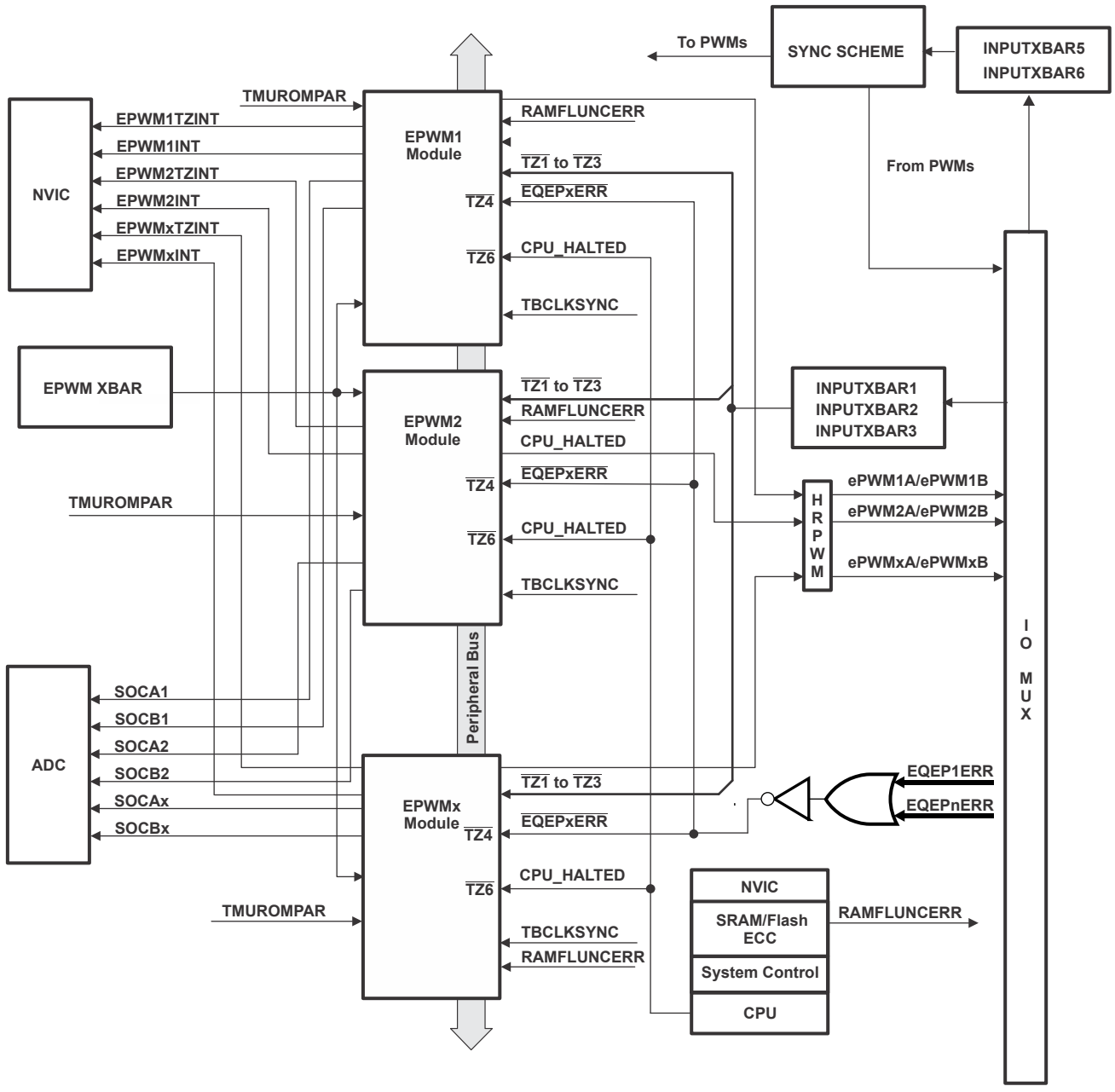


Figure 25-1. Multiple ePWM Modules

The ePWM modules are chained together by way of a clock synchronization scheme that allows them to operate as a single system when required. Additionally, this synchronization scheme can be extended to the capture

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peripheral submodules (eCAP). The number of submodules is device-dependent and based on target application needs. Submodules can also operate standalone.

Each ePWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software.
- Programmable phase-control support for lag or lead operation relative to other ePWM modules.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs.
- All events can trigger both CPU interrupts and ADC start of conversion (SOC)
- Programmable event prescaling minimizes CPU overhead on interrupts.
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives.

Each ePWM module is connected to the input/output signals shown in Figure 25-2. The signals are described in detail in subsequent sections.

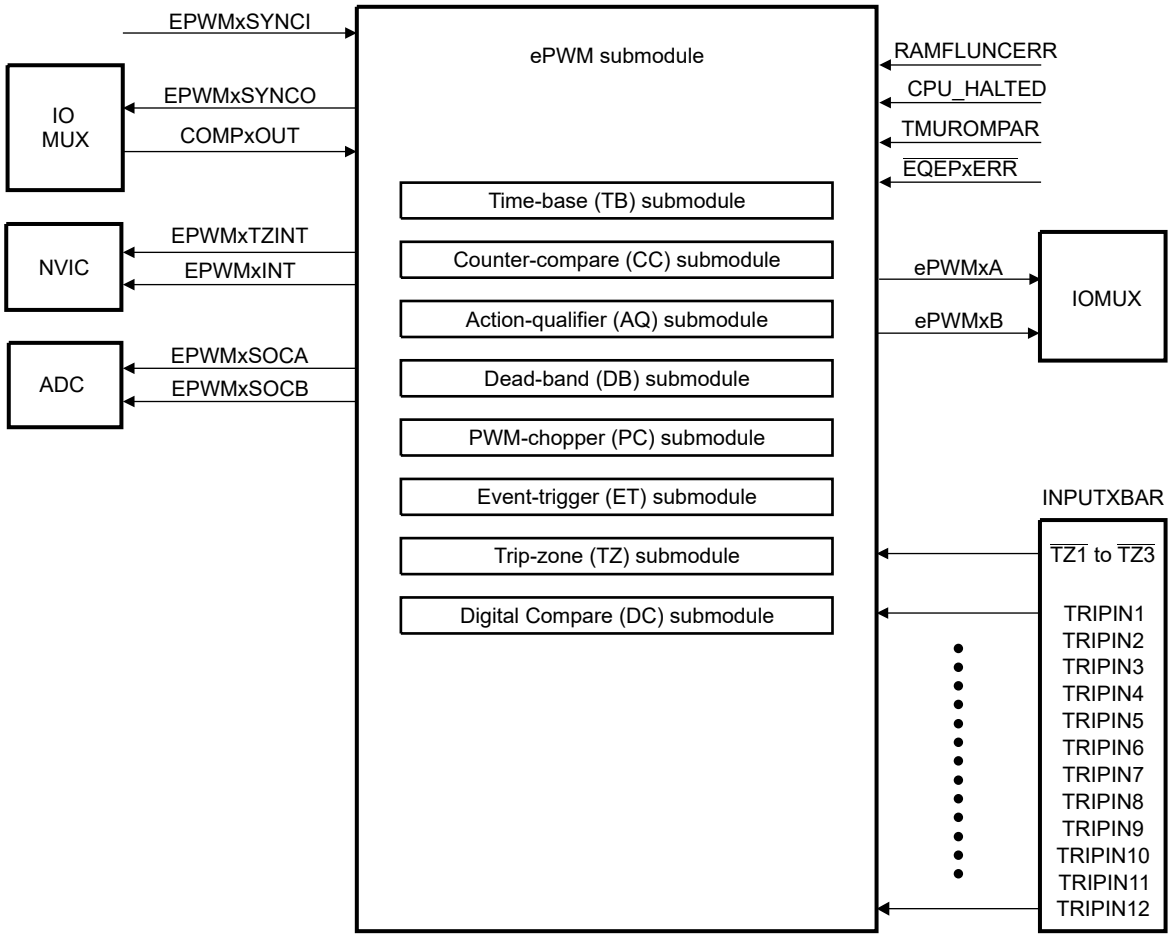


Figure 25-2. Submodules and Signal Connections for an ePWM Module

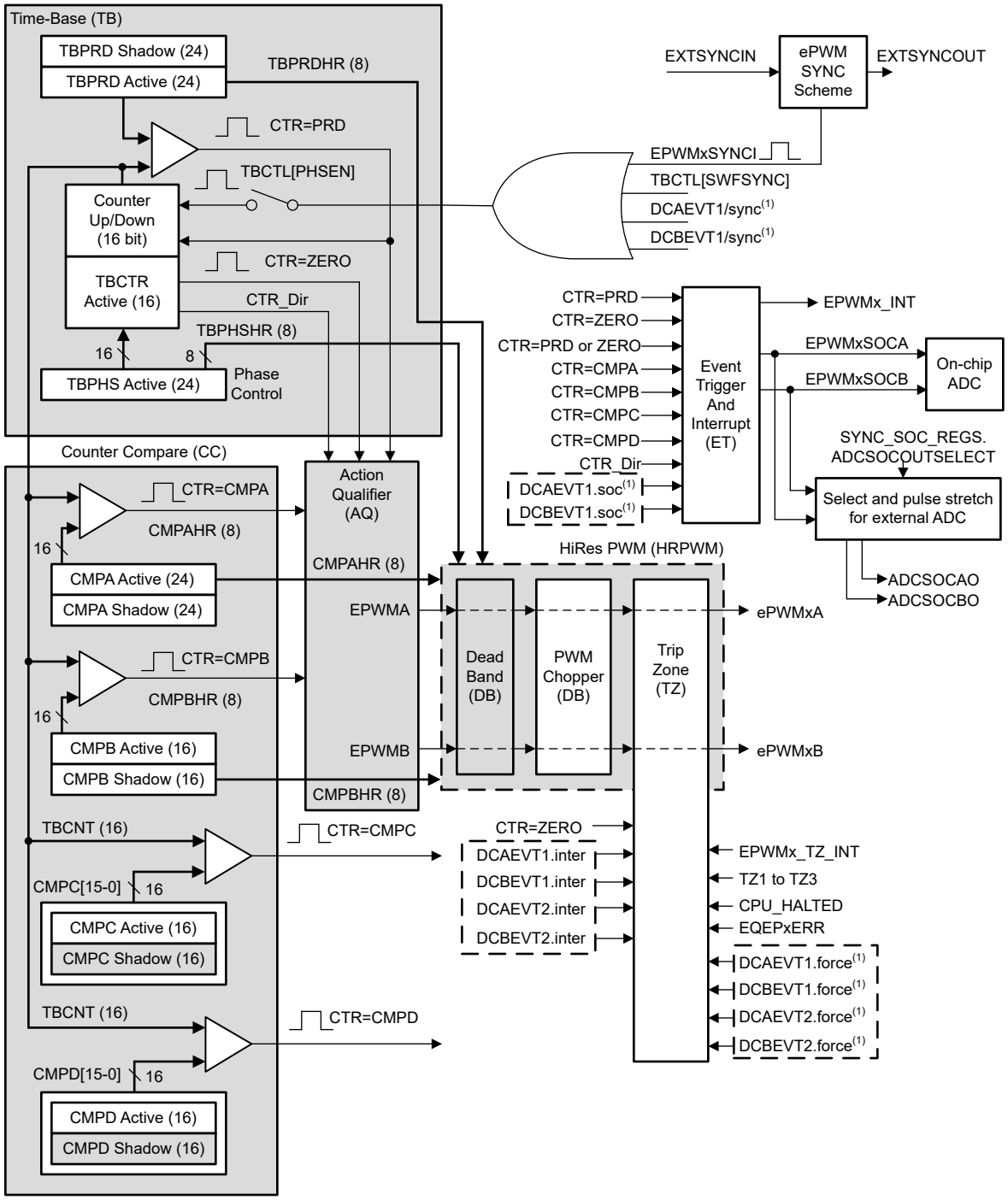
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Figure 25-3 shows more internal details of a single ePWM module. The main signals used by the ePWM module are:

- **PWM output signals (EPWMxA and EPWMxB):** The PWM output signals are made available external to the device.
- **Trip-zone signals ($\overline{TZ1}$ to $\overline{TZ6}$):** These input signals alert the ePWM module of fault conditions external to the ePWM module. Each submodule on a device can be configured to either use or ignore any of the trip-zone signals. The $\overline{TZ1}$ to $\overline{TZ3}$ trip-zone signals can be configured as asynchronous inputs through the GPIO peripheral using the Input X-BAR logic. $\overline{TZ4}$ is connected to an inverted EQEPx error signal (EQEPxERR), which can be generated from any one of the EQEP modules. $\overline{TZ5}$ is tied low. $\overline{TZ6}$ is connected to the CPU_HALTED output signal from the CPUSS. This allows the user to configure an automatic trip action when the CPU halts.
- **Time-base synchronization input (EPWMxSYNCI), output (EPWMxSYNCO), and peripheral (EPWMxSYNCPER) signals:** Each ePWM module can be synchronized with other ePWM modules or other peripherals, using EPWMSYNCINSEL. Each ePWM module can also generate a synchronization output signal. The source of the EPWMxSYNCOUT can be selected and enabled by EPWMSYNCOUTEN and TBCTL2.OSHTSYNCMODE. For more information, see Section 25.4.3.3 .

  Each ePWM module also generates another PWMSYNC signal called EPWMxSYNCPER. EPWMxSYNCPER goes to the CMPSS for synchronization purposes. Functionality is configured using the HRPCTL register, but has no relation with the HRPWM. For more information on how EPWMxSYNCPER is used by the CMPSS, see the respective chapter.
- **ADC start-of-conversion signals (EPWMxSOCA and EPWMxSOCB):** Each ePWM module has two ADC start of conversion signals. Any ePWM module can trigger a start of conversion. Whichever event triggers the start of conversion is configured in the event-trigger submodule of the ePWM. See Section 25.10 for more details.
- **Comparator output signals (COMPxOUT):** Output signals from the comparator module can be applied through the Input X-BAR and EPWM X-BAR to certain trip inputs (see Section 19.2.1 and Section 19.1 for options) and in conjunction with the trip zone signals can generate digital compare events.
- **Peripheral bus:** The ePWM peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the ePWM register file.

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Note

These events are generated by the ePWM Digital Compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 25-3. ePWM Modules and Critical Internal Signal Interconnects

25.2 Configuring Device Pins

To connect the device input pins to the module, the Input X-BAR must be used. TRIPx signals TRIP4-12, excluding TRIP6, must be routed through the PWM X-Bar in addition to the Input X-Bar. Examples of ePWM

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signals that often need to be sourced from device pins are TZx, TRIPx, and EXTSYNCIN. See the Section 19 chapter for information on routing input signals to the ePWM module. Any GPIO on the device can be configured as an input. See Section 14.2.3 for information about how to synchronize the pin state to the ULPCLK and apply an optional glitch filter to the input. To invert the logic of the incoming signal, configure the IOMUX register as described in Section 16.2.3 . To connect the input to an internal pull-up or pull-down resistor, see Section 16.2.5 .

The IOMUX registers must be configured to route the ePWM module input and output signals to IOs on the device. See Section 16.2.1 for more information about how to configure an IO for a specific peripheral function.

25.3 ePWM Modules Overview

Eight submodules are included in every ePWM peripheral. Each of these submodules performs specific tasks that can be configured by software.

Table 25-1 lists the key submodules together with a list of the main configuration parameters. For example, if you need to adjust or control the duty cycle of a PWM waveform, see the counter-compare submodule in Section 25.3 for relevant details.

Table 25-1. Submodule Configuration Parameters

Submodule	Configuration Parameter or Option
Time Base (TB)	• Scale the time-base clock (TBCLK) relative to the ePWM clock (EPWMCLK). • Configure the PWM time-base counter (TBCTR) frequency or period. • Set the mode for the time-base counter: – count-up mode: used for asymmetric PWM – count-down mode: used for asymmetric PWM – count-up-and-down mode: used for symmetric PWM • Configure the time-base phase relative to another ePWM module. • Synchronize the time-base counter between modules through hardware or software. • Configure the direction (up or down) of the time-base counter after a synchronization event. • Simultaneous writes to the TBPRD registers on all PWM's corresponding to the configuration on EPWMXLINK. • Configure how the time-base counter behaves when the device is halted by an emulator. • Specify the source for the synchronization output of the ePWM module • Configure one shot and global load of registers in this module.
Counter Compare (CC)	• Specify the PWM duty cycle for output EPWMxA and output EPWMxB • Specify the time at which switching events occur on the EPWMxA or EPWMxB output • Specify the programmable delay for interrupt and SOC generation with additional comparators • Simultaneous writes to the CMPA, CMPB, CMPC, CMPD registers on all PWM's corresponding to the configuration on EPWMXLINK. • Configure one shot and global load of registers in this module.
Action Qualifier (AQ)	• Specify the type of action taken when a time-base counter-compare, trip-zone submodule, or comparator event occurs: – No action taken – Output EPWMxA and EPWMxB switched high – Output EPWMxA and EPWMxB switched low – Output EPWMxA and EPWMxB toggled • Force the PWM output state through software control • Configure and control the PWM dead band through software • Configure one shot and global load of registers in this module.

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Table 25-1. Submodule Configuration Parameters (continued)

Submodule	Configuration Parameter or Option
Dead-Band Generator (DB)	• Control of traditional complementary dead-band relationship between upper and lower switches • Specify the output rising-edge-delay value • Specify the output falling-edge delay value • Bypass the dead-band module entirely. In this case the PWM waveform is passed through without modification. • Option to enable half-cycle clocking for double resolution. • Allow ePWMxB phase shifting with respect to the ePWMxA output. • Configure one shot and global load of registers in this module.
PWM Chopper (PC)	• Create a chopping (carrier) frequency. • Pulse width of the first pulse in the chopped pulse train. • Duty cycle of the second and subsequent pulses. • Bypass the PWM chopper module entirely. In this case the PWM waveform is passed through without modification.
Trip Zone (TZ)	• Configure the ePWM module to react to one, all, or none of the trip-zone signals or digital compare events. • Specify the trip action taken when a fault occurs: – Force EPWMxA and EPWMxB high – Force EPWMxA and EPWMxB low – Force EPWMxA and EPWMxB to a high-impedance state – Configure EPWMxA and EPWMxB to ignore any trip condition. • Configure how often the ePWM reacts to each trip-zone signal: – One-shot – Cycle-by-cycle • Enable the trip-zone to initiate an interrupt. • Bypass the trip-zone module entirely. • Programmable option for cycle-by-cycle trip clear • If desired, independently configure trip actions taken when time-base counter is counting down.
Event Trigger (ET)	• Enable the ePWM events that trigger an interrupt. • Enable ePWM events that trigger an ADC start-of-conversion event. • Specify the rate at which events cause triggers (every occurrence or every 2nd or up to 15th occurrence) • Poll, set, or clear event flags
Digital Compare (DC)	• Enables comparator (COMP) module outputs and trip zone signals which are configured using the Input X-BAR to create events and filtered events • Specify event-filtering options to capture TBCTR counter, generate blanking window, or insert delay in PWM output or time-base counter based on captured value.

25.4 Time-Base (TB) Submodule

Each ePWM module has a time-base submodule that determines all of the event timing for the ePWM module. Built-in synchronization logic allows the time-base of multiple ePWM modules to work together as a single system.

Figure 25-4 illustrates the time-base submodule within the ePWM.

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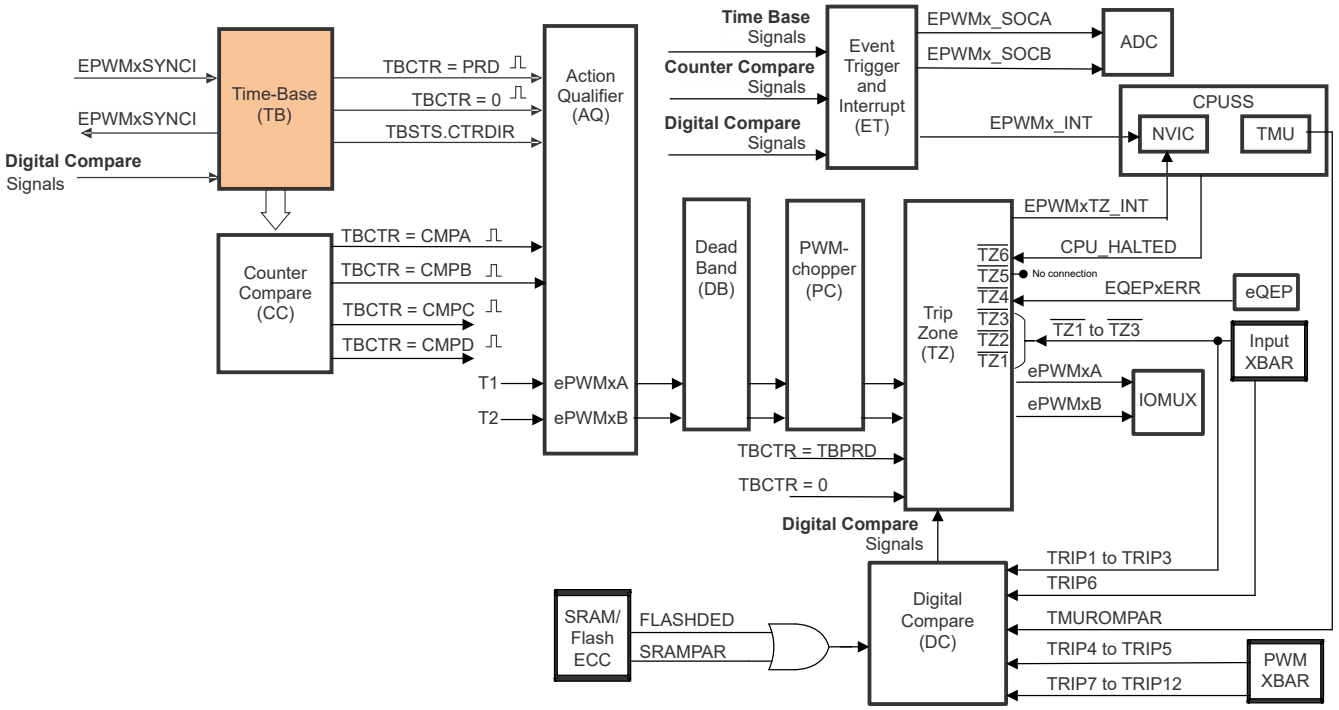


Figure 25-4. Time-Base Submodule

25.4.1 Purpose of the Time-Base Submodule

The time-base submodule can be configured for the following:

- Specify the ePWM time-base counter (TBCTR) frequency or period to control how often events occur.
- Manage time-base synchronization with other ePWM modules.
- Maintain a phase relationship with other ePWM modules.
- Set the time-base counter to count-up, count-down, or count-up-and-down mode.
- Generate the following events:
  - CTR = PRD: Time-base counter equal to the specified period (TBCTR = TBPRD).
  - CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00).
- Configure the rate of the time-base clock; a prescaled version of the ePWM clock (EPWMCLK). This allows the time-base counter to increment/decrement at a slower rate.

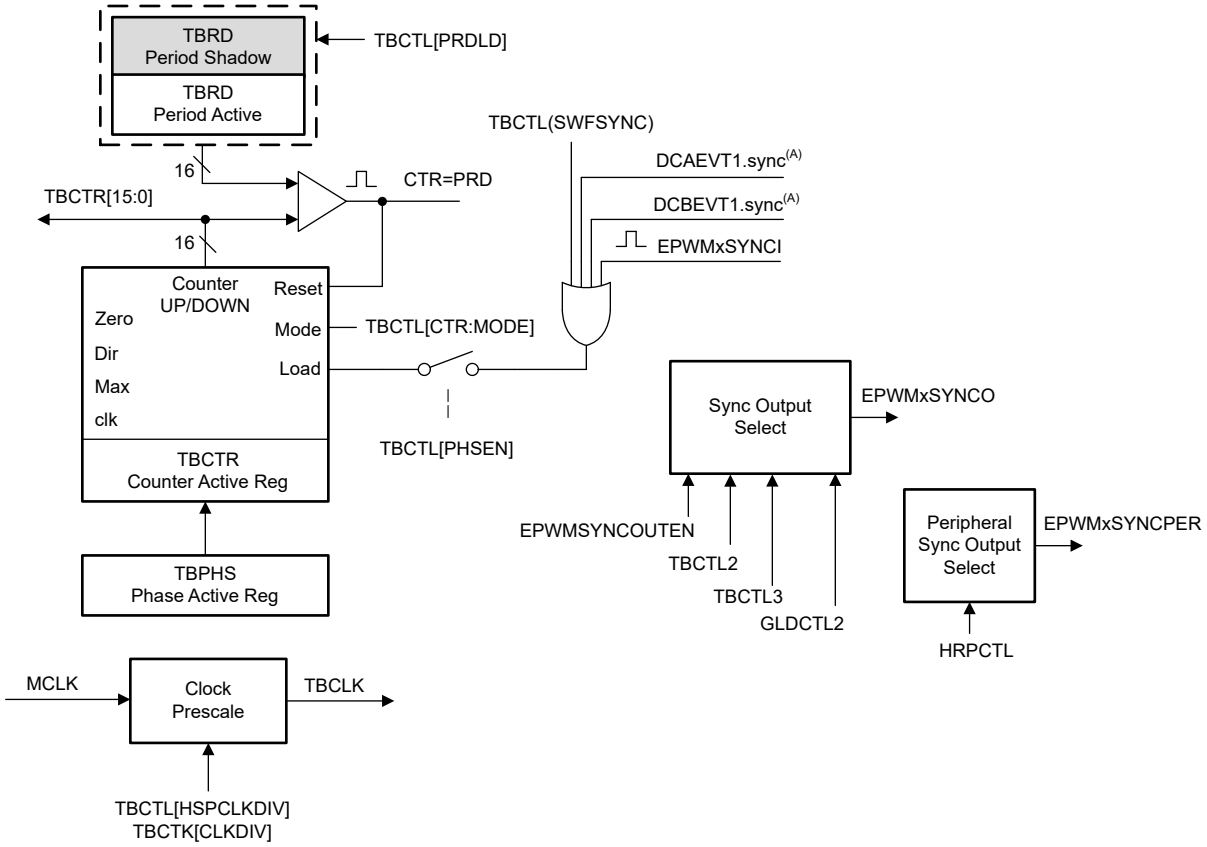
Note

If required by the application code to update the TBCTR value through software while the TBCTR is counting, note that the time-base module needs at least 1 TBCLK cycle for the time-base related events to be realized. Hence, the TBCTR can be written with TBCTR = PRD-1 instead of TBCTR = PRD (in case the counter is counting up) and can be written as TBCTR = 1 instead of TBCTR = 0 (in case the counter is counting down) for the events to be realized.

25.4.2 Controlling and Monitoring the Time-Base Submodule

The block diagram in Figure 25-5 shows the critical signals and registers of the time-base submodule. Table 25-2 provides descriptions of the key signals associated with the time-base submodule.

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A. These signals are generated by the digital compare (DC) submodule.

Figure 25-5. Time-Base Submodule Signals and Registers

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Table 25-2. Key Time-Base Signals

Signal	Description
EPWMxSYNCI	Time-base synchronization input. Input pulse used to synchronize the time-base counter with the counter of other ePWM modules. For more information on all of the signals available for synchronization, see EPWMSYNCINSEL. For information on the synchronization order of a particular device, see Section 25.4.3.3 .
EPWMxSYNCO	Time-base synchronization output. This output pulse is used to synchronize the counter of other ePWM modules. Using EPWMSYNCOUTEN, TBCTL2, TBCTL3 and GLDCTL2, the source of the output pulse is selected.
EPWMxSYNCPER	Time-base peripheral synchronization output. This output signal is used to synchronize the CMPSS to the EPWM. The output signal can be configured using the HRPCTL register. Note that this signal has no relation with the HRPWM.
CTR = PRD	Time-base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCTR = TBPRD.
CTR = Zero	Time-base counter equal to zero This signal is generated whenever the counter value is zero. That is when TBCTR equals 0x00.
CTR = CMPB	Time-base counter equal to active counter-compare B register (TBCTR = CMPB). This event is generated by the counter-compare submodule and used by the synchronization out logic
CTR_dir	Time-base counter direction. Indicates the current direction of the ePWM's time-base counter. The signal is high when the counter is increasing and the signal is low when the counter is decreasing.
CTR_max	Time-base counter equal max value. (TBCTR = 0xFFFF) Generated event when the TBCTR value reaches the maximum value. This signal is only used only as a status bit
TBCLK	Time-base clock. This is a prescaled version of the ePWM clock (EPWMCLK) and is used by all submodules within the ePWM. This clock determines the rate at which time-base counter increments or decrements.

25.4.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the time-base period (TBPRD) register and the mode of the time-base counter. Figure 25-6 shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count, down-count, and up-down-count time-base counter modes when the period is set to 4 (TBPRD = 4). The time increment for each step is defined by the time-base clock (TBCLK) which is a prescaled version of the ePWM clock (EPWMCLK).

The time-base counter has three modes of operation selected by the time-base control register (TBCTL):

- **Up-Down Count Mode:** In up-down count mode, the time-base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the time-base counter then decrements until the counter reaches zero. At this point, the counter repeats the pattern and begins to increment.
- **Up-Count Mode:** In up-count mode, the time-base counter starts from zero and increments until the counter reaches the value in the period register (TBPRD). When the period value is reached, the time-base counter resets to zero and begins to increment once again.
- **Down-Count Mode:** In down-count mode, the time-base counter starts from the period (TBPRD) value and decrements until the counter reaches zero. When the counter reaches zero, the time-base counter is reset to the period value and begins to decrement once again.

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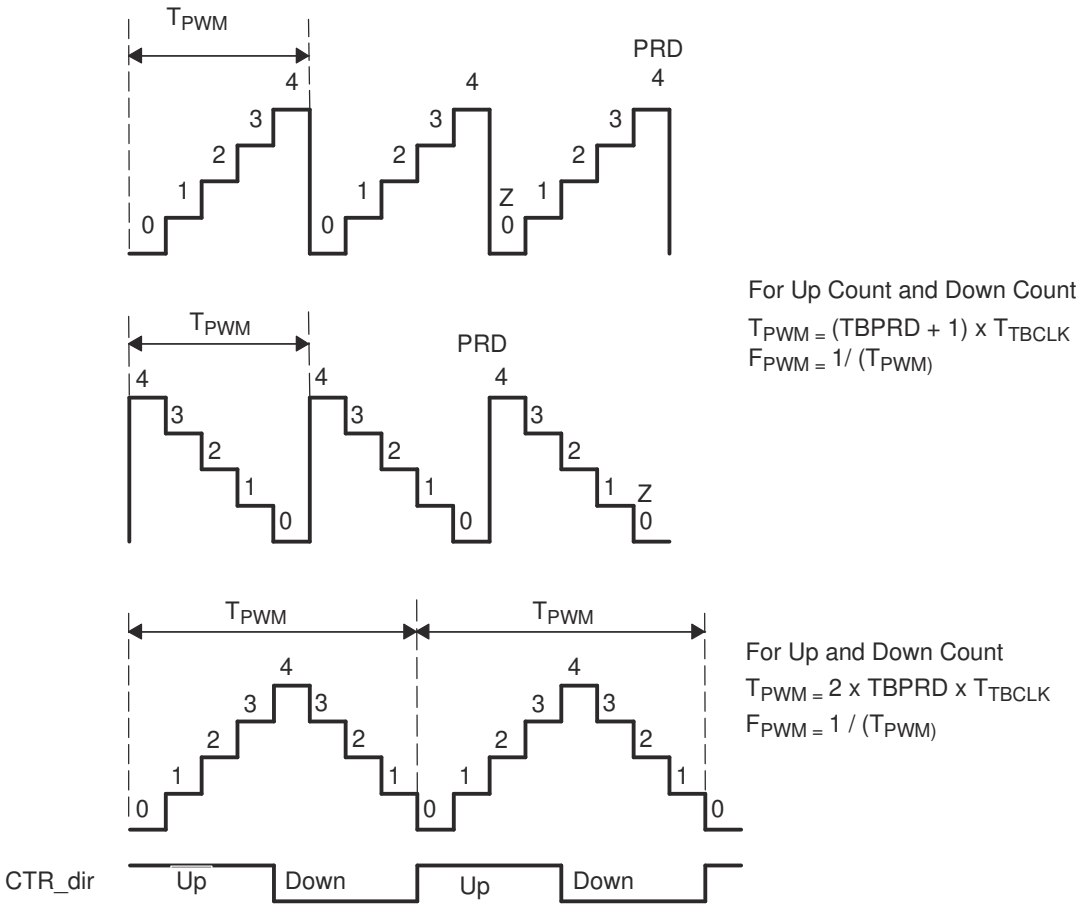


Figure 25-6. Time-Base Frequency and Period

25.4.3.1 Time-Base Period Shadow Register

The time-base period register (TBPRD) has a shadow register. Shadowing allows the register update to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the ePWM module:

- **Active Register:** The active register controls the hardware and is responsible for actions that the hardware causes or invokes.
- **Shadow Register:** The shadow register buffers provide a temporary holding location for the active register and have no direct effect on any control hardware. At a strategic point in time, the shadow register content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

The memory address of the shadow period register is the same as the active register. Which register is written to or read from is determined by the TBCTL[PRDLD] bit. This bit enables and disables the TBPRD shadow register as follows:

- **Time-Base Period Shadow Mode:** The TBPRD shadow register is enabled when TBCTL[PRDLD] = 0. Reads from and writes to the TBPRD memory address go to the shadow register. The shadow register contents are transferred to the active register (TBPRD (Active) ← TBPRD (shadow)) when the time-base counter equals zero (TBCTR = 0x00) and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. The PRDLDSYNC bit is valid only if TBCTL[PRDLD] = 0. By default the TBPRD shadow register is enabled. The sources for the SYNC input is explained in Section 25.4.3.2 .

  The global load control mechanism can also be used with the time-base period register by configuring the appropriate bits in the global load configuration register (GLDCFG). When global load mode is selected the

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transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL). Global load control mechanism is explained in Section 25.4.6 .

- **Time-Base Period Immediate Load Mode:** If immediate load mode is selected (TBCTL[PRDLD] = 1), then a read from or a write to the TBPRD memory address goes directly to the active register.

25.4.3.2 Time-Base Clock Synchronization

The TBCLKSYNC bit in the PERCLKCR register from SYSCTL allows all users to globally synchronize all enabled ePWM modules to the time-base clock (TBCLK). When set, all enabled ePWM module clocks are started with the first rising edge of TBCLK aligned. For synchronized TBCLKs, the prescalers for each ePWM module must be set identically.

The proper procedure for enabling ePWM clocks is as follows:

1. Enable ePWM source clock MCLK by putting the device in RUN or SLEEP mode
2. Set PERCLKCR.TBCLKSYNC = 0
3. Set PWREN.ENABLE bit and write the key to PWREN.KEY in the ePWM registers to allow writes to ePWM registers after 4 cycles.
4. Configure ePWM modules
5. Set PERCLKCR.TBCLKSYNC = 1

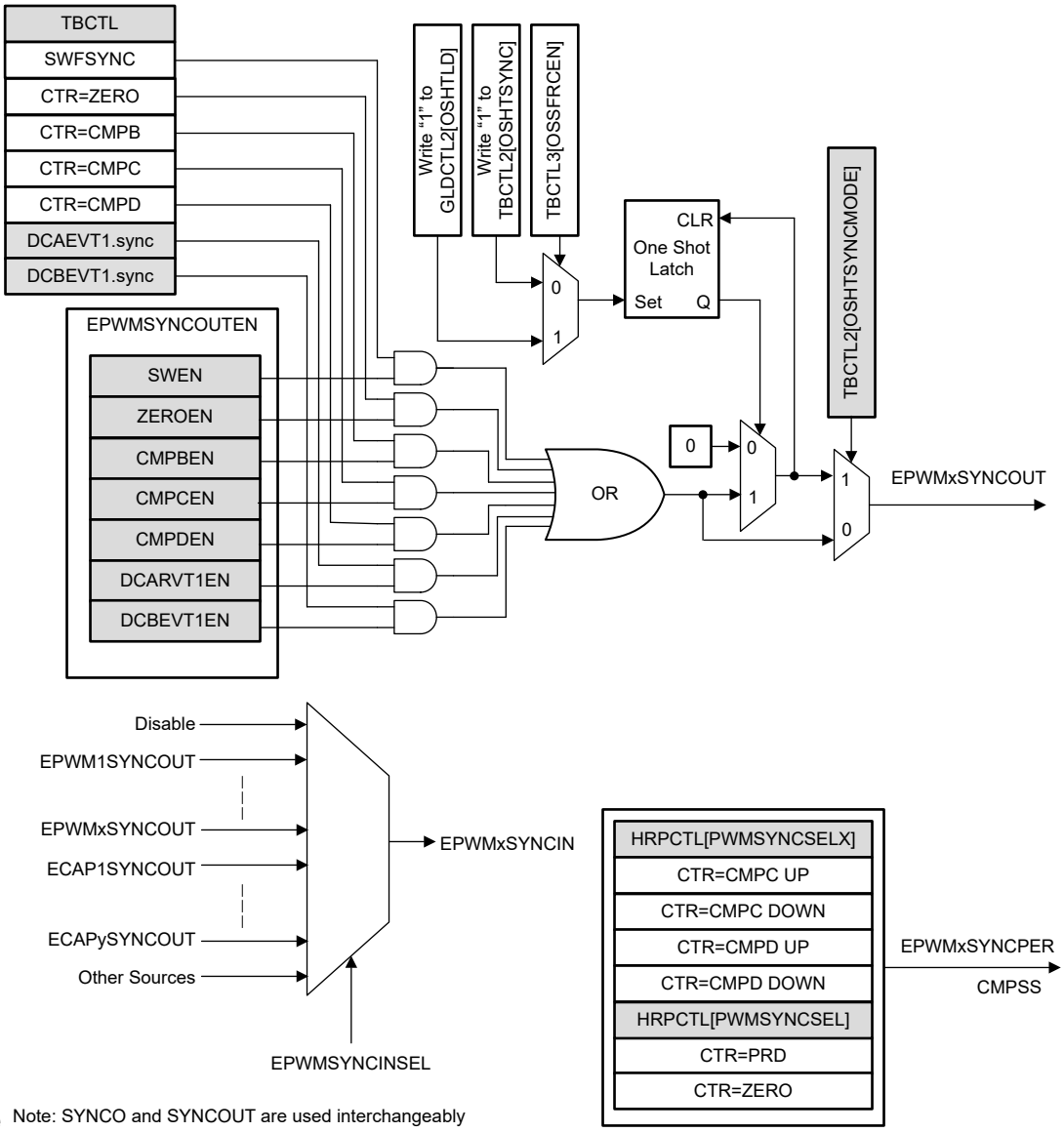
25.4.3.3 Time-Base Counter Synchronization

The ePWM synchronization scheme allows for increased flexibility of synchronization of the ePWM modules. Each ePWM module has a synchronization input (SYNCI), a synchronization output (SYNCO) and a peripheral synchronization output (SYNCPER). In Figure 25-7, EXTSYNCIN1 is sourced from INPUTXBAR5 and EXTSYNCIN2 is sourced from INPUTXBAR6, which can be configured to select any GPIO as the

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synchronization input. Refer to Section 25.4.3.4 for a list of all sync inputs including INPUTXBAR5 and INPUTXBAR6. Figure 25-8 shows the sources that can be used for EXTSYNCOUT.

Figure 25-7. Time-Base Counter Synchronization



Scheme Note: SYNCO and SYNCOUT are used interchangeably

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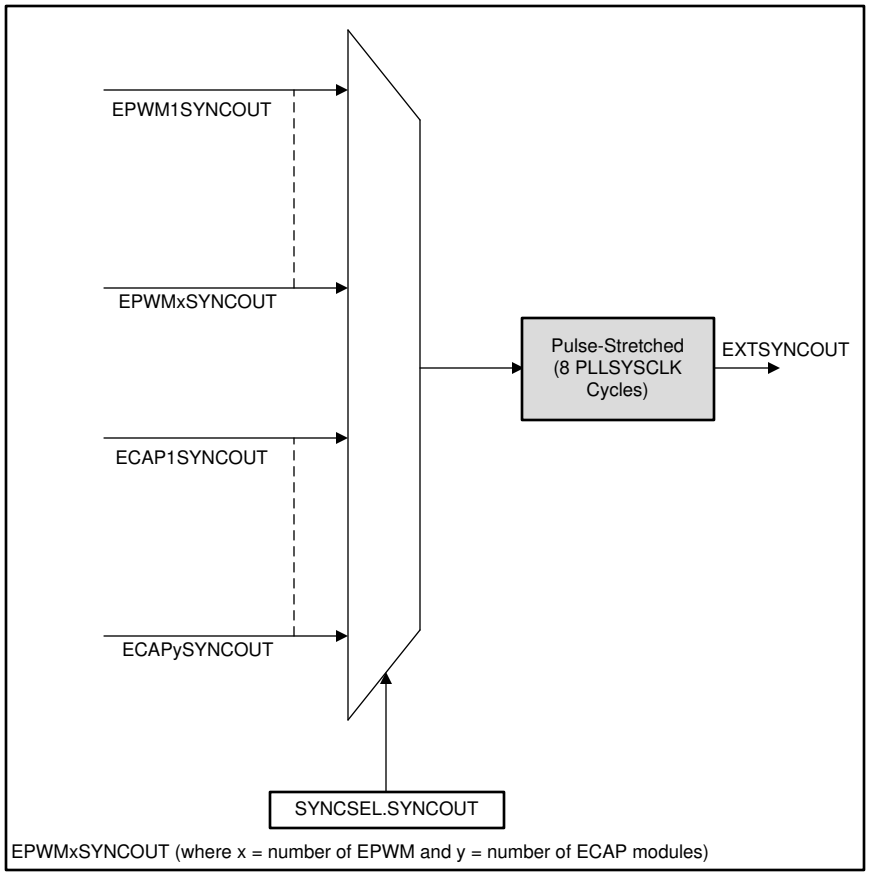


Figure 25-8. ePWM External SYNC Output

Note

See the data sheet for the number of ePWM and eCAP modules available on your specific device.

Each ePWM module can be configured to use or ignore the synchronization input. If the TBCTL[PHSEN] bit is set, then the time-base counter (TBCTR) of the ePWM module is automatically loaded with the phase register (TBPHS) contents when one of the following conditions occur:

- **EPWMxSYNCI: Synchronization Input Pulse:** The value of the phase register is loaded into the counter register when an input synchronization pulse is detected (TBPHS → TBCTR). This operation occurs on the next valid time-base clock (TBCLK) edge.

  The delay from internal control module to target modules is given by:
  - if (TBCLK = EPWMCLK): 2 x EPWMCLK
  - if (TBCLK < EPWMCLK): 1 x TBCLK
- **Software Forced Synchronization Pulse:** Writing a 1 to the TBCTL[SWFSYNC] control bit invokes a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on EPWMxSYNCI.
- **Digital Compare Event Synchronization Pulse:** DCAEVT1 and DCBEVT1 digital compare events can be configured to generate synchronization pulses which have the same affect as EPWMxSYNCI.

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Note

If the EPWMxSYNCI signal is held high, the sync does not continuously occur. The EPWMxSYNCI is rising edge activated. When modifying the TBPHS register during run-time, missed action qualifier events can occur due to sudden jumps in the TBCTR value at the time of the SYNCIN pulse. To recreate the behavior of missed action qualifier events, configure an action qualifier event on a T1 or T2 event on a SYNCIN event. The T1 or T2 action qualifier event must be enabled and disabled during runtime depending on the value of TBPHS.

This feature enables the ePWM module to be automatically synchronized to the time base of another ePWM module. Lead or lag phase control can be added to the waveforms generated by different ePWM modules to synchronize them. In up-down-count mode, the TBCTL[PHSDIR] bit configures the direction of the time-base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The PHSDIR bit is ignored in count-up or count-down modes. See Figure 25-9 through Figure 25-10 for examples.

Clearing the TBCTL[PHSEN] bit configures the ePWM to ignore the synchronization input pulse.

25.4.3.4 ePWM Sync Selection

The below table specifies the sources for the ePWM Sync options in the EPWMSYNCINSEL.SEL register field.

Table 25-3. PWM and eCAP SYNC Selection

PWM*.SYNCINSEL ECAP*.SYNCINSEL	Input Signal
0	Disable
1	Reserved
2	Reserved
3	ECAP0_SYNCOUT
4	ECAP1_SYNCOUT
5	MCPWM0_SYNCOUT
6	MCPWM1_SYNCOUT
7	MCPWM2_SYNCOUT
8	Reserved
9	Reserved
10	ECAP2_SYNCOUT
11	EPWM0_SYNCOUT
12	EPWM1_SYNCOUT
13	EPWM2_SYNCOUT
14	EPWM3_SYNCOUT
15	EPWM4_SYNCOUT
16	EPWM5_SYNCOUT
17	ECAT_SYNC0
18	ECAT_SYNC1
19	FSIRX_TRIG1
20	INPUTXBAROUT5
21	INPUTXBAROUT6
22-31	Reserved

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25.4.4 Time-Base Counter Modes and Timing Waveforms

The time-base counter operates in one of four modes:

- Up-count mode that is asymmetrical
- Down-count mode that is asymmetrical
- Up-down-count that is symmetrical
- Frozen where the time-base counter is held constant at the current value

To illustrate the operation of the first three modes, the following timing diagrams show when events are generated and how the time-base responds to an EPWMxSYNCI signal.

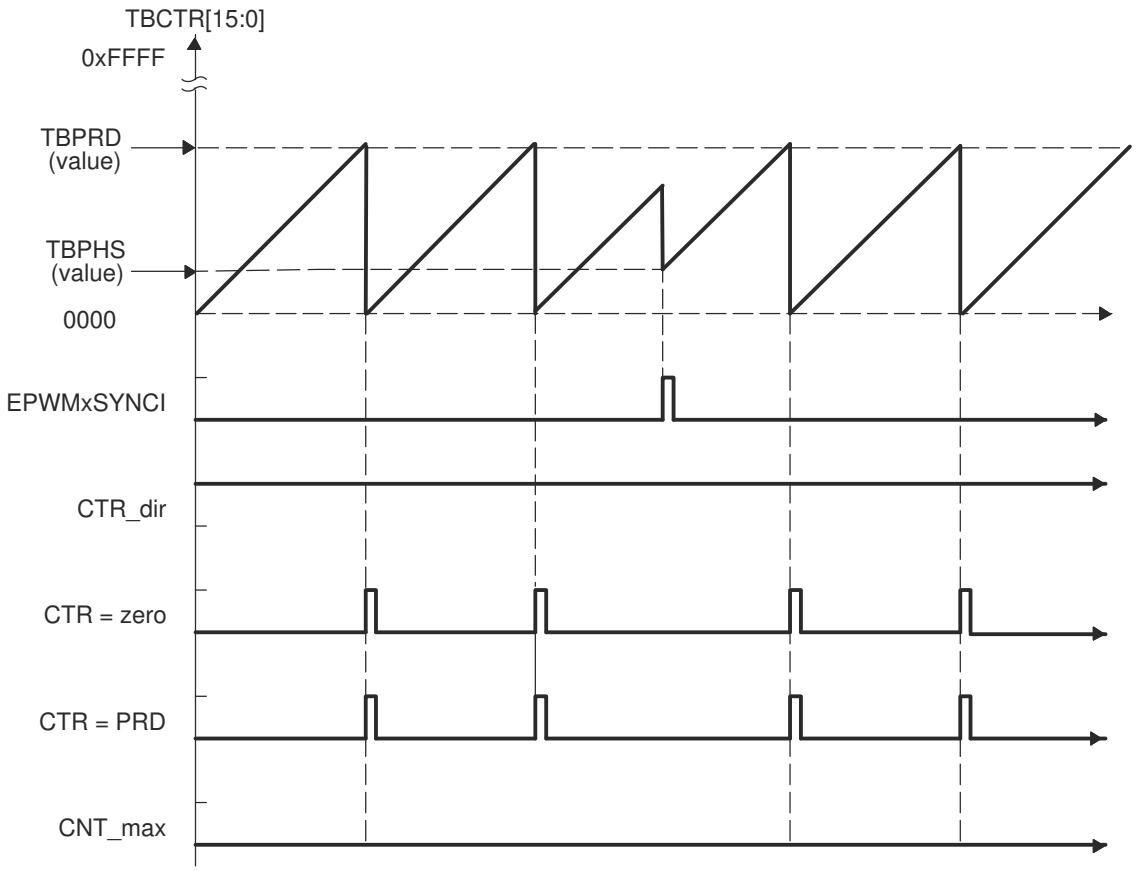


Figure 25-9. Time-Base Up-Count Mode Waveforms

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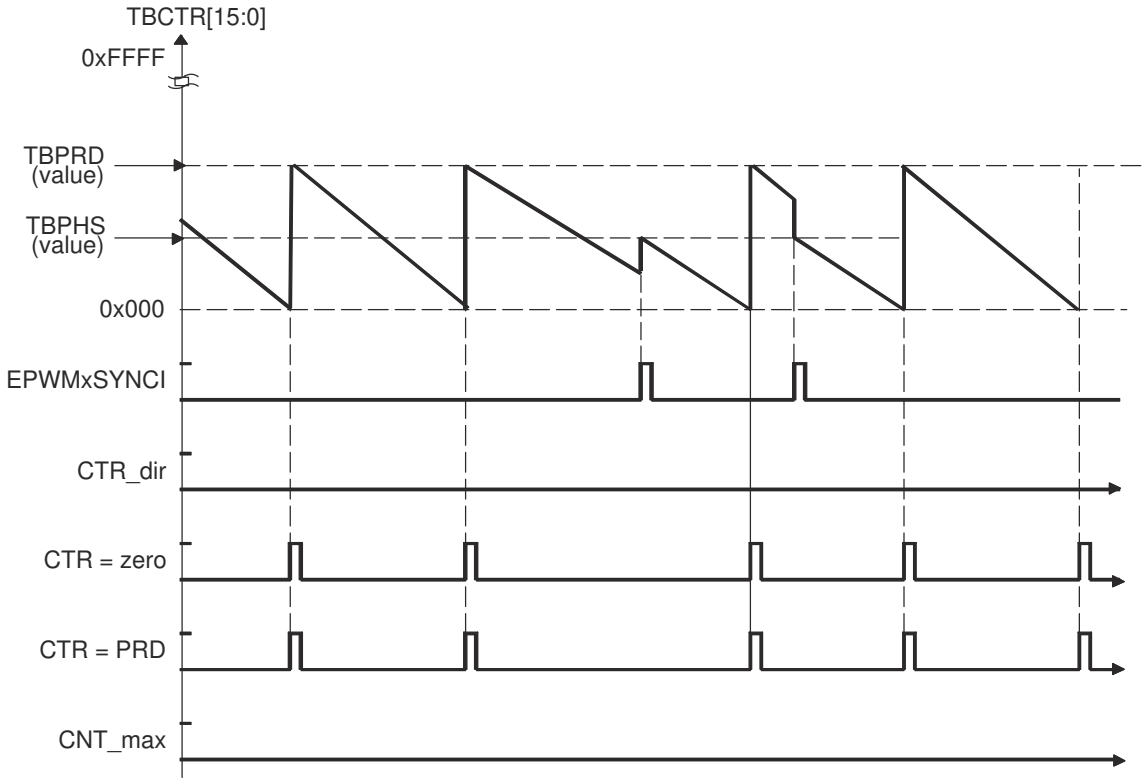


Figure 25-10. Time-Base Down-Count Mode Waveforms

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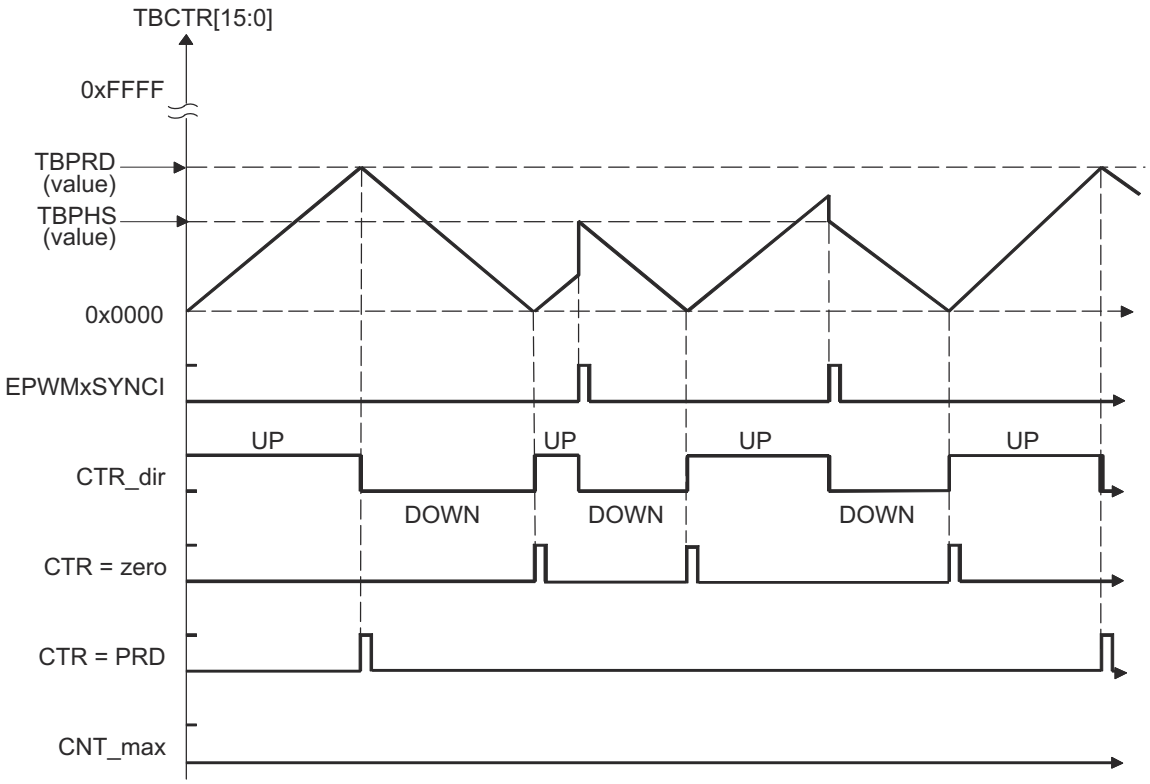


Figure 25-11. Time-Base Up-Down-Count Waveforms, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

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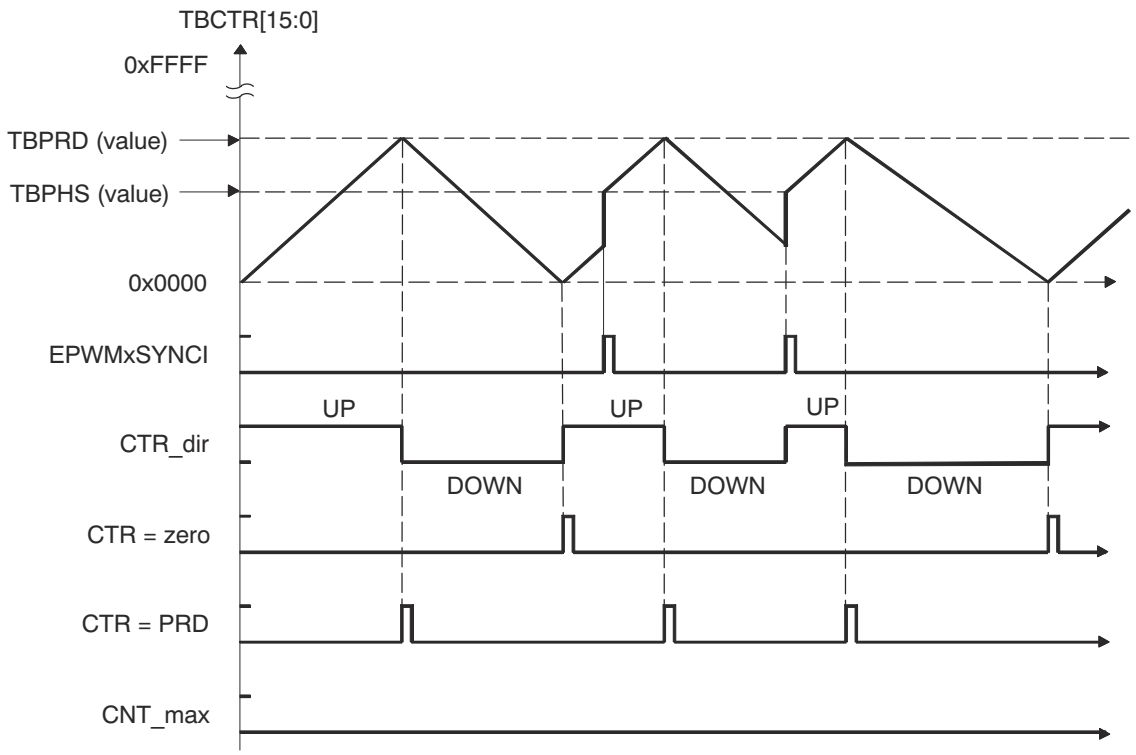


Figure 25-12. Time-Base Up-Down Count Waveforms, TBCTL[PHSDIR = 1] Count Up On Synchronization Event

25.4.5 Simultaneous Writes to TBPRD and CMPx Registers Between ePWM Modules

For variable frequency applications, there is a need for simultaneous writes of TBPRD and CMPx registers between ePWM modules. This prevents situations where a CTR = 0 or CTR = PRD pulse forces a shadow to active load of these registers before all registers are updated between ePWM modules (resulting in some registers being loaded from new shadow values while others are loaded from old shadow values). To support this, an ePWM register linking scheme for TBPRD.TBPRDHR, CMPA.CMPAHR, CMPB.CMPBHR, CMPC, and CMPD registers between PWM modules has been added.

Refer to the register description for EPWMXLINK to see the linked register bitfield values for corresponding ePWM. An example of using the EPWMXLINK is linking ePWM2 CMPA with CMPA of ePWM1 through ePWM2's EPWMXLINK[CMPALINK] register bitfield. In this case, a write to CMPA of ePWM1 also changes the CMPA value for ePWM2.

Note

For PWM instances assigned to multiple peripheral frames, XLINK doesn't work across frames. For example, if EPWM1 is assigned to frame0 and another EPWM2 is assigned to frame1 and XLINK feature is enabled between ePWM modules. A write to frame0's ePWM does not result in a change in frame1's ePWM register and vice versa that has XLINK enabled.

25.4.6 Global Load

Figure 25-13 shows the signals and registers associated with the global load feature.

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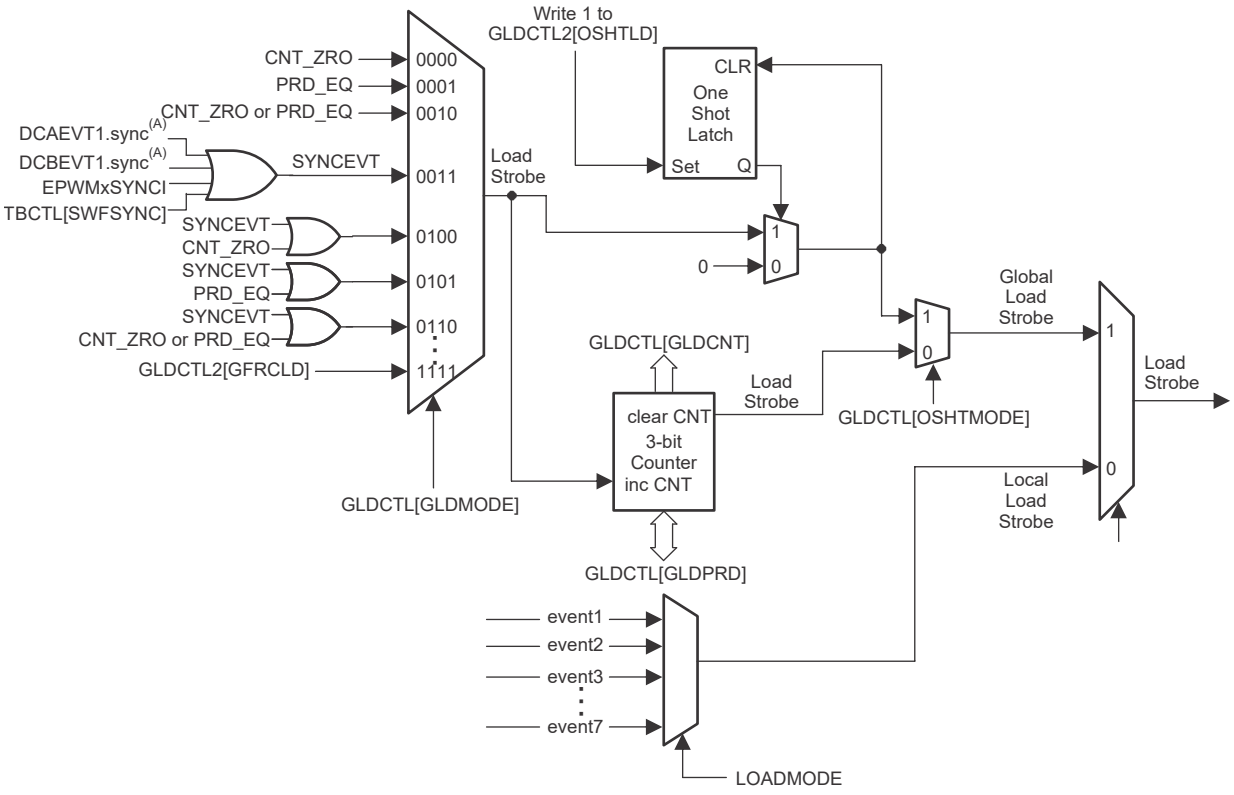


Figure 25-13. Global Load: Signals and Registers

Note

The SYNCEVT signal is only propagated through when PHSEN is SET.

When this feature is enabled, the transfer of contents from the shadow register to the active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL[GLDMODE]). When GLDCTL[GLD] = 1, shadow to active load event selection bits for individual shadowed registers are ignored and global load mode takes effect for the corresponding registers enabled by GLDCFG[REGx].

When GLDCTL[GLD] = 1 and GLDCFG[REGx] = 0, global load mode does not affect the corresponding register (REGx). Shadow to active load event selection bits for individual shadowed registers decide how the transfer of contents from shadow register to active register takes place.

25.4.6.1 Global Load Pulse Pre-Scalar

This feature provides the capability to choose shadow to active transfers to happen once in 'N' occurrences of selected global load pulse (GLDCTL[GLDMODE]). This pre-scale functionality is not available for registers that cannot or are not configured to use the global load mechanism (that is, GLDCTL[GLD] = 0 or GLDCFG[REGx] = 0).

25.4.6.2 One-Shot Load Mode

Note

Using global load in one-shot load mode, global load of registers may get delayed when a write to the GLDCTL2.OSHTLD register occurs within 3 TBCLKs of the global load event

This feature allows users to cause the shadow register to active register transfers to occur once. When GLDCTL2[OSHTLD] = 1 the shadow to active register transfer, for registers that are configured to use the global load mechanism, takes place on the event selected by GLDCTL[GLDMODE].

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Software force loading of contents from shadow register to active register is possible by using GLDCTL2[GFRCLD]. This, along with the one-shot load mode feature discussed above, provides a method to correctly update multiple PWM registers in one or more PWM modules at certain PWM events or, if desired, in the same clock cycle. This is very useful in variable frequency applications and/or multiphase interleaved applications.

25.4.6.3 One-Shot Sync Mode

To enable the one-shot sync mode to generate a SYNCOUT pulse, configure the TBCTL2[OSHTSYNCMODE] bit and set the TBCTL2[OSHTSYNC] bit as shown in Figure 25-14.

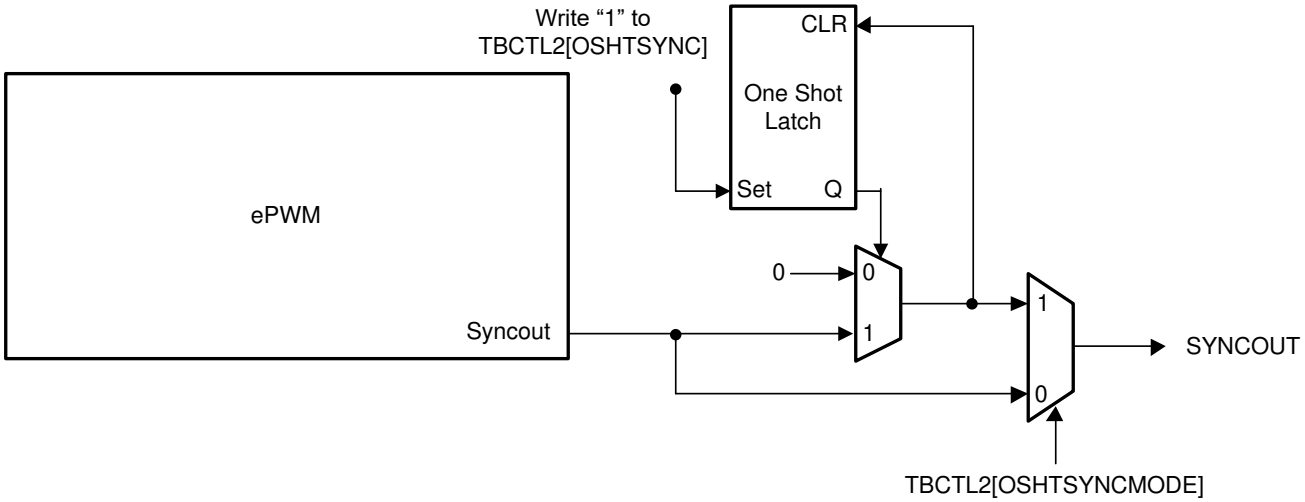


Figure 25-14. One-Shot Sync Mode

25.5 Counter-Compare (CC) Submodule

Figure 25-15 illustrates the counter-compare submodule within the ePWM.

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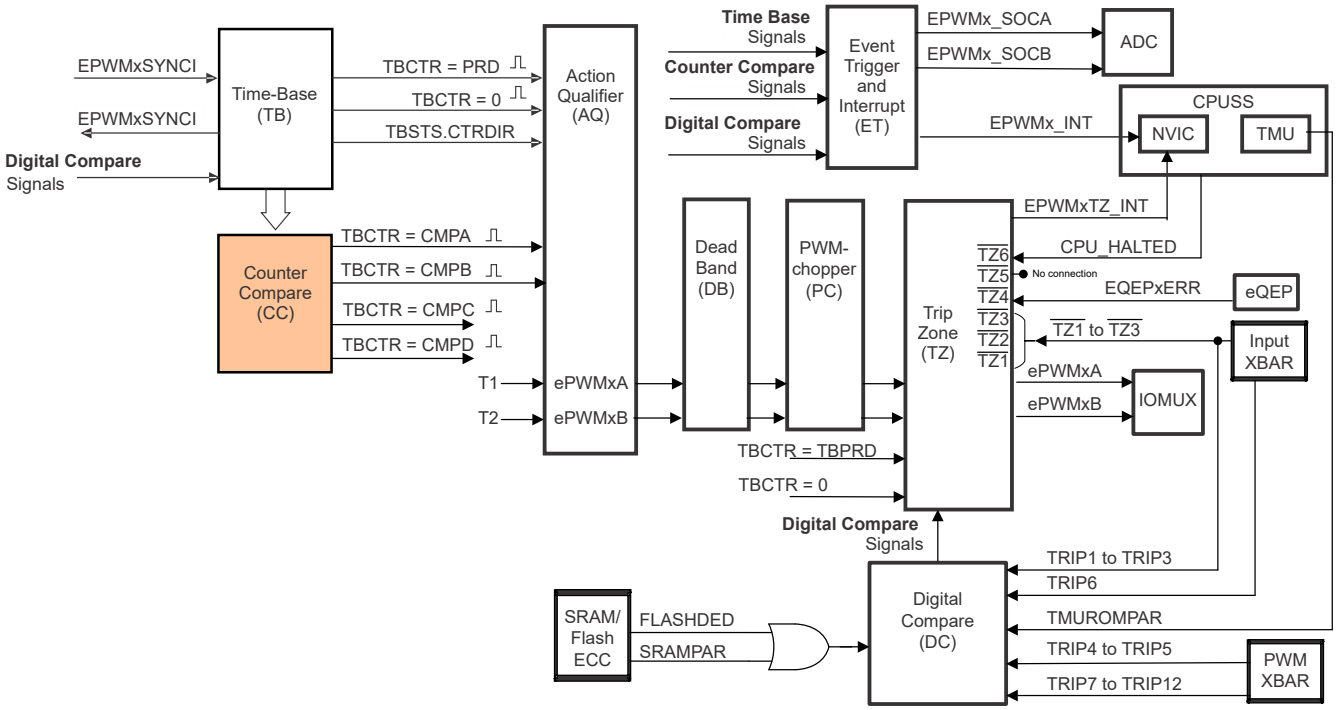


Figure 25-15. Counter-Compare Submodule

25.5.1 Purpose of the Counter-Compare Submodule

The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (CMPA), counter-compare B (CMPB), counter-compare C (CMPC), and counter-compare D (CMPD) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event.

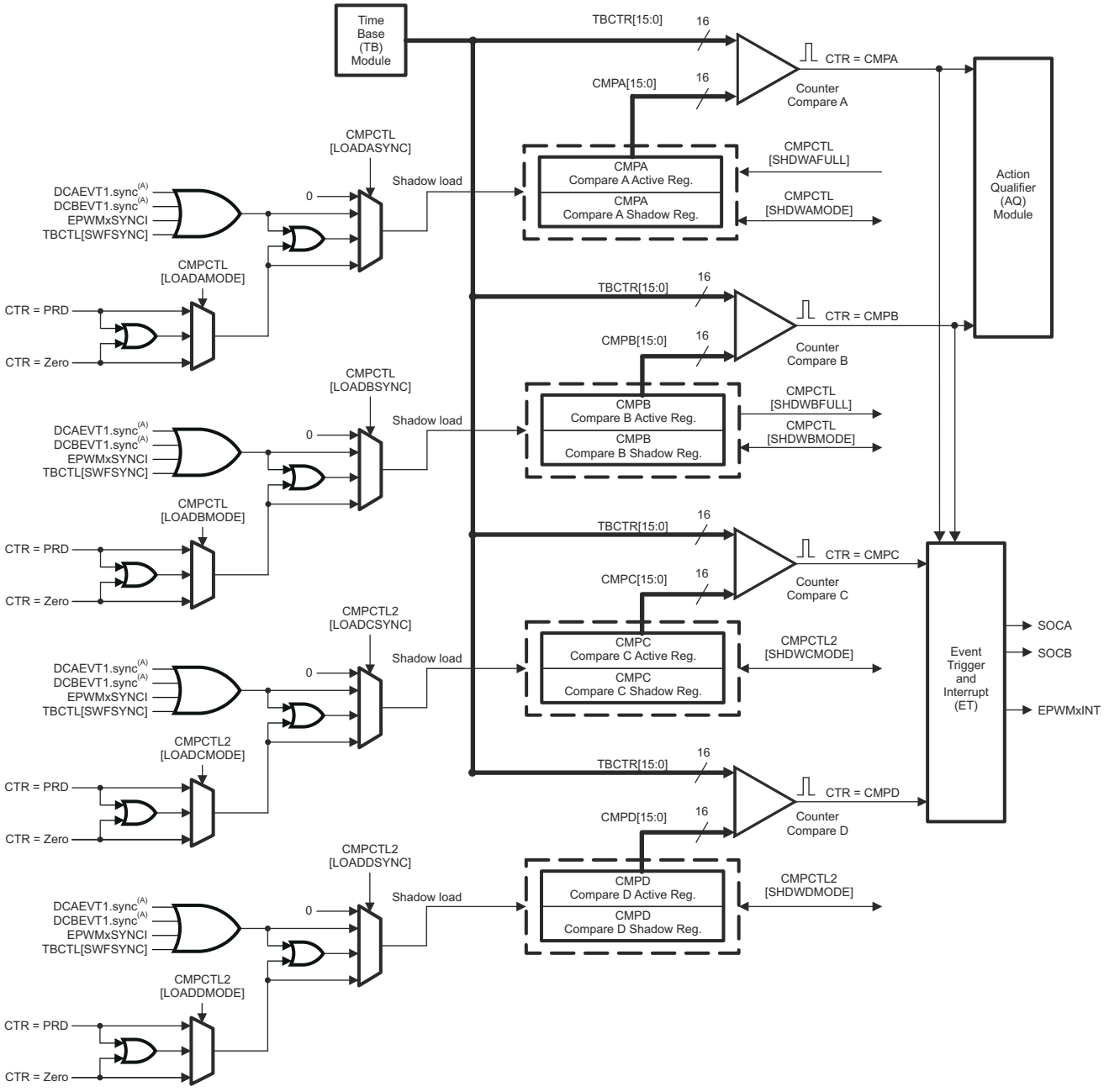
The counter-compare:

- Generates events based on programmable time stamps using the CMPA, CMPB, CMPC, and CMPD registers:
  - CTR = CMPA: Time-base counter equals counter-compare A register (TBCTR = CMPA)
  - CTR = CMPB: Time-base counter equals counter-compare B register (TBCTR = CMPB)
  - CTR = CMPC: Time-base counter equals counter-compare C register (TBCTR = CMPC)
  - CTR = CMPD: Time-base counter equals counter-compare D register (TBCTR = CMPD)
- Controls the PWM duty cycle, if the action-qualifier submodule is configured appropriately using counter-compare A (CMPA) and counter-compare B (CMPB)
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle

25.5.2 Controlling and Monitoring the Counter-Compare Submodule

The counter-compare submodule operation is shown in Figure 25-16.

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Note

These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs (for example, CMPSSx and $\overline{TZ}$ signals).

Figure 25-16. Detailed View of the Counter-Compare Submodule

25.5.3 Operational Highlights for the Counter-Compare Submodule

The counter-compare submodule is responsible for generating events that can be used in the action-qualifier and event-trigger submodules. There are four independent compare events:

1. CTR = CMPA: Time-base counter equal to counter-compare A register (TBCTR = CMPA).
2. CTR = CMPB: Time-base counter equal to counter-compare B register (TBCTR = CMPB).

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3. CTR = CMPC: Time-base counter equal to counter-compare C register (TBCTR = CMPC). This event can be used to generate an event in the event trigger submodule only.
4. CTR = CMPD: Time-base counter equal to counter-compare D register (TBCTR = CMPD). This event can be used to generate an event in the event trigger submodule only

For up-count or down-count mode, each event occurs only once per cycle. For up-down count mode, each event occurs twice per cycle if the compare value is between 0x00-TBPRD; and once per cycle if the compare value is equal to 0x00 or equal to TBPRD. These events are applies to the action-qualifier submodule where the events are qualified by the counter direction and converted into actions if enabled. Refer to Section 25.6.1 for more details.

The counter-compare registers CMPA and CMPB each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occur at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. The memory address of the active register and the shadow register is identical. The register that is written to or read from is determined by the CMPCTL[SHDWAMODE] and CMPCTL[SHDWBMODE] bits. These bits enable and disable the CMPC shadow register and CMPD shadow register, respectively. The behavior of the two load modes is:

Shadow Mode:

The shadow mode for the CMPA is enabled by clearing the CMPCTL[SHDWAMODE] bit and the shadow register for CMPB is enabled by clearing the CMPCTL[SHDWBMODE] bit. Shadow mode is enabled by default for both CMPA and CMPB.

If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the CMPCTL[LOADAMODE], CMPCTL[LOADBMODE], CMPCTL[LOADASYNC], and CMPCTL[LOADBSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNCI or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LOADAMODE/LOADBMODE

Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.

Note

Refer to Section 25.6.5 for valid configurations of CMPA/CMPB and LOADAMODE/LOADBMODE.

Immediate Load Mode:

If the immediate load mode is selected (that is, CMPCTL[SHDWAMODE] = 1 or CMPCTL[SHDWBMODE] = 1), then a read from or a write to the register goes directly to the active register.

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Additional Comparators

The counter-compare submodule on ePWMs type 2 and later are responsible for generating two additional independent compare events based on two compare registers, which is fed to Event Trigger submodule:

1. CTR = CMPC: Time-base counter equal to counter-compare C register (TBCTR = CMPC).
2. CTR = CMPD: Time-base counter equal to counter-compare D register (TBCTR = CMPD).

The counter-compare registers CMPC and CMPD each have an associated shadow register. By default this register is shadowed. The memory address of the active register and the shadow register is identical. The value in the active CMPC and CMPD register is compared to the time-base counter (TBCTR). When the values are equal, the counter compare module generates a “time-base counter equal to counter compare C or counter compare D ” event respectively. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] and CMPCTL2[SHDWDMODE] bit. These bits enable and disable the CMPC shadow register and CMPD shadow register respectively. The behavior of the two load modes is described below:

Shadow Mode:

The shadow mode for the CMPC is enabled by clearing the CMPCTL2[SHDWCMODE] bit and the shadow register for CMPD is enabled by clearing the CMPCTL2[SHDWDMODE] bit. Shadow mode is enabled by default for both CMPC and CMPD.

If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the CMPCTL2[LOADCMODE], CMPCTL2[LOADDMODE], CMPCTL2[LOADCSYNC], and CMPCTL2[LOADDSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNCI or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LOADCMODE/LOADDMODE

Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.

Immediate Load Mode:

If the immediate load mode is selected (that is, CMPCTL2[SHDWCMODE] = 1 or CMPCTL2[SHDWDMODE] = 1), then a read from or a write to the register goes directly to the active register.

Global Load Support

The global load control mechanism can also be used for all counter-compare registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When the global load mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The global load control mechanism is explained in Section 25.4.6 .

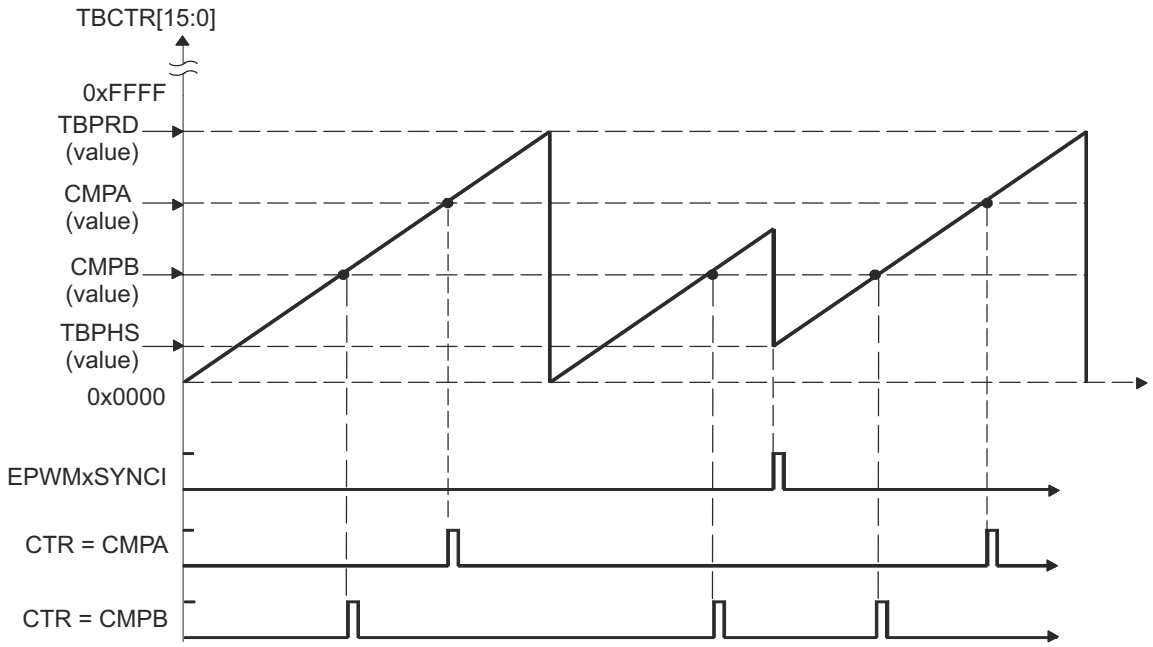
25.5.4 Count Mode Timing Waveforms

The counter-compare module can generate compare events in all three count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Down-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

To best illustrate the operation of the first three modes, the timing diagrams in Figure 25-17 through Figure 25-20 show when events are generated and how the EPWMxSYNCI signal interacts.

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Note

An EPWMxSYNCI external synchronization event can cause a discontinuity in the TBCTR count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

Figure 25-17. Counter-Compare Event Waveforms in Up-Count Mode

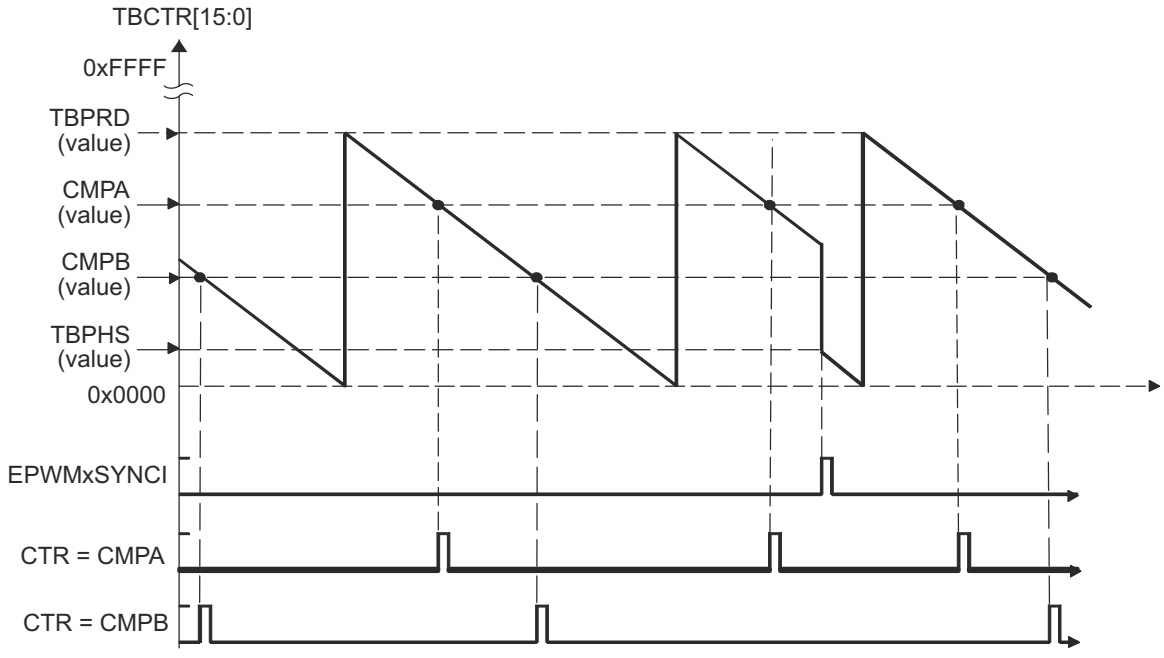


Figure 25-18. Counter-Compare Events in Down-Count Mode

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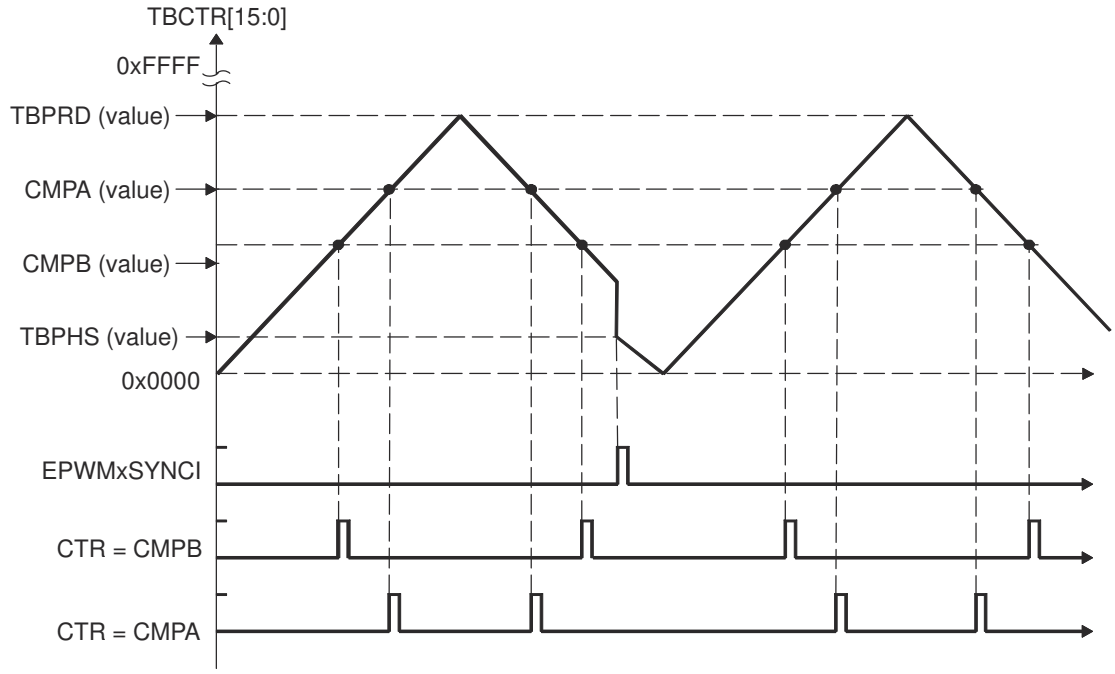


Figure 25-19. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

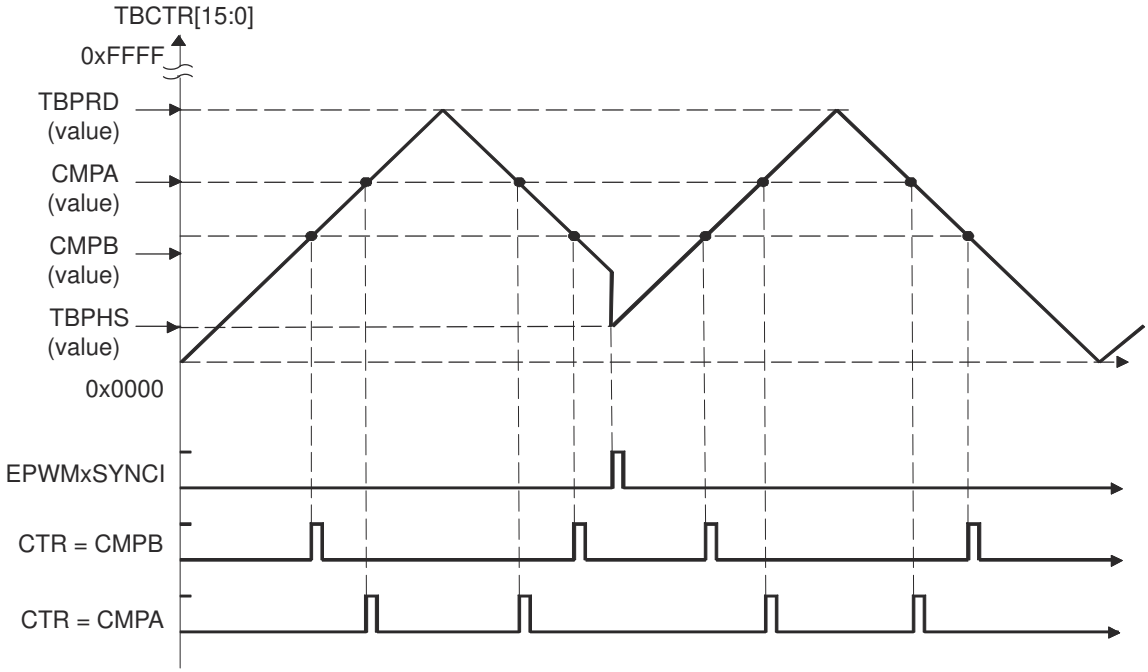


Figure 25-20. Counter-Compare Events In Up-Down-Count Mode, TBCTL[PHSDIR = 1] Count Up On Synchronization Event

25.6 Action-Qualifier (AQ) Submodule

The action-qualifier submodule has the most important role in waveform construction and PWM generation. The action-qualifier submodule decides which events are converted into various action types, thereby, producing the

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required switched waveforms at the EPWMxA and EPWMxB outputs. Figure 25-21 illustrates the action-qualifier submodule within the ePWM.

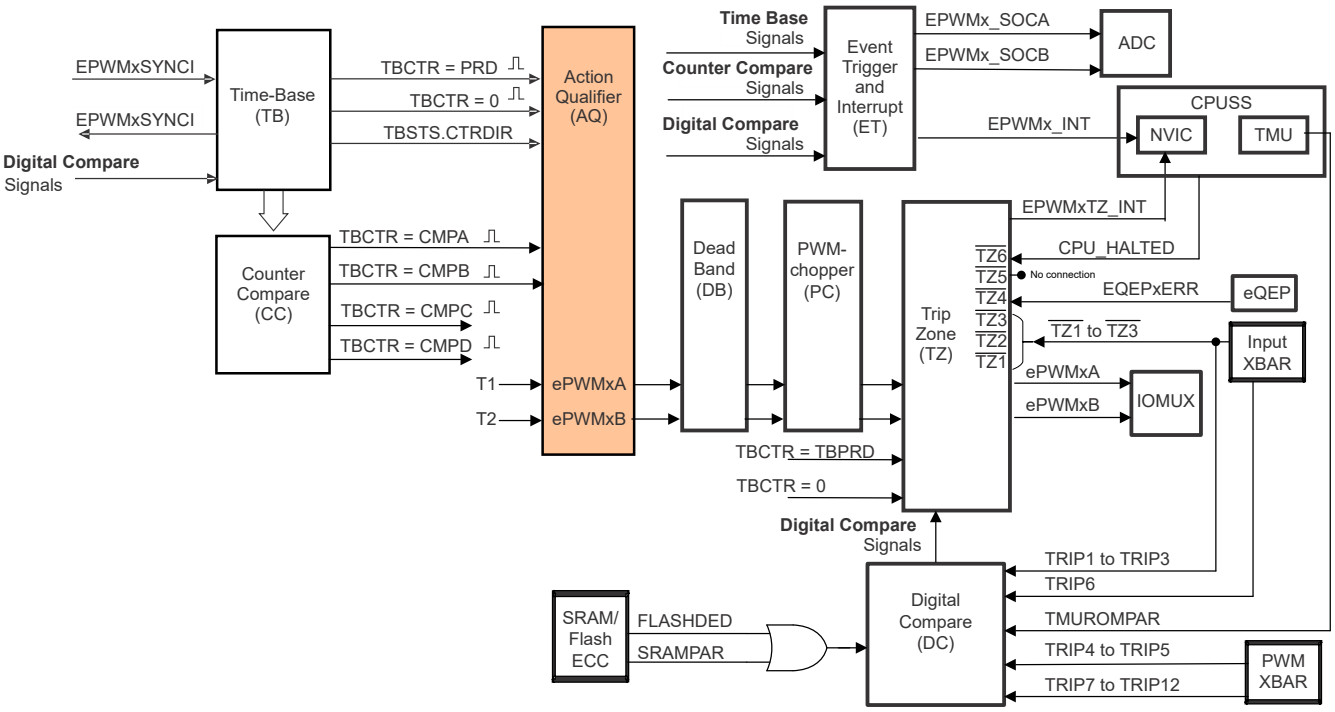


Figure 25-21. Action-Qualifier Submodule

25.6.1 Purpose of the Action-Qualifier Submodule

The action-qualifier submodule is responsible for the following:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
  - CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
  - CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
  - CTR = CMPA: Time-base counter equal to the counter-compare A register (TBCTR = CMPA)
  - CTR = CMPB: Time-base counter equal to the counter-compare B register (TBCTR = CMPB)
- T1, T2 events: Trigger events based on comparator, trip or syncin events
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when the time-base counter is decreasing

25.6.2 Action-Qualifier Submodule Control and Status Register Definitions

The action-qualifier submodule operation is shown in Figure 25-22 and monitored by way of the registers in the *ePWM Registers* section.

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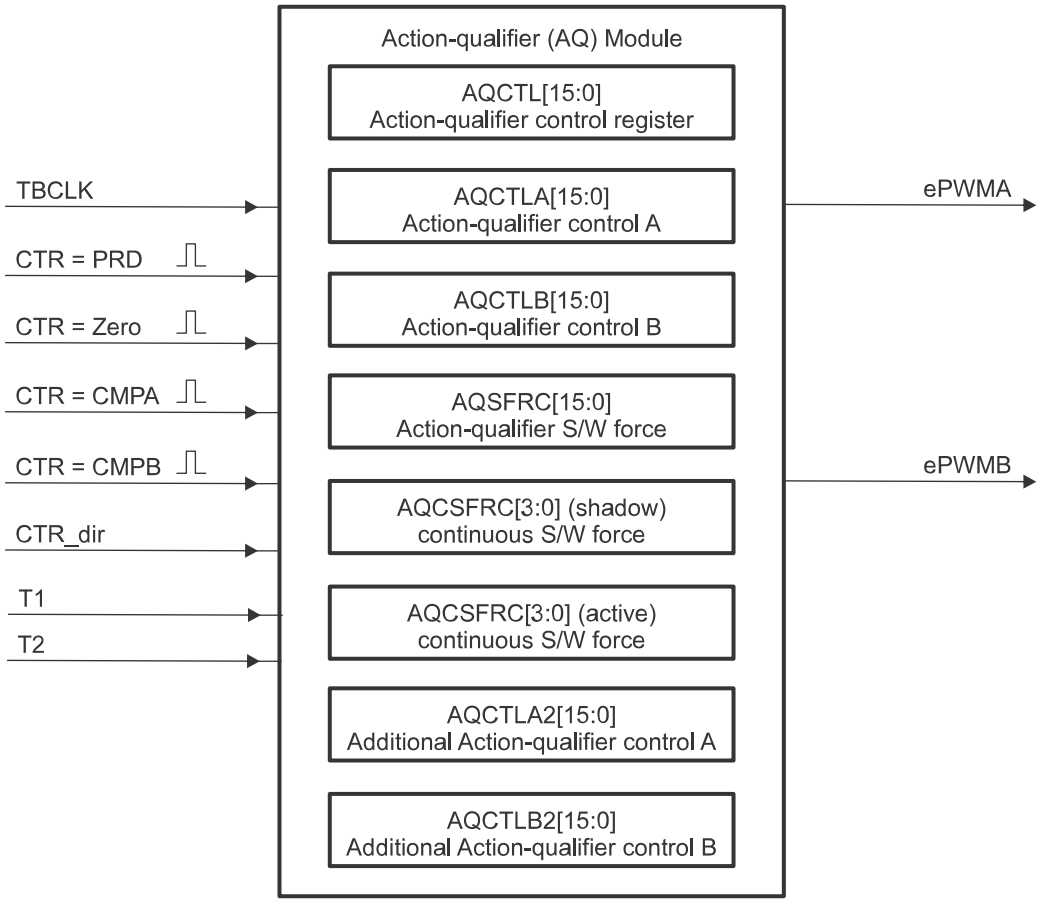


Figure 25-22. Action-Qualifier Submodule Inputs and Outputs

For convenience, the possible input events are summarized again in Table 25-4.

Table 25-4. Action-Qualifier Submodule Possible Input Events

Signal	Description	Registers Compared
CTR = PRD	Time-base counter equal to the period value	TBCTR = TBPRD
CTR = Zero	Time-base counter equal to 0	TBCTR = 0x00
CTR = CMPA	Time-base counter equal to the counter-compare A	TBCTR = CMPA
CTR = CMPB	Time-base counter equal to the counter-compare B	TBCTR = CMPB
T1 event	Based on comparator, trip, or syncin events	None
T2 event	Based on comparator, trip, or syncin events	None
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by the AQSFRC and AQCSFRC registers.

Note

If the CSFA is not used in shadow mode, the RLDCSF bit must be configured to disable shadow mode.

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The action-qualifier submodule controls how the two outputs EPWMxA and EPWMxB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs EPWMxA and EPWMxB are:

- **Set High:** Set output EPWMxA or EPWMxB to a high level.
- **Clear Low:** Set output EPWMxA or EPWMxB to a low level.
- **Toggle:** If EPWMxA or EPWMxB is currently pulled high, then pull the output low. If EPWMxA or EPWMxB is currently pulled low, then pull the output high.
- **Do Nothing:** Keep outputs EPWMxA and EPWMxB at same level as currently set. Although the "Do Nothing" option prevents an event from causing an action on the EPWMxA and EPWMxB outputs, this event can still trigger interrupts and ADC start of conversion. See the description in Section 25.10 for details.

Actions are specified independently for either output (EPWMxA or EPWMxB). Any or all events can be configured to generate actions on a given output. For example, both CTR = CMPA and CTR = CMPB can operate on output EPWMxA. All qualifier actions are configured using the control registers found in the *ePWM Registers* section.

For clarity, the illustrations in this chapter use a set of symbolic actions. These symbols are summarized in Figure 25-23. Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and the time positions are programmed by way of the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"(the default at reset).

S/W force	TB Counter equals				Trigger Events		Actions
	Zero	Comp A	Comp B	Period	T1	T2	
SW	Z	CA	CB	P	T1	T2	Do Nothing
SW	Z	CA	CB	P	T1	T2	Clear Lo
SW	Z	CA	CB	P	T1	T2	Set Hi
SW	Z	CA	CB	P	T1	T2	Toggle

Figure 25-23. Possible Action-Qualifier Actions for EPWMxA and EPWMxB Outputs

The Action Qualifier Trigger Event Source Selection register (AQTSRCSEL) is used to select the source for T1 and T2 events. T1/T2 selection and configuration of a trip/digital-compare event in Action Qualifier submodule is independent of the configuration of that event in the Trip-Zone submodule. A particular trip event can or cannot be configured to cause trip action in the Trip Zone submodule, but the same event can be used by the Action Qualifier to generate T1/T2 for controlling PWM generation.

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25.6.3 Action-Qualifier Event Priority

It is possible for the ePWM action qualifier to receive more than one event at the same time. In this case, events are assigned a priority by the hardware. The general rule is events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down count mode are shown in Table 25-5. A priority level of 1 is the highest priority and level 10 is the lowest. The priority changes slightly depending on the direction of TBCTR.

Table 25-5. Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event If TBCTR is Incrementing TBCTR = Zero up to TBCTR = TBPRD	Event If TBCTR is Decrementing TBCTR = TBPRD down to TBCTR = 1
1 (Highest)	Software forced event	Software forced event
2	T1 on up-count (T1U)	T1 on down-count (T1D)
3	T2 on up-count (T2U)	T2 on down-count (T2D)
4	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
5	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
6 (Lowest)	Counter equals zero	Counter equals period (TBPRD)

Table 25-6 shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up; therefore, down-count events never are taken.

Table 25-6. Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	T1 on up-count (T1U)
4	T2 on up-count (T2U)
5	Counter equal to CMPB on up-count (CBU)
6	Counter equal to CMPA on up-count (CAU)
7 (Lowest)	Counter equal to Zero

Table 25-7 shows the action-qualifier priority for down-count mode. In this case, the counter direction is always defined as down; therefore, up-count events never are taken.

Table 25-7. Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	T1 on down-count (T1D)
4	T2 on down-count (T2D)
5	Counter equal to CMPB on down-count (CBD)
6	Counter equal to CMPA on down-count (CAD)
7 (Lowest)	Counter equal to period (TBPRD)

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It is possible to set the compare value greater than the period. In this case, the action takes place as shown in Table 25-8.

Table 25-8. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAU/CBU	Compare on Down-Count Event CAD/CBD
Up-Count Mode	If CMPA/CMPB ≤ TBPRD period, then the event occurs on a compare match (TBCTR=CMPA or CMPB).	Never occurs.
	If CMPA/CMPB > TBPRD, then the event does not occur.	
Down-Count Mode	Never occurs.	If CMPA/CMPB < TBPRD, the event occurs on a compare match (TBCTR=CMPA or CMPB).
		If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCTR=TBPRD).
Up-Down Count Mode	If CMPA/CMPB < TBPRD and the counter is incrementing, the event occurs on a compare match (TBCTR=CMPA or CMPB).	If CMPA/CMPB < TBPRD and the counter is decrementing, the event occurs on a compare match (TBCTR=CMPA or CMPB).
	If CMPA/CMPB is ≥ TBPRD, the event occurs on a period match (TBCTR = TBPRD).	If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCTR=TBPRD).

25.6.4 AQCTLA and AQCTLB Shadow Mode Operations

To enable Action Qualifier mode changes which must occur at the end of a period even when the phase changes, use the shadowing feature of the AQCTLA and AQCTLB registers. Additionally, shadow to active load on SYNC of these registers is supported as well. Shadowing of this register is enabled and disabled by the AQCTL[SHDWAQAMODE] and AQCTL[SHDWAQBMODE] bits. These bits enable and disable the AQCTLA shadow register and AQCTLB shadow register, respectively. The behavior of the two load modes is:

Shadow Mode:

The shadow mode for the AQCTLA is enabled by setting the AQCTL[SHDWAQAMODE] bit, and the shadow register for AQCTLB is enabled by setting the AQCTL[SHDWAQBMODE] bit. Shadow mode is disabled by default for both AQCTLA and AQCTLB.

If the shadow register is enabled, then the content of the shadow register is transferred to the active register on one of the following events as specified by the AQCTL[LDAQAMODE], AQCTL[LDAQBMODE], AQCTL[LDAQASYNC], and AQCTL[LDAQBSYNC] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero
- SYNC event caused by DCAEVT1 or DCBEVT1 or EPWMxSYNCI or TBCTL[SWFSYNC]
- Both SYNC event or a selection made by LDAQAMODE/LDAQBMODE

Global Load Support

Global load control mechanism can also be used for AQCTLA:AQCTLA2, AQCTLB:AQCTLB2, and AQCSFRC registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When global load mode is selected, the transfer of contents from shadow register to active register for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The global load control mechanism is explained in Section 25.4.6 .

Immediate Load Mode:

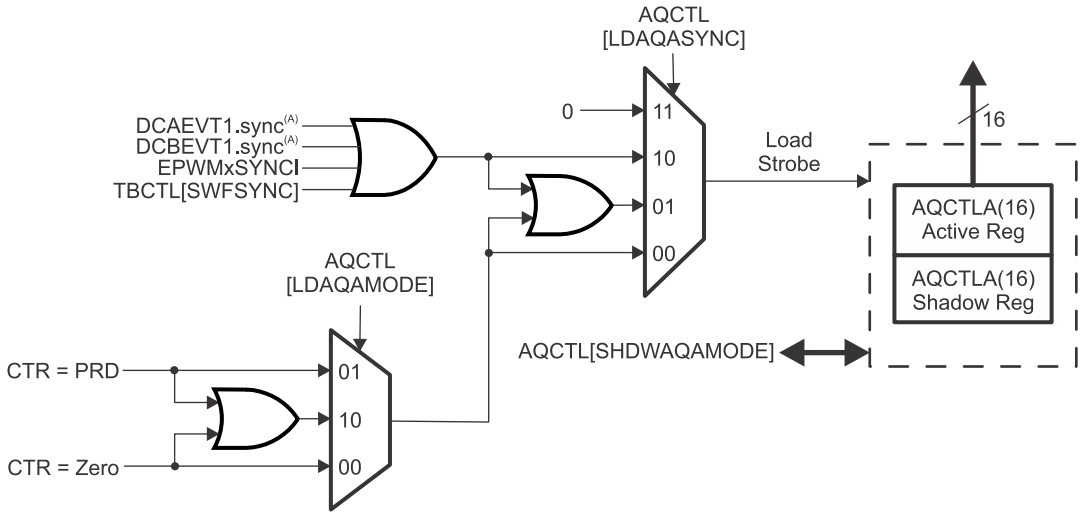
If the immediate load mode is selected (that is, AQCTL[SHDWAQAMODE] = 0 or AQCTL[SHDWAQBMODE] = 0), then a read from or a write to the register goes directly to the active register. See Figure 25-24 and Figure 25-25.

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Note

Shadow to Active Load of Action Qualifier Output A/B Control Register [AQCTLA and AQCTLB] on CMPA = 0 or CMPB = 0 boundary

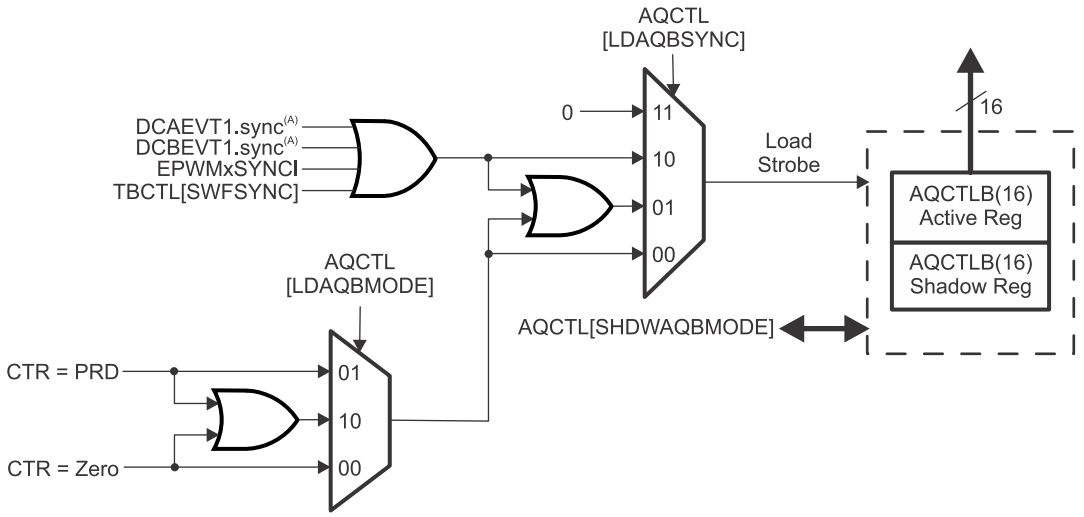
If the Counter-Compare A Register (CMPA) or Counter-Compare B Register (CMPB) is set to a value of 0 and the action qualifier action on AQCTLA and AQCTLB is configured to occur in the same instant as a shadow to active load (that is, CMPA = 0 and AQCTLA shadow to active load on TBCTR = 0 using AQCTL register LDAQAMODE and LDAQAMODE bits), then both events enter contention. It is recommended to use a Non-Zero Counter-Compare when using Shadow to Active Load of Action Qualifier Output A/B Control Register on TBCTR = 0 boundary.



Note

These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs (for example, CMPSSx and $\overline{TZ}$ signals).

Figure 25-24. AQCTL[SHDWAQAMODE]



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Note

These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs (for example, CMPSSx and $\overline{TZ}$ signals).

Figure 25-25. AQCTL[SHDWAQBMODE]

25.6.5 Configuration Requirements for Common Waveforms

Note

The waveforms in this chapter show the behavior of the ePWMs for a static compare register value. In a running system, the active compare registers (CMPA and CMPB) are typically updated from the respective shadow registers once every period. Specify when the update takes place: either when the time-base counter reaches zero or when the time-base counter reaches the period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down count mode to generate a symmetric PWM:

- If loading CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1.
- If loading CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1.

  This means there is always a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down count mode to generate an asymmetric PWM:

- To achieve 50%-0% asymmetric PWM use the following configuration: Load CMPA/CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50%-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM, you **must** load CMPA/CMPB on TBPRD. When CMPA/CMPB is not loaded on TBCTR=PRD, boundary conditions can occur depending on the timing of the write and the value written to CMPA/CMPB. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD+1 to achieve 0-100% PWM duty.

When using up-count mode to generate an asymmetric PWM with deadband enabled:

- To achieve 0%-100% PWM use the following configuration: When the CMPA value is too close to 0 or PRD such that the following conditions are met (CMPX < Deadband) or (CMPX > PRD – Deadband), the actions specified by the AQCTL register for CMPX do not take effect. To avoid this, the AQCTL settings must be altered under these conditions only to generate either high or low pulses for both CAU or CAD events (both set or both clear). Make sure that this software update is occurring synchronous to the PWM carrier cycle, and shadow mode is enabled.

When using up-down count mode to generate an asymmetric PWM with deadband enabled:

- To achieve 0%-100% PWM use the following configuration: When the CMPA value is too close to 0 or PRD such that the following conditions are met (CMPX < Deadband/2) or (CMPX > PRD – (Deadband)/2), the actions specified by the AQCTL register for CMPX do not take effect. To avoid this, the AQCTL settings must be altered under these conditions only to generate either high or low pulses for both CAU or CAD events (both set or both clear). Make sure that this software update is occurring synchronous to the PWM carrier cycle, and shadow mode is enabled.

Figure 25-26 shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCTR. In this mode, 0%-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, CMPA is used to make the comparison. When the counter is incrementing, the CMPA match pulls the PWM output high. Likewise when the counter is

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decrementing, the compare match pulls the PWM signal low. When CMPA = 0, the PWM signal is high for the entire period giving a 100% duty waveform. When CMPA = TBPRD, the PWM signal is low achieving 0% duty.

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When using this configuration in practice, if loading CMPA/CMPB on zero, then use CMPA/CMPB values greater than or equal to 1. If loading CMPA/CMPB on period, then use CMPA/CMPB values less than or equal to TBPRD-1. This means there is always a pulse of at least one TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

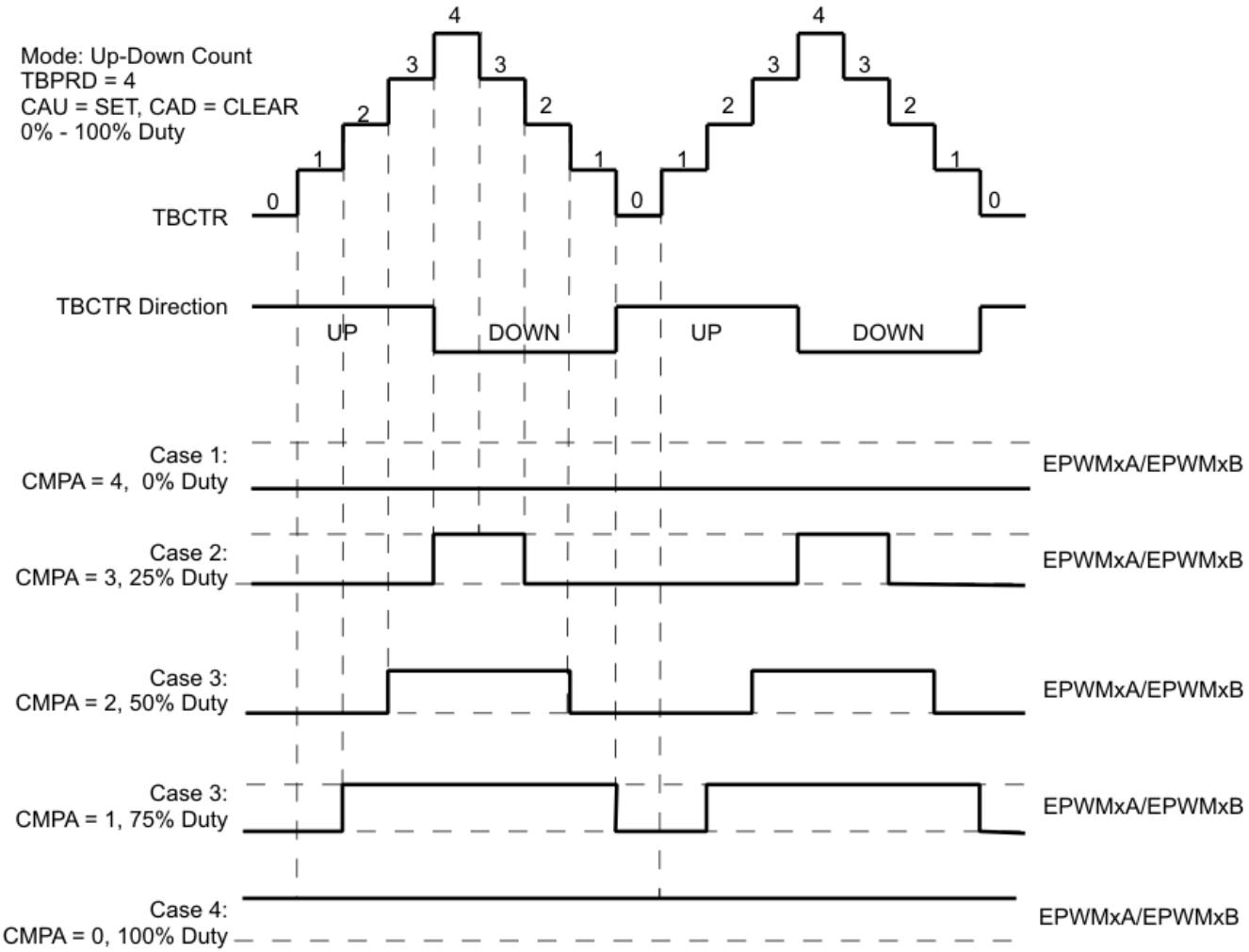
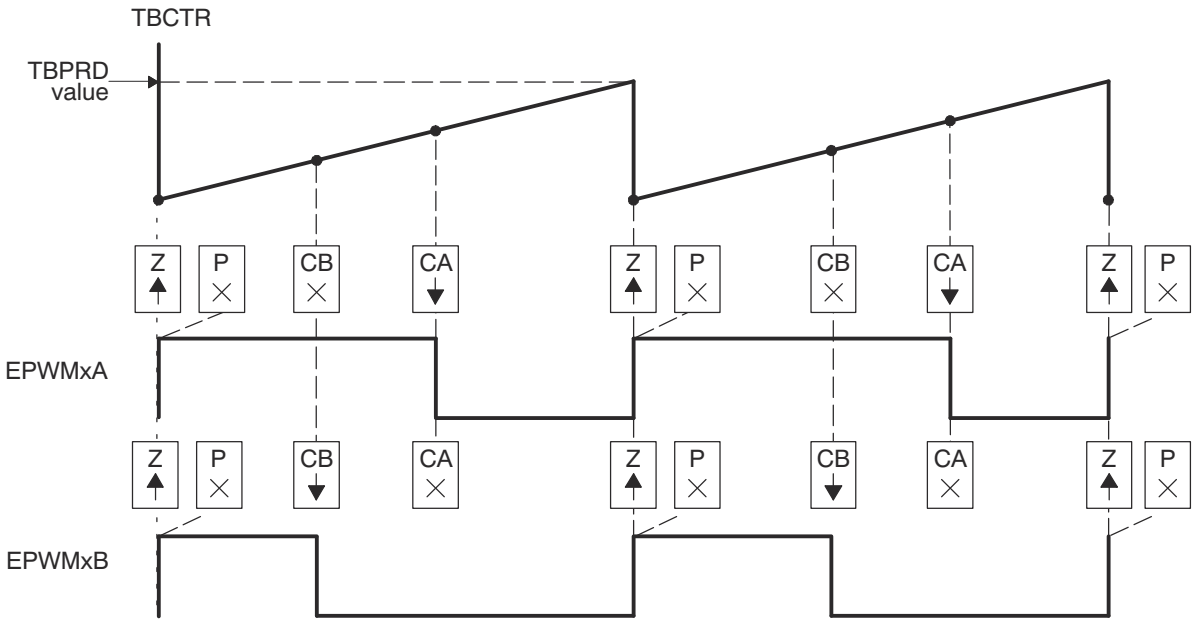


Figure 25-26. Up-Down Count Mode Symmetrical Waveform

The PWM waveforms in Figure 25-27 through Figure 25-32 show some common action-qualifier configurations. Some conventions used in the figures and examples are as follows:

- TBPRD, CMPA, and CMPB refer to the value written in the respective registers. The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either CMPA or CMPB.
- EPWMxA and EPWMxB refer to the output signals from ePWMx
- Up-Down means count-up-and count-down mode, Up means up-count mode and Down means down-count mode
- Sym = Symmetric, Asym = Asymmetric

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Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active high (that is, high time duty proportional to CMPA).

Note

Duty modulation for EPWMxB is set by CMPB and is active high (that is, high time duty proportional to CMPB).

Note

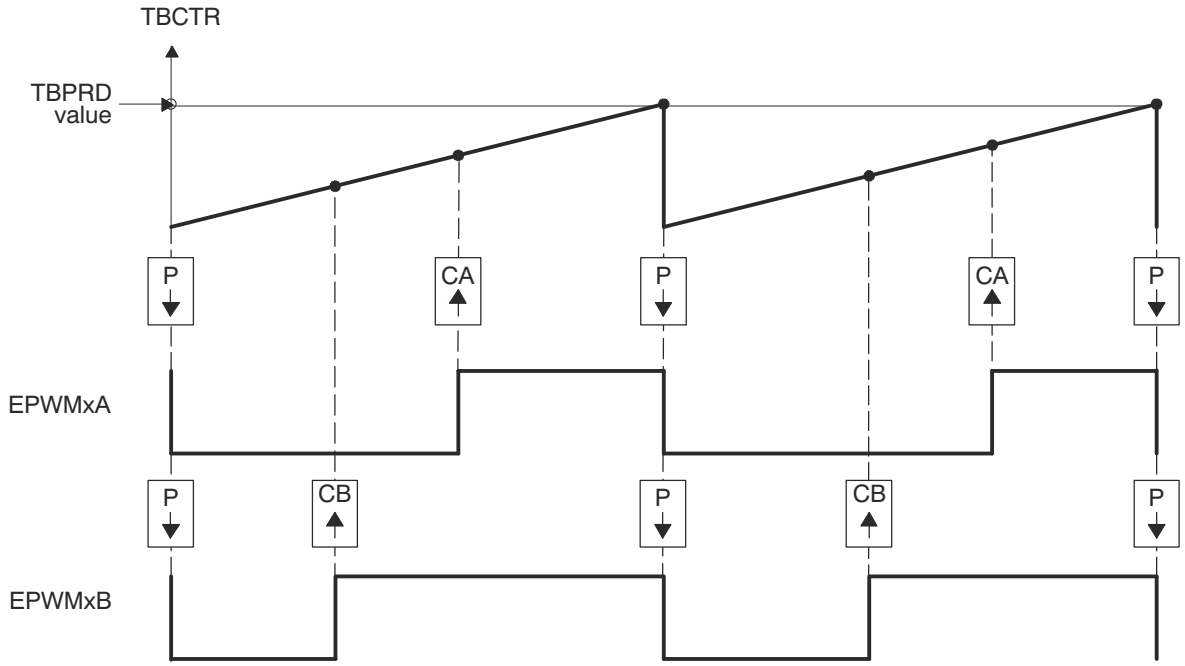
The "Do Nothing" actions (X) are shown for completeness, but are not shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCTR wraps from period to 0000.

Figure 25-27. Up, Single Edge Asymmetric Waveform, with Independent Modulation on EPWMxA and EPWMxB—Active High

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Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

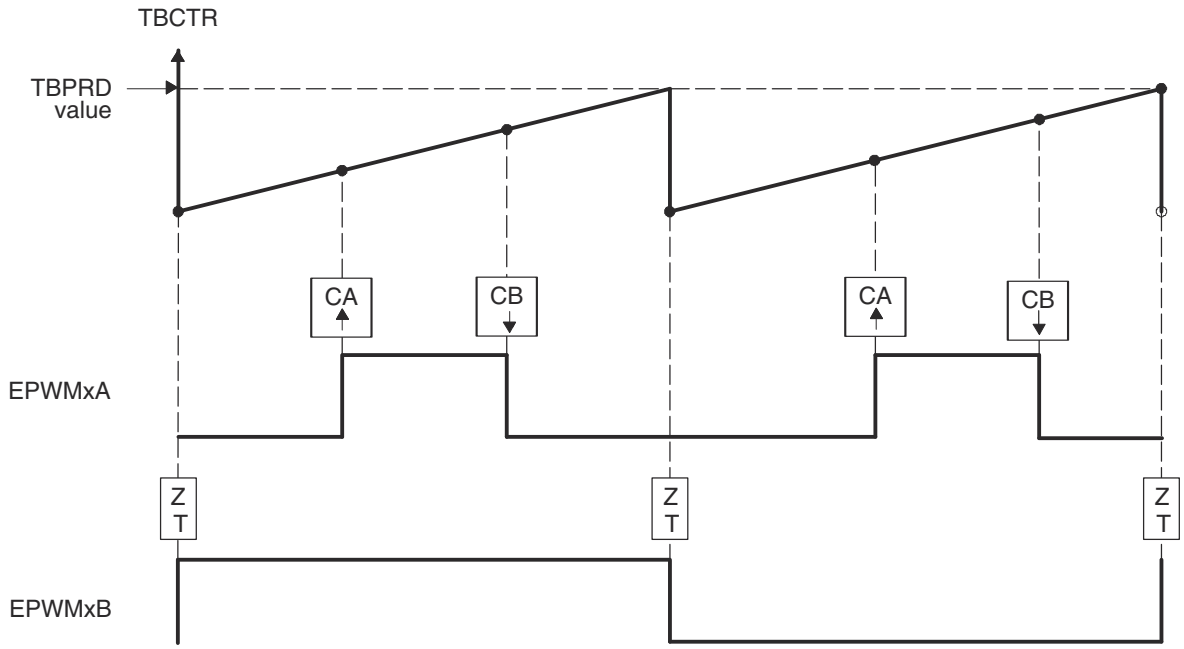
Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCTR wraps from period to 0000.

Figure 25-28. Up, Single Edge Asymmetric Waveform with Independent Modulation on EPWMxA and EPWMxB—Active Low

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Note

PWM frequency = $1/((TBPRD + 1) \times T_{TBCLK})$

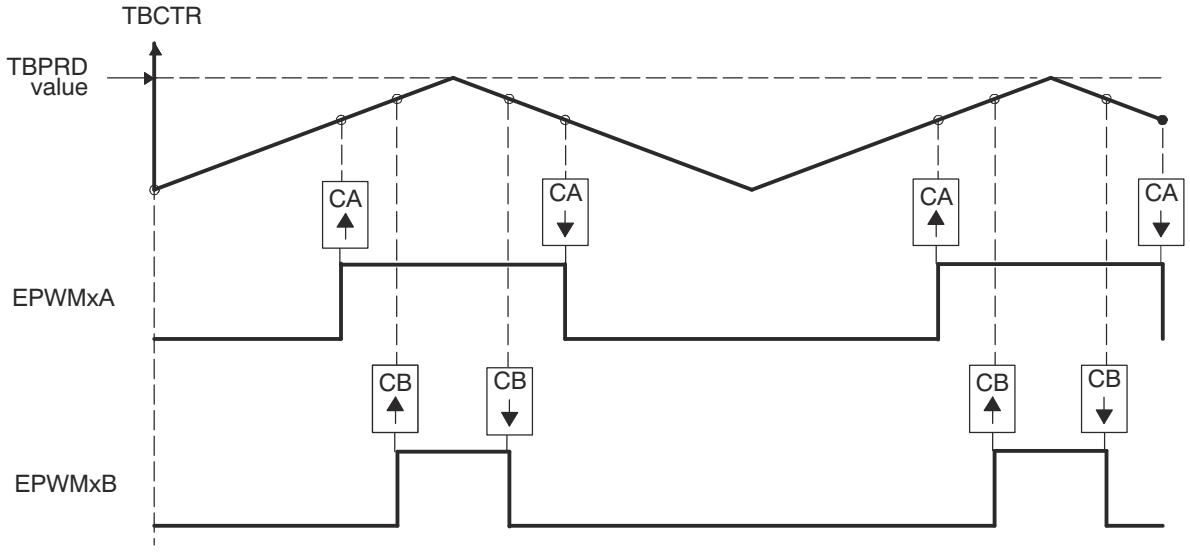
Note

Pulse can be placed anywhere within the PWM cycle (0000 - TBPRD)

Note

High time duty proportional to (CMPB - CMPA)

Figure 25-29. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on EPWMxA



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Note

PWM period = 2 x TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low (that is, the low time duty is proportional to CMPA).

Note

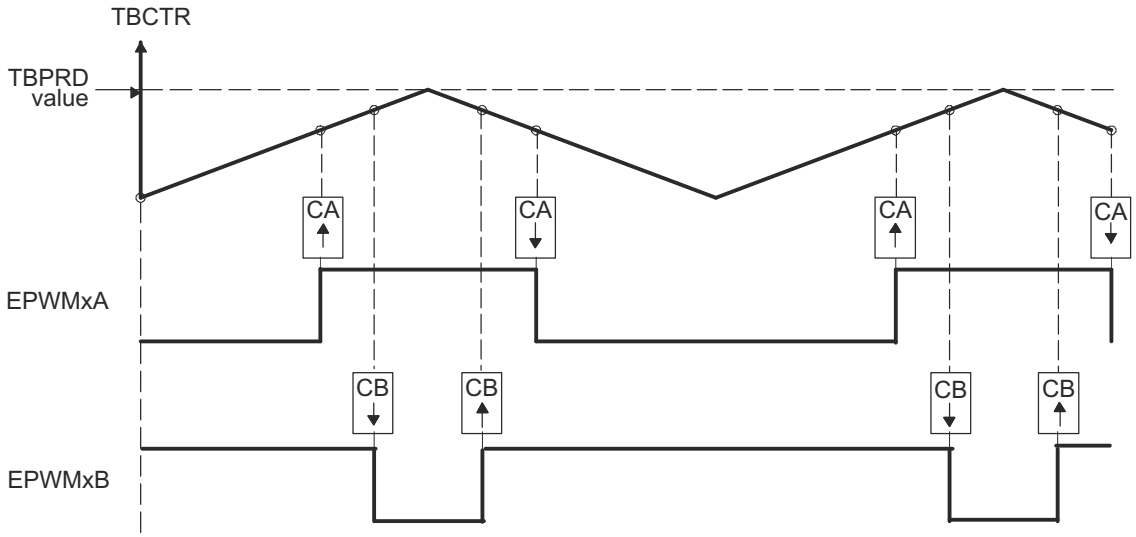
Duty modulation for EPWMxB is set by CMPB and is active low (that is, the low time duty is proportional to CMPB).

Note

Outputs EPWMxA and EPWMxB can drive independent power switches.

Figure 25-30. Up-Down Count, Dual-Edge Symmetric Waveform, with Independent Modulation on EPWMxA and EPWMxB — Active Low

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Note

PWM period = 2 × TBPRD × T_{TBCLK}

Note

Duty modulation for EPWMxA is set by CMPA, and is active low, that is, low time duty proportional to CMPA.

Note

Duty modulation for EPWMxB is set by CMPB and is active high, that is, high time duty proportional to CMPB.

Note

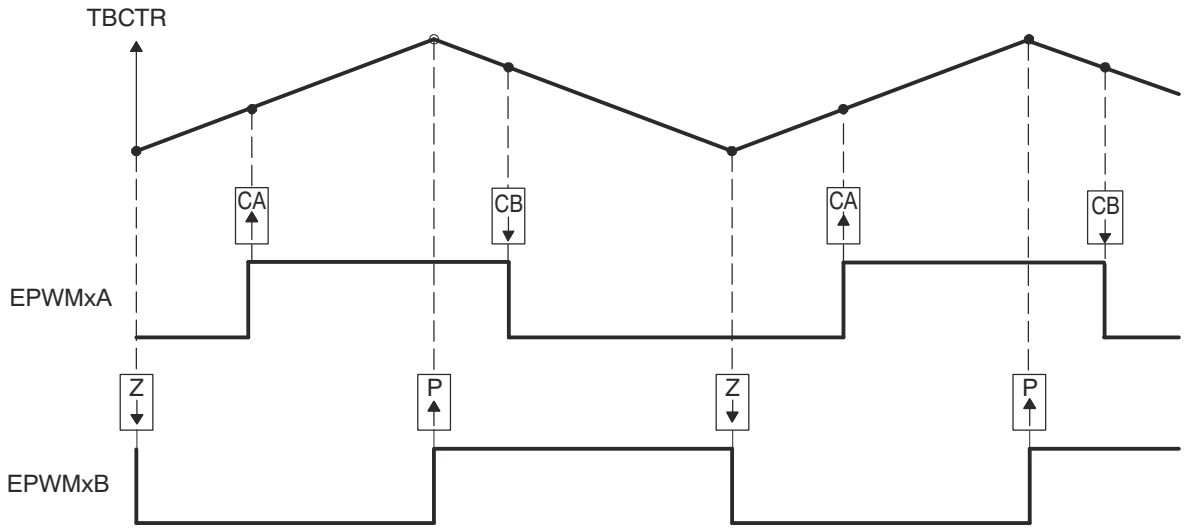
Outputs EPWMx can drive upper/lower (complementary) power switches.

Note

Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 25-31. Up-Down Count, Dual-Edge Symmetric Waveform, with Independent Modulation on EPWMxA and EPWMxB — Complementary

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Note

PWM period = 2 × TBPRD × TBCLK

Note

Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.

Note

Duty modulation for EPWMxA is set by CMPA and CMPB.

Note

Low time duty for EPWMxA is proportional to (CMPA + CMPB).

Note

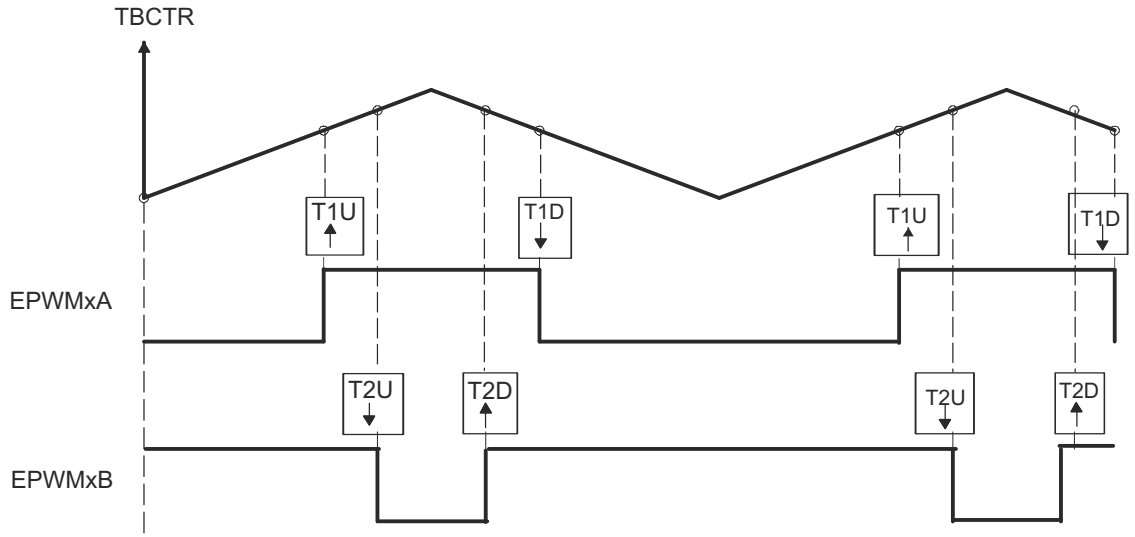
To change this example to active high, CMPA and CMPB actions need to be inverted (that is, Clear on CMPA, Set on CMPB).

Note

Duty modulation for EPWMxB is fixed at 50% (utilizes spare action resources for EPWMxB).

Figure 25-32. Up-Down Count, Dual-Edge Asymmetric Waveform, with Independent Modulation on EPWMxA—Active Low

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Note

PWM period = 2 × TBPRD × TTBCLK

Note

Independent T1 event actions when counter is counting up and when the counter is counting down are used to generate EPWMxA output.

Note

Independent T2 event actions when counter is counting up and when the counter is counting down are used to generate EPWMxB output.

Note

TZ1 is selected as the source for T1.

Note

TZ2 is selected as the source for T2.

Figure 25-33. Up-Down Count, PWM Waveform Generation Utilizing T1 and T2 Events

25.7 Dead-Band Generator (DB) Submodule

Figure 25-34 illustrates the dead-band submodule within the ePWM.

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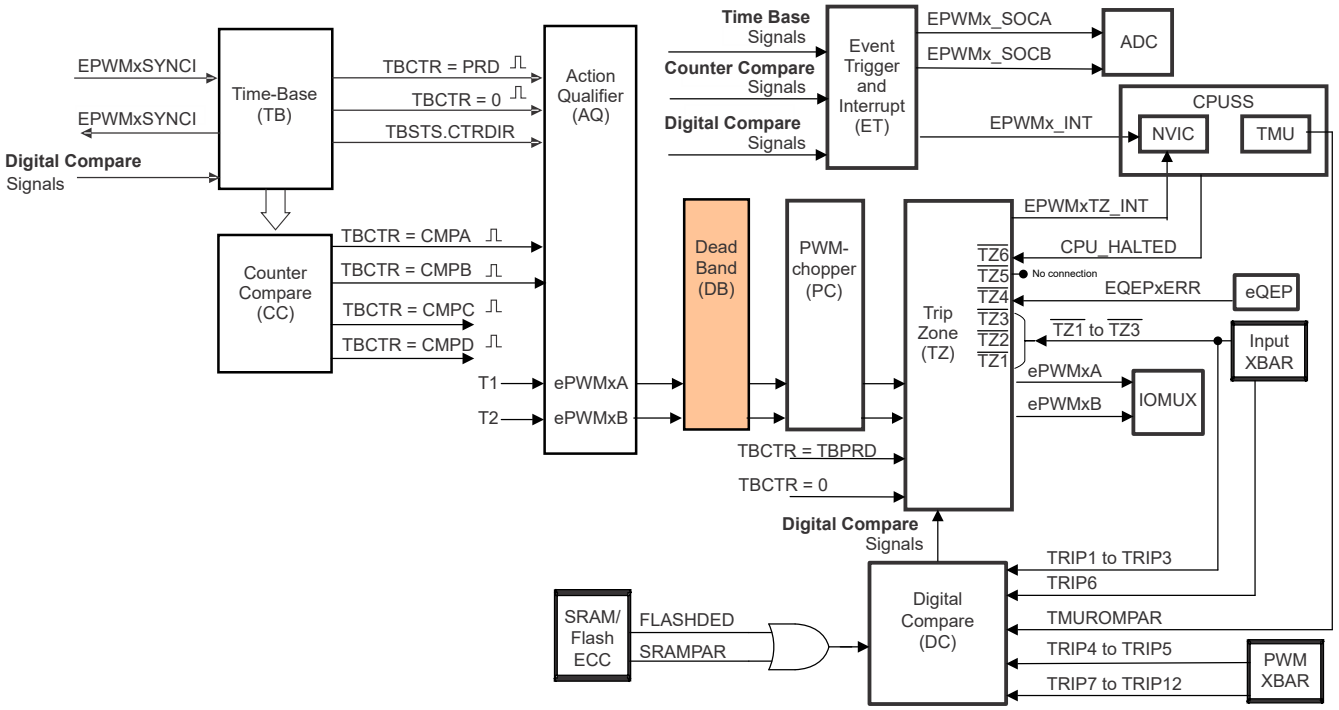


Figure 25-34. Dead-Band Submodule

25.7.1 Purpose of the Dead-Band Submodule

The action-qualifier (AQ) module section discussed how the AQ module can generate the required dead band by having full control over edge placement using both the CMPA and CMPB resources of the ePWM module. However, if the more classical edge delay-based dead band with polarity control is required, then the dead-band submodule described here must be used.

The key functions of the dead-band module are:

- Generating appropriate signal pairs (EPWMxA and EPWMxB) with dead-band relationship from a single EPWMxA input
- Programming signal pairs for:
  - Active high (AH)
  - Active low (AL)
  - Active high complementary (AHC)
  - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in diagram)

25.7.2 Dead-band Submodule Additional Operating Modes

High-resolution deadband RED and FED requires half-cycle clocking mode (DBCTL[HALFCYCLE] = 1). Both RED and FED cannot be applied together to both ePWMxA and ePWMxB. RED and FED together can be applied only to either OutA OR OutB.

Phase shifting B-channel with respect to the A-channel: When PWMxB is derived from PWMxA using the DEDB_MODE bit and by delaying rising edge and falling edge by the phase shift amount. When the duty cycle value on PWMxA is less than this phase shift amount, PWMxA's falling edge has precedence over the delayed rising edge for PWMxB. Make sure the duty cycle value of the current waveform applied to the dead-band module is greater than the required phase shift amount.

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Note

The PWM chopper is not enabled when high-resolution deadband is enabled.

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Shadow Mode:

The shadow mode for the DBRED is enabled by setting the DBCTL[SHDWDBREDMODE] bit and the shadow register for DBFED is enabled by setting the DBCTL [SHDWDBFEDMODE] bit. Shadow mode is disabled by default for both DBRED and DBFED

If the shadow register is enabled, then the content of the shadow register is transferred to the active register on one of the following events as specified by the DBCTL [LOADREDMODE] and DBCTL [LOADFEDMODE] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

The DBCTL register can be shadowed. The shadow mode for DBCTL is enabled by setting the DBCTL2[SHDWDBCTLMODE] bit. If the shadow register is enabled then the content of the shadow register is transferred to the active register on one of the following events as specified by the DBCTL2[LOADDBCTLMODE] register bit:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD)
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

Note

The application software must enable shadow load mode in the DBCTL[SHDWDBREDMODE] and DBCTL[SHDWDBFEDMODE] **before** programming values for the DBRED and DBFED registers. If the shadow register is enabled **after** programming the DBRED and DBFED registers, the DBRED and DBFED registers are loaded with a value of 0.

Global Load Support

Global load control mechanism can also be used for DBRED:DBREDHR, DBFED:DBFEDHR, and DBCTL registers by configuring the appropriate bits in the global load configuration register (GLDCFG). When global load mode is selected the transfer of contents from shadow register to active register, for all registers that have this mode enabled, occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The Global load control mechanism is explained in Section 25.4.6 .

Note

When DBRED/DBFED active is loaded with a new shadow value while DB counters are counting, the new DBRED/DBFED value only affects the NEXT PWMx edge and not the current edge.

A Deadband value of zero cannot be used when the Global Shadow to Active Load is set to occur at CTR=ZERO. Similarly, a Deadband value of PRD cannot be used when the Global Shadow to Active Load is set to occur at CTR=PRD. TBPRDHR cannot be used with Global load. If high-resolution period must be changed in the application, users must write to the individual period registers from an ePWM ISR (The ISR must be synchronous with the PWM switching period), where the Global Load One-Shot bit is also written to.

25.7.3 Operational Highlights for the Dead-Band Submodule

The configuration options for the dead-band submodule are shown in Figure 25-35.

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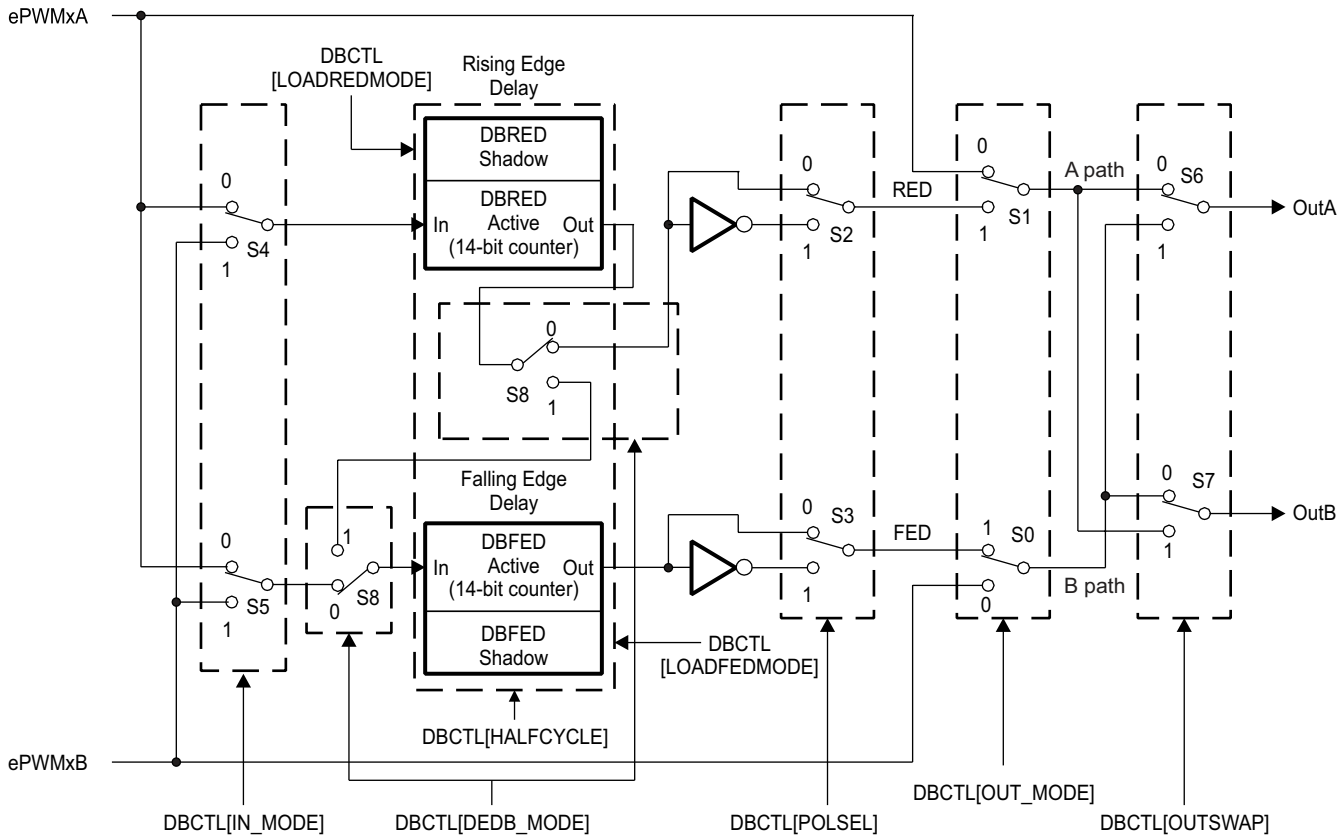


Figure 25-35. Configuration Options for the Dead-Band Submodule

Although all combinations are supported, not all are typical usage modes. Table 25-9 documents some classical dead-band configurations. These modes assume that the DBCTL[IN_MODE] is configured such that EPWMxA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in Table 25-9 fall into the following categories:

- **Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED):** Allows the user to fully disable the dead-band submodule from the PWM signal path.
- **Mode 2-5: Classical Dead-Band Polarity Settings:** These represent typical polarity configurations that can address all the active-high and active-low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in Figure 25-36. Note that to generate equivalent waveforms to Figure 25-36, configure the action-qualifier submodule to generate the signal as shown for EPWMxA.
- **Mode 6: Bypass rising-edge delay (RED) and Mode 7: Bypass falling-edge delay (FED):** Finally the last two entries in Table 25-9 show combinations where either the falling-edge delay (FED) or rising-edge delay (RED) blocks are bypassed.

Figure 25-36 shows waveforms for typical cases where 0% < duty < 100%.

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Table 25-9. Classical Dead-Band Operating Modes

Mode	Mode Description	DBCTL[POLSEL]		DBCTL[OUT_MODE]	
		S3	S2	S1	S0
1	EPWMxA and EPWMxB Passed Through (No Delay)	X	X	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	EPWMxA Out = EPWMxA In (No Delay) EPWMxB Out = EPWMxA In with Falling-Edge Delay	0 or 1	0 or 1	0	1
7	EPWMxA Out = EPWMxA In with Rising-Edge Delay EPWMxB Out = EPWMxB In with No Delay	0 or 1	0 or 1	1	0

Table 25-10. Additional Dead-Band Operating Modes

Mode Description	DBCTL[DEDB-MODE]	DBCTL[OUTSWAP]	
	S8	S6	S7
EPWMxA and EPWMxB signals are as defined by OUT-MODE bits.	0	0	0
EPWMxA = A-path as defined by OUT-MODE bits. EPWMxB = A-path as defined by OUT-MODE bits (rising-edge delay or delay-bypassed A-signal path)	0	0	1
EPWMxA = B-path as defined by OUT-MODE bits (falling-edge delay or delay-bypassed B-signal path) EPWMxB = B-path as defined by OUT-MODE bits	0	1	0
EPWMxA = B-path as defined by OUT-MODE bits (falling-edge delay or delay-bypassed B-signal path) EPWMxB = A-path as defined by OUT-MODE bits (rising-edge delay or delay-bypassed A-signal path)	0	1	1
Rising-edge delay applied to EPWMxA / EPWMxB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling-edge delay applied to EPWMxA / EPWMxB as selected by S5 switch (IN-MODE bits) on B signal path only.	0	X	X
Rising-edge delay and falling-edge delay applied to source selected by S4 switch (IN-MODE bits) and output to B signal path only.(1)	1	X	X

(1) When this bit is set to 1, the user can always either set OUT_MODE bits such that Apath = InA or set OUTSWAP bits such that EPWMxA=Bpath. Otherwise, EPWMxA is invalid.

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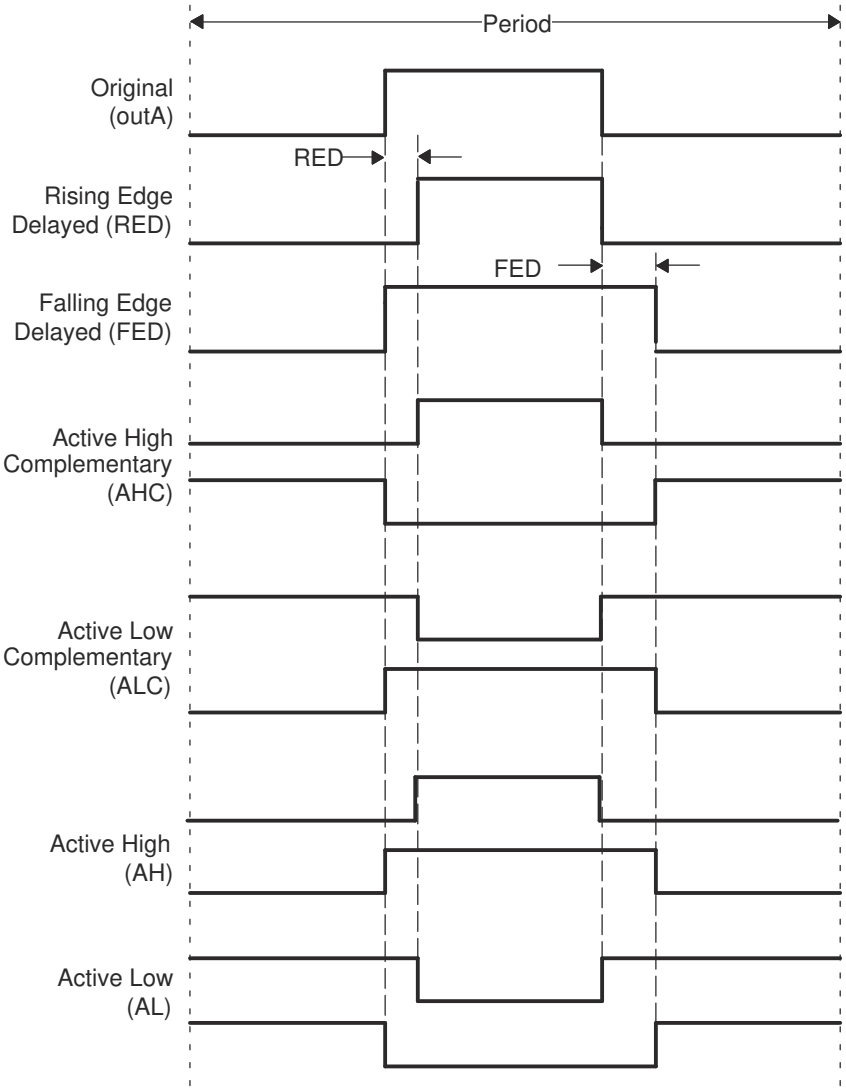


Figure 25-36. Dead-Band Waveforms for Typical Cases (0% < Duty < 100%)

The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the DBRED and DBFED registers. These are 10-bit registers and the value represents the number of TBCLK (time-base clock) pulses by which a signal edge is delayed. For example, the formula to calculate falling-edge-delay and rising-edge-delay is:

FED = DBFED × T_{TBCLK}

RED = DBRED × T_{TBCLK}

Where T_{TBCLK} is the period of TBCLK, the prescaled version of EPWMCLK.

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For convenience, delay values for various TBCLK options are shown in Table 25-11. The ePWM input clock frequency that these delay values been computed by is 100MHz.

Table 25-11. Dead-Band Delay Values in µs as a Function of DBFED and DBRED

Dead-Band Value	Dead-Band Delay (µs)		
DBFED, DBRED	TBCLK = EPWMCLK/1	TBCLK = EPWMCLK /2	TBCLK = EPWMCLK/4
1	0.01	0.02	0.04
5	0.05	0.10	0.20
10	0.10	0.20	0.40
100	1.00	2.00	4.00
200	2.00	4.00	8.00
400	4.00	8.00	16.00
500	5.00	10.00	20.00
600	6.00	12.00	24.00
700	7.00	14.00	28.00
800	8.00	16.00	32.00
900	9.00	18.00	36.00
1000	10.00	20.00	40.00

When half-cycle clocking is enabled, the formula to calculate the falling-edge-delay and rising-edge-delay becomes:

FED = DBFED × $T_{TBCLK}/2$

RED = DBRED × $T_{TBCLK}/2$

25.8 PWM Chopper (PC) Submodule

The PWM chopper submodule allows a high-frequency carrier signal to modulate the PWM waveform generated by the action-qualifier and dead-band submodules. This capability is important if pulse transformer-based gate drivers to control the power switching elements are needed. Figure 25-37 illustrates the PWM chopper submodule within the ePWM.

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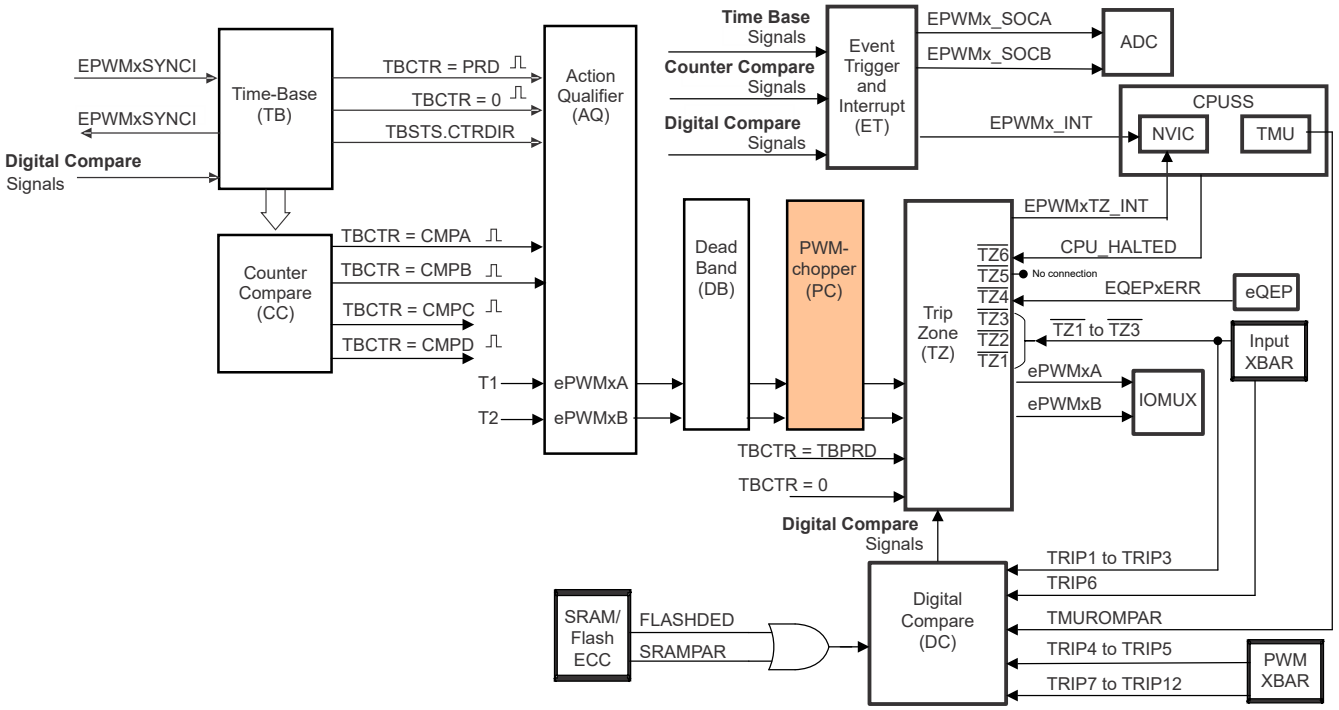


Figure 25-37. PWM Chopper Submodule

25.8.1 Purpose of the PWM Chopper Submodule

The key functions of the PWM chopper submodule are:

- Programmable chopping (carrier) frequency
- Programmable pulse width of first pulse
- Programmable duty cycle of second and subsequent pulses
- Can be fully bypassed if not required

25.8.2 Operational Highlights for the PWM Chopper Submodule

Figure 25-38 shows the operational details of the PWM chopper submodule. The carrier clock is derived from EPWMCLK. The clock frequency and duty cycle are controlled using the CHPFREQ and CHPDUTY bits in the PCCTL register. The one-shot block is a feature that provides a high energy first pulse to make sure hard and fast power switch turn on, while the subsequent pulses sustain pulses, making sure the power switch remains on. The one-shot width is programmed using the OSHTWTH bits. The PWM chopper submodule can be fully disabled (bypassed) using the CHPEN bit.

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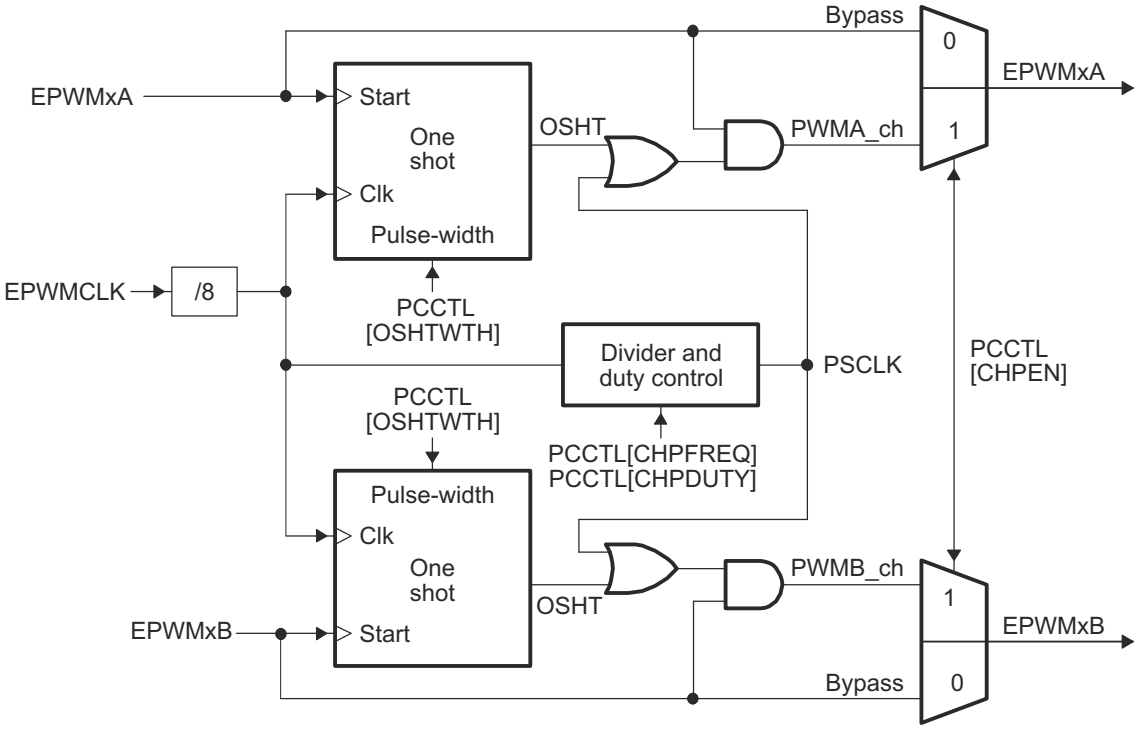


Figure 25-38. PWM Chopper Submodule Operational Details

25.8.3 Waveforms

Figure 25-39 shows simplified waveforms of the chopping action only; one-shot and duty-cycle control are not shown. Details of the one-shot and duty-cycle control are discussed in the following sections.

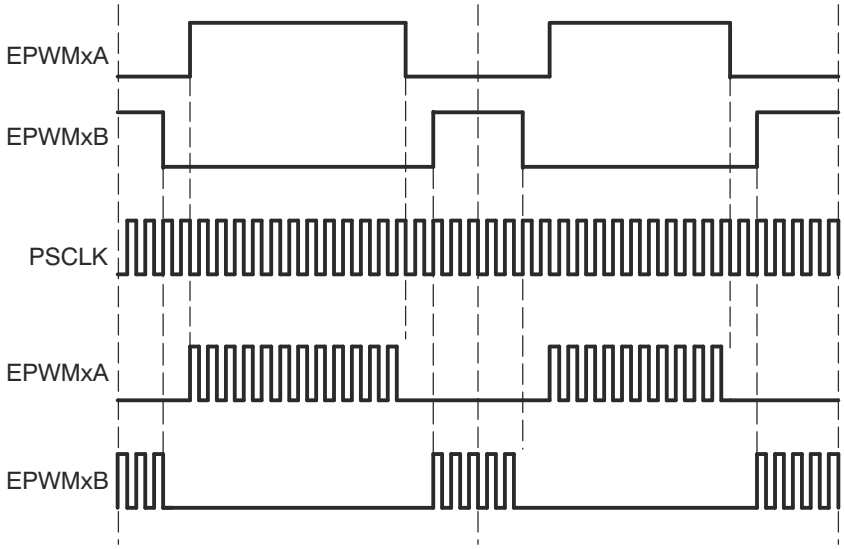


Figure 25-39. Simple PWM Chopper Submodule Waveforms Showing Chopping Action Only

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25.8.3.1 One-Shot Pulse

The width of the first pulse can be programmed to any of 16 possible pulse width values. The width or period of the first pulse is given by:

$$T_{1stpulse} = T_{EPWMCLK} \times 8 \times OSHTWTH$$

Where $T_{EPWMCLK}$ is the period of the system clock (EPWMCLK) and OSHTWTH is the four control bits (value from 1 to 16)

Figure 25-40 shows the first and subsequent sustaining pulses and Table 25-12 gives the possible pulse width values for a EPWMCLK = 80MHz.

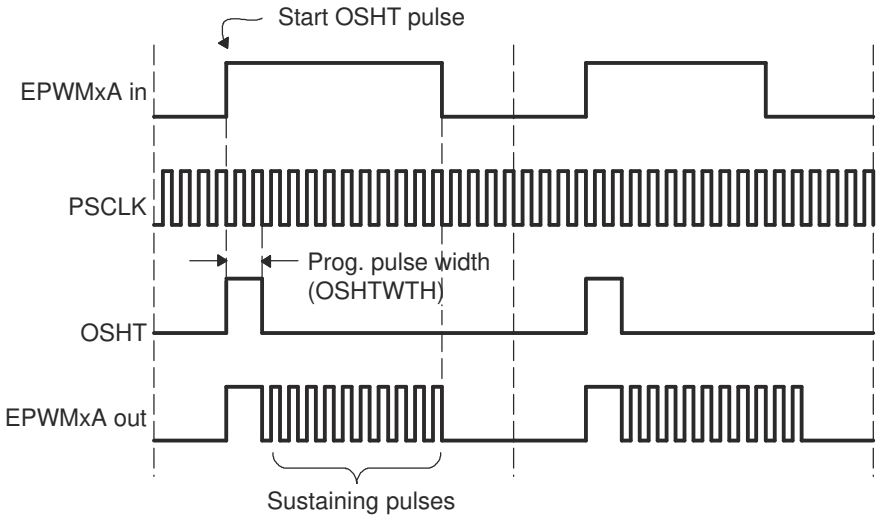


Figure 25-40. PWM Chopper Submodule Waveforms Showing the First Pulse and Subsequent Sustaining Pulses

Table 25-12. Possible Pulse Width Values for EPWMCLK = 80MHz

OSHTWTH (hex)	Pulse Width (ns)
0	100
1	200
2	300
3	400
4	500
5	600
6	700
7	800
8	900
9	1000
A	1100
B	1200
C	1300
D	1400
E	1500
F	1600

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25.8.3.2 Duty Cycle Control

Pulse transformer-based gate drive designs need to comprehend the magnetic properties or characteristics of the transformer and associated circuitry. Saturation is one such consideration. To assist the gate drive designer, the duty cycles of the second and subsequent pulses have been made programmable. These sustaining pulses make sure the correct drive strength and polarity is maintained on the power switch gate during the on period, and hence a programmable duty cycle allows a design to be tuned or optimized using software control.

Figure 25-41 shows the duty cycle control that is possible by programming the CHPDUTY bits. One of seven possible duty ratios can be selected ranging from 12.5% to 87.5%.

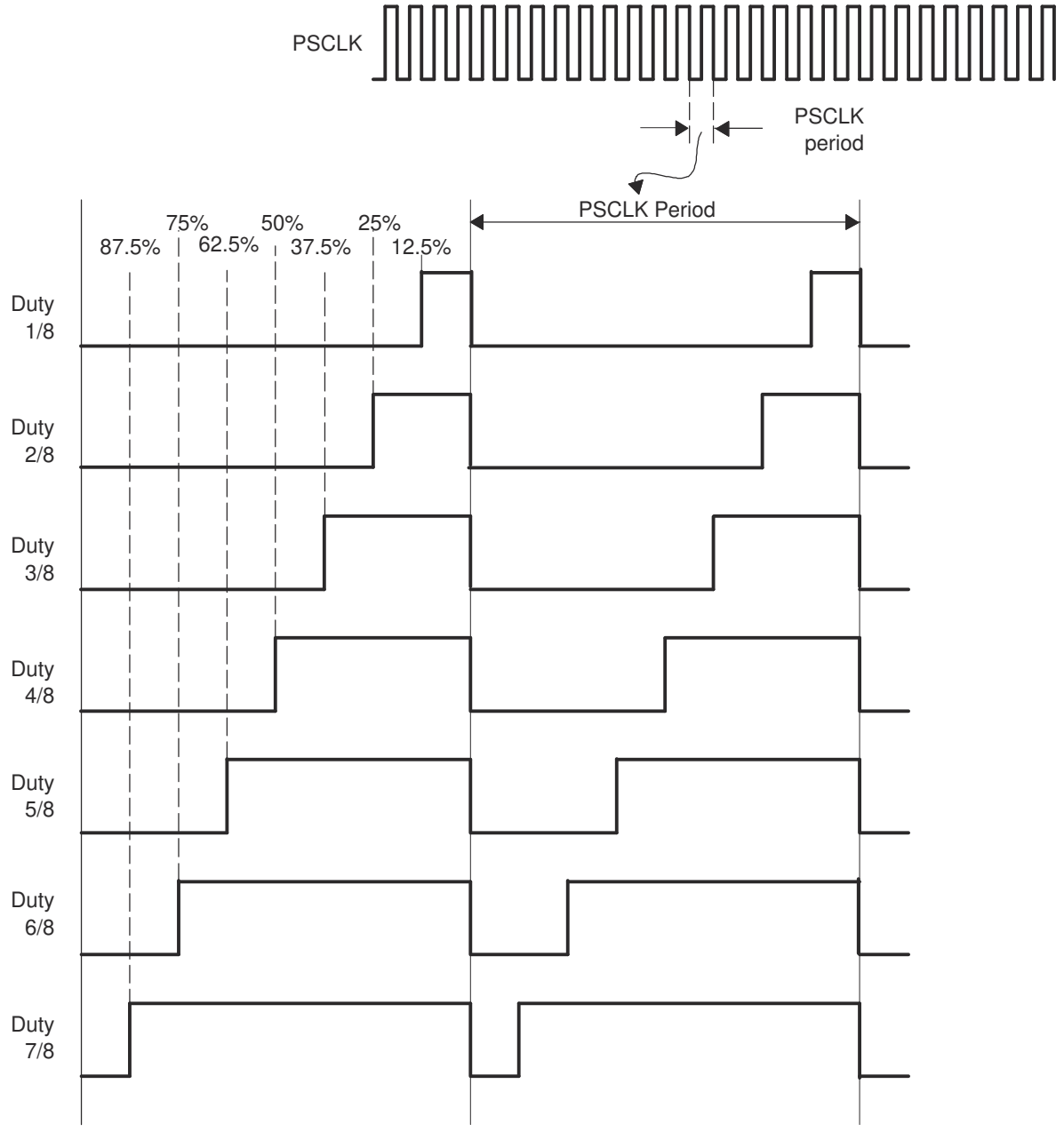


Figure 25-41. PWM Chopper Submodule Waveforms Showing the Pulse Width (Duty Cycle) Control of Sustaining Pulses

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25.9 Trip-Zone (TZ) Submodule

Each ePWM module is connected to six $\overline{TZn}$ signals ($\overline{TZ1}$ to $\overline{TZ6}$). $\overline{TZ1}$ to $\overline{TZ3}$ are sourced from the INPUT XBAR. $\overline{TZ4}$ is sourced from an inverted EQEPxERR signal. $\overline{TZ6}$ is sourced from the CPU_HALTED output from the CPU. These signals indicate external fault or trip conditions, and the ePWM outputs can be programmed to respond accordingly when faults occurs. Figure 25-42 illustrates the trip-zone submodule within the ePWM.

Note

$\overline{TZ5}$ is unused/disconnected on this device.

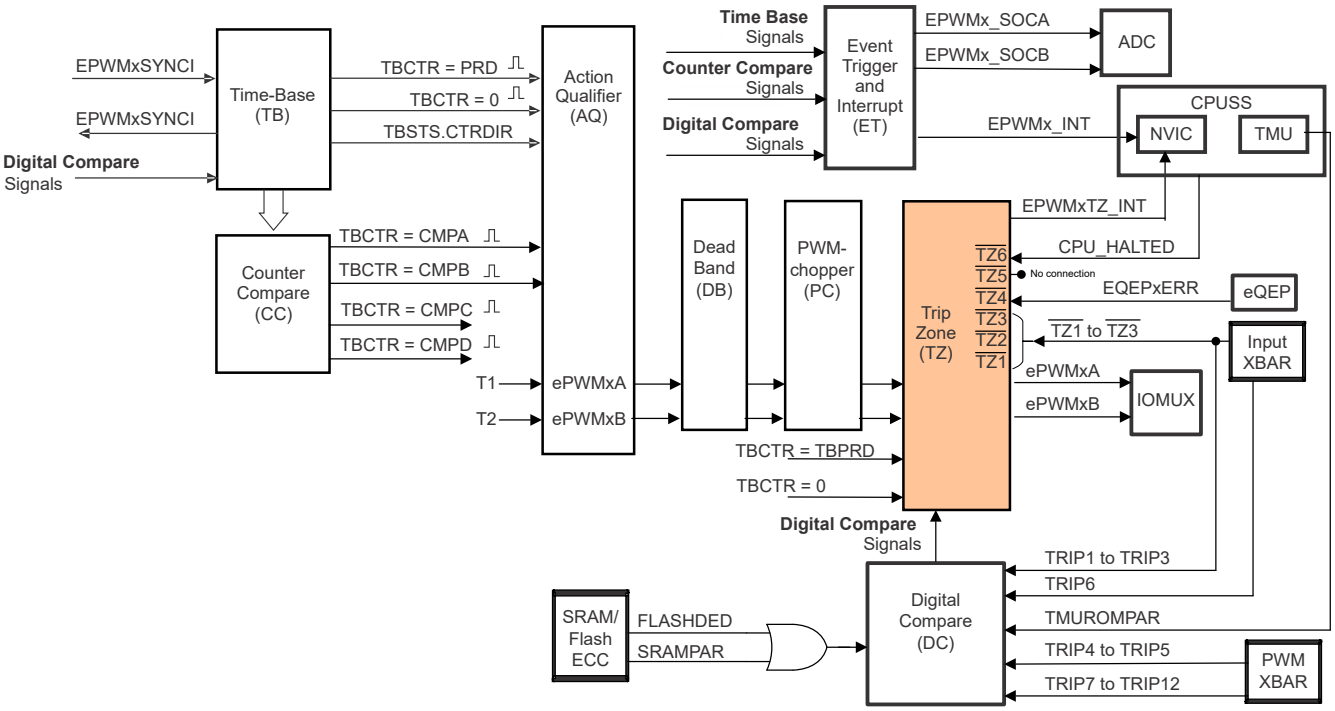


Figure 25-42. Trip-Zone Submodule

25.9.1 Purpose of the Trip-Zone Submodule

The key functions of the trip-zone submodule are:

- Trip inputs $\overline{TZ1}$ to $\overline{TZ6}$ can be flexibly mapped to any ePWM module.
- Upon a fault condition, outputs EPWMxA and EPWMxB can be forced to one of the following:
  - High
  - Low
  - High-impedance
  - No action taken
- Support for one-shot trip (OSHT) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Support for digital compare tripping (DC) based on state of on-chip analog comparator module outputs and $\overline{TZ1}$ to $\overline{TZ3}$ signals.
- Each trip-zone input and digital compare (DC) submodule DCAEVT1/2 or DCBEVT1/2 force event can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone input.
- Software-forced tripping is also supported.
- The trip-zone submodule can be fully bypassed if the trip-zone submodule is not required.

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25.9.2 Operational Highlights for the Trip-Zone Submodule

The following sections describe the operational highlights and configuration options for the trip-zone submodule.

The trip-zone signals $\overline{TZ1}$ to $\overline{TZ6}$ (also collectively referred to as $\overline{TZn}$) are active-low input signals. When one of these signals goes low, or when a DCAEVT1/2 or DCBEVT1/2 force happens based on the TZDCSEL register event selection, the indication is that a trip event has occurred. Each ePWM module can be individually configured to ignore or use each of the trip-zone signals or DC events. Which trip-zone signals or DC events are used by a particular ePWM module is determined by the TZSEL register for that specific ePWM module. The trip-zone signals can or cannot be synchronized to the ePWMclock (EPWMCLK) and digitally filtered within the GPIO MUX block. A minimum of 3 × TBCLK low pulse width on $\overline{TZn}$ inputs is sufficient to trigger a fault condition on the ePWM module. If the pulse width is less than this, the trip condition cannot be latched by CBC or OST latches. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on $\overline{TZn}$ inputs. The GPIOs or peripherals must be appropriately configured. For more information, see the *System Control and Interrupts* chapter.

Each $\overline{TZn}$ input can be individually configured to provide either a cycle-by-cycle or one-shot trip event for an ePWM module. DCAEVT1 and DCBEVT1 events can be configured to directly trip an ePWM module or provide a one-shot trip event to the module. Likewise, DCAEVT2 and DCBEVT2 events can also be configured to directly trip an ePWM module or provide a cycle-by-cycle trip event to the module. This configuration is determined by the TZSEL[DCAEVT1/2], TZSEL[DCBEVT1/2], TZSEL[CBCn], and TZSEL[OSHTn] control bits (where n corresponds to the trip input), respectively.

- **Cycle-by-Cycle (CBC):**

  When a cycle-by-cycle trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the EPWMxA and EPWMxB outputs. Table 25-13 lists some of the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up or while the counter is counting down by appropriately configuring bits in the TZCTL2 register. Actions specified in the TZCTL2 register take effect only when the ETZE bit in TZCTL2 is set.

  Additionally, when a cycle-by-cycle trip event occurs, the cycle-by-cycle trip event flag (TZFLG[CBC]) is set and a EPWMx_TZINT interrupt is generated when enabled in the TZEINT register and interrupt controller. A corresponding flag for the event that caused the CBC event is also set in register TZCBCFLG.

  If the CBC interrupt is enabled using the TZEINT register and DCAEVT2 or DCBEVT2 are selected as CBC trip sources using the TZSEL register, it is not necessary to also enable the DCAEVT2 or DCBEVT2 interrupts in the TZEINT register, as the DC events trigger interrupts through the CBC mechanism.

  The specified condition on the inputs is automatically cleared based on the selection made with TZCLR[CBCPULSE] if the trip event is no longer present. The TZFLG[CBC] and TZCBCFLG flag bits remain set until the flag bits are manually cleared by writing to the TZCLR[CBC] and TZCBCCLR flag bits. If the cycle-by-cycle trip event is still present when the TZFLG[CBC] and TZCBCFLG register bits are cleared, then these bits are again immediately set.

- **One-Shot (OSHT):**

  When a one-shot trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the EPWMxA and EPWMxB output. Table 25-13 lists some of the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up and while the counter is counting down by appropriately configuring bits in TZCTL2 register. Actions specified in TZCTL2 register take effect only when ETZE bit in TZCTL2 is set.

  Additionally, when a one-shot trip event occurs, the one-shot trip event flag (TZFLG[OST]) is set and a EPWMx_TZINT interrupt is generated when enabled in the TZEINT register and interrupt controller. A corresponding flag for the event that caused the OST event is also set in register TZOSTFLG. The one-shot trip condition must be cleared manually by writing to the TZCLR[OST] bit. If desired, the TZOSTFLG register bit can be cleared by manually writing to the corresponding bit in the TZOSTCLR register.

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If the one-shot interrupt is enabled using the TZEINT register and DCAEVT1 or DCBEVT1 are selected as OSHT trip sources using the TZSEL register, it is not necessary to also enable the DCAEVT1 or DCBEVT1 interrupts in the TZEINT register, as the DC events trigger interrupts through the OSHT mechanism.

Note

Clear the TZFLG and TZOSTFLG flags after making sure that the TRIPIN source of the OST has become inactive. Otherwise, if interrupts are enabled, depending on when the flags are cleared, an OST interrupt can occur and the OST flags are zero.

- **Digital Compare Events (DCAEVT1/2 and DCBEVT1/2):**

Note

When using DCAEVT1/2.force and DCBEVT1/2.force for one-shot or CBC trip event, set the DCxCTL.EVTxFRCSYNCSEL = 0. The async path does not set the one-shot or CBC trip condition.

A digital compare DCAEVT1/2 or DCBEVT1/2 event is generated based on a combination of the DCAH/DCAL and DCBH/DCBL signals as selected by the TZDCSEL register. The signals which source the DCAH/DCAL and DCBH/DCBL signals are selected using the DCTRIPSEL register and can be either trip zone input pins or analog comparator CMPSSx signals. For more information on the digital compare submodule signals, see Section 25.11 .

When a digital compare event occurs, the action specified in the TZCTL[DCAEVT1/2] and TZCTL[DCBEVT1/2] bits is carried out immediately on the EPWMxA and EPWMxB output. Table 25-13 lists the possible actions. Independent actions can be specified based on the occurrence of the event while the counter is counting up and while the counter is counting down by appropriately configuring bits in TZCTLDCA and TZCTLDCB register. Actions specified in TZCTLDCA and TZCTLDCB registers take effect only when ETZE bit in TZCTL2 is set.

In addition, the relevant DC trip event flag (TZFLG[DCAEVT1/2] / TZFLG[DCBEVT1/2]) is set and a EPWMx_TZINT interrupt is generated when enabled in the TZEINT register and interrupt controller.

The specified condition on the pins is automatically cleared when the DC trip event is no longer present. The TZFLG[DCAEVT1/2] or TZFLG[DCBEVT1/2] flag bit remains set until the flag is manually cleared by writing to the TZCLR[DCAEVT1/2] or TZCLR[DCBEVT1/2] bit. If the DC trip event is still present when the TZFLG[DCAEVT1/2] or TZFLG[DCBEVT1/2] flag is cleared, then the flag is again immediately set.

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The action taken when a trip event occurs can be configured individually for each of the ePWM output pins by way of the TZCTL, TZCTL2, TZCTLDCA, and TZCTLDCB register bit fields. Some of the possible actions, shown in Table 25-13, can be taken on a trip event.

Table 25-13. Possible Actions On a Trip Event

TZCTL Register Bitfield Settings	EPWMxA and EPWMxB	Comment
0,0	High-Impedance	Tripped
0,1	Force to High State	Tripped
1,0	Force to Low State	Tripped
1,1	No Change	Do Nothing. No change is made to the output.

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Trip-Zone Configurations

Scenario A:

A one-shot trip event on $\overline{TZ1}$ pulls both EPWM1A, EPWM1B low and also forces EPWM2A and EPWM2B high.

- Configure the ePWM1 registers as follows:
  - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM1
  - TZCTL[TZA] = 2: EPWM1A is forced low on a trip event.
  - TZCTL[TZB] = 2: EPWM1B is forced low on a trip event.
- Configure the ePWM2 registers as follows:
  - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM2
  - TZCTL[TZA] = 1: EPWM2A is forced high on a trip event.
  - TZCTL[TZB] = 1: EPWM2B is forced high on a trip event.

Scenario B:

A cycle-by-cycle event on $\overline{TZ5}$ pulls both EPWM1A, EPWM1B low.
A one-shot event on $\overline{TZ1}$ or $\overline{TZ6}$ puts EPWM2A into a high impedance state.

- Configure the ePWM1 registers as follows:
  - TZSEL[CBC5] = 1: enables $\overline{TZ5}$ as a cycle-by-cycle event source for ePWM1
  - TZCTL[TZA] = 2: EPWM1A is forced low on a trip event.
  - TZCTL[TZB] = 2: EPWM1B is forced low on a trip event.
- Configure the ePWM2 registers as follows:
  - TZSEL[OSHT1] = 1: enables $\overline{TZ1}$ as a one-shot event source for ePWM2
  - TZSEL[OSHT6] = 1: enables $\overline{TZ6}$ as a one-shot event source for ePWM2
  - TZCTL[TZA] = 0: EPWM2A is put into a high-impedance state on a trip event.
  - TZCTL[TZB] = 3: EPWM2B ignores the trip event.

Note

When configuring the GPIOs and INPUT X-BAR/EPWM X-BAR options, be aware that a change in the X-BAR input selections can cause an unwanted event. Therefore, set up the GPIO and X-BAR input configurations before enabling the ePWM Trip-Zone. If a requirement is to change the GPIO/X-BAR configurations while the ePWM Trip-Zone is enabled, the user can turn off the TRIPs by clearing the TZSEL register and reconfiguring the TRIP selection (TZSEL) after the INPUT XBAR selection is changed.

25.9.3 Generating Trip Event Interrupts

Figure 25-43 and Figure 25-44 illustrate the trip-zone submodule control and interrupt logic, respectively. DCAEVT1/2 and DCBEVT1/2 signals are described in further detail in Section 25.11 .

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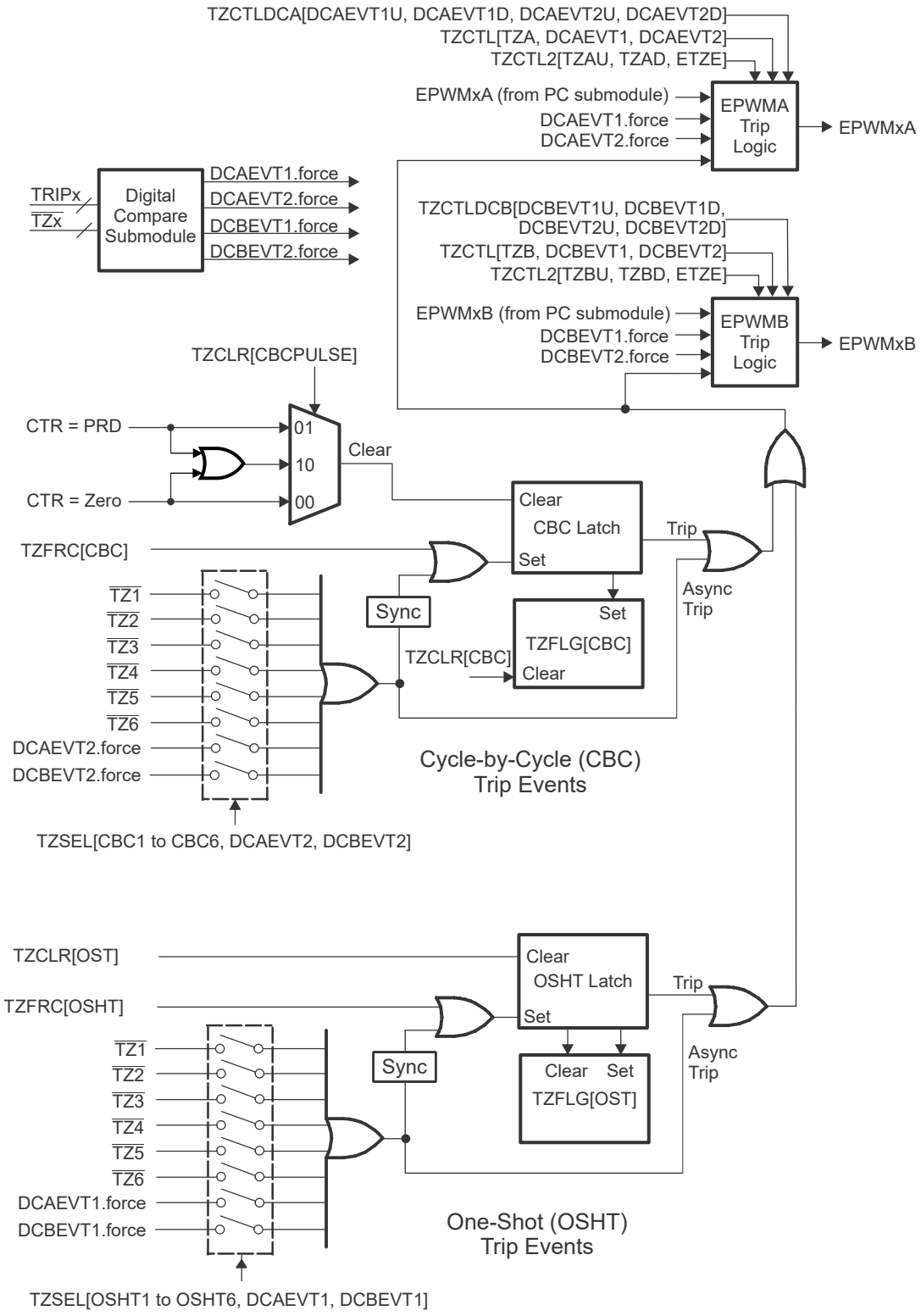


Figure 25-43. Trip-Zone Submodule Mode Control Logic

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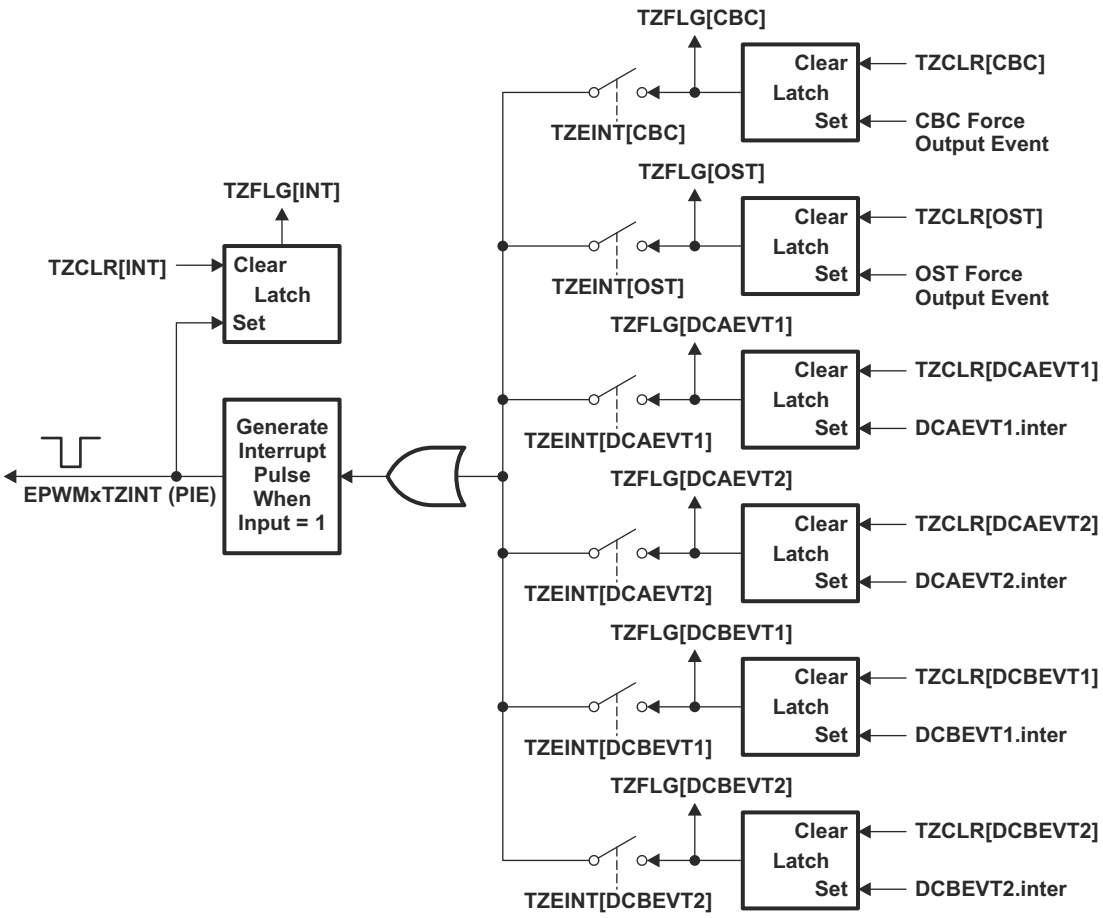


Figure 25-44. Trip-Zone Submodule Interrupt Logic

These individual flags for the CBC, OST, and DCxEVTy can be used to detect the source of the EPWMxTZINT Interrupt. When multiple sources are used to generate the EPWMxTZINT interrupt, reading and clearing the flags takes different actions based on the specific event.

25.10 Event-Trigger (ET) Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base, counter-compare, and digital-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests and ADC start of conversion at:
  - Every event
  - Every second event
  - Up to every fifteenth event
- Provides full visibility of event generation using event counters and flags
- Allows software forcing of Interrupts and ADC start of conversion

The event-trigger submodule manages the events generated by the time-base submodule, the counter-compare submodule, and the digital-compare submodule to generate an interrupt to the CPU and a start of conversion pulse to the ADC when a selected event occurs. Figure 25-45 illustrates the event-trigger submodule within the ePWM.

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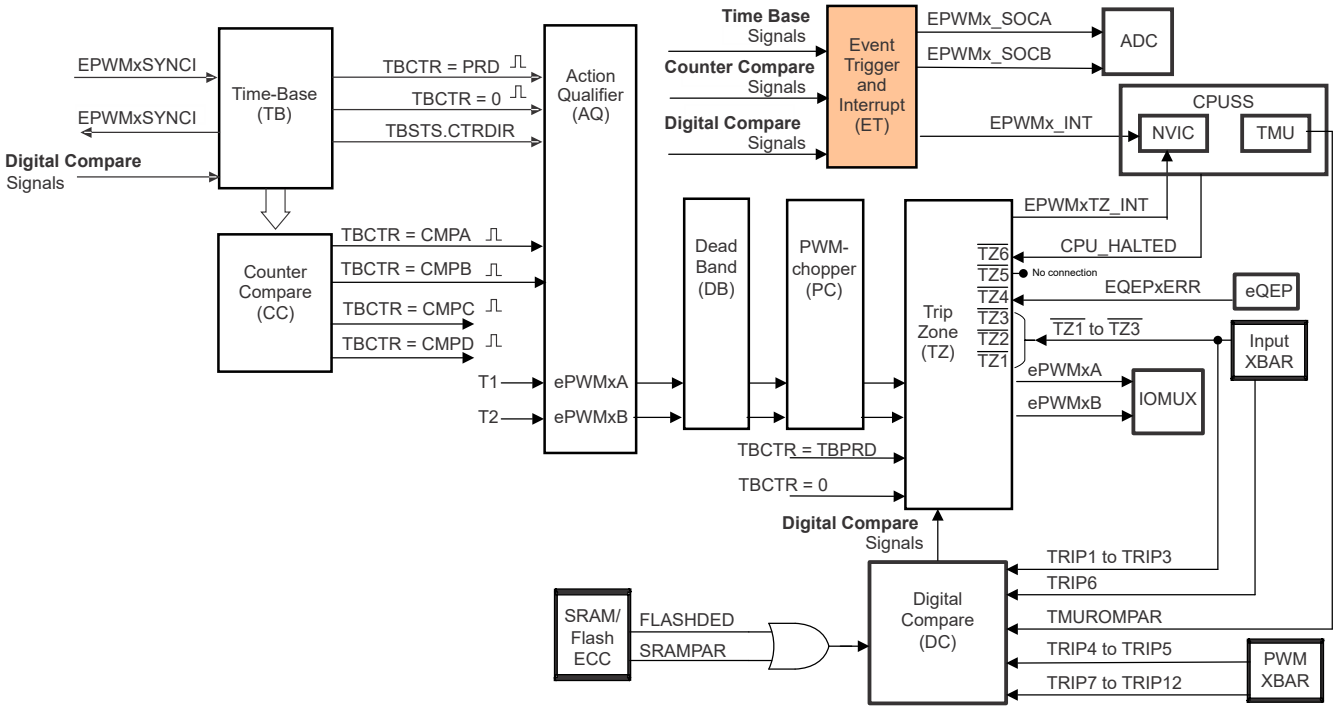


Figure 25-45. Event-Trigger Submodule

25.10.1 Operational Overview of the ePWM Event-Trigger Submodule

The event-trigger submodule monitors various event conditions (shown as inputs on the left side of Figure 25-46) and can be configured to prescale these events before issuing an Interrupt request or an ADC start of conversion. The event-trigger prescaling logic can issue Interrupt requests and ADC start of conversion at:

- Every event
- Every second event
- Up to every fifteenth event

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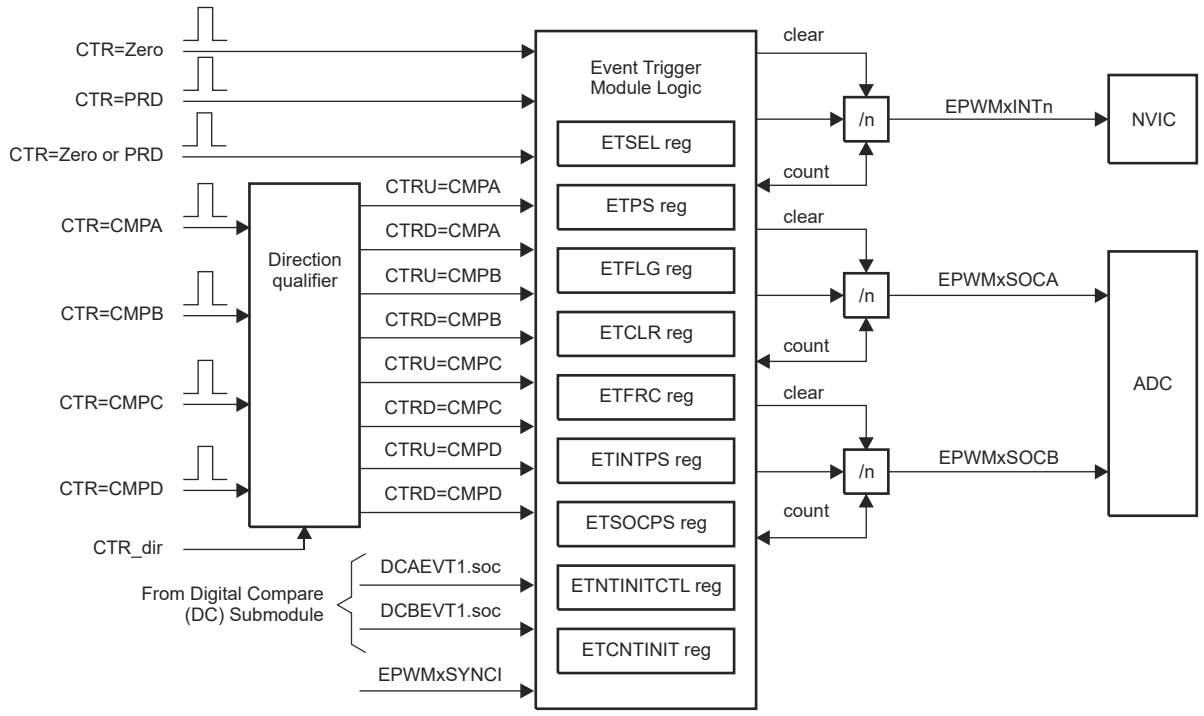


Figure 25-46. Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs

- ETSEL - This selects which of the possible events trigger an interrupt or start an ADC conversion.
- ETPS - This programs the event prescaling options mentioned above.
- ETFLG - These are flag bits indicating status of the selected and prescaled events.
- ETCLR - These bits allow clearing the flag bits in the ETFLG register using software.
- ETFRC - These bits allow software forcing of an event. Useful for debugging or software intervention.
- ETINTPS - This programs the interrupt event prescaling options, supporting count and period up to 15 events.
- ETSOCPS - This programs the SOC event prescaling options, supporting count and period up to 15 events.
- ETCNTINITCTL - These bits enable ETCNTINIT initialization using SYNC event or using software force.
- ETCNTINIT - These bits allow initializing INT/SOCA/SOCB counters on SYNC events (or software force) with user programmed value.

A more detailed look at how the various register bits interact with the Interrupt and ADC start of conversion logic are shown in Figure 25-47, Figure 25-48, and Figure 25-49.

Figure 25-47 shows the event-trigger's interrupt generation logic. The interrupt-period (ETPS[INTPRD]) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt.
- Generate an interrupt on every event.
- Generate an interrupt on every second event.
- Generate an interrupt on every third event.

The selection made on ETPS[INTPSSEL] bit determines whether ETINTPS register, INTCNT2 and INTPRD2 bit fields determine frequency of events (interrupt once every 0-15 events).

The event that can cause an interrupt is configured by the interrupt selection (ETSEL[INTSEL]) and (ETSEL[INTSELCMP]) bits. The event can be one of the following:

- Time-base counter equal to zero (TBCTR = 0x00).
- Time-base counter equal to period (TBCTR = TBPRD).
- Time-base counter equal to zero or period (TBCTR = 0x00 || TBCTR = TBPRD).

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- Time-base counter equal to the compare A register (CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is decrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is incrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is decrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is incrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is decrementing.

The number of events that have occurred can be read from the interrupt event counter ETPS[INTCNT] or ETINTPS[INTCNT2] register bits based off of the selection made using ETPS[INTPSSEL]. That is, when the specified event occurs the ETPS[INTCNT] or ETINTPS[INTCNT2] bits are incremented until the bits reach the value specified by ETPS[INTPRD] or ETINTPS[INTPRD2] determined again by the selection made in ETPS[INTPSSEL]. When ETPS[INTCNT] = ETPS[INTPRD], the counter stops counting and the counter output is set. The counter is only cleared when an interrupt is sent to the interrupt controller.

When ETPS[INTCNT] reaches ETPS[INTPRD], the following behavior occurs. [The following behavior is also applicable to ETINTPS[INTCNT2] and ETINTPS[INTPRD2]:

- If interrupts are enabled, ETSEL[INTEN] = 1 and the interrupt flag is clear, ETFLG[INT] = 0, then an interrupt pulse is generated and the interrupt flag is set, ETFLG[INT] = 1, and the event counter is cleared ETPS[INTCNT] = 0. The counter begins counting events again.
- If interrupts are disabled, ETSEL[INTEN] = 0, or the interrupt flag is set, ETFLG[INT] = 1, the counter stops counting events when the counter reaches the period value ETPS[INTCNT] = ETPS[INTPRD].
- If interrupts are enabled, but the interrupt flag is already set, then the counter holds the output high until the ENTFLG[INT] flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing a 0 to the INTPRD bits automatically clears the counter (INTCNT = 0) and the counter output resets (so no interrupts are generated). For all other writes to INTPRD, INTCNT retains the previous value. INTCNT resets when INTCNT overflows. Writing a 1 to the ETFRC[INT] bit increments the event counter INTCNT. The counter behaves as previously described when INTCNT = INTPRD. When INTPRD = 0, the counter is disabled and hence no events are detected and the ETFRC[INT] bit is also ignored. The same applies to ETINTPS[INTCNT2] and ETINTPS[INTPRD2].

The previous definition means that an interrupt on every event, on every second event, or on every third event if using the INTCNT and INTPRD can be generated. An interrupt on every event up to 15 events if using the INTCNT2 and INTPRD2 can be generated.

The INTCNT2 value can be initialized with the value from ETCNTINIT[INTINIT] based on the selection made in ETCNTINITCTL[INTINITEN]. When ETCNTINITCTL[INTINITEN] is set, then initialization of INTCNT2 counter with contents of ETCNTINIT[INTINIT] on a SYNC event or software force is determined by ETCNTINITCTL[INTINITFRC].

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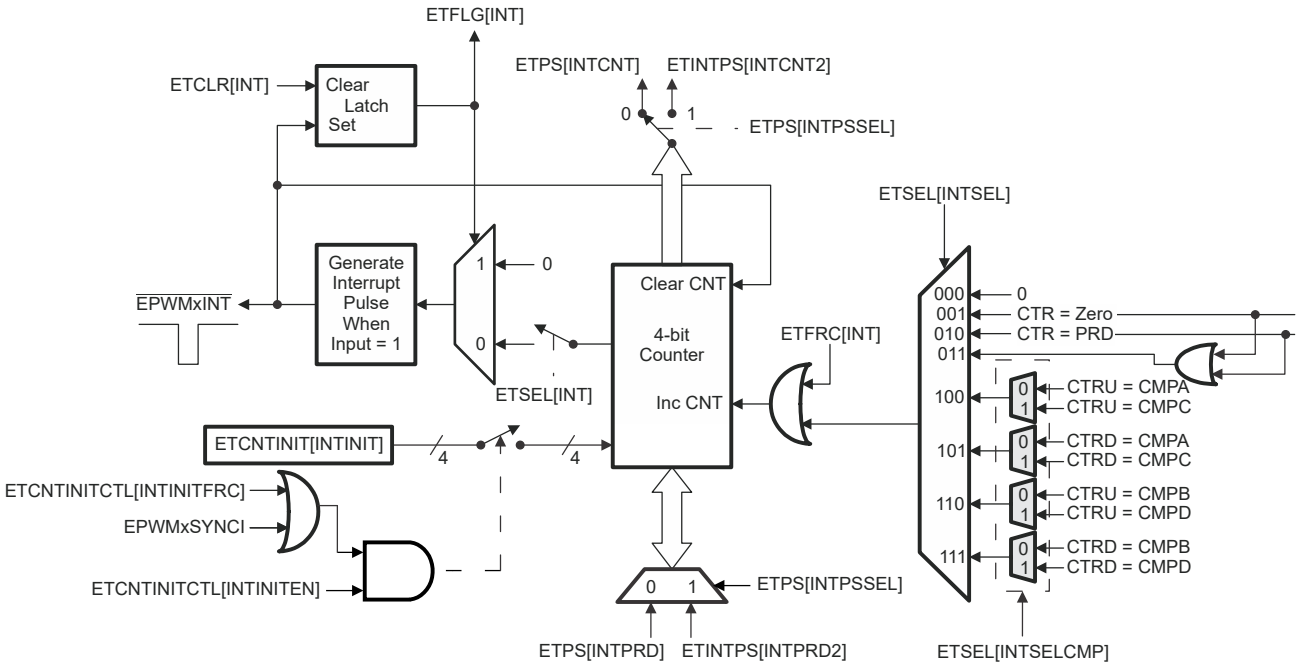
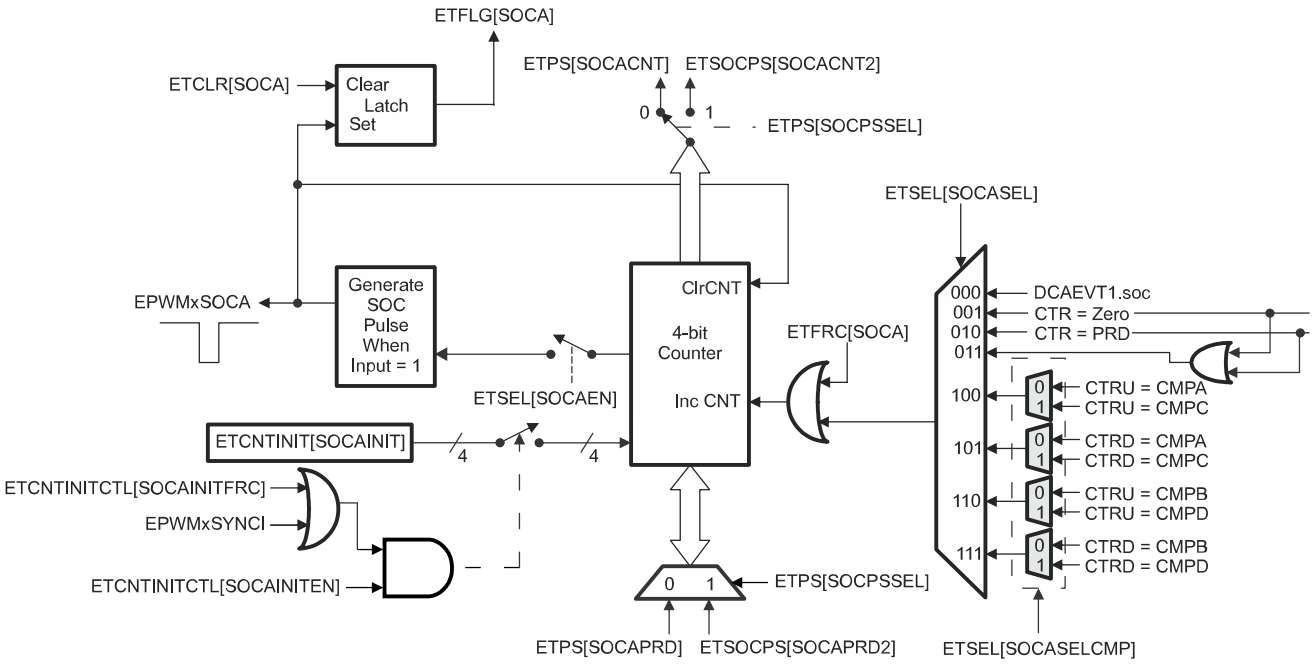


Figure 25-47. Event-Trigger Interrupt Generator

Figure 25-48 shows the operation of the event-trigger's start-of-conversion-A (SOCA) pulse generator. The enhancements include SOCASELCMP and SOCBSELCMP bit fields defined in the ETSEL register enable CMPC and CMPD events respectively to cause a start of conversion. The ETPS[SOCPSSEL] bit field determines whether SOCACNT2 and SOCAPRD2 take control or not. The ETPS[SOCACNT] counter and ETPS[SOCAPRD] period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag ETFLG[SOCA] is latched when a pulse is generated, but the interrupt generator does not stop further pulse generation. The enable and disable bit ETSEL[SOCAEN] stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that triggers an SOCA and SOCB pulse can be configured separately in the ETSEL[SOCASEL] and ETSEL[SOCBSEL] bits. The possible events are the same events that can be specified for the interrupt generation logic with the addition of the DCAEVT1.soc and DCBEVT1.soc event signals from the digital compare (DC) submodule. The SOCACNT2 initialization scheme is very similar to the interrupt generator with respective enable, value initialize and SYNC or software force options.

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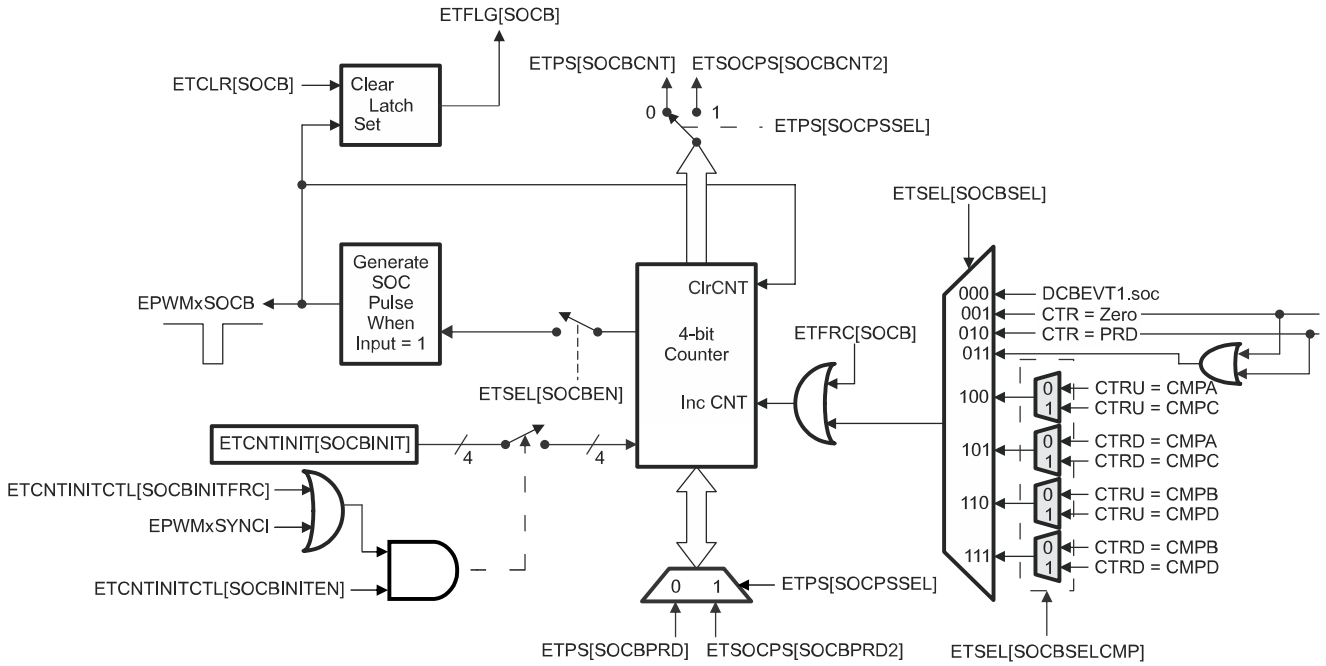


Note

NOTE: The DCAEVT1.soc signals are generated by the Digital Compare (DC) submodule in Section 25.11 .

Figure 25-48. Event-Trigger SOCA Pulse Generator

Figure 25-49 shows the operation of the event-trigger's start-of-conversion-B (SOCB) pulse generator. The event-trigger's SOCB pulse generator operates the same way as the SOCA.



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Note

NOTE: The DCBEVT1.soc signals are generated by the Digital Compare (DC) submodule in Section 25.11 .

Figure 25-49. Event-Trigger SOCB Pulse Generator

25.11 Digital Compare (DC) Submodule

Figure 25-50 illustrates the digital-compare submodule within the ePWM.

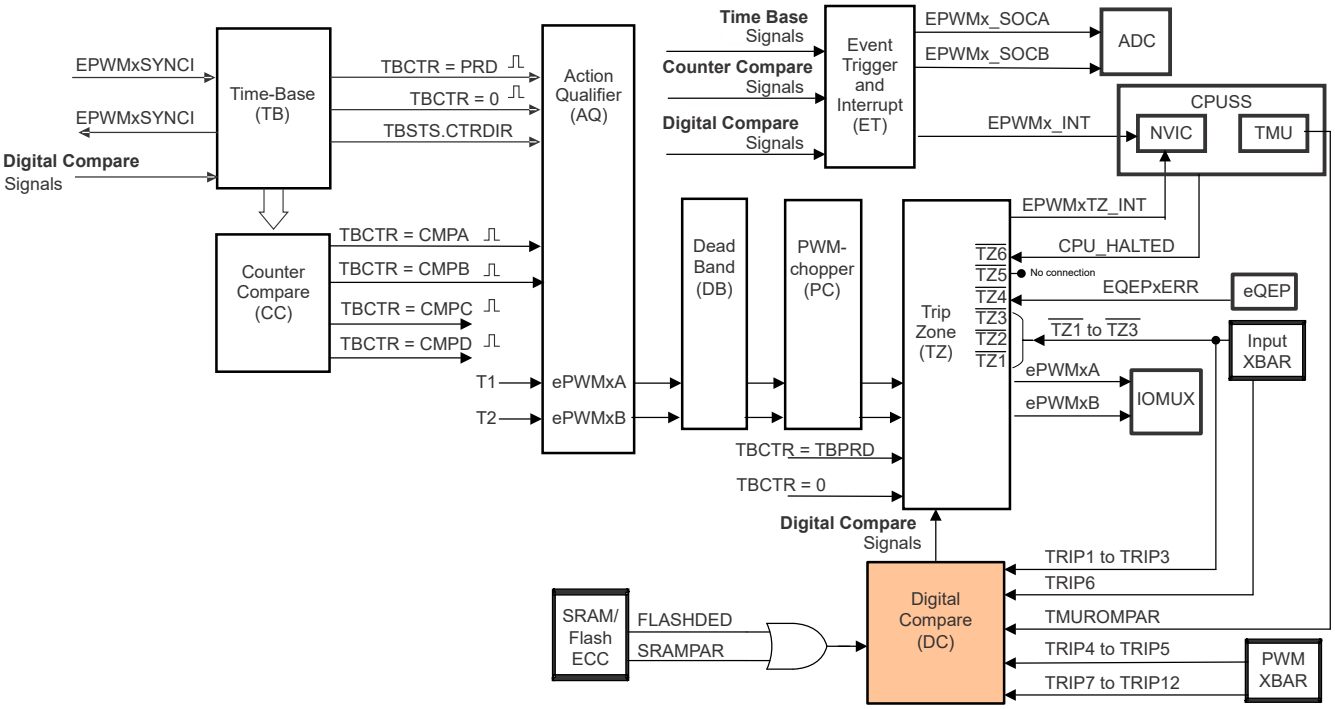


Figure 25-50. Digital-Compare Submodule

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25.11.1 Purpose of the Digital Compare Submodule

The key functions of the digital compare submodule are:

- Analog comparator (COMP) module outputs fed though the Input X-BAR, EPWM X-BAR, externally using the GPIO peripheral, interrupt controller signals, ECC error signals, $\overline{TZ1}$, $\overline{TZ2}$, and $\overline{TZ3}$ inputs generate Digital Compare A High/Low (DCAH, DCAL) and Digital Compare B High/Low (DCBH, DCBL) signals.
- DCAH/L and DCBH/L signals trigger events that can then either be filtered or applied directly to the trip-zone, event-trigger, and time-base submodules to:
  - generate a trip zone interrupt
  - generate an ADC start of conversion
  - force an event
  - generate a synchronization event for synchronizing the ePWM module TBCTR.
- Event filtering (blanking window logic) can optionally blank the input signal to remove noise.

25.11.2 Enhanced Trip Action Using CMPSS

To allow multiple CMPSS at a time to affect DCA/BEVTx events and trip actions, there is a OR logic to bring together ALL trip inputs (up to 15) from sources external to the ePWM module and feed into DCAH, DCAL, DCBH, and DCBL as a “combinational input” using the DCTRIPSEL register. This is configured by selecting “Trip combination input” (value of 0xF) in the DCTRIPSEL register.

There is a discrete choice of which trip inputs to put through the combinational logic for generating the DCAH, DCAL, DCBH, and DCBL signals. This is achieved using the DCAHTRIPSEL, DCALTRIPSEL, DCBHTRIPSEL, and DCBLTRIPSEL register selections. Inputs selected for combinational input are passed through to the DCTRIPSEL register.

25.11.3 Using CMPSS to Trip the ePWM on a Cycle-by-Cycle Basis

When using the CMPSS to trip the ePWM on a cycle-by-cycle basis, steps can be taken to prevent an asserted comparator trip state in one PWM cycle from extending into the following cycle. The CMPSS can be used to signal a trip condition to the downstream ePWM modules. For applications like peak current mode control, only one trip event per PWM cycle is expected. Under certain conditions, it is possible for a sustained or late trip event (arriving near the end of a PWM cycle) to carry over into the next PWM cycle if precautions are not taken. If either the CMPSS Digital Filter or the ePWM Digital Compare (DC) submodule is configured to qualify the comparator trip signal, “N” number of clock cycles of qualification are introduced before the ePWM trip logic can respond to logic changes of the trip signal. Once an ePWM trip condition is qualified, the trip condition remains active for N clock cycles after the comparator trip signal has de-asserted. If a qualified comparator trip signal remains asserted within N clock cycles prior to the end of a PWM cycle, the trip condition is not cleared until after the following PWM cycle has started. Thus, the new PWM cycle detects a trip condition as soon as the cycle begins.

To avoid this undesired trip condition, the application can take steps to make sure that the qualified trip signal seen by the ePWM trip logic is deasserted prior to the end of each PWM cycle. This can be accomplished through various methods:

- Design the system such that a comparator trip is not asserted within N clock cycles prior to the end of the PWM cycle.
- Activate blanking of the comparator trip signal using the ePWM event filter at least two clock cycles prior to the PWMSYNCPER signal and continue blanking for at least N clock cycles into the next PWM cycle.
- If the CMPSS COMPxLATCH path is used, clear the COMPxLATCH at least N clock cycles prior to the end of the PWM cycle. The latch can be cleared by software (using COMPSTSCLR) or by generating an early PWMSYNCPER signal. The ePWM modules on this device include the ability to generate PWMSYNCPER upon a CMPC or CMPD match (using HRPCTL) for arbitrary PWMSYNCPER placement within the PWM cycle.

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25.11.4 Operation Highlights of the Digital Compare Submodule

The following sections describe the operational highlights and configuration options for the digital compare submodule.

25.11.4.1 Digital Compare Events

As described in Section 25.11.1 , trip zone inputs ($\overline{TZ1}$, $\overline{TZ2}$, and $\overline{TZ3}$) and CMPSSx signals from the analog comparator (COMP) module can be selected using the DCTRIPSEL bits to generate the Digital Compare A High and Low (DCAH/L) and Digital Compare B High and Low (DCBH/L) signals. Then, the configuration of the TZDCSEL register qualifies the actions on the selected DCAH/L and DCBH/L signals, which generate the DCAEVT1/2 and DCBEVT1/2 events (Event Qualification A and B).

Note

The $\overline{TZn}$ signals, when used as a DCEVT tripping functions, are treated as a normal input signal and can be defined to be active-high or active-low inputs. ePWM outputs are asynchronously tripped when either the $\overline{TZn}$, DCAEVTx.force, or DCBEVTx.force signals are active. For the condition to remain latched, a minimum of 3 * TBCLK sync pulse width is required. If pulse width is < 3*TBCLK sync pulse width, the trip condition can or can not get latched by CBC or OST latches.

The DCAEVT1/2 and DCBEVT1/2 events can then be filtered to provide a filtered version of the event signals (DCEVTFILT) or the filtering can be bypassed. Filtering is discussed further in Event Filtering. Either the DCAEVT1/2 and DCBEVT1/2 event signals or the filtered DCEVTFILT event signals can generate a force to the trip zone module, a TZ interrupt, an ADC SOC, or a PWM sync signal.

- **force signal:** DCAEVT1/2.force signals force trip zone conditions which either directly influence the output on the EPWMxA pin (using TZCTL, TZCTLDCA, TZCTLDCB register configurations) or, if the DCAEVT1/2 signals are selected as one-shot or cycle-by-cycle trip sources (using the TZSEL register), the DCAEVT1/2.force signals can effect the trip action using the TZCTL or TZCTL2 register configurations. The DCBEVT1/2.force signals behaves similarly, but affect the EPWMxB output pin instead of the EPWMxA output pin.

  The priority of conflicting actions on the TZCTL, TZCTL2, TZCTLDCA and TZCTLDCB registers is as follows (highest priority overrides lower priority):

  Output EPWMxA:
  - TZA (highest) -> DCAEVT1 -> DCAEVT2 (lowest)
  - TZAU (highest) -> DCAEVT1U -> DCAEVT2U (lowest)
  - TZAD (highest) -> DCAEVT1D -> DCAEVT2D (lowest)

  Output EPWMxB:
  - TZB (highest) -> DCBEVT1 -> DCBEVT2 (lowest)
  - TZBU (highest) -> DCBEVT1U -> DCBEVT2U (lowest)
  - TZBD (highest) -> DCBEVT1D -> DCBEVT2D (lowest)
- **interrupt signal:** DCAEVT1/2.interrupt signals generate trip zone interrupts to the interrupt controller. To enable the interrupt, set the DCAEVT1, DCAEVT2, DCBEVT1, or DCBEVT2 bits in the TZEINT register. Once one of these events occurs, an EPWMxTZINT interrupt is triggered, and the corresponding bit in the TZCLR register must be set to clear the interrupt.
- **soc signal:** The DCAEVT1.soc signal interfaces with the event-trigger submodule and can be selected as an event which generates an ADC start-of-conversion-A (SOCA) pulse using the ETSEL[SOCASEL] bit. Likewise, the DCBEVT1.soc signal can be selected as an event which generates an ADC start-of-conversion-B (SOCB) pulse using the ETSEL[SOCBSEL] bit.
- **sync signal:** The DCAEVT1.sync and DCBEVT1.sync events are ORed with the EPWMxSYNCI input signal and the TBCTL[SWFSYNC] signal to generate a synchronization pulse to the time-base counter.

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25.11.4.2 Event Filtering

Blank Control Logic: The DCAEVT1/2 and DCBEVT1/2 events can be filtered using event filtering logic to remove noise by optionally blanking events for a certain period of time. This is useful for cases where the analog comparator outputs can be selected to trigger DCAEVT1/2 and DCBEVT1/2 events, and the blank control logic is used to filter out potential noise on the signal prior to tripping the PWM outputs or generating an interrupt or ADC start-of-conversion. Blank control logic is used to define a blanking window, which ignores all event occurrences on the signal while the window is active. The blanking window is configured in the DCFCTL, DCFOFFSET, and DCFWINDOW registers. The DCFCTL register enables the blanking window and aligns the blanking window to either a CTR = PRD pulse or a CTR = 0 pulse or both CTR = PRD and CTR = 0 as specified by DCFCTL[PULSESEL]. DCFCTL[SRCSEL] selects the DCxEVTy event source for the DCEVTFILT signal. An offset value in TBCLK counts is programmed into the DCFOFFSET register, which determines at what point after the CTR = PRD or CTR = 0 pulse the blanking window starts. The duration of the blanking window, in number of TBCLK counts after the offset counter expires, is written to the DCFWINDOW register by the application. Before and after the blanking window ends, events can generate soc, sync, interrupt, and force signals as before. Figure 25-51 shows the details of the event filtering logic.

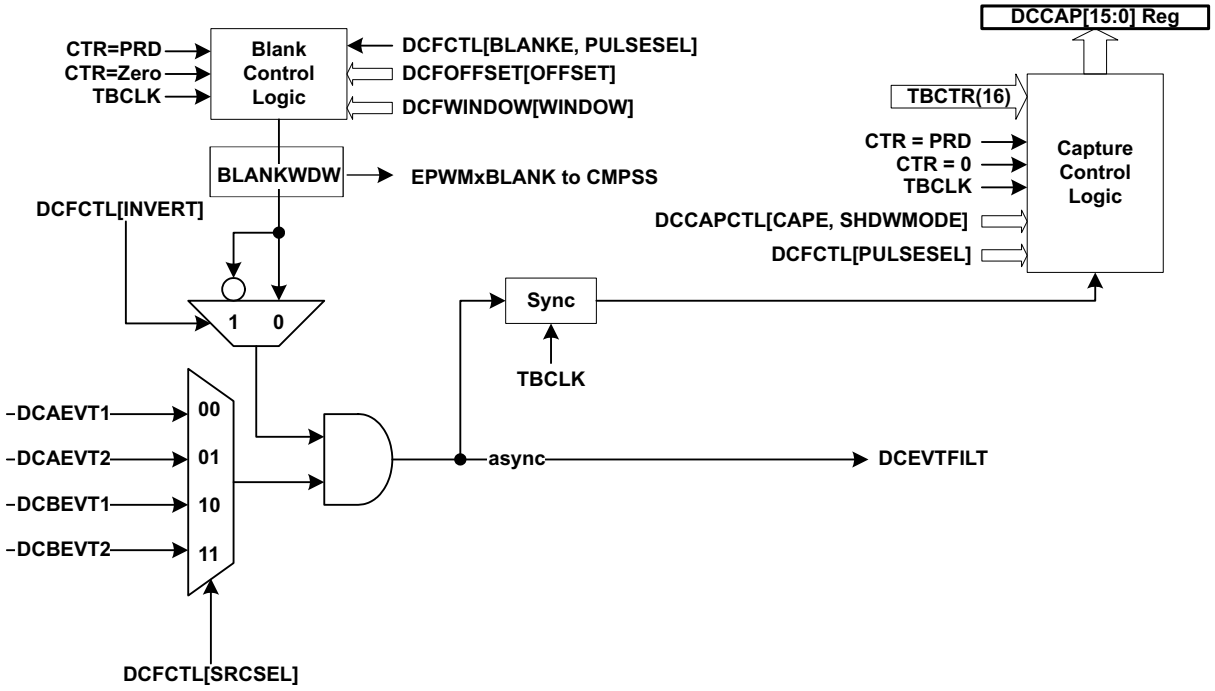


Figure 25-51. Event Filtering

Capture Control Logic: The event filtering can also capture the TBCTR value of the selected DCxEVTy event as configured in the DCCAPCTL register. When capture control logic is enabled, the selected DCxEVTy event triggers capture of the TBCTR to the active register. The CPU reads directly from the active register unless shadow mode is enabled by DCCAPCTL[SHDWMODE]. When shadow mode is enabled, the active register information is copied to shadow register on the event specified by DCFCCTL[PULSESEL], and the CPU reads from the shadow register. After the selected DCxEVTy event, no further capture events occur until the event specified by DCCAPCTL[CAPMODE]. The CAPMODE can be configured two ways: (1) no further capture events occur until the event defined by DCFCTL[PULSESEL] or (2) no further capture events occur until the compare-event flag at DCCAPCTL[CAPSTS] is cleared by DCCAPCTL[CAPCLR].

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25.11.4.3 Valley Switching

Event filtering depicts the valley switching function along with the event filtering logic described in Event Filtering. This function can be used to achieve programmable valley switching without any additional external circuitry. This module provides an on-chip hardware mechanism that can:

- Capture the oscillation period
- Accurately delay the PWM switching instant
- Allow a programmable number of edges before the delay takes effect
- Provide multiple choices of triggers and events
- Allow easy adaptability for optimum performance under changing system/operating conditions

The DCxEVTy signal needs further processing to support valley switching. Here is a brief description of how valley switching function is enabled:

1. Select one of the DCxEVTy events as input to the valley switching block (DCFCTL[SRCSEL]) with an option to add the blanking window (Blank Control Logic). This is where the comparator output (or external input) above is selected as an input to the valley switching block.
2. Configure the edge filter to capture ‘n’ rising, falling or both edges through the edge selection logic (DCFCTL[EDGEMODE, EDGECOUNT]).
3. Select the correct event to reset and restart the edge filter (VCAPCTL[TRIGSEL]). Edge capturing event is triggered or armed by this selected edge.
4. Enable valley capture logic (VCAPCTL[VCAPE]).
5. Select the start edge that indicates the start of capture for oscillation period measurement (VCNTCFG[STARTEDGE]). This is where the 16-bit counter starts counting.
6. Select the stop edge (VCNTCFG[STOPEDGE]) that indicates the edge at which the 16-bit counter stops counting. The captured counter value (CNTVAL) provides oscillation period information.
   - The STOPEDGE value must always be greater than STARTEDGE value.
7. Configure and apply the captured delay (CNTVAL) to the edge filtered DCxEVTy signal. The CNTVAL value can be applied as is or applied in conjunction with a software programmed value (useful for offset adjustment) (SWVDELVAL) or only a fraction of the delay can be applied with or without SWVDELVAL. This is useful to correctly apply a delay corresponding to the valley point. (VCAPCTL[VDELAYDIV])
8. Configure VCAPCTL[EDGEFILTDLYSEL] to apply hardware delay based on the captured value above.

Once the counter is stopped, counter value is copied into CNTVAL register and counter is reset to zero. No further captures are done until the logic is triggered again by occurrence of event selected by VCAPCTL[TRIGSEL]. In this implementation, the software trigger is used as the source for VCAPCTL[TRIGSEL]. Upon occurrence of the trigger event, irrespective of the current status of the counter, the counter is reset and starts counting from zero upon occurrence of the STARTEDGE. Similarly, upon occurrence of the trigger event, the edge filter is reset and starts counting from zero upon occurrence of the STARTEDGE.

Output from the valley switching block (DCEVTFILT) is then used to synchronize the PWM time-base. The process is shown in Figure 25-52.

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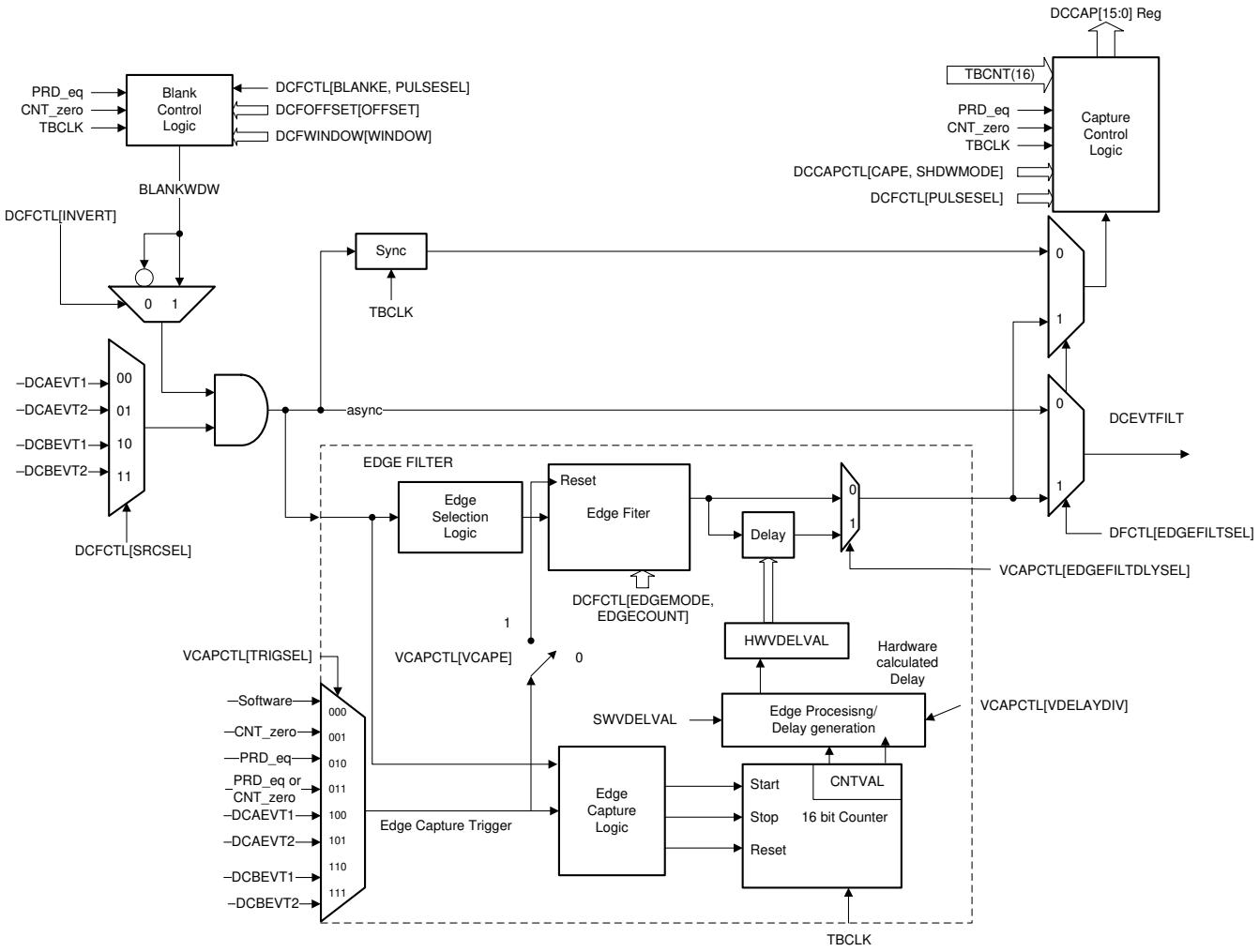


Figure 25-52. Valley Switching

25.12 PWM X-BAR

The ePWM Crossbar (X-BAR) enables selection of various trigger sources into specific dedicated EPWM trip inputs TRIPx. See Section 19.2 for more information on input selection options and PWM X-BAR / ePWM module connections.

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25.13 Applications to Power Topologies

An ePWM module has all the local resources necessary to operate completely as a standalone module or to operate in synchronization with other identical ePWM modules.

25.13.1 Overview of Multiple Modules

Previously in this chapter, all discussions have described the operation of a single module. To facilitate the understanding of multiple modules working together in a system, the ePWM module described in reference is represented by the more simplified block diagram shown in Figure 25-53. This simplified ePWM block shows only the key resources needed to explain how a multiswitch power topology is controlled with multiple ePWM modules working together.

Figure 25-53. Simplified ePWM Module

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25.13.2 Key Configuration Capabilities

The key configuration choices available to each module are as follows:

- Options for SyncIn
  - Load own counter with phase register on an incoming sync strobe—enable (EN) switch closed
  - Do nothing or ignore incoming sync strobe—enable switch open
  - Sync Source mode, provides a sync at PWM boundaries—SyncOut connected to CTR = PRD
  - Sync Source mode, provides a sync at any programmable point in time—SyncOut connected to CTR = CMPB
  - Module is in standalone mode and provides no sync to other modules—SyncOut connected to X (disabled)
- Options for SyncOut
  - Sync Source mode, provides a sync at PWM boundaries—SyncOut connected to CTR = PRD
  - Sync Source mode, provides a sync at any programmable point in time—SyncOut connected to CTR = CMPB
  - Module is in standalone mode and provides no sync to other modules—SyncOut connected to X (disabled)

For each choice of SyncOut, a module can also choose to load the counter with a new phase value on a SyncIn strobe input or choose to ignore the value (that is, by the enable switch). Although various combinations are possible, the two most common—Sync Source module and Sync Receiver module modes—are shown in Figure 25-54.

Figure 25-54. EPWM1 Configured as a Typical Sync Source, EPWM2 Configured as a Sync Receiver

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25.13.3 Controlling Dual 3-Phase Inverters for Motors (ACI and PMSM)

The idea of multiple modules controlling a single power stage can be extended to the 3-phase inverter case. In such a case, six switching elements are controlled using three PWM modules, one for each leg of the inverter. Each leg must switch at the same frequency and all legs must be synchronized. A sync receivers configuration easily addresses this requirement. Figure 25-55 shows how six PWM modules control two independent 3-phase inverters; each running a motor.

As in the cases shown in the previous sections, we have a choice of running each inverter at a different frequency (module 1 and module 4 are sync source as in Figure 25-55), or both inverters can be synchronized by using one sync source (module 1) and five sync receivers. In this case, the frequency of modules 4, 5, and 6 (all equal) can be integer multiples of the frequency for modules 1, 2, and 3 (also all equal).

Figure 25-55. Control of Dual 3-Phase Inverter Stages as Is Commonly Used in Motor Control

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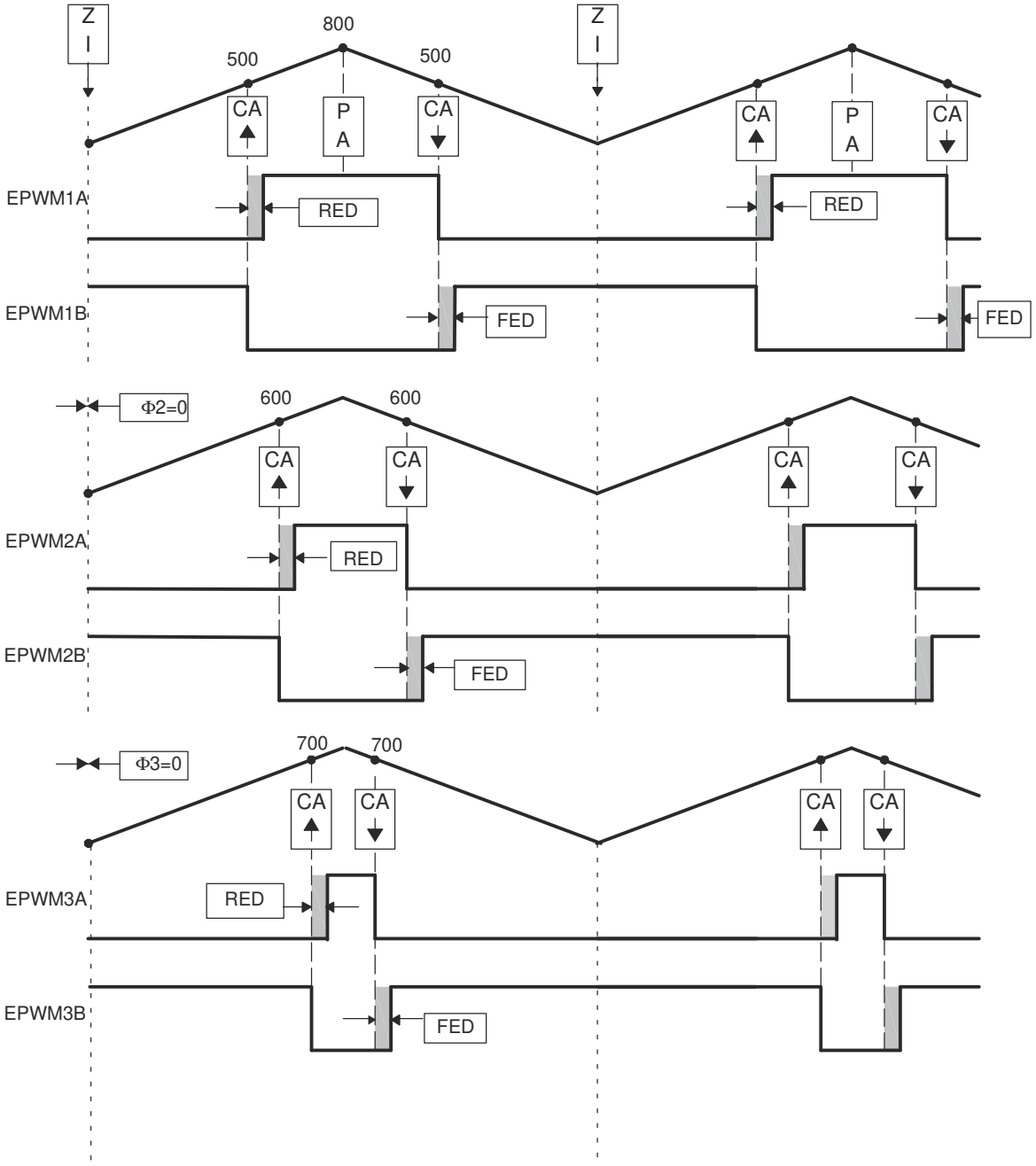


Figure 25-56. 3-Phase Inverter Waveforms for Control of Dual 3-Phase Inverter Stages (Only One Inverter Shown)

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25.14 High-Resolution Pulse Width Modulator (HRPWM)

Figure 25-57 shows a block diagram of the HRPWM. This module extends the time resolution capabilities of the conventionally derived digital pulse width modulator (PWM). HRPWM is typically used when PWM resolution falls below approximately 9-10 bits. The key features of HRPWM are:

- Extended time resolution capability
- Used in both duty cycle and phase-shift control methods
- Finer time granularity control or edge positioning using extensions to the Compare A, Compare B and Phase registers
- Implemented using the A and B signal path of PWM, that is, on the EPWMxA and EPWMxB output
- Dead band high-resolution control for falling and rising edge delay in half cycle clocking operation
- Self-check diagnostics software mode to check if the micro edge positioner (MEP) logic is running how designed
- Enables high-resolution output swapping on the EPWMxA and EPWMxB output
- Enables high-resolution output on EPWMxB signal output using inversion of EPWMxA signal output
- Enables high-resolution period, duty and phase control on the EPWMxA and EPWMxB output on devices with an ePWM module

Note

See the device data sheet to determine if your device has an ePWM module with high-resolution period support.

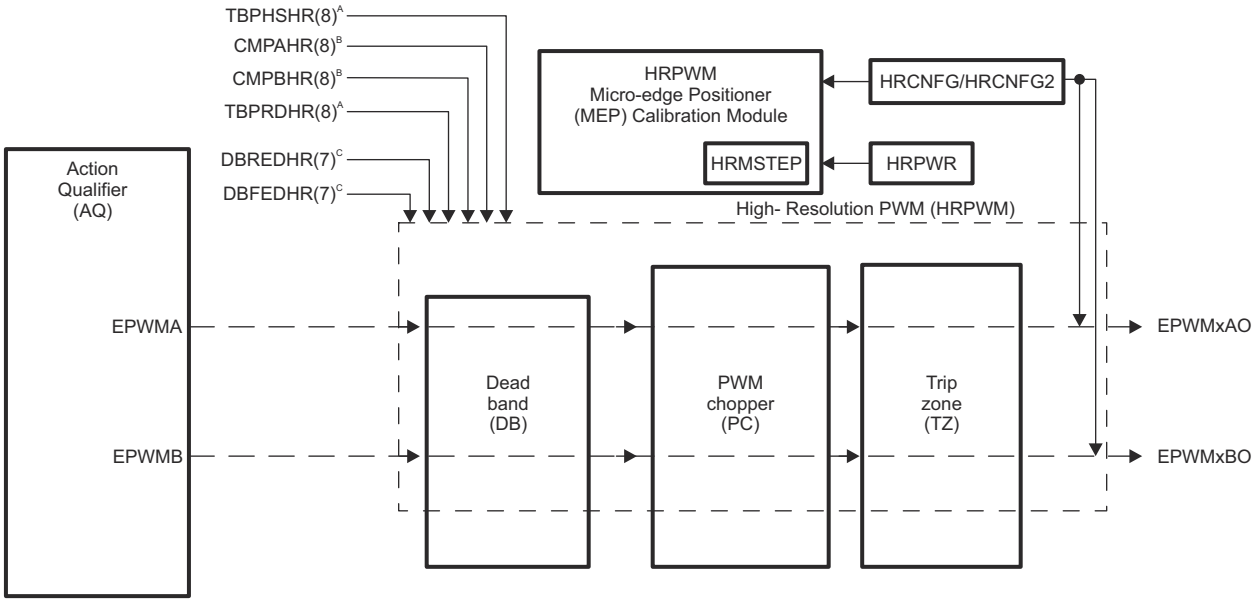


Figure 25-57. HRPWM Block Diagram

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The ePWM peripheral is used to perform a function mathematically equivalent to a digital-to-analog converter (DAC). As shown in Figure 25-58, the effective resolution for conventionally generated PWM is a function of PWM frequency (or period) and system clock frequency.

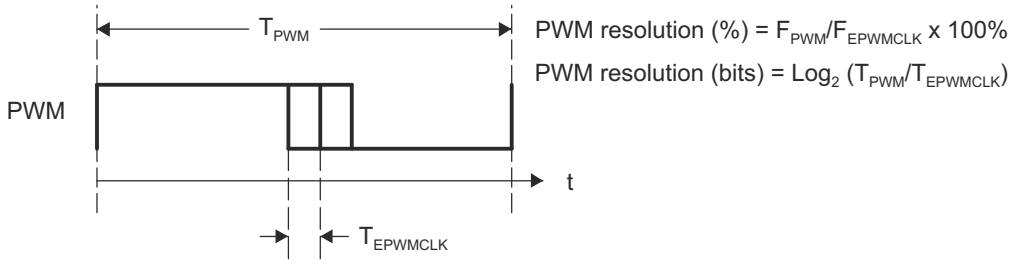


Figure 25-58. Resolution Calculations for Conventionally Generated PWM

If the required PWM operating frequency does not offer sufficient resolution in PWM mode, consider using HRPWM. As an example of improved performance offered by HRPWM, Table 25-14 shows resolution in bits for various PWM frequencies. These values assume a MEP step size of 180ps. See the device data sheet for typical and maximum performance specifications for the MEP.

Table 25-14. Resolution for PWM and HRPWM

PWM Frequency (kHz)	Regular Resolution (PWM) 100MHz EPWMCLK		High Resolution (HRPWM)	
	Bits	%	Bits	%
20	12.3	0.02	18.1	0.000
50	11	0.05	16.8	0.001
100	10	0.1	15.8	0.002
150	9.4	0.15	15.2	0.003
200	9	0.2	14.8	0.004
250	8.6	0.25	14.4	0.005
500	7.6	0.5	13.4	0.009
1000	6.6	1	12.4	0.018
1500	6.1	1.5	11.9	0.027
2000	5.6	2	11.4	0.036

Although each application can differ, typical low-frequency PWM operation (below 250kHz) does not require HRPWM. HRPWM capability is most useful for high-frequency PWM requirements of power conversion topologies such as:

- Single-phase buck, boost, and flyback
- Multiphase buck, boost, and flyback
- Phase-shifted full bridge
- Direct modulation of D-Class power amplifiers

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25.14.1 Operational Description of HRPWM

The HRPWM is based on micro-edge positioner (MEP) technology. MEP logic is capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. The time step accuracy is on the order of 150ps. See the device data sheet for the typical MEP step size on a particular device. The HRPWM also has a self-check software diagnostics mode to check if the MEP logic is running as designed under all operating conditions. Details on software diagnostics and functions are in Section 25.14.1.7 .

Figure 25-59 shows the relationship between one coarse system clock and edge position in terms of MEP steps, which are controlled using an 8-bit field in the Compare A extension register (CMPAHR). The same operating logic applies to CMPBHR as well.

To generate an HRPWM waveform, configure the ePWM registers to generate a conventional PWM of a given frequency and polarity. The HRPWM works together with the ePWM registers to extend edge resolution. Although many programming combinations are possible, only a few are needed and practical. These methods are described in Section 25.14.1.8 .

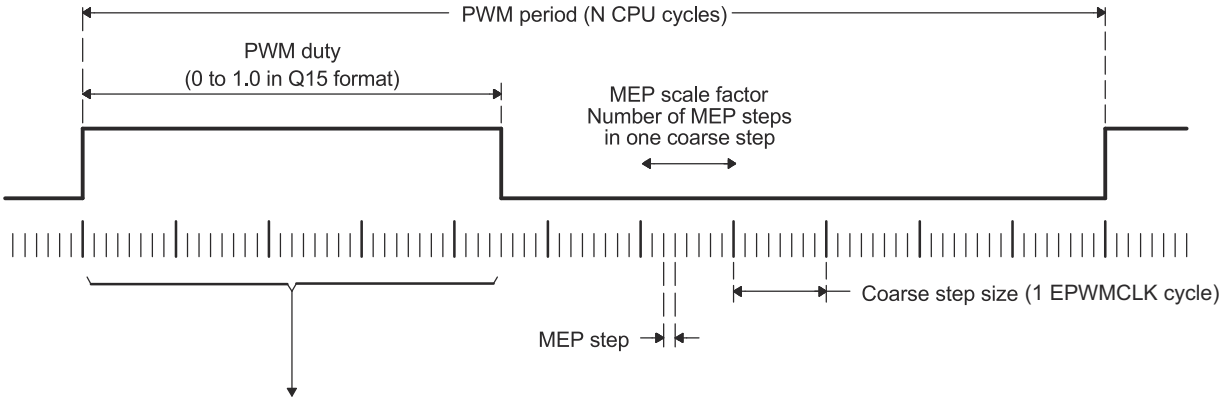


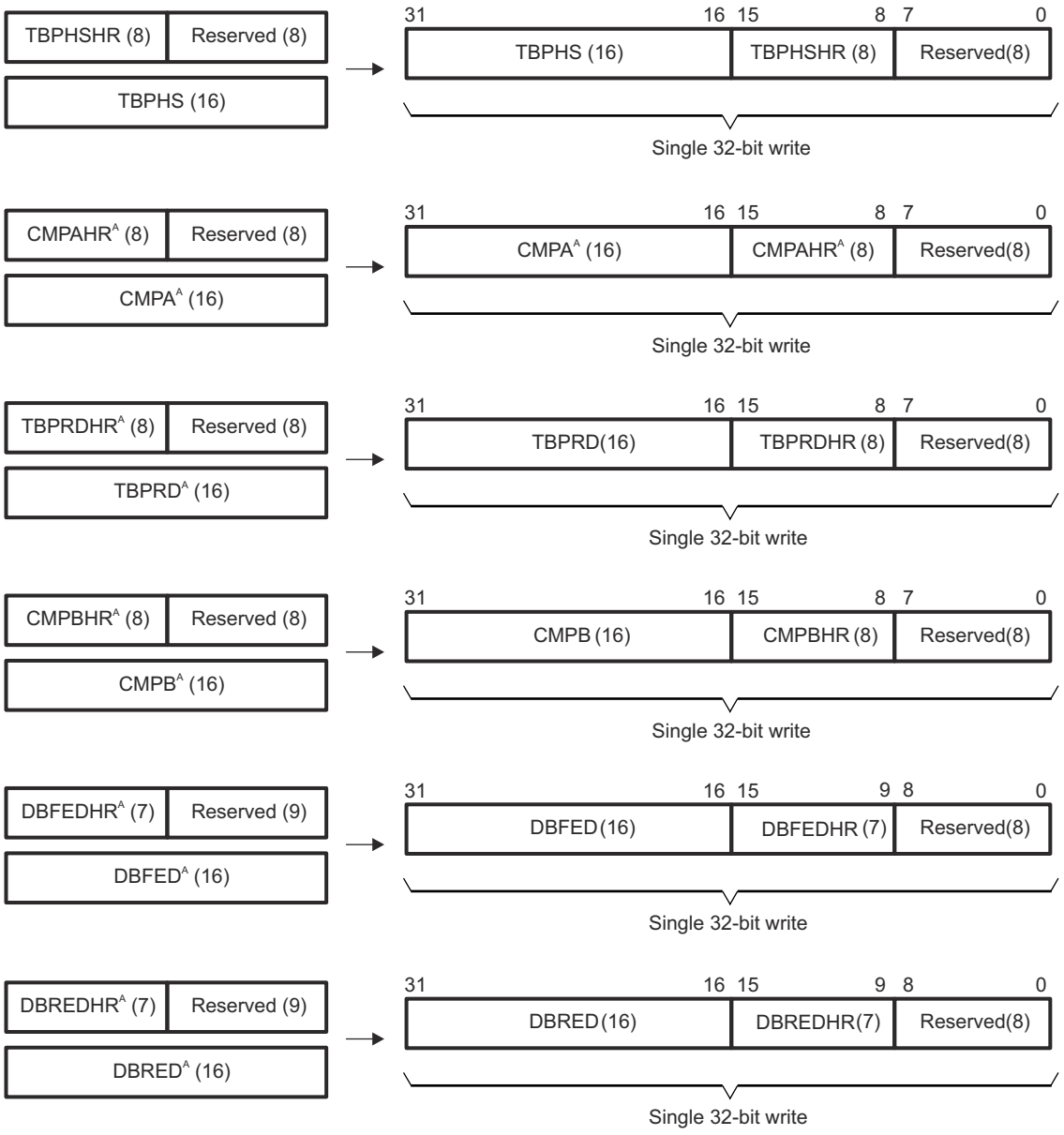
Figure 25-59. Operating Logic Using MEP

25.14.1.1 Controlling the HRPWM Capabilities

The MEP of the HRPWM is controlled by six extension registers. These HRPWM registers are concatenated with the 16-bit TBPHS, TBPRD, CMPA, CMPBM, DBREDM, and DBFEDM registers used to control PWM operation.

- TBPHSHR - Time Base Phase High Resolution Register
- CMPAHR - Counter Compare A High Resolution Register; CMPAHR is for use with the AQ output of Channel A, and is not related to CMPA
- TBPRDHR - Time Base Period High Resolution Register. (available on some devices)
- CMPBHR - Counter Compare B High Resolution Register; CMPBHR is for use with the AQ output of Channel B, and is not related to CMPB
- DBREDHR - Dead-band Generator Rising Edge Delay High Resolution Register
- DBFEDHR - Dead-band Generator Falling Edge Delay High Resolution Register

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Note

Dependent upon your device, these registers can be mirrored and can be written to at two different memory locations.

Figure 25-60. HRPWM Extension Registers and Memory Configuration

Note

HRPWM capabilities on Deadband Rising Edge Delay and Falling Edge Delay is applicable only during dead band half cycle clocking Operation. The number of MEP steps is half in size [bits 15:9] than duty and phase high-resolution registers for the same reason.

HRPWM capabilities are controlled using the Channel A and B PWM signal path. HRPWM support on the Dead band signal path is available by properly configuring the HRCNFG2 register. shows how the HRPWM interfaces with the 8-bit extension registers.

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25.14.1.2 HRPWM Source Clock

25.14.1.3 Configuring the HRPWM

Once the ePWM has been configured to provide conventional PWM of a given frequency and polarity, the HRPWM is configured by programming the HRCNFG register in that particular ePWM module's register space. This register provides the following configuration options:

Edge Mode The MEP can be programmed to provide precise position control on the rising edge (RE), falling edge (FE) or both edges (BE) at the same time. FE and RE are used for power topologies requiring duty cycle control (CMPA or CMPB high-resolution control), while BE is used for topologies requiring phase shifting, for example, phase shifted full bridge (TBPHS or TBPRD high-resolution control).

Control Mode The MEP is programmed to be controlled either from the CMPAHR/CMPBHR register in case of duty cycle control or the TBPHSHR register (phase control). RE or FE control mode can be used with the CMPAHR or CMPBHR register. BE control mode can be used with the TBPHSHR register. When the MEP is controlled from the TBPRDHR register (period control), the duty cycle and phase can also be controlled using the respective high-resolution registers.

Note

If TBPHSHR control mode is used, TBPHSHR applies the HR delay on the secondary PWM to the right from its original waveform irrespective of its counter mode and direction of counter after a sync event.

Shadow Mode This mode provides the same shadowing (double buffering) option as in regular PWM mode. This option is valid only when operating from the CMPAHR, CMPBHR, and TBPRDHR registers and can be chosen to be the same as the regular load option for the CMPA/CMPB register. If TBPHSHR is used, then this option has no effect.

High-Resolution B Signal Control The B signal path of an ePWM channel can generate a high-resolution output by outputting an inverted version of the high-resolution ePWMxA signal on the ePWMxB pin. A Type 2 or Type 4 HRPWM module can also enable high-resolution features on the B signal path independently of the A signal path as well.

Swap ePWMxA and ePWMxB Outputs This mode enables the swapping of the high-resolution A and B outputs. The mode selection allows either A and B Outputs Unchanged or A Output Comes Out On B and B Output Comes Out On A.

Auto-conversion Mode This mode is used in conjunction with the scale factor optimization (SFO) software only. For a type 4 HRPWM module, below is a description of the Auto-conversion Mode taking CMPAHR as an example. If auto-conversion is enabled, CMPAHR = fraction(PWMduty * PWMperiod)<<8. The scale factor optimization software calculates the MEP scale factor in the background code and automatically updates the HRMSTEP register with the calculated number of MEP steps per coarse step. The MEP Calibration Module then uses the values in the HRMSTEP and CMPAHR registers to automatically calculate the appropriate number of MEP steps represented by the fractional duty cycle and moves the high-resolution ePWM signal edge accordingly. If auto-conversion is disabled, the CMPAHR register behaves like a type 0 HRPWM module and CMPAHR = (fraction(PWMduty * PWMperiod) * MEP Scale Factor + 0.5)<<8). All calculations need to be performed by your code in this mode, and the HRMSTEP register is ignored. Auto-conversion for high-resolution period has the same behavior as auto-conversion for high-resolution duty cycle. Auto-conversion must always be enabled for high-resolution period mode.

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Note

If the HRPWM module is configured in UP-DOWN counter mode, the shadow mode for the HRPWM registers must be set to load on both ZERO AND PERIOD. New values from the user are loaded to the shadow registers only at CTR = ZERO, but the shadow mode of for the registers must be set to both ZERO AND PERIOD. The CTR = PRD event is used for specific internal logic inside the HRPWM module.

Auto-conversion Mode performs the calculation for CMPBHR , DBREDHR, and DBFEDHR. The scale factor optimization software calculates the MEP scale factor in the background code and automatically updates the HRMSTEP register with the calculated number of MEP steps per coarse step. The MEP Calibration Module then uses the values in the HRMSTEP and CMPBHR or DBREDHR/DBFEDHR register to automatically calculate the appropriate number of MEP steps represented by the fractional components and moves the high-resolution ePWM signal edge accordingly. If auto-conversion is disabled, CMPBHR behaves the same as CMPAHR. CMPBHR = (fraction(PWMduty ˣ PWMperiod) ˣ MEP Scale Factor + 0.5)<<8).

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25.14.1.4 Configuring High-Resolution in Deadband Rising-Edge and Falling-Edge Delay

Once the ePWM has been configured to provide conventional PWM of a given frequency, polarity, and dead band enabled in half-cycle clocking mode, the high-resolution operation on dead band RED and FED lines are enabled by programming the HRCNFG2 register in that particular ePWM module register space. This register provides the following configuration options:

Edge Mode The MEP can be programmed to provide precise position control on the dead band rising edge (RED), dead band falling edge (FED), or both edges (rising edge of DBRED signal and falling edge of DBFED signal) at the same time.

Control Mode Selects the time event that loads the shadow value in the active register for DBRED and DBFED in high-resolution mode. Select the pulse to match the selection in the ePWM DBCTL[LOADREDMODE] and DBCTL[LOADFEDMODE] bits.

25.14.1.5 Principle of Operation

The MEP logic is capable of placing an edge in one of 255 (8 bits) discrete time steps (see the device data sheet for typical MEP step size). The MEP works with the TBM and CCM registers to be certain that time steps are applied and that edge placement accuracy is maintained over a wide range of PWM frequencies, system clock frequencies, and other operating conditions. Table 25-15 shows the typical range of operating frequencies supported by the HRPWM.

Table 25-15. Relationship Between MEP Steps, PWM Frequency, and Resolution

System (MHz)	MEP Steps Per EPWMCLK (1)(2)(3)	PWM Minimum (Hz) (4)	PWM Maximum (MHz)	Resolution at Maximum (Bits) (5)
60.0	93	916	3.00	10.9
70.0	79	1068	3.50	10.6
80.0	69	1221	4.00	10.4
90.0	62	1373	4.50	10.3
100.0	56	1526	5.00	10.1

(1) TBCLK = EPWMCLK.
(2) Table data based on a MEP time resolution of 180ps (this is an example value. See the device data sheet for MEP limits)
(3) MEP steps applied = $T_{EPWMCLK}$/180ps in this example.
(4) PWM minimum frequency is based on a maximum period value,(TBPRD = 65535). PWM mode is asymmetrical up-count.
(5) Resolution in bits is given for the maximum PWM frequency stated.

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25.14.1.5.1 Edge Positioning

Note

The following example is presented using the [CMPA:CMPAHR] register combination. The theory of operation and equations are the same, if intending to use the [CMPBM:CMPBHRM] for duty cycle control.

In a typical power control loop, a digital controller issues a duty command, usually expressed in a per unit or percentage terms. Assume that for a particular operating point, the demanded duty cycle is 0.405 or 40.5% on time and the required converter PWM frequency is 1.25MHz. In conventional PWM generation with a system clock of 100MHz, the duty cycle choices are in the vicinity of 40.5%. As shown in Figure 25-61, a compare value of 32 counts (duty = 40%) is the closest to 40.5% that can be attained. This is equivalent to an edge position of 320ns instead of the desired 324ns. This data is shown in Table 25-16.

By utilizing the MEP, an edge position much closer to the desired point of 324ns can be achieved. Table 25-16 shows that in addition to the CMPA value, 22 steps of the MEP (CMPAHR register) positions the edge at 323.96ns, resulting in almost zero error. In this example, assume that the MEP has a step resolution of 180ps.

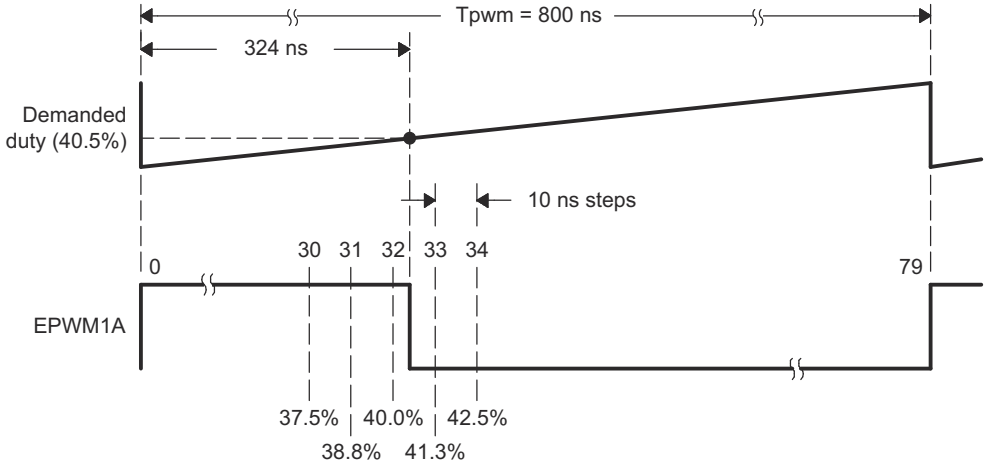


Figure 25-61. Required PWM Waveform for a Requested Duty = 40.5%

Table 25-16. CMPA versus Duty (left), and [CMPA:CMPAHR] versus Duty (right)

CMPA (count)(1)(2) (3)	Duty (%)	High Time (ns)	CMPA (count)	CMPAHR (count)	Duty (%)	High Time (ns)
28	***35.0***	280	32	18	***40.405***	323.24
29	***36.3***	290	32	19	***40.428***	323.42
30	***37.5***	300	32	20	***40.450***	323.60
31	***38.8***	310	32	21	***40.473***	323.78
32	***40.0***	320	32	22	***40.495***	323.96
33	***41.3***	330	32	23	***40.518***	324.14
34	***42.5***	340	32	24	***40.540***	324.32
			32	25	***40.563***	324.50
Required			32	26	***40.585***	324.68
32.40	***40.5***	324	32	27	***40.608***	324.86

(1) Assumed MEP step size for the above example = 180ps. See the device-specific data sheet for typical and maximum MEP values.
(2) TBCLK = 100MHz, 10ns
(3) For a PWM Period register value of 80 counts, PWM Period = 80 * 10ns = 800ns, PWM frequency = 1/800ns = 1.25MHz

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25.14.1.5.2 Scaling Considerations

The mechanics of how to position an edge precisely in time has been demonstrated using the resources of the standard CMPA and MEP (CMPAHR) registers. In a practical application, however, it is necessary to seamlessly provide the CPU a mapping function from a per-unit (fractional) duty cycle to a final integer (non-fractional) representation that is written to the [CMPA:CMPAHR] register combination.

To do this, first examine the scaling or mapping steps involved. It is common in control software to express duty cycle in a per-unit or percentage basis. This has the advantage of performing all needed math calculations without concern for the final absolute duty cycle, expressed in clock counts or high time in nanoseconds (ns). Furthermore, it makes the code more transportable across multiple converter types running different PWM frequencies.

To implement the mapping scheme, a two-step scaling procedure is required.

Assumptions for this example:

TBCLK	=	10ns (100MHz)
PWM frequency	=	1.25MHz (1/800ns)
Required PWM duty cycle, **PWMDuty**	=	0.405 (40.5%)
PWM period in terms of coarse steps, **PWMPeriod** (800ns/10ns)	=	80
Number of MEP steps per coarse step at 180ps (10ns/180ps), **MEP_ScaleFactor**	=	55
Value to keep CMPAHR within the range of 1-255 and fractional rounding constant (default value)	=	0.5 (0080h in Q8 format)

Step 1: Percentage Integer Duty value conversion for CMPA register

CMPA register value	=	int(**PWMDuty***PWMPeriod**); int means integer part
	=	int(0.405 * 80)
	=	int(32.4)
CMPA register value	=	32 (20h)

Step 2: Fractional value conversion for CMPAHR register

CMPAHR	=	(frac(**PWMDuty***PWMPeriod**)*MEP_ScaleFactor** + 0.5) <<8); frac means fractional part
	=	(frac(32.4) * 55 + 0.5) <<8; Shifting is to move the value to the high byte of CMPAHR.
	=	(0.4 * 55 + 0.5) <<8
	=	(22 + 0.5) <<8
	=	22.5 * 256; Shifting left by 8 is the same as multiplying by 256.
	=	5760 (1680h)
CMPAHR	=	1680h CMPAHR value = 1600h (lower 8 bits are ignored by hardware).

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Note

If the AUTOCONV bit (HRCNFG.6) is set and the MEP_ScaleFactor is in the HRMSTEP register, then CMPAHR / CMPBHR register value = frac (PWMDuty*PWMperiod<<8). The rest of the conversion calculations are performed automatically in hardware, and the correct MEP-scaled signal edge appears on the ePWM channel output. If AUTOCONV is not set, the above calculations must be performed by software.

The MEP scale factor (MEP_ScaleFactor) varies with the system clock and DSP operating conditions. TI provides an MEP scale factor optimizing (SFO) software C function, which uses the built in diagnostics in each HRPWM and returns the best scale factor for a given operating point.

The scale factor varies slowly over a limited range so the optimizing C function can be run very slowly in a background loop.

The CMPA, CMPB, CMPAHR and CMPBHR registers are configured in memory so that the 32-bit data capability of the CPU can write this as a single concatenated value, that is, [CMPA:CMPAHR], [CMPB:CMPBHR], and so on.

The mapping scheme has been implemented in both C and assembly, as shown in Section 25.14.1.8 . The actual implementation takes advantage of the 32-bit CPU architecture and is somewhat different from the steps shown in Section 25.14.1.5.2 .

For time-critical control loops where every cycle counts, the assembly version is recommended. This is a cycle optimized function (11 EPWMCLK cycles) that takes a Q15 duty value as input and writes a single [CMPA:CMPAHR] value.

25.14.1.5.3 Duty Cycle Range Limitation

In high-resolution mode, the MEP is not active for 100% of the PWM period and becomes operational:

- Three EPWMCLK cycles after the period starts when high-resolution period (TBPRDHR) control is not enabled.
- When high-resolution period (TBPRDHR) control is enabled using the HRPCTL register:
  - In up-count mode: three EPWMCLK cycles after the period starts until three EPWMCLK cycles before the period ends.
  - In up-down count mode: when counting up, three cycles after CTR = 0 until three cycles before CTR = PRD, and when counting down, three cycles after CTR = PRD until three cycles before CTR = 0.
- When using DBREDHR or DBFEDHR, DBRED or DBFED (the register corresponding to the edge with high-resolution displacement) must be greater than or equal to 7.

Duty cycle range limitations are illustrated in Figure 25-62 to Figure 25-65. This limitation imposes a duty cycle limit on the MEP. For example, precision edge control is not available all the way down to 0% duty cycle. When high-resolution period control is disabled, regular PWM duty control is fully operational down to 0% duty cycle despite the unavailability of HRPWM features in the first three cycles. In most applications, this cannot be an issue as the controller regulation point is usually not designed to be close to 0% duty cycle. To better understand the useable duty cycle range, see Table 25-17. When high-resolution period control is enabled (HRPCTL[HRPE] = 1), the duty cycle must not fall within the restricted range; otherwise, there can be undefined behavior on the ePWMxA output.

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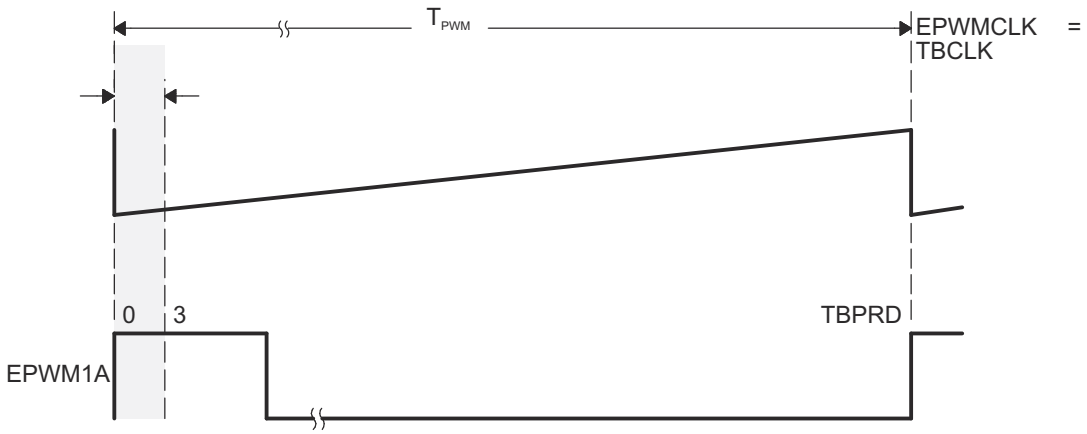


Figure 25-62. Low % Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 0)

Table 25-17. Duty Cycle Range Limitation for Three EPWMCLK/TBCLK Cycles

PWM Frequency(1) (kHz)	3 Cycles Minimum Duty	3 Cycles Maximum Duty(2)
200	0.6%	99.4%
400	1.2%	98.8%
600	1.8%	98.2%
800	2.4%	97.6%
1000	3%	97%
1200	3.6%	96.4%
1400	4.2%	95.8%
1600	4.8%	95.2%
1800	5.4%	94.6%
2000	6%	94%

(1) EPWMCLK = TBCLK = 100MHz

(2) This limitation applies only if high-resolution period (TBPRDHR) control is enabled.

If the application demands HRPWM operation below the minimum duty cycle limitation, then the HRPWM can be configured to operate in count-down mode with the rising edge position (REP) controlled by the MEP when high-resolution period is disabled (HRPCTL[HRPE] = 0). This is illustrated in Figure 25-63. In this configuration, the minimum duty cycle limitation is no longer an issue. However, there is a maximum duty limitation with same percent numbers as given in Table 25-17.

CAUTION

If the application has enabled high-resolution period control (HRPCTL[HRPE] = 1), the duty cycle must not fall within the restricted range; otherwise, there can be undefined behavior on the ePWM output.

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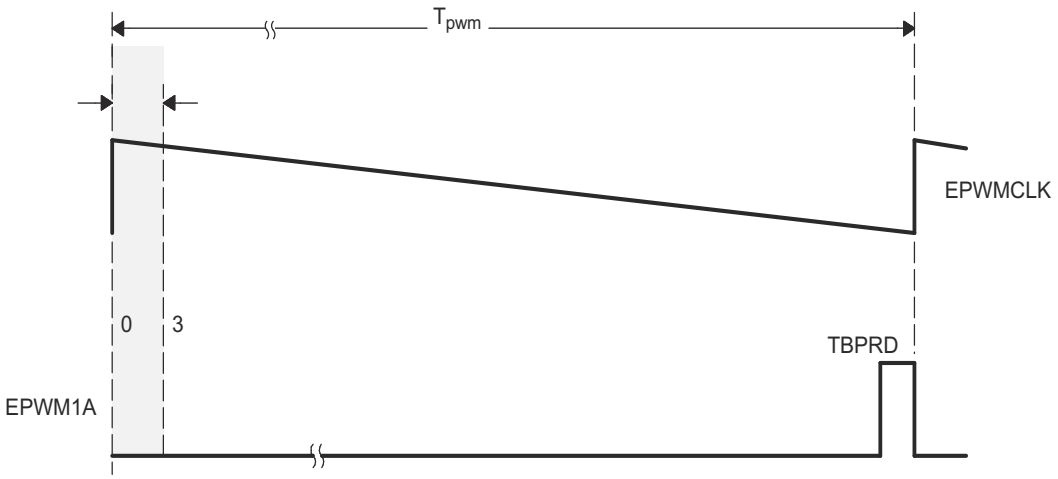


Figure 25-63. High % Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 0)

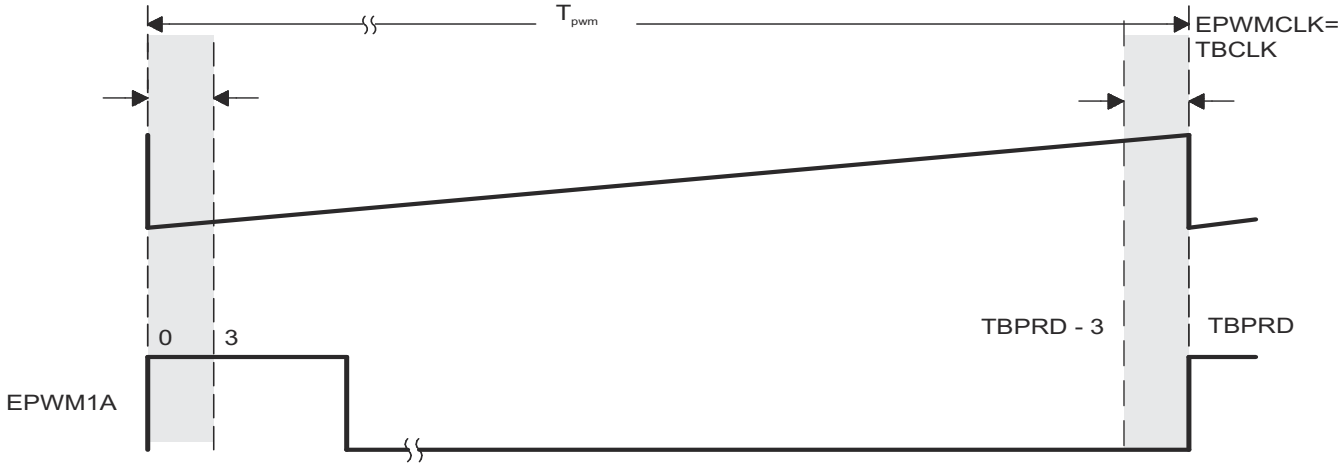


Figure 25-64. Up-Count Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 1)

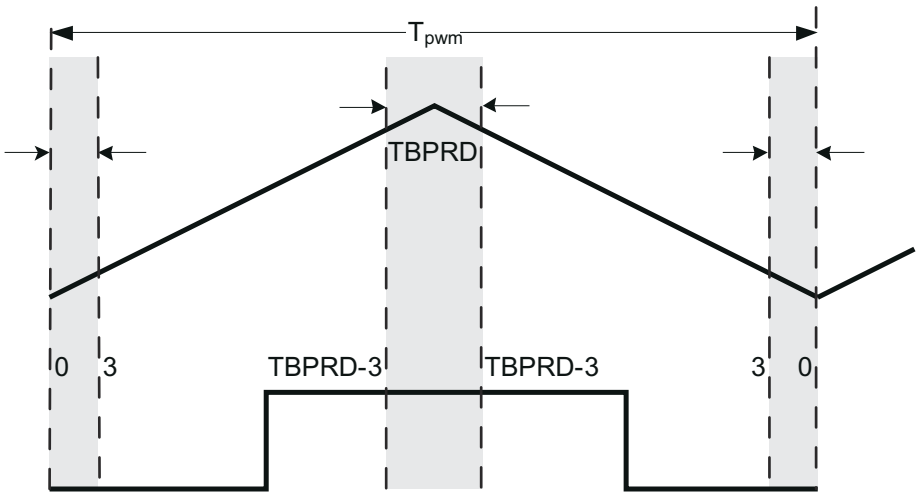


Figure 25-65. Up-Down Count Duty Cycle Range Limitation Example (HRPCTL[HRPE] = 1)

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25.14.1.5.4 High-Resolution Period

High-resolution period control using the MEP logic is supported on devices with a Type 1 ePWM module or greater.

Note

When high-resolution period control is enabled, on ePWMxA only, and not ePWMxB output and conversely, the non high-resolution output has ±1 TBCLK cycle jitter in up-count mode and ±2 TBCLK cycle jitter in up-down count mode.

One-shot load mode must not be used when high-resolution mode is enabled.

When high-resolution period is enabled (HRPCTL[HRPE] = 1) and shadow-to-active loading is configured to load on a sync event (TBCTL2[PRDLDSYNC] = 0x1 or 0x2), the load happens every ZERO event instead of the sync event. Refer to the device-specific errata for a work around.

The scaling procedure described for duty cycle in Section 25.14.1.5.2 applies for high-resolution period as well:

Assumptions for this example:

TBCLK	= 10ns (100MHz)
Required PWM frequency	= 175kHz (period of 571.428)
Number of MEP steps per coarse step at 180ps (10ns/180ps), (MEP_ScaleFactor)	= 55
Value to keep TBPRDHR within range of 1-255 and fractional rounding constant (default value)	= 0.5 (0080h in Q8 format)

Problem:

In up-count mode:

- If TBPRD = 571, then PWM frequency = 174.82kHz (period = (571 + 1) × T_{TBCLK}).
- If TBPRD = 570, then PWM frequency = 175.13kHz (period = (570 + 1) × T_{TBCLK}).

In up-down count mode:

- If TBPRD = 286, then PWM frequency = 174.82kHz (period = (286 × 2) × T_{TBCLK}).
- If TBPRD = 285, then PWM frequency = 175.44kHz (period = (285 × 2) × T_{TBCLK}).

Solution:

With 55 MEP steps per coarse step at 180ps each:

Step 1: Percentage Integer Period value conversion for TBPRD register

Integer period value	= 571 × T_{TBCLK}
	= int (571.428) × T_{TBCLK}
	= int (PWMperiod) × T_{TBCLK}
In up-count mode:	
TBPRD	= 570 (TBPRD = period value - 1)
	= 023Ah
In up-down count mode:	= 285 (TBPRD = period value/2)
TBPRD	= 011Dh

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Step 2: Fractional value conversion for TBPRDHR register

In up-count mode:

TBPRDHR register value	= (frac(PWMperiod) * MEP_ScaleFactor + 0.5)
If auto-conversion enabled and HRMSTEP =	
MEP_ScaleFactor value (55):	= frac (PWMperiod) << 8 (Shifting is to move the value to the high byte of TBPRDHR)
TBPRDHR register value	= frac (571.428) << 8
	= 0.428 * 256
	= 6D00h
The auto-conversion then automatically performs the calculation, such that TBPRDHR MEP delay is scaled by hardware to:	= ((TBPRDHR(15:0) >> 8) × HRMSTEP + 80h) << 8
	= (006Dh * 55 + 80h) >> 8
	= (17EBh) >> 8
Period MEP delay	= 0017h MEP Steps

In up-down count mode:

TBPRDHR register value	= (frac(PWMperiod) * MEP_ScaleFactor + 0.5)
If auto-conversion enabled and HRMSTEP =	
MEP_ScaleFactor value (55):	= frac (PWMperiod / 2) << 8 (Shifting is to move the value to the high byte of TBPRDHR)
TBPRDHR register value	= frac (285.714) << 8
	= 0.714 * 256
	= B600h
The auto-conversion then automatically performs the calculation, such that TBPRDHR MEP delay is scaled by hardware to:	= ((TBPRDHR(15:0) >> 8) × HRMSTEP + 80h) << 8
	= (00B6h * 55 + 80h) >> 8
	= (279Ah) >> 8
Period MEP delay	= 0027h MEP Steps

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25.14.1.5.4.1 High-Resolution Period Configuration

To use high-resolution period, the ePWMx module must be initialized in the exact order presented.

The following steps use CMPA with shadow registers and the corresponding HRCNFG bits for high-resolution operation on EPWMxA. For high-resolution operation on EPWMxB, make the appropriate substitutions with the B channel fields.

1. Enable ePWMx clock
2. Enable HRPWM clock
3. Disable TBCLKSYNC
4. Configure ePWMx registers - AQ, TBPRD, CC, and so on.
   - ePWMx can only be configured for up-count or up-down count modes. High-resolution period is not compatible with down-count mode.
   - TBPRD and CC registers must be configured for shadow loads.
   - CMPCTL[LOADAMODE]
     - In up-count mode: CMPCTL[LOADAMODE] = 1 (load on CTR = PRD)
     - In up-down count mode: CMPCTL[LOADAMODE] = 2 (load on CTR = 0 or CTR = PRD)
5. Configure the HRCNFG register such that:
   - HRCNFG[HRLOAD] = 2 (load on either CTR = 0 or CTR = PRD)
   - HRCNFG[AUTOCONV] = 1 (Enable auto-conversion)
   - HRCNFG[EDGMODE] = 3 (MEP control on both edges)
6. For TBPHS:TBPHSHR synchronization with high-resolution period, set both HRPCTL[TBPSHRLOADE] = 1 and TBCTL[PHSEN] = 1. In up-down count mode these bits must be set to 1 regardless of the contents of TBPHSHR.
7. Enable high-resolution period control (HRPCTL[HRPE] = 1)
8. Enable TBCLKSYNC
9. TBCTL[SWFSYNC] = 1
10. HRMSTEP must contain an accurate MEP scale factor (# of MEP steps per EPWMCLK coarse step) because auto-conversion is enabled. The MEP scale factor can be acquired using the SFO() function.
11. To control high-resolution period, write to the TBPRDHR(M) registers.

Note

When high-resolution period mode is enabled, an EPWMxSYNC pulse introduces ±1-2 cycle jitter to the PWM (±1 cycle in up-count mode and ±2 cycle in up-down count mode). Otherwise, the jitter occurs on every PWM cycle with the synchronization pulse.

When a software synchronization pulse can be issued only once during high-resolution period initialization. If a software sync pulse is applied while the PWM is running, the jitter appears on the PWM output at the time of the sync pulse.

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25.14.1.6 Deadband High-Resolution Operation

Note

In up-count mode, the dead-band module is not available when any high-resolution mode is enabled.

Assumptions for this example:

System clock	= 10ns (100MHz)
Deadband enabled in half-cycle mode, TBCLK = EPWMCLK	
Required PWM frequency	1.33MHz (1/750ns)
Required PWM duty cycle	0.5 (50%)
Required Deadband Rising-Edge Delay	5% over duty
Required Deadband Rising-Edge Delay in ns	(0.05 * 375ns) = 18.75ns

Note

Similar to the duty cycle restrictions when using HRPWM, the DBRED and DBFED values must be greater than 3 to use high-resolution deadband.

Deadband delay values as a function of DBFED and DBRED:

When half-cycle clocking is enabled, the formula to calculate the falling-edge delay (FED) and rising-edge delay (RED) becomes:

FED = DBFED * TBCLK / 2

RED = DBRED * TBCLK / 2

DBRED and DBFED calculated values:

Required Deadband Rising-Edge Delay in ns = 18.75ns

DBRED = RED / (TBCLK / 2)

DBRED = 18.75ns/5ns

DBRED Required = 3.75ns

With 55 MEP steps per coarse step at 180ps each:

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Step 1: Integer Deadband value conversion for DBREDM register

Integer DBRED value	= int (RED / (TBCLK / 2))
	= int (3.75)
DBRED	= 3

Step 2: Fractional value conversion for Deadband high-resolution register DBREDHR

DBREDHR register value	= (frac(DBRED Required) * MEP_ScaleFactor + 0.5) << 8 (Shifting is to move the value to the high byte of DBREDHR)
	= (frac (3.75) * 55 + 0.5) << 8
	= (0.75 * 55 + 0.5) << 8
	= (41.75) * 256 Shifting left by 8 is the same as multiplying by 256.
DBREDHR value	= 29C0h MEP Steps
	Hardware ignores lower 9 bits in the above calculated DBREDHR value

Note

If the AUTOCONV bit (HRCNFG.6) is set and the MEP_ScaleFactor is in the HRMSTEP register, then DBREDHR:DBRED = frac((required DB value) < <8). The rest of the conversion calculations are performed automatically in hardware, and the correct MEP-scaled signal edge appears on the ePWM channel output. If AUTOCONV is not set, the above calculations must be performed by software.

25.14.1.7 Scale Factor Optimizing Software (SFO)

The micro edge positioner (MEP) logic is capable of placing an edge in one of 255 discrete time steps. As previously mentioned, the size of these steps is on the order of 150ps (see the device data sheet for typical MEP step size on your device). The MEP step size varies based on worst-case process parameters, operating temperature, and voltage. MEP step size increases with decreasing voltage and increasing temperature and decreases with increasing voltage and decreasing temperature. Applications that use the HRPWM feature can use the TI-supplied MEP scale factor optimization (SFO) software function. The SFO function helps to dynamically determine the number of MEP steps per EPWMCLK period while the HRPWM is in operation.

To utilize the MEP capabilities effectively, the correct value for the MEP scaling factor needs to be known by the software. To accomplish this, the HRPWM module has built in self-check and diagnostic capabilities that can be used to determine the optimum MEP scale factor value for any operating condition. TI provides a C-callable library containing one SFO function that utilizes this hardware and determines the optimum MEP scale factor. As such, MEP control and diagnostics registers are reserved for TI use.

A detailed description of the SFO library - SFO_TI_Build_V8.lib software can be found in SFO Library Software - SFO TI_Build_V8.lib.

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25.14.1.8 HRPWM Examples Using Optimized Assembly Code

The best way to understand how to use the HRPWM capabilities is through two real examples:

1. Simple buck converter using asymmetrical PWM (count-up) with active high polarity.
2. DAC function using simple R+C reconstruction filter.

The following examples all have initialization and configuration code written in C. To make these easier to understand, the #defines shown below are used.

Section 25.14.1.8.1 assumes MEP step size of 150ps and does not use the SFO library.

#Defines for HRPWM Header Files

```
// HRPWM (High Resolution PWM) //
================================
// HRCNFG
#define HR_Disable 0x0
#define HR_REP 0x1          // Rising Edge position
#define HR_FEP 0x2          // Falling Edge position
#define HR_BEP 0x3          // Both Edge position #define HR_CMP 0x0 // CMPAHR controlled
#define HR_PHS 0x1          // TBPHSHR controlled #define HR_CTR_ZERO 0x0 // CTR = Zero event
#define HR_CTR_PRD 0x1      // CTR = Period event
#define HR_CTR_ZERO_PRD 0x2 // CTR = ZERO or Period event
#define HR_NORM_B  0x0      // Normal ePWMxB output
#define HR_INVERT_B 0x1     // ePWMxB is inverted ePWMxA output
```

25.15 EPWM Interrupts & Triggers

25.15.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 25-18. CPU Interrupts Triggered by EPWM

NVIC Interrupt Name	Peripheral Instance Name	Register Group	EPWM Interrupt Configuration Registers	Description
EPWM0_INT	EPWM0	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM0 event interrupt. Single, configurable source condition.
EPWM0_TZ_INT	EPWM0	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM0 trip zone interrupt. Multiple OR'd, configurable source conditions.
EPWM1_INT	EPWM1	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM1 event interrupt. Single, configurable source condition.
EPWM1_TZ_INT	EPWM1	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM1 trip zone interrupt. Multiple OR'd, configurable source conditions.
EPWM2_INT	EPWM2	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM2 event interrupt. Single, configurable source condition.
EPWM2_TZ_INT	EPWM2	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM2 trip zone interrupt. Multiple OR'd, configurable source conditions.

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Table 25-18. CPU Interrupts Triggered by EPWM (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	EPWM Interrupt Configuration Registers	Description
EPWM3_INT	EPWM3	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM3 event interrupt. Single, configurable source condition.
EPWM3_TZ_INT	EPWM3	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM3 trip zone interrupt. Multiple OR'd, configurable source conditions.
EPWM4_INT	EPWM4	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM4 event interrupt. Single, configurable source condition.
EPWM4_TZ_INT	EPWM4	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM4 trip zone interrupt. Multiple OR'd, configurable source conditions.
EPWM5_INT	EPWM5	N/A	ETSEL.INTSEL, ETSEL.INTEN, ETFLG.INT, ETFRC.INT, ETCLR.INT	EPWM5 event interrupt. Single, configurable source condition.
EPWM5_TZ_INT	EPWM5	N/A	TZSEL, TZEINT, TZFLG, TZFRC, TZCLR	EPWM5 trip zone interrupt. Multiple OR'd, configurable source conditions.

25.15.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 25-19. DMA Triggers from the EPWM

Trigger Name	Peripheral Instance Name	Register Group	EPWM DMA Configuration Registers	Description
EPWM0_SOCA	EPWM0	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM0 SOCA DMA trigger. Single, configurable source condition.
EPWM0_SOCB	EPWM0	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM0 SOCB DMA trigger. Single, configurable source condition.
EPWM1_SOCA	EPWM1	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM1 SOCA DMA trigger. Single, configurable source condition.
EPWM1_SOCB	EPWM1	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM1 SOCB DMA trigger. Single, configurable source condition.
EPWM2_SOCA	EPWM2	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM2 SOCA DMA trigger. Single, configurable source condition.

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Table 25-19. DMA Triggers from the EPWM (continued)

Trigger Name	Peripheral Instance Name	Register Group	EPWM DMA Configuration Registers	Description
EPWM2_SOCB	EPWM2	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM2 SOCB DMA trigger. Single, configurable source condition.
EPWM3_SOCA	EPWM3	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM3 SOCA DMA trigger. Single, configurable source condition.
EPWM3_SOCB	EPWM3	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM3 SOCB DMA trigger. Single, configurable source condition.
EPWM4_SOCA	EPWM4	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM4 SOCA DMA trigger. Single, configurable source condition.
EPWM4_SOCB	EPWM4	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM4 SOCB DMA trigger. Single, configurable source condition.
EPWM5_SOCA	EPWM5	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM5 SOCA DMA trigger. Single, configurable source condition.
EPWM5_SOCB	EPWM5	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM5 SOCB DMA trigger. Single, configurable source condition.

25.15.3 ADC Sequencer Triggers

See the Section 20.3.3 section for more details about how to configure triggers for individual ADC sequencers.

Table 25-20. ADC Triggers from the EPWM

Trigger Name	Peripheral Instance Name	Register Group	EPWM ADC Trigger Configuration Registers	Description
EPWM0_SOCA	EPWM0	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM0 SOCA ADC trigger. Single, configurable source condition.
EPWM0_SOCB	EPWM0	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM0 SOCB ADC trigger. Single, configurable source condition.
EPWM1_SOCA	EPWM1	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM1 SOCA ADC trigger. Single, configurable source condition.
EPWM1_SOCB	EPWM1	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM1 SOCB ADC trigger. Single, configurable source condition.

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Table 25-20. ADC Triggers from the EPWM (continued)

Trigger Name	Peripheral Instance Name	Register Group	EPWM ADC Trigger Configuration Registers	Description
EPWM2_SOCA	EPWM2	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM2 SOCA ADC trigger. Single, configurable source condition.
EPWM2_SOCB	EPWM2	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM2 SOCB ADC trigger. Single, configurable source condition.
EPWM3_SOCA	EPWM3	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM3 SOCA ADC trigger. Single, configurable source condition.
EPWM3_SOCB	EPWM3	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM3 SOCB ADC trigger. Single, configurable source condition.
EPWM4_SOCA	EPWM4	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM4 SOCA ADC trigger. Single, configurable source condition.
EPWM4_SOCB	EPWM4	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM4 SOCB ADC trigger. Single, configurable source condition.
EPWM5_SOCA	EPWM5	N/A	ETSEL.SOCASEL, ETSEL.SOCAEN, ETFLG.SOCA, ETFRC.SOCA, ETCLR.SOCA	EPWM5 SOCA ADC trigger. Single, configurable source condition.
EPWM5_SOCB	EPWM5	N/A	ETSEL.SOCBSEL, ETSEL.SOCBEN, ETFLG.SOCB, ETFRC.SOCB, ETCLR.SOCB	EPWM5 SOCB ADC trigger. Single, configurable source condition.

25.16 EPWM Registers

This Section describes the EPWM Registers.

25.16.1 EPWM Base Address Table

Table 25-21. EPWM Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Epwm1Regs	EPWM_REGS	EPWM1	0x400B_5000
Epwm2Regs	EPWM_REGS	EPWM2	0x400B_6000
Epwm3Regs	EPWM_REGS	EPWM3	0x400B_7000
Epwm4Regs	EPWM_REGS	EPWM4	0x400B_8000
Epwm5Regs	EPWM_REGS	EPWM5	0x400B_9000

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25.16.2 EPWM_REGS Registers

Table 25-22 lists the memory-mapped registers for the EPWM_REGS registers. All register offset addresses not listed in Table 25-22 should be considered as reserved locations and the register contents should not be modified.

Table 25-22. EPWM_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	TBCTL	Time Base Control Register		Go
2h	TBCTL2	Time Base Control Register 2		Go
6h	EPWMSYNCINSEL	EPWMxSYNCIN Source Select Register		Go
8h	TBCTR	Time Base Counter Register		Go
Ah	TBSTS	Time Base Status Register		Go
Ch	EPWMSYNCOUTEN	EPWMxSYNCOUT Source Enable Register		Go
Eh	TBCTL3	Time Base Control Register 3		Go
10h	CMPCTL	Counter Compare Control Register		Go
12h	CMPCTL2	Counter Compare Control Register 2		Go
18h	DBCTL	Dead-Band Generator Control Register		Go
1Ah	DBCTL2	Dead-Band Generator Control Register 2		Go
20h	AQCTL	Action Qualifier Control Register		Go
22h	AQTSRCSEL	Action Qualifier Trigger Event Source Select Register		Go
28h	PCCTL	PWM Chopper Control Register		Go
30h	VCAPCTL	Valley Capture Control Register		Go
32h	VCNTCFG	Valley Counter Config Register		Go
40h	HRCNFG	HRPWM Configuration Register		Go
42h	HRPWR	HRPWM Power Register		Go
44h	HRCAL	HRPWM Calibration Register		Go
46h	HRPRD	HRPWM Period Register		Go
48h	HRCNT0	HRPWM Counter 0 Register		Go
4Ah	HRCNT1	HRPWM Counter 1 Register		Go
4Ch	HRMSTEP	HRPWM MEP Step Register		Go
4Eh	HRCNFG2	HRPWM Configuration 2 Register		Go
5Ah	HRPCTL	High Resolution Period Control Register		Go
5Ch	TRREM	HRPWM High Resolution Remainder Register		Go
68h	GLDCTL	Global PWM Load Control Register		Go
6Ah	GLDCFG	Global PWM Load Config Register		Go
70h	EPWMXLINK	EPWMx Link Register		Go
80h	AQCTLA	Action Qualifier Control Register For Output A		Go
82h	AQCTLA2	Additional Action Qualifier Control Register For Output A		Go
84h	AQCTLB	Action Qualifier Control Register For Output B		Go
86h	AQCTLB2	Additional Action Qualifier Control Register For Output B		Go
8Eh	AQSFRC	Action Qualifier Software Force Register		Go
92h	AQCSFRC	Action Qualifier Continuous S/W Force Register		Go
A0h	DBREDHR	Dead-Band Generator Rising Edge Delay High Resolution Mirror Register		Go
A2h	DBRED	Dead-Band Generator Rising Edge Delay High Resolution Mirror Register		Go

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Table 25-22. EPWM_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
A4h	DBFEDHR	Dead-Band Generator Falling Edge Delay High Resolution Register		Go
A6h	DBFED	Dead-Band Generator Falling Edge Delay Count Register		Go
C0h	TBPHS	Time Base Phase High		Go
C4h	TBPRDHR	Time Base Period High Resolution Register		Go
C6h	TBPRD	Time Base Period Register		Go
D4h	CMPA	Counter Compare A Register		Go
D8h	CMPB	Compare B Register		Go
DEh	CMPC	Counter Compare C Register		Go
E2h	CMPD	Counter Compare D Register		Go
E8h	GLDCTL2	Global PWM Load Control Register 2		Go
EEh	SWVDELVAL	Software Valley Mode Delay Register		Go
100h	TZSEL	Trip Zone Select Register		Go
104h	TZDCSEL	Trip Zone Digital Comparator Select Register		Go
108h	TZCTL	Trip Zone Control Register		Go
10Ah	TZCTL2	Additional Trip Zone Control Register		Go
10Ch	TZCTLDCA	Trip Zone Control Register Digital Compare A		Go
10Eh	TZCTLDCB	Trip Zone Control Register Digital Compare B		Go
11Ah	TZEINT	Trip Zone Enable Interrupt Register		Go
126h	TZFLG	Trip Zone Flag Register		Go
128h	TZCBCFLG	Trip Zone CBC Flag Register		Go
12Ah	TZOSTFLG	Trip Zone OST Flag Register		Go
12Eh	TZCLR	Trip Zone Clear Register		Go
130h	TZCBCCLR	Trip Zone CBC Clear Register		Go
132h	TZOSTCLR	Trip Zone OST Clear Register		Go
136h	TZFRC	Trip Zone Force Register		Go
148h	ETSEL	Event Trigger Selection Register		Go
14Ch	ETPS	Event Trigger Pre-Scale Register		Go
150h	ETFLG	Event Trigger Flag Register		Go
154h	ETCLR	Event Trigger Clear Register		Go
158h	ETFRC	Event Trigger Force Register		Go
15Ch	ETINTPS	Event-Trigger Interrupt Pre-Scale Register		Go
160h	ETSOCPS	Event-Trigger SOC Pre-Scale Register		Go
164h	ETCNTINITCTL	Event-Trigger Counter Initialization Control Register		Go
168h	ETCNTINIT	Event-Trigger Counter Initialization Register		Go
180h	DCTRIPSEL	Digital Compare Trip Select Register		Go
186h	DCACTL	Digital Compare A Control Register		Go
188h	DCBCTL	Digital Compare B Control Register		Go
18Eh	DCFCTL	Digital Compare Filter Control Register		Go
190h	DCCAPCTL	Digital Compare Capture Control Register		Go
192h	DCFOFFSET	Digital Compare Filter Offset Register		Go
194h	DCFOFFSETCNT	Digital Compare Filter Offset Counter Register		Go
196h	DCFWINDOW	Digital Compare Filter Window Register		Go
198h	DCFWINDOWCNT	Digital Compare Filter Window Counter Register		Go

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Table 25-22. EPWM_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
19Ah	BLANKPULSEMIXSEL	Blanking window trigger pulse select register		Go
19Eh	DCCAP	Digital Compare Counter Capture Register		Go
1A4h	DCAHTRIPSEL	Digital Compare AH Trip Select		Go
1A6h	DCALTRIPSEL	Digital Compare AL Trip Select		Go
1A8h	DCBHTRIPSEL	Digital Compare BH Trip Select		Go
1AAh	DCBLTRIPSEL	Digital Compare BL Trip Select		Go
1F4h	EPWMLOCK	EPWM Lock Register		Go
1FAh	HWVDELVAL	Hardware Valley Mode Delay Register		Go
1FCh	VCNTVAL	Hardware Valley Counter Register		Go

Complex bit access types are encoded to fit into small table cells. Table 25-23 shows the codes that are used for access types in this section.

Table 25-23. EPWM_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
WOnce	W Once	Write Write once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 TBCTL Register (Offset = 0h) [Reset = 0083h]

TBCTL is shown in Figure 25-66 and described in Table 25-24.

Return to the Summary Table.

Time Base Control Register

Figure 25-66. TBCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W-0h		R/W-0h	R/W-0h			R/W-1h	
7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	RESERVED		PRDLD	PHSEN	CTRMODE	
R/W-1h	R-0/W1S-0h	R-0h		R/W-0h	R/W-0h	R/W-3h	

Table 25-25. TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events 00: Stop after the next time-base counter increment or decrement 01: Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) - Down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) - Up-down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) 1x: Free run Reset type: SYSRSn
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (TBCTR) will count after a synchronization event occurs and a new phase value is loaded from the phase (TBPHS) register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored. 0: Count down after the synchronization event. 1: Count up after the synchronization event. Reset type: SYSRSn
12-10	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value (TBCLK = EPWMCLK/(HSPCLKDIV * CLKDIV): 000: /1 (default on reset) 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Reset type: SYSRSn

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Table 25-25. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-7	HSPCLKDIV	R/W	1h	High Speed Time Base Clock Pre-Scale Bits These bits determine part of the time-base clock prescale value. TBCLK = EPWMCLK / (HSPCLKDIV x CLKDIV). This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager (EV) peripheral. 000: /1 001: /2 (default on reset) 010: /4 011: /6 100: /8 101: /10 110: /12 111: /14 Reset type: SYSRSn
6	SWFSYNC	R-0/W1S	0h	Software Forced Sync Pulse 0: Writing a 0 has no effect and reads always return a 0. 1: Writing a 1 forces a one-time synchronization pulse to be generated. SWFSYNC can be enabled to affect EPWMxSYNCO by setting the EPWMSYNCOUTEN.SWEN bit. Reset type: SYSRSn
5-4	RESERVED	R	0h	Reserved
3	PRDLD	R/W	0h	Active Period Reg Load from Shadow Select 0: The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. A write/read to the TBPRD register accesses the shadow register. 1: Immediate Mode (Shadow register bypassed): A write or read to the TBPRD register accesses the active register. Reset type: SYSRSn
2	PHSEN	R/W	0h	Counter Reg Load from Phase Reg Enable 0: Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS). 1: Allow Counter to be loaded from the Phase register (TBPHS) and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6. Reset type: SYSRSn
1-0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00: Up-count mode 01: Down-count mode 10: Up-down count mode 11: Freeze counter operation (default on reset) Reset type: SYSRSn

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2 TBCTL2 Register (Offset = 2h) [Reset = 0000h]

TBCTL2 is shown in Figure 25-67 and described in Table 25-25.

Return to the Summary Table.

Time Base Control Register 2

Figure 25-67. TBCTL2 Register

15	14	13	12	11	10	9	8
PRDLDSYNC		RESERVED		RESERVED			
R/W-0h		R-0h		R-0-0h			
7	6	5	4	3	2	1	0
OSHTSYNC	OSHTSYNCMODE	RESERVED	RESERVED				
R-0/W1S-0h	R/W-0h	R/W-0h	R-0-0h				

Table 25-27. TBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PRDLDSYNC	R/W	0h	Shadow to Active Period Register Load on SYNC event 00: Shadow to Active Load of TBPRD occurs only when TBCTR = 0 (same as legacy). 01: Shadow to Active Load of TBPRD occurs both when TBCTR = 0 and when SYNC occurs. 10: Shadow to Active Load of TBPRD occurs only when a SYNC is received. 11: Reserved Note: This bit selection is valid only if TBCTL[PRDLD]=0. Reset type: SYSRSn
13-12	RESERVED	R	0h	Reserved
11-8	RESERVED	R-0	0h	Reserved
7	OSHTSYNC	R-0/W1S	0h	Oneshot sync bit 0: Writing a '0' has no effect. 1: Allow one sync pulse to propogate. Reset type: SYSRSn
6	OSHTSYNCMODE	R/W	0h	Oneshot sync enable bit 0: Oneshot sync mode disabled 1: Oneshot sync mode enabled Reset type: SYSRSn
5	RESERVED	R/W	0h	Reserved
4-0	RESERVED	R-0	0h	Reserved

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3 EPWMSYNCINSEL Register (Offset = 6h) [Reset = 0001h]

EPWMSYNCINSEL is shown in Figure 25-68 and described in Table 25-26.

Return to the Summary Table.

EPWMxSYNCIN Source Select Register

Figure 25-68. EPWMSYNCINSEL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			SEL				
R-0h			R/W-1h				

Table 25-29. EPWMSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4-0	SEL	R/W	1h	These bits determine the source of the EPWMxSYNCI signal. 0x00 Disabled Other Values defined in the 'ePWM SYNC Selection' table Reset type: SYSRSn

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4 TBCTR Register (Offset = 8h) [Reset = 0000h]

TBCTR is shown in Figure 25-69 and described in Table 25-27.

Return to the Summary Table.

Time Base Counter Register

Figure 25-69. TBCTR Register

15	14	13	12	11	10	9	8
TBCTR							
R/W-0h							
7	6	5	4	3	2	1	0
TBCTR							
R/W-0h							

Table 25-31. TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TBCTR	R/W	0h	Time Base Counter Register Reset type: SYSRSn

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5 TBSTS Register (Offset = Ah) [Reset = 0001h]

TBSTS is shown in Figure 25-70 and described in Table 25-28.

Return to the Summary Table.

Time Base Status Register

Figure 25-70. TBSTS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED					CTRMAX	SYNCI	CTRDIR
R-0-0h					R/W1C-0h	R/W1C-0h	R-1h

Table 25-33. TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R-0	0h	Reserved
2	CTRMAX	R/W1C	0h	Time-Base Counter Max Latched Status Bit 0: Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect. 1: Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event. Reset type: SYSRSn
1	SYNCI	R/W1C	0h	Input Synchronization Latched Status Bit 0: Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred. 1: Reading a 1 on this bit indicates that an external synchronization event has occurred (EPWMxSYNCI). Writing a 1 to this bit will clear the latched event. Reset type: SYSRSn
0	CTRDIR	R	1h	Time Base Counter Direction Status Bit 0: Time-Base Counter is currently counting down. 1: Time-Base Counter is currently counting up. Note: This bit is only valid when the counter is not frozen. Reset type: SYSRSn

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6 EPWMSYNCOUTEN Register (Offset = Ch) [Reset = 0001h]

EPWMSYNCOUTEN is shown in Figure 25-71 and described in Table 25-29.

Return to the Summary Table.

EPWMxSYNCOUT Source Enable Register

Figure 25-71. EPWMSYNCOUTEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT1EN	DCAEVT1EN	CMPDEN	CMPCEN	CMPBEN	ZEROEN	SWEN
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 25-35. EPWMSYNCOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	DCBEVT1EN	R/W	0h	This bit enables the DCBEVT1.sync event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a DCBEVT1.sync event Reset type: SYSRSn
5	DCAEVT1EN	R/W	0h	This bit enables the DCAEVT1.sync event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon a DCAEVT1.sync event Reset type: SYSRSn
4	CMPDEN	R/W	0h	This bit enables the TBCTR = CMPD event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare D event (TBCTR = CMPD) Reset type: SYSRSn
3	CMPCEN	R/W	0h	This bit enables the TBCTR = CMPC event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare C event (TBCTR = CMPC) Reset type: SYSRSn
2	CMPBEN	R/W	0h	This bit enables the TBCTR = CMPB event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare B event (TBCTR = CMPB) Reset type: SYSRSn

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Table 25-35. EPWMSYNCOUTEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ZEROEN	R/W	0h	This bit enables the TBCTR = 0x0000 event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon the value of TBCTR changing to 0x0000 Reset type: SYSRSn
0	SWEN	R/W	1h	This bit enables the TBCTL.SWFSYNC bit to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period when the TBCTL.SWFSYNC bit is set Reset type: SYSRSn

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7 TBCTL3 Register (Offset = Eh) [Reset = 0000h]

TBCTL3 is shown in Figure 25-72 and described in Table 25-30.

Return to the Summary Table.

Time Base Control Register 3

Figure 25-72. TBCTL3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							OSSFRCEN
R-0h							R/W-0h

Table 25-37. TBCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	OSSFRCEN	R/W	0h	This bit determines which bit sets the EPWMxSYNCOUT One Shot Latch. 0 TBCTL2[OSHTSYNC] sets the One Shot Latch 1 GLDCTL2[OSHTLD] sets the One Shot Latch Reset type: SYSRSn

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8 CMPCTL Register (Offset = 10h) [Reset = 0000h]

CMPCTL is shown in Figure 25-73 and described in Table 25-31.

Return to the Summary Table.

Counter Compare Control Register

Figure 25-73. CMPCTL Register

15	14	13	12	11	10	9	8
RESERVED		LOADBSYNC		LOADASYNC		SHDWBFULL	SHDWAFULL
R-0-0h		R/W-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	SHDWBMODE	RESERVED	SHDWAMODE	LOADBMODE		LOADAMODE	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h		R/W-0h	

Table 25-39. CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R-0	0h	Reserved
13-12	LOADBSYNC	R/W	0h	Shadow to Active CMPB Register Load on SYNC event 00: Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0. Reset type: SYSRSn
11-10	LOADASYNC	R/W	0h	Shadow to Active CMPA Register Load on SYNC event 00: Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0. Reset type: SYSRSn
9	SHDWBFULL	R	0h	Counter-compare B (CMPB) Shadow Register Full Status Flag This bit self clears once a loadstrobe occurs. 0: CMPB shadow register not full yet 1: Indicates the CMPB shadow register is full a CPU write will overwrite current shadow value Reset type: SYSRSn
8	SHDWAFULL	R	0h	Counter-compare A (CMPA) Shadow Register Full Status Flag The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not affect the flag. This bit self clears once a load-strobe occurs. 0: CMPA shadow register not full yet 1: Indicates the CMPA shadow register is full, a CPU write will overwrite the current shadow value Reset type: SYSRSn
7	RESERVED	R-0	0h	Reserved

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Table 25-39. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SHDWBMODE	R/W	0h	Counter-compare B (CMPB) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A (CMPA) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action Reset type: SYSRSn
3-2	LOADBMODE	R/W	0h	Active Counter-Compare B (CMPB) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWBMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn
1-0	LOADAMODE	R/W	0h	Active Counter-Compare A (CMPA) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWAMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn

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9 CMPCTL2 Register (Offset = 12h) [Reset = 0000h]

CMPCTL2 is shown in Figure 25-74 and described in Table 25-32.

Return to the Summary Table.

Counter Compare Control Register 2

Figure 25-74. CMPCTL2 Register

15	14	13	12	11	10	9	8
RESERVED		LOADDSYNC		LOADCSYNC		RESERVED	
R-0-0h		R/W-0h		R/W-0h		R-0-0h	
7	6	5	4	3	2	1	0
RESERVED	SHDWDMODE	RESERVED	SHDWCMODE	LOADDMODE		LOADCMODE	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h		R/W-0h	

Table 25-41. CMPCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R-0	0h	Reserved
13-12	LOADDSYNC	R/W	0h	Shadow to Active CMPD Register Load on SYNC event 00: Shadow to Active Load of CMPD occurs according to LOADDMODE 01: Shadow to Active Load of CMPD occurs both according to LOADDMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPD occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWDMODE] = 0. Reset type: SYSRSn
11-10	LOADCSYNC	R/W	0h	Shadow to Active CMPC Register Load on SYNC event 00: Shadow to Active Load of CMPC occurs according to LOADCMODE 01: Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPC occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0. Reset type: SYSRSn
9-7	RESERVED	R-0	0h	Reserved
6	SHDWDMODE	R/W	0h	Counter-Compare D Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SHDWCMODE	R/W	0h	Counter-Compare C Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action. Reset type: SYSRSn

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Table 25-41. CMPCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	LOADDMODE	R/W	0h	Active Counter-Compare D (CMPD) Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: Has no effect in Immediate mode. Reset type: SYSRSn
1-0	LOADCMODE	R/W	0h	Active Counter-Compare C (CMPC) Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: Has no effect in Immediate mode. Reset type: SYSRSn

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10 DBCTL Register (Offset = 18h) [Reset = 0000h]

DBCTL is shown in Figure 25-75 and described in Table 25-33.

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Dead-Band Generator Control Register

Figure 25-75. DBCTL Register

15	14	13	12	11	10	9	8
HALFCYCLE	DEDB_MODE	OUTSWAP		SHDWDBFED MODE	SHDWDBRED MODE	LOADFEDMODE	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
LOADREDMODE		IN_MODE		POLSEL		OUT_MODE	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-43. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HALFCYCLE	R/W	0h	Half Cycle Clocking Enable Bit 0: Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate. 1: Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2. Reset type: SYSRSn
14	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control (S8 switch) 0: Rising edge delay applied to InA/InB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch (INMODE bits) on B signal path only. 1: Rising edge delay and falling edge delay applied to source selected by S4 switch (INMODE bits) and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid. Reset type: SYSRSn
13-12	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 13 controls the S6 switch and bit 12 controls the S7 switch. 00: OutA and OutB signals are as defined by OUT-MODE bits. 01: OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). 10: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = B-path as defined by OUT-MODE bits. 11: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). Reset type: SYSRSn

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Table 25-43. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SHDWDBFEDMODE	R/W	0h	FED Dead-Band Load Mode 0: Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate 'FED dead-band action.' 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy). Reset type: SYSRSn
10	SHDWDBREDMODE	R/W	0h	RED Dead-Band Load Mode 0: Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate 'RED dead-band action.' 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy). Reset type: SYSRSn
9-8	LOADFEDMODE	R/W	0h	Active DBFED Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode. Reset type: SYSRSn
7-6	LOADREDMODE	R/W	0h	Active DBRED Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode. Reset type: SYSRSn
5-4	IN_MODE	R/W	0h	Dead-Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays. 00: EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay. 01: EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal. 10: EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal. 11: EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal. Reset type: SYSRSn

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Table 25-43. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes. 00: Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default). 01: Active low complementary (ALC) mode. EPWMxA is inverted. 10: Active high complementary (AHC). EPWMxB is inverted. 11: Active low (AL) mode. Both EPWMxA and EPWMxB are inverted. Reset type: SYSRSn
1-0	OUT_MODE	R/W	0h	Dead-Band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch. 00: DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect. 01: Apath = InA (delay is by-passed for A signal path) Bpath = FED (Falling Edge Delay in B signal path) 10: Apath = RED (Rising Edge Delay in A signal path) Bpath = InB (delay is by-passed for B signal path) 11: DBM is fully enabled (i.e. both RED and FED active) Reset type: SYSRSn

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11 DBCTL2 Register (Offset = 1Ah) [Reset = 0000h]

DBCTL2 is shown in Figure 25-76 and described in Table 25-34.

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Dead-Band Generator Control Register 2

Figure 25-76. DBCTL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED					SHDWDBCTLMODE	LOADDBCTLMODE	
R-0-0h					R/W-0h	R/W-0h	

Table 25-45. DBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R-0	0h	Reserved
2	SHDWDBCTLMODE	R/W	0h	DBCTL Load Mode 0: Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register. 1: Shadow mode - All writes and reads to bits [5:0] of the DBCTL register are shadowed. All other bits still access the active register. Reset type: SYSRSn
1-0	LOADDBCTLMODE	R/W	0h	Active DBCTL Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode Reset type: SYSRSn

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12 AQCTL Register (Offset = 20h) [Reset = 0000h]

AQCTL is shown in Figure 25-77 and described in Table 25-35.

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Action Qualifier Control Register

Figure 25-77. AQCTL Register

15	14	13	12	11	10	9	8
RESERVED				LDAQBSYNC		LDAQASYNC	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	SHDWAQBMODE	RESERVED	SHDWAQAMODE	LDAQBMODE		LDAQAMODE	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h		R/W-0h	

Table 25-47. AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-10	LDAQBSYNC	R/W	0h	Shadow to Active AQCTLB Register Load on SYNC event 00: Shadow to Active Load of AQCTLB occurs according to LDAQBMODE 01: Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLB occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQBMODE] = 1. Reset type: SYSRSn
9-8	LDAQASYNC	R/W	0h	Shadow to Active AQCTLA Register Load on SYNC event 00: Shadow to Active Load of AQCTLA occurs according to LDAQAMODE 01: Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLA occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQAMODE] = 1. Reset type: SYSRSn
7	RESERVED	R-0	0h	Reserved
6	SHDWAQBMODE	R/W	0h	Action Qualifier B Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SHDWAQAMODE	R/W	0h	Action Qualifier A Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register. Reset type: SYSRSn

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Table 25-47. AQCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	LDAQBMODE	R/W	0h	Active Action Qualifier B Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: has no effect in Immediate mode. Reset type: SYSRSn
1-0	LDAQAMODE	R/W	0h	Active Action Qualifier A Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: has no effect in Immediate mode. Reset type: SYSRSn

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13 AQTSRCSEL Register (Offset = 22h) [Reset = 0000h]

AQTSRCSEL is shown in Figure 25-78 and described in Table 25-36.

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Action Qualifier Trigger Event Source Select Register

Figure 25-78. AQTSRCSEL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
T2SEL				T1SEL			
R/W-0h				R/W-0h			

Table 25-49. AQTSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-4	T2SEL	R/W	0h	T2 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved Reset type: SYSRSn
3-0	T1SEL	R/W	0h	T1 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved Reset type: SYSRSn

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14 PCCTL Register (Offset = 28h) [Reset = 0000h]

PCCTL is shown in Figure 25-79 and described in Table 25-37.

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PWM Chopper Control Register

Figure 25-79. PCCTL Register

15	14	13	12	11	10	9	8
RESERVED						CHPDUTY	
R-0-0h						R/W-0h	
7	6	5	4	3	2	1	0
CHPFREQ			OSHTWTH				CHPEN
R/W-0h			R/W-0h				R/W-0h

Table 25-51. PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10-8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 000: Duty = 1/8 (12.5%) 001: Duty = 2/8 (25.0%) 010: Duty = 3/8 (37.5%) 011: Duty = 4/8 (50.0%) 100: Duty = 5/8 (62.5%) 101: Duty = 6/8 (75.0%) 110: Duty = 7/8 (87.5%) 111: Reserved Reset type: SYSRSn
7-5	CHPFREQ	R/W	0h	Chopping Clock Frequency 000: Divide by 1 (no prescale, = 12.5 MHz at 100 MHz TBCLK) 001: Divide by 2 (6.25 MHz at 100 MHz TBCLK) 010: Divide by 3 (4.16 MHz at 100 MHz TBCLK) 011: Divide by 4 (3.12 MHz at 100 MHz TBCLK) 100: Divide by 5 (2.50 MHz at 100 MHz TBCLK) 101: Divide by 6 (2.08 MHz at 100 MHz TBCLK) 110: Divide by 7 (1.78 MHz at 100 MHz TBCLK) 111: Divide by 8 (1.56 MHz at 100 MHz TBCLK) Reset type: SYSRSn
4-1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0000: 1 x EPWMCLK / 8 wide (= 80 ns at 100 MHz EPWMCLK) 0001: 2 x EPWMCLK / 8 wide (= 160 ns at 100 MHz EPWMCLK) 0010: 3 x EPWMCLK / 8 wide (= 240 ns at 100 MHz EPWMCLK) 0011: 4 x EPWMCLK / 8 wide (= 320 ns at 100 MHz EPWMCLK) 0100: 5 x EPWMCLK / 8 wide (= 400 ns at 100 MHz EPWMCLK) 0101: 6 x EPWMCLK / 8 wide (= 480 ns at 100 MHz EPWMCLK) 0110: 7 x EPWMCLK / 8 wide (= 560 ns at 100 MHz EPWMCLK) 0111: 8 x EPWMCLK / 8 wide (= 640 ns at 100 MHz EPWMCLK) 1000: 9 x EPWMCLK / 8 wide (= 720 ns at 100 MHz EPWMCLK) 1001: 10 x EPWMCLK / 8 wide (= 800 ns at 100 MHz EPWMCLK) 1010: 11 x EPWMCLK / 8 wide (= 880 ns at 100 MHz EPWMCLK) 1011: 12 x EPWMCLK / 8 wide (= 960 ns at 100 MHz EPWMCLK) 1100: 13 x EPWMCLK / 8 wide (= 1040 ns at 100 MHz EPWMCLK) 1101: 14 x EPWMCLK / 8 wide (= 1120 ns at 100 MHz EPWMCLK) 1110: 15 x EPWMCLK / 8 wide (= 1200 ns at 100 MHz EPWMCLK) 1111: 16 x EPWMCLK / 8 wide (= 1280 ns at 100 MHz EPWMCLK) Reset type: SYSRSn

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Table 25-51. PCCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHPEN	R/W	0h	PWM-Chopping Enable 0: Disable (bypass) PWM chopping function 1: Enable chopping function Reset type: SYSRSn

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15 VCAPCTL Register (Offset = 30h) [Reset = 0000h]

VCAPCTL is shown in Figure 25-80 and described in Table 25-38.

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Valley Capture Control Register

Figure 25-80. VCAPCTL Register

15	14	13	12	11	10	9	8
RESERVED					EDGEFILTDLYSEL	VDELAYDIV	
R-0-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
VDELAYDIV	RESERVED		TRIGSEL			VCAPSTART	VCAPE
R/W-0h	R-0-0h		R/W-0h			R-0/W1S-0h	R/W-0h

Table 25-53. VCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	EDGEFILTDLYSEL	R/W	0h	Valley Switching Mode Delay Selection 0: No delay applied to the edge filter output 1: HWDELAYVAL delay applied to the edge filter output Reset type: SYSRSn
9-7	VDELAYDIV	R/W	0h	Valley Delay Mode Divide Enable 000: HWVDELVAL = SWVDELVAL 001: HWVDELVAL = VCNTVAL+SWVDELVAL 010: HWVDELVAL = VCNTVAL>>1+SWVDELVAL 011: HWVDELVAL = VCNTVAL>>2+SWVDELVAL 100: HWVDELVAL = VCNTVAL>>4+SWVDELVAL Note: Delay value between the consecutive edge captures can optionally be divided by using these bits. Reset type: SYSRSn
6-5	RESERVED	R-0	0h	Reserved
4-2	TRIGSEL	R/W	0h	Status of Numbered of Captured Events 000: Capture sequence is triggered by software via writes to VCAPCTL[VCAPSTART]. 001: Capture sequence is triggered by CNT_zero event. 010: Capture sequence is triggered by PRD_eq event. 011: Capture sequence is triggered by CNT_zero or PRD_eq event. 100: Capture sequence is triggered by DCAEVT1 event. 101: Capture sequence is triggered by DCAEVT2 event. 110: Capture sequence is triggered by DCBEVT1 event. 111: Capture sequence is triggered by DCBEVT2 event. Note: Valley capture sequence triggered by the selected event in this register field. Once the chosen event occurs the capture sequence is armed. Event captures occur based of the event chosen in DCFCTL[SRCSEL] register. Note: Same event may not be chosen in both DCFCTL[SRCSEL] and VCAPCTL[TRIGSEL] registers. Note: Once the chosen event in VCAPCTL[TRIGSEL] occurs, irrespective of the current capture status, capture sequence is retriggered. Reset type: SYSRSn

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Table 25-53. VCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VCAPSTART	R-0/W1S	0h	Valley Capture Start 0: Writing a 0 has no effect 1: Trigger the capture sequence once if VCAPCTL[TRIGSEL]=0x0 Note: This bit is used to start valley capture sequence through software. VCAPCTL[TRIGSEL] has to be chosen for software trigger for this bit to have any effect. Writing of 1 will result in one capture sequence trigger. Reset type: SYSRSn
0	VCAPE	R/W	0h	Valley Capture Enable/Disable 0: Disabled 1: Enabled Reset type: SYSRSn

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16 VCNTCFG Register (Offset = 32h) [Reset = 0000h]

VCNTCFG is shown in Figure 25-81 and described in Table 25-39.

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Valley Counter Config Register

Figure 25-81. VCNTCFG Register

15	14	13	12	11	10	9	8
STOPEDGESTS	RESERVED			STOPEDGE			
R-0h	R-0-0h			R/W-0h			
7	6	5	4	3	2	1	0
STARTEDGESTS	RESERVED			STARTEDGE			
R-0h	R-0-0h			R/W-0h			

Table 25-55. VCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	STOPEDGESTS	R	0h	Stop Edge Status Bit 0: Stop edge has not occurred 1: Stop edge occurred Note: This bit is set only after the trigger sequence is armed (upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]) and STOPEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL] Reset type: SYSRSn
14-12	RESERVED	R-0	0h	Reserved
11-8	STOPEDGE	R/W	0h	Counter Stop Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would stop counting upon the occurrence of chosen number of events thorough this bit field. Stop counting on occurrence of: 0000: Do not stop 0001 1st edge 0010: 2nd edge 0011: 3rd edge ... 1,1,1,1: 15th edge Reset type: SYSRSn
7	STARTEDGESTS	R	0h	Start Edge Status Bit 0: Start edge has not occurred 1: Start edge occurred Note: This bit is set only after the trigger sequence is armed (upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]) and STARTEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL] Reset type: SYSRSn
6-4	RESERVED	R-0	0h	Reserved

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Table 25-55. VCNTCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	STARTEDGE	R/W	0h	Counter Start Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would start counting upon the occurrence of chosen number of events thorough this bit field. Start counting on occurrence of 0000: Do not start 0001: 1st edge 0010: 2nd edge 0011: 3rd edge ... 1111: 15th edge Reset type: SYSRSn

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17 HRCNFG Register (Offset = 40h) [Reset = 0000h]

HRCNFG is shown in Figure 25-82 and described in Table 25-40.

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HRPWM Configuration Register
This register is only accessible on EPWM modules with HRPWM capabilities.

Figure 25-82. HRCNFG Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	HRLOADB		CTLMODEB	EDGMODEB	
R/W-0h		R-0-0h	R/W-0h		R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
SWAPAB	AUTOCONV	SELOUTB	HRLOAD		CTLMODE	EDGMODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	

Table 25-57. HRCNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved
13	RESERVED	R-0	0h	Reserved
12-11	HRLOADB	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPBHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Reserved Reset type: SYSRSn
10	CTLMODEB	R/W	0h	Control Mode Bits Selects the register (CMP/TBPRD or TBPHS) that controls the MEP: 0: CMPBHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode). Reset type: SYSRSn
9-8	EDGMODEB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPBHR) 10: MEP control of falling edge (CMPBHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR) Reset type: SYSRSn
7	SWAPAB	R/W	0h	Swap ePWM A & B Output Signals This bit enables the swapping of the A & B signal outputs. The selection is as follows: 0: ePWMxA and ePWMxB outputs are unchanged. 1: ePWMxA signal appears on ePWMxB output and ePWMxB signal appears on ePWMxA output. Reset type: SYSRSn

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Table 25-57. HRCNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AUTOCONV	R/W	0h	Auto Convert Delay Line Value Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor. 0: Automatic HRMSTEP scaling is disabled. 1: Automatic HRMSTEP scaling is enabled. If application software is manually scaling the fractional duty cycle, or phase (i.e. software sets CMPAHR = (fraction(PWMduty * PWMperiod) * MEP Scale Factor)<<8 + 0x080 for duty cycle), then this mode must be disabled. Reset type: SYSRSn
5	SELOUTB	R/W	0h	EPWMxB Output Select Bit This bit selects which signal is output on the ePWMxB channel output. The inversion will take the high resolution mode into account and the inverted signal will contain any high resolution modification. The inversion takes place as the last step in modifying the ePWMxB signal. 0: ePWMxB output is normal. 1: ePWMxB output is inverted version of ePWMxA signal. Reset type: SYSRSn
4-3	HRLOAD	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPAHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Reserved Reset type: SYSRSn
2	CTLMODE	R/W	0h	Control Mode Bits Selects the register (CMP/TBPRD or TBPHS) that controls the MEP: 0: CMPAHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode). Reset type: SYSRSn
1-0	EDGMODE	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPAHR) 10: MEP control of falling edge (CMPAHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR) Reset type: SYSRSn

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18 HRPWR Register (Offset = 42h) [Reset = 0000h]

HRPWR is shown in Figure 25-83 and described in Table 25-41.

Return to the Summary Table.

HRPWM Power Register
This register is only accessible on EPWM modules with HRPWM capabilities.

Figure 25-83. HRPWR Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED					RESERVED	
R/W-0h	R-0-0h					R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
R/W-0h		R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	

Table 25-59. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	R/W	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption. 1: Enables MEP calibration logic Reset type: SYSRSn
14-10	RESERVED	R-0	0h	Reserved
9-6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1-0	RESERVED	R/W	0h	Reserved

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19 HRCAL Register (Offset = 44h) [Reset = 0000h]

HRCAL is shown in Figure 25-84 and described in Table 25-42.

Return to the Summary Table.

HRPWM Calibration Register

Figure 25-84. HRCAL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
HRCAL							
R/W-0h							

Table 25-61. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-0	HRCAL	R/W	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run. Reset type: SYSRSn

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20 HRPRD Register (Offset = 46h) [Reset = 0000h]

HRPRD is shown in Figure 25-85 and described in Table 25-43.

Return to the Summary Table.

HRPWM Period Register

Figure 25-85. HRPRD Register

15	14	13	12	11	10	9	8
HRPRD							
R/W-0h							
7	6	5	4	3	2	1	0
HRPRD							
R/W-0h							

Table 25-63. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HRPRD	R/W	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. Reset type: SYSRSn

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21 HRCNT0 Register (Offset = 48h) [Reset = 0000h]

HRCNT0 is shown in Figure 25-86 and described in Table 25-44.

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HRPWM Counter 0 Register

Figure 25-86. HRCNT0 Register

15	14	13	12	11	10	9	8
HRCNT0							
R/W-0h							
7	6	5	4	3	2	1	0
HRCNT0							
R/W-0h							

Table 25-65. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HRCNT0	R/W	0h	The HRCNT0 counter increments on every ring oscillator clock pulse. Reset type: SYSRSn

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22 HRCNT1 Register (Offset = 4Ah) [Reset = 0000h]

HRCNT1 is shown in Figure 25-87 and described in Table 25-45.

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HRPWM Counter 1 Register

Figure 25-87. HRCNT1 Register

15	14	13	12	11	10	9	8
HRCNT1							
R/W-0h							
7	6	5	4	3	2	1	0
HRCNT1							
R/W-0h							

Table 25-67. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HRCNT1	R/W	0h	The HRCNT1 counter increments on every system clock pulse. Reset type: SYSRSn

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23 HRMSTEP Register (Offset = 4Ch) [Reset = 0000h]

HRMSTEP is shown in Figure 25-88 and described in Table 25-46.

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HRPWM MEP Step Register
This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Figure 25-88. HRMSTEP Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
HRMSTEP							
R/W-0h							

Table 25-69. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-0	HRMSTEP	R/W	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run. Reset type: SYSRSn

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24 HRCNFG2 Register (Offset = 4Eh) [Reset = 0000h]

HRCNFG2 is shown in Figure 25-89 and described in Table 25-47.

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HRPWM Configuration 2 Register
This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Figure 25-89. HRCNFG2 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED					
R/W-0h	R-0/W1S-0h	R-0-0h					
7	6	5	4	3	2	1	0
RESERVED		CTLMODEDBFED		CTLMODEDBRED		EDGMODEDB	
R-0-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-71. HRCNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R-0/W1S	0h	Reserved
13-6	RESERVED	R-0	0h	Reserved
5-4	CTLMODEDBFED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADFEDMODE] Selects the time event that loads the DBFEDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01 Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10 Load on either CTR = Zero or CTR = PRD 11 Reserved Reset type: SYSRSn
3-2	CTLMODEDBRED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADREDMODE] Selects the time event that loads the DBREDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01 Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10 Load on either CTR = Zero or CTR = PRD 11 Reserved Reset type: SYSRSn
1-0	EDGMODEDB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00 HRPWM capability is disabled (default on reset) 01 MEP control of rising edge (DBREDHR) 10 MEP control of falling edge (DBFEDHR) 11 MEP control of both edges (rising edge of DBREDHR or falling edge of DBFEDHR) Reset type: SYSRSn

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25 HRPCTL Register (Offset = 5Ah) [Reset = 0000h]

HRPCTL is shown in Figure 25-90 and described in Table 25-48.

Return to the Summary Table.

High Resolution Period Control Register
Fields in this register related to HRPWM are only applicable on EPWM modules with HRPWM capabilities.

Figure 25-90. HRPCTL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	PWMSYNCSELX			RESERVED	TBPHSHRLOADE	PWMSYNCSEL	HRPE
R-0-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-73. HRPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R-0	0h	Reserved
6-4	PWMSYNCSELX	R/W	0h	Extended selection bits for EPWMSYNCPER 000: EPWMSYNCPER is defined by PWMSYNCSEL - > default condition (compatible with previous EPWM versions) 001: Reserved 010: Reserved 011: Reserved 100: CTR = CMPC, Count direction Up 101: CTR = CMPC, Count direction Down 110: CTR = CMPD, Count direction Up 111: CTR = CMPD, Count direction Down Reset type: SYSRSn
3	RESERVED	R/W	0h	Reserved
2	TBPHSHRLOADE	R/W	0h	TBPHSHR Load Enable This bit allows you to synchronize ePWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple ePWM modules operating at the same frequency to be phase aligned with high-resolution. 0: Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event: 1: Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature. This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled for up-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled. Reset type: SYSRSn

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Table 25-73. HRPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PWMSYNCSEL	R/W	0h	PWMSYNC Source Select Bit: This bit selects the source for the EPWMSYNCPER signal that goes to the CMPSS and GPDAC: 0 CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 1 CTR = zero: Time-base counter equal to zero (TBCTR = 0x00) Reset type: SYSRSn
0	HRPE	R/W	0h	High Resolution Period Enable Bit 0: High resolution period feature disabled. In this mode the ePWM behaves as a Type 4 ePWM. 1: High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 0,1 (down-count mode) is not supported. Reset type: SYSRSn

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26 TRREM Register (Offset = 5Ch) [Reset = 0000h]

TRREM is shown in Figure 25-91 and described in Table 25-49.

Return to the Summary Table.

HRPWM High Resolution Remainder Register
This register is only accessible on EPWM modules with HRPWM capabilities.

Figure 25-91. TRREM Register

15	14	13	12	11	10	9	8
RESERVED					TRREM		
R-0-0h					R/W-0h		
7	6	5	4	3	2	1	0
TRREM							
R/W-0h							

Table 25-75. TRREM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10-0	TRREM	R/W	0h	HRPWM Remainder Bits: This 11-bit value keeps track of the remainder portion of the HRPWM algorithm calculations. This value keeps track of the remainder portion of the HRPWM hardware calculations. Notes: 1. The lower 8-bits of the TRREM register can be automatically initialized with the TBPHSHR value on a SYNCIN or TBCTL[SWFSYNC] event or DC event (if enabled). The user can also write a value with the CPU. 2. Priority of TRREM register updates: Sync (software or hardware) TBPHSHR copied to TRREM : Highest Priority HRPWM Hardware (updates TRREM register): Next priority CPU Write To TRREM Register: Lowest Priority 3. Bit 10 of TRREM register is not used in asymmetrical mode. This bit can be forced to zero. TRREM will be initialized to 0x0 and 0x100 in Up and Up-down modes respectively. Asymmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,0 Symmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,1 Reset type: SYSRSn

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27 GLDCTL Register (Offset = 68h) [Reset = 0000h]

GLDCTL is shown in Figure 25-92 and described in Table 25-50.

Return to the Summary Table.

Global PWM Load Control Register

Figure 25-92. GLDCTL Register

15	14	13	12	11	10	9	8
RESERVED			GLDCNT			GLDPRD	
R-0-0h			R-0h			R/W-0h	
7	6	5	4	3	2	1	0
GLDPRD	RESERVED	OSHTMODE	GLDMODE				GLD
R/W-0h	R-0-0h	R/W-0h	R/W-0h				R/W-0h

Table 25-77. GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R-0	0h	Reserved
12-10	GLDCNT	R	0h	Global Load Strobe Counter Register These bits indicate how many selected events have occurred: 000: No events 001: 1 event 010: 2 events 011: 3 events 100: 4 events 101: 5 events 110: 6 events 111: 7 events Reset type: SYSRSn
9-7	GLDPRD	R/W	0h	Global Load Strobe Period Select Register These bits select how many selected events need to occur before a load strobe is generated 000: Disable counter 001: Generate strobe on GLDCNT = 001 (1st event) 010: Generate strobe on GLDCNT = 010 (2nd event) 011: Generate strobe on GLDCNT = 011 (3rd event) 100: Generate strobe on GLDCNT = 011 (4th event) 101: Generate strobe on GLDCNT = 001 (5th event) 110: Generate strobe on GLDCNT = 010 (6th event) 111: Generate strobe on GLDCNT = 011 (7th event) Reset type: SYSRSn
6	RESERVED	R-0	0h	Reserved
5	OSHTMODE	R/W	0h	One Shot Load Mode Control Bit 0: One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes. 1: One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1. Note: One Shot mode can only be used with global shadow to active load mode enabled (GLDCTL[GLD]=1) Reset type: SYSRSn

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Table 25-77. GLDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	GLDMODE	R/W	0h	Global Load Pulse selection for Shadow to Active Mode Reloads 0000: Load on Counter = 0 (CNT_ZRO) 0001: Load on Counter = Period (PRD_EQ) 0010: Load on either Counter = 0, or Counter = Period 0011: Load on SYNCEVT - this is logical OR of DCAEVT1.sync, DCBEVT1.sync, EPWMxSYNCI and TBCTL[SWFSYNC] 0100: Load on SYNCEVT or CNT_ZRO 0101: Load on SYNCEVT or PRD_EQ 0110: Load on SYNCEVT or CNT_ZRO or PRD_EQ 1000: Reserved ... 1110: Reserved 1111: Load on GLDCTL2[GFRCLD] write Reset type: SYSRSn
0	GLD	R/W	0h	Global Shadow to Active Load Event Control 0: Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified (Compatible with previous EPWM versions). 1: When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored. Reset type: SYSRSn

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28 GLDCFG Register (Offset = 6Ah) [Reset = 0000h]

GLDCFG is shown in Figure 25-93 and described in Table 25-51.

Return to the Summary Table.

Global PWM Load Config Register

Figure 25-93. GLDCFG Register

15	14	13	12	11	10	9	8
RESERVED					AQCSFRC	AQCTLB_AQCTLB2	AQCTLA_AQCTLA2
R-0-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DBCTL	DBFED_DBFEDHR	DBRED_DBREDHR	CMPD	CMPC	CMPB_CMPBHR	CMPA_CMPAHR	TBPRD_TBPRDHR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-79. GLDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	AQCSFRC	R/W	0h	Global load event configuration for AQCSFRC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
9	AQCTLB_AQCTLB2	R/W	0h	Global load event configuration for AQCTLB_AQCTLB2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
8	AQCTLA_AQCTLA2	R/W	0h	Global load event configuration for AQCTLA_AQCTLA2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
7	DBCTL	R/W	0h	Global load event configuration for DBCTL 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
6	DBFED_DBFEDHR	R/W	0h	Global load event configuration for DBFED_DBFEDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn

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Table 25-79. GLDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DBRED_DBREDHR	R/W	0h	Global load event configuration for DBRED_DBREDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
4	CMPD	R/W	0h	Global load event configuration for CMPD 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
3	CMPC	R/W	0h	Global load event configuration for CMPC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
2	CMPB_CMPBHR	R/W	0h	Global load event configuration for CMPB_CMPBHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
1	CMPA_CMPAHR	R/W	0h	Global load event configuration for CMPA_CMPAHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn
0	TBPRD_TBPRDHR	R/W	0h	Global load event configuration for TBPRD_TBPRDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1 Reset type: SYSRSn

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29 EPWMXLINK Register (Offset = 70h) [Reset = 000XXXXXh]

EPWMXLINK is shown in Figure 25-94 and described in Table 25-52.

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EPWMx Link Register
This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

Figure 25-94. EPWMXLINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GLDCTL2LINK				RESERVED								CMPDLINK			
R/W-0h				R-0-0h								R/W-Xh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPCLINK				CMPBLINK				CMPALINK				TBPRDLINK			
R/W-Xh				R/W-Xh				R/W-Xh				R/W-Xh			

Table 25-81. EPWMXLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	GLDCTL2LINK	R/W	0h	GLDCTL2 Link Bits Writes to the GLDCTL2 registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's GLDCTL2 registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn
27-20	RESERVED	R-0	0h	Reserved
19-16	CMPDLINK	R/W	Xh	CMPD Link Bits Writes to the CMPD registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPD registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn
15-12	CMPCLINK	R/W	Xh	CMPC Link Bits Writes to the CMPC registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPC registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn
11-8	CMPBLINK	R/W	Xh	CMPB_CMPBHR Link Bits Writes to the CMPB_CMPBHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPB_CMPBHR registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn

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Table 25-81. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	CMPALINK	R/W	Xh	CMPA_CMPAHR Link Bits Writes to the CMPA_CMPAHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPA_CMPAHR registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn
3-0	TBPRDLINK	R/W	Xh	TBPRD_TBPRDHR Link Bits Writes to the TBPRD:TBPRDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's TBPRD_TBPRDHR registers. 0000: ePWM1 0001: ePWM2 ... Up to the last instance of ePWM. All others are reserved. Reset type: SYSRSn

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30 AQCTLA Register (Offset = 80h) [Reset = 0000h]

AQCTLA is shown in Figure 25-95 and described in Table 25-53.

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Action Qualifier Control Register For Output A

Figure 25-95. AQCTLA Register

15	14	13	12	11	10	9	8
RESERVED				CBD		CBU	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-83. AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 25-83. AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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31 AQCTLA2 Register (Offset = 82h) [Reset = 0000h]

AQCTLA2 is shown in Figure 25-96 and described in Table 25-54.

Return to the Summary Table.

Additional Action Qualifier Control Register For Output A

Figure 25-96. AQCTLA2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-85. AQCTLA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
3-2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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32 AQCTLB Register (Offset = 84h) [Reset = 0000h]

AQCTLB is shown in Figure 25-97 and described in Table 25-55.

Return to the Summary Table.

Action Qualifier Control Register For Output B

Figure 25-97. AQCTLB Register

15	14	13	12	11	10	9	8
RESERVED				CBD		CBU	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-87. AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 25-87. AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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33 AQCTLB2 Register (Offset = 86h) [Reset = 0000h]

AQCTLB2 is shown in Figure 25-98 and described in Table 25-56.

Return to the Summary Table.

Additional Action Qualifier Control Register For Output B

Figure 25-98. AQCTLB2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-89. AQCTLB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
3-2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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34 AQSFRC Register (Offset = 8Eh) [Reset = 0000h]

AQSFRC is shown in Figure 25-99 and described in Table 25-57.

Return to the Summary Table.

Action Qualifier Software Force Register

Figure 25-99. AQSFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W-0h		R-0/W1S-0h	R/W-0h		R-0/W1S-0h	R/W-0h	

Table 25-91. AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options 00: Load on time-base counter equals zero 01: Load on time-base counter equals period 10: Load on time-base counter equals zero or counter equals period 11: Load immediately (the active register is directly accessed by the CPU and is not loaded from the shadow register). Reset type: SYSRSn
5	OTSFB	R-0/W1S	0h	One-Time Software Forced Event on Output B 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on output B. 1: Initiates a single software forced event Reset type: SYSRSn
4-3	ACTSFB	R/W	0h	Action When One-Time Software Force B is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -> High, High -> Low) Note: This action is not qualified by counter direction (CNT_dir) Reset type: SYSRSn
2	OTSFA	R-0/W1S	0h	One-Time Software Forced Event on Output A 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated). This is a one-shot forced event. It can be overridden by another subsequent event on output A. 1: Initiates a single software forced event Reset type: SYSRSn
1-0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -> High, High -> Low) Note: This action is not qualified by counter direction (CNT_dir) Reset type: SYSRSn

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35 AQCSFRC Register (Offset = 92h) [Reset = 0000h]

AQCSFRC is shown in Figure 25-100 and described in Table 25-58.

Return to the Summary Table.

Action Qualifier Continuous S/W Force Register

Figure 25-100. AQCSFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				CSFB		CSFA	
R-0-0h				R/W-0h		R/W-0h	

Table 25-93. AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R-0	0h	Reserved
3-2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use AQSFRC[RLDCSF]. 00: Software forcing is disabled and has no effect 01: Forces a continuous low on output B 10: Forces a continuous high on output B 11: Software forcing is disabled and has no effect Reset type: SYSRSn
1-0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. 00: Software forcing is disabled and has no effect 01: Forces a continuous low on output A 10: Forces a continuous high on output A 11: Software forcing is disabled and has no effect Reset type: SYSRSn

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36 DBREDHR Register (Offset = A0h) [Reset = 0000h]

DBREDHR is shown in Figure 25-101 and described in Table 25-59.

Return to the Summary Table.

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Figure 25-101. DBREDHR Register

15	14	13	12	11	10	9	8
DBREDHR							RESERVED
R/W-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R-0h

Table 25-95. DBREDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	DBREDHR	R/W	0h	Dead Band Rising Edge Delay High Resolution Bits Reset type: SYSRSn
8	RESERVED	R	0h	Reserved
7-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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37 DBRED Register (Offset = A2h) [Reset = 0000h]

DBRED is shown in Figure 25-102 and described in Table 25-60.

Return to the Summary Table.

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Figure 25-102. DBRED Register

15	14	13	12	11	10	9	8
RESERVED		DBRED					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
DBRED							
R/W-0h							

Table 25-97. DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-0	DBRED	R/W	0h	Rising edge delay value Reset type: SYSRSn

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38 DBFEDHR Register (Offset = A4h) [Reset = 0000h]

DBFEDHR is shown in Figure 25-103 and described in Table 25-61.

Return to the Summary Table.

Dead-Band Generator Falling Edge Delay High Resolution Register

Figure 25-103. DBFEDHR Register

15	14	13	12	11	10	9	8
DBFEDHR							RESERVED
R/W-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R-0h							R-0h

Table 25-99. DBFEDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	DBFEDHR	R/W	0h	Dead Band Falling Edge Delay High Resolution Bits Reset type: SYSRSn
8	RESERVED	R	0h	Reserved
7-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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39 DBFED Register (Offset = A6h) [Reset = 0000h]

DBFED is shown in Figure 25-104 and described in Table 25-62.

Return to the Summary Table.

Dead-Band Generator Falling Edge Delay Count Register

Figure 25-104. DBFED Register

15	14	13	12	11	10	9	8
RESERVED		DBFED					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
DBFED							
R/W-0h							

Table 25-101. DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-0	DBFED	R/W	0h	Falling Edge Delay Count 14-bit counter Reset type: SYSRSn

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40 TBPHS Register (Offset = C0h) [Reset = 00000000h]

TBPHS is shown in Figure 25-105 and described in Table 25-63.

Return to the Summary Table.

Time Base Phase High

Figure 25-105. TBPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBPHS																TBPHSHR															
R/W-0h																R/W-0h															

Table 25-103. TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TBPHS	R/W	0h	Phase Offset Register These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal. - If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase. - If TBCTL[PHSEN] = 1, then the time-base counter (TBCTR) will be loaded with the phase (TBPHS) when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal (EPWMxSYNCI) or by a software forced synchronization. Reset type: SYSRSn
15-0	TBPHSHR	R/W	0h	Phase Offset (High Resolution) Register. TBPHSHR must not be used. Instead TRREM (HRPWM remainder register) must be used to mimic the functionality of TBPHSHR. The lower 8 bits in this register are ignored - writes are ignored and reads return zero Reset type: SYSRSn

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41 TBPRDHR Register (Offset = C4h) [Reset = 0000h]

TBPRDHR is shown in Figure 25-106 and described in Table 25-64.

Return to the Summary Table.

Time Base Period High Resolution Register

Figure 25-106. TBPRDHR Register

15	14	13	12	11	10	9	8
TBPRDHR							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 25-105. TBPRDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TBPRDHR	R/W	0h	Period High Resolution Bits The upper 8-bits contain the high-resolution portion of the period value. The TBPRDHR register is not affected by the TBCTL[PRDLD] bit. Reads from this register always reflect the shadow register. Likewise writes are also to the shadow register. The TBPRDHR register is only used when the high resolution period feature is enabled. This register is only available with ePWM modules which support high-resolution period control. Reset type: SYSRSn
7-0	RESERVED	R	0h	Reserved

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42 TBPRD Register (Offset = C6h) [Reset = 0000h]

TBPRD is shown in Figure 25-107 and described in Table 25-65.

Return to the Summary Table.

Time Base Period Register

Figure 25-107. TBPRD Register

15	14	13	12	11	10	9	8
TBPRD							
R/W-0h							
7	6	5	4	3	2	1	0
TBPRD							
R/W-0h							

Table 25-107. TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TBPRD	R/W	0h	Time Base Period Register These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. - If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero. - If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - The active and shadow registers share the same memory map address. Reset type: SYSRSn

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43 CMPA Register (Offset = D4h) [Reset = 00000000h]

CMPA is shown in Figure 25-108 and described in Table 25-66.

Return to the Summary Table.

Counter Compare A Register

Figure 25-108. CMPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPA																CMPAHR															
R/W-0h																R/W-0h															

Table 25-109. CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMPA	R/W	0h	Compare A Register The value in the active CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare A' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address. Reset type: SYSRSn
15-0	CMPAHR	R/W	0h	Compare A HRPWM Extension Register The UPPER 8-bits contain the high-resolution portion (most significant 8-bits) of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register. The lower 8 bits in this register are ignored Reset type: SYSRSn

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44 CMPB Register (Offset = D8h) [Reset = 00000000h]

CMPB is shown in Figure 25-109 and described in Table 25-67.

Return to the Summary Table.

Compare B Register

Figure 25-109. CMPB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPB																CMPBHR															
R/W-0h																R/W-0h															

Table 25-111. CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMPB	R/W	0h	Compare B Register The value in the active CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare B' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address. Reset type: SYSRSn
15-0	CMPBHR	R/W	0h	Compare B High Resolution Bits The lower 8 bits in this register are ignored Reset type: SYSRSn

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45 CMPC Register (Offset = DEh) [Reset = 0000h]

CMPC is shown in Figure 25-110 and described in Table 25-68.

Return to the Summary Table.

Counter Compare C Register
LINK feature access should always be 16-bit

Figure 25-110. CMPC Register

15	14	13	12	11	10	9	8
CMPC							
R/W-0h							
7	6	5	4	3	2	1	0
CMPC							
R/W-0h							

Table 25-113. CMPC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMPC	R/W	0h	Compare C Register The value in the active CMPC register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare C' event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWCMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADCMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWCMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address. Reset type: SYSRSn

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46 CMPD Register (Offset = E2h) [Reset = 0000h]

CMPD is shown in Figure 25-111 and described in Table 25-69.

Return to the Summary Table.

Counter Compare D Register
LINK feature access should always be 16-bit

Figure 25-111. CMPD Register

15	14	13	12	11	10	9	8
CMPD							
R/W-0h							
7	6	5	4	3	2	1	0
CMPD							
R/W-0h							

Table 25-115. CMPD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMPD	R/W	0h	Compare D Register The value in the active CMPD register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare D' event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWDMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWDMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADDMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWDMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address. Reset type: SYSRSn

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47 GLDCTL2 Register (Offset = E8h) [Reset = 0000h]

GLDCTL2 is shown in Figure 25-112 and described in Table 25-70.

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Global PWM Load Control Register 2

Figure 25-112. GLDCTL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						GFRCLD	OSHTLD
R-0-0h						R-0/W1S-0h	R-0/W1S-0h

Table 25-117. GLDCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R-0	0h	Reserved
1	GFRCLD	R-0/W1S	0h	Force Load Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Force one load event at the input of the event pre-scale counter. This bit is intended to be used for testing and/or software force loading of the events in global load mode. Reset type: SYSRSn
0	OSHTLD	R-0/W1S	0h	Enable Reload Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence writing 1 to this bit would allow one load strobe event to pass through and block further strobe events. Reset type: SYSRSn

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48 SWVDELVAL Register (Offset = EEh) [Reset = 0000h]

SWVDELVAL is shown in Figure 25-113 and described in Table 25-71.

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Software Valley Mode Delay Register

Figure 25-113. SWVDELVAL Register

15	14	13	12	11	10	9	8
SWVDELVAL							
R/W-0h							
7	6	5	4	3	2	1	0
SWVDELVAL							
R/W-0h							

Table 25-119. SWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SWVDELVAL	R/W	0h	Software Valley Delay Value Register This register can be optionally used define offset value for the hardware calculated delay HWDELAYVAL as defined in VCAPCTL[VDELAYDIV] bits. Reset type: SYSRSn

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49 TZSEL Register (Offset = 100h) [Reset = 0000h]

TZSEL is shown in Figure 25-114 and described in Table 25-72.

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Trip Zone Select Register

Figure 25-114. TZSEL Register

15	14	13	12	11	10	9	8
DCBEVT1	DCAEVT1	OSHT6	OSHT5	OSHT4	OSHT3	OSHT2	OSHT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-121. TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Select 0: Disable DCBEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCBEVT1 as one-shot-trip source for this ePWM module. Reset type: SYSRSn
14	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Select 0: Disable DCAEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCAEVT1 as one-shot-trip source for this ePWM module. Reset type: SYSRSn
13	OSHT6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a one-shot trip source for this ePWM module 1: Enable TZ6 as a one-shot trip source for this ePWM module Reset type: SYSRSn
12	OSHT5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a one-shot trip source for this ePWM module 1: Enable TZ5 as a one-shot trip source for this ePWM module Reset type: SYSRSn
11	OSHT4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a one-shot trip source for this ePWM module 1: Enable TZ4 as a one-shot trip source for this ePWM module Reset type: SYSRSn
10	OSHT3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a one-shot trip source for this ePWM module 1: Enable TZ3 as a one-shot trip source for this ePWM module Reset type: SYSRSn
9	OSHT2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a one-shot trip source for this ePWM module 1: Enable TZ2 as a one-shot trip source for this ePWM module Reset type: SYSRSn
8	OSHT1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a one-shot trip source for this ePWM module 1: Enable TZ1 as a one-shot trip source for this ePWM module Reset type: SYSRSn

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Table 25-121. TZSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Select 0: Disable DCBEVT2 as a CBC trip source for this ePWM module 1: Enable DCBEVT2 as a CBC trip source for this ePWM module Reset type: SYSRSn
6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Select 0: Disable DCAEVT2 as a CBC trip source for this ePWM module 1: Enable DCAEVT2 as a CBC trip source for this ePWM module Reset type: SYSRSn
5	CBC6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a CBC trip source for this ePWM module 1: Enable TZ6 as a CBC trip source for this ePWM module Reset type: SYSRSn
4	CBC5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a CBC trip source for this ePWM module 1: Enable TZ5 as a CBC trip source for this ePWM module Reset type: SYSRSn
3	CBC4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a CBC trip source for this ePWM module 1: Enable TZ4 as a CBC trip source for this ePWM module Reset type: SYSRSn
2	CBC3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a CBC trip source for this ePWM module 1: Enable TZ3 as a CBC trip source for this ePWM module Reset type: SYSRSn
1	CBC2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a CBC trip source for this ePWM module 1: Enable TZ2 as a CBC trip source for this ePWM module Reset type: SYSRSn
0	CBC1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a CBC trip source for this ePWM module 1: Enable TZ1 as a CBC trip source for this ePWM module Reset type: SYSRSn

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50 TZDCSEL Register (Offset = 104h) [Reset = 0000h]

TZDCSEL is shown in Figure 25-115 and described in Table 25-73.

Return to the Summary Table.

Trip Zone Digital Comparator Select Register

Figure 25-115. TZDCSEL Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2			DCBEVT1
R-0-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
DCBEVT1		DCAEVT2			DCAEVT1		
R/W-0h		R/W-0h			R/W-0h		

Table 25-123. TZDCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-9	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Selection 000: Event disabled 001: DCBH = low, DCBL = don't care 010: DCBH = high, DCBL = don't care 011: DCBL = low, DCBH = don't care 100: DCBL = high, DCBH = don't care 101: DCBL = high, DCBH = low 110: Reserved 111: Reserved Reset type: SYSRSn
8-6	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Selection 000: Event disabled 001: DCBH = low, DCBL = don't care 010: DCBH = high, DCBL = don't care 011: DCBL = low, DCBH = don't care 100: DCBL = high, DCBH = don't care 101: DCBL = high, DCBH = low 110: Reserved 111: Reserved Reset type: SYSRSn
5-3	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved Reset type: SYSRSn

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Table 25-123. TZDCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved Reset type: SYSRSn

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51 TZCTL Register (Offset = 108h) [Reset = 0000h]

TZCTL is shown in Figure 25-116 and described in Table 25-74.

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Trip Zone Control Register

Figure 25-116. TZCTL Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2		DCBEVT1	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DCAEVT2		DCAEVT1		TZB		TZA	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 25-125. TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-10	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state. 10: Force EPWMxB to a low state. 11: Do Nothing, trip action is disabled Reset type: SYSRSn
9-8	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state. 10: Force EPWMxB to a low state. 11: Do Nothing, trip action is disabled Reset type: SYSRSn
7-6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled Reset type: SYSRSn
5-4	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled Reset type: SYSRSn
3-2	TZB	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2Trip Action On EPWMxB When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the TZSEL register. 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state 10: Force EPWMxB to a low state 11: Do nothing, no action is taken on EPWMxB. Reset type: SYSRSn

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Table 25-125. TZCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	TZA	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the TZSEL register. 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state 10: Force EPWMxA to a low state 11: Do nothing, no action is taken on EPWMxA. Reset type: SYSRSn

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52 TZCTL2 Register (Offset = 10Ah) [Reset = 0000h]

TZCTL2 is shown in Figure 25-117 and described in Table 25-75.

Return to the Summary Table.

Additional Trip Zone Control Register

Figure 25-117. TZCTL2 Register

15	14	13	12	11	10	9	8
ETZE	RESERVED			TZBD			TZBU
R/W-0h	R-0-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
TZBU		TZAD			TZAU		
R/W-0h		R/W-0h			R/W-0h		

Table 25-127. TZCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ETZE	R/W	0h	TZCTL2 Enable 0: Use trip action from TZCTL (legacy EPWM compatibility) 1: Use trip action defined in TZCTL2, TZCTLDCA and TZCTLDCB. Settings in TZCTL are ignored Reset type: SYSRSn
14-12	RESERVED	R-0	0h	Reserved
11-9	TZBD	R/W	0h	TZ1 to TZ6 Trip Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
8-6	TZBU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
5-3	TZAD	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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Table 25-127. TZCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	TZAU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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53 TZCTLDCA Register (Offset = 10Ch) [Reset = 0000h]

TZCTLDCA is shown in Figure 25-118 and described in Table 25-76.

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Trip Zone Control Register Digital Compare A

Figure 25-118. TZCTLDCA Register

15	14	13	12	11	10	9	8
RESERVED				DCAEVT2D			DCAEVT2U
R-0-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
DCAEVT2U		DCAEVT1D			DCAEVT1U		
R/W-0h		R/W-0h			R/W-0h		

Table 25-129. TZCTLDCA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-9	DCAEVT2D	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
8-6	DCAEVT2U	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
5-3	DCAEVT1D	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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Table 25-129. TZCTLDCA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCAEVT1U	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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54 TZCTLDCB Register (Offset = 10Eh) [Reset = 0000h]

TZCTLDCB is shown in Figure 25-119 and described in Table 25-77.

Return to the Summary Table.

Trip Zone Control Register Digital Compare B

Figure 25-119. TZCTLDCB Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2D			DCBEVT2U
R-0-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
DCBEVT2U		DCBEVT1D			DCBEVT1U		
R/W-0h		R/W-0h			R/W-0h		

Table 25-131. TZCTLDCB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R-0	0h	Reserved
11-9	DCBEVT2D	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
8-6	DCBEVT2U	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn
5-3	DCBEVT1D	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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Table 25-131. TZCTLDCB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	DCBEVT1U	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -> High, High -> Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled Reset type: SYSRSn

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55 TZEINT Register (Offset = 11Ah) [Reset = 0000h]

TZEINT is shown in Figure 25-120 and described in Table 25-78.

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Trip Zone Enable Interrupt Register

Figure 25-120. TZEINT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED
R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0-0h

Table 25-133. TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R-0	0h	Reserved
6	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Interrupt Enable 0: Disabled 1: Enabled Reset type: SYSRSn
5	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Interrupt Enable 0: Disabled 1: Enabled Reset type: SYSRSn
4	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Interrupt Enable 0: Disabled 1: Enabled Reset type: SYSRSn
3	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Interrupt Enable 0: Disabled 1: Enabled Reset type: SYSRSn
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0: Disable one-shot interrupt generation 1: Enable Interrupt generation a one-shot trip event will cause a EPWMx_TZINT PIE interrupt. Reset type: SYSRSn
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0: Disable cycle-by-cycle interrupt generation. 1: Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMx_TZINT PIE interrupt. Reset type: SYSRSn
0	RESERVED	R-0	0h	Reserved

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56 TZFLG Register (Offset = 126h) [Reset = 0000h]

TZFLG is shown in Figure 25-121 and described in Table 25-79.

Return to the Summary Table.

Trip Zone Flag Register

Figure 25-121. TZFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R-0-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 25-135. TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R-0	0h	Reserved
6	DCBEVT2	R	0h	Latched Status Flag for Digital Compare Output B Event 2 0: Indicates no trip event has occurred on DCBEVT2 1: Indicates a trip event has occurred for the event defined for DCBEVT2 Reset type: SYSRSn
5	DCBEVT1	R	0h	Latched Status Flag for Digital Compare Output B Event 1 0: Indicates no trip event has occurred on DCBEVT1 1: Indicates a trip event has occurred for the event defined for DCBEVT1 Reset type: SYSRSn
4	DCAEVT2	R	0h	Latched Status Flag for Digital Compare Output A Event 2 0: Indicates no trip event has occurred on DCAEVT2 1: Indicates a trip event has occurred for the event defined for DCAEVT2 Reset type: SYSRSn
3	DCAEVT1	R	0h	Latched Status Flag for Digital Compare Output A Event 1 0: Indicates no trip event has occurred on DCAEVT1 1: Indicates a trip event has occurred for the event defined for DCAEVT1 Reset type: SYSRSn
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0: No one-shot trip event has occurred. 1: Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the TZCLR register. Reset type: SYSRSn

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Table 25-135. TZFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0: No cycle-by-cycle trip event has occurred. 1: Indicates a trip event has occurred on a signal selected as a cycle-by-cycle trip source. The TZFLG[CBC] bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the signal is automatically cleared when the ePWM time-base counter reaches zero (TBCTR = 0x00) if the trip condition is no longer present. The condition on the signal is only cleared when the TBCTR = 0x00 no matter where in the cycle the CBC flag is cleared. This bit is cleared by writing the appropriate value to the TZCLR register. Reset type: SYSRSn
0	INT	R	0h	Latched Trip Interrupt Status Flag 0: Indicates no interrupt has been generated. 1: Indicates an EPWMx_TZINT PIE interrupt was generated because of a trip condition. No further EPWMx_TZINT PIE interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the TZCLR register. Reset type: SYSRSn

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57 TZCBCFLG Register (Offset = 128h) [Reset = 0000h]

TZCBCFLG is shown in Figure 25-122 and described in Table 25-80.

Return to the Summary Table.

Trip Zone CBC Flag Register

Figure 25-122. TZCBCFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 25-137. TZCBCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7	DCBEVT2	R	0h	Latched Status Flag for Digital Compare B Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT2. 1: Reading a 1 indicates a trip has occured on the DCBEVT2 selected event. Reset type: SYSRSn
6	DCAEVT2	R	0h	Latched Status Flag for Digital Compare A Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT2. 1: Reading a 1 indicates a trip has occured on the DCAEVT2 selected event. Reset type: SYSRSn
5	CBC6	R	0h	Latched Status Flag for CBC6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC6. 1: Reading a 1 indicates a trip has occured on the CBC6 selected event. Reset type: SYSRSn
4	CBC5	R	0h	Latched Status Flag for CBC5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC5. 1: Reading a 1 indicates a trip has occured on the CBC5 selected event. Reset type: SYSRSn
3	CBC4	R	0h	Latched Status Flag for CBC4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC4. 1: Reading a 1 indicates a trip has occured on the CBC4 selected event. Reset type: SYSRSn
2	CBC3	R	0h	Latched Status Flag for CBC3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC3. 1: Reading a 1 indicates a trip has occured on the CBC3 selected event. Reset type: SYSRSn

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Table 25-137. TZCBCFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CBC2	R	0h	Latched Status Flag for CBC2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC2. 1: Reading a 1 indicates a trip has occured on the CBC2 selected event. Reset type: SYSRSn
0	CBC1	R	0h	Latched Status Flag for CBC1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC1. 1: Reading a 1 indicates a trip has occured on the CBC1 selected event. Reset type: SYSRSn

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58 TZOSTFLG Register (Offset = 12Ah) [Reset = 0000h]

TZOSTFLG is shown in Figure 25-123 and described in Table 25-81.

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Trip Zone OST Flag Register

Figure 25-123. TZOSTFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 25-139. TZOSTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7	DCBEVT1	R	0h	Latched Status Flag for Digital Compare B Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT1. 1: Reading a 1 indicates a trip has occured on the DCBEVT1 selected event. Reset type: SYSRSn
6	DCAEVT1	R	0h	Latched Status Flag for Digital Compare A Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT1. 1: Reading a 1 indicates a trip has occured on the DCAEVT1 selected event. Reset type: SYSRSn
5	OST6	R	0h	Latched Status Flag for OST6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST6. 1: Reading a 1 indicates a trip has occured on the OST6 selected event. Reset type: SYSRSn
4	OST5	R	0h	Latched Status Flag for OST5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST5. 1: Reading a 1 indicates a trip has occured on the OST5 selected event. Reset type: SYSRSn
3	OST4	R	0h	Latched Status Flag for OST4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST4. 1: Reading a 1 indicates a trip has occured on the OST4 selected event. Reset type: SYSRSn
2	OST3	R	0h	Latched Status Flag for OST3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST3. 1: Reading a 1 indicates a trip has occured on the OST3 selected event. Reset type: SYSRSn

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Table 25-139. TZOSTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OST2	R	0h	Latched Status Flag for OST2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST2. 1: Reading a 1 indicates a trip has occured on the OST2 selected event. Reset type: SYSRSn
0	OST1	R	0h	Latched Status Flag for OST1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST1. 1: Reading a 1 indicates a trip has occured on the OST1 selected event. Reset type: SYSRSn

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59 TZCLR Register (Offset = 12Eh) [Reset = 0000h]

TZCLR is shown in Figure 25-124 and described in Table 25-82.

Return to the Summary Table.

Trip Zone Clear Register

Figure 25-124. TZCLR Register

15	14	13	12	11	10	9	8
CBCPULSE		RESERVED					
R/W-0h		R-0-0h					
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R-0-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 25-141. TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CBCPULSE	R/W	0h	Clear Pulse for Cycle-By-Cycle (CBC) Trip Latch This bit field determines which pulse clears the CBC trip latch. 00: CTR = zero pulse clears CBC trip latch. (Same as legacy designs.) 01: CTR = PRD pulse clears CBC trip latch. 10: CTR = zero or CTR = PRD pulse clears CBC trip latch. 11: CBC trip latch is not cleared Reset type: SYSRSn
13-7	RESERVED	R-0	0h	Reserved
6	DCBEVT2	R-0/W1S	0h	Clear Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT2 event trip condition. Reset type: SYSRSn
5	DCBEVT1	R-0/W1S	0h	Clear Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT1 event trip condition. Reset type: SYSRSn
4	DCAEVT2	R-0/W1S	0h	Clear Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT2 event trip condition. Reset type: SYSRSn
3	DCAEVT1	R-0/W1S	0h	Clear Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT1 event trip condition. Reset type: SYSRSn
2	OST	R-0/W1S	0h	Clear Flag for One-Shot Trip (OST) Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition. Reset type: SYSRSn
1	CBC	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC) Trip Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition. Reset type: SYSRSn

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Table 25-141. TZCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R-0/W1S	0h	Global Interrupt Clear Flag 0: Has no effect. Always reads back a 0. 1: Clears the trip-interrupt flag for this ePWM module (TZFLG[INT]). NOTE: No further EPWMx_TZINT PIE interrupts will be generated until the flag is cleared. If the TZFLG[INT] bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. Reset type: SYSRSn

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60 TZCBCCLR Register (Offset = 130h) [Reset = 0000h]

TZCBCCLR is shown in Figure 25-125 and described in Table 25-83.

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Trip Zone CBC Clear Register

Figure 25-125. TZCBCCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 25-143. TZCBCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7	DCBEVT2	R-0/W1S	0h	Clear Flag for Digital Compare Output B Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCBEVT2] bit. Reset type: SYSRSn
6	DCAEVT2	R-0/W1S	0h	Clear Flag for Digital Compare Output A Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCAEVT2] bit. Reset type: SYSRSn
5	CBC6	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC6] bit. Reset type: SYSRSn
4	CBC5	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC5] bit. Reset type: SYSRSn
3	CBC4	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC4] bit. Reset type: SYSRSn
2	CBC3	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC3] bit. Reset type: SYSRSn
1	CBC2	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC2] bit. Reset type: SYSRSn
0	CBC1	R-0/W1S	0h	Clear Flag for Cycle-By-Cycle (CBC1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC1] bit. Reset type: SYSRSn

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61 TZOSTCLR Register (Offset = 132h) [Reset = 0000h]

TZOSTCLR is shown in Figure 25-126 and described in Table 25-84.

Return to the Summary Table.

Trip Zone OST Clear Register

Figure 25-126. TZOSTCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 25-145. TZOSTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7	DCBEVT1	R-0/W1S	0h	Clear Flag for Digital Compare Output B Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCBEVT1] bit. Reset type: SYSRSn
6	DCAEVT1	R-0/W1S	0h	Clear Flag for Digital Compare Output A Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCAEVT1] bit. Reset type: SYSRSn
5	OST6	R-0/W1S	0h	Clear Flag for Oneshot (OST6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST6] bit. Reset type: SYSRSn
4	OST5	R-0/W1S	0h	Clear Flag for Oneshot (OST5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST5] bit. Reset type: SYSRSn
3	OST4	R-0/W1S	0h	Clear Flag for Oneshot (OST4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST4] bit. Reset type: SYSRSn
2	OST3	R-0/W1S	0h	Clear Flag for Oneshot (OST3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST3] bit. Reset type: SYSRSn
1	OST2	R-0/W1S	0h	Clear Flag for Oneshot (OST2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST2] bit. Reset type: SYSRSn
0	OST1	R-0/W1S	0h	Clear Flag for Oneshot (OST1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST1] bit. Reset type: SYSRSn

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62 TZFRC Register (Offset = 136h) [Reset = 0000h]

TZFRC is shown in Figure 25-127 and described in Table 25-85.

Return to the Summary Table.

Trip Zone Force Register

Figure 25-127. TZFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED
R-0-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0-0h

Table 25-147. TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R-0	0h	Reserved
6	DCBEVT2	R-0/W1S	0h	Force Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT2 event trip condition and sets the TZFLG[DCBEVT2] bit. Reset type: SYSRSn
5	DCBEVT1	R-0/W1S	0h	Force Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT1 event trip condition and sets the TZFLG[DCBEVT1] bit. Reset type: SYSRSn
4	DCAEVT2	R-0/W1S	0h	Force Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCAEVT2 event trip condition and sets the TZFLG[DCAEVT2] bit. Reset type: SYSRSn
3	DCAEVT1	R-0/W1S	0h	Force Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0 1: Writing 1 forces the DCAEVT1 event trip condition and sets the TZFLG[DCAEVT1] bit. Reset type: SYSRSn
2	OST	R-0/W1S	0h	Force a One-Shot Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a one-shot trip event and sets the TZFLG[OST] bit. Reset type: SYSRSn
1	CBC	R-0/W1S	0h	Force a Cycle-by-Cycle Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a cycle-by-cycle trip event and sets the TZFLG[CBC] bit. Reset type: SYSRSn
0	RESERVED	R-0	0h	Reserved

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63 ETSEL Register (Offset = 148h) [Reset = 0000h]

ETSEL is shown in Figure 25-128 and described in Table 25-86.

Return to the Summary Table.

Event Trigger Selection Register

Figure 25-128. ETSEL Register

15	14	13	12	11	10	9	8
SOCBEN	SOCBSEL			SOCAEN	SOCASEL		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	INTSELCMP	SOCBSELCMP	SOCASELCMP	INTEN	INTSEL		
R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

Table 25-149. ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBEN	R/W	0h	Enable the ADC Start of Conversion B (EPWMxSOCB) Pulse 0: Disable EPWMxSOCB. 1: Enable EPWMxSOCB pulse. Reset type: SYSRSn
14-12	SOCBSEL	R/W	0h	EPWMxSOCB Selection Options These bits determine when a EPWMxSOCB pulse will be generated. 000: Enable DCBEVT1.soc event 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCBSELCMP bit. Reset type: SYSRSn
11	SOCAEN	R/W	0h	Enable the ADC Start of Conversion A (EPWMxSOCA) Pulse 0: Disable EPWMxSOCA. 1: Enable EPWMxSOCA pulse. Reset type: SYSRSn

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Table 25-149. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	SOCASEL	R/W	0h	EPWMxSOCA Selection Options These bits determine when a EPWMxSOCA pulse will be generated. 000: Enable DCAEVT1.soc event 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCASELCMP bit. Reset type: SYSRSn
7	RESERVED	R-0	0h	Reserved
6	INTSELCMP	R/W	0h	EPWMxINT Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to INTSEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to INTSEL selection mux. Reset type: SYSRSn
5	SOCBSELCMP	R/W	0h	EPWMxSOCB Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCBSEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCBSEL selection mux. Reset type: SYSRSn

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Table 25-149. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOCASELCMP	R/W	0h	EPWMxSOCA Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCASEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCASEL selection mux. Reset type: SYSRSn
3	INTEN	R/W	0h	Enable ePWM Interrupt (EPWMx_INT) Generation 0: Disable EPWMx_INT generation 1: Enable EPWMx_INT generation Reset type: SYSRSn
2-0	INTSEL	R/W	0h	ePWM Interrupt (EPWMx_INT) Selection Options 000: Reserved 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD). This mode is useful in up-down count mode. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by INTSELCMP bit. Reset type: SYSRSn

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64 ETPS Register (Offset = 14Ch) [Reset = 0000h]

ETPS is shown in Figure 25-129 and described in Table 25-87.

Return to the Summary Table.

Event Trigger Pre-Scale Register

Figure 25-129. ETPS Register

15	14	13	12	11	10	9	8
SOCBCNT		SOCBPRD		SOCACNT		SOCAPRD	
R-0h		R/W-0h		R-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		SOCPSSEL	INTPSSEL	INTCNT		INTPRD	
R-0-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	

Table 25-151. ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SOCBCNT	R	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Counter Register These bits indicate how many selected ETSEL[SOCBSEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred. Reset type: SYSRSn
13-12	SOCBPRD	R/W	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Period Select These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCBEN] = 1). The SOCB pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCB] = 1). Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared. 00: Disable the SOCB event counter. No EPWMxSOCB pulse will be generated 01: Generate the EPWMxSOCB pulse on the first event: ETPS[SOCBCNT] = 0,1 10: Generate the EPWMxSOCB pulse on the second event: ETPS[SOCBCNT] = 1,0 11: Generate the EPWMxSOCB pulse on the third event: ETPS[SOCBCNT] = 1,1 Reset type: SYSRSn
11-10	SOCACNT	R	0h	ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Counter Register These bits indicate how many selected ETSEL[SOCASEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred. Reset type: SYSRSn

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Table 25-151. ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	SOCAPRD	R/W	0h	ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Period Select These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCAEN] = 1). The SOCA pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCA] = 1). Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared. 00: Disable the SOCA event counter. No EPWMxSOCA pulse will be generated 01: Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 0,1 10: Generate the EPWMxSOCA pulse on the second event: ETPS[SOCACNT] = 1,0 11: Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 1,1 Reset type: SYSRSn
7-6	RESERVED	R-0	0h	Reserved
5	SOCPSSEL	R/W	0h	EPWMxSOC A/B Pre-Scale Selection Bits 0: Selects ETPS [SOCACNT/SOCBCNT] and [SOCAPRD/ SOCBPRD] registers to determine frequency of events (SOC pulse once every 0-3 events). 1: Selects ETSOCPS [SOCACNT2/SOCBCNT2] and [SOCAPRD2/ SOCBPRD2] registers to determine frequency of events (SOC pulse once every 0-15 events). Reset type: SYSRSn
4	INTPSSEL	R/W	0h	EPWMxINTn Pre-Scale Selection Bits 0: Selects ETPS [INTCNT, and INTPRD] registers to determine frequency of events (interrupt once every 0-3 events). 1: Selects ETINTPS [INTCNT2, and INTPRD2] registers to determine frequency of events (interrupt once every 0-15 events). Reset type: SYSRSn
3-2	INTCNT	R	0h	ePWM Interrupt Event (EPWMx_INT) Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD]. 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred. Reset type: SYSRSn

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Table 25-151. ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	INTPRD	R/W	0h	ePWM Interrupt (EPWMx_INT) Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled (ETSEL[INT] = 1). If the interrupt status flag is set from a previous interrupt (ETFLG[INT] = 1) then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared. Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented. 00: Disable the interrupt event counter. No interrupt will be generated and ETFRC[INT] is ignored. 01: Generate an interrupt on the first event INTCNT = 01 (first event) 10: Generate interrupt on ETPS[INTCNT] = 1,0 (second event) 11: Generate interrupt on ETPS[INTCNT] = 1,1 (third event) Reset type: SYSRSn

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65 ETFLG Register (Offset = 150h) [Reset = 0000h]

ETFLG is shown in Figure 25-130 and described in Table 25-88.

Return to the Summary Table.

Event Trigger Flag Register

Figure 25-130. ETFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0-0h				R-0h	R-0h	R-0-0h	R-0h

Table 25-153. ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R-0	0h	Reserved
3	SOCB	R	0h	Latched ePWM ADC Start-of-Conversion A (EPWMxSOCB) Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCB output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on EPWMxSOCB. The EPWMxSOCB output will continue to be generated even if the flag bit is set. Reset type: SYSRSn
2	SOCA	R	0h	Latched ePWM ADC Start-of-Conversion A (EPWMxSOCA) Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCA output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on EPWMxSOCA. The EPWMxSOCA output will continue to be generated even if the flag bit is set. Reset type: SYSRSn
1	RESERVED	R-0	0h	Reserved
0	INT	R	0h	Latched ePWM Interrupt (EPWMx_INT) Status Flag 0: Indicates no event occurred 1: Indicates that an ePWMx interrupt (EPWMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the ETFLG[INT] bit is still set. If an interrupt is pending, it will not be generated until after the ETFLG[INT] bit is cleared. Reset type: SYSRSn

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66 ETCLR Register (Offset = 154h) [Reset = 0000h]

ETCLR is shown in Figure 25-131 and described in Table 25-89.

Return to the Summary Table.

Event Trigger Clear Register

Figure 25-131. ETCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0-0h				R-0/W1S-0h	R-0/W1S-0h	R-0-0h	R-0/W1S-0h

Table 25-155. ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R-0	0h	Reserved
3	SOCB	R-0/W1S	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCB) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCB] flag bit Reset type: SYSRSn
2	SOCA	R-0/W1S	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCA) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCA] flag bit Reset type: SYSRSn
1	RESERVED	R-0	0h	Reserved
0	INT	R-0/W1S	0h	ePWM Interrupt (EPWMx_INT) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[INT] flag bit and enable further interrupts pulses to be generated Reset type: SYSRSn

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67 ETFRC Register (Offset = 158h) [Reset = 0000h]

ETFRC is shown in Figure 25-132 and described in Table 25-90.

Return to the Summary Table.

Event Trigger Force Register

Figure 25-132. ETFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0-0h				R-0/W1S-0h	R-0/W1S-0h	R-0-0h	R-0/W1S-0h

Table 25-157. ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R-0	0h	Reserved
3	SOCB	R-0/W1S	0h	SOCB Force Bit The SOCB pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCB] flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates a pulse on EPWMxSOCB and set the SOCBFLG bit. This bit is used for test purposes. Reset type: SYSRSn
2	SOCA	R-0/W1S	0h	SOCA Force Bit The SOCA pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCA] flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates a pulse on EPWMxSOCA and set the SOCAFLG bit. This bit is used for test purposes. Reset type: SYSRSn
1	RESERVED	R-0	0h	Reserved
0	INT	R-0/W1S	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register. The INT flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates an interrupt on EPWMxINT and set the INT flag bit. This bit is used for test purposes. Reset type: SYSRSn

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68 ETINTPS Register (Offset = 15Ch) [Reset = 0000h]

ETINTPS is shown in Figure 25-133 and described in Table 25-91.

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Event-Trigger Interrupt Pre-Scale Register

Figure 25-133. ETINTPS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
INTCNT2				INTPRD2			
R-0h				R/W-0h			

Table 25-159. ETINTPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7-4	INTCNT2	R	0h	EPWMxINT Counter 2 When ETPS[INTPSSEL]=1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events Reset type: SYSRSn
3-0	INTPRD2	R/W	0h	EPWMxINT Period 2 Select When ETPS[INTPSSEL] = 1, these bits select how many selected events need to occur before an interrupt is generated: 0000: Disable counter 0001: Generate interrupt on INTCNT = 1 (first event) 0010: Generate interrupt on INTCNT = 2 (second event) 0011: Generate interrupt on INTCNT = 3 (third event) 0100: Generate interrupt on INTCNT = 4 (fourth event) ... 1111: Generate interrupt on INTCNT = 15 (fifteenth event) Reset type: SYSRSn

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69 ETSOCPS Register (Offset = 160h) [Reset = 0000h]

ETSOCPS is shown in Figure 25-134 and described in Table 25-92.

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Event-Trigger SOC Pre-Scale Register

Figure 25-134. ETSOCPS Register

15	14	13	12	11	10	9	8
SOCBCNT2				SOCBPRD2			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
SOCACNT2				SOCAPRD2			
R-0h				R/W-0h			

Table 25-161. ETSOCPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SOCBCNT2	R	0h	EPWMxSOCB Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events Reset type: SYSRSn
11-8	SOCBPRD2	R/W	0h	EPWMxSOCB Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCB pulse is generated: 0000: Disable counter 0001: Generate SOC pulse on SOCBCNT2 = 1 (first event) 0010: Generate SOC pulse on SOCBCNT2 = 2 (second event) 0011: Generate SOC pulse on SOCBCNT2 = 3 (third event) 0100: Generate SOC pulse on SOCBCNT2 = 4 (fourth event) ... 1111: Generate SOC pulse on SOCBCNT2 = 15 (fifteenth event) Reset type: SYSRSn
7-4	SOCACNT2	R	0h	EPWMxSOCA Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events Reset type: SYSRSn

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Table 25-161. ETSOCPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	SOCAPRD2	R/W	0h	EPWMxSOCA Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCA pulse is generated: 0000: Disable counter 0001: Generate SOC pulse on SOCACNT2 = 1 (first event) 0010: Generate SOC pulse on SOCACNT2 = 2 (second event) 0011: Generate SOC pulse on SOCACNT2 = 3 (third event) 0100: Generate SOC pulse on SOCACNT2 = 4 (fourth event) ... 1111: Generate SOC pulse on SOCACNT2 = 15 (fifteenth event) Reset type: SYSRSn

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70 ETCNTINITCTL Register (Offset = 164h) [Reset = 0000h]

ETCNTINITCTL is shown in Figure 25-135 and described in Table 25-93.

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Event-Trigger Counter Initialization Control Register

Figure 25-135. ETCNTINITCTL Register

15	14	13	12	11	10	9	8
SOCBINITEN	SOCAINITEN	INTINITEN	SOCBINITFRC	SOCAINITFRC	INTINITFRC	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0-0h							

Table 25-163. ETCNTINITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBINITEN	R/W	0h	EPWMxSOCB Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCB counter with contents of ETCNTINIT[SOCBINIT] on a SYNC event or software force. Reset type: SYSRSn
14	SOCAINITEN	R/W	0h	EPWMxSOCA Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCA counter with contents of ETCNTINIT[SOCAINIT] on a SYNC event or software force. Reset type: SYSRSn
13	INTINITEN	R/W	0h	EPWMxINT Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxINT counter 2 with contents of ETCNTINIT[INTINIT] on a SYNC event or software force. Reset type: SYSRSn
12	SOCBINITFRC	R-0/W1S	0h	EPWMxSOCB Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCB counter to be initialized with the contents of ETCNTINIT[SOCBINIT]. Reset type: SYSRSn
11	SOCAINITFRC	R-0/W1S	0h	EPWMxSOCA Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCA counter to be initialized with the contents of ETCNTINIT[SOCAINIT]. Reset type: SYSRSn
10	INTINITFRC	R-0/W1S	0h	EPWMxINT Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxINT counter to be initialized with the contents of ETCNTINIT[INTINIT]. Reset type: SYSRSn
9-0	RESERVED	R-0	0h	Reserved

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71 ETCNTINIT Register (Offset = 168h) [Reset = 0000h]

ETCNTINIT is shown in Figure 25-136 and described in Table 25-94.

Return to the Summary Table.

Event-Trigger Counter Initialization Register

Figure 25-136. ETCNTINIT Register

15	14	13	12	11	10	9	8
RESERVED				SOCBINIT			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
SOCAINIT				INTINIT			
R/W-0h				R/W-0h			

Table 25-165. ETCNTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-8	SOCBINIT	R/W	0h	EPWMxSOCB Counter 2 Initialization Bits The ET EPWMxSOCB counter is initialized with the contents of this register on an ePWM SYNC event or a software force. Reset type: SYSRSn
7-4	SOCAINIT	R/W	0h	EPWMxSOCA Counter 2 Initialization Bits The ET EPWMxSOCA counter is initialized with the contents of this register on an ePWM SYNC event or a software force. Reset type: SYSRSn
3-0	INTINIT	R/W	0h	EPWMxINT Counter 2 Initialization Bits The ET EPWMxINT counter is initialized with the contents of this register on an ePWM SYNC event or a software force. Reset type: SYSRSn

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72 DCTRIPSEL Register (Offset = 180h) [Reset = 0000h]

DCTRIPSEL is shown in Figure 25-137 and described in Table 25-95.

Return to the Summary Table.

Digital Compare Trip Select Register

Figure 25-137. DCTRIPSEL Register

15	14	13	12	11	10	9	8
DCBLCOMPSEL				DCBHCOMPSEL			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
DCALCOMPSEL				DCAHCOMPSEL			
R/W-0h				R/W-0h			

Table 25-167. DCTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DCBLCOMPSEL	R/W	0h	Digital Compare B Low Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBLTRIPSEL register ORed together) Reset type: SYSRSn
11-8	DCBHCOMPSEL	R/W	0h	Digital Compare B High Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBHTRIPSEL register ORed together) Reset type: SYSRSn
7-4	DCALCOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCALTRIPSEL register ORed together) Reset type: SYSRSn

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Table 25-167. DCTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DCAHCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCAHTRIPSEL register ORed together) Reset type: SYSRSn

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73 DCACTL Register (Offset = 186h) [Reset = 0000h]

DCACTL is shown in Figure 25-138 and described in Table 25-96.

Return to the Summary Table.

Digital Compare A Control Register

Figure 25-138. DCACTL Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED		EVT2FRCSYNCSEL	EVT2SRCSEL
R-0h	R/W-0h		R/W-0h	R-0-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-169. DCACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCAEVT2LAT signal. 0 : The DCAEVT2LAT latch is cleared. 1 : The DCAEVT2LAT latch is set. Reset type: SYSRSn
14-13	EVT2LATCLRSEL	R/W	0h	DCAEVT2 Latched clear source select: 00: CNT_ZERO event clears DCAEVT2 latch. 01: PRD_EQ event clears DCAEVT2 latch. 10: CNT_ZERO event or PRD_EQ event clears DCAEVT2 latch. 11: Reserved. Reset type: SYSRSn
12	EVT2LATSEL	R/W	0h	DCAEVT2 Latched signal select: 0: Does not select the DCAEVT2 latched signal as source of DCAEVT2.force. 1: Selects the DCAEVT2 latched signal as source of DCAEVT2.force. Reset type: SYSRSn
11-10	RESERVED	R-0	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCAEVT2 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously Reset type: SYSRSn
8	EVT2SRCSEL	R/W	0h	DCAEVT2 Source Signal Select 0: Source Is DCAEVT2 Signal 1: Source Is DCEVTFILT Signal Reset type: SYSRSn
7	EVT1LAT	R	0h	Indicates the status of DCAEVT1LAT signal. 0 : The DCAEVT1LAT latch is cleared. 1 : The DCAEVT1LAT latch is set. Reset type: SYSRSn

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Table 25-169. DCACTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	EVT1LATCLRSEL	R/W	0h	DCAEVT1 Latched clear source select: 00: CNT_ZERO event clears DCAEVT1 latch. 01: PRD_EQ event clears DCAEVT1 latch. 10: CNT_ZERO event or PRD_EQ event clears DCAEVT1 latch. 11 : Reserved. Reset type: SYSRSn
4	EVT1LATSEL	R/W	0h	DCAEVT1 Latched signal select: 0: Does not select the DCAEVT1 latched signal as source of DCAEVT1.force. 1: Selects the DCAEVT1 latched signal as source of DCAEVT1.force. Reset type: SYSRSn
3	EVT1SYNCE	R/W	0h	DCAEVT1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled Reset type: SYSRSn
2	EVT1SOCE	R/W	0h	DCAEVT1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled Reset type: SYSRSn
1	EVT1FRCSYNCSEL	R/W	0h	DCAEVT1 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously Reset type: SYSRSn
0	EVT1SRCSEL	R/W	0h	DCAEVT1 Source Signal Select 0: Source Is DCAEVT1 Signal 1: Source Is DCEVTFILT Signal Reset type: SYSRSn

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74 DCBCTL Register (Offset = 188h) [Reset = 0000h]

DCBCTL is shown in Figure 25-139 and described in Table 25-97.

Return to the Summary Table.

Digital Compare B Control Register

Figure 25-139. DCBCTL Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED		EVT2FRCSYNCSEL	EVT2SRCSEL
R-0h	R/W-0h		R/W-0h	R-0-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-171. DCBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCBEVT2LAT signal. 0 The DCBEVT2LAT latch is cleared. 1 The DCBEVT2LAT latch is set. Reset type: SYSRSn
14-13	EVT2LATCLRSEL	R/W	0h	DCBEVT2 Latched clear source select: 00 CNT_ZERO event clears DCBEVT2 latch. 01 PRD_EQ event clears DCBEVT2 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT2 latch. 11 Reserved. Reset type: SYSRSn
12	EVT2LATSEL	R/W	0h	DCBEVT2 Latched signal select: 0 Does not select the DCBEVT2 latched signal (Refer figure 'Modifications to DCBEVT1.force/DCBEVT2.force generation.') as source of DCBEVT2.force. 1 Selects the DCBEVT2 latched signal as source of DCBEVT2.force. Reset type: SYSRSn
11-10	RESERVED	R-0	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCBEVT2 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously Reset type: SYSRSn
8	EVT2SRCSEL	R/W	0h	DCBEVT2 Source Signal Select 0: Source Is DCBEVT2 Signal 1: Source Is DCEVTFILT Signal Reset type: SYSRSn
7	EVT1LAT	R	0h	Indicates the status of DCBEVT1LAT signal. 0 The DCBEVT1LAT latch is cleared. 1 The DCBEVT1LAT latch is set. Reset type: SYSRSn

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Table 25-171. DCBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	EVT1LATCLRSEL	R/W	0h	DCBEVT1 Latched clear source select: 00 CNT_ZERO event clears DCBEVT1 latch. 01 PRD_EQ event clears DCBEVT1 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT1 latch. 11 Reserved. Reset type: SYSRSn
4	EVT1LATSEL	R/W	0h	DCBEVT1 Latched signal select: 0 Does not select the DCBEVT1 latched signal (Refer figure 'Modifications to DCBEVT1.force/DCBEVT2.force generation.') as source of DCBEVT1.force. 1 Selects the DCBEVT1 latched signal as source of DCBEVT1.force. Reset type: SYSRSn
3	EVT1SYNCE	R/W	0h	DCBEVT1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled Reset type: SYSRSn
2	EVT1SOCE	R/W	0h	DCBEVT1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled Reset type: SYSRSn
1	EVT1FRCSYNCSEL	R/W	0h	DCBEVT1 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously Reset type: SYSRSn
0	EVT1SRCSEL	R/W	0h	DCBEVT1 Source Signal Select 0: Source Is DCBEVT1 Signal 1: Source Is DCEVTFILT Signal Reset type: SYSRSn

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75 DCFCTL Register (Offset = 18Eh) [Reset = 0000h]

DCFCTL is shown in Figure 25-140 and described in Table 25-98.

Return to the Summary Table.

Digital Compare Filter Control Register

Figure 25-140. DCFCTL Register

15	14	13	12	11	10	9	8
EDGESTATUS			EDGECOUNT			EDGEMODE	
R-0h			R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	EDGEFILTSEL	PULSESEL		BLANKINV	BLANKE	SRCSEL	
R-0-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	

Table 25-173. DCFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	EDGESTATUS	R	0h	Edge Status: These bits reflect the total number of edges currently captured. When the value matches the EDGECOUNT, the status bits are set to zero. and a TBCLK wide pulse is generated which can then be output on the DCEVTFILT signal. The edge counter can be reset by writing 000 to the EDGECOUNT value: Reset type: SYSRSn
12-10	EDGECOUNT	R/W	0h	Edge Count: These bits select how many edges to count before generating a TBCLK wide pulse on the DCEVTFILT signal: 000: no edges, reset current EDGESTATUS bits to 0,0,0 001: 1 edge 010: 2 edges 011: 3 edges 100: 4 edges 101: 5 edges 110: 6 edges 111: 7 edges Reset type: SYSRSn
9-8	EDGEMODE	R/W	0h	Edge Mode Select: 00: Low To High Edge 01: High To Low Edge 10: Both Edges 11: Reserved Reset type: SYSRSn
7	RESERVED	R-0	0h	Reserved
6	EDGEFILTSEL	R/W	0h	Edge Filter Select: 0: Edge Filter Not Selected 1: Edge Filter Selected Reset type: SYSRSn
5-4	PULSESEL	R/W	0h	Pulse Select For Blanking & Capture Alignment 00: Time-base counter equal to period (TBCTR = TBPRD) 01: Time-base counter equal to zero (TBCTR = 0x00) 10: Time-base counter equal to zero (TBCTR = 0x00) or period (TBCTR = TBPRD) 11: BLANKPULSEMIX Reset type: SYSRSn

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Table 25-173. DCFCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BLANKINV	R/W	0h	Blanking Window Inversion 0: Blanking window not inverted 1: Blanking window inverted Reset type: SYSRSn
2	BLANKE	R/W	0h	Blanking Window Enable/Disable 0: Blanking window is disabled 1: Blanking window is enabled Reset type: SYSRSn
1-0	SRCSEL	R/W	0h	Filter Block Signal Source Select 00: Source Is DCAEVT1 Signal 01: Source Is DCAEVT2 Signal 10: Source Is DCBEVT1 Signal 11: Source Is DCBEVT2 Signal Reset type: SYSRSn

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76 DCCAPCTL Register (Offset = 190h) [Reset = 0000h]

DCCAPCTL is shown in Figure 25-141 and described in Table 25-99.

Return to the Summary Table.

Digital Compare Capture Control Register

Figure 25-141. DCCAPCTL Register

15	14	13	12	11	10	9	8
CAPMODE	CAPCLR	CAPSTS	RESERVED				
R/W-0h	R-0/W1S-0h	R-0h	R-0-0h				
7	6	5	4	3	2	1	0
RESERVED						SHDWMODE	CAPE
R-0-0h						R/W-0h	R/W-0h

Table 25-175. DCCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CAPMODE	R/W	0h	Counter Capture Mode 0: When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs, further trip (capture) events are ignored until the next PRD_eq or CNT_zero event (as selected by the PULSESEL bit in the DCFCTL register) re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCCAPCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCCAPCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event (whichever is selected by PULSESEL bit in DCFCTL register). CPU reads of this register will return the shadow register value. 1: When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs - it will set the CAPSTS flag and further trip (capture) events are ignored until this bit is cleared. CAPSTS can be cleared by writing to CAPCLR bit in DCCAPCTL register and it re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCCAPCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCCAPCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event (whichever is selected by PULSESEL bit in DCFCTL register). CPU reads of this register will return the shadow register value. Reset type: SYSRSn
14	CAPCLR	R-0/W1S	0h	DC Capture Latched Status Clear Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear this CAPSTS (set) condition. Reset type: SYSRSn
13	CAPSTS	R	0h	Latched Status Flag for Capture Event 0: No DC capture event occurred. 1: A DC capture event has occurred. Reset type: SYSRSn
12-2	RESERVED	R-0	0h	Reserved

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Table 25-175. DCCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SHDWMODE	R/W	0h	TBCTR Counter Capture Shadow Select Mode 0: Enable shadow mode. The DCCAP active register is copied to shadow register on a TBCTR = TBPRD or TBCTR = zero event as defined by the DCFCTL[PULSESEL] bit. CPU reads of the DCCAP register will return the shadow register contents. 1: Active Mode. In this mode the shadow register is disabled. CPU reads from the DCCAP register will always return the active register contents. Reset type: SYSRSn
0	CAPE	R/W	0h	TBCTR Counter Capture Enable/Disable 0: Disable the time-base counter capture. 1: Enable the time-base counter capture. Reset type: SYSRSn

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77 DCFOFFSET Register (Offset = 192h) [Reset = 0000h]

DCFOFFSET is shown in Figure 25-142 and described in Table 25-100.

Return to the Summary Table.

Digital Compare Filter Offset Register

Figure 25-142. DCFOFFSET Register

15	14	13	12	11	10	9	8
DCFOFFSET							
R/W-0h							
7	6	5	4	3	2	1	0
DCFOFFSET							
R/W-0h							

Table 25-177. DCFOFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFOFFSET	R/W	0h	Blanking Window Offset These 16-bits specify the number of TBCLK cycles from the blanking window reference to the point when the blanking window is applied. The blanking window reference is either period or zero as defined by the DCFCTL[PULSESEL] bit. This offset register is shadowed and the active register is loaded at the reference point defined by DCFCTL[PULSESEL]. The offset counter is also initialized and begins to count down when the active register is loaded. When the counter expires, the blanking window is applied. If the blanking window is currently active, then the blanking window counter is restarted. Reset type: SYSRSn

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78 DCFOFFSETCNT Register (Offset = 194h) [Reset = 0000h]

DCFOFFSETCNT is shown in Figure 25-143 and described in Table 25-101.

Return to the Summary Table.

Digital Compare Filter Offset Counter Register

Figure 25-143. DCFOFFSETCNT Register

15	14	13	12	11	10	9	8
DCFOFFSETCNT							
R-0h							
7	6	5	4	3	2	1	0
DCFOFFSETCNT							
R-0h							

Table 25-179. DCFOFFSETCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFOFFSETCNT	R	0h	Blanking Offset Counter These 16-bits are read only and indicate the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next period or zero event as defined by the DCFCTL[PULSESEL] bit. The offset counter is not affected by the free/soft emulation bits. That is, it will always continue to count down if the device is halted by a emulation stop. Reset type: SYSRSn

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79 DCFWINDOW Register (Offset = 196h) [Reset = 0000h]

DCFWINDOW is shown in Figure 25-144 and described in Table 25-102.

Return to the Summary Table.

Digital Compare Filter Window Register

Figure 25-144. DCFWINDOW Register

15	14	13	12	11	10	9	8
DCFWINDOW							
R/W-0h							
7	6	5	4	3	2	1	0
DCFWINDOW							
R/W-0h							

Table 25-181. DCFWINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFWINDOW	R/W	0h	Blanking Window Width 00h: No blanking window is generated. 01-FFFFh: Specifies the width of the blanking window in TBCLK cycles. The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is not restarted and the blanking window is cut short prematurely. Care should be taken to avoid this situation. The blanking window can cross a PWM period boundary. Reset type: SYSRSn

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80 DCFWINDOWCNT Register (Offset = 198h) [Reset = 0000h]

DCFWINDOWCNT is shown in Figure 25-145 and described in Table 25-103.

Return to the Summary Table.

Digital Compare Filter Window Counter Register

Figure 25-145. DCFWINDOWCNT Register

15	14	13	12	11	10	9	8
DCFWINDOWCNT							
R-0h							
7	6	5	4	3	2	1	0
DCFWINDOWCNT							
R-0h							

Table 25-183. DCFWINDOWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCFWINDOWCNT	R	0h	Blanking Window Counter These 16 bits are read only and indicate the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again. Reset type: SYSRSn

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81 BLANKPULSEMIXSEL Register (Offset = 19Ah) [Reset = 0000h]

BLANKPULSEMIXSEL is shown in Figure 25-146 and described in Table 25-104.

Return to the Summary Table.

Blanking window trigger pulse select register

Figure 25-146. BLANKPULSEMIXSEL Register

15	14	13	12	11	10	9	8
RESERVED						CDD	CDU
R-0-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-185. BLANKPULSEMIXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R-0	0h	Reserved
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event Reset type: SYSRSn
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event Reset type: SYSRSn
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event Reset type: SYSRSn
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event Reset type: SYSRSn
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event Reset type: SYSRSn
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal (BLANKPULSEMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event Reset type: SYSRSn

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Table 25-185. BLANKPULSEMIXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event Reset type: SYSRSn
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event Reset type: SYSRSn
1	PRD	R/W	0h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the blanking window trigger (BLANKPULSEMIX). 0: Period match event is not enabled 1: Enable period match event Reset type: SYSRSn
0	ZRO	R/W	0h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the blanking window trigger (BLANKPULSEMIX). 0: Zero match event is not enabled 1: Enable zero match event Reset type: SYSRSn

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82 DCCAP Register (Offset = 19Eh) [Reset = 0000h]

DCCAP is shown in Figure 25-147 and described in Table 25-105.

Return to the Summary Table.

Digital Compare Counter Capture Register

Figure 25-147. DCCAP Register

15	14	13	12	11	10	9	8
DCCAP							
R-0h							
7	6	5	4	3	2	1	0
DCCAP							
R-0h							

Table 25-187. DCCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DCCAP	R	0h	Digital Compare Time-Base Counter Capture To enable time-base counter capture, set the DCCAPCLT[CAPE] bit to 1. If enabled, reflects the value of the time-base counter (TBCTR) on the low to high edge transition of a filtered (DCEVTFLT) event. Further capture events are ignored until the next period or zero as selected by the DCFCTL[PULSESEL] bit. Shadowing of DCCAP is enabled and disabled by the DCCAPCTL[SHDWMODE] bit. By default this register is shadowed. - If DCCAPCTL[SHDWMODE] = 0, then the shadow is enabled. In this mode, the active register is copied to the shadow register on the TBCTR = TBPRD or TBCTR = zero as defined by the DCFCTL[PULSESEL] bit. CPU reads of this register will return the shadow register value. - If DCCAPCTL[SHDWMODE] = 1, then the shadow register is disabled. In this mode, CPU reads will return the active register value. The active and shadow registers share the same memory map address. Reset type: SYSRSn

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83 DCAHTRIPSEL Register (Offset = 1A4h) [Reset = 0000h]

DCAHTRIPSEL is shown in Figure 25-148 and described in Table 25-106.

Return to the Summary Table.

Digital Compare AH Trip Select

Figure 25-148. DCAHTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-189. DCAHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAH mux Reset type: SYSRSn

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Table 25-189. DCAHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAH mux Reset type: SYSRSn
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAH mux Reset type: SYSRSn

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84 DCALTRIPSEL Register (Offset = 1A6h) [Reset = 0000h]

DCALTRIPSEL is shown in Figure 25-149 and described in Table 25-107.

Return to the Summary Table.

Digital Compare AL Trip Select

Figure 25-149. DCALTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-191. DCALTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux Reset type: SYSRSn

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Table 25-191. DCALTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux Reset type: SYSRSn

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85 DCBHTRIPSEL Register (Offset = 1A8h) [Reset = 0000h]

DCBHTRIPSEL is shown in Figure 25-150 and described in Table 25-108.

Return to the Summary Table.

Digital Compare BH Trip Select

Figure 25-150. DCBHTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-193. DCBHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCBH mux Reset type: SYSRSn

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Table 25-193. DCBHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCBH mux Reset type: SYSRSn
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCBH mux Reset type: SYSRSn

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86 DCBLTRIPSEL Register (Offset = 1AAh) [Reset = 0000h]

DCBLTRIPSEL is shown in Figure 25-151 and described in Table 25-109.

Return to the Summary Table.

Digital Compare BL Trip Select

Figure 25-151. DCBLTRIPSEL Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 25-195. DCBLTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux Reset type: SYSRSn

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Table 25-195. DCBLTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux Reset type: SYSRSn
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux Reset type: SYSRSn

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87 EPWMLOCK Register (Offset = 1F4h) [Reset = 00000000h]

EPWMLOCK is shown in Figure 25-152 and described in Table 25-110.

Return to the Summary Table.

EPWM Lock Register

Figure 25-152. EPWMLOCK Register

31	30	29	28	27	26	25	24
KEY							
R-0/W-0h							
23	22	21	20	19	18	17	16
KEY							
R-0/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			DCLOCK	TZCLRLOCK	TZCFGLOCK	GLLOCK	HRLOCK
R-0h			R/WOnce-0h	R/WOnce-0h	R/WOnce-0h	R/WOnce-0h	R/WOnce-0h

Table 25-197. EPWMLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	KEY	R-0/W	0h	Write to this register succeeds only if this field is written with a value of 0xa5a5 Note: [1] Due to this KEY, only 32-bit writes will succeed (provided the KEY matches). 16-bit writes to the upper or lower half of this register will be ignored Reset type: SYSRSn
15-5	RESERVED	R	0h	Reserved
4	DCLOCK	R/WOnce	0h	0:Digital Compare registers from 0xC0 to 0xD9 offsets are protected by EALLOW. 1: Digital Compare registers from 0xC0 to 0xD9 offsets are locked and not writable. Reset type: SYSRSn
3	TZCLRLOCK	R/WOnce	0h	0:Trip Zone registers from 0x97 to 0x9B offsets are protected by EALLOW. 1: Trip Zone registers from 0x97 to 0x9B offsets are locked and not writable. Reset type: SYSRSn
2	TZCFGLOCK	R/WOnce	0h	0:TripZone registers from 0x80 to 0x8D and TZTRIPOUTSEL at 0x9D offsets are protected by EALLOW. 1: TripZone registers from 0x80 to 0x8D and TZTRIPOUTSEL at 0x9D offsets are locked and not writable. Reset type: SYSRSn
1	GLLOCK	R/WOnce	0h	0:Global Load registers from 0x34 to 0x35 offsets are protected by EALLOW. 1: Global Load registers from 0x34 to 0x35 offsets are locked and not writable Reset type: SYSRSn

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Table 25-197. EPWMLOCK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HRLOCK	R/WOnce	0h	0: HRPWM registers from 0x20 to 0x2D offsets are protected by EALLOW 1: HRPWM registers from 0x20 and 0x2D offsets are locked and not writable. Reset type: SYSRSn

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88 HWVDELVAL Register (Offset = 1FAh) [Reset = 0000h]

HWVDELVAL is shown in Figure 25-153 and described in Table 25-111.

Return to the Summary Table.

Hardware Valley Mode Delay Register

Figure 25-153. HWVDELVAL Register

15	14	13	12	11	10	9	8
HWVDELVAL							
R-0h							
7	6	5	4	3	2	1	0
HWVDELVAL							
R-0h							

Table 25-199. HWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	HWVDELVAL	R	0h	Hardware Valley Delay Value Register This read only register reflects the hardware delay value calculated by the equations defined in VCAPCTL[VDELAYDIV]. This reflects the latest value from the hardware calculations and can change every time valley capture sequence is triggered and VCAP1 and VCAP2 values are updated. Reset type: SYSRSn

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89 VCNTVAL Register (Offset = 1FCh) [Reset = 0000h]

VCNTVAL is shown in Figure 25-154 and described in Table 25-112.

Return to the Summary Table.

Hardware Valley Counter Register

Figure 25-154. VCNTVAL Register

15	14	13	12	11	10	9	8
VCNTVAL							
R-0h							
7	6	5	4	3	2	1	0
VCNTVAL							
R-0h							

Table 25-201. VCNTVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VCNTVAL	R	0h	Valley Time Base Counter Register This register reflects the captured VCNT value upon occurrence of STOPEDGE selected in VCNTCFG register. Reset type: SYSRSn

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Chapter 26

Multi-Channel Pulse Width Modulator (MCPWM)

The Multi-channel pulse-width modulator (MCPWM) peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. These systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS), and other forms of power conversion. The MCPWM peripheral can also perform a digital-to-analog (DAC) function, where the duty cycle is equivalent to a DAC analog value; sometimes referred to as a power DAC.

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26.1 Introduction

The MCPWM is capable of generating complex waveforms with minimal CPU overhead or intervention. The peripheral is comprised of several submodules, each with an independent function. This chapter contains sections describing each submodule.

Note

Signal and submodule names follow the naming convention MCPWMx_yA and MCPWMx_yB where:

- 'x' indicates a generic module of MCPWM
- 'y' indicates an A/B channel pair

For example, the MCPWM module 1 and channel pair 3 signal names are:

- MCPWM1_3A
- MCPWM1_3B

26.1.1 EPWM Related Collateral

Foundational Materials

- *Real-Time Control Reference Guide*
  - Refer to the PWM section

Getting Started Materials

- *C2000 ePWM Developer's Guide Application Report*
- Enhanced Pulse Width Modulator (ePWM) Training for C2000 MCUs (Video)
- *Flexible PWMs Enable Multi-Axis Drives, Multi-Level Inverters Application Report*
- Getting Started with the C2000 ePWM Module (Video)
- *Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Control Application Report*
  - Chapters 1 to 6 are Fundamental material, derivations, and explanations that are useful for learning about how PWM can be used to implement a DAC. Subsequent chapters are Getting Started and Expert material for implementing in a system.
- *Using the Enhanced Pulse Width Modulator (ePWM) Module Application Report*

Expert Materials

- *CRM/ZVS PFC Implementation Based on C2000 Type-4 PWM Module Application Report*
- *Leverage New Type ePWM Features for Multiple Phase Control Application Report*

Note

The AM13E232x ePWM module is the same peripheral as the C2000 Type 4 ePWM module. While many of the above application reports refer to the C2000™ Family MCUs, many of the ePWM peripheral level configuration concepts can be applied to the AM13E232x ePWM.

26.1.2 MCPWM Overview

Each MCPWM module consists of up to 3 PWM channel pairs (6 channels in total) with the following signal names:

- MCPWMx_1A
- MCPWMx_1B
- MCPWMx_2A
- MCPWMx_2B
- MCPWMx_3A
- MCPWMx_3B

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Note that not all channels must be used within an MCPWM module. You can configure the IOMUX to avoid routing unused channels to the device pins.

Features

Each MCPWM module supports the following features:

- Dedicated 16-bit counter with period and frequency control.
- Up to six PWM outputs (three channel pairs).
  - Each channel pair can be used in the following configurations:
    - Two independent PWM outputs with single-edge operation.
    - Two independent PWM outputs with dual-edge symmetric operation.
    - One independent PWM output with dual-edge asymmetric operation.
- Connected to other MCPWM modules as well as the enhanced capture peripheral (eCAP) by a clock synchronization scheme.
- Asynchronous override control of PWM signals through software.
- Programmable phase-control support for lead or log operation relative to other MCPWM modules.
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising edge and falling edge delay control.
- Programmable trip zone with cycle-by-cycle and one-shot trips for fault conditions.
  - Configurable trip states to force high, low, or high-impedance state at PWM outputs.
- Events triggering CPU interrupts and ADC start of conversions (SOCs).
- Programmable event prescaling to minimize CPU overhead on interrupts.

MCPWM Signals

Each MCPWM module consists of six submodules and is connected within a system as shown in Figure 26-1.

Figure 26-1. Submodules and Signal Connections for an MCPWM Module

Figure 26-2 shows more internal details of a single MCPWM module. The relevant signals used by the MCPWM module are:

- **MCPWMx_yA and MCPWMx_yB**
  - The MCPWM output signals.
- **$\overline{\text{TZ1}}$ to $\overline{\text{TZ8}}$**
  - Trip-Zone input signals used to monitor fault conditions external to the MCPWM module.
  - Each submodule can be configured to use or ignore any of the Trip-Zone signals.
  - Each TZx signal is directly connected to the output of one of the eight PWM XBAR outputs.
- **MCPWMxSYNCI**
  - Time-Base synchronization input signal.
- **MCPWMxSYNCO**
  - Time-Base synchronization output signal.
- **MCPWMxSYNCPER**
  - Time-Base synchronization peripheral signal which can be configured to go to the CMPSS for synchronization purposes. For more information on how MCPWMxSYNCPER is used by the CMPSS, see the *Comparator Subsystem (CMPSS)* chapter.
- **MCPWMx_INT**
  - MCPWM output signal to trigger CPU interrupts.
- **SOCA to SOCD:**
  - Signals sent from MCPWM to ADC to trigger a start-of-conversion (SOC).
  - Each MCPWM module has four ADC start of conversion signals (SOCA, SOCB, SOCC, SOCD).
  - The condition used to trigger the ADC SOC can be configured in the Event-Trigger submodule.
- **Peripheral Bus:**
  - The peripheral bus is 32-bits wide and allows both 16-bit and 32-bit writes to the MCPWM register file.

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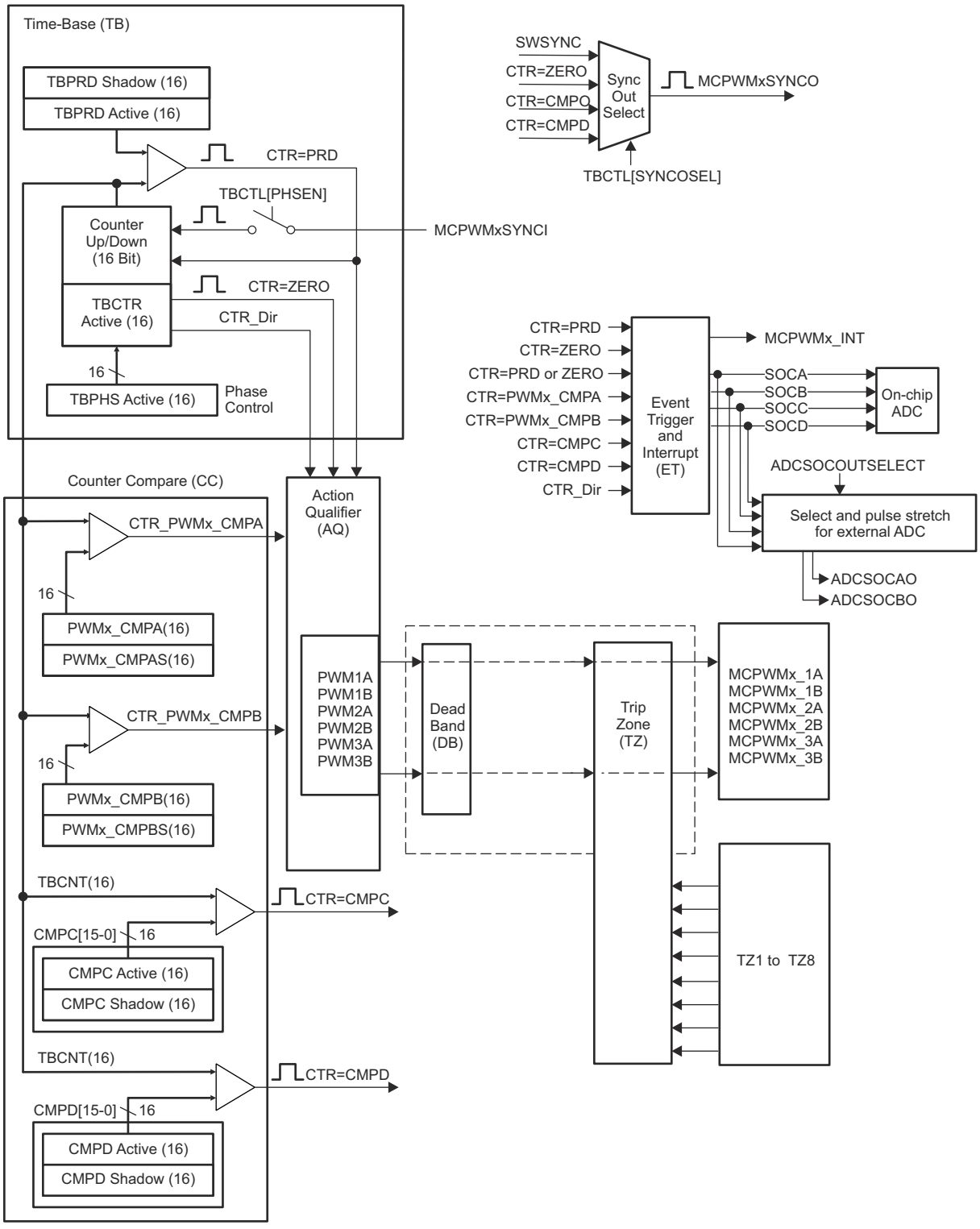


Figure 26-2. MCPWM Modules and Critical Internal Signal Interconnects

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26.2 Configuring Device Pins

26.3 MCPWM Modules Overview

The six MCPWM submodules each perform specific tasks that can be configured through software. The table below summarizes the key parameters that can be configured by each submodule.

Table 26-1. Submodule Configuration Parameters

Submodule	Configurable Parameters
Time Base (TB)	• Time-Base clock (TBCLK), scaled relative to the MCPWM clock (MCPWMCLK). • PWM Time-Base counter (TBCTR) frequency and period. • Count mode for the Time-Base counter: – Up-count mode, used for an asymmetric PWM. – Up-and-down count mode, used for a symmetric PWM. • Time-Base phase, relative to another MCPWM module. • Synchronization between module Time-Base counters through hardware or software. • Count direction (up or down) of the Time-Base counter after a synchronization event. • Time-Base counter behavior when the device is halted by an emulator. • Source for the synchronization output of the MCPWM module. • One-shot and global load of registers in this module.
Counter Compare (CC)	• PWM duty cycle for MCPWMx_yA and MCPWMx_yB outputs. • The time at which switching events occur on MCPWMx_yA and MCPWMx_yB outputs. • Delay for interrupt and SOC generation with additional comparators. • One-shot and global load of registers in this module.
Action Qualifier (AQ)	• Action taken when a Time-Base Counter-Compare event occurs: – No action taken – MCPWMx_yA and MCPWMx_yB high – MCPWMx_yA and MCPWMx_yB low – MCPWMx_yA and MCPWMx_yB toggled • State that the PWM output is forced to through software control. • PWM dead band through software. • One-shot and global load of registers in this module.
Dead-Band Generator (DB)	• Dead-Band relationship between upper and lower switches. • PWM rising-edge delay value. • PWM falling-edge delay value. • MCPWMxB phase shifting with respect to the MCPWMxA. • One shot and global load of registers in this module.
Trip Zone (TZ)	• Trip-Zone input sources and Digital Compare Event input sources. • PWM trip state when a fault occurs: – Force high – Force low – Force to a high-impedance state – Ignore any trip condition. • How often the MCPWM reacts to and clears each Trip-Zone signal: – One-shot (OST) – Cycle-by-cycle (CBC)
Event Trigger (ET)	• Events that trigger an interrupt. • Events that trigger an ADC start-of-conversion (SOC) event. • Rate at which events cause triggers (every occurrence or every 2nd or up to 15th occurrence). • Poll, set, or clear event flags.

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26.4 Time-Base (TB) Submodule

Each MCPWM module has a Time-Base submodule that determines the event timing for the MCPWM module. Built-in synchronization logic allows the Time-Base of multiple MCPWM modules to work as a single system.

Figure 26-3 illustrates the Time-Base submodule within the MCPWM.

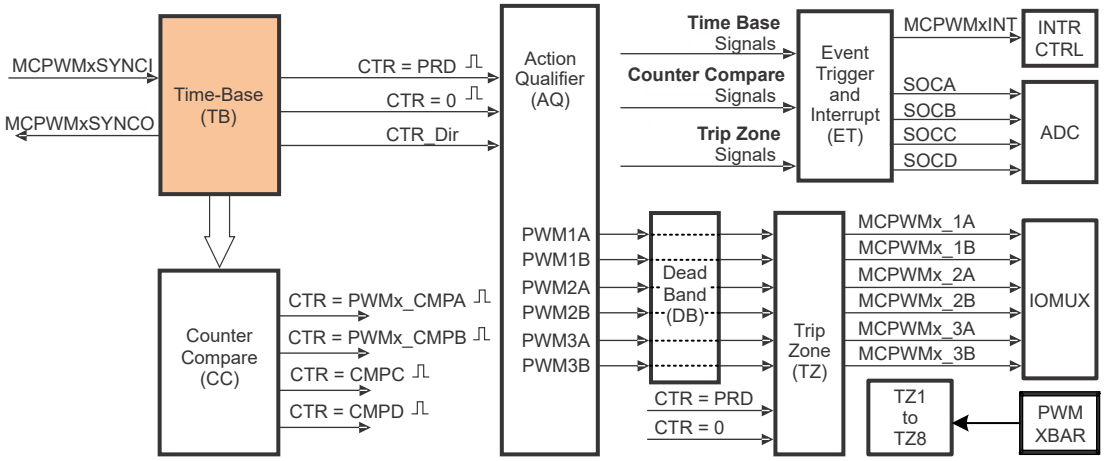


Figure 26-3. Time-Base Submodule

26.4.1 Purpose of the Time-Base Submodule

The Time-Base submodule can be configured to do the following:

- Configure the rate of the MCPWM clock through prescalers.
- Specify the Time-Base counter (TBCTR) period to control the frequency of events.
- Manage Time-Base synchronization with other MCPWM modules.
- Set the Time-Base counter to up-count mode or up-down count mode.
- Generate the following events:
  - CTR = PRD: Time-Base counter equal to the specified period (TBCTR = TBPRD).
  - CTR = Zero: Time-Base counter equal to zero (TBCTR = 0).

If the application requires updating the TBCTR value through software while the TBCTR is counting, note that the module needs at least 1 TBCLK cycle for Time-Base events to occur. The TBCTR can be written with TBCTR = PRD-1 instead of TBCTR = PRD (when counting up) and can be written as TBCTR = 1 instead of TBCTR = 0 (when counting down) for Time-Base event occurrence.

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26.4.2 Controlling and Monitoring the Time-Base Submodule

The block diagram in Figure 26-4 shows the critical signals and registers of the Time-Base submodule. Table 26-2 provides descriptions of the key signals associated with the Time-Base submodule.

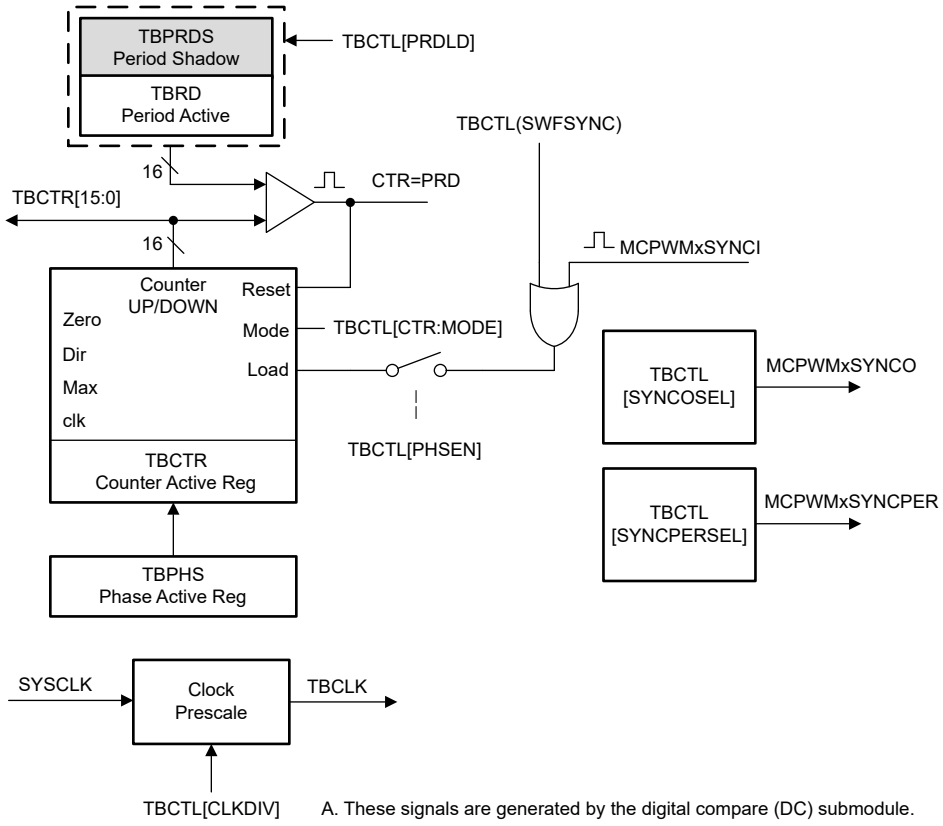


Figure 26-4. Time-Base Submodule Signals and Registers

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Table 26-2. Key Time-Base Signals

Signal	Description
MCPWMxSYNCI	Time-Base synchronization input. Input pulse used to synchronize the Time-Base counter with the counter of other MCPWM modules. For information on the synchronization order of a particular device, see Section 26.4.3.3 .
MCPWMxSYNCO	Time-Base synchronization output. This output pulse is used to synchronize the counter of other MCPWM modules. Using the TBCTL.SYNCOSEL bit, the source of the output pulse is selected.
MCPWMxSYNCPER	Time-Base peripheral synchronization output. This output signal is used to synchronize the CMPSS to the MCPWM. The output signal can be configured using the TBCTL register.
CTR = PRD	Time-Base counter equal to the specified period. This signal is generated whenever the counter value is equal to the active period register value. That is when TBCTR = TBPRD.
CTR = Zero	Time-Base counter equal to zero. This signal is generated whenever the counter value is zero. That is when TBCTR equals 0x00.
CTR = PWMx_CMPB	Time-Base counter equal to active counter-compare B register (TBCTR = PWMx_CMPB). This event is generated by the Counter-Compare submodule and used by the synchronization out logic. There is one CMPB register per PWM channel pair, denoted by "x".
CTRDIR	Time-Base counter direction. Indicates the current direction of the MCPWM Time-Base counter. The signal is high when the counter is increasing and the signal is low when the counter is decreasing. The state of this signal can be observed in the TBSTS register.
TBCLK	Time-Base clock. This is a prescaled version of the MCPWM clock (MCPWMCLK) and is used by all submodules within the MCPWM. This clock determines the rate at which time-base counter increments or decrements.

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26.4.3 Calculating PWM Period and Frequency

The frequency of PWM events is controlled by the Time-Base period (TBPRD) register and the mode of the Time-Base counter. Figure 26-5 shows the period (T_{pwm}) and frequency (F_{pwm}) relationships for the up-count and up-down-count count modes when the period is set to 4 (TBPRD = 4). The time increment for each step is defined by the Time-Base clock (TBCLK) which is a prescaled version of the MCPWM clock (MCPWMCLK).

The Time-Base counter has two modes of operation selected by the Time-base control register (TBCTL.CTRMODE):

- **Up-Count Mode:**
  - In up-count mode, the Time-Base counter starts from zero and increments until the counter reaches the value in the period register (TBPRD). When the period value is reached, the Time-Base counter resets to zero and begins to increment once again.

  Up-Down Count Mode:
  - In up-down count mode, the Time-Base counter starts from zero and increments until the period (TBPRD) value is reached. When the period value is reached, the Time-Base counter then decrements until the counter reaches zero. At this point, the counter repeats the pattern and begins to increment.

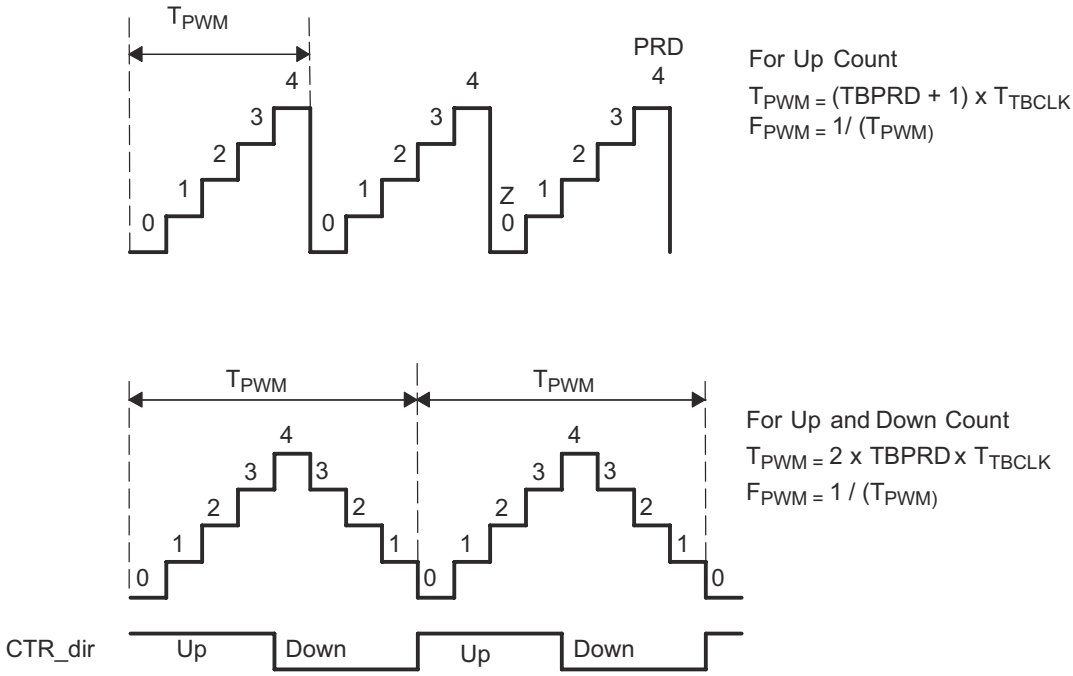


Figure 26-5. Time-Base Frequency and Period

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26.4.3.1 Time-Base Period Shadow Register

The Time-Base period register (TBPRD) has a shadow register as well. Note that two separate addresses are used for the MCPWM active and shadow registers. Shadowing allows register updates to be synchronized with the hardware. The following definitions are used to describe all shadow registers in the MCPWM module:

- **Active Register:** The active register controls the hardware and is responsible for actions that the hardware causes or invokes.
- **Shadow Register:** The shadow register buffers provide a temporary holding location for the active register and have no direct effect on any control hardware. At a strategic point in time, the shadow register content is transferred to the active register. This prevents corruption or spurious operation due to the register being asynchronously modified by software.

Time-Base Period Shadow Mode

TBPRD shadow mode (TBPRDS) is selected when TBCTL[PRDLD] = 0. When shadow mode is selected, users write to the shadow register instead of the active register for shadow loading to occur. The value written to the shadow register is loaded to the active register on the next shadow load event or global load event (if global load is being used).

If shadow mode is selected, the Time-Base period shadow register contents are transferred to the active register (TBPRDS → TBPRD) when the time-base counter equals zero (TBCTR = 0x00). The PRDLDSYNC bit is valid only if TBCTL[PRDLD] = 0. A write to the active register (TBPRD) immediately updates TBPRD.

Time-Base Period Global Load

- The global load control mechanism can also be used with the Time-Base period register by configuring the appropriate bits in the global load configuration register (GLDCTL.GLD). When global load mode is selected, the transfer of contents from shadow register to active register (for all registers that have a corresponding shadow register) occurs on the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL.GLDMODE).

Time-Base Period Immediate Load Mode

TBPRD immediate load mode is selected when TBCTL[PRDLD] = 1. When immediate load mode is selected, a read from or a write to the TBPRD memory address goes directly to the active register. A write to the shadow register does not update the active register.

26.4.3.2 Time-Base Clock Synchronization

The TBCLKSYNC bit in the peripheral clock enable registers allows users to globally synchronize all enabled MCPWM module clocks. When set, all enabled MCPWM module clocks are started with the first rising edge of TBCLK aligned. To have fully synchronized clocks, the prescalers for each MCPWM module must be set identically.

The proper procedure for enabling MCPWM clocks is as follows:

1. Enable MCPWM module clocks
2. Set TBCLKSYNC = 0
3. Configure MCPWM modules
4. Set TBCLKSYNC = 1

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26.4.3.3 Time-Base Counter Synchronization

The MCPWM synchronization scheme allows for increased flexibility in synchronization of the MCPWM modules. Each MCPWM module has a synchronization input (MCPWMxSYNCI), a synchronization output (MCPWMxSYNCO) and a peripheral synchronization output (MCPWMxSYNCPER). Refer to Section 26.4.3.4 for a list of all sync inputs including INPUTXBAR5 and INPUTXBAR6. The TBCTL.SYNCOSEL bit shows the sources that can be used for SYNCO.

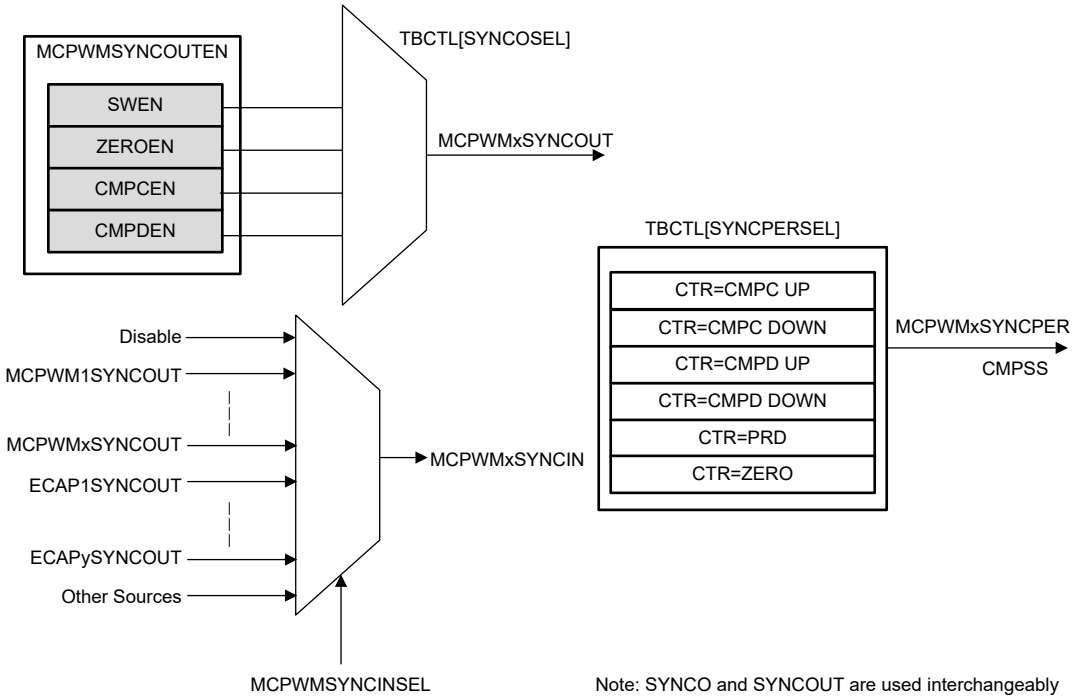


Figure 26-6. Time-Base Counter Synchronization Scheme

Figure 26-7. MCPWM External SYNC Output

Note

See the datasheet for the number of MCPWM and eCAP modules available on your specific device.

Each MCPWM module can be configured to use or ignore the synchronization input. If the TBCTL[PHSEN] bit is set, then the Time-Base counter (TBCTR) of the MCPWM module is automatically loaded with the phase register (TBPHS) contents when one of the following conditions occur:

- **Synchronization Input Pulse**
  - The value of the phase register is loaded into the counter register (TBPHS → TBCTR) when an input synchronization pulse is detected via MCPWMxSYNCI. This operation occurs on the next valid Time-Base clock (TBCLK) edge.
  - There is delay from internal control module to target modules:
    - If TBCLK = MCPWMCLK, the delay is 2 MCPWMCLK periods
    - If TBCLK < MCPWMCLK, the delay is 1 TBCLK period
- **Software-Forced Synchronization Pulse**
  - Writing a 1 to the TBCTL[SWFSYNC] control bit triggers a software forced synchronization. This pulse is ORed with the synchronization input signal, and therefore has the same effect as a pulse on MCPWMxSYNCI.

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Note

The MCPWMxSYNCI is rising edge activated. If the MCPWMxSYNCI signal is held high, the sync does not continuously occur.

When modifying the TBPHS register during run-time, missed action qualifier events can occur due to sudden jumps in the TBCTR value at the time of the SYNCIN pulse. To recreate the behavior of missed action qualifier events, a CMPB event can be needed if CMPB is not already utilized.

This feature enables the MCPWM module to be automatically synchronized to the Time-Base of another MCPWM module. Lead or lag phase control can be added to the waveforms generated by different MCPWM modules to synchronize them. In up-down-count mode, the TBCTL[PHSDIR] bit configures the direction of the Time-Base counter immediately after a synchronization event. The new direction is independent of the direction prior to the synchronization event. The PHSDIR bit is ignored in count-up or count-down modes (see Section 26.4.5 for examples).

Clearing the TBCTL[PHSEN] bit configures the MCPWM to ignore the synchronization input pulse.

26.4.3.4 MCPWM Sync Selection

The below table specifies the sources for the MCPWM Sync options in the TBCTL.SYNCISEL register field.

Table 26-3. PWM and eCAP SYNC Selection

PWM*.SYNCINSEL ECAP*.SYNCINSEL	Input Signal
0	Disable
1	Reserved
2	Reserved
3	ECAP0_SYNCOUT
4	ECAP1_SYNCOUT
5	MCPWM0_SYNCOUT
6	MCPWM1_SYNCOUT
7	MCPWM2_SYNCOUT
8	Reserved
9	Reserved
10	ECAP2_SYNCOUT
11	EPWM0_SYNCOUT
12	EPWM1_SYNCOUT
13	EPWM2_SYNCOUT
14	EPWM3_SYNCOUT
15	EPWM4_SYNCOUT
16	EPWM5_SYNCOUT
17	ECAT_SYNC0
18	ECAT_SYNC1
19	FSIRX_TRIG1
20	INPUTXBAROUT5
21	INPUTXBAROUT6
22-31	Reserved

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26.4.4 Phase Locking the Time-Base Clocks of Multiple MCPWM Modules

The TBCLKSYNC bit can be used to globally synchronize the time-base clocks of all enabled MCPWM modules on a device. This bit is part of the device's clock enable registers and is described in the *System Control and Interrupts* chapter. When TBCLKSYNC = 0, the time-base clock of all MCPWM modules is stopped (default). When TBCLKSYNC = 1, all MCPWM time-base clocks are started with the rising edge of TBCLK aligned. For synchronized TBCLKs, the prescaler bits in the TBCTL register of each MCPWM module must be set identically. The proper procedure for enabling the MCPWM clocks is:

1. Enable the individual MCPWM module clocks.
2. Set TBCLKSYNC = 0. This stops the time-base clock within any enabled MCPWM module.
3. Configure the prescaler values and desired MCPWM modes.
4. Set TBCLKSYNC = 1.

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26.4.5 Time-Base Counter Modes and Timing Waveforms

The time-base counter operates in one of three modes:

- Up-count mode that is asymmetrical
- Up-down-count that is symmetrical
- Frozen where the time-base counter is held constant at the current value

To illustrate the operation of the first three modes, the following timing diagrams show when events are generated and how the time-base responds to an MCPWMxSYNCI signal.

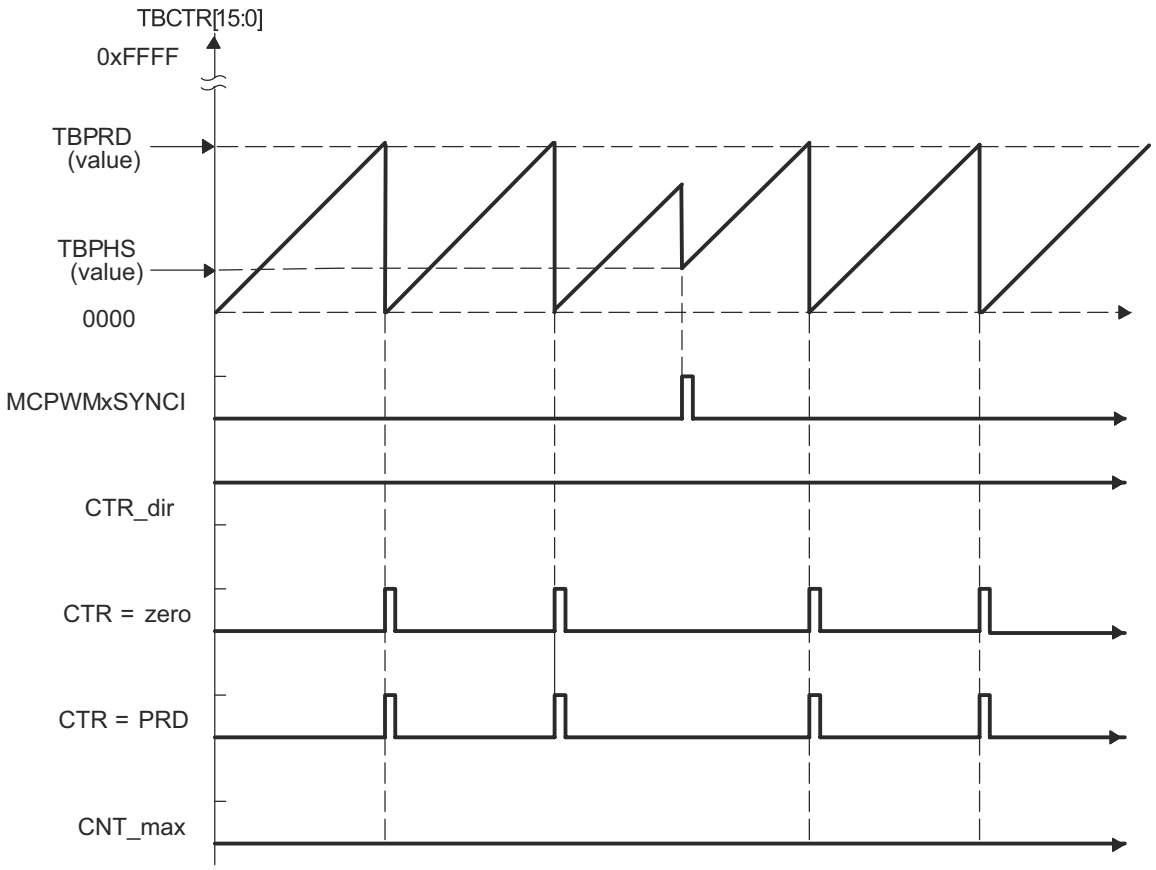


Figure 26-8. Time-Base Up-Count Mode Waveforms

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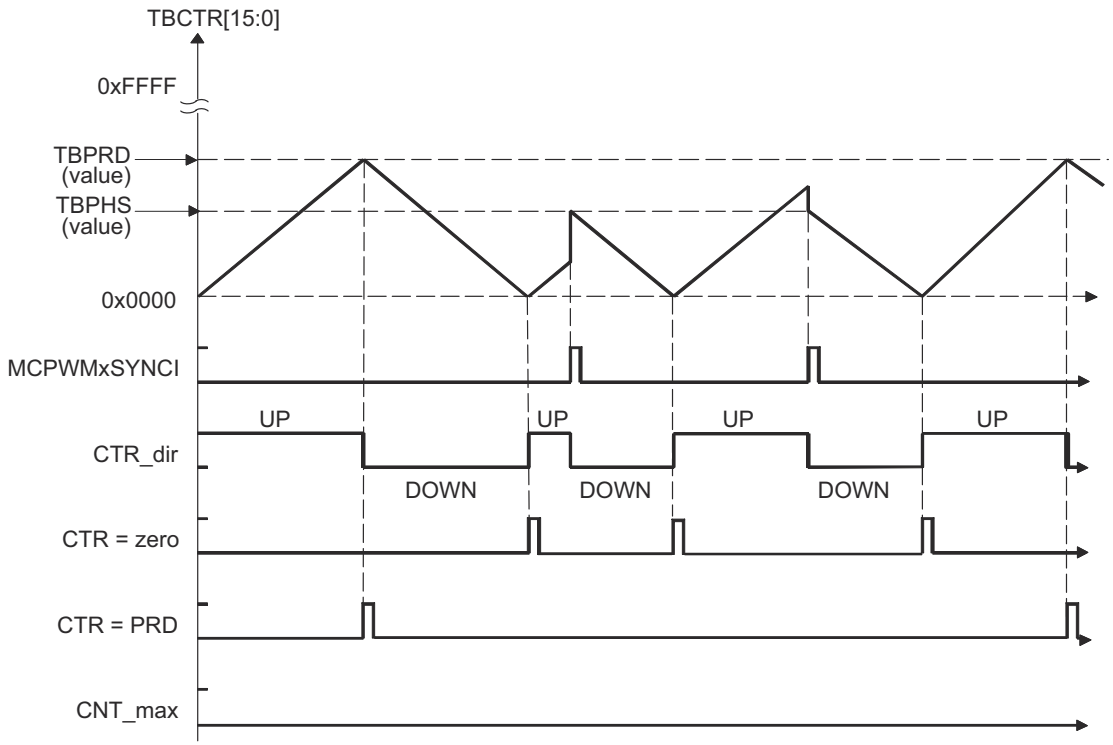


Figure 26-9. Time-Base Up-Down Count Waveforms, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

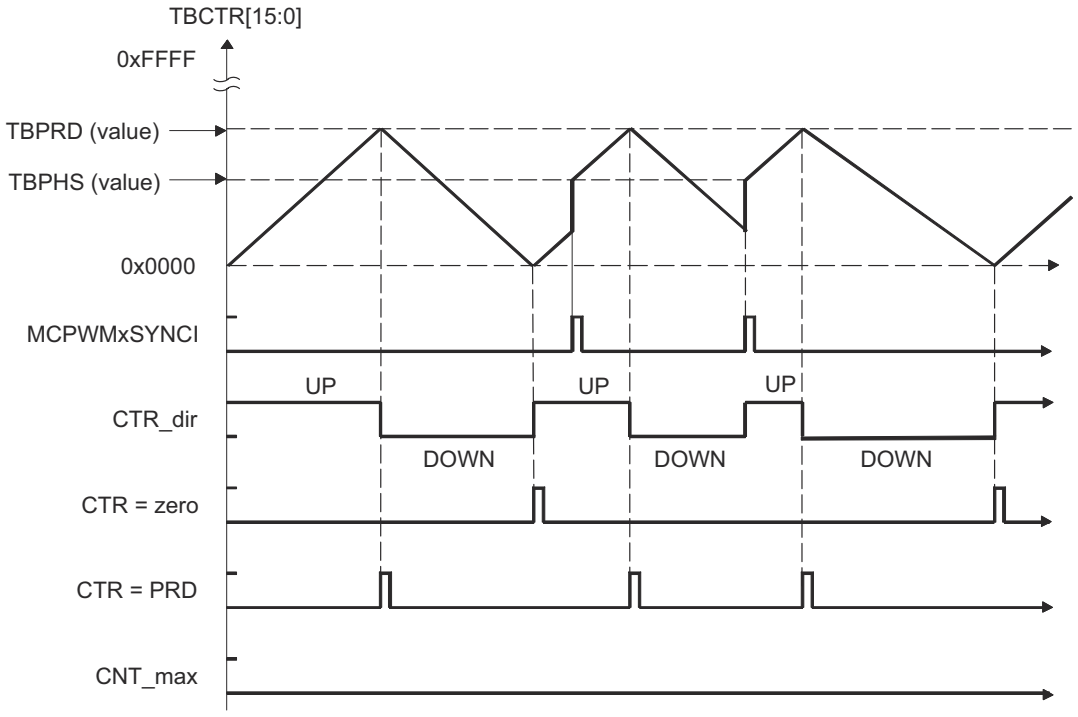


Figure 26-10. Time-Base Up-Down Count Waveforms, TBCTL[PHSDIR = 1] Count Up On Synchronization Event

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26.4.6 Global Load

Figure 26-11 shows the signals and registers associated with the global load feature.

When this feature is enabled, the transfer of contents from the shadow register to the active register, for all registers that have a shadow register, occurs at the same event as defined by the configuration bits in Global Shadow to Active Load Control Register (GLDCTL[GLDMODE]). When GLDCTL[GLD] = 1, shadow to active load event selection bits for individual shadowed registers are ignored and global load mode takes effect for all registers with a corresponding shadow register.

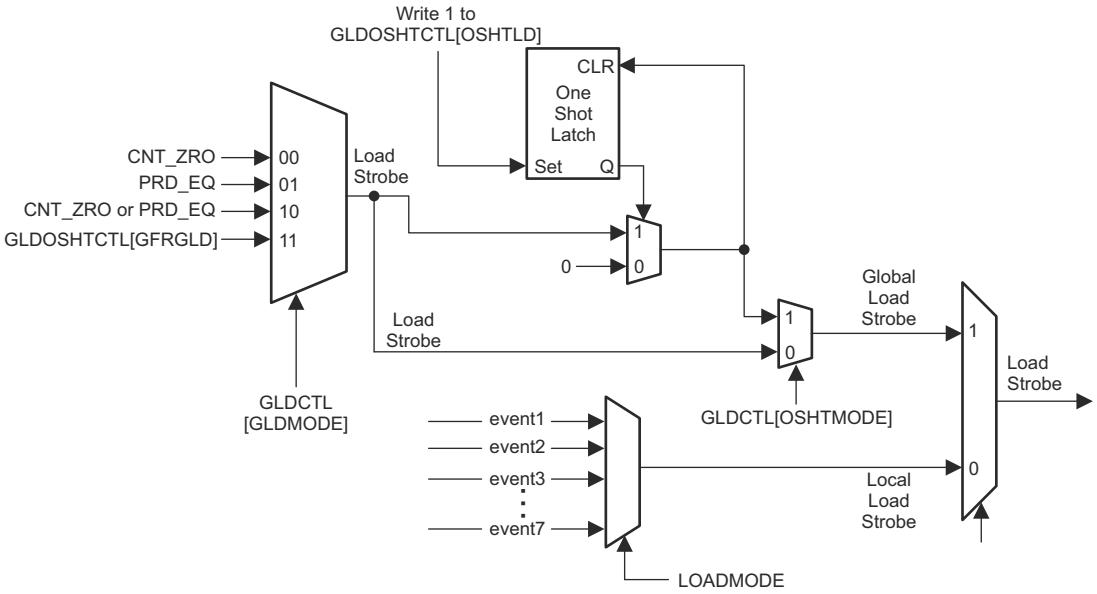


Figure 26-11. Global Load: Signals and Registers

26.4.6.1 One-Shot Load Mode

This feature causes the shadow-register to active-register transfers to occur once. When GLDOSHTCTL[OSHTLD] = 1 and one shot global load is enabled using GLDCTL[OSHTMODE], the shadow-register to active-register transfer takes place on the event selected by GLDCTL[GLDMODE]. Software force loading of contents from the shadow register to an active register is possible by using GLDOSHTCTL[GFRCLD].

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26.5 Counter-Compare (CC) Submodule

Figure 26-12 illustrates the counter-compare submodule within the MCPWM.

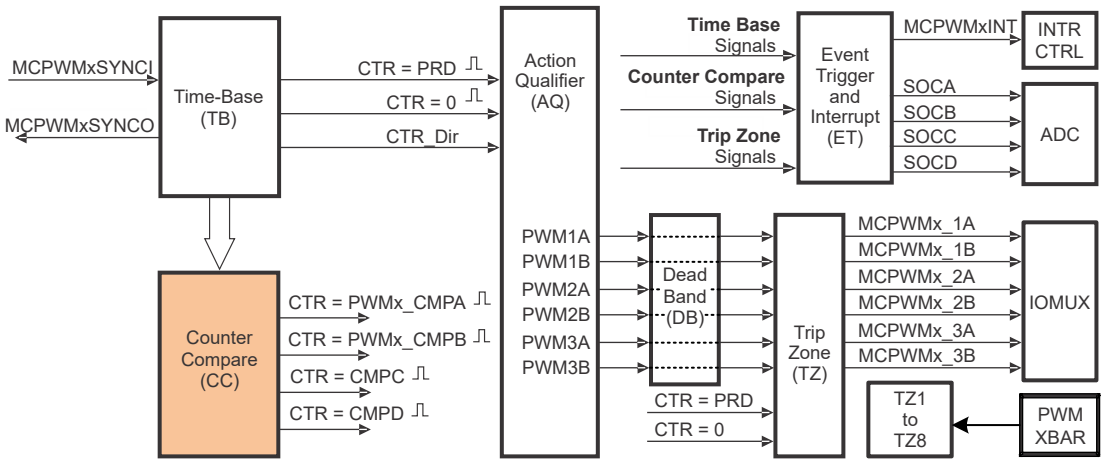


Figure 26-12. Counter-Compare Submodule

26.5.1 Purpose of the Counter-Compare Submodule

The counter-compare submodule takes as input the time-base counter value. This value is continuously compared to the counter-compare A (PWMx_CMPA), counter-compare B (PWMx_CMPB), counter-compare C (CMPC), and counter-compare D (CMPD) registers. When the time-base counter is equal to one of the compare registers, the counter-compare unit generates an appropriate event. Note that each MCPWM module can have up to three PWM pairs, denoted by "PWMx". There is a CMPA and CMPB register for each pair, but only one CMPC and CMPD register for the entire MCPWM module.

The counter-compare:

- Generates events based on programmable time stamps using the CMPA, CMPB, CMPC, and CMPD registers:
  - CTR = PWMx_CMPA: Time-base counter equals counter-compare A register for PWMx (TBCTR = PWMx_CMPA)
  - CTR = PWMx_CMPB: Time-base counter equals counter-compare B register (TBCTR = PWMx_CMPB)
  - CTR = PWMx_CMPC: Time-base counter equals counter-compare C register (TBCTR = CMPC)
  - CTR = PWMx_CMPD: Time-base counter equals counter-compare D register (TBCTR = CMPD)
- Controls the PWM duty cycle, if the action-qualifier submodule is configured appropriately using counter-compare A (PWMx_CMPA) and counter-compare B (PWMx_CMPB)
- Shadows new compare values to prevent corruption or glitches during the active PWM cycle

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26.5.2 Controlling and Monitoring the Counter-Compare Submodule

The counter-compare submodule operation is shown in Figure 26-13.

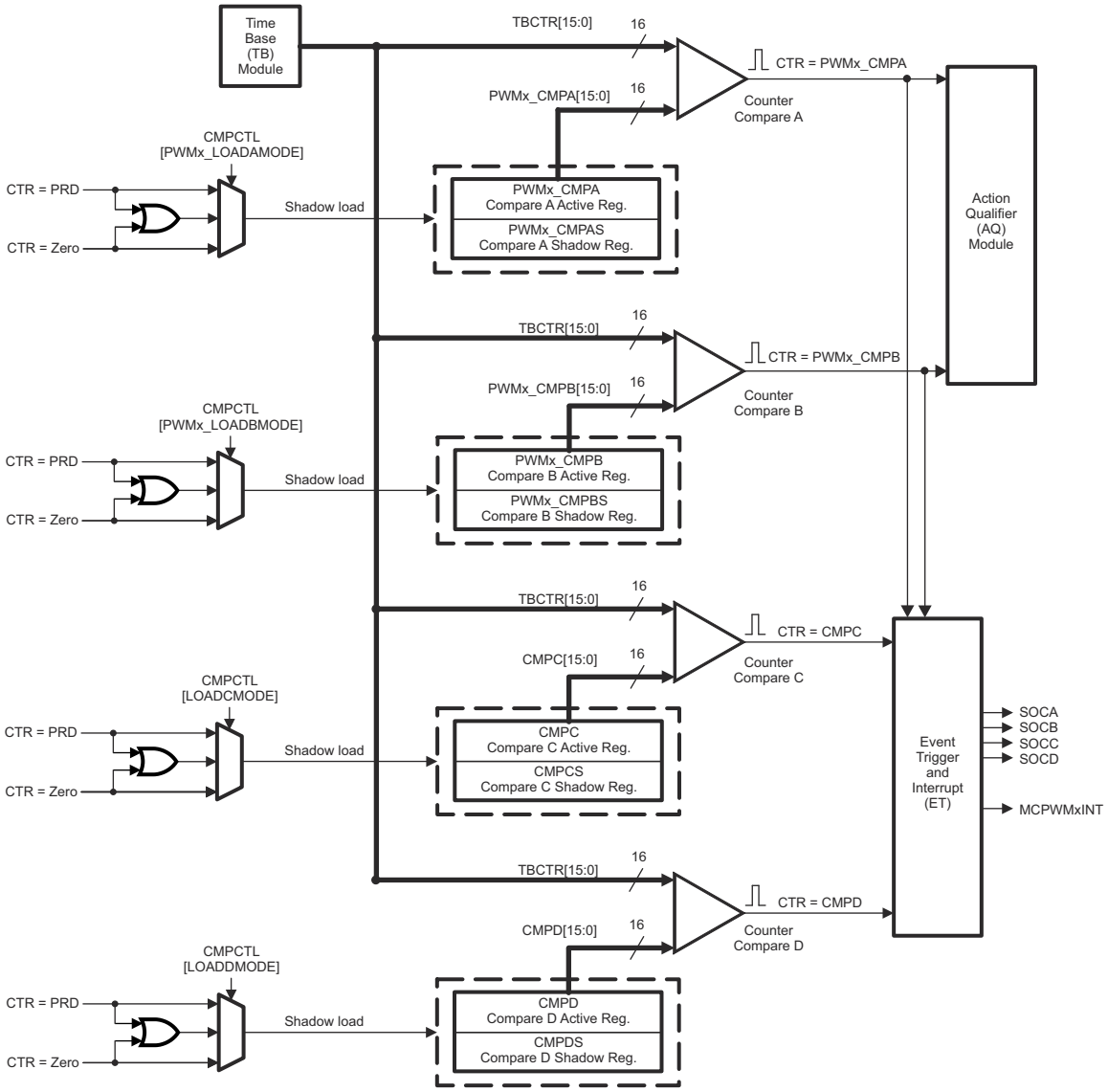


Figure 26-13. Detailed View of the Counter-Compare Submodule

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26.5.3 Operational Highlights for the Counter-Compare Submodule

The counter-compare submodule is responsible for generating events that can be used in the action-qualifier and event-trigger submodules:

1. CTR = PWMx_CMPA: Time-base counter equal to counter-compare A register (TBCTR = PWMx_CMPA).
2. CTR = PWMx_CMPB: Time-base counter equal to counter-compare B register (TBCTR = PWMx_CMPB).
3. CTR = CMPC: Time-base counter equal to counter-compare C register (TBCTR = CMPC). This event can be used to generate an event in the event trigger submodule only.
4. CTR = CMPD: Time-base counter equal to counter-compare D register (TBCTR = CMPD). This event can be used to generate an event in the event trigger submodule only.

For up-count mode, each event occurs only once per cycle. For up-down count mode, each event occurs twice per cycle if the compare value is between 0x00-TBPRD; and once per cycle if the compare value is equal to 0x00 or equal to TBPRD. These events are applied to the action-qualifier submodule where the events are qualified by the counter direction and converted into actions if enabled. Refer to Section 26.6.1 for more details.

The counter-compare registers PWMx_CMPA and PWMx_CMPB each have an associated shadow register. Shadowing provides a way to keep updates to the registers synchronized with the hardware. When shadowing is used, updates to the active registers only occur at strategic points. This prevents corruption or spurious operation due to the register being asynchronously modified by software. There is a separate memory address for the active and shadow registers. To utilize the shadow loading feature, the CPU writes to the corresponding shadow register instead of the active register. The behavior of the two load modes are described as follows:

Shadow Mode:

The shadow mode for the PWMx_CMPA and PWMx_CMPB is always enabled, however the user must write to the corresponding shadow register(PWMx_CMPAS or PWMx_CMPBS) for shadow loading to occur.

The content of the shadow register is transferred to the active register on one of the following events as specified by the CMPCTL[PWMx_LOADAMODE] and CMPCTL[PWMx_LOADBMODE] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00).
- Both CTR = PRD or CTR = Zero.

Only the active register contents are used by the counter-compare submodule to generate events to be sent to the action-qualifier.

Note

Refer to Section 26.6.5 for valid configurations of CMPA/CMPB and LOADAMODE/LOADBMODE.

Immediate Load Mode:

Immediate load mode occurs when the CPU writes directly to the active register(PWMx_CMPA or PWMx_CMPB).

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Additional Comparators

The counter-compare submodule is responsible for generating two additional independent compare events based on two compare registers, which is fed to Event Trigger submodule:

1. CTR = PWMx_CMPC: Time-base counter equal to counter-compare C register (TBCTR = CMPC).
2. CTR = PWMx_CMPD: Time-base counter equal to counter-compare D register (TBCTR = CMPD).

The counter-compare registers CMPC and CMPD each have an associated shadow register. The memory address of the active register and the shadow register are separate, similar to PWMx_CMPA and PWMx_CMPB. The value in the active CMPC and CMPD register is compared to the time-base counter (TBCTR). When the values are equal, the counter compare module generates an event. The shadow and active mode functionality is identical to the functionality for PWMx_CMPA and PWMx_CMPB described above.

Global Load Support

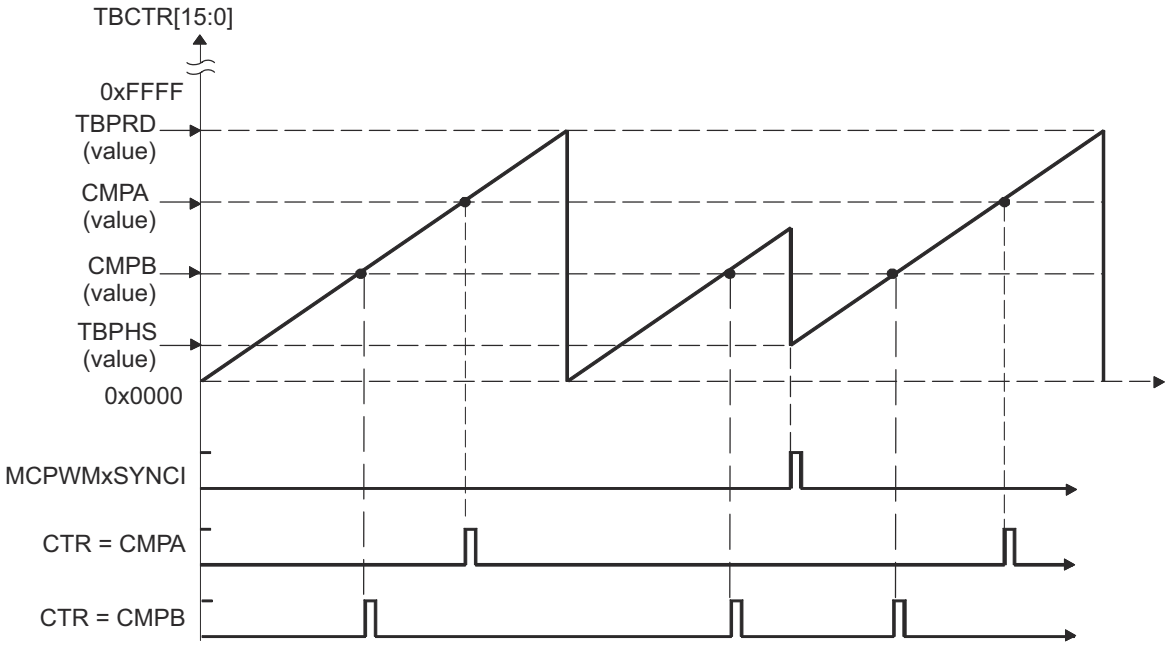
The global load control mechanism can also be used for all counter-compare registers by configuring the appropriate bits in the global load configuration register (GLDCTL). When the global load mode is selected the transfer of contents from shadow register to active register, for all registers that have a corresponding shadow register, occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The global load control mechanism is explained in Section 26.4.6 .

26.5.4 Count Mode Timing Waveforms

The counter-compare module can generate compare events in both count modes:

- Up-count mode: used to generate an asymmetrical PWM waveform.
- Up-down-count mode: used to generate a symmetrical PWM waveform.

To best illustrate the operation of the two count modes, the timing diagrams in Figure 26-14 through Figure 26-16 show when events are generated and how the MCPWMxSYNCI signal interacts.



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Note

An MCPWMxSYNCI external synchronization event can cause a discontinuity in the TBCTR count sequence. This can lead to a compare event being skipped. This skipping is considered normal operation and must be taken into account.

Figure 26-14. Counter-Compare Event Waveforms in Up-Count Mode

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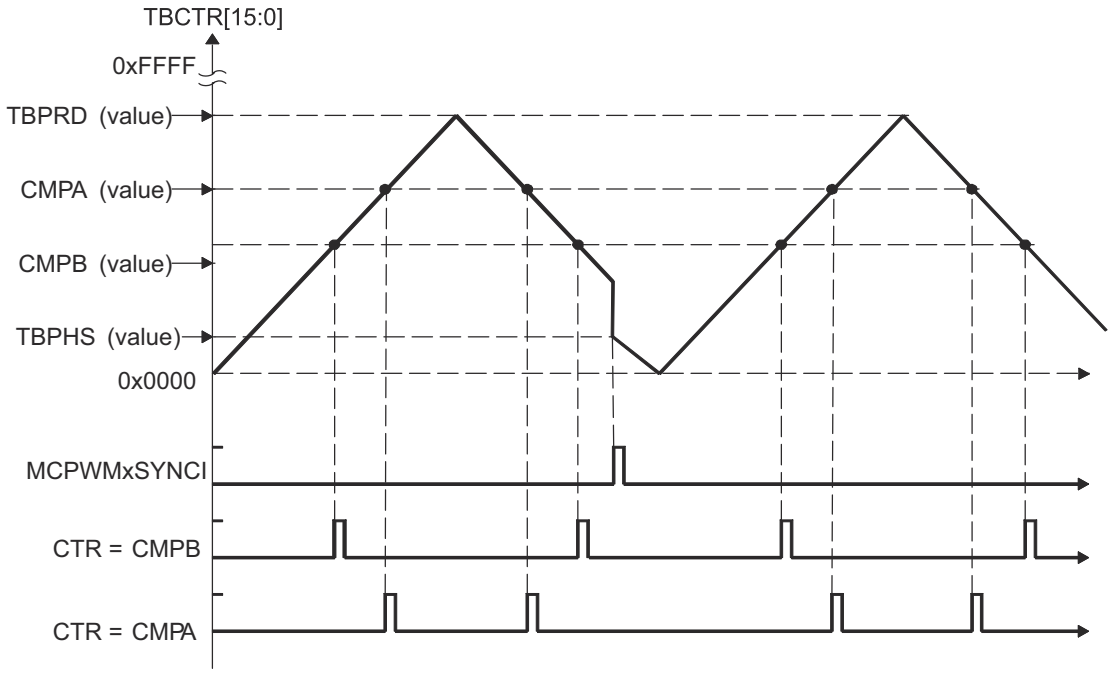


Figure 26-15. Counter-Compare Events In Up-Down Count Mode, TBCTL[PHSDIR = 0] Count Down On Synchronization Event

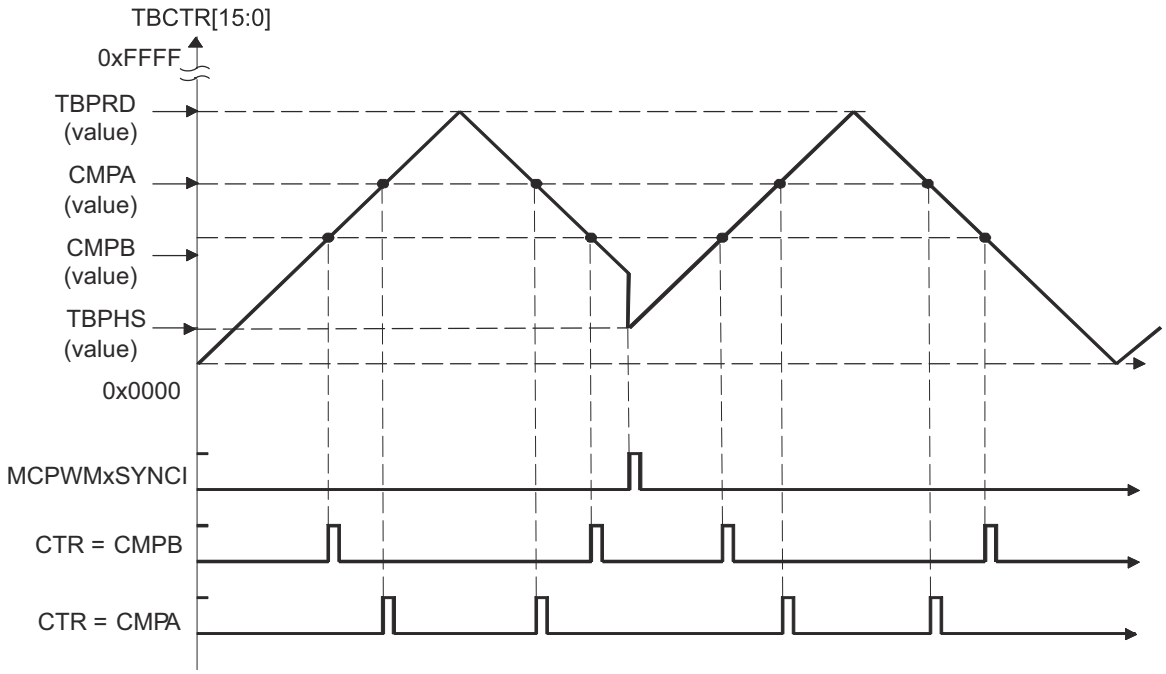


Figure 26-16. Counter-Compare Events In Up-Down Count Mode, TBCTL[PHSDIR = 1] Count Up On Synchronization Event

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26.6 Action-Qualifier (AQ) Submodule

The action-qualifier submodule defines the behavior of MCPWMx_yA and MCPWMx_yB outputs for each MCPWM TBCTR event. This module can trigger a rising or falling edge on the PWM outputs.

Figure 26-17 illustrates the action-qualifier submodule within the MCPWM.

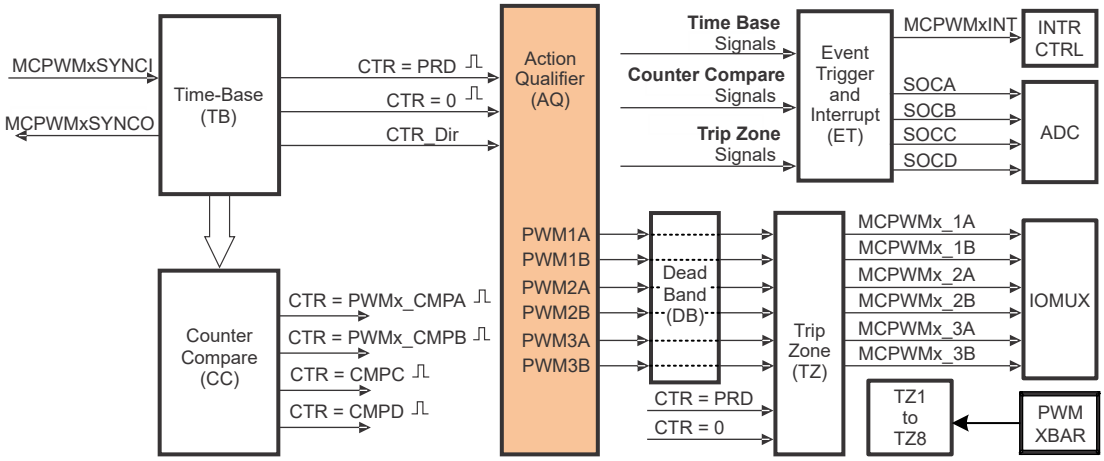


Figure 26-17. Action-Qualifier Submodule

26.6.1 Purpose of the Action-Qualifier Submodule

The action-qualifier submodule is responsible for the following:

- Qualifying and generating actions (set, clear, toggle) based on the following events:
  - CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
  - CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
  - CTR = PWMx_CMPA: Time-base counter equal to the counter-compare A register (TBCTR = PWMx_CMPA)
  - CTR = PWMx_CMPB: Time-base counter equal to the counter-compare B register (TBCTR = PWMx_CMPB)
- Managing priority when these events occur concurrently
- Providing independent control of events when the time-base counter is increasing and when the time-base counter is decreasing

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26.6.2 Action-Qualifier Submodule Control and Status Register Definitions

The action-qualifier submodule operation is shown in Figure 26-18 and monitored by way of the registers in *MCPWM Registers*.

For convenience, the possible input events are summarized again in Table 26-4.

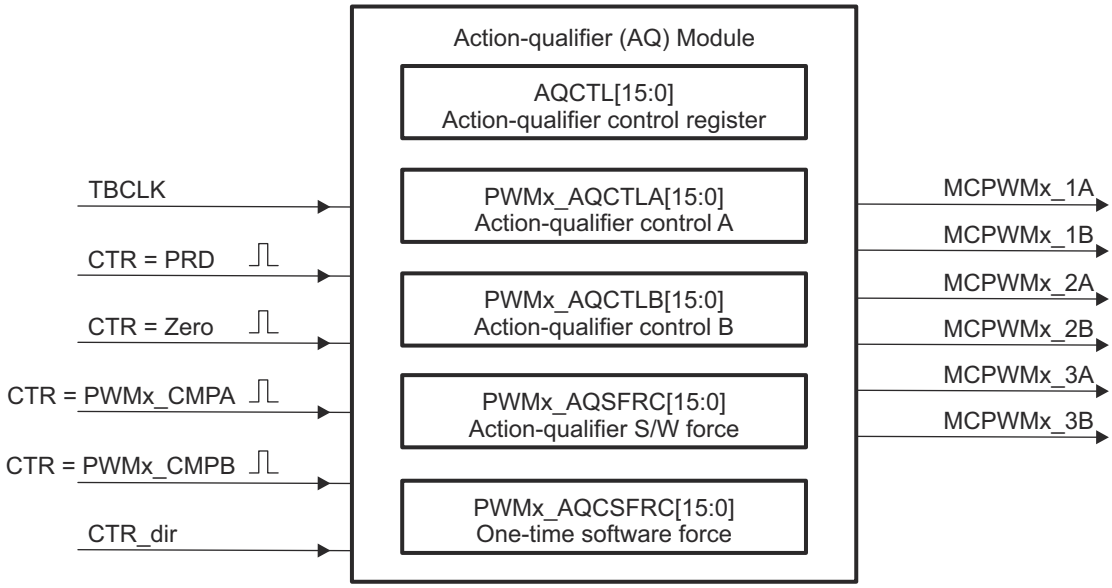


Figure 26-18. Action-Qualifier Submodule Inputs and Outputs

Table 26-4. Action-Qualifier Submodule Possible Input Events

Signal	Description	Registers Compared
CTR = PRD	Time-base counter equal to the period value	TBCTR = TBPRD
CTR = Zero	Time-base counter equal to 0	TBCTR = 0x00
CTR = CMPA	Time-base counter equal to the counter-compare A	TBCTR = PWMx_CMPA
CTR = CMPB	Time-base counter equal to the counter-compare B	TBCTR = PWMx_CMPB
Software forced event	Asynchronous event initiated by software	

The software forced action is a useful asynchronous event. This control is handled by the PWMx_AQSFRC and PWMx_AQOTSFRC register.

The action-qualifier submodule controls how the outputs MCPWMx_yA and MCPWMx_yB behave when a particular event occurs. The event inputs to the action-qualifier submodule are further qualified by the counter direction (up or down). This allows for independent action on outputs on both the count-up and count-down phases.

The possible actions imposed on outputs MCPWMx_yA and MCPWMx_yB are:

- **Set High:** Set output MCPWMx_yA or MCPWMx_yB to a high level.
- **Clear Low:** Set output MCPWMx_yA or MCPWMx_yB to a low level.
- **Toggle:** If MCPWMx_yA or MCPWMx_yB is currently pulled high, then pull the output low. If MCPWMx_yA or MCPWMx_yB is currently pulled low, then pull the output high.
- **Do Nothing:** Keep outputs MCPWMx_yA and MCPWMx_yB at same level as currently set. Although the "Do Nothing" option prevents an event from causing an action on the MCPWMx_yA and MCPWMx_yB outputs, this event can still trigger interrupts and ADC start of conversion. See the description in Section 26.9 for details.

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Actions are specified independently for either output (MCPWMx_yA or MCPWMx_yB). Any or all events can be configured to generate actions on a given output. For example, both CTR = PWMx_CMPA and CTR = PWMx_CMPB can operate on output MCPWMx_yA. For each PWM pair "x", independent action qualifier events are specified. All qualifier actions are configured using the control registers found in *MCPWM Registers*.

For clarity, the illustrations in this chapter use a set of symbolic actions. These symbols are summarized in Figure 26-19. Each symbol represents an action as a marker in time. Some actions are fixed in time (zero and period) while the CMPA and CMPB actions are moveable and the time positions are programmed by way of the counter-compare A and B registers, respectively. To turn off or disable an action, use the "Do Nothing option"(the default at reset).

S/W force	TB Counter equals				Actions
	Zero	Comp A	Comp B	Period	
SW	Z	CA	CB	P	Do Nothing
SW	Z	CA	CB	P	Clear Lo
SW	Z	CA	CB	P	Set Hi
SW	Z	CA	CB	P	Toggle

Figure 26-19. Possible Action-Qualifier Actions for MCPWMx_yA and MCPWMx_yB Outputs

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26.6.3 Action-Qualifier Event Priority

It is possible for the MCPWM action qualifier to receive more than one event at the same time. In this case, events are assigned a priority by the hardware. The general rule is events occurring later in time have a higher priority and software forced events always have the highest priority. The event priority levels for up-down count mode are shown in Table 26-5. A priority level of 1 is the highest priority and level 10 is the lowest. The priority changes slightly depending on the direction of TBCTR.

Table 26-5. Action-Qualifier Event Priority for Up-Down Count Mode

Priority Level	Event If TBCTR is Incrementing TBCTR = Zero up to TBCTR = TBPRD	Event If TBCTR is Decrementing TBCTR = TBPRD down to TBCTR = 1
1 (Highest)	Software forced event	Software forced event
2	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
3	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
4 (Lowest)	Counter equals zero	Counter equals period (TBPRD)

Table 26-6 shows the action-qualifier priority for up-count mode. In this case, the counter direction is always defined as up; therefore, down-count events never are taken.

Table 26-6. Action-Qualifier Event Priority for Up-Count Mode

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	Counter equal to CMPB on up-count (CBU)
4	Counter equal to CMPA on up-count (CAU)
5 (Lowest)	Counter equal to Zero

It is possible to set the compare value greater than the period. In this case, the action takes place as shown in Table 26-7.

Table 26-7. Behavior if CMPA/CMPB is Greater than the Period

Counter Mode	Compare on Up-Count Event CAD/CBD	Compare on Down-Count Event CAD/CBD
Up-Count Mode	If CMPA/CMPB ≤ TBPRD period, then the event occurs on a compare match (TBCTR = CMPA or CMPB). If CMPA/CMPB > TBPRD, then the event does not occur.	Never occurs.
Up-Down Count Mode	If CMPA/CMPB < TBPRD and the counter is incrementing, the event occurs on a compare match (TBCTR = CMPA or CMPB). If CMPA/CMPB is ≥ TBPRD, the event occurs on a period match (TBCTR = TBPRD).	If CMPA/CMPB < TBPRD and the counter is decrementing, the event occurs on a compare match (TBCTR = CMPA or CMPB). If CMPA/CMPB ≥ TBPRD, the event occurs on a period match (TBCTR = TBPRD).

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26.6.4 AQCTLA and AQCTLB Shadow Mode Operations

Shadow Mode:

Shadowing is always enabled for PWMx_AQCTLA and PWMx_AQCTLB. To utilize shadowing, the user must write to the corresponding shadow registers (PWMx_AQCTLAS and PWMx_AQCTLBS).

The content of the shadow register is transferred to the active register on one of the following events as specified by the AQCTL[PWMx_LDAQAMODE] and AQCTL[PWMx_LDAQBMODE] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

Global Load Support

Global load control mechanism can also be used for PWMx_AQCTLA and PWMx_AQCTLB registers when global load is enabled via the global load configuration register (GLDCTL). When global load mode is selected, the transfer of contents from the shadow registers to active registers occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The global load control mechanism is explained in Section 26.4.6 .

Immediate Load Mode:

To utilize immediate load mode, global load must be disabled and the user must write to the active register instead of the shadow register. See Figure 26-20 and Figure 26-21.

Note

Shadow to Active Load of Action Qualifier Output A/B Control Register [PWMx_AQCTLA and PWMx_AQCTLB] on CMPA = 0 or CMPB = 0 boundary

If the Counter-Compare A Register (PWMx_CMPA) or Counter-Compare B Register (PWMx_CMPB) is set to a value of 0 and the action qualifier action on PWMx_AQCTLA and PWMx_AQCTLB is configured to occur in the same instant as a shadow to active load (that is, CMPA = 0 and AQCTLA shadow to active load on TBCTR = 0 using AQCTL register LDAQAMODE and LDAQAMODE bits), then both events can enter contention depending on the timing of the write to PWMx_CMPA or PWMx_CMPB, resulting in a missed action qualifier event for one MCPWM period. It is recommended to use a Non-Zero Counter-Compare when using Shadow to Active Load of Action Qualifier Output A/B Control Register on TBCTR = 0 boundary.

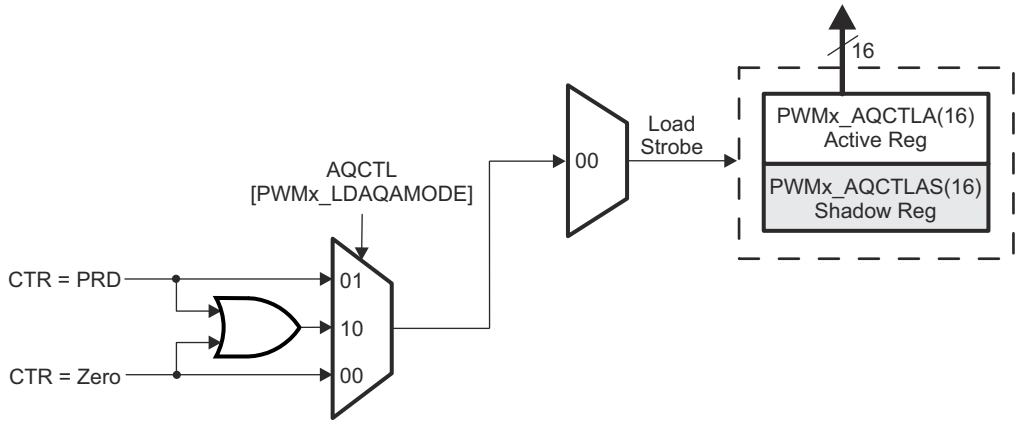


Figure 26-20. AQCTL[PWMx_LDAQAMODE]

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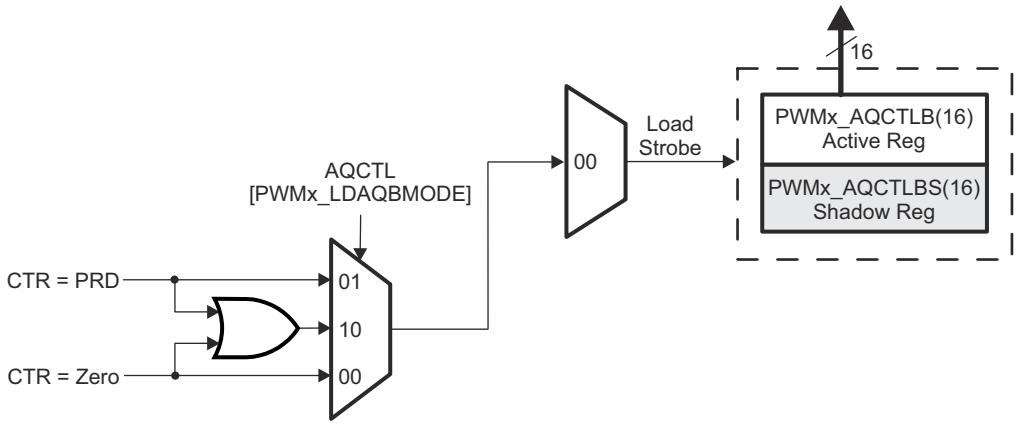


Figure 26-21. AQCTL[PWMx_LDAQBMODE]

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26.6.5 Configuration Requirements for Common Waveforms

Note

The waveforms in this chapter show the behavior of the MCPWMs for a static compare register value. In a running system, the active compare registers (PWMx_CMPA and PWMx_CMPB) are typically updated from the respective shadow registers (PWMx_CMPAS and PWMx_CMPBS) once every period. Specify when the update takes place: either when the time-base counter reaches zero or when the time-base counter reaches the period. There are some cases when the action based on the new value can be delayed by one period or the action based on the old value can take effect for an extra period. Some PWM configurations avoid this situation. These include, but are not limited to, the following:

Use up-down count mode to generate a symmetric PWM:

- If loading PWMx_CMPA/PWMx_CMPB on zero, then use PWMx_CMPA/PWMx_CMPB values greater than or equal to 1.
- If loading PWMx_CMPA/PWMx_CMPB on period, then use PWMx_CMPA/PWMx_CMPB values less than or equal to TBPRD - 1.

  This means there is always a pulse of at least 1 TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

Use up-down count mode to generate an asymmetric PWM:

- To achieve 50%-0% asymmetric PWM, use the following configuration: load PWMx_CMPA/PWMx_CMPB on period and use the period action to clear the PWM and a compare-up action to set the PWM. Modulate the compare value from 0 to TBPRD to achieve 50%-0% PWM duty.

When using up-count mode to generate an asymmetric PWM:

- To achieve 0-100% asymmetric PWM, load PWMx_CMPA/PWMx_CMPB on TBPRD. When PWMx_CMPA/PWMx_CMPB is not loaded on TBCTR = PRD, boundary conditions can occur depending on the timing of the write and the value written to PWMx_CMPA/PWMx_CMPB. Use the Zero action to set the PWM and a compare-up action to clear the PWM. Modulate the compare value from 0 to TBPRD + 1 to achieve 0-100% PWM duty.

When using up-count mode to generate an asymmetric PWM with dead-band enabled:

- To achieve 0%-100% PWM, use the following configuration: When the PWMx_CMPA value is too close to 0 or PRD such that the following conditions are met (CMPX < Deadband) or (CMPX > PRD – Deadband), the actions specified by the AQCTL register for CMPX do not take effect. To avoid this, the AQCTL settings must be altered under these conditions only to generate either high or low pulses for both CAU or CAD events (both set or both clear). Make sure that this software update is occurring synchronous to the PWM carrier cycle, and shadow mode is enabled.

When using up-down count mode to generate an asymmetric PWM with dead-band enabled:

- To achieve 0%-100% PWM, use the following configuration: When the PWMx_CMPA value is too close to 0 or PRD such that the following conditions are met (CMPX < Deadband/2) or (CMPX > PRD – (Deadband)/2), the actions specified by the AQCTL register for CMPX do not take effect. To avoid this, the AQCTL settings must be altered under these conditions only to generate either high or low pulses for both CAU or CAD events (both set or both clear). Make sure that this software update is occurring synchronous to the PWM carrier cycle, and shadow mode is enabled.

See *Using Enhanced Pulse Width Modulator (ePWM) Module for 0-100% Duty Cycle Control*.

Figure 26-22 shows how a symmetric PWM waveform can be generated using the up-down-count mode of the TBCTR. In this mode, 0%-100% DC modulation is achieved by using equal compare matches on the up count and down count portions of the waveform. In the example shown, PWMx_CMPA is used to make the comparison. When the counter is incrementing, the PWMx_CMPA match pulls the PWM output high. Likewise when the counter is decrementing, the compare match pulls the PWM signal low. When PWMx_CMPA = 0, the

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PWM signal is high for the entire period giving a 100% duty waveform. When PWMx_CMPA = TBPRD, the PWM signal is low achieving 0% duty.

When using this configuration in practice, if loading PWMx_CMPA/PWMx_CMPB on zero, then use PWMx_CMPA/PWMx_CMPB values greater than or equal to 1. If loading PWMx_CMPA/PWMx_CMPB on period, then use PWMx_CMPA/PWMx_CMPB values less than or equal to TBPRD - 1. This means there is always a pulse of at least 1 TBCLK cycle in a PWM period which, when very short, tend to be ignored by the system.

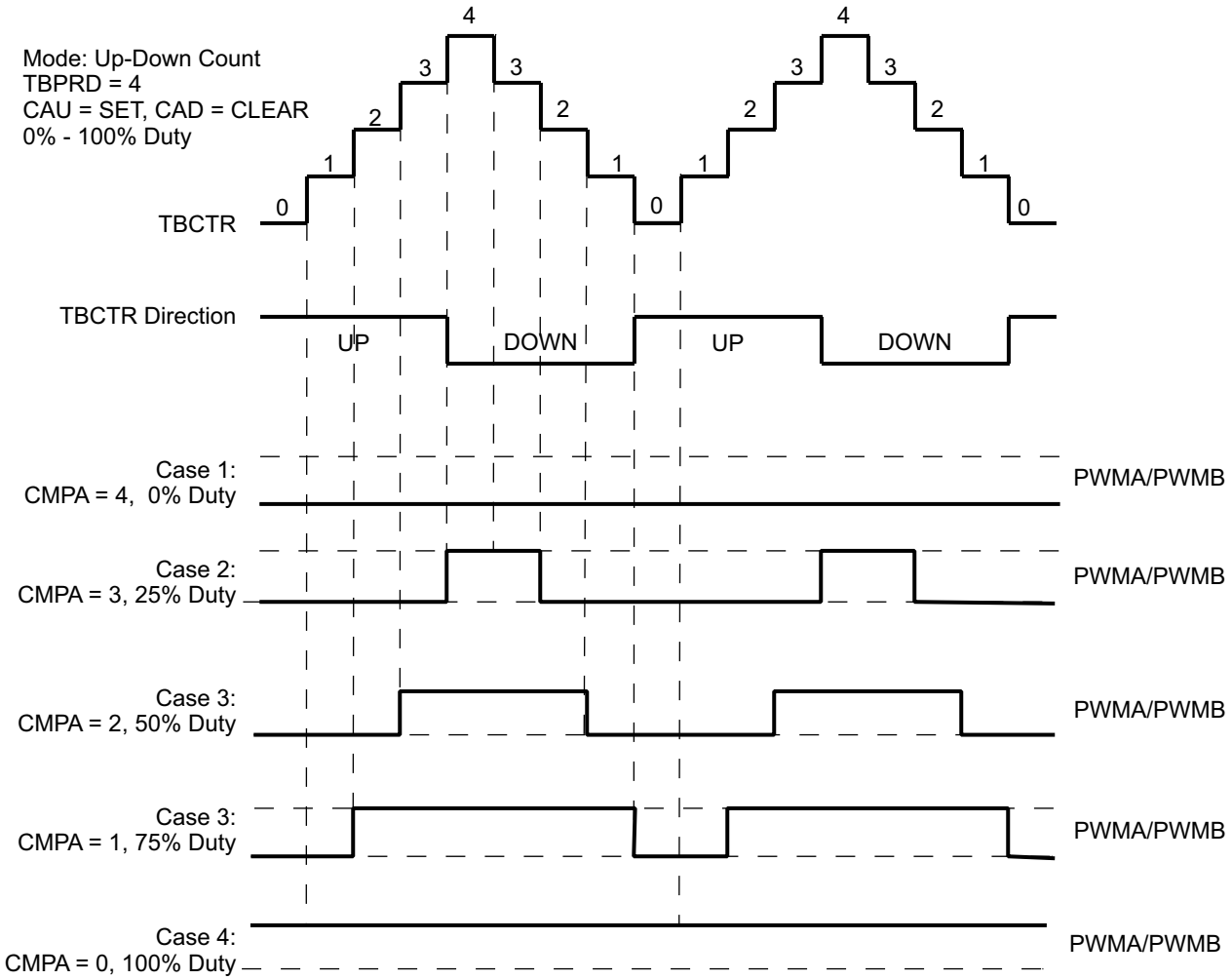


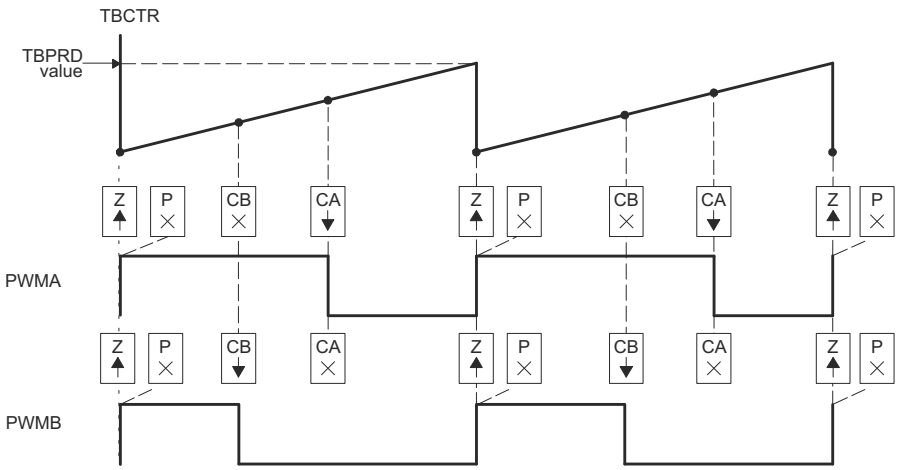
Figure 26-22. Up-Down Count Mode Symmetrical Waveform

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The following PWM waveforms show some common action-qualifier configurations. Some conventions used in the figures and examples are as follows:

- TBPRD, PWMx_CMPA, and PWMx_CMPB refer to the value written in the respective registers. The active register, not the shadow register, is used by the hardware.
- CMPx, refers to either PWMx_CMPA or PWMx_CMPB.
- MCPWMx_yA and MCPWMx_yB refer to the output signals from MCPWMx, Channel pair y.
- Up-Down means count-up and count-down mode, Up means up-count mode.
- Sym = Symmetric, Asym = Asymmetric.

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Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for MCPWMx_yA is set by PWMy_CMPA, and is active high (that is, high time duty proportional to PWMy_CMPA).

Note

Duty modulation for MCPWMx_yB is set by PWMy_CMPB and is active high (that is, high time duty proportional to PWMy_CMPB).

Note

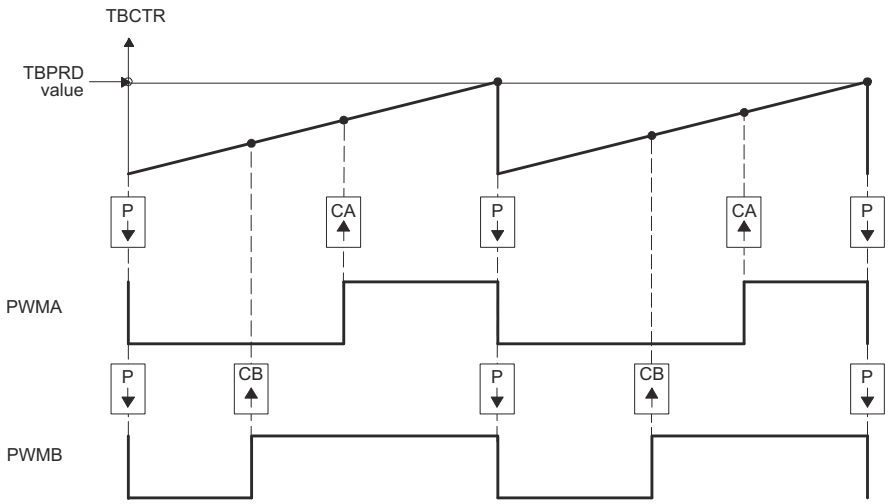
The "Do Nothing" actions (X) are shown for completeness, but are not shown on subsequent diagrams.

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCTR wraps from period to 0000.

Figure 26-23. Up, Single Edge Asymmetric Waveform, with Independent Modulation on PWMxA and PWMxB—Active High

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Note

PWM period = (TBPRD + 1) × T_{TBCLK}

Note

Duty modulation for MCPWMx_yA is set by PWMy_CMPA, and is active low (that is, the low time duty is proportional to PWMy_CMPA).

Note

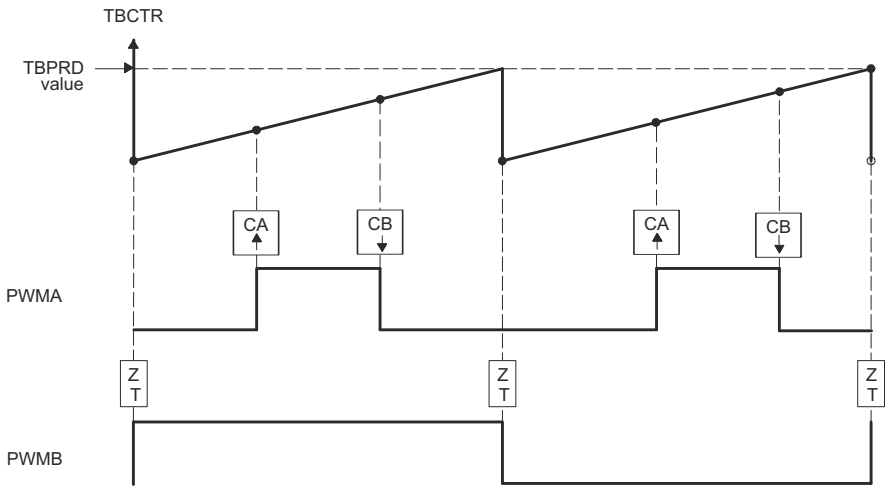
Duty modulation for MCPWMx_yB is set by PWMy_CMPB and is active low (that is, the low time duty is proportional to PWMy_CMPB).

Note

Actions at zero and period, although appearing to occur concurrently, are actually separated by one TBCLK period. TBCTR wraps from period to 0000.

Figure 26-24. Up, Single Edge Asymmetric Waveform with Independent Modulation on PWMxA and PWMxB—Active Low

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Note

PWM frequency = 1/((TBPRD + 1) × T_{TBCLK})

Note

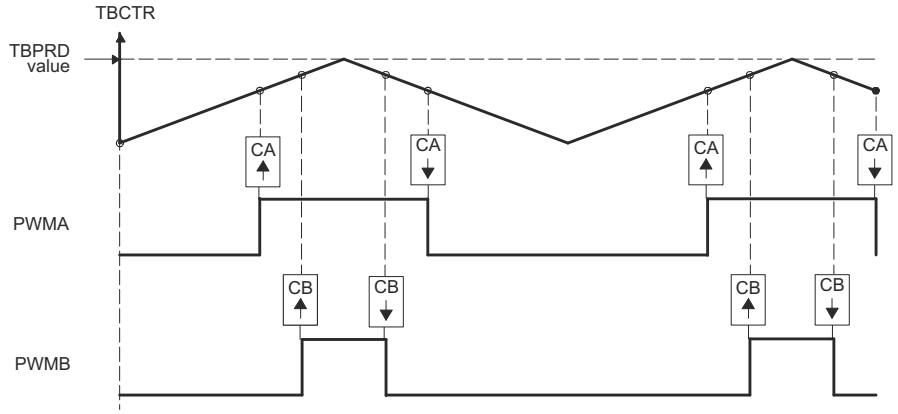
Pulse can be placed anywhere within the PWM cycle (0000 - TBPRD)

Note

High time duty proportional to (CMPB - CMPA)

Figure 26-25. Up-Count, Pulse Placement Asymmetric Waveform With Independent Modulation on PWMxA

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Note

PWM period = 2 x TBPRD × T_{TBCLK}

Note

Duty modulation for MCPWMx_yA is set by PWMy_CMPA, and is active low (that is, the low time duty is proportional to PWMy_CMPA).

Note

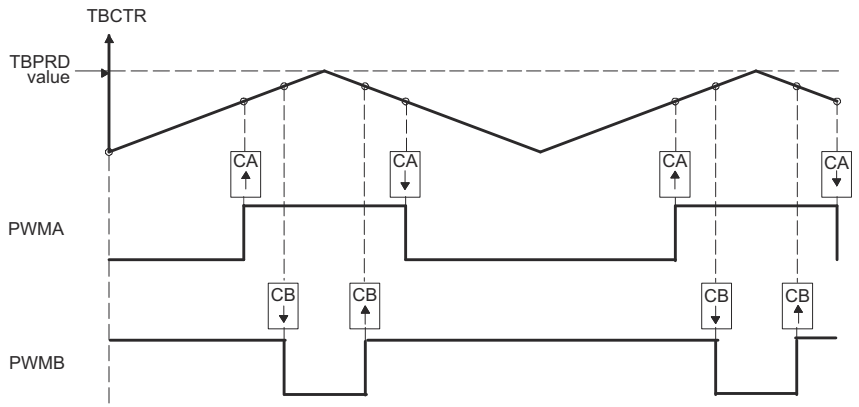
Duty modulation for MCPWMx_yB is set by PWMy_CMPB and is active low (that is, the low time duty is proportional to PWMy_CMPB).

Note

Outputs MCPWMx_yA and MCPWMx_yB can drive independent power switches.

Figure 26-26. Up-Down Count, Dual-Edge Symmetric Waveform, with Independent Modulation on PWMxA and PWMxB — Active Low

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Note

PWM period = 2 × TBPRD × T_{TBCLK}

Note

Duty modulation for MCPWMx_yA is set by PWMy_CMPA, and is active low, that is, low time duty proportional to PWMy_CMPA.

Note

Duty modulation for MCPWMx_yB is set by PWMy_CMPB and is active high, that is, high time duty proportional to PWMy_CMPB.

Note

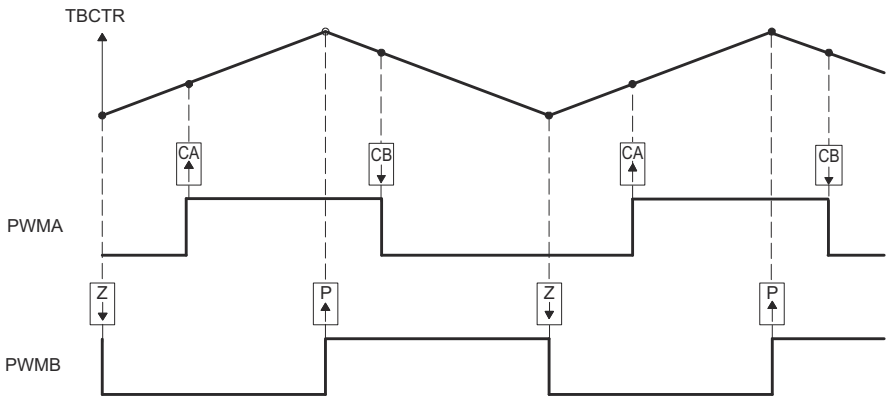
Outputs MCPWMx can drive upper/lower (complementary) power switches.

Note

Dead-band = CMPB - CMPA (fully programmable edge placement by software). Note the dead-band module is also available if the more classical edge delay method is required.

Figure 26-27. Up-Down Count, Dual-Edge Symmetric Waveform, with Independent Modulation on PWMxA and PWMxB — Complementary

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Note

PWM period = 2 × TBPRD × TBCLK

Note

Rising edge and falling edge can be asymmetrically positioned within a PWM cycle. This allows for pulse placement techniques.

Note

Duty modulation for MCPWMx_yA is set by PWMy_CMPA and PWMy_CMPB.

Note

Low time duty for MCPWMx_yA is proportional to (PWMy_CMPA + PWMy_CMPB).

Note

To change this example to active high, PWMy_CMPA and PWMy_CMPB actions need to be inverted (that is, Clear on PWMy_CMPA, Set on PWMy_CMPB).

Note

Duty modulation for MCPWMx_yB is fixed at 50% (utilizes spare action resources for MCPWMx_yB).

Figure 26-28. Up-Down Count, Dual-Edge Asymmetric Waveform, with Independent Modulation on PWMxA—Active Low

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26.7 Dead-Band Generator (DB) Submodule

Figure 26-29 illustrates the dead-band submodule within the MCPWM.

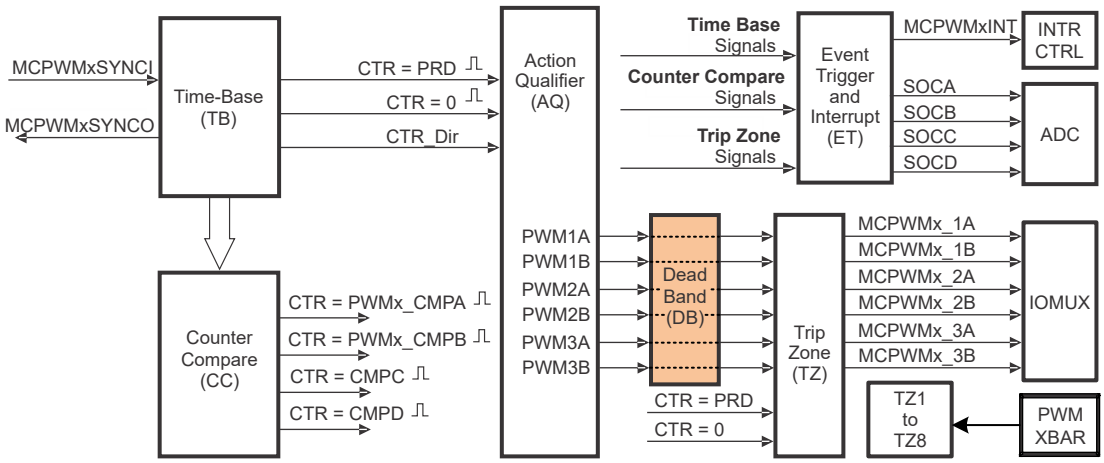


Figure 26-29. Dead-band Generator Submodule

26.7.1 Purpose of the Dead-Band Submodule

The action-qualifier (AQ) module section discussed how the AQ module can generate the required dead band by having full control over edge placement using both the PWMx_CMPA and PWMx_CMPB resources of the MCPWM module. However, if the more classical edge delay-based dead band with polarity control is required, then the dead-band submodule described here must be used.

The key functions of the dead-band module are:

- Generating appropriate signal pairs (MCPWMx_yA and MCPWMx_yB) with dead-band relationship from a single MCPWMx_yA input
- Programming signal pairs for:
  - Active high (AH)
  - Active low (AL)
  - Active high complementary (AHC)
  - Active low complementary (ALC)
- Adding programmable delay to rising edges (RED)
- Adding programmable delay to falling edges (FED)
- Can be totally bypassed from the signal path (note dotted lines in diagram)

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26.7.2 Dead-Band Submodule Additional Operating Modes

On the type-1 ePWM, RED can appear on one channel output and FED can appear on the other channel output.

The dead-band module for MCPWM is unchanged from a type-4 ePWM with the following exceptions:

- Addition of memory-mapped shadow registers for DBCTL, DBFED, and DBRED.
- High-resolution dead-band and half-cycle clocking mode are removed.
- The shadow register for DBCTL is removed.

The following list shows the distinct difference between type-1 and type-4 ePWM modules with respect to dead-band operating modes:

- By adding S6, S7, and S8 in Figure 26-30, RED and FED can appear on both the A-channel and B-channel outputs. Additionally, both RED and FED together can be applied to either the A-channel or B-channel outputs to allow B-channel phase shifting with respect to the A-channel.

Note

Phase shifting B-channel with respect to the A-channel using the dead-band submodule additional operating modes has limitations with respect to the choice of RED and FED delay with respect to the operating duty cycle of the PWMxA and PWMxB outputs.

- The dead-band counters have also been increased to 14 bits
- Dead-band and dead-band high-resolution registers are now shadowed

Note

Cannot have both RED and FED together applied to both PWMxA and PWMxB. RED and FED together can be applied only to either OutA OR OutB.

Phase shifting B-channel with respect to the A-channel: When PWMxB is derived from PWMxA using the DEDB_MODE bit and by delaying rising edge and falling edge by the phase shift amount. When the duty cycle value on PWMxA is less than this phase shift amount, PWMxA's falling edge has precedence over the delayed rising edge for PWMxB. Make sure the duty cycle value of the current waveform applied to the dead-band module is greater than the required phase shift amount.

The type-4 action qualifier and dead-band outputs of the ePWM module are delayed by one TBCLK cycle in comparison to the type-2 ePWM module, although the type-4 ePWM behavior is the same as the type-3 ePWM. Both PWMA and PWMB signals are delayed under all circumstances.

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Shadow Mode:

The shadow mode for the DBRED and DBFED registers is always enabled; however, write to the memory-mapped shadow registers (DBREDS, DBFEDS) to utilize shadow loading. Writing to the active register results in an immediate load.

If writing to the shadow register, the content of the shadow register is transferred to the active register on one of the following events as specified by the DBCTL [LOADREDMODE] and DBCTL [LOADFEDMODE] register bits:

- CTR = PRD: Time-base counter equal to the period (TBCTR = TBPRD).
- CTR = Zero: Time-base counter equal to zero (TBCTR = 0x00)
- Both CTR = PRD and CTR = Zero

Global Load Support

Global load control mechanism can also be used for DBRED and DBFED registers by configuring the appropriate bits in the global load configuration register (GLDCTL). When global load mode is selected the transfer of contents from shadow register to active register, for all registers that have a shadow register, occurs at the same event as defined by the configuration bits in the Global Shadow to Active Load Control Register (GLDCTL). The Global load control mechanism is explained in Section 26.4.6 .

Note

When DBRED/DBFED active is loaded with a new shadow value while DB counters are counting, the new DBRED/DBFED value only affects the NEXT PWMx edge and not the current edge.

A dead-band value of zero cannot be used when the Global Shadow to Active Load is set to occur at CTR = ZERO. Similarly, a dead-band value of PRD cannot be used when the Global Shadow to Active Load is set to occur at CTR = PRD.

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26.7.3 Operational Highlights for the Dead-Band Submodule

The configuration options for the dead-band submodule are shown in Figure 26-30.

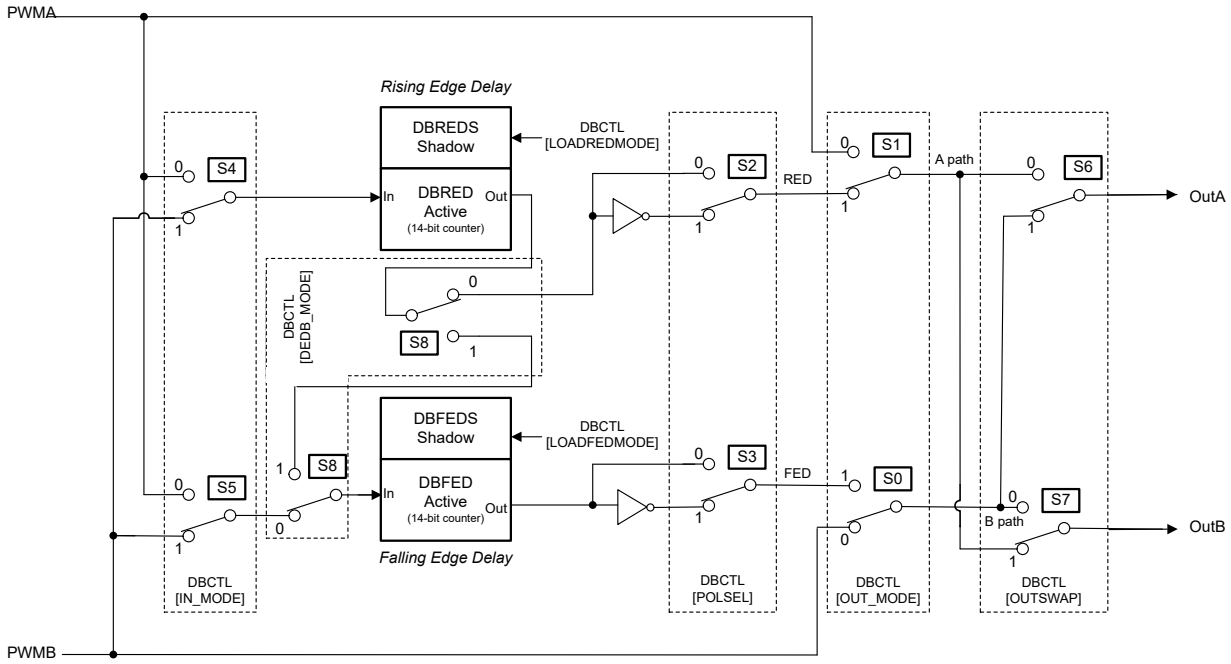


Figure 26-30. Configuration Options for the Dead-Band Submodule

Note

The Dead-Band (DB) submodule is disabled

Note

Dead-band settings are configured by the same register bits for all PWM pairs. Separate dead-band settings for individual PWM pairs within a single MCPWM module is **not supported**.

Although all combinations are supported, not all are typical usage modes. Table 26-8 documents some classical dead-band configurations. These modes assume that the DBCTL[IN_MODE] is configured such that MCPWMx_yA In is the source for both falling-edge and rising-edge delay. Enhanced, or non-traditional modes can be achieved by changing the input signal source. The modes shown in Table 26-8 fall into the following categories:

- **Mode 1: Bypass both falling-edge delay (FED) and rising-edge delay (RED):** Allows the user to fully disable the dead-band submodule from the PWM signal path. **(DEFAULT)**
- **Mode 2-5: Classical Dead-Band Polarity Settings:** These represent typical polarity configurations that can address all the active-high and active-low modes required by available industry power switch gate drivers. The waveforms for these typical cases are shown in Figure 26-31. Note that to generate equivalent waveforms to Figure 26-31, configure the action-qualifier submodule to generate the signal as shown for MCPWMx_yA.
- **Mode 6: Bypass rising-edge delay (RED) and Mode 7: Bypass falling-edge delay (FED):** Finally the last two entries in Table 26-8 show combinations where either the falling-edge delay (FED) or rising-edge delay (RED) blocks are bypassed.

Figure 26-31 shows waveforms for typical cases where 0% < duty < 100%.

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Table 26-8. Classical Dead-Band Operating Modes

Mode	Mode Description	DBCTL[POLSEL]		DBCTL[OUT_MODE]	
		S3	S2	S1	S0
1	MCPWMx_yA and MCPWMx_yB Passed Through (No Delay)	X	X	0	0
2	Active High Complementary (AHC)	1	0	1	1
3	Active Low Complementary (ALC)	0	1	1	1
4	Active High (AH)	0	0	1	1
5	Active Low (AL)	1	1	1	1
6	MCPWMx_yA Out = MCPWMx_yA In (No Delay) MCPWMx_yB Out = MCPWMx_yA In with Falling-Edge Delay	0 or 1	0 or 1	0	1
7	MCPWMx_yA Out = MCPWMx_yA In with Rising-Edge Delay MCPWMx_yB Out = MCPWMx_yB In with No Delay	0 or 1	0 or 1	1	0

Table 26-9. Additional Dead-Band Operating Modes

Mode Description	DBCTL[DEDB-MODE]	DBCTL[OUTSWAP]	
	S8	S6	S7
MCPWMx_yA and MCPWMx_yB signals are as defined by OUT-MODE bits.	0	0	0
MCPWMx_yA = A-path as defined by OUT-MODE bits. MCPWMx_yB = A-path as defined by OUT-MODE bits (rising-edge delay or delay-bypassed A-signal path)	0	0	1
MCPWMx_yA = B-path as defined by OUT-MODE bits (falling-edge delay or delay-bypassed B-signal path) MCPWMx_yB = B-path as defined by OUT-MODE bits	0	1	0
MCPWMx_yA = B-path as defined by OUT-MODE bits (falling-edge delay or delay-bypassed B-signal path) MCPWMx_yB = A-path as defined by OUT-MODE bits (rising-edge delay or delay-bypassed A-signal path)	0	1	1
Rising-edge delay applied to MCPWMx_yA / MCPWMx_yB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling-edge delay applied to MCPWMx_yA / MCPWMx_yB as selected by S5 switch (IN-MODE bits) on B signal path only.	0	X	X
Rising-edge delay and falling-edge delay applied to source selected by S4 switch (IN-MODE bits) and output to B signal path only.(1)	1	X	X

(1) When this bit is set to 1, the user can always either set OUT_MODE bits such that Apath = InA or set OUTSWAP bits such that MCPWMx_yA=Bpath. Otherwise, MCPWMx_yA is invalid.

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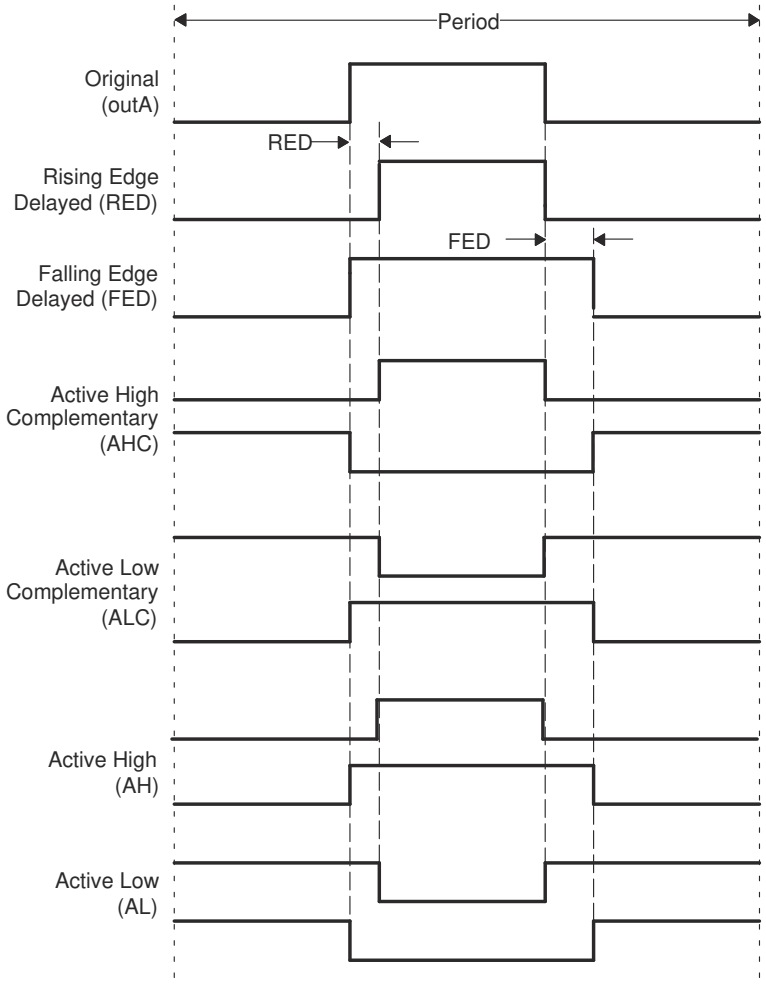


Figure 26-31. Dead-Band Waveforms for Typical Cases (0% < Duty < 100%)

The dead-band submodule supports independent values for rising-edge (RED) and falling-edge (FED) delays. The amount of delay is programmed using the DBRED and DBFED registers. These are 10-bit registers and the value represents the number of TBCLK (time-base clock) pulses by which a signal edge is delayed. For example, the formula to calculate falling-edge-delay and rising-edge-delay is:

FED = DBFED × T_{TBCLK}

RED = DBRED × T_{TBCLK}

Where T_{TBCLK} is the period of TBCLK, the prescaled version of PWMCLK. The TBCLK.CLKDIV register bitfield supports divider options from /1 to /32768.

Table 26-10. TBCLK Prescale Options

TBCTL.CLKDIV Binary Value (Decimal)	Prescale/Divider Value
0000 (0) **(Default)**	TBCLK = PWMCLK/1
0001 (1)	TBCLK = PWMCLK/2
0010 (2)	TBCLK = PWMCLK/4
0011 (3)	TBCLK = PWMCLK/8
0100 (4)	TBCLK = PWMCLK/16

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Table 26-10. TBCLK Prescale Options (continued)

TBCTL.CLKDIV Binary Value (Decimal)	Prescale/Divider Value
0101 (5)	TBCLK = PWMCLK/32
0110 (6)	TBCLK = PWMCLK/64
0111 (7)	TBCLK = PWMCLK/128
1000 (8)	TBCLK = PWMCLK/256
1001 (9)	TBCLK = PWMCLK/512
1010 (10)	TBCLK = PWMCLK/1024
1011 (11)	TBCLK = PWMCLK/2048
1100 (12)	TBCLK = PWMCLK/4096
1101 (13)	TBCLK = PWMCLK/8192
1110 (14)	TBCLK = PWMCLK/16384
1111 (15)	TBCLK = PWMCLK/32768

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The final dead-band delay values for some common TBCLK options are shown in the table below for convenience.

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26.8 Trip-Zone (TZ) Submodule

Each MCPWM module is connected to eight $\overline{TZn}$ signals ($\overline{TZ1}$ to $\overline{TZ8}$). All eight $\overline{TZn}$ signals are sourced from the PWM X-BAR. Refer to the *Crossbar (X-BAR)* chapter to see what signals can be routed to the MCPWM module to be used as a trip source. These signals indicate external fault or trip conditions, and the MCPWM outputs can be programmed to respond accordingly when faults occur.

Figure 26-32 illustrates the trip-zone submodule within the MCPWM.

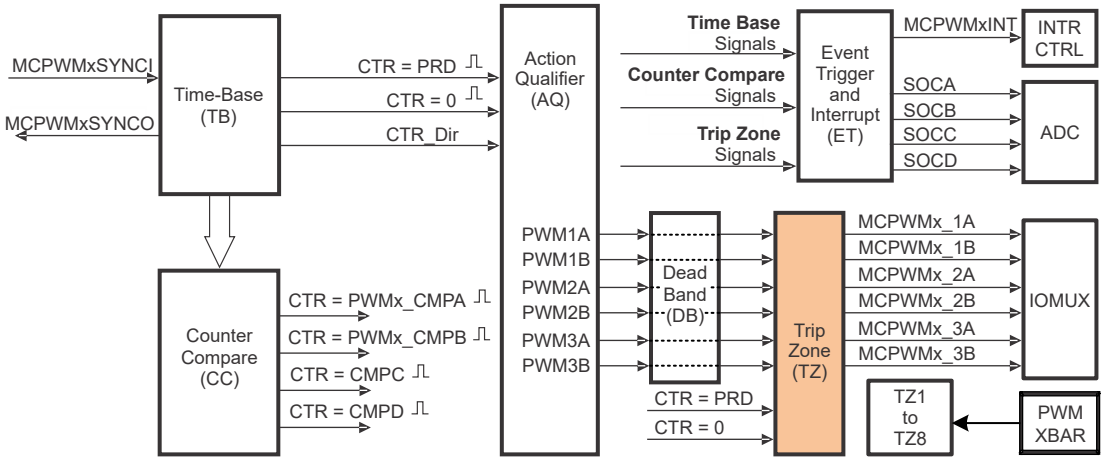


Figure 26-32. Trip-Zone Submodule

26.8.1 Purpose of the Trip-Zone Submodule

The key functions of the trip-zone submodule are:

- Trip inputs $\overline{TZ1}$ to $\overline{TZ8}$ can be flexibly mapped to any MCPWM module.
- Upon a fault condition, outputs MCPWMx_yA and MCPWMx_yB can be forced to one of the following:
  - High
  - Low
  - High-impedance
  - No action taken
- Support for one-shot trip (OST) for major short circuits or over-current conditions.
- Support for cycle-by-cycle tripping (CBC) for current limiting operation.
- Each trip-zone input can be allocated to either one-shot or cycle-by-cycle operation.
- Interrupt generation is possible on any trip-zone input.
- The trip-zone submodule can be fully bypassed if the trip-zone submodule is not required.

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26.8.2 Operational Highlights for the Trip-Zone Submodule

The following sections describe the operational highlights and configuration options for the trip-zone submodule.

Trip Zone Inputs

The trip-zone signals $\overline{TZ1}$ to $\overline{TZ8}$ (also collectively referred to as $\overline{TZn}$) are active-low input signals. When one of these signals goes low, the indication is that a trip event has occurred. Each MCPWM module can be individually configured to ignore or use each of the trip-zone signals. Note that the trip zone settings for all PWM pairs are configured by the same register bits, separate trip-zone settings for separate PWM pairs within a single MCPWM module is not supported. The trip-zone signals used by a particular MCPWM module can be enabled or disabled in the TZSEL register for that specific MCPWM module. The trip-zone signals can also be digitally filtered within the block.

A minimum of 3 × TBCLK low pulse width on $\overline{TZn}$ inputs is sufficient to trigger a fault condition on the MCPWM module. If the pulse width is less than this, the trip condition cannot be latched by CBC or OST latches. The asynchronous trip makes sure that if clocks are missing for any reason, the outputs can still be tripped by a valid event present on $\overline{TZn}$ inputs. The GPIOs or peripherals must be appropriately configured.

Conguration of the MCPWM input signal sources is done using the PWM XBAR module. The table below indicates which PWM XBAR signal is routed to each $\overline{TZn}$.

Cycle-By-Cycle and One-Shot Trips

Each $\overline{TZn}$ input can be individually configured to provide either a cycle-by-cycle (CBC) or one-shot (OST) trip event for an MCPWM module. This configuration is determined by the TZSEL[CBCn], and TZSEL[OSTn] control bits (where n corresponds to the trip input), respectively.

- **Cycle-by-Cycle (CBC)**
  - When a cycle-by-cycle trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the MCPWMx_yA and MCPWMx_yB outputs. The same trip actions are taken on all PWM pairs, denoted by "y". Table 26-12 lists some of the possible actions.
  - Additionally, when a cycle-by-cycle trip event occurs, the cycle-by-cycle trip event flag (INTFLAG[CBC]) is set and a PWMx interrupt is generated if the INTEN[CBC] bit is set. A corresponding flag for the specific event that caused the CBC interrupt is also set in the TZCBCOSTFLAG register, which can be cleared by writing to the corresponding flag in TZCBCOSTCLR.
  - The specified condition on the inputs is automatically cleared based on the selection made with INTCLR[CBC] if the trip event is no longer present. Therefore, in this mode, the trip event is cleared or reset every PWM cycle. The INTFLG[CBC] and TZCBCOSTFLAG flag bits remain set until the flag bits are manually cleared by writing to the INTCLR[CBC] and TZCBCOSTCLR flag bits. If the cycle-by-cycle trip event is still present when the INTFLG[CBC] and TZCBCOSTFLAG register bits are cleared, then these bits are again immediately set.
- **One-Shot (OST)**
  - When a one-shot trip event occurs, the action specified in the TZCTL[TZA] and TZCTL[TZB] bits is carried out immediately on the MCPWMx_yA and MCPWMx_yB output. The same trip actions are taken on all PWM pairs, denoted by "y". Table 26-12 lists some of the possible actions.
  - Additionally, when a one-shot trip event occurs, the one-shot trip event flag (INTFLG[OST]) is set and a PWMx interrupt is generated if the INTEN[OST] bit is set.. A corresponding flag for the event that caused the OST event is also set in register TZCBCOSTFLAG. The one-shot trip condition must be cleared manually by writing to the INTCLR[OST] bit. If desired, the TZCBCOSTFLAG register bit can also be cleared by manually writing to the corresponding bit in the TZCBCOSTCLR register.

Note

Clear the INTFLAG and TZCBCOSTFLAG flags after making sure that the TRIPIN source of the OST has become inactive. Otherwise, if interrupts are enabled, depending on when the flags are cleared, an OST interrupt can occur where the OST flags are zero.

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Trip Event Actions

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The action taken when a trip event occurs can be configured individually for the A outputs and B outputs of the MCPWM module, but the action is the same across all A outputs and the same across all B outputs. Trip actions are specified by the TZCTL register. Some of the possible actions, shown in Table 26-12, can be taken on a trip event.

Table 26-12. Possible Actions On a Trip Event

TZCTL[TZx] Register Bitfield Settings	MCPWMx_yA and MCPWMx_yB	Comment
0,0	High-Impedance	Tripped
0,1	Force to High State	Tripped
1,0	Force to Low State	Tripped
1,1	No Change	Do Nothing. No change is made to the output.

Trip-Zone Configurations

Scenario A:
A one-shot trip event on $\overline{TZ1}$ pulls the MCPWM1_yA, MCPWM1_yB outputs low.

- Configure the MCPWM1 registers as follows:
  - TZSEL[OST1] = 1: enables $\overline{TZ1}$ as a one-shot event source for MCPWM1
  - TZCTL[TZA] = 2: MCPWM1_yA is forced low on a trip event.
  - TZCTL[TZB] = 2: MCPWM1_yB is forced low on a trip event.

Scenario B:
A cycle-by-cycle event on $\overline{TZ1}$ or $\overline{TZ6}$ puts MCPWM1_yA into a high-impedance state, MCPWM1_yB is unaffected.

- Configure the MCPWM1 registers as follows:
  - TZSEL[CBC1] = 1: enables $\overline{TZ1}$ as a cycle-by-cycle event source for MCPWM1
  - TZSEL[CBC6] = 1: enables $\overline{TZ6}$ as a cycle-by-cycle event source for MCPWM1
  - TZCTL[TZA] = 0: MCPWM1_yA is put into a high-impedance state on a trip event.
  - TZCTL[TZB] = 3: MCPWM1_yB ignores the trip event.

Note

When configuring the GPIOs and INPUT X-BAR/MCPWM X-BAR options, be aware that a change in the X-BAR input selections can cause an unwanted event. Therefore, set up the GPIO and X-BAR input configurations before enabling the MCPWM Trip-Zone. If a requirement is to change the GPIO/X-BAR configurations while the MCPWM Trip-Zone is enabled, the user can turn off the TRIPs by clearing the TZSEL register and reconfiguring the TRIP selection (TZSEL) after the INPUT X-BAR selection is changed.

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26.8.3 Generating Trip Event Interrupts

Figure 26-33 illustrates the trip-zone submodule control logic.

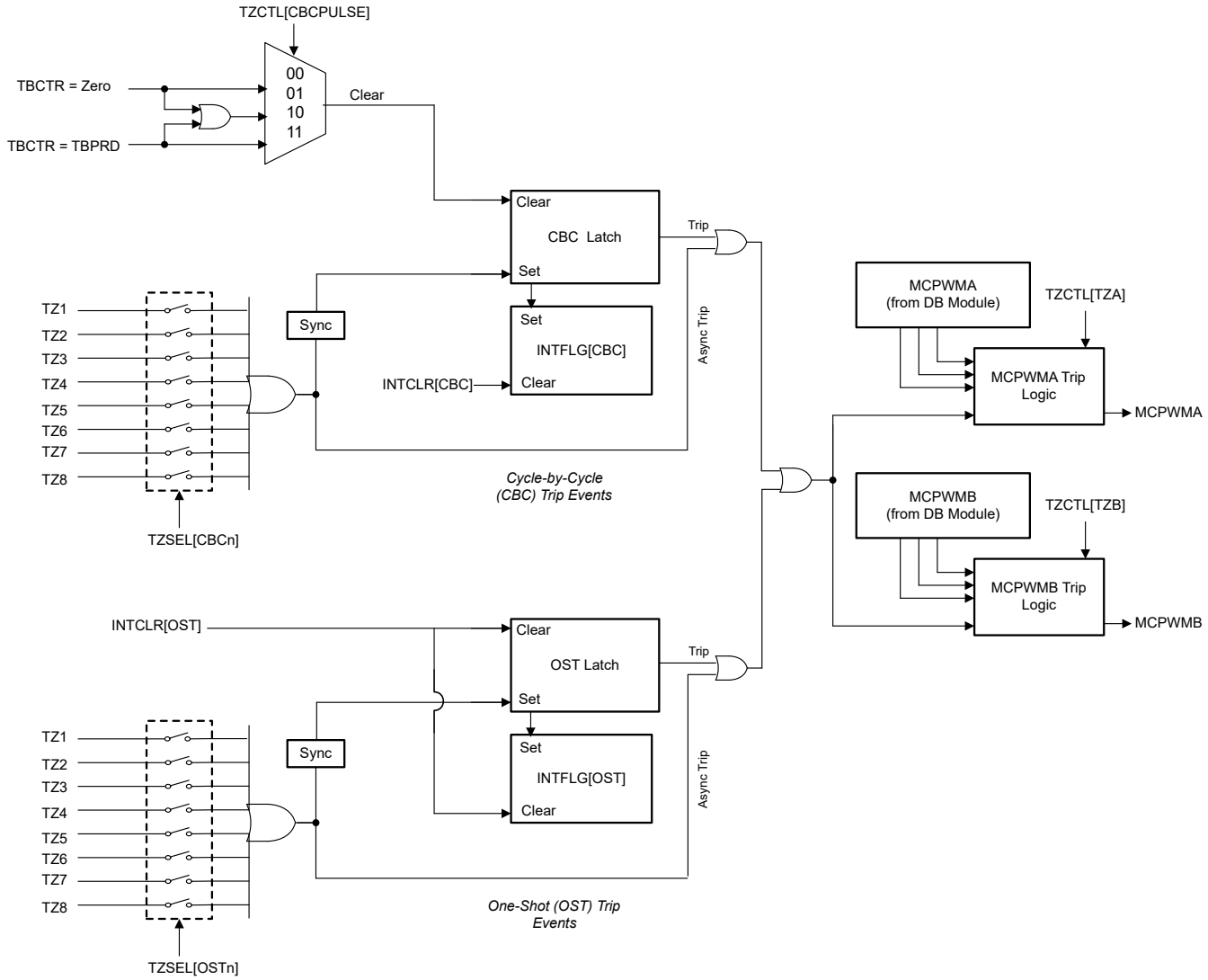


Figure 26-33. Trip-Zone Submodule Mode Control Logic

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26.9 Event-Trigger (ET) Submodule

The key functions of the event-trigger submodule are:

- Receives event inputs generated by the time-base and counter-compare submodules
- Uses the time-base direction information for up/down event qualification
- Uses prescaling logic to issue interrupt requests and ADC start of conversion at:
  - Every event
  - Every second event
  - ...
  - Up to every seventh event
- Uses TZ signals to interrupt the CPU on a trip zone event
- Provides full visibility of event generation using event counters and flags
- Allows software forcing of interrupts

The event-trigger submodule manages the events generated by the time-base submodule, counter-compare submodule, and trip-zone submodule to generate an interrupt to the CPU or a start of conversion pulse to the ADC when a selected event occurs.

Figure 26-34 illustrates the event-trigger submodule within the MCPWM.

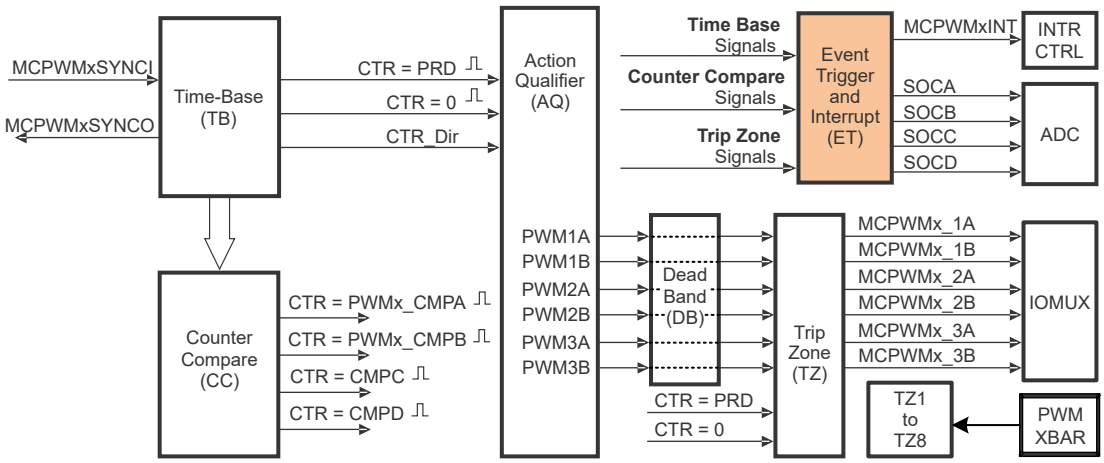


Figure 26-34. Event-Trigger Submodule

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26.9.1 Operational Overview of the MCPWM Event-Trigger Submodule

The event-trigger submodule monitors various event conditions (shown as inputs on the left side of Figure 26-35) and can be configured to prescale these events before issuing an Interrupt request or an ADC start of conversion. The event-trigger prescaling logic can issue interrupt requests and ADC start-of-conversion at:

- Every event
- Every second event
- Up to every seventh event

Figure 26-35. Event-Trigger Submodule Showing Event Inputs and Prescaled Outputs

- ETSEL: This selects which of the possible events trigger events ET1 or ET2.
- ETPERIOD: This programs the event prescaling options mentioned above.
- ETCNT: This indicates how many events have occurred if the prescaling feature is used.
- INTEN: This enables interrupt sources for the MCPWM.
- INTFLAG: These are flag bits indicating whether an E1x or trip event has occurred.
- INTCLR: These bits allow clearing the flag bits in the INTFLAG register using software.
- INTFRC: These bits allow software forcing of an event. Useful for debugging or software intervention.
- SOCEN: This enables ADC start of conversion events.
- SOCSEL: This selects the trigger sources for the ADC start of conversion events.
- SOCPERIOD: This programs the event prescaling options for SOC events.
- SOCCNT: This indicates how many SOC events have been generated when using the prescaling feature.
- SOCFLAG: This indicates which SOC events have been generated.
- SOCCLR: This clears the SOCFLAG bits when written to using software.

A more detailed look at how the various register bits interact with the interrupt and ADC start-of-conversion logic are shown in Figure 26-36 and Figure 26-37.

Figure 26-36 shows the event-trigger interrupt generation logic. The interrupt-period (ETPERIOD[ETx_PERIOD]) bits specify the number of events required to cause an interrupt pulse to be generated. The choices available are:

- Do not generate an interrupt.
- Generate an interrupt on every event.
- Generate an interrupt on every second event.
- Generate an interrupt on up to every seventh event.

The event that can cause an interrupt is configured by the interrupt enable(INTEN) register and event trigger selection (ETSEL) register. The event can be one of the following:

- Time-base counter equal to zero (TBCTR = 0x00).
- Time-base counter equal to period (TBCTR = TBPRD).
- Time-base counter equal to zero or period (TBCTR = 0x00 || TBCTR = TBPRD).
- Time-base counter equal to the compare A register (CMPA) when the timer is incrementing.
- Time-base counter equal to the compare A register (CMPA) when the timer is decrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is incrementing.
- Time-base counter equal to the compare B register (CMPB) when the timer is decrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is incrementing.
- Time-base counter equal to the compare C register (CMPC) when the timer is decrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is incrementing.
- Time-base counter equal to the compare D register (CMPD) when the timer is decrementing.
- One-shot trip event.
- Cycle-by-cycle trip event.

The number of events that have occurred can be read from the interrupt event counter ETCNT[ETx_CNT] register bits based off of the selection made using ETSEL. The specified event increments the

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ETCNT[ETx_CNT] bits until the bits reach the value specified by ETPERIOD[ETx_PERIOD]. When ETPS[INTCNT] = ETPS[INTPRD], the counter stops counting and the counter output is set. The counter is cleared when an INTFLAG[ETx] event is generated.

When ETCNT[ETx_CNT] reaches ETPERIOD[ETx_PERIOD], the following behavior occurs:

If interrupts are enabled, INTEN[ETx] = 1 and the interrupt flag is clear,INTFLAG[ETx] = 0, then an interrupt pulse is generated and the interrupt flag is set, INTFLAG[ETx] = 1. The counter is reset and begins counting events again

- If interrupts are disabled, INTEN[ETx] = 0, or the interrupt flag is set, INTFLAG[ETx] = 1, the counter stops counting events when the counter reaches the period value ETCNT[ETx_CNT] = ETPERIOD[ETx_PERIOD].
- If interrupts are enabled, but the interrupt flag is already set, then the counter holds the output high until the INTFLAG[ETx] flag is cleared. This allows for one interrupt to be pending while one is serviced.

Writing a 0 or a value that is less than the current ETCNT value to the ETPERIOD bits results in the counter going to an undefined state.

The previous definition means that an interrupt on every event up to 7 events if using the ETCNT and ETPERIOD can be generated.

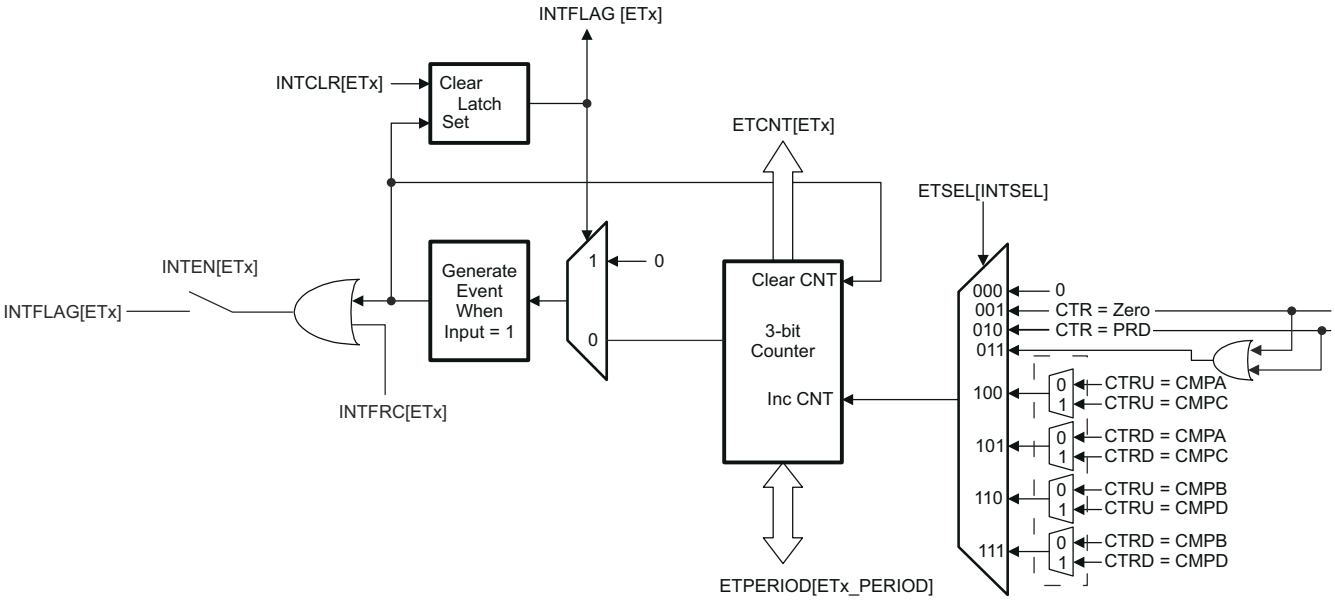


Figure 26-36. Event-Trigger Interrupt Generator

Figure 26-37 shows the operation of the event-trigger's start-of-conversion (SOCx) pulse generator. The SOCCNT[SOCx_CNT] counters and SOCPERIOD[SOCx_PERIOD] period values behave similarly to the interrupt generator except that the pulses are continuously generated. That is, the pulse flag SOCFLAG[SOCx] is latched when a pulse is generated, but the interrupt generator does not stop further pulse generation. The enable and disable bit SOCEN[SOCx_ENABLE] stops pulse generation, but input events can still be counted until the period value is reached as with the interrupt generation logic. The event that triggers an SOCx pulse can be configured separately in the SOCSEL[SOCx_SEL] bits. The possible events are the same events that can be specified for the interrupt generation logic.

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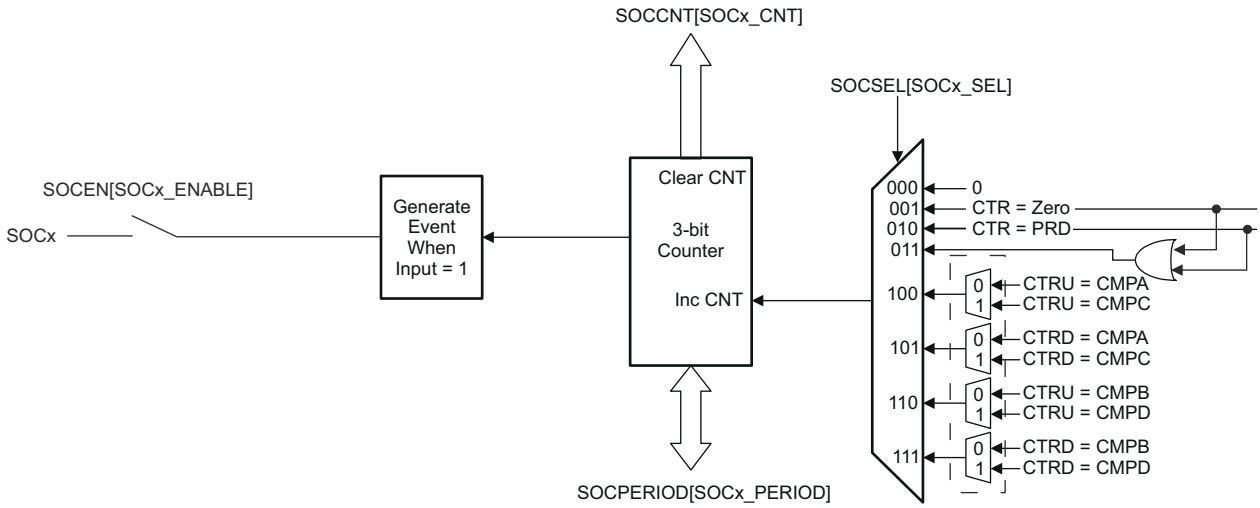


Figure 26-37. Event-Trigger Start-of-Conversion (SOC) Pulse Generator

26.10 PWM X-BAR

The ePWM Crossbar (X-BAR) enables selection of various trigger sources into specific dedicated EPWM trip inputs TRIPx. See Section 19.2 for more information on input selection options and PWM X-BAR / ePWM module connections.

26.11 MCPWM Interrupts & Triggers

26.11.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 26-13. CPU Interrupts Triggered by MCPWM

NVIC Interrupt Name	Peripheral Instance Name	Register Group	MCPWM Interrupt Configuration Registers	Description
MCPWM0_INT	MCPWM0	N/A	INTEN, INTFLAG, INTFRC, INTCLR	MCPWM0 interrupt. Multiple OR'd, configurable source conditions.
MCPWM1_INT	MCPWM1	N/A	INTEN, INTFLAG, INTFRC, INTCLR	MCPWM1 interrupt. Multiple OR'd, configurable source conditions.
MCPWM2_INT	MCPWM2	N/A	INTEN, INTFLAG, INTFRC, INTCLR	MCPWM2 interrupt. Multiple OR'd, configurable source conditions.

26.11.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

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Table 26-14. DMA Triggers from the MCPWM

Trigger Name	Peripheral Instance Name	Register Group	MCPWM DMA Configuration Registers	Description
MCPWM0_SOCA	MCPWM0	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM0 SOCA DMA trigger. Single, configurable source condition.
MCPWM0_SOCB	MCPWM0	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM0 SOCB DMA trigger. Single, configurable source condition.
MCPWM0_SOCC	MCPWM0	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM0 SOCC DMA trigger. Single, configurable source condition.
MCPWM0_SOCD	MCPWM0	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM0 SOCD DMA trigger. Single, configurable source condition.
MCPWM1_SOCA	MCPWM1	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM1 SOCA DMA trigger. Single, configurable source condition.
MCPWM1_SOCB	MCPWM1	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM1 SOCB DMA trigger. Single, configurable source condition.
MCPWM1_SOCC	MCPWM1	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM1 SOCC DMA trigger. Single, configurable source condition.
MCPWM1_SOCD	MCPWM1	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM1 SOCD DMA trigger. Single, configurable source condition.
MCPWM2_SOCA	MCPWM2	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM2 SOCA DMA trigger. Single, configurable source condition.

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Table 26-14. DMA Triggers from the MCPWM (continued)

Trigger Name	Peripheral Instance Name	Register Group	MCPWM DMA Configuration Registers	Description
MCPWM2_SOCB	MCPWM2	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM2 SOCB DMA trigger. Single, configurable source condition.
MCPWM2_SOCC	MCPWM2	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM2 SOCC DMA trigger. Single, configurable source condition.
MCPWM2_SOCD	MCPWM2	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM2 SOCD DMA trigger. Single, configurable source condition.

26.11.3 ADC Sequencer Triggers

See the Section 20.3.3 section for more details about how to configure triggers for individual ADC sequencers.

Table 26-15. ADC Triggers from the MCPWM

Trigger Name	Peripheral Instance Name	Register Group	MCPWM ADC Trigger Configuration Registers	Description
MCPWM0_SOCA	MCPWM0	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM0 SOCA ADC trigger. Single, configurable source condition.
MCPWM0_SOCB	MCPWM0	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM0 SOCB ADC trigger. Single, configurable source condition.
MCPWM0_SOCC	MCPWM0	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM0 SOCC ADC trigger. Single, configurable source condition.
MCPWM0_SOCD	MCPWM0	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM0 SOCD ADC trigger. Single, configurable source condition.
MCPWM1_SOCA	MCPWM1	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM1 SOCA ADC trigger. Single, configurable source condition.

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Table 26-15. ADC Triggers from the MCPWM (continued)

Trigger Name	Peripheral Instance Name	Register Group	MCPWM ADC Trigger Configuration Registers	Description
MCPWM1_SOCB	MCPWM1	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM1 SOCB ADC trigger. Single, configurable source condition.
MCPWM1_SOCC	MCPWM1	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM1 SOCC ADC trigger. Single, configurable source condition.
MCPWM1_SOCD	MCPWM1	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM1 SOCD ADC trigger. Single, configurable source condition.
MCPWM2_SOCA	MCPWM2	N/A	SOCEN.SOCA_ENABLE, SOCSEL.SOCA_SEL, SOCPERIOD.SOCA_PERIOD, SOCCNT.SOCA_CNT, SOCFLAG.SOCA, SOCCLR.SOCA	MCPWM2 SOCA ADC trigger. Single, configurable source condition.
MCPWM2_SOCB	MCPWM2	N/A	SOCEN.SOCB_ENABLE, SOCSEL.SOCB_SEL, SOCPERIOD.SOCB_PERIOD, SOCCNT.SOCB_CNT, SOCFLAG.SOCB, SOCCLR.SOCB	MCPWM2 SOCB ADC trigger. Single, configurable source condition.
MCPWM2_SOCC	MCPWM2	N/A	SOCEN.SOCC_ENABLE, SOCSEL.SOCC_SEL, SOCPERIOD.SOCC_PERIOD, SOCCNT.SOCC_CNT, SOCFLAG.SOCC, SOCCLR.SOCC	MCPWM2 SOCC ADC trigger. Single, configurable source condition.
MCPWM2_SOCD	MCPWM2	N/A	SOCEN.SOCD_ENABLE, SOCSEL.SOCD_SEL, SOCPERIOD.SOCD_PERIOD, SOCCNT.SOCD_CNT, SOCFLAG.SOCD, SOCCLR.SOCD	MCPWM2 SOCD ADC trigger. Single, configurable source condition.

26.12 MCPWM Registers

This Section describes the MCPWM Registers.

26.12.1 MCPWM Base Address Table

Table 26-16. MCPWM Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Mcpwm0Regs	MCPWM_6CH_REGS	MCPWM0	0x4001_0000
Mcpwm1Regs	MCPWM_6CH_REGS	MCPWM1	0x4001_1000
Mcpwm2Regs	MCPWM_6CH_REGS	MCPWM2	0x4001_2000

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26.12.2 MCPWM_6CH_REGS Registers

Table 26-17 lists the memory-mapped registers for the MCPWM_6CH_REGS registers. All register offset addresses not listed in Table 26-17 should be considered as reserved locations and the register contents should not be modified.

Table 26-17. MCPWM_6CH_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	REVISION	IP revision id register		Go
10h	TBCTL	Time base control register		Go
14h	TBPRD	Time base period register		Go
18h	TBPRDS	Time base period shadow register		Go
1Ch	TBPHS	Time base phase offset register		Go
20h	TBSTS	Time base status register		Go
24h	TBSTSCLR	Time base status clear register		Go
28h	TBCTR	Time base counter register		Go
30h	CMPCTL	Counter compare control register		Go
40h	CMPC	Counter compare C register		Go
44h	CMPD	Counter compare D register		Go
48h	CMPCS	Counter compare C shadow register		Go
4Ch	CMPDS	Counter compare D shadow register		Go
50h	AQCTL	Action qualifier control register		Go
60h	SOCEN	Start of conversion enable		Go
64h	SOCSEL	Start of conversion selection		Go
68h	SOCPERIOD	Start of conversion period		Go
6Ch	SOCCNT	Start of conversion count		Go
70h	SOCFLAG	Start of conversion flag		Go
74h	SOCCLR	Start of conversion clear		Go
80h	ETSEL	Event trigger selection		Go
84h	ETPERIOD	Event trigger period		Go
88h	ETCNT	Event trigger count		Go
90h	INTEN	Interrupt Enable Register		Go
94h	INTFLAG	Interrupt Flag Register		Go
98h	INTCLR	Interrupt Clear Register		Go
9Ch	INTFRC	Interrupt Force Register		Go
A0h	TZSEL	Trip Zone Selection		Go
ACh	TZCTL	Trip Zone control		Go
B0h	TZCBCOSTFLAG	Trip Zone CBC and OST Flag Register		Go
B4h	TZCBCOSTCLR	Trip Zone CBC and OST Clear Register		Go
C0h	DBCTL	Dead band control register		Go
D0h	DBFED	Dead band fall edge delay		Go
D4h	DBRED	Dead band rise edge delay		Go
D8h	DBFEDS	Dead band fall edge delay shadow register		Go
DCh	DBREDS	Dead band rise edge delay shadow register		Go
F0h	GLDCTL	Global load control register		Go
F4h	GLDOSHTCTL	Global load one shot control register		Go
F8h	GLDOSHTSTS	Global load one shot status register		Go
100h	PWM1_CMPA	PWM1 counter compare A register		Go

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Table 26-17. MCPWM_6CH_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
104h	PWM1_CMPAS	PWM1 counter compare A shadow register		Go
108h	PWM1_CMPB	PWM1 counter compare B register		Go
10Ch	PWM1_CMPBS	PWM1 counter compare B shadow register		Go
120h	PWM1_AQCTLA	PWM1 action qualifier A register		Go
124h	PWM1_AQCTLAS	PWM1 action qualifier A shadow register		Go
128h	PWM1_AQCTLB	PWM1 action qualifier B register		Go
12Ch	PWM1_AQCTLBS	PWM1 action qualifier B shadow register		Go
130h	PWM1_AQSFRC	PWM1 action qualifier software force		Go
134h	PWM1_AQOTSFRC	PWM1 action qualifier one time software force		Go
300h	PWM2_CMPA	PWM2 counter compare A register		Go
304h	PWM2_CMPAS	PWM2 counter compare A shadow register		Go
308h	PWM2_CMPB	PWM2 counter compare B register		Go
30Ch	PWM2_CMPBS	PWM2 counter compare B shadow register		Go
320h	PWM2_AQCTLA	PWM2 action qualifier A register		Go
324h	PWM2_AQCTLAS	PWM2 action qualifier A shadow register		Go
328h	PWM2_AQCTLB	PWM2 action qualifier B register		Go
32Ch	PWM2_AQCTLBS	PWM2 action qualifier B shadow register		Go
330h	PWM2_AQSFRC	PWM2 action qualifier software force		Go
334h	PWM2_AQOTSFRC	PWM2 action qualifier one time software force		Go
500h	PWM3_CMPA	PWM3 counter compare A register		Go
504h	PWM3_CMPAS	PWM3 counter compare A shadow register		Go
508h	PWM3_CMPB	PWM3 counter compare B register		Go
50Ch	PWM3_CMPBS	PWM3 counter compare B shadow register		Go
520h	PWM3_AQCTLA	PWM3 action qualifier A register		Go
524h	PWM3_AQCTLAS	PWM3 action qualifier A shadow register		Go
528h	PWM3_AQCTLB	PWM3 action qualifier B register		Go
52Ch	PWM3_AQCTLBS	PWM3 action qualifier B shadow register		Go
530h	PWM3_AQSFRC	PWM3 action qualifier software force		Go
534h	PWM3_AQOTSFRC	PWM3 action qualifier one time software force		Go

Complex bit access types are encoded to fit into small table cells. Table 26-18 shows the codes that are used for access types in this section.

Table 26-18. MCPWM_6CH_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		

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Table 26-18. MCPWM_6CH_REGS Access Type Codes (continued)

Access Type	Code	Description
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 REVISION Register (Offset = 0h) [Reset = 00000007h]

REVISION is shown in Figure 26-38 and described in Table 26-19.

Return to the Summary Table.

IP revision id register

Figure 26-38. REVISION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				CAP_PRESENT	CMPCD_PRESENT	PWM3_PRESENT	PWM2_PRESENT
R-0-0h				R-0h	R-1h	R-1h	R-1h

Table 26-20. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3	CAP_PRESENT	R	0h	This hardcoded field defines the presence of Capture mode feature. Reset type: SYSRSn
2	CMPCD_PRESENT	R	1h	This hardcoded field defines the presence of Compare C and D registers. Reset type: SYSRSn
1	PWM3_PRESENT	R	1h	This hardcoded field defines the presence of PWM3 channels. Reset type: SYSRSn
0	PWM2_PRESENT	R	1h	This hardcoded field defines the presence of PWM2 channels. Reset type: SYSRSn

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2 TBCTL Register (Offset = 10h) [Reset = 00000002h]

TBCTL is shown in Figure 26-39 and described in Table 26-20.

Return to the Summary Table.

Time base control register

Figure 26-39. TBCTL Register

31	30	29	28	27	26	25	24
RESERVED		SYNCISEL					SYNCPERSEL
R-0-0h		R/W-0h					R/W-0h
23	22	21	20	19	18	17	16
SYNCPERSEL		FREE_SOFT		RESERVED	SYNCOSEL		
R/W-0h		R/W-0h		R-0-0h	R/W-0h		
15	14	13	12	11	10	9	8
SWSYNC	RESERVED			PHSDIR	PHSEN	RESERVED	PRDLD
R-0/W1S-0h	R-0-0h			R/W-0h	R/W-0h	R-0-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED		CLKDIV				CTRMODE	
R-0-0h		R/W-0h				R/W-2h	

Table 26-22. TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R-0	0h	Reserved
29-25	SYNCISEL	R/W	0h	These bits determines the source of SYNCIN signal. 0x0 : Disabled using SOC tieoff. 0x1-0x1F : Refer to PWM chapter of TRM. Reset type: SYSRSn
24-22	SYNCPERSEL	R/W	0h	Sync peripheral Select 000: Reserved (Disabled) 001: Reserved (Disabled) 010: CTR = PRD 011: CTR = 0 100: CTR = CMPC, Count direction Up 101: CTR = CMPC, Count direction Down 110: CTR = CMPD, Count direction Up 111: CTR = CMPD, Count direction Down Reset type: SYSRSn
21-20	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the time-base counter during emulation events 00: Stop after the next time-base counter increment or decrement 01: Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) - Up-down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) 1x: Free run Reset type: SYSRSn
19	RESERVED	R-0	0h	Reserved

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Table 26-22. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	SYNCOSEL	R/W	0h	Sync Output Select 000: SWFSYNC 001: CTR = zero: Time-base counter equal to zero (TBCTR = 0x00) 010: CTR = CMPC : Time-base counter equal to counter-compare C (TBCTR = CMPC) 011: CTR = CMPD : Time-base counter equal to counter-compare D (TBCTR = CMPD) 1xx: Disabled MCPWMxSYNCO sync signal Reset type: SYSRSn
15	SWSYNC	R-0/W1S	0h	Software Forced Sync Pulse 0: Writing a 0 has no effect and reads always return a 0. 1: Writing a 1 forces a one-time synchronization pulse to be generated. Reset type: SYSRSn
14-12	RESERVED	R-0	0h	Reserved
11	PHSDIR	R/W	0h	Phase Direction Bit. This bit is only used when the time-base counter is configured in the up-down-count mode. In the up-count mode, this bit is ignored. The bit indicates the direction of the time-base counter (TBCTR) after a sync event occurs and a new phase value is loaded from the phase (TBPHS) register. 0: Count down after the sync event. 1: Count up after the sync event. Reset type: SYSRSn
10	PHSEN	R/W	0h	Load Phase register to time-base counter(TBCNTR) 0: Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS). 1: Allow Counter to be loaded from the Phase register (TBPHS) when an MCPWMxSYNCI input signal occurs or a software-forced sync (SWSYNC). Reset type: SYSRSn
9	RESERVED	R-0	0h	Reserved
8	PRDLD	R/W	0h	Shadow to Active load of TBPRD register 0: Shadow to Active Load of TBPRD occurs when TBCTR = 0 1 : Disabled shadow to active load of TBPRD Reset type: SYSRSn
7-6	RESERVED	R-0	0h	Reserved

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Table 26-22. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value (TBCLK = MCPWMCLK/CLKDIV): 0000: /1 (default on reset) 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 1001: /512 1010: /1024 1011: /2048 1100: /4096 1101: /8192 1110: /16384 1111: /32768 Reset type: SYSRSn
1-0	CTRMODE	R/W	2h	The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00: Up-count mode 01: Up-down count mode 1x: Freeze counter operation (default on reset) Reset type: SYSRSn

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3 TBPRD Register (Offset = 14h) [Reset = 00000000h]

TBPRD is shown in Figure 26-40 and described in Table 26-21.

Return to the Summary Table.

Time base period register

Figure 26-40. TBPRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TBPRD															
R-0-0h																R/W-0h															

Table 26-24. TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	TBPRD	R/W	0h	Time Base Period Register These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. - If TBCTL[PRDLD] = 0, then the shadow is enabled. This register will also loaded from the shadow register when the time-base counter equals zero. - If TBCTL[PRDLD] = 1, then the shadow is disabled. Reset type: SYSRSn

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4 TBPRDS Register (Offset = 18h) [Reset = 00000000h]

TBPRDS is shown in Figure 26-41 and described in Table 26-22.

Return to the Summary Table.

Time base period shadow register

Figure 26-41. TBPRDS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TBPRDS															
R-0-0h																R/W-0h															

Table 26-26. TBPRDS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	TBPRDS	R/W	0h	Time Base Period Shadow Register The value in the TBPRDS register is loaded into TBPRD register when shadow to active load occurs. Reset type: SYSRSn

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5 TBPHS Register (Offset = 1Ch) [Reset = 00000000h]

TBPHS is shown in Figure 26-42 and described in Table 26-23.

Return to the Summary Table.

Time base phase offset register

Figure 26-42. TBPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TBPHS															
R-0-0h																R/W-0h															

Table 26-28. TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	TBPHS	R/W	0h	Phase Offset Register These bits set time-base counter phase of the PWM relative to the sync (MCPWMxSYNCI / SWFSYNC) - If TBCTL[PHSEN] = 0, then the sync event is ignored. - If TBCTL[PHSEN] = 1, then the time-base counter (TBCTR) will be loaded with the phase (TBPHS) when a sync event occurs. The sync event can be initiated by the input sync signal (MCPWMxSYNCI) or by a software forced sync. Reset type: SYSRSn

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6 TBSTS Register (Offset = 20h) [Reset = 00000000h]

TBSTS is shown in Figure 26-43 and described in Table 26-24.

Return to the Summary Table.

Time base status register

Figure 26-43. TBSTS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						SYNCI	CTRDIR
R-0-0h						R-0h	R-0h

Table 26-30. TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	SYNCI	R	0h	Input Synchronization Latched Status Bit 0: No external sync event has occurred. 1: External sync event has occurred (MCPWMxSYNCI). Reset type: SYSRSn
0	CTRDIR	R	0h	Time Base Counter Direction Status Bit 0: Time-Base Counter is currently counting up. 1: Time-Base Counter is currently counting down. Note: This bit is only valid when the counter is not frozen. Reset type: SYSRSn

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7 TBSTSCLR Register (Offset = 24h) [Reset = 00000000h]

TBSTSCLR is shown in Figure 26-44 and described in Table 26-25.

Return to the Summary Table.

Time base status clear register

Figure 26-44. TBSTSCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						SYNCI	RESERVED
R-0-0h						R-0/W1S-0h	R-0-0h

Table 26-32. TBSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	SYNCI	R-0/W1S	0h	Input Synchronization Latched Status Clear 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TBSTS[SYNCI] bit. Reset type: SYSRSn
0	RESERVED	R-0	0h	Reserved

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8 TBCTR Register (Offset = 28h) [Reset = 00000000h]

TBCTR is shown in Figure 26-45 and described in Table 26-26.

Return to the Summary Table.

Time base counter register

Figure 26-45. TBCTR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TBCTR															
R-0-0h																R/W-0h															

Table 26-34. TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	TBCTR	R/W	0h	Time Base Counter Register Reset type: SYSRSn

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9 CMPCTL Register (Offset = 30h) [Reset = 00000000h]

CMPCTL is shown in Figure 26-46 and described in Table 26-27.

Return to the Summary Table.

Counter compare control register

Figure 26-46. CMPCTL Register

31	30	29	28	27	26	25	24
RESERVED				LOADDMODE		LOADCMODE	
R-0-0h				R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RESERVED				PWM3_LOADBMODE		PWM3_LOADAMODE	
R-0-0h				R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PWM2_LOADBMODE		PWM2_LOADAMODE	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PWM1_LOADBMODE		PWM1_LOADAMODE	
R-0-0h				R/W-0h		R/W-0h	

Table 26-36. CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R-0	0h	Reserved
27-26	LOADDMODE	R/W	0h	Shadow to Active load of CMPD register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter CCM_CD_PRESENT = 1 Reset type: SYSRSn
25-24	LOADCMODE	R/W	0h	Shadow to Active load of CMPC register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter CCM_CD_PRESENT = 1 Reset type: SYSRSn
23-20	RESERVED	R-0	0h	Reserved

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Table 26-36. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-18	PWM3_LOADBMODE	R/W	0h	Shadow to Active load of PWM3_CMPB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM3_PRESENT = 1 Reset type: SYSRSn
17-16	PWM3_LOADAMODE	R/W	0h	Shadow to Active load of PWM3_CMPA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM3_PRESENT = 1 Reset type: SYSRSn
15-12	RESERVED	R-0	0h	Reserved
11-10	PWM2_LOADBMODE	R/W	0h	Shadow to Active load of PWM2_CMPB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM2_PRESENT = 1 Reset type: SYSRSn
9-8	PWM2_LOADAMODE	R/W	0h	Shadow to Active load of PWM2_CMPA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM2_PRESENT = 1 Reset type: SYSRSn
7-4	RESERVED	R-0	0h	Reserved
3-2	PWM1_LOADBMODE	R/W	0h	Shadow to Active load of PWM1_CMPB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn

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Table 26-36. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PWM1_LOADAMODE	R/W	0h	Shadow to Active load of PWM1_CMPA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn

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10 CMPC Register (Offset = 40h) [Reset = 00000000h]

CMPC is shown in Figure 26-47 and described in Table 26-28.

Return to the Summary Table.

Counter compare C register

Figure 26-47. CMPC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMPC															
R-0-0h																R/W-0h															

Table 26-38. CMPC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	CMPC	R/W	0h	Compare C register The value in the CMPC register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare C' event. Shadowing of this register is enabled and disabled by the CMPCTL[LOADCMODE] field. By default this register is shadowed. Reset type: SYSRSn

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11 CMPD Register (Offset = 44h) [Reset = 00000000h]

CMPD is shown in Figure 26-48 and described in Table 26-29.

Return to the Summary Table.

Counter compare D register

Figure 26-48. CMPD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMPD															
R-0-0h																R/W-0h															

Table 26-40. CMPD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	CMPD	R/W	0h	Compare D register The value in the CMPD register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a 'time-base counter equal to counter compare D' event. Shadowing of this register is enabled and disabled by the CMPCTL[LOADDMODE] field. By default this register is shadowed. Reset type: SYSRSn

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12 CMPCS Register (Offset = 48h) [Reset = 00000000h]

CMPCS is shown in Figure 26-49 and described in Table 26-30.

Return to the Summary Table.

Counter compare C shadow register

Figure 26-49. CMPCS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMPCS															
R-0-0h																R/W-0h															

Table 26-42. CMPCS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	CMPCS	R/W	0h	Compare C Shadow Register The value in the CMPCS register is loaded into CMPC register when shadow to active load occurs. Reset type: SYSRSn

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13 CMPDS Register (Offset = 4Ch) [Reset = 00000000h]

CMPDS is shown in Figure 26-50 and described in Table 26-31.

Return to the Summary Table.

Counter compare D shadow register

Figure 26-50. CMPDS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMPDS															
R-0-0h																R/W-0h															

Table 26-44. CMPDS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	CMPDS	R/W	0h	Compare D Shadow Register The value in the CMPDS register is loaded into CMPD register when shadow to active load occurs. Reset type: SYSRSn

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14 AQCTL Register (Offset = 50h) [Reset = 00000000h]

AQCTL is shown in Figure 26-51 and described in Table 26-32.

Return to the Summary Table.

Action qualifier control register

Figure 26-51. AQCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED				PWM3_LDAQBMODE		PWM3_LDAQAMODE	
R-0-0h				R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PWM2_LDAQBMODE		PWM2_LDAQAMODE	
R-0-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PWM1_LDAQBMODE		PWM1_LDAQAMODE	
R-0-0h				R/W-0h		R/W-0h	

Table 26-46. AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R-0	0h	Reserved
19-18	PWM3_LDAQBMODE	R/W	0h	Shadow to Active load of PWM3_AQCTLB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM3_PRESENT = 1 Reset type: SYSRSn
17-16	PWM3_LDAQAMODE	R/W	0h	Shadow to Active load of PWM3_AQCTLA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM3_PRESENT = 1 Reset type: SYSRSn
15-12	RESERVED	R-0	0h	Reserved

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Table 26-46. AQCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	PWM2_LDAQBMODE	R/W	0h	Shadow to Active load of PWM2_AQCTLB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM2_PRESENT = 1 Reset type: SYSRSn
9-8	PWM2_LDAQAMODE	R/W	0h	Shadow to Active load of PWM2_AQCTLA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: This field can be present only when the configuration parameter PWM2_PRESENT = 1 Reset type: SYSRSn
7-4	RESERVED	R-0	0h	Reserved
3-2	PWM1_LDAQBMODE	R/W	0h	Shadow to Active load of PWM1_AQCTLB register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn
1-0	PWM1_LDAQAMODE	R/W	0h	Shadow to Active load of PWM1_AQCTLA register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn

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15 SOCEN Register (Offset = 60h) [Reset = 00000000h]

SOCEN is shown in Figure 26-52 and described in Table 26-33.

Return to the Summary Table.

Start of conversion enable

Figure 26-52. SOCEN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCD_ENABLE	SOCC_ENABLE	SOCB_ENABLE	SOCA_ENABLE
R-0-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 26-48. SOCEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3	SOCD_ENABLE	R/W	0h	SOCD Selection Enable 0 - SOCD disable 1- SOCD enable Reset type: SYSRSn
2	SOCC_ENABLE	R/W	0h	SOCC Selection Enable 0 - SOCC disable 1- SOCC enable Reset type: SYSRSn
1	SOCB_ENABLE	R/W	0h	SOCB Selection Enable 0 - SOCB disable 1- SOCB enable Reset type: SYSRSn
0	SOCA_ENABLE	R/W	0h	SOCA Selection Enable 0 - SOCA disable 1- SOCA enable Reset type: SYSRSn

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16 SOCSEL Register (Offset = 64h) [Reset = 00000000h]

SOCSEL is shown in Figure 26-53 and described in Table 26-34.

Return to the Summary Table.

Start of conversion selection

Figure 26-53. SOCSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			SOCD_SEL					RESERVED			SOCC_SEL				
R-0-0h			R/W-0h					R-0-0h			R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			SOCB_SEL					RESERVED			SOCA_SEL				
R-0-0h			R/W-0h					R-0-0h			R/W-0h				

Table 26-50. SOCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R-0	0h	Reserved

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Table 26-50. SOCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	SOCD_SEL	R/W	0h	SOCD Selection Options These bits determine when SOCD pulse will be generated. 00000: Reserved (SOC D disabled) 00001: Reserved (SOC D disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (SOC D disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (SOC D disabled) Reset type: SYSRSn
23-21	RESERVED	R-0	0h	Reserved

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Table 26-50. SOCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	SOCC_SEL	R/W	0h	SOCC Selection Options These bits determine when SOCC pulse will be generated. 00000: Reserved (SOC C disabled) 00001: Reserved (SOC C disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (SOC C disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (SOC C disabled) Reset type: SYSRSn
15-13	RESERVED	R-0	0h	Reserved

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Table 26-50. SOCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	SOCB_SEL	R/W	0h	SOCB Selection Options These bits determine when SOCB pulse will be generated. 00000: Reserved (SOC B disabled) 00001: Reserved (SOC B disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (SOC B disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (SOC B disabled) Reset type: SYSRSn
7-5	RESERVED	R-0	0h	Reserved

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Table 26-50. SOCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	SOCA_SEL	R/W	0h	SOCA Selection Options These bits determine when SOCA pulse will be generated. 00000: Reserved (SOC A disabled) 00001: Reserved (SOC A disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (SOC A disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (SOC A disabled) Reset type: SYSRSn

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17 SOCPERIOD Register (Offset = 68h) [Reset = 00000000h]

SOCPERIOD is shown in Figure 26-54 and described in Table 26-35.

Return to the Summary Table.

Start of conversion period

Figure 26-54. SOCPERIOD Register

31	30	29	28	27	26	25	24
RESERVED					SOCD_PERIOD		
R-0-0h					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					SOCC_PERIOD		
R-0-0h					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED					SOCB_PERIOD		
R-0-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					SOCA_PERIOD		
R-0-0h					R/W-0h		

Table 26-52. SOCPERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R-0	0h	Reserved
26-24	SOCD_PERIOD	R/W	0h	SOCD Period These bits determine how many selected SOCSEL[SOCD_SEL] events need to occur before an SOCD pulse is generated. To be generated, the pulse must be enabled (SOCEN[SOCD_ENABLE] = 1). The SOCD pulse will be generated even if the status flag is set from a previous start of conversion (SOCFLAG[SOCD] = 1). Once the SOCD pulse is generated, the SOCCNT[SOCD_CNT] bits will automatically be cleared. Reset type: SYSRSn
23-19	RESERVED	R-0	0h	Reserved
18-16	SOCC_PERIOD	R/W	0h	SOCC Period These bits determine how many selected SOCSEL[SOCC_SEL] events need to occur before an SOCC pulse is generated. To be generated, the pulse must be enabled (SOCEN[SOCC_ENABLE] = 1). The SOCC pulse will be generated even if the status flag is set from a previous start of conversion (SOCFLAG[SOCC] = 1). Once the SOCC pulse is generated, the SOCCNT[SOCC_CNT] bits will automatically be cleared. Reset type: SYSRSn
15-11	RESERVED	R-0	0h	Reserved
10-8	SOCB_PERIOD	R/W	0h	SOCB Period These bits determine how many selected SOCSEL[SOCB_SEL] events need to occur before an SOCB pulse is generated. To be generated, the pulse must be enabled (SOCEN[SOCB_ENABLE] = 1). The SOCB pulse will be generated even if the status flag is set from a previous start of conversion (SOCFLAG[SOCB] = 1). Once the SOCB pulse is generated, the SOCCNT[SOCB_CNT] bits will automatically be cleared. Reset type: SYSRSn

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Table 26-52. SOCPERIOD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	SOCA_PERIOD	R/W	0h	SOCA Period These bits determine how many selected SOCSEL[SOCA_SEL] events need to occur before an SOCA pulse is generated. To be generated, the pulse must be enabled (SOCEN[SOCA_ENABLE] = 1). The SOCA pulse will be generated even if the status flag is set from a previous start of conversion (SOCFLAG[SOCA] = 1). Once the SOCA pulse is generated, the SOCCNT[SOCA_CNT] bits will automatically be cleared. Reset type: SYSRSn

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18 SOCCNT Register (Offset = 6Ch) [Reset = 00000000h]

SOCCNT is shown in Figure 26-55 and described in Table 26-36.

Return to the Summary Table.

Start of conversion count

Figure 26-55. SOCCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					SOCD_CNT			RESERVED					SOCC_CNT		
R-0-0h					R-0h			R-0-0h					R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SOCB_CNT			RESERVED					SOCA_CNT		
R-0-0h					R-0h			R-0-0h					R-0h		

Table 26-54. SOCCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R-0	0h	Reserved
26-24	SOCD_CNT	R	0h	SOC D Counter Register These bits indicate how many selected SOCSEL[SOCD_SEL] events have occurred. These bits are automatically cleared when a SOCD pulse is generated. Reset type: SYSRSn
23-19	RESERVED	R-0	0h	Reserved
18-16	SOCC_CNT	R	0h	SOC C Counter Register These bits indicate how many selected SOCSEL[SOCC_SEL] events have occurred. These bits are automatically cleared when a SOCC pulse is generated. Reset type: SYSRSn
15-11	RESERVED	R-0	0h	Reserved
10-8	SOCB_CNT	R	0h	SOC B Counter Register These bits indicate how many selected SOCSEL[SOCB_SEL] events have occurred. These bits are automatically cleared when a SOCB pulse is generated. Reset type: SYSRSn
7-3	RESERVED	R-0	0h	Reserved
2-0	SOCA_CNT	R	0h	SOC A Counter Register These bits indicate how many selected SOCSEL[SOCA_SEL] events have occurred. These bits are automatically cleared when a SOCA pulse is generated. Reset type: SYSRSn

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19 SOCFLAG Register (Offset = 70h) [Reset = 00000000h]

SOCFLAG is shown in Figure 26-56 and described in Table 26-37.

Return to the Summary Table.

Start of conversion flag

Figure 26-56. SOCFLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCD	SOCC	SOCB	SOCA
R-0-0h				R-0h	R-0h	R-0h	R-0h

Table 26-56. SOCFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3	SOCD	R	0h	Latched SOC D Status Flag SOCD output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on SOCD. The SOCD output will continue to be generated even if the flag bit is set. Reset type: SYSRSn
2	SOCC	R	0h	Latched SOC C Status Flag SOCC output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on SOCC. The SOCC output will continue to be generated even if the flag bit is set. Reset type: SYSRSn
1	SOCB	R	0h	Latched SOC B Status Flag SOCB output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on SOCB. The SOCB output will continue to be generated even if the flag bit is set. Reset type: SYSRSn
0	SOCA	R	0h	Latched SOC A Status Flag SOCA output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on SOCA. The SOCA output will continue to be generated even if the flag bit is set. Reset type: SYSRSn

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20 SOCCLR Register (Offset = 74h) [Reset = 00000000h]

SOCCLR is shown in Figure 26-57 and described in Table 26-38.

Return to the Summary Table.

Start of conversion clear

Figure 26-57. SOCCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED				SOCD	SOCC	SOCB	SOCA
R-0-0h				R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 26-58. SOCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R-0	0h	Reserved
3	SOCD	R-0/W1S	0h	Clear SOC D Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the SOCFLAG[SOCD] bit. Reset type: SYSRSn
2	SOCC	R-0/W1S	0h	Clear SOC C Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the SOCFLAG[SOCC] bit. Reset type: SYSRSn
1	SOCB	R-0/W1S	0h	Clear SOC B Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the SOCFLAG[SOCB] bit. Reset type: SYSRSn
0	SOCA	R-0/W1S	0h	Clear SOC A Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the SOCFLAG[SOCA] bit. Reset type: SYSRSn

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21 ETSEL Register (Offset = 80h) [Reset = 00000000h]

ETSEL is shown in Figure 26-58 and described in Table 26-39.

Return to the Summary Table.

Event trigger selection

Figure 26-58. ETSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ET2_SEL					RESERVED			ET1_SEL				
R-0-0h			R/W-0h					R-0-0h			R/W-0h				

Table 26-60. ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R-0	0h	Reserved

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Table 26-60. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ET2_SEL	R/W	0h	Event trigger2 Selection Options These bits determine when event trigger pulse will be generated. 00000: Reserved (ET2 Disabled) 00001: Reserved (ET2 Disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (ET2 Disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (ET2 Disabled) Reset type: SYSRSn
7-5	RESERVED	R-0	0h	Reserved

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Table 26-60. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	ET1_SEL	R/W	0h	Event trigger1 Selection Options These bits determine when event trigger pulse will be generated. 00000: Reserved (ET1 Disabled) 00001: Reserved (ET1 Disabled) 00010: Enable event time-base counter equal to zero (TBCTR = 0x0000) 00011: Enable event time-base counter equal to period (TBCTR = TBPRD) 00100: Enable event time-base counter equal to zero or period (TBCTR = 0x00 or TBCTR = TBPRD) 00101 - 00111: Reserved (ET1 Disabled) 01000: Enable event time-base counter equal to CMPC when the timer is incrementing 01001: Enable event time-base counter equal to CMPD when the timer is incrementing 01010: Enable event time-base counter equal to PWM1_CMPA when the timer is incrementing 01011: Enable event time-base counter equal to PWM1_CMPB when the timer is incrementing 01100: Enable event time-base counter equal to PWM2_CMPA when the timer is incrementing 01101: Enable event time-base counter equal to PWM2_CMPB when the timer is incrementing 01110: Enable event time-base counter equal to PWM3_CMPA when the timer is incrementing 01111: Enable event time-base counter equal to PWM3_CMPB when the timer is incrementing 10000: Enable event time-base counter equal to CMPC when the timer is decrementing 10001: Enable event time-base counter equal to CMPD when the timer is decrementing 10010: Enable event time-base counter equal to PWM1_CMPA when the timer is decrementing 10011: Enable event time-base counter equal to PWM1_CMPB when the timer is decrementing 10100: Enable event time-base counter equal to PWM2_CMPA when the timer is decrementing 10101: Enable event time-base counter equal to PWM2_CMPB when the timer is decrementing 10110: Enable event time-base counter equal to PWM3_CMPA when the timer is decrementing 10111: Enable event time-base counter equal to PWM3_CMPB when the timer is decrementing 11000 - 11111: Reserved (ET1 Disabled) Reset type: SYSRSn

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22 ETPERIOD Register (Offset = 84h) [Reset = 00000000h]

ETPERIOD is shown in Figure 26-59 and described in Table 26-40.

Return to the Summary Table.

Event trigger period

Figure 26-59. ETPERIOD Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED					ET2_PERIOD		
R-0-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					ET1_PERIOD		
R-0-0h					R/W-0h		

Table 26-62. ETPERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R-0	0h	Reserved
10-8	ET2_PERIOD	R/W	0h	These bits determine how many selected ETSEL[ET2_SEL] events need to occur before an interrupt is generated. If the interrupt status flag is set from a previous interrupt (INTFLG[ET2] = 1) then no interrupt will be generated until the flag is cleared via the INTCLR[ET2] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETCNT[ET2_CNT] bits will automatically be cleared. Writing a PERIOD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a PERIOD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero PERIOD value is written, the counter is incremented. Reset type: SYSRSn
7-3	RESERVED	R-0	0h	Reserved
2-0	ET1_PERIOD	R/W	0h	These bits determine how many selected ETSEL[ET1_SEL] events need to occur before an interrupt is generated. If the interrupt status flag is set from a previous interrupt (INTFLG[ET1] = 1) then no interrupt will be generated until the flag is cleared via the INTCLR[ET1] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETCNT[ET1_CNT] bits will automatically be cleared. Writing a PERIOD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a PERIOD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero PERIOD value is written, the counter is incremented. Reset type: SYSRSn

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23 ETCNT Register (Offset = 88h) [Reset = 00000000h]

ETCNT is shown in Figure 26-60 and described in Table 26-41.

Return to the Summary Table.

Event trigger count

Figure 26-60. ETCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ET2_CNT			RESERVED					ET1_CNT		
R-0-0h					R-0h			R-0-0h					R-0h		

Table 26-64. ETCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R-0	0h	Reserved
10-8	ET2_CNT	R	0h	Event trigger2 Counter Register These bits indicate how many selected ET_SEL[ET2_SEL] events have occurred. These bits are automatically cleared once INTFLAG.ET2 is generated (irrespective of INTEN.ET2 configuration). Reset type: SYSRSn
7-3	RESERVED	R-0	0h	Reserved
2-0	ET1_CNT	R	0h	Event trigger1 Counter Register These bits indicate how many selected ET_SEL[ET1_SEL] events have occurred. These bits are automatically cleared once INTFLAG.ET1 is generated (irrespective of INTEN.ET1 configuration). Reset type: SYSRSn

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24 INTEN Register (Offset = 90h) [Reset = 00000000h]

INTEN is shown in Figure 26-61 and described in Table 26-42.

Return to the Summary Table.

Interrupt Enable Register

Figure 26-61. INTEN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CNT_OVF	ET2	ET1	OST	CBC	RESERVED
R-0-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 26-66. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	CNT_OVF	R/W	0h	Counter Overflow Interrupt Enable 1 : Enables CNT_OVF interrupt 0 : Disable CNT_OVF interrupt Reset type: SYSRSn
4	ET2	R/W	0h	Event Trigger 2 Interrupt Enable 1 : Enables ET2 interrupt 0 : Disable ET2 interrupt Reset type: SYSRSn
3	ET1	R/W	0h	Event Trigger 1 Interrupt Enable 1 : Enables ET1 interrupt 0 : Disable ET1 interrupt Reset type: SYSRSn
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 1 : Enables OST interrupt 0 : Disable OST interrupt Reset type: SYSRSn
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 1 : Enables CBC interrupt 0 : Disable CBC interrupt Reset type: SYSRSn
0	RESERVED	R	0h	Reserved

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25 INTFLAG Register (Offset = 94h) [Reset = 00000000h]

INTFLAG is shown in Figure 26-62 and described in Table 26-43.

Return to the Summary Table.

Interrupt Flag Register

Figure 26-62. INTFLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CNT_OVF	ET2	ET1	OST	CBC	INT
R-0-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 26-68. INTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	CNT_OVF	R	0h	Latched Status Flag for A Counter Overflow Event 1 : CNT_OVF flag is set 0 : CNT_OVF flag is not set Reset type: SYSRSn
4	ET2	R	0h	Latched Status Flag for A Event Trigger 2 Event 1: ET2 flag is set 0: ET2 flag is not set Reset type: SYSRSn
3	ET1	R	0h	Latched Status Flag for A Event Trigger 1 Event 1: ET1 flag is set 0: ET1 flag is not set Reset type: SYSRSn
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 1: OST flag is set 0: OST flag is not set Reset type: SYSRSn
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 1: CBC flag is set 0: CBC flag is not set Reset type: SYSRSn
0	INT	R	0h	Global Interrupt Status Flag 1: Global flag is set 0: Global flag is not set Reset type: SYSRSn

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26 INTCLR Register (Offset = 98h) [Reset = 00000000h]

INTCLR is shown in Figure 26-63 and described in Table 26-44.

Return to the Summary Table.

Interrupt Clear Register

Figure 26-63. INTCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CNT_OVF	ET2	ET1	OST	CBC	INT
R-0-0h		R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 26-70. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	CNT_OVF	R-0/W1S	0h	Clear Counter Overflow Flag Writing '1' will clear INTFLAG[CNT_OVF] register. Reset type: SYSRSn
4	ET2	R-0/W1S	0h	Clear Event Trigger 2 Flag Writing '1' will clear INTFLAG[ET2] register. Reset type: SYSRSn
3	ET1	R-0/W1S	0h	Clear Event Trigger 1 Flag Writing '1' will clear INTFLAG[ET1] register. Reset type: SYSRSn
2	OST	R-0/W1S	0h	Clear One-Shot Trip Latch Writing '1' will clear INTFLAG[OST] register. Reset type: SYSRSn
1	CBC	R-0/W1S	0h	Clear Cycle-by-Cycle Trip Latch Writing '1' will clear INTFLAG[CBC] register. Reset type: SYSRSn
0	INT	R-0/W1S	0h	Clear Global Interrupt Flag Writing '1' will clear INTFLAG[INT] register. Reset type: SYSRSn

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27 INTFRC Register (Offset = 9Ch) [Reset = 00000000h]

INTFRC is shown in Figure 26-64 and described in Table 26-45.

Return to the Summary Table.

Interrupt Force Register

Figure 26-64. INTFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CNT_OVF	ET2	ET1	OST	CBC	RESERVED
R-0-0h		R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0h

Table 26-72. INTFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	CNT_OVF	R-0/W1S	0h	Force Counter Overflow Interrupt Writing '1' will set INTFLAG[CNT_OVF] register. Reset type: SYSRSn
4	ET2	R-0/W1S	0h	Force Event Trigger 2 Interrupt Writing '1' will set INTFLAG[ET2] register. Reset type: SYSRSn
3	ET1	R-0/W1S	0h	Force Event Trigger 1 Interrupt Writing '1' will set INTFLAG[ET1] register. Reset type: SYSRSn
2	OST	R-0/W1S	0h	Force One-Shot Trip Interrupt Writing '1' will set INTFLAG[OST] register. Reset type: SYSRSn
1	CBC	R-0/W1S	0h	Force Cycle-by-Cycle Trip Interrupt Writing '1' will set INTFLAG[CBC] register. Reset type: SYSRSn
0	RESERVED	R	0h	Reserved

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28 TZSEL Register (Offset = A0h) [Reset = 00000000h]

TZSEL is shown in Figure 26-65 and described in Table 26-46.

Return to the Summary Table.

Trip Zone Selection

Figure 26-65. TZSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
OST8	OST7	OST6	OST5	OST4	OST3	OST2	OST1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
CBC8	CBC7	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 26-74. TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R-0	0h	Reserved
23	OST8	R/W	0h	Select Trip-zone 8 (TZ8) for OST generation 0: Disable TZ8 as a OST trip source for this MCPWM module 1: Enable TZ8 as a OST trip source for this MCPWM module Reset type: SYSRSn
22	OST7	R/W	0h	Select Trip-zone 7 (TZ7) for OST generation 0: Disable TZ7 as a OST trip source for this MCPWM module 1: Enable TZ7 as a OST trip source for this MCPWM module Reset type: SYSRSn
21	OST6	R/W	0h	Select Trip-zone 6 (TZ6) for OST generation 0: Disable TZ6 as a OST trip source for this MCPWM module 1: Enable TZ6 as a OST trip source for this MCPWM module Reset type: SYSRSn
20	OST5	R/W	0h	Select Trip-zone 5 (TZ5) for OST generation 0: Disable TZ5 as a OST trip source for this MCPWM module 1: Enable TZ5 as a OST trip source for this MCPWM module Reset type: SYSRSn
19	OST4	R/W	0h	Select Trip-zone 4 (TZ4) for OST generation 0: Disable TZ4 as a OST trip source for this MCPWM module 1: Enable TZ4 as a OST trip source for this MCPWM module Reset type: SYSRSn
18	OST3	R/W	0h	Select Trip-zone 3 (TZ3) for OST generation 0: Disable TZ3 as a OST trip source for this MCPWM module 1: Enable TZ3 as a OST trip source for this MCPWM module Reset type: SYSRSn

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Table 26-74. TZSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OST2	R/W	0h	Select Trip-zone 2 (TZ2) for OST generation 0: Disable TZ2 as a OST trip source for this MCPWM module 1: Enable TZ2 as a OST trip source for this MCPWM module Reset type: SYSRSn
16	OST1	R/W	0h	Select Trip-zone 1 (TZ1) for OST generation 0: Disable TZ1 as a OST trip source for this MCPWM module 1: Enable TZ1 as a OST trip source for this MCPWM module Reset type: SYSRSn
15-8	RESERVED	R-0	0h	Reserved
7	CBC8	R/W	0h	Select Trip-zone 8 (TZ8) for CBC generation 0: Disable TZ8 as a CBC trip source for this MCPWM module 1: Enable TZ8 as a CBC trip source for this MCPWM module Reset type: SYSRSn
6	CBC7	R/W	0h	Select Trip-zone 7 (TZ7) for CBC generation 0: Disable TZ7 as a CBC trip source for this MCPWM module 1: Enable TZ7 as a CBC trip source for this MCPWM module Reset type: SYSRSn
5	CBC6	R/W	0h	Select Trip-zone 6 (TZ6) for CBC generation 0: Disable TZ6 as a CBC trip source for this MCPWM module 1: Enable TZ6 as a CBC trip source for this MCPWM module Reset type: SYSRSn
4	CBC5	R/W	0h	Select Trip-zone 5 (TZ5) for CBC generation 0: Disable TZ5 as a CBC trip source for this MCPWM module 1: Enable TZ5 as a CBC trip source for this MCPWM module Reset type: SYSRSn
3	CBC4	R/W	0h	Select Trip-zone 4 (TZ4) for CBC generation 0: Disable TZ4 as a CBC trip source for this MCPWM module 1: Enable TZ4 as a CBC trip source for this MCPWM module Reset type: SYSRSn
2	CBC3	R/W	0h	Select Trip-zone 3 (TZ3) for CBC generation 0: Disable TZ3 as a CBC trip source for this MCPWM module 1: Enable TZ3 as a CBC trip source for this MCPWM module Reset type: SYSRSn
1	CBC2	R/W	0h	Select Trip-zone 2 (TZ2) for CBC generation 0: Disable TZ2 as a CBC trip source for this MCPWM module 1: Enable TZ2 as a CBC trip source for this MCPWM module Reset type: SYSRSn
0	CBC1	R/W	0h	Select Trip-zone 1 (TZ1) for CBC generation 0: Disable TZ1 as a CBC trip source for this MCPWM module 1: Enable TZ1 as a CBC trip source for this MCPWM module Reset type: SYSRSn

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29 TZCTL Register (Offset = ACh) [Reset = 00000010h]

TZCTL is shown in Figure 26-66 and described in Table 26-47.

Return to the Summary Table.

Trip Zone control

Figure 26-66. TZCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		CBCPULSE		TZB		TZA	
R-0-0h		R/W-1h		R/W-0h		R/W-0h	

Table 26-76. TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5-4	CBCPULSE	R/W	1h	Clear Pulse for Cycle-By-Cycle (CBC) Trip Latch This bit field determines which pulse clears the CBC trip latch. 00: CBC trip latch is not cleared 01: CTR = ZERO pulse clears CBC trip latch 10: CTR = PRD pulse clears CBC trip latch 11: CTR = ZERO or CTR = PRD pulse clears CBC trip latch Reset type: SYSRSn
3-2	TZB	R/W	0h	Trip action on PWMxB 00: High-impedance (PWMxB = High-impedance state) 01: Force PWMxB to a high state 10: Force PWMxB to a low state 11: Do nothing, no action is taken on PWMxB. Reset type: SYSRSn
1-0	TZA	R/W	0h	Trip action on PWMxA 00: High-impedance (PWMxA = High-impedance state) 01: Force PWMxA to a high state 10: Force PWMxA to a low state 11: Do nothing, no action is taken on PWMxA. Reset type: SYSRSn

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30 TZCBCOSTFLAG Register (Offset = B0h) [Reset = 00000000h]

TZCBCOSTFLAG is shown in Figure 26-67 and described in Table 26-48.

Return to the Summary Table.

Trip Zone CBC and OST Flag Register

Figure 26-67. TZCBCOSTFLAG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
OST8	OST7	OST6	OST5	OST4	OST3	OST2	OST1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
CBC8	CBC7	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 26-78. TZCBCOSTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R-0	0h	Reserved
23	OST8	R	0h	Latched Status Flag for OST TZ8 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ8. 1: Reading a 1 indicates a OST trip has occured by TZ8. Reset type: SYSRSn
22	OST7	R	0h	Latched Status Flag for OST TZ7 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ7. 1: Reading a 1 indicates a OST trip has occured by TZ7. Reset type: SYSRSn
21	OST6	R	0h	Latched Status Flag for OST TZ6 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ6. 1: Reading a 1 indicates a OST trip has occured by TZ6. Reset type: SYSRSn
20	OST5	R	0h	Latched Status Flag for OST TZ5 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ5. 1: Reading a 1 indicates a OST trip has occured by TZ5. Reset type: SYSRSn
19	OST4	R	0h	Latched Status Flag for OST TZ4 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ4. 1: Reading a 1 indicates a OST trip has occured by TZ4. Reset type: SYSRSn
18	OST3	R	0h	Latched Status Flag for OST TZ3 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ3. 1: Reading a 1 indicates a OST trip has occured by TZ3. Reset type: SYSRSn

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Table 26-78. TZCBCOSTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OST2	R	0h	Latched Status Flag for OST TZ2 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ2. 1: Reading a 1 indicates a OST trip has occured by TZ2. Reset type: SYSRSn
16	OST1	R	0h	Latched Status Flag for OST TZ1 Trip Latch 0: Reading a 0 indicates that no OST trip has occurred by TZ1. 1: Reading a 1 indicates a OST trip has occured by TZ1. Reset type: SYSRSn
15-8	RESERVED	R-0	0h	Reserved
7	CBC8	R	0h	Latched Status Flag for CBC TZ8 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ8. 1: Reading a 1 indicates a CBC trip has occured by TZ8. Reset type: SYSRSn
6	CBC7	R	0h	Latched Status Flag for CBC TZ7 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ7. 1: Reading a 1 indicates a CBC trip has occured by TZ7. Reset type: SYSRSn
5	CBC6	R	0h	Latched Status Flag for CBC TZ6 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ6. 1: Reading a 1 indicates a CBC trip has occured by TZ6. Reset type: SYSRSn
4	CBC5	R	0h	Latched Status Flag for CBC TZ5 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ5. 1: Reading a 1 indicates a CBC trip has occured by TZ5. Reset type: SYSRSn
3	CBC4	R	0h	Latched Status Flag for CBC TZ4 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ4. 1: Reading a 1 indicates a CBC trip has occured by TZ4. Reset type: SYSRSn
2	CBC3	R	0h	Latched Status Flag for CBC TZ3 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ3. 1: Reading a 1 indicates a CBC trip has occured by TZ3. Reset type: SYSRSn
1	CBC2	R	0h	Latched Status Flag for CBC TZ2 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ2. 1: Reading a 1 indicates a CBC trip has occured by TZ2. Reset type: SYSRSn
0	CBC1	R	0h	Latched Status Flag for CBC TZ1 Trip Latch 0: Reading a 0 indicates that no CBC trip has occurred by TZ1. 1: Reading a 1 indicates a CBC trip has occured by TZ1. Reset type: SYSRSn

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31 TZCBCOSTCLR Register (Offset = B4h) [Reset = 00000000h]

TZCBCOSTCLR is shown in Figure 26-68 and described in Table 26-49.

Return to the Summary Table.

Trip Zone CBC and OST Clear Register

Figure 26-68. TZCBCOSTCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
OST8	OST7	OST6	OST5	OST4	OST3	OST2	OST1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
CBC8	CBC7	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 26-80. TZCBCOSTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R-0	0h	Reserved
23	OST8	R-0/W1S	0h	Clear OST TZ8 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST8] bit. Reset type: SYSRSn
22	OST7	R-0/W1S	0h	Clear OST TZ7 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST7] bit. Reset type: SYSRSn
21	OST6	R-0/W1S	0h	Clear OST TZ6 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST6] bit. Reset type: SYSRSn
20	OST5	R-0/W1S	0h	Clear OST TZ5 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST5] bit. Reset type: SYSRSn
19	OST4	R-0/W1S	0h	Clear OST TZ4 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST4] bit. Reset type: SYSRSn
18	OST3	R-0/W1S	0h	Clear OST TZ3 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST3] bit. Reset type: SYSRSn

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Table 26-80. TZCBCOSTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OST2	R-0/W1S	0h	Clear OST TZ2 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST2] bit. Reset type: SYSRSn
16	OST1	R-0/W1S	0h	Clear OST TZ1 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[OST1] bit. Reset type: SYSRSn
15-8	RESERVED	R-0	0h	Reserved
7	CBC8	R-0/W1S	0h	Clear CBC TZ8 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC8] bit. Reset type: SYSRSn
6	CBC7	R-0/W1S	0h	Clear CBC TZ7 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC7] bit. Reset type: SYSRSn
5	CBC6	R-0/W1S	0h	Clear CBC TZ6 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC6] bit. Reset type: SYSRSn
4	CBC5	R-0/W1S	0h	Clear CBC TZ5 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC5] bit. Reset type: SYSRSn
3	CBC4	R-0/W1S	0h	Clear CBC TZ4 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC4] bit. Reset type: SYSRSn
2	CBC3	R-0/W1S	0h	Clear CBC TZ3 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC3] bit. Reset type: SYSRSn
1	CBC2	R-0/W1S	0h	Clear CBC TZ2 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC2] bit. Reset type: SYSRSn
0	CBC1	R-0/W1S	0h	Clear CBC TZ1 Status Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCOSTFLAG[CBC1] bit. Reset type: SYSRSn

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32 DBCTL Register (Offset = C0h) [Reset = 00000000h]

DBCTL is shown in Figure 26-69 and described in Table 26-50.

Return to the Summary Table.

Dead band control register

Figure 26-69. DBCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED				LOADREDMODE		LOADFEDMODE	
R-0-0h				R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							DEDB_MODE
R-0-0h							R/W-0h
7	6	5	4	3	2	1	0
OUTSWAP		IN_MODE		POLSEL		OUT_MODE	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-82. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R-0	0h	Reserved
19-18	LOADREDMODE	R/W	0h	Shadow to Active load of DBRED register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn
17-16	LOADFEDMODE	R/W	0h	Shadow to Active load of DBFED register 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Reset type: SYSRSn
15-9	RESERVED	R-0	0h	Reserved
8	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control (S8 switch) 0: Rising edge delay applied to InA/InB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch (INMODE bits) on B signal path only. 1: Rising edge delay and falling edge delay applied to source selected by S4 switch (INMODE bits) and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid. Reset type: SYSRSn

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Table 26-82. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 7 controls the S6 switch and bit 6 controls the S7 switch. 00: OutA and OutB signals are as defined by OUT-MODE bits. 01: OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). 10: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = B-path as defined by OUT-MODE bits. 11: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). Reset type: SYSRSn
5-4	IN_MODE	R/W	0h	Dead-Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is PWMxA In is the source for both falling and rising-edge delays. 00: PWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay. 01: PWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. PWMxA In (from the action-qualifier) is the source for falling-edge delayed signal. 10: PWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. PWMxB In (from the action-qualifier) is the source for falling-edge delayed signal. 11: PWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal. Reset type: SYSRSn
3-2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes. 00: Active high (AH) mode. Neither PWMxA nor PWMxB is inverted (default). 01: Active low complementary (ALC) mode. PWMxA is inverted. 10: Active high complementary (AHC). PWMxB is inverted. 11: Active low (AL) mode. Both PWMxA and PWMxB are inverted. Reset type: SYSRSn
1-0	OUT_MODE	R/W	0h	Dead-Band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch. 00: DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect. 01: Apath = InA (delay is by-passed for A signal path) Bpath = FED (Falling Edge Delay in B signal path) 10: Apath = RED (Rising Edge Delay in A signal path) Bpath = InB (delay is by-passed for B signal path) 11: DBM is fully enabled (i.e. both RED and FED active) Reset type: SYSRSn

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33 DBFED Register (Offset = D0h) [Reset = 00000000h]

DBFED is shown in Figure 26-70 and described in Table 26-51.

Return to the Summary Table.

Dead band fall edge delay

Figure 26-70. DBFED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DBFED													
R-0-0h																		R/W-0h													

Table 26-84. DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R-0	0h	Reserved
13-0	DBFED	R/W	0h	Falling Edge Delay Count 14-bit counter Reset type: SYSRSn

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34 DBRED Register (Offset = D4h) [Reset = 00000000h]

DBRED is shown in Figure 26-71 and described in Table 26-52.

Return to the Summary Table.

Dead band rise edge delay

Figure 26-71. DBRED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DBRED													
R-0-0h																		R/W-0h													

Table 26-86. DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R-0	0h	Reserved
13-0	DBRED	R/W	0h	Rising Edge Delay Count 14-bit counter Reset type: SYSRSn

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35 DBFEDS Register (Offset = D8h) [Reset = 00000000h]

DBFEDS is shown in Figure 26-72 and described in Table 26-53.

Return to the Summary Table.

Dead band fall edge delay shadow register

Figure 26-72. DBFEDS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DBFEDS													
R-0-0h																		R/W-0h													

Table 26-88. DBFEDS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R-0	0h	Reserved
13-0	DBFEDS	R/W	0h	DBFED Shadow Register The value in the DBFEDS register is loaded into DBFED register when shadow to active load occurs. Reset type: SYSRSn

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36 DBREDS Register (Offset = DCh) [Reset = 00000000h]

DBREDS is shown in Figure 26-73 and described in Table 26-54.

Return to the Summary Table.

Dead band rise edge delay shadow register

Figure 26-73. DBREDS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		DBREDS													
R-0-0h																		R/W-0h													

Table 26-90. DBREDS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R-0	0h	Reserved
13-0	DBREDS	R/W	0h	DBRED Shadow Register The value in the DBREDS register is loaded into DBRED register when shadow to active load occurs. Reset type: SYSRSn

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37 GLDCTL Register (Offset = F0h) [Reset = 00000000h]

GLDCTL is shown in Figure 26-74 and described in Table 26-55.

Return to the Summary Table.

Global load control register

Figure 26-74. GLDCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		GLDMODE		RESERVED		OSHTMODE	GLD
R-0-0h		R/W-0h		R-0-0h		R/W-0h	R/W-0h

Table 26-92. GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5-4	GLDMODE	R/W	0h	Select global load event 00: CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: CTR = Zero or CTR = PRD 11: GLDOSHTCTL[GFRCLD] - Softwrae load Reset type: SYSRSn
3-2	RESERVED	R-0	0h	Reserved
1	OSHTMODE	R/W	0h	Global load one-shot enable 0: Disable global load one-shot 1: Enable global load one-shot Reset type: SYSRSn
0	GLD	R/W	0h	Global load enable 0: Disable global load 1: Enable global load Reset type: SYSRSn

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38 GLDOSHTCTL Register (Offset = F4h) [Reset = 00000000h]

GLDOSHTCTL is shown in Figure 26-75 and described in Table 26-56.

Return to the Summary Table.

Global load one shot control register

Figure 26-75. GLDOSHTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED					GFRCLD	OSHTCLR	OSHTLD
R-0-0h					R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 26-94. GLDOSHTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R-0	0h	Reserved
2	GFRCLD	R-0/W1S	0h	Force Load Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Force load event. This bit is intended to be used for testing and/or software force loading of the events in global load mode. Reset type: SYSRSn
1	OSHTCLR	R-0/W1S	0h	Clear One Shot latch 0: Writing of 0 will be ignored. Always reads back a 0. 1: Turns the one shot latch condition OFF. Reset type: SYSRSn
0	OSHTLD	R-0/W1S	0h	Enable Reload Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence writing 1 to this bit would allow one load strobe event to pass through and block further strobe events. Reset type: SYSRSn

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39 GLDOSHTSTS Register (Offset = F8h) [Reset = 00000000h]

GLDOSHTSTS is shown in Figure 26-76 and described in Table 26-57.

Return to the Summary Table.

Global load one shot status register

Figure 26-76. GLDOSHTSTS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED							OSHTLATCH
R-0-0h							R-0h

Table 26-96. GLDOSHTSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R-0	0h	Reserved
0	OSHTLATCH	R	0h	One shot latch output 0: one shot latch condition is OFF. 1: one shot latch condition is ON. Reset type: SYSRSn

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40 PWM1_CMPA Register (Offset = 100h) [Reset = 00000000h]

PWM1_CMPA is shown in Figure 26-77 and described in Table 26-58.

Return to the Summary Table.

PWM1 counter compare A register

Figure 26-77. PWM1_CMPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM1_CMPA															
R-0-0h																R/W-0h															

Table 26-98. PWM1_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM1_CMPA	R/W	0h	PWM1 Compare A register The value in the PWM1_CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM1 counter-compare module generates a 'time-base counter equal to CMP A' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM1A or the PWM1B output depending on the configuration of the PWM1_AQCTLA and PWM1_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM1_LOADAMODE] field. By default this register is shadowed. Reset type: SYSRSn

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41 PWM1_CMPAS Register (Offset = 104h) [Reset = 00000000h]

PWM1_CMPAS is shown in Figure 26-78 and described in Table 26-59.

Return to the Summary Table.

PWM1 counter compare A shadow register

Figure 26-78. PWM1_CMPAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM1_CMPAS															
R-0-0h																R/W-0h															

Table 26-100. PWM1_CMPAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM1_CMPAS	R/W	0h	PWM1 Compare A Shadow Register The value in the PWM1_CMPAS register is loaded into PWM!_CMPA register when shadow to active load occurs. Reset type: SYSRSn

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42 PWM1_CMPB Register (Offset = 108h) [Reset = 00000000h]

PWM1_CMPB is shown in Figure 26-79 and described in Table 26-60.

Return to the Summary Table.

PWM1 counter compare B register

Figure 26-79. PWM1_CMPB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM1_CMPB															
R-0-0h																R/W-0h															

Table 26-102. PWM1_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM1_CMPB	R/W	0h	PWM1 Compare B register The value in the PWM1_CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM1 counter-compare module generates a 'time-base counter equal to CMP B' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM1A or the PWM1B output depending on the configuration of the PWM1_AQCTLA and PWM1_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM1_LOADBMODE] field. By default this register is shadowed. Reset type: SYSRSn

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43 PWM1_CMPBS Register (Offset = 10Ch) [Reset = 00000000h]

PWM1_CMPBS is shown in Figure 26-80 and described in Table 26-61.

Return to the Summary Table.

PWM1 counter compare B shadow register

Figure 26-80. PWM1_CMPBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM1_CMPBS															
R-0-0h																R/W-0h															

Table 26-104. PWM1_CMPBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM1_CMPBS	R/W	0h	PWM1 Compare B Shadow Register The value in the PWM1 CMPBS register is loaded into PWM1 CMPB register when shadow to active load occurs. Reset type: SYSRSn

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44 PWM1_AQCTLA Register (Offset = 120h) [Reset = 00000000h]

PWM1_AQCTLA is shown in Figure 26-81 and described in Table 26-62.

Return to the Summary Table.

PWM1 action qualifier A register

Figure 26-81. PWM1_AQCTLA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-106. PWM1_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM1_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM1_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM1_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM1_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-106. PWM1_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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45 PWM1_AQCTLAS Register (Offset = 124h) [Reset = 00000000h]

PWM1_AQCTLAS is shown in Figure 26-82 and described in Table 26-63.

Return to the Summary Table.

PWM1 action qualifier A shadow register

Figure 26-82. PWM1_AQCTLAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-108. PWM1_AQCTLAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM1_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM1_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM1_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM1_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-108. PWM1_AQCTLAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM1A output low. 10: Set: force PWM1A output high. 11: Toggle PWM1A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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46 PWM1_AQCTLB Register (Offset = 128h) [Reset = 00000000h]

PWM1_AQCTLB is shown in Figure 26-83 and described in Table 26-64.

Return to the Summary Table.

PWM1 action qualifier B register

Figure 26-83. PWM1_AQCTLB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-110. PWM1_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM1_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM1_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM1_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM1_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-110. PWM1_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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47 PWM1_AQCTLBS Register (Offset = 12Ch) [Reset = 00000000h]

PWM1_AQCTLBS is shown in Figure 26-84 and described in Table 26-65.

Return to the Summary Table.

PWM1 action qualifier B shadow register

Figure 26-84. PWM1_AQCTLBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-112. PWM1_AQCTLBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM1_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM1_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM1_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM1_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-112. PWM1_AQCTLBS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM1B output low. 10: Set: force PWM1B output high. 11: Toggle PWM1B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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48 PWM1_AQSFRC Register (Offset = 130h) [Reset = 00000000h]

PWM1_AQSFRC is shown in Figure 26-85 and described in Table 26-66.

Return to the Summary Table.

PWM1 action qualifier software force

Figure 26-85. PWM1_AQSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	PWMB			RESERVED	PWMA		
R-0-0h	R/W-0h			R-0-0h	R/W-0h		

Table 26-114. PWM1_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R-0	0h	Reserved
6-4	PWMB	R/W	0h	Action qualifier software force on PWMB 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output B 010: Forces a continuous high on output B 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM1_AQOTSFRC[PWMB] = '1'. 110: Set (high) when PWM1_AQOTSFRC[PWMB] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM1_AQOTSFRC[PWMB] = '1'. Reset type: SYSRSn
3	RESERVED	R-0	0h	Reserved
2-0	PWMA	R/W	0h	Action qualifier software force on PWMA 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output A 010: Forces a continuous high on output A 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM1_AQOTSFRC[PWMA] = '1'. 110: Set (high) when PWM1_AQOTSFRC[PWMA] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM1_AQOTSFRC[PWMA] = '1'. Reset type: SYSRSn

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49 PWM1_AQOTSFRC Register (Offset = 134h) [Reset = 00000000h]

PWM1_AQOTSFRC is shown in Figure 26-86 and described in Table 26-67.

Return to the Summary Table.

PWM1 action qualifier one time software force

Figure 26-86. PWM1_AQOTSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED			PWMB	RESERVED			PWMA
R-0-0h			R-0/W1S-0h	R-0-0h			R-0/W1S-0h

Table 26-116. PWM1_AQOTSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R-0	0h	Reserved
4	PWMB	R-0/W1S	0h	Action qualifier one time software force on PWMB 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMB. 1: Initiates a single software forced event Reset type: SYSRSn
3-1	RESERVED	R-0	0h	Reserved
0	PWMA	R-0/W1S	0h	Action qualifier one time software force on PWMA 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMA. 1: Initiates a single software forced event Reset type: SYSRSn

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50 PWM2_CMPA Register (Offset = 300h) [Reset = 00000000h]

PWM2_CMPA is shown in Figure 26-87 and described in Table 26-68.

Return to the Summary Table.

PWM2 counter compare A register

Figure 26-87. PWM2_CMPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM2_CMPA															
R-0-0h																R/W-0h															

Table 26-118. PWM2_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM2_CMPA	R/W	0h	PWM2 Compare A register The value in the PWM2_CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM2 counter-compare module generates a 'time-base counter equal to CMP A' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM2A or the PWM2B output depending on the configuration of the PWM2_AQCTLA and PWM2_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM2_LOADAMODE] field. By default this register is shadowed. Reset type: SYSRSn

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51 PWM2_CMPAS Register (Offset = 304h) [Reset = 00000000h]

PWM2_CMPAS is shown in Figure 26-88 and described in Table 26-69.

Return to the Summary Table.

PWM2 counter compare A shadow register

Figure 26-88. PWM2_CMPAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM2_CMPAS															
R-0-0h																R/W-0h															

Table 26-120. PWM2_CMPAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM2_CMPAS	R/W	0h	PWM2 Compare A Shadow Register The value in the PWM2_CMPAS register is loaded into PWM2_CMPA register when shadow to active load occurs. Reset type: SYSRSn

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52 PWM2_CMPB Register (Offset = 308h) [Reset = 00000000h]

PWM2_CMPB is shown in Figure 26-89 and described in Table 26-70.

Return to the Summary Table.

PWM2 counter compare B register

Figure 26-89. PWM2_CMPB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM2_CMPB															
R-0-0h																R/W-0h															

Table 26-122. PWM2_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM2_CMPB	R/W	0h	PWM2 Compare B register The value in the PWM2_CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM2 counter-compare module generates a 'time-base counter equal to CMP B' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM2A or the PWM2B output depending on the configuration of the PWM2_AQCTLA and PWM2_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM2_LOADBMODE] field. By default this register is shadowed. Reset type: SYSRSn

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53 PWM2_CMPBS Register (Offset = 30Ch) [Reset = 00000000h]

PWM2_CMPBS is shown in Figure 26-90 and described in Table 26-71.

Return to the Summary Table.

PWM2 counter compare B shadow register

Figure 26-90. PWM2_CMPBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM2_CMPBS															
R-0-0h																R/W-0h															

Table 26-124. PWM2_CMPBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM2_CMPBS	R/W	0h	PWM2 Compare B Shadow Register The value in the PWM2_CMPBS register is loaded into PWM2_CMPB register when shadow to active load occurs. Reset type: SYSRSn

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54 PWM2_AQCTLA Register (Offset = 320h) [Reset = 00000000h]

PWM2_AQCTLA is shown in Figure 26-91 and described in Table 26-72.

Return to the Summary Table.

PWM2 action qualifier A register

Figure 26-91. PWM2_AQCTLA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-126. PWM2_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM2_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM2_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM2_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM2_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-126. PWM2_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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55 PWM2_AQCTLAS Register (Offset = 324h) [Reset = 00000000h]

PWM2_AQCTLAS is shown in Figure 26-92 and described in Table 26-73.

Return to the Summary Table.

PWM2 action qualifier A shadow register

Figure 26-92. PWM2_AQCTLAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-128. PWM2_AQCTLAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM2_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM2_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM2_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM2_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-128. PWM2_AQCTLAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM2A output low. 10: Set: force PWM2A output high. 11: Toggle PWM2A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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56 PWM2_AQCTLB Register (Offset = 328h) [Reset = 00000000h]

PWM2_AQCTLB is shown in Figure 26-93 and described in Table 26-74.

Return to the Summary Table.

PWM2 action qualifier B register

Figure 26-93. PWM2_AQCTLB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-130. PWM2_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM2_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM2_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM2_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM2_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-130. PWM2_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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57 PWM2_AQCTLBS Register (Offset = 32Ch) [Reset = 00000000h]

PWM2_AQCTLBS is shown in Figure 26-94 and described in Table 26-75.

Return to the Summary Table.

PWM2 action qualifier B shadow register

Figure 26-94. PWM2_AQCTLBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-132. PWM2_AQCTLBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM2_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM2_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM2_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM2_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-132. PWM2_AQCTLBS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM2B output low. 10: Set: force PWM2B output high. 11: Toggle PWM2B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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58 PWM2_AQSFRC Register (Offset = 330h) [Reset = 00000000h]

PWM2_AQSFRC is shown in Figure 26-95 and described in Table 26-76.

Return to the Summary Table.

PWM2 action qualifier software force

Figure 26-95. PWM2_AQSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	PWMB			RESERVED	PWMA		
R-0-0h	R/W-0h			R-0-0h	R/W-0h		

Table 26-134. PWM2_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R-0	0h	Reserved
6-4	PWMB	R/W	0h	Action qualifier software force on PWMB 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output B 010: Forces a continuous high on output B 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM2_AQOTSFRC[PWMB] = '1'. 110: Set (high) when PWM2_AQOTSFRC[PWMB] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM2_AQOTSFRC[PWMB] = '1'. Reset type: SYSRSn
3	RESERVED	R-0	0h	Reserved
2-0	PWMA	R/W	0h	Action qualifier software force on PWMA 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output A 010: Forces a continuous high on output A 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM2_AQOTSFRC[PWMA] = '1'. 110: Set (high) when PWM2_AQOTSFRC[PWMA] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM2_AQOTSFRC[PWMA] = '1'. Reset type: SYSRSn

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59 PWM2_AQOTSFRC Register (Offset = 334h) [Reset = 00000000h]

PWM2_AQOTSFRC is shown in Figure 26-96 and described in Table 26-77.

Return to the Summary Table.

PWM2 action qualifier one time software force

Figure 26-96. PWM2_AQOTSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED			PWMB	RESERVED			PWMA
R-0-0h			R-0/W1S-0h	R-0-0h			R-0/W1S-0h

Table 26-136. PWM2_AQOTSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R-0	0h	Reserved
4	PWMB	R-0/W1S	0h	Action qualifier one time software force on PWMB 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMB. 1: Initiates a single software forced event Reset type: SYSRSn
3-1	RESERVED	R-0	0h	Reserved
0	PWMA	R-0/W1S	0h	Action qualifier one time software force on PWMA 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMA. 1: Initiates a single software forced event Reset type: SYSRSn

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60 PWM3_CMPA Register (Offset = 500h) [Reset = 00000000h]

PWM3_CMPA is shown in Figure 26-97 and described in Table 26-78.

Return to the Summary Table.

PWM3 counter compare A register

Figure 26-97. PWM3_CMPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM3_CMPA															
R-0-0h																R/W-0h															

Table 26-138. PWM3_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM3_CMPA	R/W	0h	PWM3 Compare A register The value in the PWM3_CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM3 counter-compare module generates a 'time-base counter equal to CMP A' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM3A or the PWM3B output depending on the configuration of the PWM3_AQCTLA and PWM3_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM3_LOADAMODE] field. By default this register is shadowed. Reset type: SYSRSn

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61 PWM3_CMPAS Register (Offset = 504h) [Reset = 00000000h]

PWM3_CMPAS is shown in Figure 26-98 and described in Table 26-79.

Return to the Summary Table.

PWM3 counter compare A shadow register

Figure 26-98. PWM3_CMPAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM3_CMPAS															
R-0-0h																R/W-0h															

Table 26-140. PWM3_CMPAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM3_CMPAS	R/W	0h	PWM3 Compare A Shadow Register The value in the PWM3_CMPAS register is loaded into PWM3_CMPA register when shadow to active load occurs. Reset type: SYSRSn

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62 PWM3_CMPB Register (Offset = 508h) [Reset = 00000000h]

PWM3_CMPB is shown in Figure 26-99 and described in Table 26-80.

Return to the Summary Table.

PWM3 counter compare B register

Figure 26-99. PWM3_CMPB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM3_CMPB															
R-0-0h																R/W-0h															

Table 26-142. PWM3_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM3_CMPB	R/W	0h	PWM3 Compare B register The value in the PWM3_CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the PWM3 counter-compare module generates a 'time-base counter equal to CMP B' event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the PWM3A or the PWM3B output depending on the configuration of the PWM3_AQCTLA and PWM3_AQCTLB registers Shadowing of this register is enabled and disabled by the CMPCTL[PWM3_LOADBMODE] field. By default this register is shadowed. Reset type: SYSRSn

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63 PWM3_CMPBS Register (Offset = 50Ch) [Reset = 00000000h]

PWM3_CMPBS is shown in Figure 26-100 and described in Table 26-81.

Return to the Summary Table.

PWM3 counter compare B shadow register

Figure 26-100. PWM3_CMPBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PWM3_CMPBS															
R-0-0h																R/W-0h															

Table 26-144. PWM3_CMPBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-0	PWM3_CMPBS	R/W	0h	PWM3 Compare B Shadow Register The value in the PWM3 CMPBS register is loaded into PWM3 CMPB register when shadow to active load occurs. Reset type: SYSRSn

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64 PWM3_AQCTLA Register (Offset = 520h) [Reset = 00000000h]

PWM3_AQCTLA is shown in Figure 26-101 and described in Table 26-82.

Return to the Summary Table.

PWM3 action qualifier A register

Figure 26-101. PWM3_AQCTLA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-146. PWM3_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM3_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM3_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM3_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM3_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-146. PWM3_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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65 PWM3_AQCTLAS Register (Offset = 524h) [Reset = 00000000h]

PWM3_AQCTLAS is shown in Figure 26-102 and described in Table 26-83.

Return to the Summary Table.

PWM3 action qualifier A shadow register

Figure 26-102. PWM3_AQCTLAS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-148. PWM3_AQCTLAS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM3_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM3_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM3_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM3_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-148. PWM3_AQCTLAS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM3A output low. 10: Set: force PWM3A output high. 11: Toggle PWM3A output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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66 PWM3_AQCTLB Register (Offset = 528h) [Reset = 00000000h]

PWM3_AQCTLB is shown in Figure 26-103 and described in Table 26-84.

Return to the Summary Table.

PWM3 action qualifier B register

Figure 26-103. PWM3_AQCTLB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-150. PWM3_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM3_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM3_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM3_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM3_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-150. PWM3_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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67 PWM3_AQCTLBS Register (Offset = 52Ch) [Reset = 00000000h]

PWM3_AQCTLBS is shown in Figure 26-104 and described in Table 26-85.

Return to the Summary Table.

PWM3 action qualifier B shadow register

Figure 26-104. PWM3_AQCTLBS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CBD		CBU		CAD		CAU		PRD		ZRO	
R-0-0h				R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 26-152. PWM3_AQCTLBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R-0	0h	Reserved
11-10	CBD	R/W	0h	Action When TBCTR = PWM3_CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
9-8	CBU	R/W	0h	Action When TBCTR = PWM3_CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
7-6	CAD	R/W	0h	Action When TBCTR = PWM3_CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
5-4	CAU	R/W	0h	Action When TBCTR = PWM3_CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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Table 26-152. PWM3_AQCTLBS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRD	R/W	0h	Action When TBCTR = TBPRD 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn
1-0	ZRO	R/W	0h	Action When TBCTR = 0 00: Do nothing (action disabled) 01: Clear: force PWM3B output low. 10: Set: force PWM3B output high. 11: Toggle PWM3B output: low output signal will be forced high, and a high signal will be forced low. Reset type: SYSRSn

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68 PWM3_AQSFRC Register (Offset = 530h) [Reset = 00000000h]

PWM3_AQSFRC is shown in Figure 26-105 and described in Table 26-86.

Return to the Summary Table.

PWM3 action qualifier software force

Figure 26-105. PWM3_AQSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	PWMB			RESERVED	PWMA		
R-0-0h	R/W-0h			R-0-0h	R/W-0h		

Table 26-154. PWM3_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R-0	0h	Reserved
6-4	PWMB	R/W	0h	Action qualifier software force on PWMB 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output B 010: Forces a continuous high on output B 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM3_AQOTSFRC[PWMB] = '1'. 110: Set (high) when PWM3_AQOTSFRC[PWMB] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM3_AQOTSFRC[PWMB] = '1'. Reset type: SYSRSn
3	RESERVED	R-0	0h	Reserved
2-0	PWMA	R/W	0h	Action qualifier software force on PWMA 000: Does nothing (softwrae force disabled) 001: Forces a continuous low on output A 010: Forces a continuous high on output A 011: Does nothing (softwrae force disabled) 100: Does nothing (softwrae force disabled) 101: Clear (low) when PWM3_AQOTSFRC[PWMA] = '1'. 110: Set (high) when PWM3_AQOTSFRC[PWMA] = '1'. 111: Toggle (Low -> High, High -> Low) when PWM3_AQOTSFRC[PWMA] = '1'. Reset type: SYSRSn

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69 PWM3_AQOTSFRC Register (Offset = 534h) [Reset = 00000000h]

PWM3_AQOTSFRC is shown in Figure 26-106 and described in Table 26-87.

Return to the Summary Table.

PWM3 action qualifier one time software force

Figure 26-106. PWM3_AQOTSFRC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED			PWMB	RESERVED			PWMA
R-0-0h			R-0/W1S-0h	R-0-0h			R-0/W1S-0h

Table 26-156. PWM3_AQOTSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R-0	0h	Reserved
4	PWMB	R-0/W1S	0h	Action qualifier one time software force on PWMB 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMB. 1: Initiates a single software forced event Reset type: SYSRSn
3-1	RESERVED	R-0	0h	Reserved
0	PWMA	R-0/W1S	0h	Action qualifier one time software force on PWMA 0: Writing a 0 has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on PWMA. 1: Initiates a single software forced event Reset type: SYSRSn

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Chapter 27

Sigma Delta Filter Module (SDFM)

The sigma delta filter module (SDFM) is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each input channel can receive an independent delta-sigma (ΔΣ) modulator bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator (secondary filter) for immediate digital threshold comparisons for over-current and under-current monitoring, and zeros crossing detection.

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27.7 Theoretical SDFM Filter Output 1900
27.8 SDFM Interrupts & Triggers 1901
27.9 SDFM Registers 1903

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27.1 Introduction

Figure 27-1 shows the SDFM CPU Interface.

Figure 27-1. Sigma Delta Filter Module (SDFM) CPU Interface

27.1.1 SDFM Related Collateral

Foundational Materials

- Nuts and Bolts of the Delta-Sigma Converter (Video)
- Sigma Delta Filter Module (SDFM) Training for C2000™ MCUs (Video)

Getting Started Materials

- *Achieving Better Signal Integrity With Isolated Delta-Sigma Modulators in Motor Drives Application Report*
  - Critical information for a hardware designer
- Using Sigma Delta Filter Module (SDFM) to Measure the Analog Input Signal
  - NOTE: This is a non-TI (third party) site.

Expert Materials

- *Isolated Current Shunt and Voltage Measurement Kit Application Report*
- Isolated, Shunt-Based Current Sensing Reference Design
- The case for isolated delta-sigma modulators: Is my system fast enough for short-circuit detection?

27.1.2 Features

SDFM features include:

- Eight external pins per SDFM module
  - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Different configurable modulator clock modes supported:
  - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable or disable (or both) individual filter module
  - Ability to synchronize all four independent filters of an SDFM module by using the Main Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.

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27.1.3 Block Diagram

Each SDFM module has four independent filter modules. These filter modules are identical and can be configured independently. Each individual filter module has the following units:

- Input control unit
- Primary filter (data filter) unit
- Secondary filter (comparator filter) unit with 4 independent comparators

Figure 27-2 shows the SDFM module block diagram. The SDFM port operation is configured and controlled by the registers listed in *SDFM Registers*.

Figure 27-2. Sigma Delta Filter Module (SDFM) Block Diagram

Each filter module shown in Figure 27-3 has a primary (data) filter and a secondary (comparator) filter pair that receives the same bit stream. Except for the input bit stream, both the primary and secondary filter are completely independent of each other. Each of these filter modules can be independently configured. So, in a SDFM module, there is a total of four primary filters and four secondary filters.

Figure 27-3. Block Diagram of One Filter Module

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27.2 Input Qualification

Impulse noise sources such as EMI, crosstalk, and so on, has the possibility of corrupting SDCLK and SDDATA bit streams, resulting in corrupted SDFM filtered data. This impulse noise effects can be mitigated when using the input qualification feature that synchronizes SDCLK/SDDATA signals with PLLRAWCLK1. By default, both SDCLK and SDDATA bit stream are not synchronized. SDCLK can be synchronized to PLLRAWCLK1 by setting SDCTLPARMx.SDCLKSYNC = 1 and SDDATA can be synchronized to PLLRAWCLK1 by setting SDCTLPARMx.SDDATASYNC = 1. Figure 27-4 shows optional Input Qualification option on SDCLK and SDDATA lines.

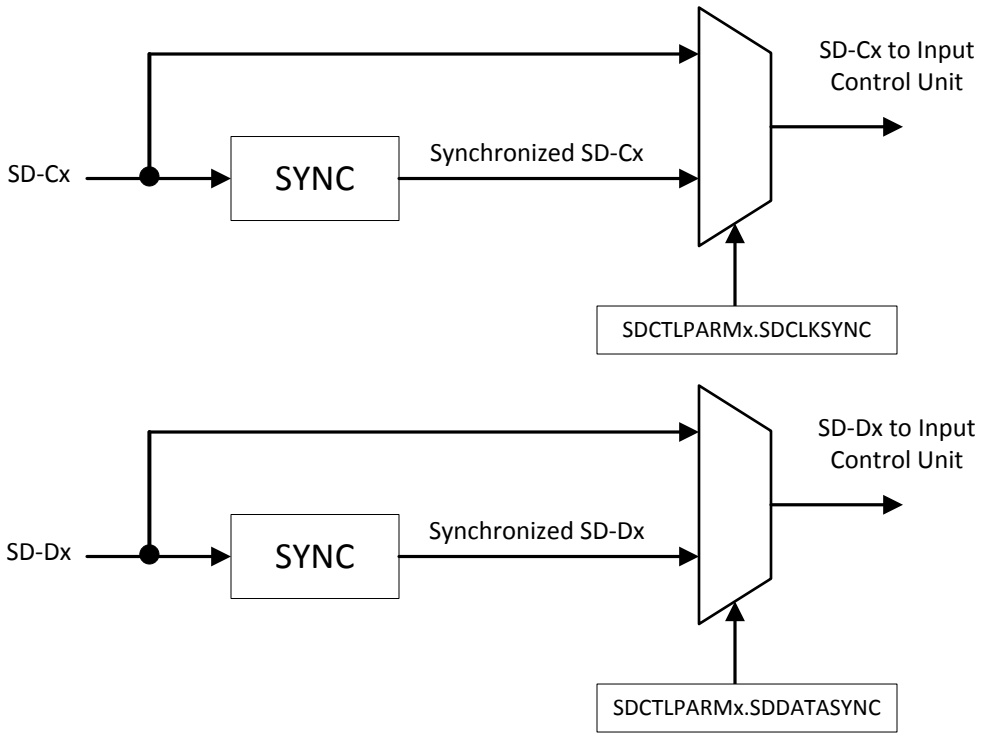


Figure 27-4. Input Qualification on SD-Cx and SD-Dx

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27.3 Input Control Unit

The input control unit receives sigma delta modulated data and a sigma delta modulated clock. The modulated data received is captured and passed on to the data filter unit and comparator unit. This unit can be configured to receive the modulated data in Table 27-1 and Figure 27-5 show how SDCTLPARMx.MOD bits can be configured in

Table 27-1. Modulator Clock Modes

Modulator Mode [MOD]	Description
0	The modulator clock is running with the modulator data rate. The modulator data is strobed at every rising edge of the modulator clock.
1	
2	
3	

Note

To achieve the maximum value, the sigma-delta modulator has to be operated at absolute maximum positive or negative full scale, which is outside of the recommended full scale range of 80% of most sigma-delta modulators.

Figure 27-5. Different Modulator Modes Supported

27.4 Sinc Filter

Both the comparator filter and data filter available in SDFM have the Sinc^N filter as the core. The Sinc^N filter is essentially a low-pass filter that converts the input bit stream into digital data by digital filtering and decimation. This filtered digital data represents analog input given to the sigma delta modulator. Simplified Sinc^N architecture consists of cascaded integrators and differentiators separated by a down-sampler as shown in Figure 27-6. The Z-transfer function of the Sinc filter of order N is shown in Figure 27-7.

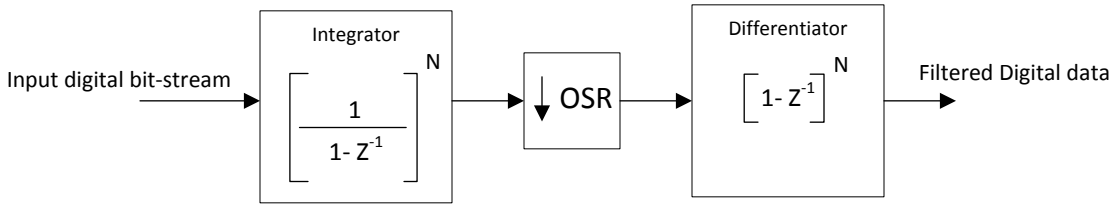


Figure 27-6. Simplified Sinc Filter Architecture

$$H(Z) = \left[\frac{1 - Z^{-OSR}}{1 - Z^{-1}} \right]^N$$

N = Order of Sinc filter
OSR = Over Sampling Ratio

Figure 27-7. Z-Transform of Sinc Filter of Order N

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Effective resolution of the Sinc filter (ENOB) depends upon filter type, OSR and sigma-delta modulator frequency. Typically, higher resolution or ENOB can be achieved by higher OSR for a given filter type; however, the tradeoff is increased filter delay. It is important to choose the right sigma delta modulator by studying the optimal speed versus resolution tradeoff. Refer to the corresponding sigma delta modulator data sheet to determine the effective resolution for a given Sinc filter configuration. Figure 27-8 shows the frequency response of different filter structures when OSR = 32 and when the sigma delta modulator frequency is 10MHz.

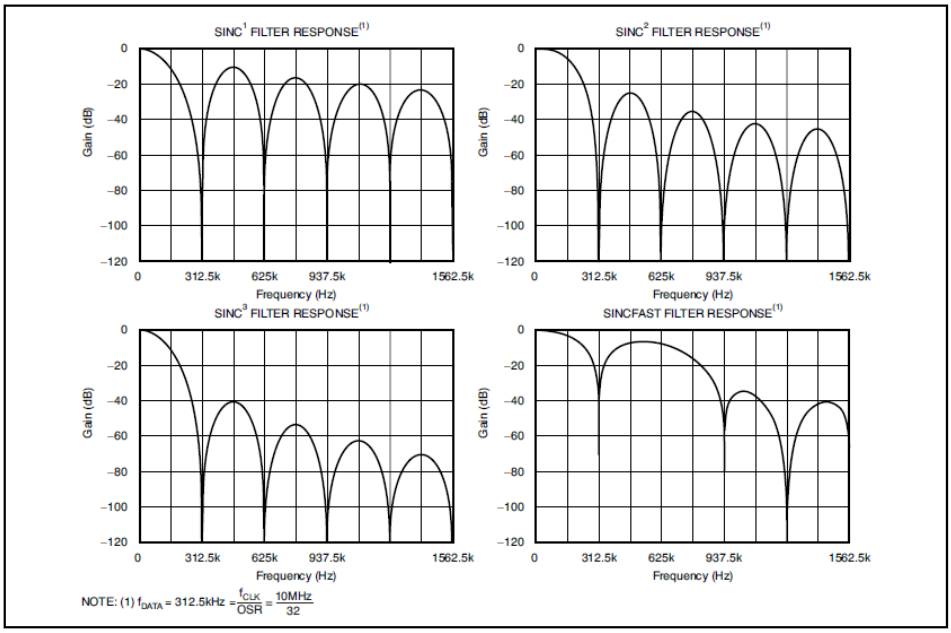


Figure 27-8. Frequency Response of Different Sinc Filters

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The order of different sinc filter is shown in Table 27-2.

Table 27-2. Order of Sinc Filter

Filter Type	Order of Sinc Filter
Sinc1	1
Sinc2	2
Sinc3	3
SincFast	3

27.4.1 Data Rate and Latency of the Sinc Filter

The data rate of the sinc filter (filter throughput) represented in samples/sec is calculated by the following formula:

$$Data\ rate\ of\ Sinc\ filter = \frac{Modulator\ data\ rate}{OSR} \quad (40)$$

The latency of the sinc filter represented in secs is defined as the amount of time taken by a sinc filter type to deliver the correct filtered output upon initiation. For a given filter type, latency is calculated by the following formula:

$$Latency\ of\ Sinc\ filter = \frac{Order\ of\ Sinc\ filter}{Data\ rate\ of\ Sinc\ filter} \quad (41)$$

Example configuration:

Sinc filter type	= sinc3
Modulator data rate	= 10MHz
OSR	= 256
Data rate of Sinc Filter	= 10MHz/256 = 39.1K samples/second
Sinc filter latency	= 76.8µs

Sinc filter type	= sinc2
Modulator data rate	= 10MHz
OSR	= 256
Data rate of Sinc Filter	= 10MHz/256 = 39.1K samples/second
Sinc filter latency	=51.2µs

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27.5 Data (Primary) Filter Unit

The data filter is a configurable Sinc filter which supports the following filter types: Sinc1, Sinc2, Sinc3, and SincFast. The data filter OSR (DOSR) settings can be configured from 1 to 256 and is independent of the comparator filter. Effective resolution of the data filter (ENOB) depends upon Data filter type, DOSR, and sigma-delta modulator frequency. By default, the data filter is disabled and setting of SDDFPARMx.FEN = 1 enables the data filter. The data filter output is represented in signed integer in two's complement format. This filter unit translates a low input signal as '-1' and a high input signal as '1'. The resulting calculation gives both positive and negative values for the output of the data filter. Table 27-3 shows the different full scale values that the data filter can store using different OSRs.

See Section 27.4.1 to understand how to calculate data rate and latency of data filter.

Table 27-3. Peak Data Values for Different DOSR/Filter Combinations

DOSR	Sinc1	Sinc2	Sinc3	SincFast
x	x	x^2	x^3	$2x^2$
4	–4 to 4	–16 to 16	–64 to 64	–32 to 32
8	–8 to 8	–64 to 64	–512 to 512	–128 to 128
16	–16 to 16	–256 to 256	–4096 to 4096	–512 to 512
32	–32 to 32	–1024 to 1024	–32,768 to 32,768	–2048 to 2048
64	–64 to 64	–4096 to 4096	–262,144 to 262,144	–8192 to 8192
128	–128 to 128	–16,384 to 16,384	–2,097,152 to 2,097,152	–32,768 to 32,768
256	–256 to 256	–65,536 to 65,536	–16,777,216 to 16,777,216	–131,072 to 131,072

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27.5.1 32-bit or 16-bit Data Filter Output Representation

The data filter output can be represented in either 32-bit or 16-bit format.

32-bit data filter representation:

- When SDDPARMx.DR = 1, data filter output is represented in 32-bit format. Writes to shift control bits do not have any bearing on the output of the data filter in this configuration.

16-bit data filter representation:

- By default, data filter output is represented in 16-bit format
- When SDDPARMx.DR = 0, data filter output is represented in 16-bit format. But it is the responsibility of the user to configure the corresponding shift control bits in the SDDPARMx register to control which 16-bit part of the 32-bit word is sent to the register map.

  For example, for the data filter configuration below:
  - Filter type = Sinc3
  - OSR = 128
  - SDDPARMx.DR = 0

  The data filter with a signed output value can be in the range of –2,097,152 to 2,097,152. But, 16-bit signed output supports values only from –32,768 to 32,767. Therefore, it is required to configure shift control bits (SDDPARMx.SH) to 7 to represent the data filter output correctly in 16-bit format. Table 27-4 shows the configuration settings of shift control bits for different OSR and filter types.

Table 27-4. Shift Control Bit Configuration Settings

OSR	Sinc1	Sinc2	SincFast	Sinc3
1 to 31	0	0	0	0
32 to 40	0	0	0	1
41 to 50	0	0	0	2
51 to 63	0	0	0	3
64 to 80	0	0	0	4
81 to 101	0	0	0	5
102 to 127	0	0	0	6
128 to 161	0	0	1	7
162 to 181	0	0	1	8
182 to 203	0	1	2	8
204 to 255	0	1	2	9
256	0	2	3	

CAUTION

Configuring shift control bits incorrectly results in getting an incorrect 16-bit data filter output.

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27.5.2 SDSYNC Event

Primary (data) filters can be synchronized with respect to the PWM event (called SDSYNC event). The SDSYNC signal from the PWM module is used to reset the DOSR counter. This feature is by default disabled and can be enabled by setting SDDFPARMx.SDSYNCEN = 1.

Figure 27-9. SDSYNC Event

Because of the inherent architecture of the Sinc filter (Sinc1, Sinc2, Sinc3, SincFast), the first few samples, depending upon filter type, are incorrect. Table 27-5 shows the number of incorrect samples on the following conditions:

- When Sinc filter is enabled and configured for first time.
- When Sinc filter is disabled and re-enabled or reconfigured in the middle of operation.
- When data filter receives SDSYNC event from PWM.

Table 27-5. Number of Incorrect Samples Tabulated

Filter Type	Number of Incorrect Samples After the Filter is Enabled and Configured
Sinc1	No incorrect sample.
Sinc2	The first sample of the Sinc2 filter is incorrect.
SincFast	The first two samples of the SincFast filter are incorrect.
Sinc3	The first two samples of the Sinc3 filter are incorrect.

CAUTION

SDFM comparator interrupts can be enabled only after providing sufficient settling time to make sure the comparator filter does not trip on these incorrect samples. Therefore, SDFM comparator interrupts can be enabled only after a sufficient delay is provided after the comparator filter is configured. This sufficient delay is calculated by adding the latency of the comparator filter and 5 SD-Cx clock cycles.

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27.6 Comparator (Secondary) Filter Unit

Most control systems require protection of the system by tripping the PWM in case the current or voltage goes out of bounds. The primary purpose of the secondary (comparator) filter is to allow the user to monitor input conditions with a fast settling time. This allows the user to trip PWMs to protect the system from potential damage.

Note

The secondary (comparator) filter cannot be synchronized with respect to the PWM event (SDSYNC event).

The comparator filter is a configurable Sinc filter that supports the following filter types: Sinc1, Sinc2, Sinc3, and SincFast. The comparator OSR (COSR) settings can be configured from 1 to 32 and is independent of the data filter. Effective resolution of the comparator filter (ENOB) depends upon the comparator filter type, COSR, and sigma-delta modulator frequency. By default, the comparator filter is . The comparator filter output is represented in 16-bit unsigned format. This filter unit translates a low input signal as 0 and a high input signal as 1. The resulting calculations give only positive values for the output of the comparator filter. Table 27-6 shows the different full-scale values that the comparator filter can store using different OSRs.

Table 27-6. Peak Data Values for Different OSR/Filter Combinations

OSR	Sinc1	Sinc2	Sinc3	SincFast
x	0 to x	0 to x2	0 to x3	0 to 2x2
4	0 to 4	0 to 16	0 to 64	0 to 32
8	0 to 8	0 to 64	0 to 512	0 to 128
16	0 to 16	0 to 256	0 to 4096	0 to 512
32	0 to 32	0 to 1024	0 to 32,768	0 to 2048

See Section 27.4.1 to understand how to calculate data rate and latency of comparator filter.

The output of the comparator filter is connected to digital comparators explained below.

Figure 27-10. Comparator Unit Structure

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27.6.1 Higher Threshold (HLT)

- High threshold comparator can be used to detect over-value condition.
- When comparator data > = higher threshold register, a high threshold event is generated.
- Higher threshold comparator events can be configured to trigger following events: CPU interrupt, PWM trip.
- This device has high threshold :

27.6.2 Lower Threshold (LLT)

- The low threshold comparator can be used to detect under-value condition.
- When comparator data < = Lower Threshold register, a low threshold event is generated.
- Lower threshold comparator events can be configured to trigger following events: CPU interrupt, PWM trip.
- This device has .

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27.7 Theoretical SDFM Filter Output

The following equations can be used to derive a theoretical filter output of an SDFM filter output for both a comparator filter and a data filter.

$$\text{Density of ones in bitstream} = \frac{\text{Input Voltage} + \text{Vclipping}}{2 \times \text{Vclipping}} \tag{42}$$

Where:

- Vclipping = maximum differential voltage input range of modulator
- Input voltage = Differential input voltage applied to the modulator

$$\text{Comparator Filter Output (Theoretical)} = \text{Density of ones in bitstream} \times \text{Maximum Filter Output (FilterType, COSR)} \tag{43}$$

$$\text{FilterOutput} = \left\{\frac{\text{absolute(Input voltage)}}{\text{Vclipping}}\right\} \times \text{Maximum Filter Output (FilterType, DOSR)} \tag{44}$$

$$\text{Data Filter Output_32bit(Theoretical)} = \begin{cases} \text{FilterOutput} & \text{if Input Voltage is +ve voltage} \\ \text{2's complement of FilterOutput} & \text{if input voltage is -ve voltage} \end{cases} \tag{45}$$

$$\text{Data Filter Output_16bit(Theoretical)} = \text{Data Filter Output_32bit(Theoretical)} >> \text{Shift value(FilterType, OSR)} \tag{46}$$

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For example, when using the AMC1306x25 modulator:

AMC1306x25	Vclipping = Input voltage (AINP - AINN) =	320mV 100mV
SDFM filter settings	Filter type = Comparator OSR (COSR) = Data filter OSR (DOSR) =	3 32 100

Density of 1s in bit stream	Using Equation 42	0.65625
Comparator filter output Filter type = Sinc3 COSR = 32	Using Equation 43	21504
Data filter output (32-bit) Filter type = Sinc3 DOSR = 100	Using Equation 44 and Equation 45	312500
Data filter output (32-bit) Filter type = Sinc3 DOSR = 100 (Right shift by 5)	Using Equation 46	9765

27.8 SDFM Interrupts & Triggers

27.8.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 27-7. CPU Interrupts Triggered by SDFM

NVIC Interrupt Name	Peripheral Instance Name	Register Group	SDFM Interrupt Configuration Registers	Description
SDFM	SDFM	N/A	SDCTL.MIE, SDCPARMx, SDFIFOCTLx.OVFIEN, SDIFLG, SDIFLGCLR	SDFM Error interrupt. Multiple OR'd, configurable source conditions.
SDFMDR1	SDFM	N/A	SDFIFOCTL1.DRINTSEL, SDIFLG.SDFFINT1, SDIFLGCLR.SDFFINT1	SDFM Channel 1 Data Ready interrupt. Single configurable source condition.
SDFMDR2	SDFM	N/A	SDFIFOCTL2.DRINTSEL, SDIFLG.SDFFINT2, SDIFLGCLR.SDFFINT2	SDFM Channel 2 Data Ready interrupt. Single configurable source condition.
SDFMDR3	SDFM	N/A	SDFIFOCTL3.DRINTSEL, SDIFLG.SDFFINT3, SDIFLGCLR.SDFFINT3	SDFM Channel 3 Data Ready interrupt. Single configurable source condition.

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Table 27-7. CPU Interrupts Triggered by SDFM (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	SDFM Interrupt Configuration Registers	Description
SDFMDR4	SDFM	N/A	SDFIFOCTL4.DRINTSEL, SDIFLG.SDFFINT4, SDIFLGCLR.SDFFINT4	SDFM Channel 4 Data Ready interrupt. Single configurable source condition.

27.8.1.1 SDFM SDyERR Interrupt Sources

Figure 27-11 shows the structure of SDy_ERR interrupt. SDy_ERR interrupt can be triggered by any of these 16 events.

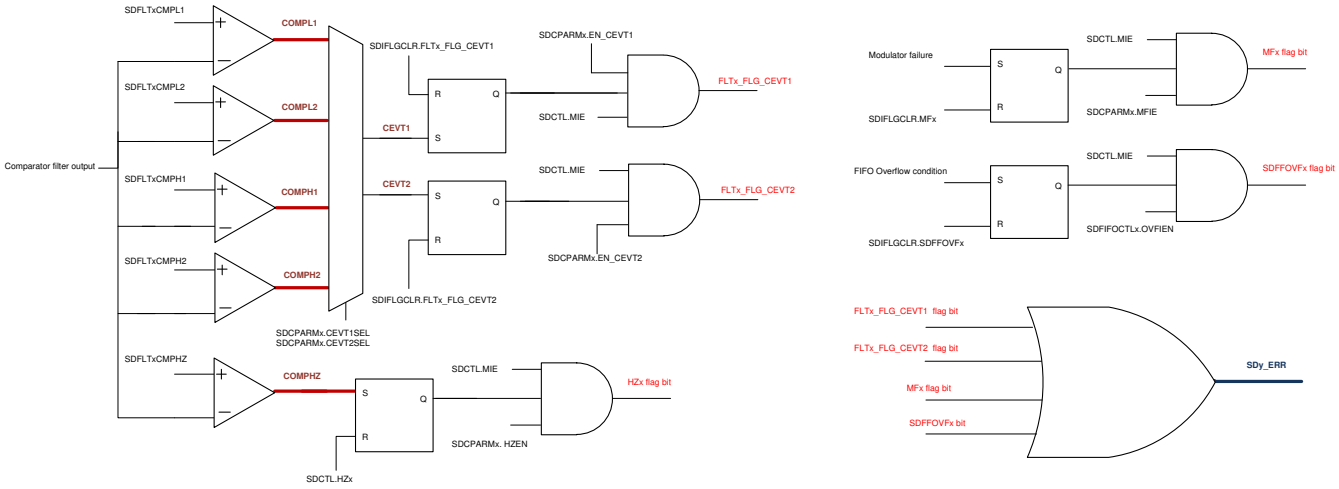


Figure 27-11. SDFM Error (SD_ERR) Interrupt Sources

Note

The HZx flag bits cannot be used to trigger an interrupt. However, the CPU can check the status of these flags in the SDSTATUS register and clear the status via the SDCTL.HZx register bits.

1. Comparator Event1 (CEVT1) CEVT1 events from any of the four comparator filter module can trigger CPU interrupt. This event can be configured to trigger SDy_ERR interrupt only if below configurations are made:
   - Enable Main interrupt enable (SDCTL.MIE = 1)
   - Enable comparator Event1 interrupt (SDCPARMx.EN_CEVT1 = 1)

   On a CEVT1 event, SDIFLG. flag bit is set.This flag bit can only be reset if the corresponding bit in SDIFLGCLR register is set and if the interrupt source is no longer active.
2. Comparator Event2 (CEVT2) CEVT2 events from any of the four comparator filter module can trigger CPU interrupt. This event can be configured to trigger SDy_ERR interrupt only if below configurations are made:
   - Enable Main interrupt enable (SDCTL.MIE = 1)
   - Enable comparator event1 interrupt (SDCPARMx.EN_CEVT2 = 1)

   On a CEVT2 event, SDIFLG.FLTx_FLG_CEVT2 flag bit is set. This flag bit can only be reset if the corresponding bit in SDIFLGCLR register is set and if the interrupt source is no longer active.
3. Modulator Failure (MFx) event Modulator failures (MFx) are generated when SD-Cx goes missing. The modulator clock is considered missing if SD-Cx does not toggle for 64-MCLKs. MFx events from any of the four filter modules can trigger CPU interrupt. This event can be configured to trigger SDy_ERR interrupt only if below configurations are made:
   - Enable Main Interrupt Enable (SDCTL.MIE = 1)
   - Enable modulator clock failure interrupt source (SDCPARMx.MFIE = 1)

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On a MFx event, SDIFLG.MFx flag bit is set. This flag bit can only be reset if the corresponding bit in SDIFLGCLR register is set and if the interrupt source is no longer active.

4. FIFO overflow (SDFFOVFx) event The number of filter data available in FIFO at any given point can be tracked in SDFIFOCTLx.SDFFST. If the number of words received in FIFO is greater than Max FIFO depth (16), SDFFOVFx event is generated. SDFFOVFx events from any of the four filter modules can trigger CPU interrupt. This event can be configured to trigger SDy_ERR interrupt, only if below configurations are made:
   - Enable SDFM FIFO (Set SDFIFOCTLx.FFEN = 1)
   - Enable SDFM FIFO overflow interrupt (Set SDFIFOCTLx.OVFIEN = 1) and
   - Enable Main interrupt enable (Set SDCTL.MIE = 1)

   On a SDFFOVFx event, all subsequent data (primary) filter data is lost and is not stored in FIFO. SDIFLG.SDFFOVFx flag bit is set on a FIFO overflow event and this bit can be cleared if the corresponding bit in SDIFLGCLR register is set and if the interrupt source is no longer active.

27.8.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 27-8. DMA Triggers from the SDFM

Trigger Name	Peripheral Instance Name	Register Group	SDFM DMA Configuration Registers	Description
SDDRINT1	SDFM	N/A	SDFIFOCTL1.DRINTSEL, SDIFLG.SDFFINT1, SDIFLGCLR.SDFFINT1	SDFM Channel 1 Data Ready interrupt. Single configurable source condition.
SDDRINT2	SDFM	N/A	SDFIFOCTL2.DRINTSEL, SDIFLG.SDFFINT2, SDIFLGCLR.SDFFINT2	SDFM Channel 2 Data Ready interrupt. Single configurable source condition.
SDDRINT3	SDFM	N/A	SDFIFOCTL3.DRINTSEL, SDIFLG.SDFFINT3, SDIFLGCLR.SDFFINT3	SDFM Channel 3 Data Ready interrupt. Single configurable source condition.
SDDRINT4	SDFM	N/A	SDFIFOCTL4.DRINTSEL, SDIFLG.SDFFINT4, SDIFLGCLR.SDFFINT4	SDFM Channel 4 Data Ready interrupt. Single configurable source condition.

27.9 SDFM Registers

This Section describes the SDFM Registers.

27.9.1 SDFM Base Address Table

Table 27-9. SDFM Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
SdfmRegs	SDFM_REGS	SDFM	0x4049_1000

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27.9.2 SDFM_REGS Registers

Table 27-10 lists the memory-mapped registers for the SDFM_REGS registers. All register offset addresses not listed in Table 27-10 should be considered as reserved locations and the register contents should not be modified.

Table 27-10. SDFM_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	SDIFLG	SD Interrupt Flag Register		Go
4h	SDIFLGCLR	SD Interrupt Flag Clear Register		Go
8h	SDCTL	SD Control Register		Go
Ch	SDMFILEN	SD Master Filter Enable		Go
Eh	SDSTATUS	SD Status Register		Go
10h	SDINTMODE	SD Interrupt Mode register		Go
20h	SDCTLPARM1	Control Parameter Register for Ch1		Go
22h	SDDFPARM1	Data Filter Parameter Register for Ch1		Go
24h	SDDPARM1	Data Parameter Register for Ch1		Go
26h	SDFLT1CMPH1	High-level Threshold Register for Ch1		Go
28h	SDFLT1CMPL1	Low-level Threshold Register for Ch1		Go
2Ah	SDCPARM1	Comparator Filter Parameter Register for Ch1		Go
2Ch	SDDATA1	Data Filter Data Register (16 or 32bit) for Ch1		Go
30h	SDDATFIFO1	Filter Data FIFO Output(32b) for Ch1		Go
34h	SDCDATA1	Comparator Filter Data Register (16b) for Ch1		Go
36h	SDFLT1CMPH2	Second high level threhold for CH1		Go
38h	SDFLT1CMPHZ	High-level (Z) Threshold Register for Ch1		Go
3Ah	SDFIFOCTL1	FIFO Control Register for Ch1		Go
3Ch	SDSYNC1	SD Filter Sync control for Ch1		Go
3Eh	SDFLT1CMPL2	Second low level threhold for CH1		Go
40h	SDCTLPARM2	Control Parameter Register for Ch2		Go
42h	SDDFPARM2	Data Filter Parameter Register for Ch2		Go
44h	SDDPARM2	Data Parameter Register for Ch2		Go
46h	SDFLT2CMPH1	High-level Threshold Register for Ch2		Go
48h	SDFLT2CMPL1	Low-level Threshold Register for Ch2		Go
4Ah	SDCPARM2	Comparator Filter Parameter Register for Ch2		Go
4Ch	SDDATA2	Data Filter Data Register (16 or 32bit) for Ch2		Go
50h	SDDATFIFO2	Filter Data FIFO Output(32b) for Ch2		Go
54h	SDCDATA2	Comparator Filter Data Register (16b) for Ch2		Go
56h	SDFLT2CMPH2	Second high level threhold for CH2		Go
58h	SDFLT2CMPHZ	High-level (Z) Threshold Register for Ch2		Go
5Ah	SDFIFOCTL2	FIFO Control Register for Ch2		Go
5Ch	SDSYNC2	SD Filter Sync control for Ch2		Go
5Eh	SDFLT2CMPL2	Second low level threhold for CH2		Go
60h	SDCTLPARM3	Control Parameter Register for Ch3		Go
62h	SDDFPARM3	Data Filter Parameter Register for Ch3		Go
64h	SDDPARM3	Data Parameter Register for Ch3		Go
66h	SDFLT3CMPH1	High-level Threshold Register for Ch3		Go
68h	SDFLT3CMPL1	Low-level Threshold Register for Ch3		Go
6Ah	SDCPARM3	Comparator Filter Parameter Register for Ch3		Go

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Table 27-10. SDFM_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
6Ch	SDDATA3	Data Filter Data Register (16 or 32bit) for Ch3		Go
70h	SDDATFIFO3	Filter Data FIFO Output(32b) for Ch3		Go
74h	SDCDATA3	Comparator Filter Data Register (16b) for Ch3		Go
76h	SDFLT3CMPH2	Second high level threhold for CH3		Go
78h	SDFLT3CMPHZ	High-level (Z) Threshold Register for Ch3		Go
7Ah	SDFIFOCTL3	FIFO Control Register for Ch3		Go
7Ch	SDSYNC3	SD Filter Sync control for Ch3		Go
7Eh	SDFLT3CMPL2	Second low level threhold for CH3		Go
80h	SDCTLPARM4	Control Parameter Register for Ch4		Go
82h	SDDFPARM4	Data Filter Parameter Register for Ch4		Go
84h	SDDPARM4	Data Parameter Register for Ch4		Go
86h	SDFLT4CMPH1	High-level Threshold Register for Ch4		Go
88h	SDFLT4CMPL1	Low-level Threshold Register for Ch4		Go
8Ah	SDCPARM4	Comparator Filter Parameter Register for Ch4		Go
8Ch	SDDATA4	Data Filter Data Register (16 or 32bit) for Ch4		Go
90h	SDDATFIFO4	Filter Data FIFO Output(32b) for Ch4		Go
94h	SDCDATA4	Comparator Filter Data Register (16b) for Ch4		Go
96h	SDFLT4CMPH2	Second high level threhold for CH4		Go
98h	SDFLT4CMPHZ	High-level (Z) Threshold Register for Ch4		Go
9Ah	SDFIFOCTL4	FIFO Control Register for Ch4		Go
9Ch	SDSYNC4	SD Filter Sync control for Ch4		Go
9Eh	SDFLT4CMPL2	Second low level threhold for CH4		Go
C0h	SDCOMP1CTL	SD Comparator event filter1 Control Register		Go
C2h	SDCOMP1EVT2FLTCTL	COMPL/CEVT2 Digital filter1 Control Register		Go
C4h	SDCOMP1EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter1 Clock Control Register		Go
C6h	SDCOMP1EVT1FLTCTL	COMPH/CEVT1 Digital filter1 Control Register		Go
C8h	SDCOMP1EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter1 Clock Control Register		Go
CEh	SDCOMP1LOCK	SD compartor event filter1 Lock Register		Go
D0h	SDCOMP2CTL	SD Comparator event filter2 Control Register		Go
D2h	SDCOMP2EVT2FLTCTL	COMPL/CEVT2 Digital filter2 Control Register		Go
D4h	SDCOMP2EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter2 Clock Control Register		Go
D6h	SDCOMP2EVT1FLTCTL	COMPH/CEVT1 Digital filter2 Control Register		Go
D8h	SDCOMP2EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter2 Clock Control Register		Go
DEh	SDCOMP2LOCK	SD compartor event filter2 Lock Register		Go
E0h	SDCOMP3CTL	SD Comparator event filter3 Control Register		Go
E2h	SDCOMP3EVT2FLTCTL	COMPL/CEVT2 Digital filter3 Control Register		Go
E4h	SDCOMP3EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter3 Clock Control Register		Go
E6h	SDCOMP3EVT1FLTCTL	COMPH/CEVT1 Digital filter3 Control Register		Go
E8h	SDCOMP3EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter3 Clock Control Register		Go
EEh	SDCOMP3LOCK	SD compartor event filter3 Lock Register		Go
F0h	SDCOMP4CTL	SD Comparator event filter4 Control Register		Go

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Table 27-10. SDFM_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
F2h	SDCOMP4EVT2FLTCTL	COMPL/CEVT2 Digital filter4 Control Register		Go
F4h	SDCOMP4EVT2FLTCLKCTL	COMPL/CEVT2 Digital filter4 Clock Control Register		Go
F6h	SDCOMP4EVT1FLTCTL	COMPH/CEVT1 Digital filter4 Control Register		Go
F8h	SDCOMP4EVT1FLTCLKCTL	COMPH/CEVT1 Digital filter4 Clock Control Register		Go
FEh	SDCOMP4LOCK	SD compartor event filter4 Lock Register		Go

Complex bit access types are encoded to fit into small table cells. Table 27-11 shows the codes that are used for access types in this section.

Table 27-11. SDFM_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 SDIFLG Register (Offset = 0h) [Reset = 00000000h]

SDIFLG is shown in Figure 27-12 and described in Table 27-12.

Return to the Summary Table.

SD Interrupt Flag Register

Figure 27-12. SDIFLG Register

31	30	29	28	27	26	25	24
MIF	RESERVED						
R-0h	R-0-0h						
23	22	21	20	19	18	17	16
SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 27-13. SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R	0h	Set whenever any 'error' interrupt (MF1-4,IFL1-4,IFH1-4,SDFFOVF1-4) is active Reset type: SYSRSn
30-24	RESERVED	R-0	0h	Reserved
23	SDFFINT4	R	0h	SDFIFO data ready interrupt for Ch4 Reset type: SYSRSn
22	SDFFINT3	R	0h	SDFIFO data ready interrupt for Ch3 Reset type: SYSRSn
21	SDFFINT2	R	0h	SDFIFO data ready interrupt for Ch2 Reset type: SYSRSn
20	SDFFINT1	R	0h	SDFIFO data ready interrupt for Ch1 0: SDFIFO data ready interrupt has NOT occurred 1: SDFIFO data ready interrupt has occurred Reset type: SYSRSn
19	SDFFOVF4	R	0h	FIFO Overflow Flag for Ch4 Reset type: SYSRSn
18	SDFFOVF3	R	0h	FIFO Overflow Flag for Ch3 Reset type: SYSRSn
17	SDFFOVF2	R	0h	FIFO Overflow Flag for Ch2 Reset type: SYSRSn

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Table 27-13. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SDFFOVF1	R	0h	FIFO Overflow Flag for Ch1 0 - FIFO has not overflowed 1 - FIFO overflowed. # words received in FIFO > FIFO depth (16), NEW word is lost Reset type: SYSRSn
15	AF4	R	0h	Acknowledge flag for Filter 4 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode) Reset type: SYSRSn
14	AF3	R	0h	Acknowledge flag for Filter 3 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode) Reset type: SYSRSn
13	AF2	R	0h	Acknowledge flag for Filter 2 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode) Reset type: SYSRSn
12	AF1	R	0h	Acknowledge flag for Filter 1 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode) Reset type: SYSRSn
11	MF4	R	0h	Modulator Failure for Filter 4 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset type: SYSRSn
10	MF3	R	0h	Modulator Failure for Filter 3 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset type: SYSRSn
9	MF2	R	0h	Modulator Failure for Filter 2 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset type: SYSRSn
8	MF1	R	0h	Modulator Failure for Filter 1 0: Modulator is operating normally for Filter 1: Modulator failure for Filter Reset type: SYSRSn
7	FLT4_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter4 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset type: SYSRSn
6	FLT4_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter4 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset type: SYSRSn

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Table 27-13. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FLT3_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter3 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset type: SYSRSn
4	FLT3_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter3 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset type: SYSRSn
3	FLT2_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter2 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset type: SYSRSn
2	FLT2_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter2 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset type: SYSRSn
1	FLT1_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter1 0: CEVT2 event has not occured 1: CEVT2 event has occurred Reset type: SYSRSn
0	FLT1_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter1 0: CEVT1 event has not occured 1: CEVT1 event has occurred Reset type: SYSRSn

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2 SDIFLGCLR Register (Offset = 4h) [Reset = 00000000h]

SDIFLGCLR is shown in Figure 27-13 and described in Table 27-13.

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SD Module Interrupt Flag Clear Bits:
Writing a '1' will clear the respective flag bit in the SDIFLG register.
Writes of '0' are ignored.
Note: If user writes a '1' to clear a bit on the same cycle that the hardware is trying to set the bit to '1', then hardware has priority and the bit will not be cleared.

Figure 27-13. SDIFLGCLR Register

31	30	29	28	27	26	25	24
MIF	RESERVED						
R-0/W1S-0h	R-0-0h						
23	22	21	20	19	18	17	16
SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h
7	6	5	4	3	2	1	0
FLT4_FLG_CE VT2	FLT4_FLG_CE VT1	FLT3_FLG_CE VT2	FLT3_FLG_CE VT1	FLT2_FLG_CE VT2	FLT2_FLG_CE VT1	FLT1_FLG_CE VT2	FLT1_FLG_CE VT1
R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 27-15. SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R-0/W1S	0h	Flag-clear bit for SDFM Master Interrupt flag. Writing a 1 to clear MIF flag in SDIFLG register Writes of '0' are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted (pulsed low) Reset type: SYSRSn
30-24	RESERVED	R-0	0h	Reserved
23	SDFFINT4	R-0/W1S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch4 Reset type: SYSRSn
22	SDFFINT3	R-0/W1S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch3 Reset type: SYSRSn
21	SDFFINT2	R-0/W1S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch2 Reset type: SYSRSn
20	SDFFINT1	R-0/W1S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch1 Reset type: SYSRSn
19	SDFFOVF4	R-0/W1S	0h	SDFIFO overflow clear Ch4 Reset type: SYSRSn
18	SDFFOVF3	R-0/W1S	0h	SDFIFO overflow clear Ch3 Reset type: SYSRSn

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Table 27-15. SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	SDFFOVF2	R-0/W1S	0h	SDFIFO overflow clear Ch2 Reset type: SYSRSn
16	SDFFOVF1	R-0/W1S	0h	SDFIFO overflow clear Ch1 Reset type: SYSRSn
15	AF4	R-0/W1S	0h	Flag-clear bit for Acknowledge flag for Filter 4 Reset type: SYSRSn
14	AF3	R-0/W1S	0h	Flag Clear bit for AF3 Reset type: SYSRSn
13	AF2	R-0/W1S	0h	Flag Clear bit for AF2 Reset type: SYSRSn
12	AF1	R-0/W1S	0h	Flag Clear bit for AF1 Reset type: SYSRSn
11	MF4	R-0/W1S	0h	Flag Clear bit for MF4 Reset type: SYSRSn
10	MF3	R-0/W1S	0h	Flag Clear bit for MF3 Reset type: SYSRSn
9	MF2	R-0/W1S	0h	Flag Clear bit for MF2 Reset type: SYSRSn
8	MF1	R-0/W1S	0h	Flag Clear bit for MF1 Reset type: SYSRSn
7	FLT4_FLG_CEVT2	R-0/W1S	0h	Flag Clear bit for FLT4_FLG_CEVT2 Reset type: SYSRSn
6	FLT4_FLG_CEVT1	R-0/W1S	0h	Flag Clear bit for FLT4_FLG_CEVT1 Reset type: SYSRSn
5	FLT3_FLG_CEVT2	R-0/W1S	0h	Flag Clear bit for FLT3_FLG_CEVT2 Reset type: SYSRSn
4	FLT3_FLG_CEVT1	R-0/W1S	0h	Flag Clear bit for FLT3_FLG_CEVT1 Reset type: SYSRSn
3	FLT2_FLG_CEVT2	R-0/W1S	0h	Flag Clear bit for FLT2_FLG_CEVT2 Reset type: SYSRSn
2	FLT2_FLG_CEVT1	R-0/W1S	0h	Flag Clear bit for FLT2_FLG_CEVT1 Reset type: SYSRSn
1	FLT1_FLG_CEVT2	R-0/W1S	0h	Flag Clear bit for FLT1_FLG_CEVT2 Reset type: SYSRSn
0	FLT1_FLG_CEVT1	R-0/W1S	0h	Flag Clear bit for FLT1_FLG_CEVT1 Reset type: SYSRSn

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3 SDCTL Register (Offset = 8h) [Reset = 0000h]

SDCTL is shown in Figure 27-14 and described in Table 27-14.

Return to the Summary Table.

SD Control Register

Figure 27-14. SDCTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	MIE	RESERVED				
R-0-0h	R-0-0h	R/W-0h	R-0-0h				
7	6	5	4	3	2	1	0
RESERVED				HZ4	HZ3	HZ2	HZ1
R-0-0h				R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 27-17. SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14	RESERVED	R-0	0h	Reserved
13	MIE	R/W	0h	Master SDy_ERR interrupt enable 0: SDy_ERR Interrupt and interrupt flags are disabled 1: SDy_ERR Interrupt and interrupt flags are enabled Reset type: SYSRSn
12-4	RESERVED	R-0	0h	Reserved
3	HZ4	R-0/W1S	0h	Flag Clear bit for HZ4 Reset type: SYSRSn
2	HZ3	R-0/W1S	0h	Flag Clear bit for HZ3 Reset type: SYSRSn
1	HZ2	R-0/W1S	0h	Flag Clear bit for HZ2 Reset type: SYSRSn
0	HZ1	R-0/W1S	0h	Flag Clear bit for HZ1 Reset type: SYSRSn

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4 SDMFILEN Register (Offset = Ch) [Reset = 0000h]

SDMFILEN is shown in Figure 27-15 and described in Table 27-15.

Return to the Summary Table.

SD Master Filter Enable

Figure 27-15. SDMFILEN Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED	MFE	RESERVED	RESERVED	RESERVED
R-0-0h			R-0-0h	R/W-0h	R-0-0h	R-0-0h	R-0-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED			RESERVED			
R-0-0h	R-0-0h			R-0-0h			

Table 27-19. SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R-0	0h	Reserved
12	RESERVED	R-0	0h	Reserved
11	MFE	R/W	0h	Master Filter Enable 0: All the four data filter units of SDFM module are disabled. All FIFOs are cleared 1: Data filter units can be enabled if bit FEN is '1'. Reset type: SYSRSn
10	RESERVED	R-0	0h	Reserved
9	RESERVED	R-0	0h	Reserved
8-7	RESERVED	R-0	0h	Reserved
6-4	RESERVED	R-0	0h	Reserved
3-0	RESERVED	R-0	0h	Reserved

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5 SDSTATUS Register (Offset = Eh) [Reset = 0000h]

SDSTATUS is shown in Figure 27-16 and described in Table 27-16.

Return to the Summary Table.

SD Status Register

Figure 27-16. SDSTATUS Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED				HZ4	HZ3	HZ2	HZ1
R-0-0h				R-0h	R-0h	R-0h	R-0h

Table 27-21. SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-4	RESERVED	R-0	0h	Reserved
3	HZ4	R	0h	High-level Threshold crossing (Z) flag Ch4 Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output < SDCMPHZ4.HLTZ 1: Comparator filter output >= SDCMPHZ4.HLTZ Reset type: SYSRSn
2	HZ3	R	0h	High-level Threshold crossing (Z) flag Ch3 Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output < SDCMPHZ3.HLTZ 1: Comparator filter output >= SDCMPHZ3.HLTZ Reset type: SYSRSn
1	HZ2	R	0h	High-level Threshold crossing (Z) flag Ch2 Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output < SDCMPHZ2.HLTZ 1: Comparator filter output >= SDCMPHZ2.HLTZ Reset type: SYSRSn

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Table 27-21. SDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HZ1	R	0h	High-level Threshold crossing (Z) flag Ch1 Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output < SDCMPHZ1.HLTZ 1: Comparator filter output >= SDCMPHZ1.HLTZ Reset type: SYSRSn

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6 SDINTMODE Register (Offset = 10h) [Reset = 0000h]

SDINTMODE is shown in Figure 27-17 and described in Table 27-17.

Return to the Summary Table.

SD Interrupt Mode register

Figure 27-17. SDINTMODE Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SDINTMODESEL
R-0h							R/W-0h

Table 27-23. SDINTMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	SDINTMODESEL	R/W	0h	CompxH/L events interrupt mode select 0 CompxH/L events are treated as edge signals, rise-edge detect will be done to qualify the event for interrupt generation 1 CompxH/L events are treated as level signals. Rise-edge detect will not be performed and interrupt will be re-asserted if the event remains asserted. Reset type: SYSRSn

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7 SDCTLPARM1 Register (Offset = 20h) [Reset = 0000h]

SDCTLPARM1 is shown in Figure 27-18 and described in Table 27-18.

Return to the Summary Table.

Control Parameter Register for Ch1

Figure 27-18. SDCTLPARM1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 27-25. SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R-0	0h	Reserved
7	RESERVED	R-0	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset type: SYSRSn
3	SDCLKSEL	R/W	0h	SD1 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset type: SYSRSn
2	RESERVED	R/W	0h	Reserved
1-0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset type: SYSRSn

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8 SDDFPARM1 Register (Offset = 22h) [Reset = 0000h]

SDDFPARM1 is shown in Figure 27-19 and described in Table 27-19.

Return to the Summary Table.

Data Filter Parameter Register for Ch1

Figure 27-19. SDDFPARM1 Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
R-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

Table 27-27. SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset type: SYSRSn
11-10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset type: SYSRSn
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset type: SYSRSn
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset type: SYSRSn
7-0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset type: SYSRSn

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9 SDDPARM1 Register (Offset = 24h) [Reset = 0000h]

SDDPARM1 is shown in Figure 27-20 and described in Table 27-20.

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Data Parameter Register for Ch1

Figure 27-20. SDDPARM1 Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
R/W-0h					R/W-0h	R-0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0-0h							

Table 27-29. SDDPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset type: SYSRSn
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset type: SYSRSn
9-0	RESERVED	R-0	0h	Reserved

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10 SDFLT1CMPH1 Register (Offset = 26h) [Reset = 7FFFh]

SDFLT1CMPH1 is shown in Figure 27-21 and described in Table 27-21.

Return to the Summary Table.

High-level Threshold Register for Ch1

Figure 27-21. SDFLT1CMPH1 Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT							
R/W-7FFFh							

Table 27-31. SDFLT1CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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11 SDFLT1CMPL1 Register (Offset = 28h) [Reset = 0000h]

SDFLT1CMPL1 is shown in Figure 27-22 and described in Table 27-22.

Return to the Summary Table.

Low-level Threshold Register for Ch1

Figure 27-22. SDFLT1CMPL1 Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT							
R/W-0h							

Table 27-33. SDFLT1CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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12 SDCPARM1 Register (Offset = 2Ah) [Reset = 2000h]

SDCPARM1 is shown in Figure 27-23 and described in Table 27-23.

Return to the Summary Table.

Comparator Filter Parameter Register for Ch1

Figure 27-23. SDCPARM1 Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

Table 27-35. SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
13	CEN	R/W	1h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset type: SYSRSn
12-11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
10	HZEN	R/W	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing Reset type: SYSRSn
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset type: SYSRSn
8-7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset type: SYSRSn
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset type: SYSRSn

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Table 27-35. SDCPARM1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset type: SYSRSn
4-0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset type: SYSRSn

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13 SDDATA1 Register (Offset = 2Ch) [Reset = 00000000h]

SDDATA1 is shown in Figure 27-24 and described in Table 27-24.

Return to the Summary Table.

Data Filter Data Register (16 or 32bit) for Ch1

Figure 27-24. SDDATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-37. SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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14 SDDATFIFO1 Register (Offset = 30h) [Reset = 00000000h]

SDDATFIFO1 is shown in Figure 27-25 and described in Table 27-25.

Return to the Summary Table.

Filter Data FIFO Output(32b) for Ch1

Figure 27-25. SDDATFIFO1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-39. SDDATFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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15 SDCDATA1 Register (Offset = 34h) [Reset = 0000h]

SDCDATA1 is shown in Figure 27-26 and described in Table 27-26.

Return to the Summary Table.

Comparator Filter Data Register (16b) for Ch1

Figure 27-26. SDCDATA1 Register

15	14	13	12	11	10	9	8
DATA16							
R-0h							
7	6	5	4	3	2	1	0
DATA16							
R-0h							

Table 27-41. SDCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DATA16	R	0h	Comparator Data output - 16b only Reset type: SYSRSn

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16 SDFLT1CMPH2 Register (Offset = 36h) [Reset = 7FFFh]

SDFLT1CMPH2 is shown in Figure 27-27 and described in Table 27-27.

Return to the Summary Table.

Second high level threhold for CH1

Figure 27-27. SDFLT1CMPH2 Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT2							
R/W-7FFFh							

Table 27-43. SDFLT1CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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17 SDFLT1CMPHZ Register (Offset = 38h) [Reset = 0000h]

SDFLT1CMPHZ is shown in Figure 27-28 and described in Table 27-28.

Return to the Summary Table.

High-level (Z) Threshold Register for Ch1

Figure 27-28. SDFLT1CMPHZ Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W-0h							

Table 27-45. SDFLT1CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLTZ	R/W	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset type: SYSRSn

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18 SDFIFOCTL1 Register (Offset = 3Ah) [Reset = 0000h]

SDFIFOCTL1 is shown in Figure 27-29 and described in Table 27-29.

Return to the Summary Table.

FIFO Control Register for Ch1

Figure 27-29. SDFIFOCTL1 Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0-0h	R-0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
R-0h		R-0-0h	R/W-0h				

Table 27-47. SDFIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset type: SYSRSn
14	DRINTSEL	R/W	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt) Reset type: SYSRSn
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset type: SYSRSn
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset type: SYSRSn
11	RESERVED	R-0	0h	Reserved
10-6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4-0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) >= FIFO level (SDFFIL) Reset type: SYSRSn

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19 SDSYNC1 Register (Offset = 3Ch) [Reset = 043Fh]

SDSYNC1 is shown in Figure 27-30 and described in Table 27-30.

Return to the Summary Table.

SD Filter Sync control for Ch1

Figure 27-30. SDSYNC1 Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R-0-0h					R/W-1h	R/W-0h	R-0/W-0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R-0h	R/W-0h	R/W-3Fh					

Table 27-49. SDSYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT Reset type: SYSRSn
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset type: SYSRSn
8	WTSYNCLR	R-0/W	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset type: SYSRSn
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset type: SYSRSn
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset type: SYSRSn
5-0	SYNCSEL	R/W	3Fh	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset type: SYSRSn

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20 SDFLT1CMPL2 Register (Offset = 3Eh) [Reset = 0000h]

SDFLT1CMPL2 is shown in Figure 27-31 and described in Table 27-31.

Return to the Summary Table.

Second low level threhold for CH1

Figure 27-31. SDFLT1CMPL2 Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT2							
R/W-0h							

Table 27-51. SDFLT1CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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21 SDCTLPARM2 Register (Offset = 40h) [Reset = 0000h]

SDCTLPARM2 is shown in Figure 27-32 and described in Table 27-32.

Return to the Summary Table.

Control Parameter Register for Ch2

Figure 27-32. SDCTLPARM2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 27-53. SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RESERVED	R-0	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset type: SYSRSn
3	SDCLKSEL	R/W	0h	SD2 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset type: SYSRSn
2	RESERVED	R/W	0h	Reserved
1-0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset type: SYSRSn

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22 SDDFPARM2 Register (Offset = 42h) [Reset = 0000h]

SDDFPARM2 is shown in Figure 27-33 and described in Table 27-33.

Return to the Summary Table.

Data Filter Parameter Register for Ch2

Figure 27-33. SDDFPARM2 Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
R-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

Table 27-55. SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset type: SYSRSn
11-10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset type: SYSRSn
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset type: SYSRSn
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset type: SYSRSn
7-0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset type: SYSRSn

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23 SDDPARM2 Register (Offset = 44h) [Reset = 0000h]

SDDPARM2 is shown in Figure 27-34 and described in Table 27-34.

Return to the Summary Table.

Data Parameter Register for Ch2

Figure 27-34. SDDPARM2 Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
R/W-0h					R/W-0h	R-0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0-0h							

Table 27-57. SDDPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset type: SYSRSn
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset type: SYSRSn
9-0	RESERVED	R-0	0h	Reserved

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24 SDFLT2CMPH1 Register (Offset = 46h) [Reset = 7FFFh]

SDFLT2CMPH1 is shown in Figure 27-35 and described in Table 27-35.

Return to the Summary Table.

High-level Threshold Register for Ch2

Figure 27-35. SDFLT2CMPH1 Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT							
R/W-7FFFh							

Table 27-59. SDFLT2CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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25 SDFLT2CMPL1 Register (Offset = 48h) [Reset = 0000h]

SDFLT2CMPL1 is shown in Figure 27-36 and described in Table 27-36.

Return to the Summary Table.

Low-level Threshold Register for Ch2

Figure 27-36. SDFLT2CMPL1 Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT							
R/W-0h							

Table 27-61. SDFLT2CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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26 SDCPARM2 Register (Offset = 4Ah) [Reset = 2000h]

SDCPARM2 is shown in Figure 27-37 and described in Table 27-37.

Return to the Summary Table.

Comparator Filter Parameter Register for Ch2

Figure 27-37. SDCPARM2 Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

Table 27-63. SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
13	CEN	R/W	1h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset type: SYSRSn
12-11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
10	HZEN	R/W	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing Reset type: SYSRSn
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset type: SYSRSn
8-7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset type: SYSRSn
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset type: SYSRSn

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Table 27-63. SDCPARM2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset type: SYSRSn
4-0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset type: SYSRSn

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27 SDDATA2 Register (Offset = 4Ch) [Reset = 00000000h]

SDDATA2 is shown in Figure 27-38 and described in Table 27-38.

Return to the Summary Table.

Data Filter Data Register (16 or 32bit) for Ch2

Figure 27-38. SDDATA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-65. SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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28 SDDATFIFO2 Register (Offset = 50h) [Reset = 00000000h]

SDDATFIFO2 is shown in Figure 27-39 and described in Table 27-39.

Return to the Summary Table.

Filter Data FIFO Output(32b) for Ch2

Figure 27-39. SDDATFIFO2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-67. SDDATFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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29 SDCDATA2 Register (Offset = 54h) [Reset = 0000h]

SDCDATA2 is shown in Figure 27-40 and described in Table 27-40.

Return to the Summary Table.

Comparator Filter Data Register (16b) for Ch2

Figure 27-40. SDCDATA2 Register

15	14	13	12	11	10	9	8
DATA16							
R-0h							
7	6	5	4	3	2	1	0
DATA16							
R-0h							

Table 27-69. SDCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DATA16	R	0h	Comparator Data output - 16b only Reset type: SYSRSn

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30 SDFLT2CMPH2 Register (Offset = 56h) [Reset = 7FFFh]

SDFLT2CMPH2 is shown in Figure 27-41 and described in Table 27-41.

Return to the Summary Table.

Second high level threhold for CH2

Figure 27-41. SDFLT2CMPH2 Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT2							
R/W-7FFFh							

Table 27-71. SDFLT2CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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31 SDFLT2CMPHZ Register (Offset = 58h) [Reset = 0000h]

SDFLT2CMPHZ is shown in Figure 27-42 and described in Table 27-42.

Return to the Summary Table.

High-level (Z) Threshold Register for Ch2

Figure 27-42. SDFLT2CMPHZ Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W-0h							

Table 27-73. SDFLT2CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLTZ	R/W	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset type: SYSRSn

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32 SDFIFOCTL2 Register (Offset = 5Ah) [Reset = 0000h]

SDFIFOCTL2 is shown in Figure 27-43 and described in Table 27-43.

Return to the Summary Table.

FIFO Control Register for Ch2

Figure 27-43. SDFIFOCTL2 Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0-0h	R-0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
R-0h		R-0-0h	R/W-0h				

Table 27-75. SDFIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset type: SYSRSn
14	DRINTSEL	R/W	0h	Data-Ready Interrupt (DRINT) source select 0 = AF2 (Select non-FIFO data-ready interrupt) 1 = SDFFINT2 (Select FIFO data-ready interrupt) Reset type: SYSRSn
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset type: SYSRSn
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset type: SYSRSn
11	RESERVED	R-0	0h	Reserved
10-6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4-0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) >= FIFO level (SDFFIL) Reset type: SYSRSn

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33 SDSYNC2 Register (Offset = 5Ch) [Reset = 043Fh]

SDSYNC2 is shown in Figure 27-44 and described in Table 27-44.

Return to the Summary Table.

SD Filter Sync control for Ch2

Figure 27-44. SDSYNC2 Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R-0-0h					R/W-1h	R/W-0h	R-0/W-0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R-0h	R/W-0h	R/W-3Fh					

Table 27-77. SDSYNC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT Reset type: SYSRSn
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset type: SYSRSn
8	WTSYNCLR	R-0/W	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset type: SYSRSn
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset type: SYSRSn
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset type: SYSRSn
5-0	SYNCSEL	R/W	3Fh	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset type: SYSRSn

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34 SDFLT2CMPL2 Register (Offset = 5Eh) [Reset = 0000h]

SDFLT2CMPL2 is shown in Figure 27-45 and described in Table 27-45.

Return to the Summary Table.

Second low level threhold for CH2

Figure 27-45. SDFLT2CMPL2 Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT2							
R/W-0h							

Table 27-79. SDFLT2CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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35 SDCTLPARM3 Register (Offset = 60h) [Reset = 0000h]

SDCTLPARM3 is shown in Figure 27-46 and described in Table 27-46.

Return to the Summary Table.

Control Parameter Register for Ch3

Figure 27-46. SDCTLPARM3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 27-81. SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RESERVED	R-0	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset type: SYSRSn
3	SDCLKSEL	R/W	0h	SD3 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset type: SYSRSn
2	RESERVED	R/W	0h	Reserved
1-0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset type: SYSRSn

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36 SDDFPARM3 Register (Offset = 62h) [Reset = 0000h]

SDDFPARM3 is shown in Figure 27-47 and described in Table 27-47.

Return to the Summary Table.

Data Filter Parameter Register for Ch3

Figure 27-47. SDDFPARM3 Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
R-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

Table 27-83. SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset type: SYSRSn
11-10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset type: SYSRSn
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset type: SYSRSn
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset type: SYSRSn
7-0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset type: SYSRSn

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37 SDDPARM3 Register (Offset = 64h) [Reset = 0000h]

SDDPARM3 is shown in Figure 27-48 and described in Table 27-48.

Return to the Summary Table.

Data Parameter Register for Ch3

Figure 27-48. SDDPARM3 Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
R/W-0h					R/W-0h	R-0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0-0h							

Table 27-85. SDDPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset type: SYSRSn
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset type: SYSRSn
9-0	RESERVED	R-0	0h	Reserved

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38 SDFLT3CMPH1 Register (Offset = 66h) [Reset = 7FFFh]

SDFLT3CMPH1 is shown in Figure 27-49 and described in Table 27-49.

Return to the Summary Table.

High-level Threshold Register for Ch3

Figure 27-49. SDFLT3CMPH1 Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT							
R/W-7FFFh							

Table 27-87. SDFLT3CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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39 SDFLT3CMPL1 Register (Offset = 68h) [Reset = 0000h]

SDFLT3CMPL1 is shown in Figure 27-50 and described in Table 27-50.

Return to the Summary Table.

Low-level Threshold Register for Ch3

Figure 27-50. SDFLT3CMPL1 Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT							
R/W-0h							

Table 27-89. SDFLT3CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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40 SDCPARM3 Register (Offset = 6Ah) [Reset = 2000h]

SDCPARM3 is shown in Figure 27-51 and described in Table 27-51.

Return to the Summary Table.

Comparator Filter Parameter Register for Ch3

Figure 27-51. SDCPARM3 Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

Table 27-91. SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
13	CEN	R/W	1h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset type: SYSRSn
12-11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
10	HZEN	R/W	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing Reset type: SYSRSn
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset type: SYSRSn
8-7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset type: SYSRSn
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset type: SYSRSn

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Table 27-91. SDCPARM3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset type: SYSRSn
4-0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset type: SYSRSn

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41 SDDATA3 Register (Offset = 6Ch) [Reset = 00000000h]

SDDATA3 is shown in Figure 27-52 and described in Table 27-52.

Return to the Summary Table.

Data Filter Data Register (16 or 32bit) for Ch3

Figure 27-52. SDDATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-93. SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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42 SDDATFIFO3 Register (Offset = 70h) [Reset = 00000000h]

SDDATFIFO3 is shown in Figure 27-53 and described in Table 27-53.

Return to the Summary Table.

Filter Data FIFO Output(32b) for Ch3

Figure 27-53. SDDATFIFO3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-95. SDDATFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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43 SDCDATA3 Register (Offset = 74h) [Reset = 0000h]

SDCDATA3 is shown in Figure 27-54 and described in Table 27-54.

Return to the Summary Table.

Comparator Filter Data Register (16b) for Ch3

Figure 27-54. SDCDATA3 Register

15	14	13	12	11	10	9	8
DATA16							
R-0h							
7	6	5	4	3	2	1	0
DATA16							
R-0h							

Table 27-97. SDCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DATA16	R	0h	Comparator Data output - 16b only Reset type: SYSRSn

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44 SDFLT3CMPH2 Register (Offset = 76h) [Reset = 7FFFh]

SDFLT3CMPH2 is shown in Figure 27-55 and described in Table 27-55.

Return to the Summary Table.

Second high level threhold for CH3

Figure 27-55. SDFLT3CMPH2 Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT2							
R/W-7FFFh							

Table 27-99. SDFLT3CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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45 SDFLT3CMPHZ Register (Offset = 78h) [Reset = 0000h]

SDFLT3CMPHZ is shown in Figure 27-56 and described in Table 27-56.

Return to the Summary Table.

High-level (Z) Threshold Register for Ch3

Figure 27-56. SDFLT3CMPHZ Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W-0h							

Table 27-101. SDFLT3CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLTZ	R/W	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset type: SYSRSn

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46 SDFIFOCTL3 Register (Offset = 7Ah) [Reset = 0000h]

SDFIFOCTL3 is shown in Figure 27-57 and described in Table 27-57.

Return to the Summary Table.

FIFO Control Register for Ch3

Figure 27-57. SDFIFOCTL3 Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0-0h	R-0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
R-0h		R-0-0h	R/W-0h				

Table 27-103. SDFIFOCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset type: SYSRSn
14	DRINTSEL	R/W	0h	Data-Ready Interrupt (DRINT) source select 0 = AF3 (Select non-FIFO data-ready interrupt) 1 = SDFFINT3 (Select FIFO data-ready interrupt) Reset type: SYSRSn
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset type: SYSRSn
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset type: SYSRSn
11	RESERVED	R-0	0h	Reserved
10-6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4-0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) >= FIFO level (SDFFIL) Reset type: SYSRSn

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47 SDSYNC3 Register (Offset = 7Ch) [Reset = 043Fh]

SDSYNC3 is shown in Figure 27-58 and described in Table 27-58.

Return to the Summary Table.

SD Filter Sync control for Ch3

Figure 27-58. SDSYNC3 Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R-0-0h					R/W-1h	R/W-0h	R-0/W-0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R-0h	R/W-0h	R/W-3Fh					

Table 27-105. SDSYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT Reset type: SYSRSn
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset type: SYSRSn
8	WTSYNCLR	R-0/W	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset type: SYSRSn
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset type: SYSRSn
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset type: SYSRSn
5-0	SYNCSEL	R/W	3Fh	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset type: SYSRSn

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48 SDFLT3CMPL2 Register (Offset = 7Eh) [Reset = 0000h]

SDFLT3CMPL2 is shown in Figure 27-59 and described in Table 27-59.

Return to the Summary Table.

Second low level threhold for CH3

Figure 27-59. SDFLT3CMPL2 Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT2							
R/W-0h							

Table 27-107. SDFLT3CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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49 SDCTLPARM4 Register (Offset = 80h) [Reset = 0000h]

SDCTLPARM4 is shown in Figure 27-60 and described in Table 27-60.

Return to the Summary Table.

Control Parameter Register for Ch4

Figure 27-60. SDCTLPARM4 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	SDDATASYNC	RESERVED	SDCLKSYNC	SDCLKSEL	RESERVED	MOD	
R-0-0h	R/W-0h	R-0-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

Table 27-109. SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	RESERVED	R-0	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer. Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer. Reset type: SYSRSn
3	SDCLKSEL	R/W	0h	SD4 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock. Reset type: SYSRSn
2	RESERVED	R/W	0h	Reserved
1-0	MOD	R/W	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved Reset type: SYSRSn

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50 SDDFPARM4 Register (Offset = 82h) [Reset = 0000h]

SDDFPARM4 is shown in Figure 27-61 and described in Table 27-61.

Return to the Summary Table.

Data Filter Parameter Register for Ch4

Figure 27-61. SDDFPARM4 Register

15	14	13	12	11	10	9	8
RESERVED			SDSYNCEN	SST		AE	FEN
R-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DOSR							
R/W-0h							

Table 27-111. SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs Reset type: SYSRSn
11-10	SST	R/W	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure Reset type: SYSRSn
9	AE	R/W	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter Reset type: SYSRSn
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO Reset type: SYSRSn
7-0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256. Reset type: SYSRSn

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51 SDDPARM4 Register (Offset = 84h) [Reset = 0000h]

SDDPARM4 is shown in Figure 27-62 and described in Table 27-62.

Return to the Summary Table.

Data Parameter Register for Ch4

Figure 27-62. SDDPARM4 Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED	
R/W-0h					R/W-0h	R-0-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0-0h							

Table 27-113. SDDPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. Reset type: SYSRSn
10	DR	R/W	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement Reset type: SYSRSn
9-0	RESERVED	R-0	0h	Reserved

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52 SDFLT4CMPH1 Register (Offset = 86h) [Reset = 7FFFh]

SDFLT4CMPH1 is shown in Figure 27-63 and described in Table 27-63.

Return to the Summary Table.

High-level Threshold Register for Ch4

Figure 27-63. SDFLT4CMPH1 Register

15	14	13	12	11	10	9	8
RESERVED	HLT						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT							
R/W-7FFFh							

Table 27-115. SDFLT4CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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53 SDFLT4CMPL1 Register (Offset = 88h) [Reset = 0000h]

SDFLT4CMPL1 is shown in Figure 27-64 and described in Table 27-64.

Return to the Summary Table.

Low-level Threshold Register for Ch4

Figure 27-64. SDFLT4CMPL1 Register

15	14	13	12	11	10	9	8
RESERVED	LLT						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT							
R/W-0h							

Table 27-117. SDFLT4CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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54 SDCPARM4 Register (Offset = 8Ah) [Reset = 2000h]

SDCPARM4 is shown in Figure 27-65 and described in Table 27-65.

Return to the Summary Table.

Comparator Filter Parameter Register for Ch4

Figure 27-65. SDCPARM4 Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W-0h		R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

Table 27-119. SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
13	CEN	R/W	1h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter Reset type: SYSRSn
12-11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2 Reset type: SYSRSn
10	HZEN	R/W	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing Reset type: SYSRSn
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag Reset type: SYSRSn
8-7	CS1_CS0	R/W	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure Reset type: SYSRSn
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt Reset type: SYSRSn

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Table 27-119. SDCPARM4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt Reset type: SYSRSn
4-0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32 Reset type: SYSRSn

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55 SDDATA4 Register (Offset = 8Ch) [Reset = 00000000h]

SDDATA4 is shown in Figure 27-66 and described in Table 27-66.

Return to the Summary Table.

Data Filter Data Register (16 or 32bit) for Ch4

Figure 27-66. SDDATA4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-121. SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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56 SDDATFIFO4 Register (Offset = 90h) [Reset = 00000000h]

SDDATFIFO4 is shown in Figure 27-67 and described in Table 27-67.

Return to the Summary Table.

Filter Data FIFO Output(32b) for Ch4

Figure 27-67. SDDATFIFO4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA32HI																DATA16															
R-0h																R-0h															

Table 27-123. SDDATFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA32HI	R	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode Reset type: SYSRSn
15-0	DATA16	R	0h	Lo-order 16b in 32b mode Reset type: SYSRSn

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57 SDCDATA4 Register (Offset = 94h) [Reset = 0000h]

SDCDATA4 is shown in Figure 27-68 and described in Table 27-68.

Return to the Summary Table.

Comparator Filter Data Register (16b) for Ch4

Figure 27-68. SDCDATA4 Register

15	14	13	12	11	10	9	8
DATA16							
R-0h							
7	6	5	4	3	2	1	0
DATA16							
R-0h							

Table 27-125. SDCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DATA16	R	0h	Comparator Data output - 16b only Reset type: SYSRSn

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58 SDFLT4CMPH2 Register (Offset = 96h) [Reset = 7FFFh]

SDFLT4CMPH2 is shown in Figure 27-69 and described in Table 27-69.

Return to the Summary Table.

Second high level threhold for CH4

Figure 27-69. SDFLT4CMPH2 Register

15	14	13	12	11	10	9	8
RESERVED	HLT2						
R-0-0h	R/W-7FFFh						
7	6	5	4	3	2	1	0
HLT2							
R/W-7FFFh							

Table 27-127. SDFLT4CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output. Reset type: SYSRSn

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59 SDFLT4CMPHZ Register (Offset = 98h) [Reset = 0000h]

SDFLT4CMPHZ is shown in Figure 27-70 and described in Table 27-70.

Return to the Summary Table.

High-level (Z) Threshold Register for Ch4

Figure 27-70. SDFLT4CMPHZ Register

15	14	13	12	11	10	9	8
RESERVED	HLTZ						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W-0h							

Table 27-129. SDFLT4CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	HLTZ	R/W	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting 'zero'-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. Reset type: SYSRSn

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60 SDFIFOCTL4 Register (Offset = 9Ah) [Reset = 0000h]

SDFIFOCTL4 is shown in Figure 27-71 and described in Table 27-71.

Return to the Summary Table.

FIFO Control Register for Ch4

Figure 27-71. SDFIFOCTL4 Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED	SDFFST		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0-0h	R-0h		
7	6	5	4	3	2	1	0
SDFFST		RESERVED	SDFFIL				
R-0h		R-0-0h	R/W-0h				

Table 27-131. SDFIFOCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR Reset type: SYSRSn
14	DRINTSEL	R/W	0h	Data-Ready Interrupt (DRINT) source select 0 = AF4 (Select non-FIFO data-ready interrupt) 1 = SDFFINT4 (Select FIFO data-ready interrupt) Reset type: SYSRSn
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared Reset type: SYSRSn
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable Reset type: SYSRSn
11	RESERVED	R-0	0h	Reserved
10-6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words Reset type: SYSRSn
5	RESERVED	R-0	0h	Reserved
4-0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) >= FIFO level (SDFFIL) Reset type: SYSRSn

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61 SDSYNC4 Register (Offset = 9Ch) [Reset = 043Fh]

SDSYNC4 is shown in Figure 27-72 and described in Table 27-72.

Return to the Summary Table.

SD Filter Sync control for Ch4

Figure 27-72. SDSYNC4 Register

15	14	13	12	11	10	9	8
RESERVED					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R-0-0h					R/W-1h	R/W-0h	R-0/W-0h
7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R-0h	R/W-0h	R/W-3Fh					

Table 27-133. SDSYNC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R-0	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT Reset type: SYSRSn
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC Reset type: SYSRSn
8	WTSYNCLR	R-0/W	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG Reset type: SYSRSn
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred. Reset type: SYSRSn
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs Reset type: SYSRSn
5-0	SYNCSEL	R/W	3Fh	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table Reset type: SYSRSn

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62 SDFLT4CMPL2 Register (Offset = 9Eh) [Reset = 0000h]

SDFLT4CMPL2 is shown in Figure 27-73 and described in Table 27-73.

Return to the Summary Table.

Second low level threhold for CH4

Figure 27-73. SDFLT4CMPL2 Register

15	14	13	12	11	10	9	8
RESERVED	LLT2						
R-0-0h	R/W-0h						
7	6	5	4	3	2	1	0
LLT2							
R/W-0h							

Table 27-135. SDFLT4CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R-0	0h	Reserved
14-0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output. Reset type: SYSRSn

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63 SDCOMP1CTL Register (Offset = C0h) [Reset = 0000h]

SDCOMP1CTL is shown in Figure 27-74 and described in Table 27-74.

Return to the Summary Table.

SD Comparator event filter1 Control Register

Figure 27-74. SDCOMP1CTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h

Table 27-137. SDCOMP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset type: SYSRSn
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset type: SYSRSn
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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64 SDCOMP1EVT2FLTCTL Register (Offset = C2h) [Reset = 0000h]

SDCOMP1EVT2FLTCTL is shown in Figure 27-75 and described in Table 27-75.

Return to the Summary Table.

COMPL/CEVT2 Digital filter1 Control Register

Figure 27-75. SDCOMP1EVT2FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-139. SDCOMP1EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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65 SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [Reset = 0000h]

SDCOMP1EVT2FLTCLKCTL is shown in Figure 27-76 and described in Table 27-76.

Return to the Summary Table.

COMPL/CEVT2 Digital filter1 Clock Control Register

Figure 27-76. SDCOMP1EVT2FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-141. SDCOMP1EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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66 SDCOMP1EVT1FLTCTL Register (Offset = C6h) [Reset = 0000h]

SDCOMP1EVT1FLTCTL is shown in Figure 27-77 and described in Table 27-77.

Return to the Summary Table.

COMPH/CEVT1 Digital filter1 Control Register

Figure 27-77. SDCOMP1EVT1FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-143. SDCOMP1EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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67 SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [Reset = 0000h]

SDCOMP1EVT1FLTCLKCTL is shown in Figure 27-78 and described in Table 27-78.

Return to the Summary Table.

COMPH/CEVT1 Digital filter1 Clock Control Register

Figure 27-78. SDCOMP1EVT1FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-145. SDCOMP1EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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68 SDCOMP1LOCK Register (Offset = CEh) [Reset = 0000h]

SDCOMP1LOCK is shown in Figure 27-79 and described in Table 27-79.

Return to the Summary Table.

SD compartor event filter1 Lock Register

Figure 27-79. SDCOMP1LOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP1CTL
R-0h			R-0h	R/WSonce-0h	R-0h	R-0h	R/WSonce-0h

Table 27-147. SDCOMP1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	COMP	R/WSonce	0h	Lock write-access to the SDCOMP1EVT1/2FLTTCTL and COMP1FILCLKCTL registers. 0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset type: SYSRSn
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	SDCOMP1CTL	R/WSonce	0h	Lock write-access to the SDCOMP1CTL register. 0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP1CTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn

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69 SDCOMP2CTL Register (Offset = D0h) [Reset = 0000h]

SDCOMP2CTL is shown in Figure 27-80 and described in Table 27-80.

Return to the Summary Table.

SD Comparator event filter2 Control Register

Figure 27-80. SDCOMP2CTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h

Table 27-149. SDCOMP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset type: SYSRSn
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset type: SYSRSn
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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70 SDCOMP2EVT2FLTCTL Register (Offset = D2h) [Reset = 0000h]

SDCOMP2EVT2FLTCTL is shown in Figure 27-81 and described in Table 27-81.

Return to the Summary Table.

COMPL/CEVT2 Digital filter2 Control Register

Figure 27-81. SDCOMP2EVT2FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-151. SDCOMP2EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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71 SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [Reset = 0000h]

SDCOMP2EVT2FLTCLKCTL is shown in Figure 27-82 and described in Table 27-82.

Return to the Summary Table.

COMPL/CEVT2 Digital filter2 Clock Control Register

Figure 27-82. SDCOMP2EVT2FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-153. SDCOMP2EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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72 SDCOMP2EVT1FLTCTL Register (Offset = D6h) [Reset = 0000h]

SDCOMP2EVT1FLTCTL is shown in Figure 27-83 and described in Table 27-83.

Return to the Summary Table.

COMPH/CEVT1 Digital filter2 Control Register

Figure 27-83. SDCOMP2EVT1FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-155. SDCOMP2EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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73 SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [Reset = 0000h]

SDCOMP2EVT1FLTCLKCTL is shown in Figure 27-84 and described in Table 27-84.

Return to the Summary Table.

COMPH/CEVT1 Digital filter2 Clock Control Register

Figure 27-84. SDCOMP2EVT1FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-157. SDCOMP2EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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74 SDCOMP2LOCK Register (Offset = DEh) [Reset = 0000h]

SDCOMP2LOCK is shown in Figure 27-85 and described in Table 27-85.

Return to the Summary Table.

SD compartor event filter2 Lock Register

Figure 27-85. SDCOMP2LOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP2CTL
R-0h			R-0h	R/WSonce-0h	R-0h	R-0h	R/WSonce-0h

Table 27-159. SDCOMP2LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	COMP	R/WSonce	0h	Lock write-access to the SDCOMP2EVT1/2FLTTCTL and COMP2FILCLKCTL registers. 0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset type: SYSRSn
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	SDCOMP2CTL	R/WSonce	0h	Lock write-access to the SDCOMP2CTL register. 0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP2CTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn

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75 SDCOMP3CTL Register (Offset = E0h) [Reset = 0000h]

SDCOMP3CTL is shown in Figure 27-86 and described in Table 27-86.

Return to the Summary Table.

SD Comparator event filter3 Control Register

Figure 27-86. SDCOMP3CTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h

Table 27-161. SDCOMP3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset type: SYSRSn
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset type: SYSRSn
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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76 SDCOMP3EVT2FLTCTL Register (Offset = E2h) [Reset = 0000h]

SDCOMP3EVT2FLTCTL is shown in Figure 27-87 and described in Table 27-87.

Return to the Summary Table.

COMPL/CEVT2 Digital filter3 Control Register

Figure 27-87. SDCOMP3EVT2FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-163. SDCOMP3EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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77 SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [Reset = 0000h]

SDCOMP3EVT2FLTCLKCTL is shown in Figure 27-88 and described in Table 27-88.

Return to the Summary Table.

COMPL/CEVT2 Digital filter3 Clock Control Register

Figure 27-88. SDCOMP3EVT2FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-165. SDCOMP3EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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78 SDCOMP3EVT1FLTCTL Register (Offset = E6h) [Reset = 0000h]

SDCOMP3EVT1FLTCTL is shown in Figure 27-89 and described in Table 27-89.

Return to the Summary Table.

COMPH/CEVT1 Digital filter3 Control Register

Figure 27-89. SDCOMP3EVT1FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-167. SDCOMP3EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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79 SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [Reset = 0000h]

SDCOMP3EVT1FLTCLKCTL is shown in Figure 27-90 and described in Table 27-90.

Return to the Summary Table.

COMPH/CEVT1 Digital filter3 Clock Control Register

Figure 27-90. SDCOMP3EVT1FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-169. SDCOMP3EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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80 SDCOMP3LOCK Register (Offset = EEh) [Reset = 0000h]

SDCOMP3LOCK is shown in Figure 27-91 and described in Table 27-91.

Return to the Summary Table.

SD compartor event filter3 Lock Register

Figure 27-91. SDCOMP3LOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP3CTL
R-0h			R-0h	R/WSonce-0h	R-0h	R-0h	R/WSonce-0h

Table 27-171. SDCOMP3LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	COMP	R/WSonce	0h	Lock write-access to the SDCOMP3EVT1/2FLTTCTL and COMP3FILCLKCTL registers. 0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset type: SYSRSn
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	SDCOMP3CTL	R/WSonce	0h	Lock write-access to the SDCOMP3CTL register. 0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP3CTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn

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81 SDCOMP4CTL Register (Offset = F0h) [Reset = 0000h]

SDCOMP4CTL is shown in Figure 27-92 and described in Table 27-92.

Return to the Summary Table.

SD Comparator event filter4 Control Register

Figure 27-92. SDCOMP4CTL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED		CEVT2DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		CEVT1DIGFILTSEL		RESERVED	RESERVED
R-0h	R-0h	R-0h		R/W-0h		R-0h	R-0h

Table 27-173. SDCOMP4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11-10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved Reset type: SYSRSn
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved Reset type: SYSRSn
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

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82 SDCOMP4EVT2FLTCTL Register (Offset = F2h) [Reset = 0000h]

SDCOMP4EVT2FLTCTL is shown in Figure 27-93 and described in Table 27-93.

Return to the Summary Table.

COMPL/CEVT2 Digital filter4 Control Register

Figure 27-93. SDCOMP4EVT2FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-175. SDCOMP4EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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83 SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [Reset = 0000h]

SDCOMP4EVT2FLTCLKCTL is shown in Figure 27-94 and described in Table 27-94.

Return to the Summary Table.

COMPL/CEVT2 Digital filter4 Clock Control Register

Figure 27-94. SDCOMP4EVT2FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-177. SDCOMP4EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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84 SDCOMP4EVT1FLTCTL Register (Offset = F6h) [Reset = 0000h]

SDCOMP4EVT1FLTCTL is shown in Figure 27-95 and described in Table 27-95.

Return to the Summary Table.

COMPH/CEVT1 Digital filter4 Control Register

Figure 27-95. SDCOMP4EVT1FLTCTL Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED	THRESH					SAMPWIN
R-0/W1S-0h	R-0h	R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
SAMPWIN				RESERVED			
R/W-0h				R-0h			

Table 27-179. SDCOMP4EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R-0/W1S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value Reset type: SYSRSn
14	RESERVED	R	0h	Reserved
13-9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Reset type: SYSRSn
8-4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1. Reset type: SYSRSn
3-0	RESERVED	R	0h	Reserved

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85 SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [Reset = 0000h]

SDCOMP4EVT1FLTCLKCTL is shown in Figure 27-96 and described in Table 27-96.

Return to the Summary Table.

COMPH/CEVT1 Digital filter4 Clock Control Register

Figure 27-96. SDCOMP4EVT1FLTCLKCTL Register

15	14	13	12	11	10	9	8
RESERVED						CLKPRESCALE	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W-0h							

Table 27-181. SDCOMP4EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples. Reset type: SYSRSn

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86 SDCOMP4LOCK Register (Offset = FEh) [Reset = 0000h]

SDCOMP4LOCK is shown in Figure 27-97 and described in Table 27-97.

Return to the Summary Table.

SD compartor event filter4 Lock Register

Figure 27-97. SDCOMP4LOCK Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	COMP	RESERVED	RESERVED	SDCOMP4CTL
R-0h			R-0h	R/WSonce-0h	R-0h	R-0h	R/WSonce-0h

Table 27-183. SDCOMP4LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	COMP	R/WSonce	0h	Lock write-access to the SDCOMP4EVT1/2FLTTCTL and COMP4FILCLKCTL registers. 0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. Reset type: SYSRSn
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	SDCOMP4CTL	R/WSonce	0h	Lock write-access to the SDCOMP4CTL register. 0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP4CTL register is locked. Only a system reset can clear this bit. Reset type: SYSRSn

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Chapter 28

EtherCAT® SubordinateDevice Controller (ESC)

This chapter describes the implementation and integration of the Ethernet for Control Automation Technology (EtherCAT®) SubordinateDevice Controller (ESC). Information about the EtherCAT standards and working principles can be in found these documents:

- EtherCAT ET1100 Data sheet
- EtherCAT ESC Hardware Data sheet (Section I)
- EtherCAT IP Core for Xilinx™ FPGAs

28.1 Introduction 2002
28.2 ESC and ESCSS Description 2012
28.3 Software Initialization Sequence and Allocating Ownership 2032
28.4 ESC Configuration Constants 2032
28.5 EtherCAT Interrupts & Triggers 2033
28.6 ESC Registers 2033

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28.1 Introduction

Ethernet for Control Automation Technology (EtherCAT®) is an Ethernet-based fieldbus system, invented by Beckhoff ® Automation and standardized in IEC 61158. All the SubordinateDevice (or SubDevice) nodes connected to the bus interpret, process, and modify the data addressed to them "on the fly", without having to buffer the frame inside the node. This real-time behavior, frame processing, and forwarding requirements are implemented by the EtherCAT SubDevice controller (ESC) hardware. EtherCAT does not require software interaction for data transmission inside the SubDevice. EtherCAT only defines the MAC layer while the higher layer protocols and stack are implemented in software on the microcontrollers connected to the ESC.

The EtherCAT:

- Involves MainDevice (or MDevice) and SubordinateDevice (SubDevice) setup where SubDevice nodes are physically connected
- Specializes in precise, low jitter synchronization across SubDevice nodes
- Uses IEEE 802.3 Ethernet physical layer and standard Ethernet frames

A list of relevant terms and definitions are listed in Table 28-1.

Table 28-1. Abbreviations

Name	Definition
CPU1	Main CPU1 subsystem on this MCU
DIGIO	Digital IO profile
ENI	EtherCAT Network Information
ESC	EtherCAT SubDevice Controller
ESCSS or SS	Subsystem (specifically referring to EtherCAT Subsystem on this device)
ESI	EtherCAT SubDevice Information
ET1100	Beckhoff EtherCAT SubDevice Controller
ETG	EtherCAT Technical Group
EtherCAT	Ethernet for Control Automation Technology
FMMU	Fieldbus Memory Management Units
HAL	Hardware Abstraction Layer
MII	Medium Independent Interface
NMIWDRS	NMI Watchdog Reset
PDI	Processor Data Interface
POR	Power-on-Reset
SSC	EtherCAT SubDevice Stack Code
SII	SubDevice Information Interface
WDRS	Watchdog Reset
XRS	External Reset

28.1.1 EtherCAT Related Collateral

Foundational Materials

- EtherCAT Device Protocol Poster
- EtherCAT Protocol Series (Video)

Expert Materials

- *EtherCAT Based Connected Servo Drive using Fast Current Loop on PMSM Application Report*
- EtherCAT Technology Group - Download Section Landing Page
- Hardware Data Sheet Section I - Technology

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- Hardware Data Sheet Section II - Register Description
- PHY Selection Guide

28.1.2 ESC Features

The ESC provides the following functionality:

- Up to 2 MII ports to connect to EtherCAT PHYs
- Process data interface (PDI) through 16-bit asynchronous interface (ASYNC16)
- 64-bit distributed clocking.
  - Sync output signals to synchronize device events and latch input signals supporting time stamping for events.
  - Distributed clock features of SYNC0/1 (o/ps) and LATCH0/1 able to synchronize GPIOs and allow inputs from any GPIOs as well as other muxing options for internal device events.
- 8 Field bus Memory Management Units (FMMUs)
  - Supports all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing
- 8 Sync Managers
- I2C EEPROM interface
- Up to 4 general-purpose inputs and 4 general-purpose outputs
- 2 SYNC and 2 LATCH signals connected to GPIO pads
- 16KB RAM with parity

28.1.3 ESC Subsystem Integrated Features

In addition to the ESC features, the following are the device-specific features provided by the integration of the ESC to the MCU:

- EtherCAT reset request from MainDevice can be routed to NMI or the NVIC
- RAM Parity error routed to NMI on MCU
- DMA access to EtherCAT RAM
- Up to 4 GPI (general-purpose inputs) and up to 4 GPO (general-purpose outputs) feature integrated in addition to 16-bit ASYNC PDI interface
- I2C internal loopback feature for EEPROM Emulation
- Distributed clock feature of SYNC0 and SYNC1 able to synchronize PWMs, generate interrupt and DMA requests, trigger ECAP capture, or allow external component action through GPIO access
- Distributed clock feature of LATCH0 and LATCH1 allowing inputs from any GPIO or PWM crossbar triggers

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28.1.4 AM13E232x ESC versus Beckhoff ET1100

Table 28-2 details a comparison between the ESC IP Core implementation and the Beckhoff's ET1100 ESC.

Table 28-2. AM13E232x ESC versus Beckhoff ET1100

Feature	AM13E232x ESC	Beckhoff ET1100
Transmission Speed	100Mbit/s	100Mbit/s
Number of Ports	2 (MII Only)	4 (MII or EBUS)
FMMUs	8	8
SyncManagers	8	8
RAM (KByte)	16KB	8KB
Distributed Clocks	Yes, 64-bit	Yes, 64-bit
EBUS Support	No	Yes
Process Data Interfaces (PDI)	16-bit ASYNC	Digital I/O SPI 8-bit ASYNC/SYNC 16-bit ASYNC/SYNC

28.1.5 EtherCAT IP Block Diagram

Figure 28-1 shows the general functionality of etherCAT IP from Beckhoff. This chapter discusses how the etherCAT IP is integrated into the MCU.

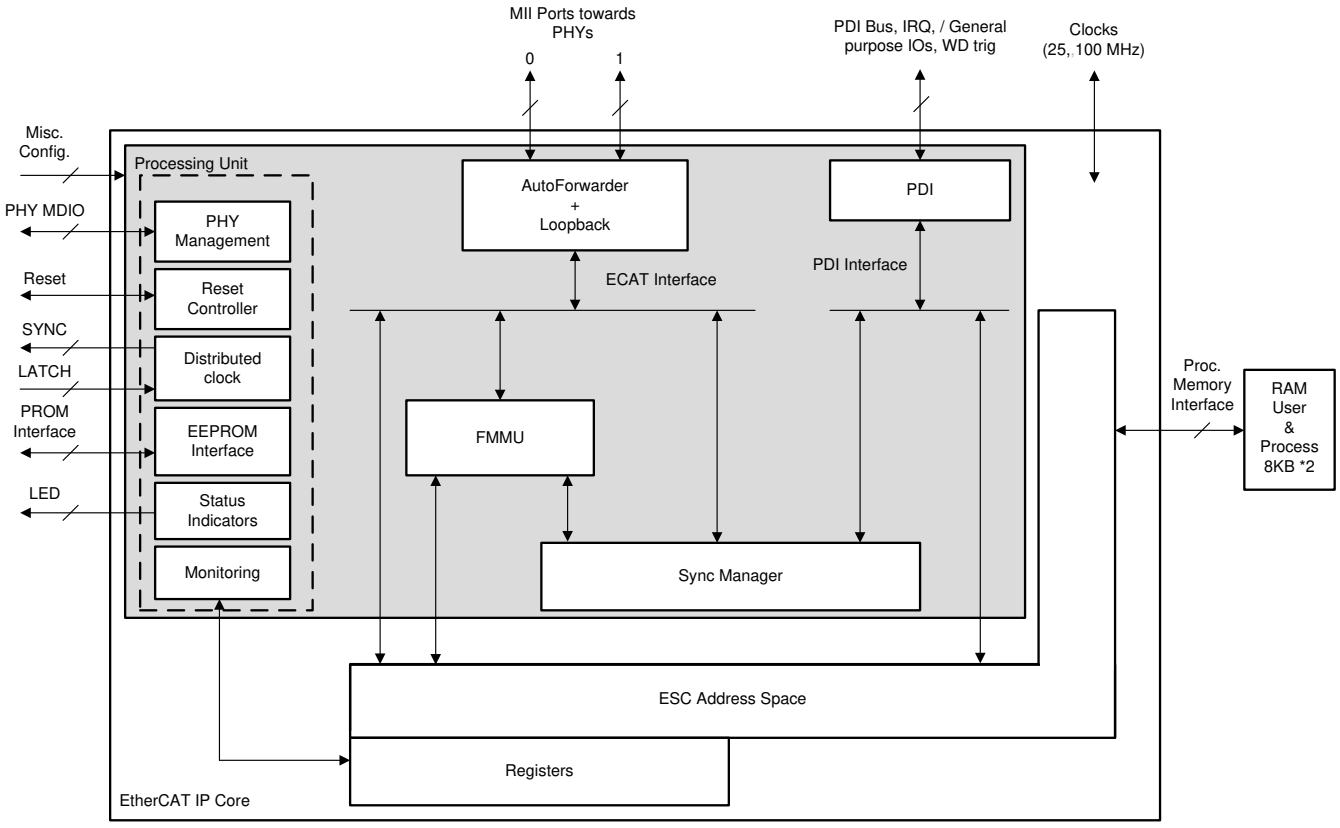


Figure 28-1. EtherCAT IP Block Diagram

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28.1.6 ESC Functional Blocks

The following introduces each of the sub-blocks. For more details, refer to the Beckhoff EtherCAT documentation.

28.1.6.1 Interface to EtherCAT MainDevice

The EtherCAT MainDevice is a remote entity normally implemented through the device with ethernet switch capability. Beckhoff suggests using either a standard ethernet physical layer interface through MII or RMII protocol, or using a low-voltage differential pair signaling with EBUS protocol. Per Beckhoff specification, up to 4 PHY ports can be supported. In this device, implementation of ESC:

- Only MII is supported for Ethernet PHY interface
- ESC supports only 2 PHY ports

28.1.6.2 Process Data Interface

Process data interface (PDI) is a connection from the ESC IP to the microcontroller and SubordinateDevice application. The implementation of the ESC supports a 16-bit asynchronous interface (ASYNC16) to the local host only.

28.1.6.3 EtherCAT Processing Unit (EPU)

The EtherCAT Processing Unit (EPU) receives, analyzes, and processes the EtherCAT data stream. The EPU is logically located between port 0 and port 1. The main purpose of the EPU is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT MainDevice and from the local application by way of the Processor Data Interface (PDI). Data exchange between the MainDevice and SubordinateDevice application is comparable to a dual-ported memory (process memory), enhanced by special functions; for example, for consistency checking (SyncManager) and data mapping (FMMU). The EPU contains the main function blocks of the EtherCAT SubordinateDevices besides Auto-Forwarding, Loop-back function, and PDI.

- **Auto-Forwarder:**
  - The Auto-forwarder function includes receiving EtherCAT frame, checksum computation and verification, timestamp capture for received frames, and forwarding to Loop-back component.
- **Loop-back Function:**
  - For the two-port implementation on this device, port 3 and port 2 are looped back by design, as shown in Figure 28-2.
  - Port 0 is a special port that is always connected to the MainDevice while designing the topology. At egress, port 0 acts as a terminal point for the network connected downstream; hence, any circulating packets get dropped at port 0 in the event of port 0 being looped-back.
  - In the event of a network or link loss downstream to the ESC port 1, the packets end in loopback.

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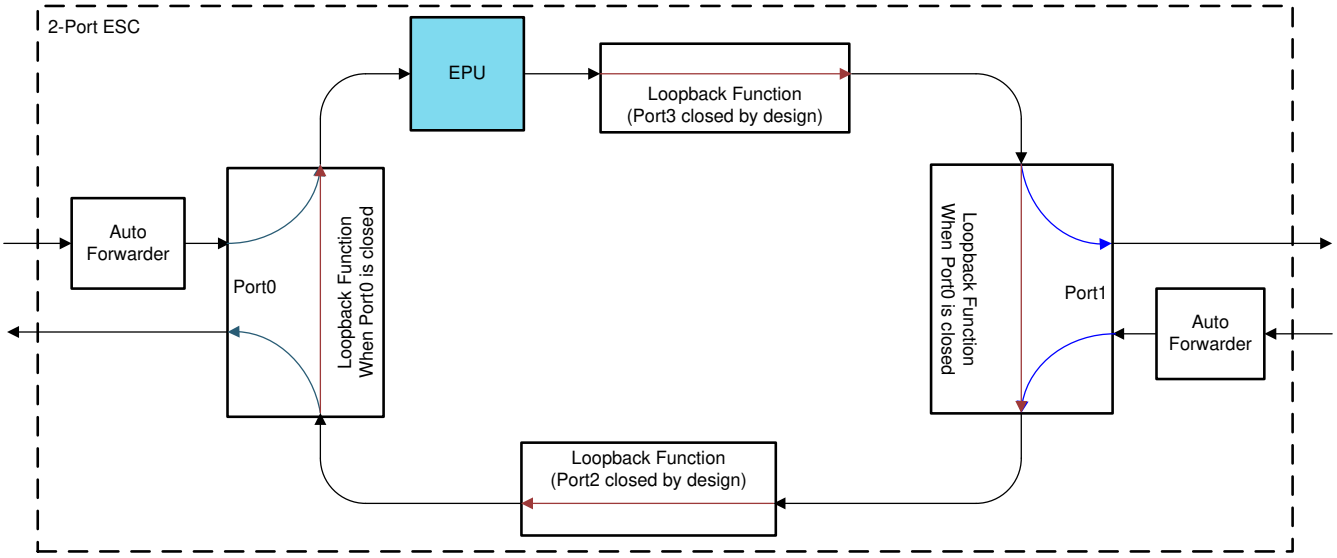


Figure 28-2. Two-port ESC Description

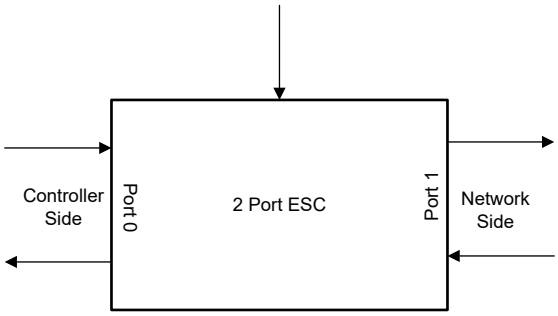


Figure 28-3. Two-port Block Diagram in EtherCAT Topology

28.1.6.4 Fieldbus Memory Management Unit (FMMU)

The fieldbus memory management unit (FMMU) maps the logical addresses of the memory elements in ESC to a physical address that allows the remote EtherCAT MainDevice to address registers and process RAM as one memory-map that can be accessed across the EtherCAT network. Mapping can be done up to bit-wise mapping.

28.1.6.5 Sync Manager

The integrity and security of the data in dual-port memory across the MainDevice and local application is maintained by the sync manager. The sync manager allows data to be accessed as buffered or mailbox, where either there is a definite read and write space or there is a sequence defined for both of the MainDevice entities.

28.1.6.6 Monitoring

The monitoring unit contains error counters and watchdogs. The watchdogs are used for observing communication and returning to a safe state in case of an error. Error counters are used for error detection and analysis.

28.1.6.7 Reset Controller

The reset controller aggregates the internal/external resets as well as asserts the reset to external pin, which can be connected to device pin to reset companion devices on the board.

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28.1.6.8 PHY Management

The PHY control is maintained through the MDIO interface that allows the configuration of the PHYs and enabling advanced features of link detection, if present.

28.1.6.9 Distributed Clock (DC)

Distributed clocks (DC) allows the tracked time at ESC be synchronized across the EtherCAT network, which makes precisely timed events possible throughout the network. Events can be realized with triggers from ESC outputs that are programmed to create a toggle at a certain absolute time tracked by the ESC or through sampling of timestamp of certain system event inputs to ESC that can further be used for synchronizing the time.

- Refer to Section 28.2.9 for more details.

28.1.6.10 EEPROM

Every ESC requires non-volatile memory to store the configuration contents of the ESI (EtherCAT SubordinateDevice Information) that are accessed by the MainDevice normally before enabling the ESC in the network. Size of the memory is configurable with a minimum of 1K bit up to 4M bit are supported depending on the ESC. This non-volatile memory is supported in simplest form by the ESC IP core as serial access EEPROM.

- For ESI EEPROM Layout and mandatory information, refer to the ESC Hardware Data Sheet Section I - Technology (ethercat_esc_datasheet_sec1_technology) document provided by Beckhoff/ETG at www.beckhoff.com.
- EEPROM is supported using the I2C interface on this device and is further explained in Section 28.2.7 .

28.1.6.11 Status / LEDs

ESC supports the status indication of application activity, link status and link errors which can be utilized for visual status indication through LEDs.

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28.1.7 EtherCAT Physical Layer

ESC devices with Ethernet Physical Layer are able to support MII interfaces, RMII interfaces, and EBUS interfaces. Since RMII PHYs include TX FIFOs, the RMII PHYs increase the packet forwarding delay of an ESC device as well as the jitter. RMII as an Ethernet Physical Layer is not supported on this device due to these reasons and therefore only the MII interface is supported.

- On this device, only MII is supported (RMII and EBUS are not supported)
- Refer to the **ESC Application Note - PHY Selection Guide (an_phy_selection_guide)** provided by Beckhoff/ETG at www.beckhoff.com for additional PHY selection details.

Table 28-3 depicts the number of pins needed for MII interface for two ports.

Table 28-3. EtherCAT Physical Layer Signals

Pin	Number of Pins for 2 Ports	MII	Direction	Description
nMII_Link	2	Yes	IN	Input signal provided by the PHY, if a 100Mbps (full duplex) link is established
RX_CLK	2	Yes	IN	Receive Clock
RX_DV	2	Yes	IN	Receive Data valid
RX_DATA[1:0]	4	Yes	IN	Receive Data
RX_DATA[3:2]	4	Yes	IN	Receive Data
RX_ERR	2	Yes	IN	Receive error
TX_CLK(1)	2	Optional	IN	Transmit Clock
TX_ENA	2	Yes	OUT	Transmit Enable
TX_DATA[1:0]	4	Yes	OUT	Transmit Data
TX_DATA[3:2]	4	Yes	OUT	Transmit Data
MCLK	1	Yes	OUT	MII Interface clock
MDIO	1	Yes	BI-Directional	MII Interface Data
Total Pins:	28 (required) + 2 (optional)			

(1) The TX_CLK signal is optional when using the TX_SHIFT register for manual compensation; however, it is recommended to route the TX_CLK signals to the MII ports for improved accuracy and to avoid the need for manual compensation.

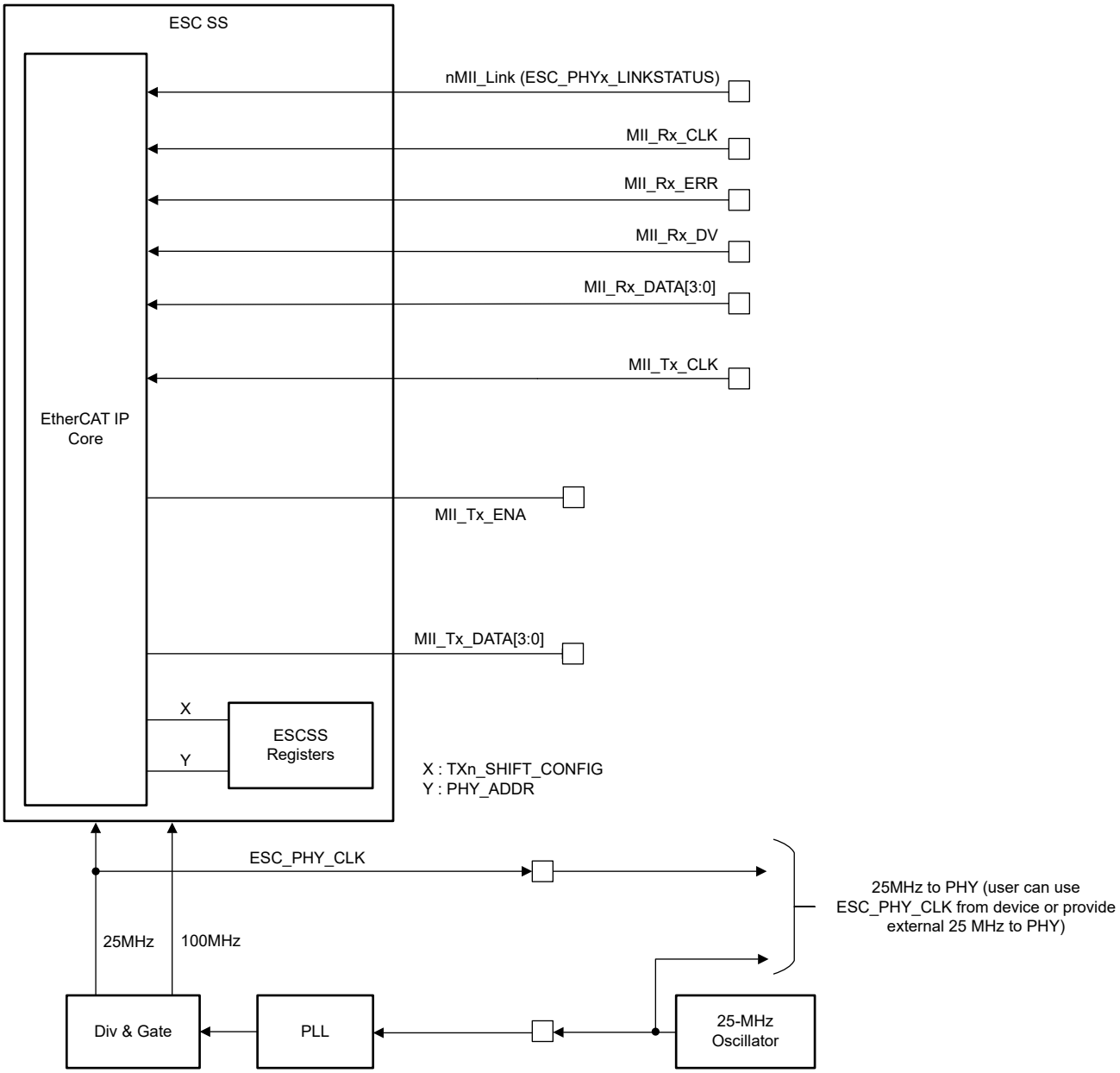
28.1.7.1 MII Interface

Ethernet IEEE802.3 specified MII interface is supported with possible minor variation in clocking to optimize the clock delay to operate the Tx FIFO. Unlike regular integration of Tx clock being sourced by the PHY, the ESC implementation allows the common source clock between PHY and ESC be used for Tx logic. The option is selected by manual Tx shift compensation which allows Tx-Data and Tx-En be compensated in steps of 10 ns to meet the timing requirements of data sampling at the PHY.

The following signals are used by the ESC to connect to an Ethernet PHY. The MDIO pins are not shown in Figure 28-4, as these pins are covered in the next section.

The MII signals TX_ERR, COL and CRS are not used by the ESC. These are not available on the MCU for EtherCAT.

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Note

Note: The PHY reset signal is also not shown in the diagram.

Figure 28-4. ESC PHY Interface Diagram

If an ESC MII interface is not used, LINK_MII has to be tied to the logic value high that indicates no link. RX_CLK, RXD, RX_ER, and especially RX_DV are connected to GND and this is taken care of by design internally when the functional IO mux for the RX pins is not configured when the IP is out of reset. The TX outputs can be left unconnected, by not configuring the Functional IO mux for respective EtherCAT functionality, unless the TX outputs are used for ESC configuration.

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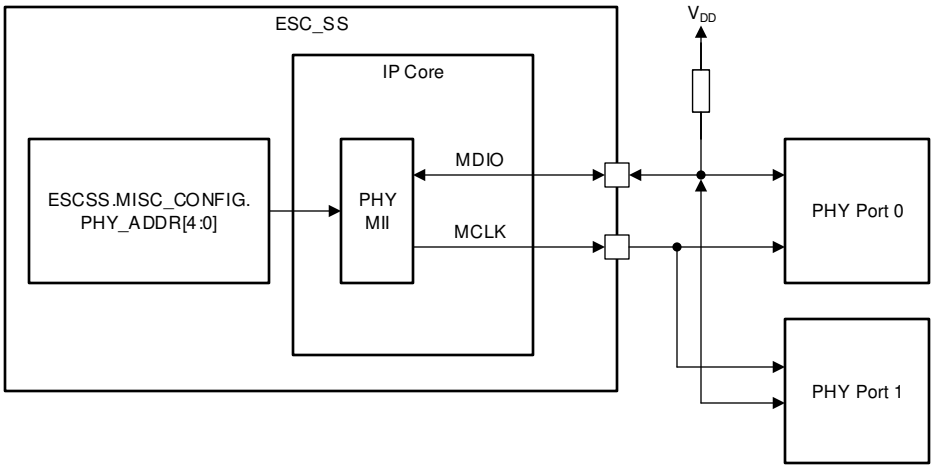
28.1.7.2 PHY Management Interface

Most ESCs with MII/RMII ports use the MII management interface for communication with the Ethernet PHYs. Most ESCs do not use the management interface for link detection or configuration of link modes. For link detection, TI recommends that the ESC use a separate signal (LINK_MII). The MII management interface can be used by the EtherCAT MainDevice – or the local MCU. Enhanced MII link detection uses the management interface for restarting auto-negotiation after communication errors occurred.

On this ESC, it is possible to make use of the MII management interface for link detection and PHY configuration.

Note

The EtherCAT link status through the MII management interface option must be enabled only if a Gigabit PHY is to be supported; the EtherCAT link must not be enabled if needing to support both 10/100 and Gigabit PHY. For this reason, the link status through the MII management interface is disabled on this ESC. Instead, use the LINKACT or PHY MII_LINK signals for link status purposes.



Note

Note: The MDIO must have a pull-up resistor (4.7 kOhm recommended) externally. MCLK is driven rail-to-rail, idle value is high.

Figure 28-5. PHY Management Interface Connectivity

28.1.7.2.1 PHY Address Configuration

The ESC typically addresses the Ethernet PHYs using the logical port number plus the PHY address offset. The Ethernet PHY addresses must correspond with the logical port number, so PHY addresses 0 and 1 are used.

A PHY address offset of 0 to 31 can be applied, which moves the PHY addresses to any consecutive address range. The ESC module expects logical port 0 to have PHY address 0 plus the PHY address offset. The PHY address offset can be selected in register ESCSS_MISC_CONFIG.PHY_ADDR[4:0].

28.1.7.2.2 PHY Reset Signal

The PHY reset signal is generated out of the ESC module. If required to release both, the PHY and ESC module synchronous out of reset, this signal can be used. Since there are no pull devices active on the MCU during and after reset, a pull down resistor must be added on this signal on the board level.

In some case, PHYs can be released from reset after releasing the ESC module. To generate a delay, the pin for nPHY_RESET can be used as an I/O and must be switched later to the alternate output function.

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28.1.7.2.3 PHY Clock

The PHY Clock connectivity is shown in Figure 28-4. On this MCU, the user has an option to clock the PHY using the ESC_PHY_CLK signal if needed; otherwise, the user can chose to provide an external 25MHz source to the PHY and ESC (both must be clocked from the same source). For more details regarding providing PHY clock, refer to Section 28.2.5.2 and see the EtherCAT data sheet from Beckhoff.

Note

Beckhoff documents strict accuracy (ppm) requirements for the shared 25MHz ESC and PHY clock. Special care must be taken within a design to make sure the EtherCAT clocking requirements are met. Relying on external components (oscillator and clock buffer) for the 25MHz source are recommended. Validation of a design during normal operating conditions can be necessary to confirm clocking requirements are adequately met, especially if using the ESC_PHY_CLK signal.

28.1.8 EtherCAT Protocol

EtherCAT uses standard IEEE 802.3 Ethernet frames, thus a standard network controller can be used and no special hardware is required on the MainDevice side. EtherCAT has a reserved EtherType of 0x88A4 that distinguishes this from other Ethernet frames. Thus, EtherCAT can run in parallel to other Ethernet protocols.

- EtherCAT does not need the IP protocol; however, the EtherCAT can be encapsulated in IP/UDP.
- The ESC processes the frame in hardware; therefore, communication performance is independent from processor power.

An EtherCAT frame is subdivided into the EtherCAT frame header followed by one or more EtherCAT datagrams. At least one EtherCAT datagram has to be in the frame. Only EtherCAT frames with Type 1 in the EtherCAT Header are currently processed by the ESCs. The ESCs also support IEEE802.1Q VLAN Tags, although the VLAN Tag contents are not evaluated by the ESC.

- If the minimum Ethernet frame size requirement is not fulfilled, padding bytes are added. Otherwise, the EtherCAT frame is exactly as large as the sum of all EtherCAT datagrams plus EtherCAT frame header.
- For further reading, including details on network time or network propagation delay, refer to the ESC Hardware Data Sheet Section I - Technology (ethercat_esc_datasheet_sec1_technology) document provided by Beckhoff/ETG at www.beckhoff.com.

28.1.9 EtherCAT State Machine (ESM)

The EtherCAT State Machine (ESM) is responsible for the coordination of the MainDevice and SubordinateDevice applications at start up and during operation. State changes are typically initiated by requests from the MainDevice. The state changes are acknowledged by the local application after the associated operations have been executed. Unsolicited state changes of the local application are also possible.

There are four states (see Figure 28-6) an ESC can support, plus one optional state:

- Initialize (Init)
- Pre-Operational
- Safe-Operational
- Operational
- Bootstrap (Optional)

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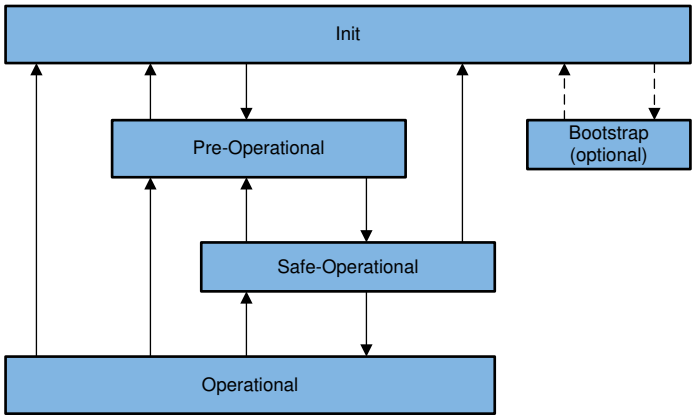


Figure 28-6. EtherCAT State Machine

Note

Not all state changes are possible, for example, the transition from Init to Operational requires the following sequence: Init → Pre-Operational → Safe-Operational → Operational.

28.1.10 More Information on EtherCAT

- For further information on EtherCAT, refer to the EtherCAT specifications, available from the EtherCAT Technology Group (ETG, www.ethercat.org).
- Refer to the IEC standard “Digital data communications for measurement and control – Fieldbus for use in industrial control systems”, IEC 61158 Type 12: EtherCAT, available from the IEC (www.iec.ch).
- Documentation on Beckhoff Automation ESC are available at the Beckhoff website (www.beckhoff.com), for example, data sheets, application notes, and ASIC pinout configuration tools.

28.1.11 Beckhoff® Automation EtherCAT IP Errata

Table 28-4 details the Beckhoff ®Automation errata of the EtherCAT IP integrated onto this device.

Table 28-4. EtherCAT IP Errata

Errata Number	Description
ER#156	WKC increment for reading reserved FMMU registers (+0xD-+0xF)
ER#158	WKC increment for writing 0x0914-0x0917
ER#162	ESC DL Control (0x0101) loop setting Auto-Close (01): if port waits for write access to be opened, the temporary loop bit (0x0100[1]) is not taken into account when a write command to ESC DL Control occurs.
ER#164	EEPROM FSM cannot accept another command within 1680 ns after finishing a previous command
ER#165	EtherCAT reset register 0x0040 cannot be written using VLAN tagged frames, because state is reset due to double ECAT_CLEAR. VLAN tagged frames are rarely used for EtherCAT.
ER#168	Changing SyncSignal cycle times during activation can lead to extremely long cycle times, resulting from (intermediate) violation of the minimum delay between two consecutive pulses. For example, changing Sync1 from a few ns before Sync0 to a few ns after Sync0 results in a missed Sync1 time, which can take up to several 32/64-bit turn-arounds until the next pulse occurs. Changing cycle time from PDI can result in usage of intermediate, inconsistent values, which can result in unwanted cycle times or extremely long delays as above.

28.2 ESC and ESCSS Description

ESC Integration on MCU shows the ESC on this MCU.

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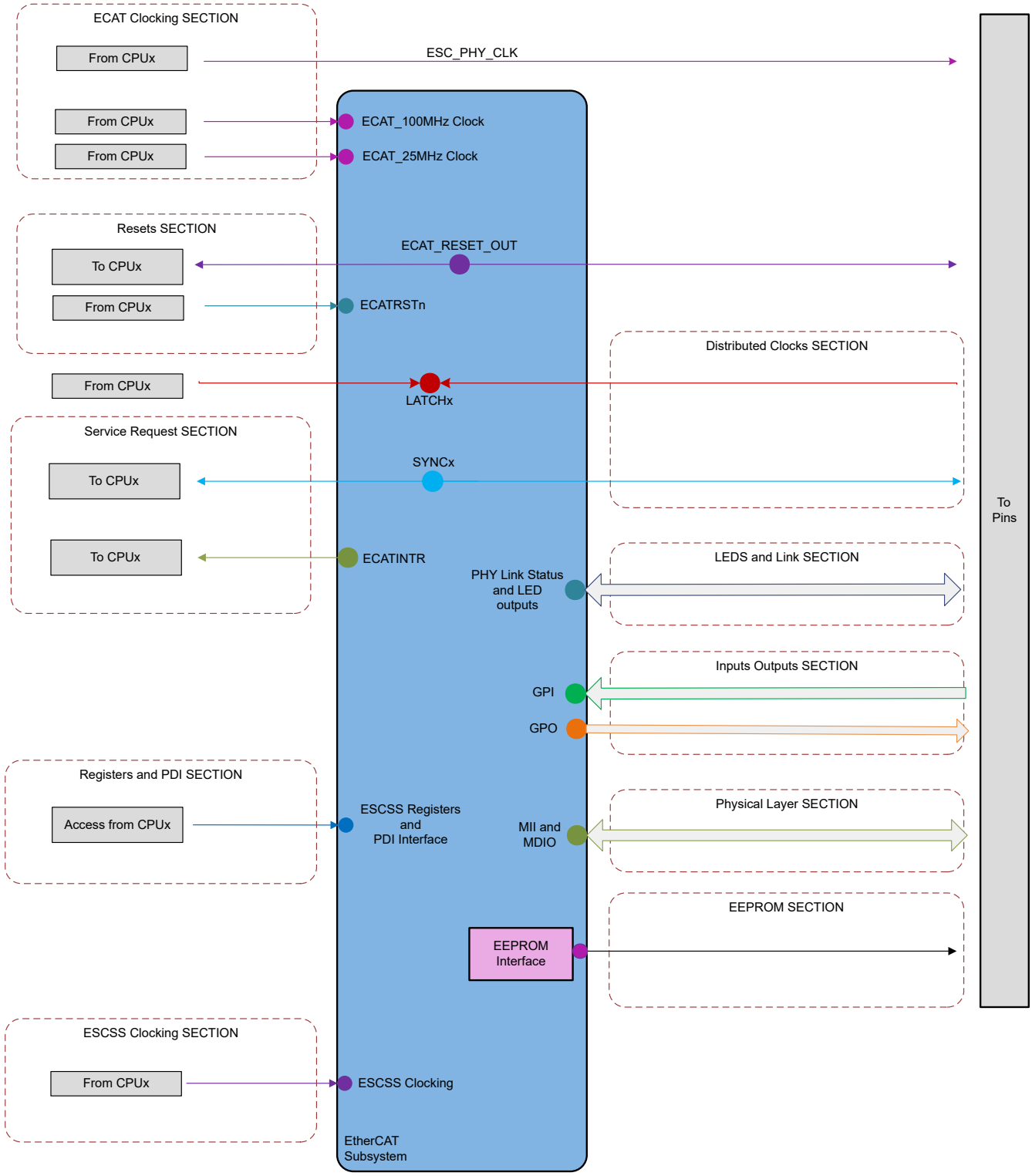


Figure 28-7. ESC Integration on MCU

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Table 28-5. ESC Integration Figure Sections

ESC Figure Sections	More Information Links
ECAT/ESCSS Clocking	ESC Clocking
Resets	ESCSS Resets
Service Request	SYNC Signals Interrupts and Interrupt Mapping
Registers and PDI	ESC SubSystem
Distributed Clocks	Distributed Clocks - Sync and Latch
LEDS and Link	LED Controls
Inputs Outputs	General Purpose Inputs and Outputs
Physical Layer	EtherCAT Physical Layer
EEPROM	SubordinateDevice Node Configuration and EEPROM

There are various actions that the controlling processor needs to perform in response to actions initiated by the EtherCAT MainDevice meant for this particular SubordinateDevice . All these interactions take place through one of the following:

- The 16-bit asynchronous interface through which registers and RAM of the EtherCAT IP are read/written.
- An interrupt request going from the ESC to the Local Host .
- SYNC0 and SYNC1 pulses generated by the ESC that are used as triggers for initiating further action.
- LATCH0 and LATCH1 that are sampled by the ESC.
- EtherCAT general-purpose inputs and outputs.

28.2.1 ESC RAM Parity and Memory Address Maps

This section details the ESC RAM parity logic, CPU1 ESC memory address map, and ESC memory address map.

28.2.1.1 ESC RAM Parity Logic

The ESC RAM has parity logic to check the data integrity of the RAM contents. The byte-wide parity is implemented, as PDI accesses to RAM can be done byte wide. To make sure that errors in parity logic itself do not mask the memory error, redundant parity generation logic is used. The parity generated by both logics is compared to make sure safe operation of the memory accesses. Use the INITIATE_MEM_INIT bit from the ESCSS_MEM_TEST register to trigger the memory initialization.

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28.2.1.2 EtherCAT Memory Map

Table 28-6. EtherCAT Memory Map

Region	Register Set	Base Address	End Address	Size(KB)
EtherCAT RAM - PDI Access	-	0x404A_1000	0x404A_4FFF	16
ESC_SS_REGS	ESCSS_REGS	0x404A_8000	0x404A_81FF	0.5
ESC_SS_CONFIG_REGS	ESCSS_CONFIG_REGS	0x404A_8200	0x404A_83FF	0.5
EtherCAT RAM - CPU Access	-	0x404C_0000	0x404C_3FFF	16

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28.2.2 Local Host Communication

Figure 28-8 shows how the ESC and ESC subsystem connects to the local host subsystem. The local host subsystem can include the CPU (CPU1) of the device and the DMA engine as the bus controller accessing the ESC. This local host subsystem is acting upon the commands that are sent by the EtherCAT MainDevice in the form of EtherCAT datagrams.

The 16-bit asynchronous interface and the interrupt request line are the main channels through which the local host subsystem interacts with the ESC. The interrupt request line can be used to trigger actions based on ESC internal events, exception conditions or time synchronized events. The DMA engine is used to transfer the contents from the process data memory to system RAM on any of these events. The user application needs to select the events that act as interrupts or DMA requests. The mask and clear events for the interrupt causes are configured to be accessed by the CPU/Co-processor that is controlling the ESC.

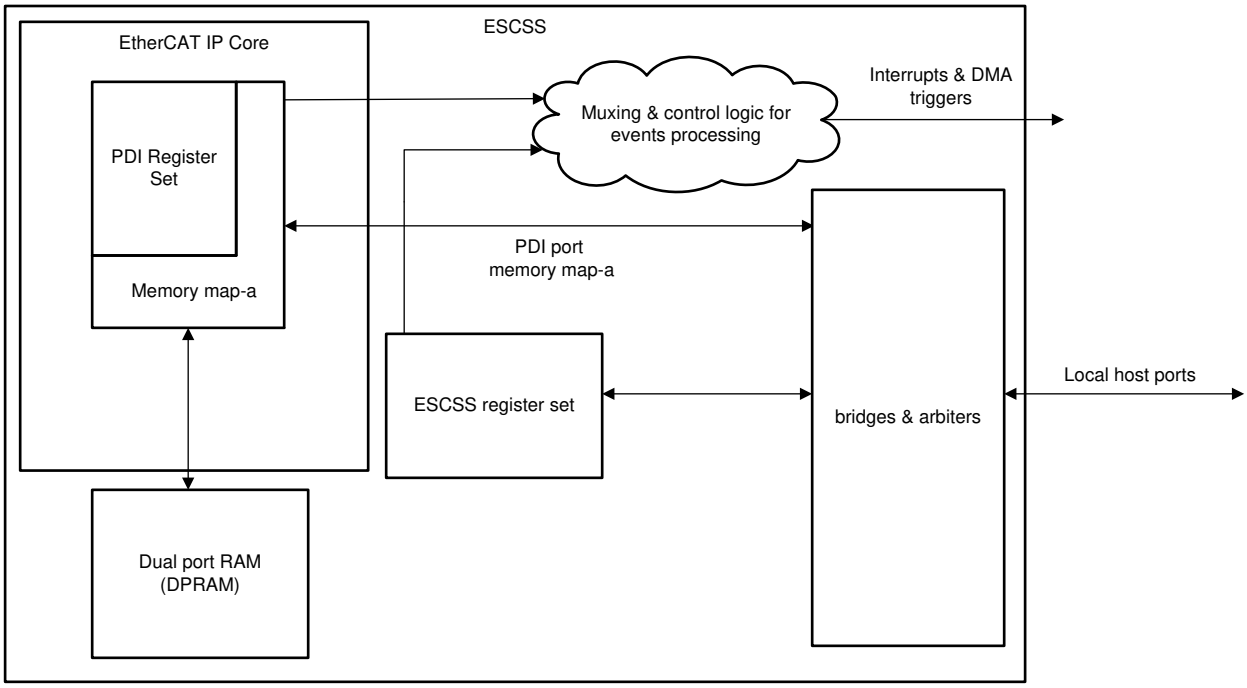


Figure 28-8. Interaction of ESCSS with the CPU Subsystem

28.2.2.1 Software Details for Operation Across Clock Domains

The registers accessible from the CPU are in the system clock domain and are synchronized to the PDI clock before being used within the EtherCAT IP. Given the frequency ratios and different styles of synchronization schemes, the application needs to assume there is a delay in getting the values transferred from one domain to other. Such a delay can vary based on the frequency of system clock and type of synchronizer used in the path.

For example, a system clock of 200MHz and ESCSS running at 100MHz requires at least 10 clock-system clock cycles delay before values are affected on the other side. If a write occurs to the PDI and some other action is performed elsewhere (not involving the PDI), then the software must perform a simple read to make sure that the write is complete.

28.2.3 Debug Emulation Mode Operation

There are two aspects of the EtherCAT IP operation that need to be considered from a debug emulation stand point.

- **Debugger Writes/Reads of EtherCAT IP registers/memories Condition:** The EtherCAT IP does not have any mechanism to identify a debug initiated read/write. Debug accesses to the registers or the ESC RAM can affect the state of the EtherCAT IP. This is addressed by the following:

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– **CPU1/:** The ENABLE_DEBUG_ACCESS bit must be set in the ESCSS Access Control Register to enable user access to the ESC RAM and EtherCAT registers for the purpose of debug. By default, this is disabled.

28.2.4 ESC SubSystem

The EtherCAT SubordinateDevice Controller SubSystem (ESCSS) wraps the ESC core with required register configurations and required logic for different functions of the EtherCAT and RAM (ESC RAM). This section covers the ESCSS integration aspects. Figure 28-9 shows the EtherCAT subsystem Integration.

- **ESCSS configuration registers interface** is the port for accessing the critical device level configurations which are a must have for the ESCSS to function.
- **ESCSS register interface** has control and status registers including SYNC, LATCH configurations, interrupt related controls, and GPIO related controls.
- **PDI Async interface** is a 16-bit wide data interface that allows the local application to access the registers internal to the EtherCAT IP Core as well as the dual-port memory (ESC RAM) through the SyncManager and the FMMUs.

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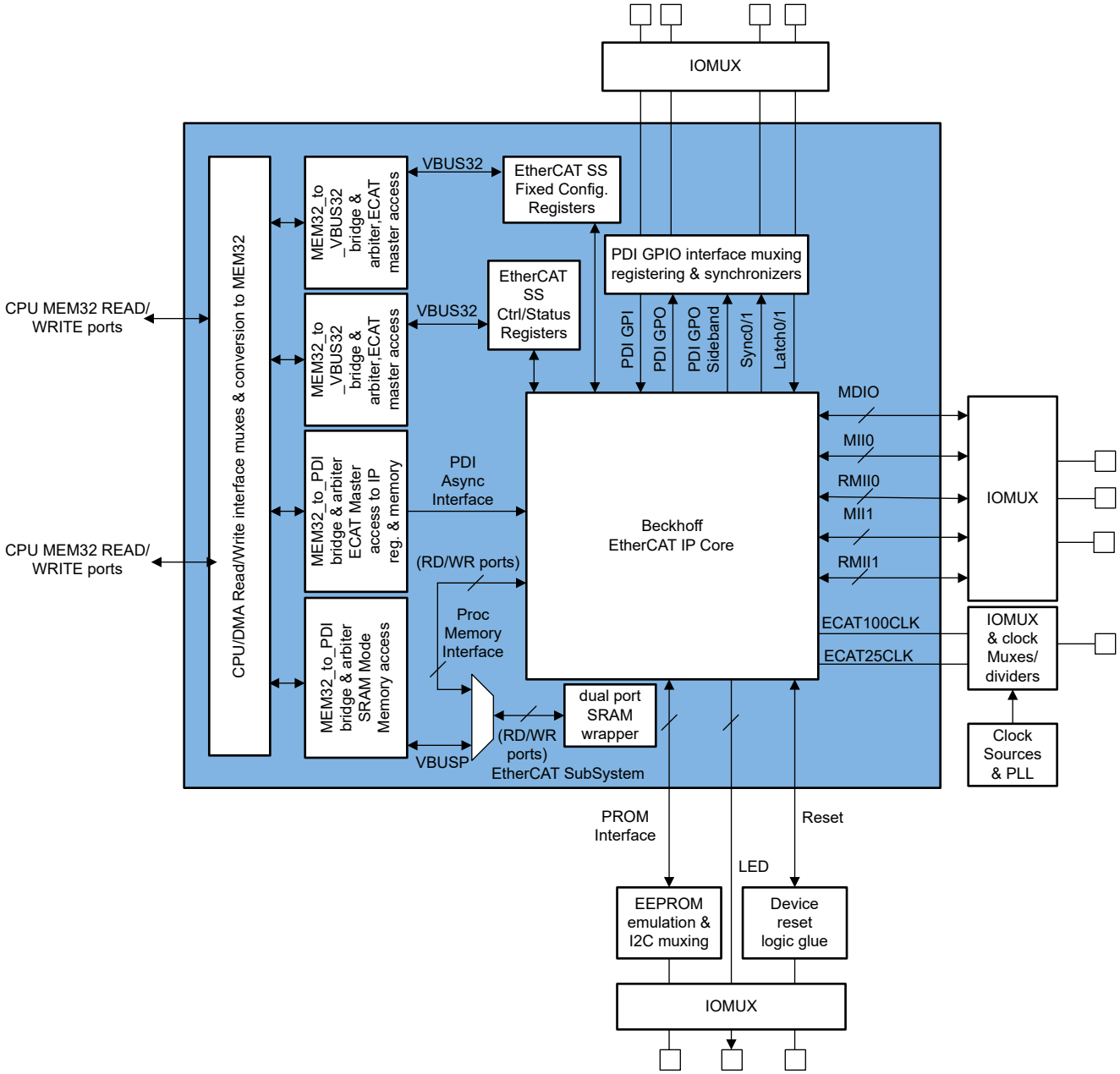


Figure 28-9. ESCSS Wrapper

28.2.4.1 CPU1 Bus Interface

Interface to the CPU1 core is retained at the ESCSS boundary as a native mem32 interface that connects the RD and WR ports independently to all of the SubordinateDevice entities within the ESCSS.

- CPU1 MEM32 RD and WR ports: Configuration Registers, Control/Status Registers, PDI
- CPU1 DMA MEM32 RD and WR ports: PDI (access to ESC RAM only)

28.2.5 Power, Clocks, and Resets

This section details the ESCSS power requirements, clocking, and resets. The EtherCAT IP has 2 clock ports and one reset output. Since the PLLs, dividers, and gating is implemented as part of system control, this setup is always handled by CPU1 during the initialization sequence.

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28.2.5.1 Power

The ESC module is inside the main power domain like other peripherals and there are no special considerations about the power-up or power-down sequences that need to be taken. Refer to the *System Controller (SYSCTL)* chapter for different power modes.

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28.2.5.2 Clocking

Two functional clock inputs are defined for the ESC: CLK25 (25MHz) and CLK100 (100MHz).

EtherCAT functional clock inputs CLK25 and CLK100 are sourced by the MCU clocking module using SYSPLLCLK0.

Note

- CLK25 and CLK100 are used for the ESC core operation. These two clocks and the clocks to the PHY **must have a common source**, which establishes a deterministic phase relationship between PHY clocks and ESC clocks.
- In MII mode, the 25MHz RX clock is sourced by the PHY while the TX clock from the PHY is optional (which effectively saves a pin). The phase differential between the PHY TX clock and CLK25 can be compensated to the TX data and TX EN using the manual compensation mode in increments of 10ns. Connecting the TX clock avoids the need to perform the manual compensation.

Figure 28-10 shows the clocks connectivity. Refer to the *System Control and Interrupts* chapter for additional details of the PLL source selections and clock dividers.

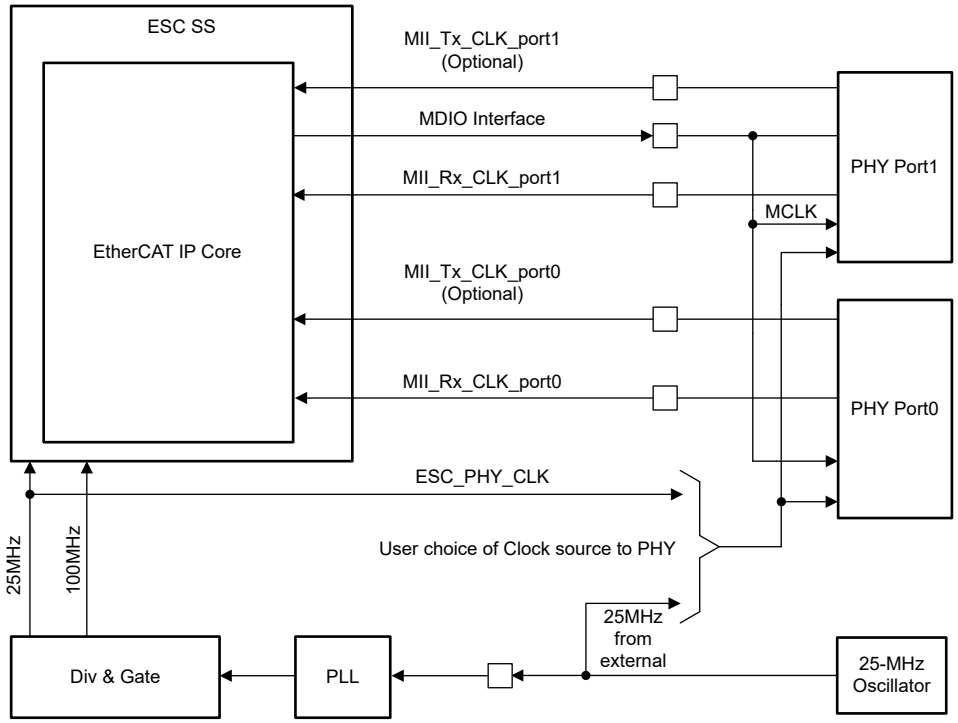


Figure 28-10. Clocking of ESC

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In the case of a low-accuracy clock (up to 100ppm) being used, a clock accuracy of 25ppm cannot be feasible, then the following restrictions apply:

- RX FIFO size cannot be reduced lower than 7 (default for 100ppm), which in turn affects the latency of the transfer as the transfer starts after half of the FIFO full threshold, thus resulting in a RX Delay.
- This ECS cannot be used as the first SubordinateDevice from the MainDevice in the network, as typically the first SubordinateDevice from the MainDevice is treated as the reference clock for the distributed clocks functionality.
- The number of iterations required for synchronizing clocks (specially the drift computation) increases.

28.2.5.3 Resets

This section describes the ESCSS sources of reset. There are other conditional reset sources that can impact ESCSS and those include all the device level reset sources including: device pin reset “XRSN” or software initiated device level reset “SYSRSn”.

Note

Whenever the device comes out of reset, software must execute the following sequence to make sure that PHY can see the full stretching of the reset:

1. Configure the EtherCAT GPIOs
2. Put the ESCSS into soft reset
3. Bring the ESCSS out of soft reset

Refer to Section 28.3 more information on proper software procedure.

28.2.5.3.1 Chip-Level Reset

Chip-level resets (such as SYSRST) are a MainDevice reset that resets the entire device including the ESC.

28.2.5.3.2 EtherCAT Soft Resets

ESCSS can be reset by three soft reset mechanisms, including:

- System control level software programmable (SOFTPRES23) that is reset only by chip-level and EtherCAT resets. Default keeps the ESC in reset that is released by the local application after setting the ESC ready for operation.
- Reset by a particular command sequence from the remote EtherCAT MainDevice.
- Reset by a particular command sequence from the local host application.

28.2.5.3.3 Reset Out (RESET_OUT)

Multiple reset sources of ESCSS are combined to make the reset vector that drives the EtherCAT and companion devices (PHYs) on this MCU. The RESET_OUT is asserted only when configured to be a reset. If configured as an interrupt or NMI, the local host completes the reset.

By default, RESET_OUT performs no action and must be setup to cause the reset to the EtherCAT core and PHY. The input events to RESET_OUT include the remote EtherCAT MainDevice, local host application, and EtherCAT soft reset.

When the intent is to perform a reset to the ESCSS and the device, the following options are available to reset the device after software has given a reset to the ESCSS:

- Use the system control SIMRESET register to generate a device reset.
- Use the watchdog or NMIWD to generate a device reset.

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28.2.6 LED Controls

There are four LED outputs from the ESC that can be routed out of GPIOs to indicate different status of the ESC. Table 28-7 is the recommendation for applications on the usage, especially for the pin sensitive systems that can support this and still meet the intent. All the LED functions are routed to the IOMUX and the user must configure the LEDs as per the available pins.

Table 28-7. Status LED Options and Priority

LED	Priority Order	Function	Recommendation	Usage Priority
RUN	5	Shows the status of ESC state machine with different blinking patterns.	In the case where color LEDs are not supported, then this needs to be supported.	Required
ERR(1)	4	Indicates the Error in ESC operation.	In the case where color LEDs are not supported, then at least the Error status needs to be reported.	Required
STATE	2	Combination of the RUN and ERR LED.	Not supported on this device.	-
LINKACT0 (ESC_LED_LINK0_ACTIVE)	3	Link Active Status for link towards the MainDevice.	Link Status on MainDevice side (Port0) is important to know, if the ESC and network downstream is part of the network or not. The prior ESC loopbacks, if this node fails. The status on this LED eases the debug.	Recommended
LINKACT1 (ESC_LED_LINK1_ACTIVE)	1	Link Active status for link towards Network side.	The Link status on the network side (Port 1) is critical from continuity through the ESC point; hence, this is kept highest priority status reporting.	Required

(1) Driven by software and not the ESC on this device.

The PHY MII_LINK (ESC_PHYx_LINKSTATUS) indication is an indication from PHY and does not indicate if the established link meets the characteristics including auto-negotiation as required by EtherCAT. Hence, the indication may not be a true status indication; however, it is critical to shorten reaction time in the event of link loss that is crucial for redundancy operation. Using LINKACT LEDs (LED_LINKx_ACTIVE) for the status output and MII_LINK (ESC_PHYx_LINKSTATUS) for the status input is the best usage; however, using the LEDs are not practical to sacrifice 4 pins. The tradeoff of whether MII_LINK is used as a link status LED or LINKACT is used depends on link loss reaction time requirements and available number of GPIOs for the system.

The PHY MII_LINK (ESC_PHYx_LINKSTATUS) signal is an active-low signal input to this microcontroller's ESC. It is possible to use the PINCMx.INV register to invert the signal's polarity before the signal enters the ESC, if the system hardware cannot provide the desired polarity for this signal.

The LINKACT LEDs (LED_LINKx_ACTIVE) is an output signal of the ESC intended to control an LED for link indication.

Table 28-8. LINKACT and PHY MII_LINK States

Link State	LINKACTx (LED_LINKx_ACTIVE) State	PHY MII_LINK (ESC_PHYx_LINKSTATUS) State
No Link	0 (LOW)	1 (HIGH)
Link WITHOUT Activity	1 (HIGH)	0 (LOW)
Link WITH Activity	Toggling / Blinking	0 (LOW)

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Note

The EtherCAT link status through the MII management interface option must be enabled if only a Gigabit PHY is to be supported and must not be enabled if needing to support both 10/100 and Gigabit PHY. For this reason, the link status through MII management interface is disabled on this ESC. Instead, use the LINKACT or PHY MII_LINK signals for link status purposes.

28.2.7 SubordinateDevice Node Configuration and EEPROM

The ESC requires non-volatile memory (for example, an EEPROM with I2C interface), which is referred to as the SubordinateDevice Information Interface (SII) memory, to store the EtherCAT SubordinateDevice Information (ESI) data.

The ESI data contains information about the SubordinateDevice device identification, supported features, and other network accessible properties.

Note

The ESI XML file is generated from Beckhoff's SubordinateDevice Stack Code (SSC) tool.

- **EtherCAT SubordinateDevice**
  - Uses the SII upon power-on or reset to load configuration data into the EtherCAT SubordinateDevice configuration registers.
- **EtherCAT MainDevice**
  - During development, the MainDevice is used to program the device SII memory with the ESI data.
  - When the ESI file isn't provided to the MainDevice, the MainDevice reads the device SII memory upon boot-up to determine the SubordinateDevice device properties such as the process data and their mapping options, the supported mailbox protocols including optional features, as well as the supported modes of synchronization.

28.2.8 General-Purpose Inputs and Outputs

The ESC subsystem implementation on this MCU supports 4 general-purpose inputs (GPI) and 4 general-purpose outputs (GPO) in addition to the PDI.

These GPI/GPOs provide an advantage for embedded applications over discrete components because the GPI/GPOs can selectively drive or sense GPIOs in a time controlled manner. For example, it can be a sensor/actuator control, status read, LED status update, and so on. The following section describes the integration and usage of this feature.

28.2.8.1 General-Purpose Inputs

General-purpose inputs are connected to the device IOMUX through an input buffer with an option to directly connect the asynchronous input flowing directly into the ECS or through a ESCSS register pipeline, which can hold the value stable while the value is captured within the ESC. The state of the GPI can be captured based on the following events:

- **Start-of-Frame (SOF):** Contents can be ready for capture in the frame if requested by the MainDevice
- **SYNC0/1:** Contents captured on a precise time tick
- **LATCH0/1:** Contents synchronized with LATCHIN read (allows simultaneous input and timestamp capture)

The ESCSS_GPIN_DAT register, containing the contents of the GPIN data, is available for reading from host CPU to allow debug access. Additionally, ESCSS_GPIN_DAT allows CPU writes for being used GPIN override purposes such as in place of using GPIOs.

GPIs are divided into 4 sets: GPI0:7, GPI8:15, GPI16:23, and GPI24:31, for clocking the capture trigger, which means the same capture trigger has to be used for the IOs within a set. Thus, either a bus can be formed out of these or individual IOs which need to be aggregated under common trigger can be combined in one set. This allows limited freedom of trigger selection for inputs. Selection of which inputs (ESCSS_GPIN_SEL) and outputs (ESCSS_GPOUT_SEL) can be connected to GPIO is possible at each single IO level.

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Figure 28-11 shows the integration of the GPI feature.

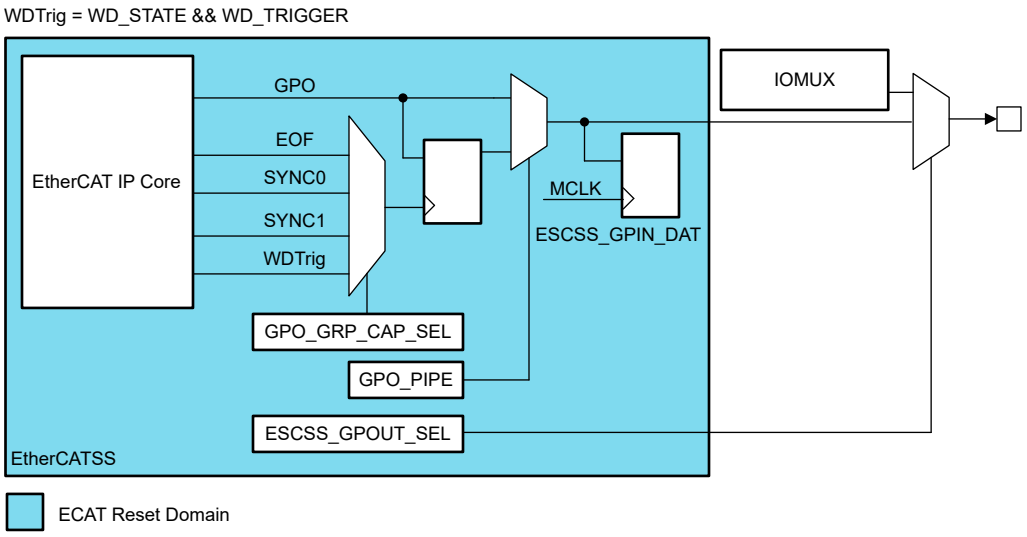


Figure 28-11. ESCSS General-Purpose Inputs Integration

Note

For software: The write data gets reflected on the ESCSS_GPIN_DAT read path only when one of the configured events, like SOF, SYNC0/1, and so on, is seen as configured after a few cycles of that event getting generated. Additionally, the copy of ESCSS_GPIN_DAT register readable by the CPU is provided without synchronization; therefore, multiple reads must be performed to confirm a stable value before using the value.

28.2.8.2 General-Purpose Output

General-purpose outputs are connected to the device IOMUX through an output buffer with an option to directly connect from the ESC IP core registers to the external world or through a ESCSS register pipeline, which can hold the output value stable. The state of the GPO can be set based on the following events:

- **End-of-Frame:**Contents can be updated by the MainDevice from the last received frame
- **SYNC0/1:** Contents can be updated based on a precise time tick
- **Watchdog Trigger:** Contents can be updated based on the last successful access to process data memory

The ESCSS_GPOUT_DAT register, containing the contents of the GPO data, is available for reading from host CPU to allow debug access or to read in place of GPIOs.

GPOs are divided into 4 sets: GPI0:7, GPI8:15, GPI16:23, and GPI24:31, for clocking the output trigger, which means the same output trigger has to be used for the IOs within a set. Thus, either a bus can be formed out of these or individual IOs which need to be aggregated under common trigger can be combined in one set. This allows limited freedom of trigger selection for inputs. Selection of which inputs (ESCSS_GPIN_SEL) and outputs (ESCSS_GPOUT_SEL) can be connected to GPIO is possible at each single IO level.

Figure 28-12 shows the integration of the GPO feature.

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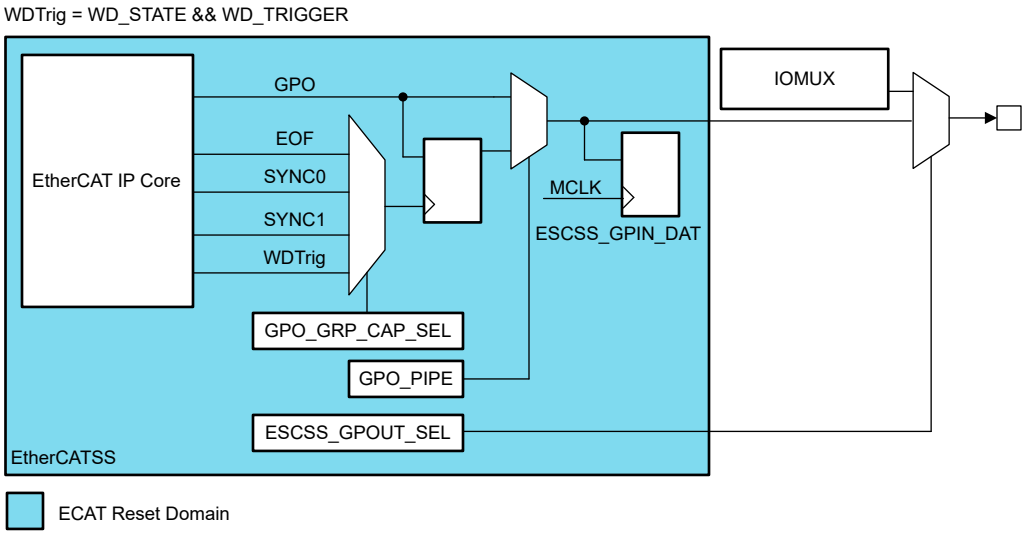


Figure 28-12. ESCSS General-Purpose Output Integration

Note

In Figure 28-12, the synchronization between ECAT100CLK or ECAT25CLK with respect to MCLK is not shown and is implicit by design. The local host can adjust for the synchronization delays as required while processing the data in either direction.

28.2.9 Distributed Clocks – Sync and Latch

Distributed clocks (DC) is a differentiating feature of the EtherCAT network. Distributed clocks allows all the SubordinateDevice nodes in the EtherCAT network to be bound in a tight margin of time to synchronize the events and the EtherCAT MainDevice command.

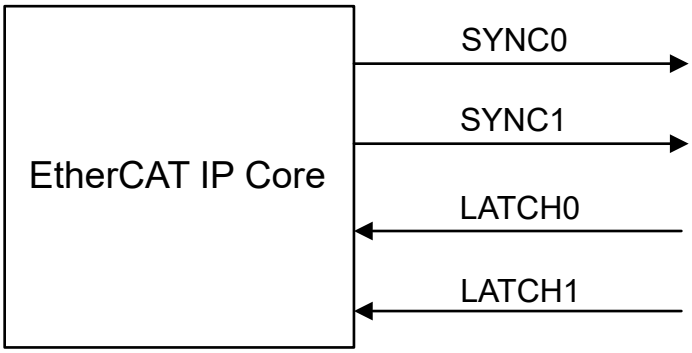


Figure 28-13. ESC SYNC and LATCH

This feature has sub-features as listed below. To enable the utility of these features at the application level, the related signals of DC are integrated tightly with the MCUs control loop logic, as well as an external component that can be a possible implementation to trigger/latch other components on the board. This section explains the integration of these signals and related nuances of usage.

Distributed clock features:

- Clock Synchronization
- Sync Signal Generation
- Latch Signal event capture

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Apart from usage for control loop synchronizations, these features are also used to synchronize the system and network time. These include the following:

- **System Time PDI Controlled:** Synchronize system time between two different EtherCAT networks.
- **Communication Timing:** Synchronize SubordinateDevice communication with sync signals, output or input events, and so on.

For further reading, including details on network time or network propagation delay, refer to the **ESC Hardware Data Sheet Section I - Technology (ethercat_esc_datasheet_sec1_technology)** document provided by Beckhoff/ETG at www.beckhoff.com.

28.2.9.1 Clock Synchronization

DC clock synchronization is the ability and procedure of the ESC to maintain the copy of the reference clock based on local clock (internal 64-bit time base) and other adjustment as derived by the procedure. The reference clock is the most accurate clock in the system and is typically held by one of the SubordinateDevices (Topologically first one after MainDevice is preferred). This time-base has a higher accuracy requirement and needs to periodically synchronize with an absolute time source like GPS or any other maintained time-base as in IEEE1588 network.

The synchronization order is as follows:

1. The MainDevice maintains a MainDevice clock that is either the absolute time synchronized or controls the reference clock.
2. The MainDevice queries the ESC time-base based on topology information and timestamps to determine the drift of the local clock for each ESC with regards to the reference clock.
3. The MainDevice programs the clock drift adjustments in each respective ESC.
4. With further periodic queries of the local clock, the MainDevice determines the drift of the local clock and keeps adjusting the clock so as to maintain the copies of the reference clocks on each ESCs in a tight limit.

While the ESC requires two clocks of 25MHz and 100MHz, the 100MHz clock is used for the internal time-base and supports the best accuracy possible. Refer to Section 28.2.5.2 for more details on clocking.

28.2.9.2 SYNC Signals

Sync signals are precise time controlled signals and are able to trigger time synchronized actions of the MainDevice. CPU core and DMA engine triggers are configured independently for every end point. The following sections describe ESC signal integration and various control triggers in the device.

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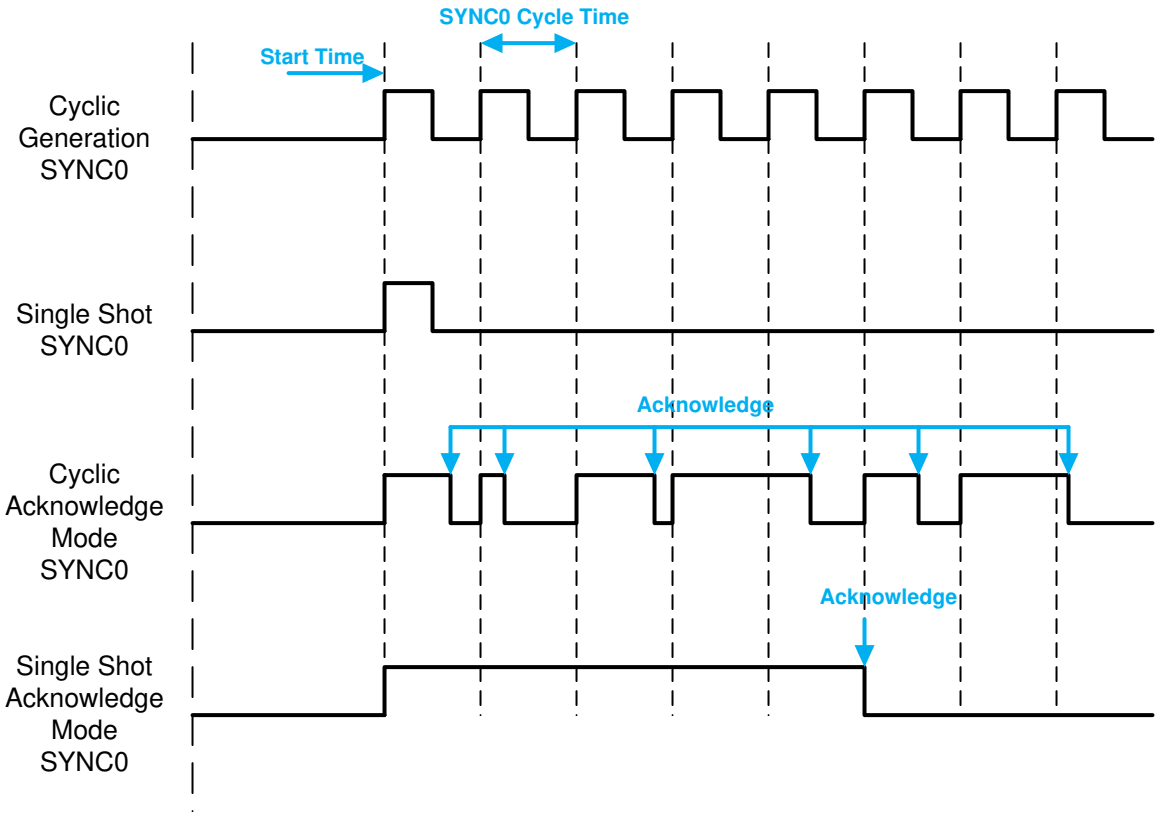


Figure 28-14. SYNC0 Signal Modes

- **SYNC0:** The SYNC0 is the primary trigger and can be generated in either a cyclic (periodic event generation like rise edge at every x period) or one-shot mode. Furthermore, these modes can be either with or without acknowledge, such that when enabled with acknowledge mode, the next event is not generated until the acknowledgment is received from the controlling MainDevice. If the acknowledgment is delayed, the event is skipped and the next periodic event is generated. Remember that the acknowledgment can be part of the interrupt servicing from the PDI and such a delay in triggering the next event is acceptable since the servicing routine can accordingly take action for the period elapsed. These modes are shown in Figure 28-14.
- **SYNC1:** The SYNC1 generation follows the SYNC0 generation with a programmable delay. Depending upon the delay time defined, SYNC1 can or cannot generate the pulse since the predefined delay from the SYNC0 event is newly measured only after the SYNC1 event (except for the start).

Note

- The SYNC0/1 when used in a system clock domain is stretched to at least 3 clock-wide pulse.
- When ESC goes through a reset, the SYNC outputs triggering external device events need to be kept at a safe value. At reset, the output values are 0 and this can be an active state when the reset occurs; therefore, the corresponding care of usage from the remote device must be taken.

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28.2.9.3 LATCH Signals

Latch inputs to the ESC can be used to capture the time-stamp or register the GPI inputs. Two latch inputs are available. Latch enables external events:

- To take a system time snapshot of the EtherCAT network, measure time, or schedule further operations.
- To capture the status of the GPI inputs either as the status of connected external components or as part of control flow.

Both of the Latch inputs can be independently configured to operate on either the rising or falling edge of the signal. The LATCH events can be individually assigned either for the PDI control or EtherCAT controller control. Additionally, one shot or continuous mode is supported.

- In **one shot mode**, the next capture of the timestamp is done on a qualifying LATCH event only after the previous event is acknowledged.
- In **continuous mode**, timestamps are successively captured on a qualifying event, regardless of a preceding event being read or not.

Figure 28-15 depicts the different sources for the LATCH0/1 so as to fulfill the application requirements. These are explained for possible use.

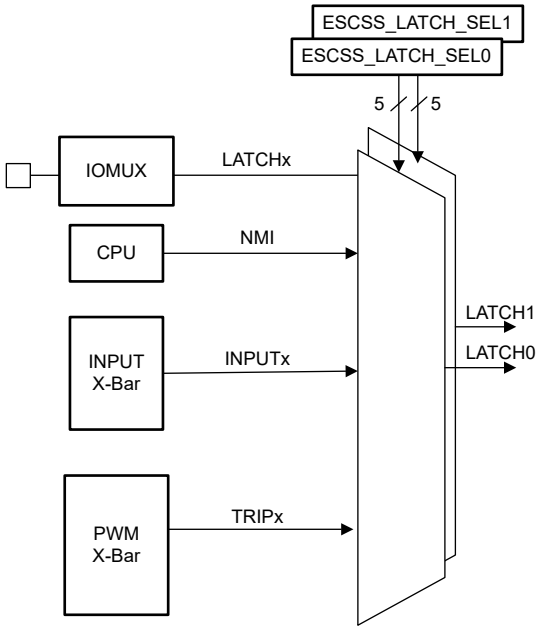


Figure 28-15. ESC Latch Input Integration

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The details of connections and mux select to these muxes is shown in Table 28-9 and selection is possible individually for each of the LATCH0 or LATCH1 signal.

Table 28-9. ESC LATCH0/1 Trigger Table

ECAT_LATCH_SELx	Signal Hookup
0	ECAT_LATCH0 (From Pin)
1	ECAT_LATCH1 (From Pin)
2	CPU_NMI
3	INPUTXBAR1
4	INPUTXBAR2
5	INPUTXBAR3
6	INPUTXBAR4
7	INPUTXBAR5
8	INPUTXBAR6
9	INPUTXBAR7
10	INPUTXBAR8
11	INPUTXBAR9
12	INPUTXBAR10
13	INPUTXBAR11
14	INPUTXBAR12
15	INPUTXBAR13
16	INPUTXBAR14
17	INPUTXBAR15
18	INPUTXBAR16
19	PWMXBAR1
20	PWMXBAR2
21	PWMXBAR3
22	PWMXBAR4
23	PWMXBAR5
24	PWMXBAR6
25	PWMXBAR7
26	PWMXBAR8
27-31	Reserved

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28.2.9.3.1 Timestamping

Timestamping allows the local application or remote EtherCAT MainDevice to measure the time events and plan the subsequent controls.

Timestamping: Device Internal Events

- Enable timestamping and logging of internal device events coming from control logic
- The same outputs of the PWM crossbar that connect to the 8 PWMs can be used as 8 input signals (PWMXBAROUT0-PWMXBAROUT7) for time stamping
- Note that there is no independent option for Latch muxing as far as PWM X-BAR inputs are concerned; unless one of the TRIP outputs are not used in control loop and such a crossbar output is dedicated for LATCH0/1 toggle

Timestamping: External Events

- Enable external board components apart from the MCU to trigger capture of the timestamp
- For example, timestamp a periodic event or pulse/edge event from a senor when the sensor data is read or accessed
- Connecting the LATCH0/1 controls through the input crossbar allows timestamp capture based on any selected GPIO toggle (such as GPTRIP15 or GPTRIP16)
  - Two GPTRIPs are provided for independent GPIO choice for LATCH0 and LATCH1
  - GPTRIP1, 2, and 3 allow the same functionality; however, those can be utilized for PWM trip zone functions where pins can or cannot need to match. If a trip zone based on GPTRIP is to be latched, one of these inputs can be used.

Timestamping: Device Exception Events

- Log and timestamp exception events within the device (example: NMI exceptions) and periodically collect information to find out systemic issues in the system
- Can be used by local application and the remote MainDevice to diagnose or debug the system

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28.2.9.4 Device Control and Synchronization

The primary advantage of DC functionality is when used in conjunction with device control functions. The precisely timed pulse/edge nature of the SYNC allows the ESC to synchronize the internal resources like PWMs, ECAPs (for capture as well as PWM) with remote system components. The following are the connections which are available for applications to program for allowing this synchronization.

28.2.9.4.1 Synchronization of PWM

The PWM Sync-chain on the MCU can be triggered either by the device external inputs from the GPIO using the input cross-bar or the PWM internal events when the chain is programmed appropriately. The SYNC0/1 inputs in this implementation also act as the external sync inputs to the PWM sync-chain. The integration is shown in Figure 28-16.

The additional select register added to the trigger crossbar register allows independent programming of the EXTSYNCx from either GPTRIP or SYNC0/1.

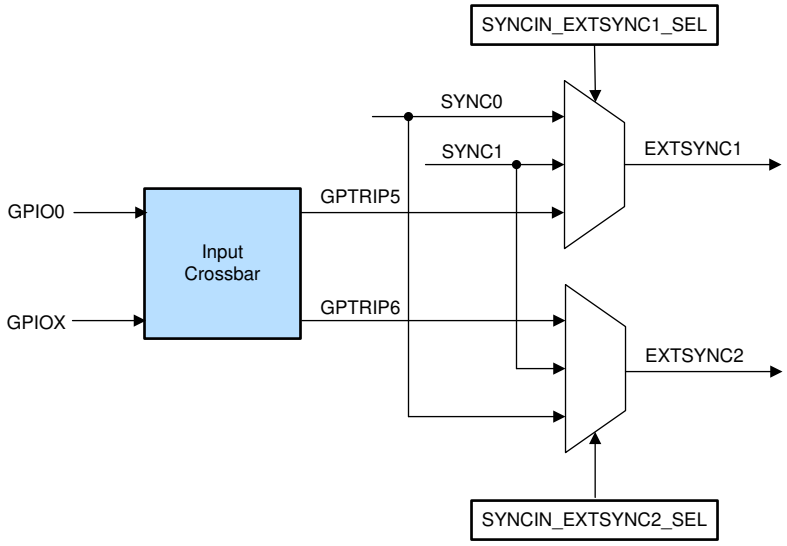


Figure 28-16. SYNC Integration for Control Functions - PWM SYNC

28.2.9.4.2 ECAP SYNC Inputs

ECAP supports accurate time capture of events that can be relatively checked against the series of events in vicinity and used for the control loop action. Additionally, ECAP has inbuilt capability of limited PWM action that can be triggered based on the selected input. Hence, the SYNC0/1 are also connected to ECAP input mux. The exact select value/vector for SYNC0/1 is defined in the *Enhanced Capture (eCAP)* chapter.

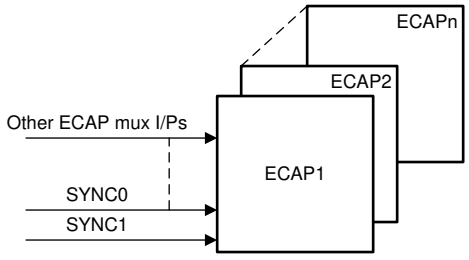


Figure 28-17. SYNC Integration for Control Functions – ECAP

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28.3 Software Initialization Sequence and Allocating Ownership

This section details the software initialization sequence when configuring CPU1 or as ESC owner. The sequence includes details on allocating ownership of the ESC peripheral.

Table 28-10. CPU1 Software Initialization Sequence

Step	Action
1	General device initialization (configure clock, enable PLL, enable peripheral clocks except EtherCAT)
2	Configure Aux Clock for EtherCAT (if using Aux clock as source)
3	Configure GPIOs for EtherCAT (set pin configurations, set GPIO qualification mode, set pad configuration)
4	Initialize interrupts and register ISR handlers
5	Set EtherCAT clock source and divider. Then configure if EtherCAT PHY is clocked from device or external PHY clock.
6	Configure the EEPROM size
7	Bring ESC out of reset using system control register
8	Perform EtherCAT memory initialization and wait until memory initialization is complete
9	(Optional) Enable debug access to the EtherCAT registers
10	(Optional) Check that EEPROM loaded successfully
11	EtherCAT subsystem configurations for interrupt masking, SYNCx connections, and so on(1)

(1) Applications must make sure that ESC outputs are in a safe state until the EEPROM is loaded and that SYNC and LATCH are configured only after the EEPROM is loaded.

28.4 ESC Configuration Constants

The following is EtherCAT IP core configurations that are static by design.

Table 28-11. ESC Configuration Constants Table

Name	Value
ESC Type	0x91
Revision	0x0
Build	0x0
FMMU Supported	0x8
SyncManagers	0x8
RAM Size	0x10
Port Descriptor	0xF
ESC Features Supported	0x1CC
Product ID	0x0
Vendor ID	0x0

Table 28-12. ESC IP Register Constants Table

EtherCAT IP Register	Offset Address	Value(1)
PDI 8/16Bit asynchronous Microcontroller configuration	0x0150	0x00
Sync/Latch PDI configuration	0x0151	0x66
Pulse Length of SyncSignals	0x0982/0x0983	0x000A

(1) These values are not changed or overwritten by EEPROM contents.

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28.5 EtherCAT Interrupts & Triggers

28.5.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 28-13. CPU Interrupts Triggered by EtherCAT

NVIC Interrupt Name	Peripheral Instance Name	Register Group	EtherCAT Interrupt Configuration Registers	Description
ECAT_INTn	ESCSS	N/A	ESCSS_INTR_RIS, ESCSS_INTR_MASK, ESCSS_INTR_MIS, ESCSS_INTR_SET, ESCSS_INTR_CLR	EtherCAT All Event interrupt. Multiple OR'd, configurable source conditions.
ECAT_SYNC0	ESCSS	N/A	ESCSS_INTR_RIS, ESCSS_INTR_MASK, ESCSS_INTR_MIS, ESCSS_INTR_SET, ESCSS_INTR_CLR	EtherCAT Precise Time Event 0 interrupt. Single configurable source condition.
ECAT_SYNC1	ESCSS	N/A	ESCSS_INTR_RIS, ESCSS_INTR_MASK, ESCSS_INTR_MIS, ESCSS_INTR_SET, ESCSS_INTR_CLR	EtherCAT Precise Time Event 1 interrupt. Single configurable source condition.
ECAT_RST	ESCSS	N/A	ESCSS_INTR_RIS, ESCSS_INTR_MASK, ESCSS_INTR_MIS, ESCSS_INTR_SET, ESCSS_INTR_CLR	EtherCAT Master Reset interrupt. Single configurable source condition.

28.5.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 28-14. DMA Triggers from the EtherCAT

Trigger Name	Peripheral Instance Name	Register Group	EtherCAT DMA Configuration Registers	Description
ECAT_SYNC_DMA_TRIG	ESCSS	N/A	ESCSS_INTR_RIS, ESCSS_INTR_MASK, ESCSS_INTR_MIS, ESCSS_INTR_SET, ESCSS_INTR_CLR	EtherCAT Precise Time Event 1 DMA trigger. Single configurable source condition.

28.6 ESC Registers

This Section describes the ESC Registers.

28.6.1 ESC Base Address Table

Table 28-15. ESC Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
EscssRegs	ESCSS_REGS	ESCSS	0x404A_8000
EscssConfigRegs	ESCSS_CONFIG_REGS	ESCSS_CONFIG	0x404A_8200

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28.6.2 ESCSS_REGS Registers

Table 28-16 lists the memory-mapped registers for the ESCSS_REGS registers. All register offset addresses not listed in Table 28-16 should be considered as reserved locations and the register contents should not be modified.

Table 28-16. ESCSS_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	ESCSS_IPREVNUM	IP Revision Number		Go
4h	ESCSS_INTR_RIS	EtherCATSS Interrupt Raw Status		Go
8h	ESCSS_INTR_MASK	EtherCATSS Interrupt Mask		Go
Ch	ESCSS_INTR_MIS	EtherCATSS Masked Interrupt Status		Go
10h	ESCSS_INTR_CLR	EtherCATSS Interrupt Clear		Go
14h	ESCSS_INTR_SET	EtherCATSS Interrupt Set to emulate		Go
18h	ESCSS_LATCH_SEL	Select for Latch0/1 inputs and LATCHIN input		Go
1Ch	ESCSS_ACCESS_CTRL	PDI interface access control config.		Go
20h	ESCSS_GPIN_DAT	GPIN data capture for debug & override		Go
24h	ESCSS_GPIN_PIPE	GPIN pipeline select		Go
28h	ESCSS_GPIN_GRP_CAP_SEL	GPIN pipe group capture trigger		Go
2Ch	ESCSS_GPOUT_DAT	GPOUT data capture for debug & override		Go
30h	ESCSS_GPOUT_PIPE	GPOUT pipeline select		Go
34h	ESCSS_GPOUT_GRP_CAP_SEL	GPOUT pipe group capture trigger		Go
38h	ESCSS_MEM_TEST	Memory Test Control		Go
3Ch	ESCSS_RESET_DEST_CONFIG	ResetOut impact or destination config		Go
40h	ESCSS_SYNC0_CONFIG	SYNC0 Configuration for various triggers		Go
44h	ESCSS_SYNC1_CONFIG	SYNC1 Configuration for various triggers		Go

Complex bit access types are encoded to fit into small table cells. Table 28-17 shows the codes that are used for access types in this section.

Table 28-17. ESCSS_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
-n		Value after reset or the default value

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1 ESCSS_IPREVNUM Register (Offset = 0h) [Reset = 00000000h]

ESCSS_IPREVNUM is shown in Figure 28-18 and described in Table 28-18.

Return to the Summary Table.

IP Revision number showing the Major & Minor IP versions 4 bit each

Figure 28-18. ESCSS_IPREVNUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IP_REV_MAJOR				IP_REV_MINOR			
R-0-0h								R-0h				R-0h			

Table 28-19. ESCSS_IPREVNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R-0	0h	Reserved
7-4	IP_REV_MAJOR	R	0h	Major IP Type increment is hardcoded reset value which increments to signify major change in IP behavior in terms of data/control flow or new feature addition. Reset type: ECAT.IPRSn
3-0	IP_REV_MINOR	R	0h	Reset value for this register is hardcoded and increments with minor changes to the IP those will not increment IP Type, but the bug fixes and changes impact behavior or software control than previous silicon version. Reset type: ECAT.IPRSn

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2 ESCSS_INTR_RIS Register (Offset = 4h) [Reset = 00000000h]

ESCSS_INTR_RIS is shown in Figure 28-19 and described in Table 28-19.

Return to the Summary Table.

Registers the Raw Interrupt status of different interrupt triggers regardless of mask.

Figure 28-19. ESCSS_INTR_RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		MASTER_RESET_RIS	TIMEOUT_ERR_RIS	DMA_DONE_RIS	IRQ_RIS	SYNC1_RIS	SYNC0_RIS
R-0-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 28-21. ESCSS_INTR_RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	MASTER_RESET_RIS	R	0h	Indicates Raw Status of the EtherCAT Master Reset event , until cleared by ESCSS_INTR_CLR 0: EtherCAT Master Reset Event did not happen since last IP reset or last clear of this bit and ECAT Master reset programmed to be Interrupt to local host. 1: EtherCAT Master Reset Event has occured. This status gets updated regardless of interrupt mask, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Information of this event is lost if ECAT Master event is programmed to be reset IP. Reset type: ECAT.IPRSn
4	TIMEOUT_ERR_RIS	R	0h	Indicates Raw Status of the past event on PDI access timeout Error, until cleared by ESCSS_INTR_CLR 0: PDI Access Timeout Error Event did not happen since reset or last clear of this bit. 1: PDI Access Timeout Error Event has triggered the interrupt/DMA trigger. This status gets updated regardless of interrupt mask as long as Timeout is enabled, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Reset type: ECAT.IPRSn

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Table 28-21. ESCSS_INTR_RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DMA_DONE_RIS	R	0h	Indicates Raw Status of the past event on DMA Done, until cleared by ESCSS_INTR_CLR 0: DMA Done Event did not happen since reset or last clear of this bit. 1: DMA Done Event has triggered the interrupt/DMA trigger. This status gets updated regardless of interrupt mask, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Reset type: ECAT.IPRSn
2	IRQ_RIS	R	0h	Indicates Raw Status of the past event on EtherCATSS IRQ, until cleared by ESCSS_INTR_CLR 0: EtherCATSS IRQ Event did not happen since reset or last clear of this bit. 1: EtherCATSS IRQ Event has triggered the interrupt/DMA trigger. This status gets updated regardless of interrupt mask, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Reset type: ECAT.IPRSn
1	SYNC1_RIS	R	0h	Indicates Raw Status of the past event on SYNC1, until cleared by ESCSS_INTR_CLR 0: SYNC1 Event did not happen since reset or last clear of this bit. 1: SYNC1 Event has triggered the interrupt/DMA trigger. This status gets updated regardless of interrupt mask, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Reset type: ECAT.IPRSn
0	SYNC0_RIS	R	0h	Indicates Raw Status of the past event on SYNC0, until cleared by ESCSS_INTR_CLR 0: SYNC0 Event did not happen since reset or last clear of this bit. 1: SYNC0 Event has triggered the interrupt/DMA trigger. This status gets updated regardless of interrupt mask, it is registered on the EtherCATSS clock domain, sticky and remains active till cleared using ESCSS_INTR_CLR. If simultaneous clear & incoming event on same clock edge the incoming event registering has priority and clear does not have effect. Reset type: ECAT.IPRSn

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3 ESCSS_INTR_MASK Register (Offset = 8h) [Reset = 00000000h]

ESCSS_INTR_MASK is shown in Figure 28-20 and described in Table 28-20.

Return to the Summary Table.

Allows to mask individual interrupt cause impacting the interrupt

Figure 28-20. ESCSS_INTR_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		MASTER_RESET_MASK	TIMEOUT_ERR_MASK	DMA_DONE_MASK	IRQ_MASK	SYNC1_MASK	SYNC0_MASK
R-0-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 28-23. ESCSS_INTR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	MASTER_RESET_MASK	R/W	0h	Masks EtherCAT Master reset event against any effect on interrupts or other CPU Interrupts. 1: EtherCAT Master Reset affects the interrupt/DMA trigger. 0: EtherCAT Master Reset masked and does not affect Interrupt. Reset type: ECAT.IPRSn
4	TIMEOUT_ERR_MASK	R/W	0h	Masks PDI access timeout Error to have effect on interrupts or other CPU Interrupts. 1: PDI Access Timeout Errors affects the interrupt/DMA trigger. 0: PDI Access Timeout Errors masked and does not affect Interrupt. Reset type: ECAT.IPRSn
3	DMA_DONE_MASK	R/W	0h	Masks DMA Done status update to have effect on interrupts or other CPU Interrupts. 1: DMA Done affects the interrupt/DMA trigger. 0: DMA Done masked and does not affect Interrupt. Raw DMA Done status is updated regardless of this setting. Reset type: ECAT.IPRSn
2	IRQ_MASK	R/W	0h	Masks EtherCATSS IRQ to have effect on interrupts or other CPU/DMA triggers. 1: EtherCATSS IRQ affects the interrupt/DMA trigger. 0: EtherCATSS IRQ masked and does not affect Interrupt/DMA trigger. Raw EtherCATSS IRQ status is updated regardless of this setting. Reset type: ECAT.IPRSn

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Table 28-23. ESCSS_INTR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SYNC1_MASK	R/W	0h	Masks SYNC1 to have effect on interrupts or other CPU/DMA triggers as programmed in HOST_TRIG_MAP registers. 1: SYNC1 affects the interrupt/DMA trigger. 0: SYNC1 masked and does not affect Interrupt/DMA trigger. Raw SYNC1 status is updated regardless of this setting. Reset type: ECAT.IPRSn
0	SYNC0_MASK	R/W	0h	Masks SYNC0 to have effect on interrupts or other CPU/DMA triggers as programmed in HOST_TRIG_MAP registers. 1: SYNC0 affects the interrupt/DMA trigger. 0: SYNC0 masked and does not affect Interrupt/DMA trigger. Raw SYNC0 status is updated regardless of this setting. Reset type: ECAT.IPRSn

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4 ESCSS_INTR_MIS Register (Offset = Ch) [Reset = 00000000h]

ESCSS_INTR_MIS is shown in Figure 28-21 and described in Table 28-21.

Return to the Summary Table.

Registers the Msked Interrupt status of different interrupt triggers. This is AND of RIS & MASK of respective fields

Figure 28-21. ESCSS_INTR_MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		MASTER_RESET_MIS	TIMEOUT_ERR_MIS	DMA_DONE_MIS	IRQ_MIS	SYNC1_MIS	SYNC0_MIS
R-0-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 28-25. ESCSS_INTR_MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	MASTER_RESET_MIS	R	0h	Indicates Masked Interrupt status of the past event on EtherCAT Master Reset, until RIS cleared by ESCSS_INTR_CLR or by Reset. 0: No pending EtherCAT Master Reset interrupt, if configured and unmasked. 1: EtherCAT Master Reset Event has triggered the interrupt/DMA trigger and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn
4	TIMEOUT_ERR_MIS	R	0h	Indicates Masked Interrupt status of the past event on PDI Access Timeout Error, until RIS cleared by ESCSS_INTR_CLR 0: No pending PDI Access Timeout Error interrupt. 1: PDI Access Timeout Error Event has triggered the interrupt/DMA trigger and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn
3	DMA_DONE_MIS	R	0h	Indicates Masked Interrupt status of the past event on DMA Done, until RIS is cleared by ESCSS_INTR_CLR 0: No pending DMA Done interrupt. 1: DMA Done Event has triggered the interrupt/DMA trigger and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn

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Table 28-25. ESCSS_INTR_MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IRQ_MIS	R	0h	Indicates Masked Interrupt status of the past event on EtherCATSS IRQ, until RIS is cleared by ESCSS_INTR_CLR 0: No pending EtherCATSS IRQ interrupt. 1: EtherCATSS IRQ Event has triggered the interrupt and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn
1	SYNC1_MIS	R	0h	Indicates Masked Interrupt status of the past event on SYNC0, until RIS is cleared by ESCSS_INTR_CLR 0: No pending SYNC1 interrupt. 1: SYNC1 Event has triggered the interrupt/DMA trigger and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn
0	SYNC0_MIS	R	0h	Indicates Masked Interrupt status of the past event on SYNC0, until RIS is cleared by ESCSS_INTR_CLR 0: No pending SYNC0 interrupt. 1: SYNC0 Event has triggered the interrupt/DMA trigger and it's pending. This is MASK qualified RIS such that application can select to service or suppress the interrupt cause behind this. Upon reset or upon RIS clear through ESCSS_INTR_CLR this field is cleared. Reset type: ECAT.IPRSn

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5 ESCSS_INTR_CLR Register (Offset = 10h) [Reset = 00000000h]

ESCSS_INTR_CLR is shown in Figure 28-22 and described in Table 28-22.

Return to the Summary Table.

Individual Interrupt cause clear register

Figure 28-22. ESCSS_INTR_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED		MASTER_RESET_CLR	TIMEOUT_ERR_CLR	DMA_DONE_CLR	IRQ_CLR	SYNC1_CLR	SYNC0_CLR
R-0-0h		R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h	R-0/W1C-0h

Table 28-27. ESCSS_INTR_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R-0	0h	Reserved
5	MASTER_RESET_CLR	R-0/W1C	0h	Clears EtherCAT Master Reset raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the EtherCAT Master reset, read always returns 0. Reset type: ECAT.IPRSn
4	TIMEOUT_ERR_CLR	R-0/W1C	0h	Clears PDI access timeout Error raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the PDI Access Timeout Error, read always returns 0. Reset type: ECAT.IPRSn
3	DMA_DONE_CLR	R-0/W1C	0h	Clears DMA Done raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the DMA Done, read always returns 0. Reset type: ECAT.IPRSn
2	IRQ_CLR	R-0/W1C	0h	Clears EtherCATSS IRQ raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the EtherCATSS IRQ, read always returns 0. Reset type: ECAT.IPRSn
1	SYNC1_CLR	R-0/W1C	0h	Clears SYNC1 raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the SYNC1, read always returns 0. Reset type: ECAT.IPRSn

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Table 28-27. ESCSS_INTR_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYNC0_CLR	R-0/W1C	0h	Clears SYNC0 raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 clears the Raw status of the SYNC0, read always returns 0. Reset type: ECAT.IPRSn

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6 ESCSS_INTR_SET Register (Offset = 14h) [Reset = 00000000h]

ESCSS_INTR_SET is shown in Figure 28-23 and described in Table 28-23.

Return to the Summary Table.

Individual Interrupt cause set register to emulate the interrupt cause

Figure 28-23. ESCSS_INTR_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED		MASTER_RESET_SET	TIMEOUT_ERR_SET	DMA_DONE_SET	IRQ_SET	SYNC1_SET	SYNC0_SET
R-0-0h		R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h	R-0/W1S-0h

Table 28-29. ESCSS_INTR_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to Set bits to take effect. Writes of other values will be ignored. Reset type: ECAT.IPRSn
7-6	RESERVED	R-0	0h	Reserved
5	MASTER_RESET_SET	R-0/W1S	0h	Sets EtherCAT Master Reset raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 Sets the Raw status of the PDI Access Timeout Error, read always returns 0. Note this emulation can only assert interrupt to CPU but it can not reset the EtherCAT IP. Reset type: ECAT.IPRSn
4	TIMEOUT_ERR_SET	R-0/W1S	0h	Sets PDI access timeout Error raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 Sets the Raw status of the PDI Access Timeout Error, read always returns 0. Reset type: ECAT.IPRSn
3	DMA_DONE_SET	R-0/W1S	0h	Sets DMA Done raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 Sets the Raw status of the DMA Done, read always returns 0. Reset type: ECAT.IPRSn
2	IRQ_SET	R-0/W1S	0h	Sets EtherCATSS IRQ raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 sets the Raw status of the EtherCATSS IRQ, read always returns 0. Reset type: ECAT.IPRSn

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Table 28-29. ESCSS_INTR_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SYNC1_SET	R-0/W1S	0h	Sets SYNC1 raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 Sets the Raw status of the SYNC1, read always returns 0. Reset type: ECAT.IPRSn
0	SYNC0_SET	R-0/W1S	0h	Sets SYNC0 raw Status (Common Mask & Clear among all hosts, only one host expected accessing). Write 1 sets the Raw status of the SYNC0, read always returns 0. Reset type: ECAT.IPRSn

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7 ESCSS_LATCH_SEL Register (Offset = 18h) [Reset = 00000000h]

ESCSS_LATCH_SEL is shown in Figure 28-24 and described in Table 28-24.

Return to the Summary Table.

Select for LATCH0/1 input Triggers as well as LATCHIN used for registering the GPIs.

Figure 28-24. ESCSS_LATCH_SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R-0-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED			LATCH1_SELECT				
R-0-0h			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			LATCH0_SELECT				
R-0-0h			R/W-0h				

Table 28-31. ESCSS_LATCH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R-0	0h	Reserved
16	RESERVED	R/W	0h	Reserved
15-13	RESERVED	R-0	0h	Reserved
12-8	LATCH1_SELECT	R/W	0h	Mux Select for LATCH1 input to ECATSS. Refer device specification for details of mux select options. Reset type: ECAT.IPRSn
7-5	RESERVED	R-0	0h	Reserved
4-0	LATCH0_SELECT	R/W	0h	Mux Select for LATCH0 input to ECATSS. Refer device specification for details of mux select options. Reset type: ECAT.IPRSn

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8 ESCSS_ACCESS_CTRL Register (Offset = 1Ch) [Reset = 00000400h]

ESCSS_ACCESS_CTRL is shown in Figure 28-25 and described in Table 28-25.

Return to the Summary Table.

Wait state control for EtherCAT access

Figure 28-25. ESCSS_ACCESS_CTRL Register

31	30	29	28	27	26	25	24
RESERVED				TIMEOUT_COUNT			
R-0-0h				R/W-0h			
23	22	21	20	19	18	17	16
TIMEOUT_COUNT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					RESERVED	ENABLE_DEBUG_ACCESS	RESERVED
R-0-0h					R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EN_TIMEOUT	WAIT_STATES						
R/W-0h	R/W-0h						

Table 28-33. ESCSS_ACCESS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R-0	0h	Reserved
27-16	TIMEOUT_COUNT	R/W	0h	This is the cycle count in SYSCLK cycles after which an access on the EtherCAT Async interface will be aborted and CPU will be given back a READY. Reset type: ECAT.IPRSn
15-11	RESERVED	R-0	0h	Reserved
10	RESERVED	R/W	1h	Reserved
9	ENABLE_DEBUG_ACCESS	R/W	0h	Enabled debug accesses through the PDI interface. 0: Debug accesses are not allowed to go through. 1: Debug accesses are allowed through the Bridge. Bridge logic will ensure that access will not hang. Reset type: ECAT.IPRSn
8	RESERVED	R/W	0h	Reserved
7	EN_TIMEOUT	R/W	0h	Enables the Timeout features which counts programmed number of Sys clocks before the Local host aborts the transaction. 0: Timeout feature is not enabled on PDI interface. 1: The timeout counter starts counting upon BUSY is asserted by EtherCAT IP. Reset type: ECAT.IPRSn
6-0	WAIT_STATES	R/W	0h	This is the predefined minimum number of wait-states which the VBUS bridge will put out accesses on the 16-bit Async interface. Reset type: ECAT.IPRSn

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9 ESCSS_GPIN_DAT Register (Offset = 20h) [Reset = 00000000h]

ESCSS_GPIN_DAT is shown in Figure 28-26 and described in Table 28-26.

Return to the Summary Table.

GPI data status for debug & overridwe

Figure 28-26. ESCSS_GPIN_DAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIN_DAT																															
R/W-0h																															

Table 28-35. ESCSS_GPIN_DAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPIN_DAT	R/W	0h	Local GPIN data register connects to GPIN pipelined register for debug & override purposes. Note: The copy of this register readable by the CPU is provided without synchronization, therefore multiple reads should be performed to confirm a stable value before using it. Reset type: ECAT.IPRSn

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10 ESCSS_GPIN_PIPE Register (Offset = 24h) [Reset = 00000000h]

ESCSS_GPIN_PIPE is shown in Figure 28-27 and described in Table 28-27.

Return to the Summary Table.

Register to select raw PAD input or pipelined input be presented to ESC.

Figure 28-27. ESCSS_GPIN_PIPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPI_PIPE																															
R/W-0h																															

Table 28-37. ESCSS_GPIN_PIPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPI_PIPE	R/W	0h	Enables the connection of GPIN to EtherCATSS through pipelined register as against the direct from IO. 0: The connection is directly from the IO pad 1: Connection is through the pipelined register which is captured on programmed event. Reset type: ECAT.IPRSn

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11 ESCSS_GPIN_GRP_CAP_SEL Register (Offset = 28h) [Reset = 00000000h]

ESCSS_GPIN_GRP_CAP_SEL is shown in Figure 28-28 and described in Table 28-28.

Return to the Summary Table.

Register to configure trigger select for the group of 8 IOs together.

Figure 28-28. ESCSS_GPIN_GRP_CAP_SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED	GPI_GRP_CAP_SEL3			RESERVED	GPI_GRP_CAP_SEL2		
R-0-0h	R/W-0h			R-0-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	GPI_GRP_CAP_SEL1			RESERVED	GPI_GRP_CAP_SEL0		
R-0-0h	R/W-0h			R-0-0h	R/W-0h		

Table 28-39. ESCSS_GPIN_GRP_CAP_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R-0	0h	Reserved
14-12	GPI_GRP_CAP_SEL3	R/W	0h	Selects the trigger to capture the IO input in pipeline register for GPI31-24 0: Start Of Frame as capture trigger 1-3: Reserved, selects default value of 0. 4: SYNC0 as capture trigger 5: SYNC1 as capture trigger 6: LATCH0 as capture trigger 7: LATCH1 as capture trigger Reset type: ECAT.IPRSn
11	RESERVED	R-0	0h	Reserved
10-8	GPI_GRP_CAP_SEL2	R/W	0h	Selects the trigger to capture the IO input in pipeline register for GPI23-16 0: Start Of Frame as capture trigger 1-3: Reserved, selects default value of 0. 4: SYNC0 as capture trigger 5: SYNC1 as capture trigger 6: LATCH0 as capture trigger 7: LATCH1 as capture trigger Reset type: ECAT.IPRSn
7	RESERVED	R-0	0h	Reserved
6-4	GPI_GRP_CAP_SEL1	R/W	0h	Selects the trigger to capture the IO input in pipeline register for GPI15-8 0: Start Of Frame as capture trigger 1-3: Reserved, selects default value of 0. 4: SYNC0 as capture trigger 5: SYNC1 as capture trigger 6: LATCH0 as capture trigger 7: LATCH1 as capture trigger Reset type: ECAT.IPRSn

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Table 28-39. ESCSS_GPIN_GRP_CAP_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R-0	0h	Reserved
2-0	GPI_GRP_CAP_SEL0	R/W	0h	Selects the trigger to capture the IO input in pipeline register for GPI7-0 0: Start Of Frame as capture trigger 1-3: Reserved, selects default value of 0. 4: SYNC0 as capture trigger 5: SYNC1 as capture trigger 6: LATCH0 as capture trigger 7: LATCH1 as capture trigger Reset type: ECAT.IPRSn

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12 ESCSS_GPOUT_DAT Register (Offset = 2Ch) [Reset = 00000000h]

ESCSS_GPOUT_DAT is shown in Figure 28-29 and described in Table 28-29.

Return to the Summary Table.

GPO data capture for debug & overridwe

Figure 28-29. ESCSS_GPOUT_DAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPOUT_DAT																															
R-0h																															

Table 28-41. ESCSS_GPOUT_DAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPOUT_DAT	R	0h	Local GPOUT data register which is synchronised version on SysClk, each bit is represents GPO IO Read is allowed for CPU to process (IO extender or so if required). Reset type: ECAT.IPRSn

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13 ESCSS_GPOUT_PIPE Register (Offset = 30h) [Reset = 00000000h]

ESCSS_GPOUT_PIPE is shown in Figure 28-30 and described in Table 28-30.

Return to the Summary Table.

Register to select pipeline of ESC output against direct route to IO pad on per IO based.

Figure 28-30. ESCSS_GPOUT_PIPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPO_PIPE																															
R/W-0h																															

Table 28-43. ESCSS_GPOUT_PIPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPO_PIPE	R/W	0h	Enables the connection of EtherCATSS GPO output to the IO pad through pipelined register as against the direct connection. 0: The connection is directly to the IO pad 1: Connection is through the pipelined register which captures EtherCATSS o/p on programmed event. Reset type: ECAT.IPRSn

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14 ESCSS_GPOUT_GRP_CAP_SEL Register (Offset = 34h) [Reset = 00000000h]

ESCSS_GPOUT_GRP_CAP_SEL is shown in Figure 28-31 and described in Table 28-31.

Return to the Summary Table.

Register to configure trigger select for pipelined register in group of 8 IOs together.

Figure 28-31. ESCSS_GPOUT_GRP_CAP_SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED		GPO_GRP_CAP_SEL3		RESERVED		GPO_GRP_CAP_SEL2	
R-0-0h		R/W-0h		R-0-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		GPO_GRP_CAP_SEL1		RESERVED		GPO_GRP_CAP_SEL0	
R-0-0h		R/W-0h		R-0-0h		R/W-0h	

Table 28-45. ESCSS_GPOUT_GRP_CAP_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R-0	0h	Reserved
13-12	GPO_GRP_CAP_SEL3	R/W	0h	Selects the trigger to capture the EtherCATSS output in pipeline register for GPO31-24 0: End Of Frame as capture trigger 1: SYNC0 as capture trigger 2: SYNC1 as capture trigger 3: WDTrig as capture trigger Reset type: ECAT.IPRSn
11-10	RESERVED	R-0	0h	Reserved
9-8	GPO_GRP_CAP_SEL2	R/W	0h	Selects the trigger to capture the EtherCATSS output in pipeline register for GPO23-16 0: End Of Frame as capture trigger 1: SYNC0 as capture trigger 2: SYNC1 as capture trigger 3: WDTrig as capture trigger Reset type: ECAT.IPRSn
7-6	RESERVED	R-0	0h	Reserved
5-4	GPO_GRP_CAP_SEL1	R/W	0h	Selects the trigger to capture the EtherCATSS output in pipeline register for GPO15-8 0: End Of Frame as capture trigger 1: SYNC0 as capture trigger 2: SYNC1 as capture trigger 3: WDTrig as capture trigger Reset type: ECAT.IPRSn
3-2	RESERVED	R-0	0h	Reserved

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Table 28-45. ESCSS_GPOUT_GRP_CAP_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	GPO_GRP_CAP_SEL0	R/W	0h	Selects the trigger to capture the EtherCATSS output in pipeline register for GPO7-0 0: End Of Frame as capture trigger 1: SYNC0 as capture trigger 2: SYNC1 as capture trigger 3: WDTrig as capture trigger Reset type: ECAT.IPRSn

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15 ESCSS_MEM_TEST Register (Offset = 38h) [Reset = 00000000h]

ESCSS_MEM_TEST is shown in Figure 28-32 and described in Table 28-32.

Return to the Summary Table.

This register controls access to memory test mode

Figure 28-32. ESCSS_MEM_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0-0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	INITIATE_MEM_INIT
R-0-0h						R-0h	R-0/W1S-0h

Table 28-47. ESCSS_MEM_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R-0	0h	Reserved
1	MEM_INIT_DONE	R	0h	Read-only status bit indicating memory initialisation completion. Gets self cleared with INITIATE_MEM_INIT is written '1'. Reset type: ECAT.IPRSn
0	INITIATE_MEM_INIT	R-0/W1S	0h	Memory Initialisation Trigger When set 1 the memory wrapper starts initialisation of DPRAM including parity programming. The bit gets Autocleared after memory initialisation starts. Write of 0 has no effect. Reset type: ECAT.IPRSn

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16 ESCSS_RESET_DEST_CONFIG Register (Offset = 3Ch) [Reset = 00000000h]

ESCSS_RESET_DEST_CONFIG is shown in Figure 28-33 and described in Table 28-33.

Return to the Summary Table.

EtherCAT RESET_OUT configuration

Figure 28-33. ESCSS_RESET_DEST_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
DEVICE_RESET_EN	RESERVED				CPU_INT_EN	CPU_NMI_EN	CPU_RESET_EN
R/W-0h	R-0-0h				R/W-0h	R/W-0h	R/W-0h

Table 28-49. ESCSS_RESET_DEST_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to this register to take effect. Writes of other values will be ignored. Reset type: ECAT.IPRSn
7	DEVICE_RESET_EN	R/W	0h	Enable the EtherCAT RESET_OUT which is combination of IP Reset out and Pin reset to drive the Device Reset (XRSn) 0: EtherCAT RESET_OUT only drives the EtherCATSS & companion component reset to PHY 1: EtherCAT RESET_OUT drives EtherCATSS, external PHY reset and device by connecting this net on to device XRSn User's note: The connection from IP Resetout to EtherCAT RESET_OUT has no relation with this selection. Reset type: ECAT.XRSn
6-3	RESERVED	R-0	0h	Reserved
2	CPU_INT_EN	R/W	0h	Enable for resetout to drive the interrupt to CPU which it belongs to. 0: IP Resetout does not drive the CPU interrupt. 1: IP Resetout drives interrupt to the CPU master to which EtherCATSS belongs. The Host completes the reset through System control Soft reset after completing required context save or tasks if any. Reset type: ECAT.IPRSn
1	CPU_NMI_EN	R/W	0h	Enable for resetout to drive the CPU NMI 0: IP Resetout does not drive the CPU NMI. 1: IP Resetout drives CPU NMI to which it belongs. NMI handler is expected to complete the required taks or context save if any and then reset the EtherCAT through the system control soft reset. Reset type: ECAT.IPRSn

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Table 28-49. ESCSS_RESET_DEST_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CPU_RESET_EN	R/W	0h	Enables EtherCAT Reset to drive the IP & PHY reset 0: EtherCAT Reset does not drive reset connection. 1: EtherCAT Reset drives EtherCAT IP and PHY Reset EtherCAT Reset Combines Master Reset, PDI sequence Reset, RESET_IN, System control soft Reset This selection is to drive the Master & PDI Reset to this combination. When this bit is set 0, application shall configure NMI/Interrupt to eventually complete the reset through system control soft reset. Reset type: ECAT.XRSn

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17 ESCSS_SYNC0_CONFIG Register (Offset = 40h) [Reset = 00000000h]

ESCSS_SYNC0_CONFIG is shown in Figure 28-34 and described in Table 28-34.

Return to the Summary Table.

SYNC0 Triggers enable for Host events like Interrupts, DMA triggers across all masters & GPIO

Figure 28-34. ESCSS_SYNC0_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	DMAx_TRIG_EN	RESERVED	CPUx_INT_EN
R-0-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 28-51. ESCSS_SYNC0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to this register to take effect. Writes of other values will be ignored. Reset type: ECAT.IPRSn
7-5	RESERVED	R-0	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	DMAx_TRIG_EN	R/W	0h	Makes the connection from SYNC0 output to DMA Trigger. 0: SYNC0 does not contribute to DMA trigger. 1: SYNC0 toggle Triggers the DMA Transfer. Reset type: ECAT.IPRSn
1	RESERVED	R/W	0h	Reserved
0	CPUx_INT_EN	R/W	0h	Makes the connection from SYNC0 output to CPUx Interrupt. 0: SYNC0 does not contribute to CPUx Interrupt regardless of mask. 1: SYNC0 follows the PIE interrupt behavior as controlled by RIS,MASK,CLR register pairs. Reset type: ECAT.IPRSn

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18 ESCSS_SYNC1_CONFIG Register (Offset = 44h) [Reset = 00000000h]

ESCSS_SYNC1_CONFIG is shown in Figure 28-35 and described in Table 28-35.

Return to the Summary Table.

SYNC1 Triggers enable for Host events like Interrupts, DMA triggers across all masters & GPIO

Figure 28-35. ESCSS_SYNC1_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED			RESERVED	RESERVED	DMAx_TRIG_EN	RESERVED	CPUx_INT_EN
R-0-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 28-53. ESCSS_SYNC1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to this register to take effect. Writes of other values will be ignored. Reset type: ECAT.IPRSn
7-5	RESERVED	R-0	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	DMAx_TRIG_EN	R/W	0h	Makes the connection from SYNC1 output to DMA Trigger. 0: SYNC1 does not contribute to DMA trigger. 1: SYNC1 toggle Triggers the DMA Transfer. Reset type: ECAT.IPRSn
1	RESERVED	R/W	0h	Reserved
0	CPUx_INT_EN	R/W	0h	Makes the connection from SYNC1 output to CPUx Interrupt. 0: SYNC1 does not contribute to CPUx Interrupt regardless of mask. 1: SYNC1 follows the interrupt behavior as controlled by RIS,MASK,CLR register pairs. Reset type: ECAT.IPRSn

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28.6.3 ESCSS_CONFIG_REGS Registers

Table 28-36 lists the memory-mapped registers for the ESCSS_CONFIG_REGS registers. All register offset addresses not listed in Table 28-36 should be considered as reserved locations and the register contents should not be modified.

Table 28-54. ESCSS_CONFIG_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	ESCSS_CONFIG_LOCK	EtherCATSS Configuration Lock		Go
4h	ESCSS_MISC_IO_CONFIG	RESET_IN, EEPROM IO connections select		Go
8h	ESCSS_PHY_IO_CONFIG	Control Register of ESCSS		Go
14h	ESCSS_GPIN_SEL	GPIN Select between IO PAD & tieoff		Go
28h	ESCSS_MISC_CONFIG	Miscelleneous Configuration		Go

Complex bit access types are encoded to fit into small table cells. Table 28-37 shows the codes that are used for access types in this section.

Table 28-55. ESCSS_CONFIG_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WSonce	W Sonce	Write Set once
Reset or Default Value		
-n		Value after reset or the default value

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1 ESCSS_CONFIG_LOCK Register (Offset = 0h) [Reset = 00000000h]

ESCSS_CONFIG_LOCK is shown in Figure 28-36 and described in Table 28-38.

Return to the Summary Table.

Lock bit for EtherCAT configuration registers

Figure 28-36. ESCSS_CONFIG_LOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED			IO_CONFIG_ENABLE	RESERVED			LOCK_ENABLE
R-0-0h			R/W-0h	R-0-0h			R/WSonce-0h

Table 28-57. ESCSS_CONFIG_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to bit 0 take effect. Writes of other values will be ignored. Reset type: ECAT.XRSn
7-5	RESERVED	R-0	0h	Reserved
4	IO_CONFIG_ENABLE	R/W	0h	This bit enables the IO configurations allowing the EtherCAT ports to take effect. Till this bit is written EtherCAT ports are not connected to the IO pad. Enable takes effect when this bit is set to 1. Changing IO selections or IO configurations after this bit is set can have unpredictable IO behavior on the device IOs. Reset type: ECAT.XRSn
3-1	RESERVED	R-0	0h	Reserved
0	LOCK_ENABLE	R/WSonce	0h	This bit enables locking the contents of all the EtherCAT configuration registers. The lock takes effect when this bit is set to 1. This bit can be set only once after ecatXRSN and gets reset after the next ecatXRSN. Reset type: ECAT.XRSn

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2 ESCSS_MISC_IO_CONFIG Register (Offset = 4h) [Reset = 00000002h]

ESCSS_MISC_IO_CONFIG is shown in Figure 28-37 and described in Table 28-39.

Return to the Summary Table.

Condiguration of RESET_IN, EEPROM I2C connections

Figure 28-37. ESCSS_MISC_IO_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED						EEPROM_I2C_IO_EN	RESERVED
R-0-0h						R/W-1h	R/W-0h

Table 28-59. ESCSS_MISC_IO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to this register to take effect. Writes of other values will be ignored. Reset type: ECAT.XRSn
7-2	RESERVED	R-0	0h	Reserved
1	EEPROM_I2C_IO_EN	R/W	1h	Enables connecting EtherCAT I2C connections to IOPAD for EEPROM control 0: EEPROM I2C Connections are not connected to IOPAD. 1: EEPROM I2C connections are driving the IOPAD connections. Reset type: ECAT.XRSn
0	RESERVED	R/W	0h	Reserved

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3 ESCSS_PHY_IO_CONFIG Register (Offset = 8h) [Reset = 00000044h]

ESCSS_PHY_IO_CONFIG is shown in Figure 28-38 and described in Table 28-40.

Return to the Summary Table.

PHY Type, clock source type select

Figure 28-38. ESCSS_PHY_IO_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
WRITE_KEY							
R-0/W-0h							
7	6	5	4	3	2	1	0
RESERVED	TX_CLK_AUTO_COMP	RESERVED		PHY_PORT_CNT		RESERVED	
R/W-0h	R/W-1h	R/W-0h		R/W-1h		R/W-0h	

Table 28-61. ESCSS_PHY_IO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R-0	0h	Reserved
15-8	WRITE_KEY	R-0/W	0h	The key value should be 0xa5 for the writes to bit 0 take effect. Writes of other values will be ignored. Reset type: ECAT.XRSn
7	RESERVED	R/W	0h	Reserved
6	TX_CLK_AUTO_COMP	R/W	1h	This setting is used to allocate the IO pad for TX_CLK for doing the Auto compensation for the samlping of TXEN & TXDATA. 0 : Manual Compensation using CLK_IN no TX_CLK Pad, IP input is tied to '0'. 1: Auto Compensation based on sampling of TX_CLK. Pad is allocated. Reset type: ECAT.XRSn
5-4	RESERVED	R/W	0h	Reserved
3-2	PHY_PORT_CNT	R/W	1h	Indicates the number of PHY ports selected for operation inaddition to Port0 which is default (information only, doesn't change configuration) 00-One port operation (Port0) 01-Two port operation(Port0,Port1) 10-Three port operation(Port0,Port1,Port2) : Reserved 11-Four port operation(Port0,Port1,Port2,Port3): Reserved Programming reserved configuration causes selection of Reset value. Reset type: ECAT.XRSn
1-0	RESERVED	R/W	0h	Reserved

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4 ESCSS_GPIN_SEL Register (Offset = 14h) [Reset = 00000000h]

ESCSS_GPIN_SEL is shown in Figure 28-39 and described in Table 28-41.

Return to the Summary Table.

Register to configure each GPI input is connected to IO-pad or not.

Figure 28-39. ESCSS_GPIN_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIN_SEL																															
R/W-0h																															

Table 28-63. ESCSS_GPIN_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPIN_SEL	R/W	0h	Allows bit-wise selection of the GPIN be connected from GPIO PAD. Once those are not driven by GPIO, will be driven from register writable from local Host. 0: No connection to GPIO PAD, but connects to ESCSS_GPIN_DAT. 1: Mux Select the GPIN from the dedicated IO PAD. For devices that have less than 32 GPIN IO PADs allocated, these selection bits corresponding to the higher unallocated GPIN bits should be left at the default value of '0' to select ECSS_GPIN_DAT as the driver for those bits. Reset type: ECAT.XRSn

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5 ESCSS_MISC_CONFIG Register (Offset = 28h) [Reset = 00000000h]

ESCSS_MISC_CONFIG is shown in Figure 28-40 and described in Table 28-42.

Return to the Summary Table.

Configuration info for the MII interface containing TX_SHIFT compensation values, PHY Address offset, EEPROM SIZE etc.

Figure 28-40. ESCSS_MISC_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_ADDR		
R-0-0h					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADDR		PDI_EMULATION	EEPROM_SIZE	TX1_SHIFT_CONFIG		TX0_SHIFT_CONFIG	
R/W-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 28-65. ESCSS_MISC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R-0	0h	Reserved
10-6	PHY_ADDR	R/W	0h	These bits will be hooked up to the PHY_OFFSET[4:0] input of the EtherCAT IP. Reset type: ECAT.XRSn
5	PDI_EMULATION	R/W	0h	This bit will be hooked up to the PDI_EMULATION input of the EtherCAT IP. Reset type: ECAT.XRSn
4	EEPROM_SIZE	R/W	0h	This bit will be hooked up to the EEPROM_SIZE input of the EtherCAT IP . This is set to 0 for EEPROMs of size 16K bits or lower. This is set to 1 for EEPROMs of size above 16K bits. Reset type: ECAT.XRSn
3-2	TX1_SHIFT_CONFIG	R/W	0h	Two bit TX_SHIFT configuration in terms of 10ns counts for port0. This is the shift added to TX_ENA & TX_DATA to match delay of PHY TX_CLK w.r.t. device internal clock. Reset type: ECAT.XRSn
1-0	TX0_SHIFT_CONFIG	R/W	0h	Two bit TX_SHIFT configuration in terms of 10ns counts for port0. This is the shift added to TX_ENA & TX_DATA to match delay of PHY TX_CLK w.r.t. device internal clock. Reset type: ECAT.XRSn

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Chapter 29

Fast Serial Interface (FSI)

This chapter contains a general description of the Fast Serial Interface (FSI) module. The FSI is a serial peripheral capable of reliable high-speed communication across isolation barriers.

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29.1 Introduction

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable high-speed communication across isolation devices. Galvanic isolation devices are used in situations where two different electronic circuits, which do not have common power and ground connections, must exchange information. Though isolation devices facilitate these signal communications, isolation devices can also introduce a large delay on the signal lines and add skew between the signals. The FSI is designed specifically to make sure reliable high-speed communication for system scenarios that involve communication across isolation barriers without adding components.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently.

For additional information on the FSI module, refer to *Fast Serial Interface (FSI) Skew Compensation*.

29.1.1 FSI Features

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Double Data Rate (DDR)
- One or two data lines
- Programmable data length
- DMA support
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally-triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- FSI-SPI compatibility mode (limited features available)
- Tag match notifications

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29.1.2 Signal Description

FSI is a point-to-point communication protocol. Hence, an FSI transmitter core communicates directly to a single FSI receiver core. Similarly, an FSI receiver core receives data from a single FSI transmitter core.

Each FSI core has three signals: one clock and two data signals. Data is always transmitted or received with the most-significant bit of each frame field being first. If multilane transmissions are not used, the TXD1 and RXD1 signals can be left unconnected and the GPIOs repurposed for other application needs. Table 29-1 and Table 29-2 describe the various signals that can be selected by the IOMUX to be brought out to device pins.

CAUTION

The maximum RXCLK rate is MCLK/2 and must not exceed this limit.

Table 29-1. FSI Receiver Core Signals

Signal Name	Direction	Description	Inactive Level(1)
RXCLK	Input	This is the receive clock input signal for the FSI receive module. This must be connected to TXCLK of the transmitting FSI module.	Logic High
RXD0	Input	This is the primary data input line for reception. This must be connected to the TXD0 of the transmitting FSI module.	Logic High
RXD1	Input	This is an additional data input line for reception. This signal must be connected to the TXD1 of the transmitting FSI module to use multilane transmission.	Logic High

(1) Inactive level refers to the state of the pin while the module is not actively receiving data.

Table 29-2. FSI Transmitter Core Signals

Signal Name	Direction	Description	Inactive Level(1)
TXCLK	Output	This is the transmit clock and is driven by the FSI transmit module. During a transmission, four clock edges are transmitted before the start of frame phase (preamble) and four clock edges follow the last bit of the frame (postamble). Data is transmitted on both edges of the clock. In FSI-SPI compatibility mode, the preamble and the post frame clock edges are not transmitted. Data is transmitted only on one edge of the clock. Data transmits on rising edge and received on falling edge of the clock.	Logic High
TXD0	Output	This is the primary data output line for transmission and is driven by the FSI transmit module. When the FSI is configured for multilane transmission, TXD0 contains all the even numbered bits of the data and CRC bytes. Other frame fields such as frame type, start-of-frame, tag, and end-of-frame are transmitted in full.	Logic High
TXD1	Output	This is an additional data output line for transmission, if the FSI is configured for multilane transmission. This signal is driven by the FSI transmit module. During transmission, the data bits are split between TXD0 and TXD1. TXD1 contains all the odd numbered bits of the data and CRC bytes. This applies only to the data words and the CRC bytes. Other data frame related information like Frame Type, Start-of-Frame, Tag and End-of-frame, the state of this line are identical to TXD0.	Logic High

(1) Inactive level refers to the state of the pin while the module is not actively transmitting, or held in reset.

29.2

The Fast Serial Interface Transmitter and Receiver modules (FSI_TX/FSI_RX) are two completely independent modules on the device. Each module has an independent set of control registers, clocking, and interrupts. The

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following sections describe the frame format and the various initialization and configuration procedures for both the transmitter and receiver.

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29.2.1 FSI Transmitter Module

The FSI transmitter module handles the framing of data, CRC generation, and signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers allow the CPU to program, control, and monitor the operation of the FSI receiver. The transmit data buffer is accessible by the CPU and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support

Figure 29-1 shows the high-level block diagram of the FSI transmitter. Figure 29-2 shows the block diagram of the transmitter core submodule.

The following sections describe the various aspects of the FSI transmitter in detail.

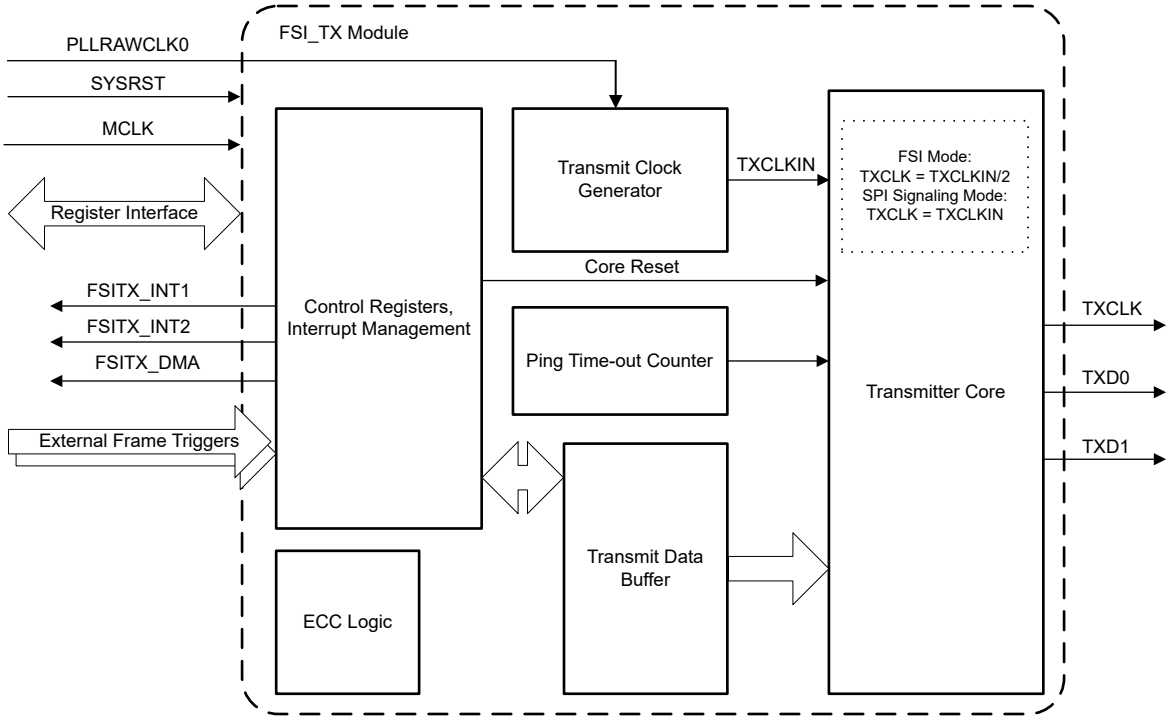


Figure 29-1. FSI Transmitter Block Diagram

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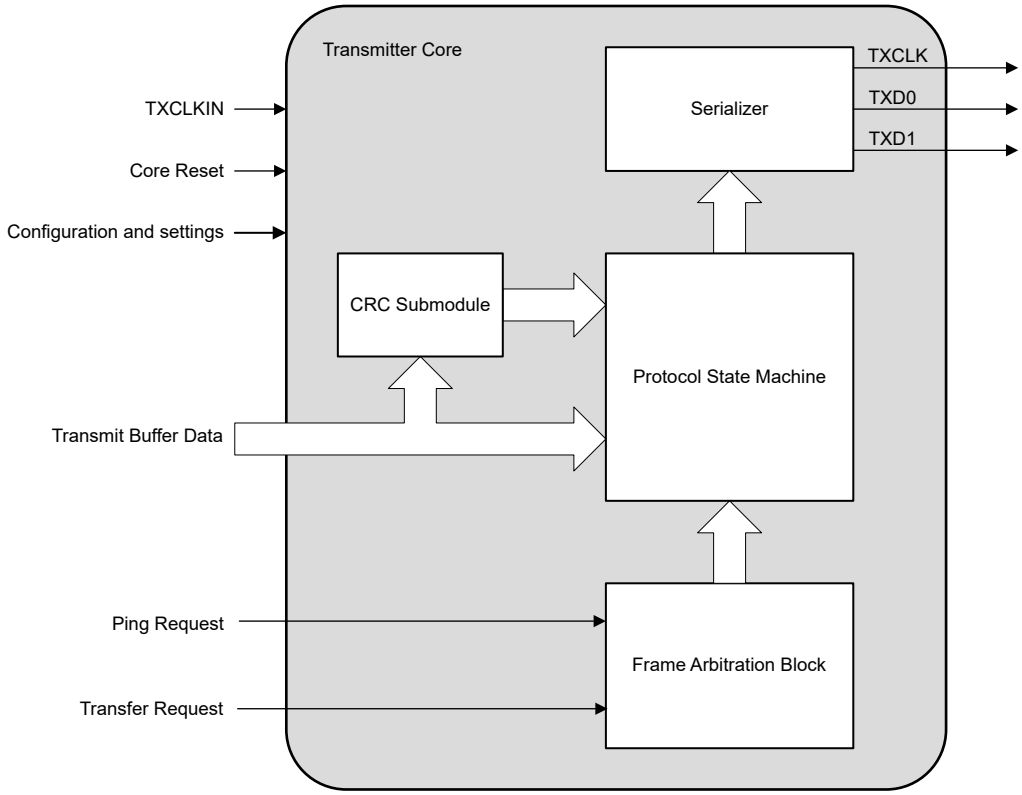


Figure 29-2. FSI Transmitter Core Block Diagram

29.2.1.1 Initialization

On the first initialization or after a module reset due to an underrun condition, the transmitter module executes the following initialization sequence to start or resume transmit operations.

1. Initialize the transmitter clock by setting TX_CLK_CTRL.CLK_RST to 1 and subsequently clearing the bit.
2. Set the clock to the transmitter core to PLLRAWCLK0 by setting TX_OPER_CTRL_LO.SEL_PLLCLK to 1.
3. Set the clock prescaler value to the desired rate by writing to TX_CLK_CTRL.PRESCALE_VAL.
4. Enable the transmitter clock divider by setting TX_CLK_CTRL.CLK_EN to 1.
5. Assert the transmitter module soft reset by writing 0xA501 to TX_MAIN_CTRL.
6. Wait four TXCLK cycles.
7. Release the transmitter core from reset by writing 0xA500 to TX_MAIN_CTRL.

After initialization and configuration, the transmitter module synchronizes with the receiver module before transmitting. The synchronization sequence is described in Section 29.3.1 .

CAUTION

Do not change TX_CLK_CTRL.PRESCALE_VAL while the clock is enabled (TX_CLK_CTRL.CLK_EN = 1). Doing so can cause undefined behavior.

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29.2.1.2 FSI_TX Clocking

The transmitter core registers and control logic run off of the device system clock (MCLK).

The FSI Transmit Clock (TXCLK) is derived from PLLRAWCLK0. PLLRAWCLK0 is divided down by configuring the clock prescaler value (TX_CLK_CTRL.PRESCALE_VAL) then setting the clock divider enable bit (TX_CLK_CTRL.CLK_EN). The clock prescaler value can be set to divide PLLRAWCLK0 by 1 (TX_CLK_CTRL.PRESCALE_VAL = 0x0 or 0x1) through 255(TX_CLK_CTRL.PRESCAL_VAL = 0xFF). Though TXCLK and MCLK are both derived from PLLRAWCLK0, TXCLK is asynchronous with respect to MCLK.

CAUTION

TXCLK must never be configured to be faster than MCLK/2.

29.2.1.3 Transmitting Frames

On the transmitter, the ping frame is the only frame that can be set up and transmitted without any further software or DMA intervention. Ping frames can be transmitted by any (or all) of the three sources: automatic ping timer, software, or external triggers.

Each available frame type can be sent multiple ways. Generically, the following steps must be executed before the frame is sent. These steps can be executed in any order before the start condition is set.

1. Configure the frame type
2. Set the frame tag
3. If the frame to be sent is a data frame:
   - Set the user data
   - Write to the data buffer
   - Set the word length if the frame is a software defined frame length
4. Set the start condition

Note

Transmit Frame Start Restriction:

A new frame transmission can be initiated by one of the methods selected in the TX_OPER_CTRL_LO.START_MODE bits. If there is already a PING frame transmission taking place, due to a hardware initiated PING timer, the new frame transmission begins as soon as the on-going PING transmission is completed.

Once a START of frame has been initiated, the next START of frame is recognized when the first frame has started transmitting the End-of-Frame (EOF) field. If a new START trigger arrives before the current transmission has reached the EOF field, the trigger is lost without a notification.

Note

There is no hardware check implemented to check whether the type field written by software is valid or not. If an invalid type is used and a frame transmission is initiated, the behavior is:

- The transmitted frame structure is exactly like an NWORD data frame. The size of the data frame is determined by the value in the TX_FRAME_CTRL.N_WORDS register.
- The frame type field of the transmitted data frame is transmitted as programmed. If this is received by an FSI receiver, a Type error is generated.

This mechanism can be used for force a Type error in a received frame for testing purposes.

The following sections describe the specific configuration for each frame type and start condition.

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29.2.1.3.1 Software Triggered Frames

The most basic way to transmit a data frame is through software. Each step must be handled by the application. To send a data frame using software, the following steps must be executed. Steps 1-6 can be executed in any order before setting TX_FRAME_CTRL.START. Some fields do not need to be reconfigured for every transmission. The frame tag, user data, and frame type are sticky and are retransmitted in the subsequent frame unless modified by software.

1. Write the data to be transmitted to the next location of the transmit data buffer.
2. Set TX_FRAME_CTRL.FRAME_TYPE to the appropriate value for the type of frame to be transmitted.
3. Set TX_FRAME_CTRL.N_WORDS to 1 less than the number of words to be transmitted if TX_FRAME_CTRL.FRAME_TYPE is set to 0011, the frame type of the software-defined length data frame. That is, if 16 words are transmitted, N = 16, set TX_FRAME_CTRL.N_WORDS to 15.
4. When the frame is assembled before transmitting, the FSITX hardware calculates the CRC to be transmitted. If TX_OPER_CTRL_LO.SW_CRC is 1, the application can calculate a custom CRC value and then set TX_USER_CRC to the result.
5. Set TX_FRAME_TAG_UDATA.FRAME_TAG to the desired tag.
6. Set TX_FRAME_TAG_UDATA.USER_DATA to the desired user data.
7. Set TX_FRAME_CTRL.START to 1 to initiate the transmission of the data frame.

Once the frame transmission has started, the TX_FRAME_CTRL.START is cleared by hardware. To monitor if the frame has completed, the software can poll TX_EVT_STS.FRAME_DONE.

29.2.1.3.2 Externally Triggered Frames

The transmitter can transmit frames when triggered by an external source. See Section 29.2.1.3.2.1 for more information on the available external triggers.

To transmit frames using an external trigger, the application must follow the same procedure as described in Section 29.2.1.3.1 . The only difference is that in Step 7, the start condition is automatically set when the external trigger condition is met rather than by software.

Note that by externally triggering frames, the frame information to be sent is pulled from the same registers described in the previous section. Because of this, it is possible to send any type of frame from an external trigger including ping, error, and data frames. Also, there is no hardware mechanism by which the FSI can determine if multiple triggers occur. The FSITX takes the data as is, and the application software makes sure that this data has been updated as necessary.

Using TX_EVT_STS fields either by polling or by interrupts, the application can populate or update the frame information to be sent in the next frame

29.2.1.3.2.1 External Frame Trigger Mux

The FSI has two muxes connected to the transmitter module. These muxes are used to select triggers to start ping frames, and generic frames. These muxes are independently configured for each type of frame. The application can select one trigger source per frame type. Use of these triggers are optional.

The external ping frame trigger is configured by setting TX_PING_CTRL.EXT_TRIG_SEL to the index of the desired trigger. TX_PING_CTRL.EXT_TRIG_EN must also be set to allow the trigger to generate a ping frame.

The generic frame trigger is configured by setting TX_OPER_CTRL_HI.EXT_TRIG_SEL to the index of the desired trigger. TX_OPER_CTRL_LO.START_MODE must be set to 0x1 for a frame to be transmitted by an external trigger.

Note

Triggers generated by PWM XBAR are asynchronous and must be at least 3 MCLKs wide.

Table 29-3. External Trigger Sources and Their Index

EXT_TRIG_SEL	External Trigger Source
0	PWMXBAR1

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Table 29-3. External Trigger Sources and Their Index (continued)

EXT_TRIG_SEL	External Trigger Source
1	PWMXBAR2
2	PWMXBAR3
3	PWMXBAR4
4	PWMXBAR5
5	PWMXBAR6
6	PWMXBAR7
7	PWMXBAR8
8	MCPWM0_SOCA
9	MCPWM0_SOCB
10	MCPWM0_SOCC
11	MCPWM0_SOCD
12	MCPWM1_SOCA
13	MCPWM1_SOCB
14	MCPWM1_SOCC
15	MCPWM1_SOCD
16	MCPWM2_SOCA
17	MCPWM2_SOCB
18	MCPWM2_SOCC
19	MCPWM2_SOCD
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	EPWM0_SOCA
29	EPWM0_SOCB
30	EPWM1_SOCA
31	EPWM1_SOCB
32	EPWM2_SOCA
33	EPWM2_SOCB
34	EPWM3_SOCA
35	EPWM3_SOCB
36	EPWM4_SOCA
37	EPWM4_SOCB
38	EPWM5_SOCA
39	EPWM5_SOCB
40	ADCSOCA
41	ADCSOCB
42	TIMG4.CPU_INT
43	TIMG12.CPU_INT
44	DMA.CPU_INT
45	FSIRX_TRIG0

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Table 29-3. External Trigger Sources and Their Index (continued)

EXT_TRIG_SEL	External Trigger Source
46	FSIRX_TRIG1
47	FSIRX_TRIG2
48	FSIRX_TRIG3
49-127	Reserved

29.2.1.3.3 Ping Frame Generation

Assuming the FSI transmitter has already been properly initialized, the following sequences can be used to configure and send ping frames.

29.2.1.3.3.1 Automatic Ping Frames

To generate periodic ping frames, the following steps must be followed:

1. Initialize the ping counter by writing 1 to TX_PING_CTRL.CNT_RST.
2. Set the desired ping tag to TX_PING_TAG.TAG.
3. Set the ping timer reference value to TX_PING_TO_REF.TO_REF.
4. Enable the ping timer by writing 1 to TX_PING_CTRL.TIMER_EN.

The ping timer is a free-running counter that counts up from 0. The current value of the ping timer counter is found in TX_PING_TO_CNT. When the current value of TX_PING_TO_CNT matches the reference value TX_PING_TO_REF.TO_REF, the TX_EVT_STS.PING_TRIGGERED is set. TX_PING_TO_CNT resets to 0 and resumes counting until the next match has occurred or the ping timer is halted by software (TX_PING_CTRL.TIMER_EN is set to 0).

29.2.1.3.3.2 Software Triggered Ping Frame

Software can also manually generate a ping frame. The process for sending a ping frame with software is very similar to sending the other types of frames. The following steps must be followed:

1. Set TX_FRAME_CTRL.FRAME_TYPE to 0000’b to denote that the frame being sent is a Ping Frame.
2. Set TX_FRAME_TAG_UDATA.FRAME_TAG to the desired value.
3. Write 1 to TX_FRAME_CTRL.START. This starts the transmission.

Once the frame transmission has started, the TX_FRAME_CTRL.START is cleared by hardware. To monitor if the frame has completed, the software can poll TX_EVT_STS.FRAME_DONE.

29.2.1.3.3.3 Externally Triggered Ping Frame

The last source for generating ping frames is an external trigger. One of up to 32 different triggers can be selected. See Section 29.2.1.3.2.1 for the list of input sources.

CAUTION

Ping frames can be triggered by both an external trigger source and the internal ping timer. If TX_PING_CTRL.EXT_TRIG_EN is set to 1, the external trigger source takes precedence and the ping timer is ignored.

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29.2.1.4 Transmit Buffer Management

The FSI transmitter has a 16-word buffer that the FSI transmitter pulls data to transmit. This buffer is implemented as a circular buffer, not a FIFO, so some care must be taken to properly interpret buffer overrun and underrun, as well as the TX_BUF_PTR_STS register. These flags and pointers work under the assumption that the software or DMA is using the buffer as a circular buffer. This mode of operation is the only way that the overrun, underrun, and pointer status are meaningful. If data is being sourced by the DMA and there is some other periodic trigger mechanism trying to initiate transfers, underrun becomes a critical error. If an underrun happens, a buffer went out of sync. This not only affects the current transfer, but can also affect all future transfers due to the ring buffer. Under such conditions, the underrun needs a soft reset to cleanly recover. Alternately, the software can manually stop the transmitting, reset the buffer pointers, clear the remaining error conditions, and then restart transmission. The software method involves a few steps, while the soft reset is a single action and makes sure of a full reset of the control registers.

Due to the flexibility of the transmit buffer, software can implement a simple ping-pong buffer or randomly load and send from any location of the buffer. If the buffer is used in this manner, error flags and status fields can be ignored without adversely affecting the transmitter capability. Additionally, the CURR_WORD_CNT is also invalid if used in this way. The application can set the buffer pointer manually by writing the 4-bit index to TX_BUF_PTR_LOAD. This forces the transmitter to start picking the data from the indicated location in the buffer.

29.2.1.5 CRC Submodule

The FSI transmitter can supply the CRC to the frame being transmitted through the embedded hardware CRC submodule or by supplying a user-defined value. This is controlled by setting TX_OPER_CTRL_LO.SW_CRC appropriately.

If hardware CRC generation is selected (TX_OPER_CTRL_LO.SW_CRC = 0, the default), the CRC is computed by hardware on the data and user data fields using the CRC polynomial 0x7 ($x^8 + x^2 + x + 1$). The transmitter module automatically computes the CRC on the data fields without user intervention when the frame is transmitted. For more information on how the CRC is generated by the CRC submodule, refer to Section 29.2.6 .

If software CRC generation is selected (TX_OPER_CTRL_LO.SW_CRC = 1), the CRC must be computed by software and placed in the TX_USER_CRC register. The next frame to be transmitted uses the value placed in the TX_USER_CRC register in place of the CRC value generated by the hardware.

As the TX_USER_CRC register is software-programmable, the application can use this field as an extra data field for application-specific purposes. If TX_USER_CRC is used in this manner, the CRC detection on the receiver is not valid and must be ignored.

29.2.1.6 Conditions in Which the Transmitter Must Undergo a Soft Reset

Unlike the receiver, there are no detectable errors that require a soft reset. A buffer overrun or underrun interrupt can or cannot require a soft reset to resume proper operation. This determination is up to the application software. Refer to Section 29.2.1.4 for more information on the transmit buffer.

29.2.1.7 Reset

The entire transmitter module and all transmitter registers are reset by SYSRST. The transmitter core is reset by SYSRST or by writing a 1 to TX_MAIN_CTRL.CORE_RST.

A module reset causes the registers to be reset to the default state.

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29.2.2 FSI Receiver Module

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after the data lines pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers allow the CPU to program, control, and monitor the operation of the FSI receiver. The receive data buffer is accessible by the CPU and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- FSI-SPI compatibility mode

Figure 29-3 provides a high-level overview of the internal modules present in the FSI receiver. Figure 29-4 shows a view of the FSI receiver core submodule. Not all data paths and internal connections are shown.

The following sections describe the various aspects of the FSI receiver module.

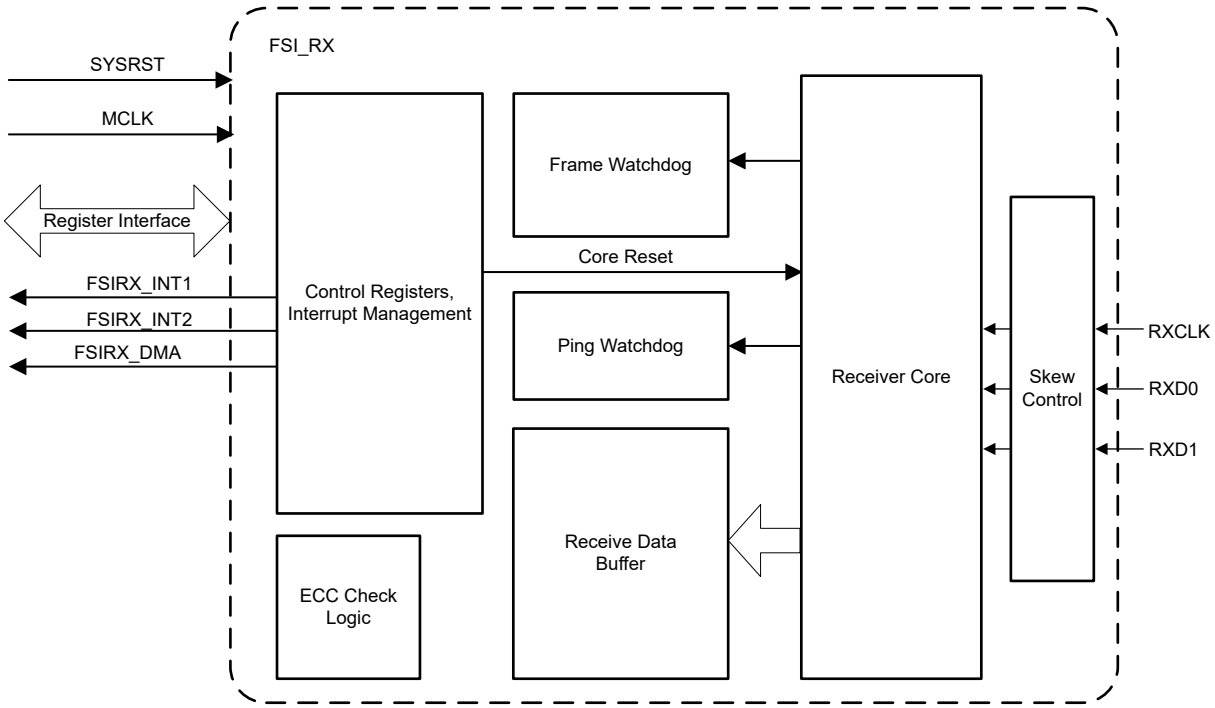


Figure 29-3. FSI Receiver Block Diagram

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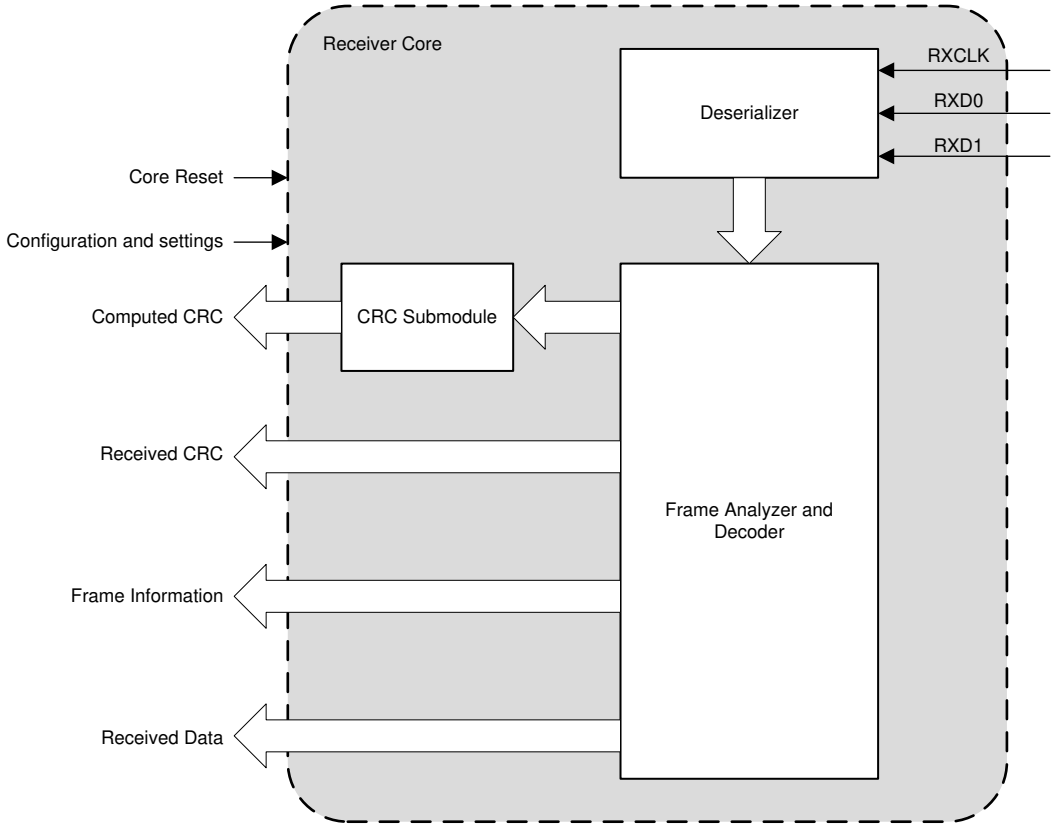


Figure 29-4. FSI Receiver Core Block Diagram

29.2.2.1 Initialization

On the first initialization or after a module reset following any frame error, the receiver module asserts and releases the receiver core reset bit (RX_MAIN_CTRL.CORE_RST) prior to any other initialization. Once the receiver module is initialized, the following steps are executed:

1. If required, assign interrupt sources to the necessary interrupt line.
2. If required, configure the ping watchdog to periodically check for an active link to the transmitter. See Section 29.2.2.4 for configuration details.
3. If required, configure the frame watchdog to make sure that each frame is received within a predetermined window. See Section 29.2.2.5 for configuration details.
4. Initialize the receive buffer pointer by writing to the RX_BUF_PTR_LOAD register. Received data is placed into the buffer starting with the address loaded in this register.
5. Make sure all errors and flags have been cleared from the RX_EVT_STS register.

At this point the receiver is ready to receive any incoming frames. Software can now either poll on the RX_EVT_STS register for various conditions. For example, when the RX_EVT_STS.FRAME_DONE and no other flags are set, the receiver has successfully received a frame without error.

Next, the application configures the various features such as the ping and frame watchdogs, DMA, external triggering, and so on. These features are described in subsequent sections. The receiver module is now ready to synchronize with the transmitter then begin reception. The synchronization sequence is described in Section 29.3.1 .

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29.2.2.2 FSI_RX Clocking

The receiver module registers and control logic are clocked by the device system clock (MCLK). The receiver state machine is clocked by the receiver input clock pin (RXCLK).

CAUTION

RXCLK must never be faster than MCLK.

29.2.2.3 Receiving Frames

Once the receiver has been properly configured and synchronized, incoming messages are handled as described below. Note that there is no equivalent to a chip-select signal to gate incoming data. Every valid clock edge latches data into the receiver.

The header information of the received frame is placed in the respective register fields.

- RX_FRAME_INFO.FRAME_TYPE contains the received frame type.
- RX_FRAME_TAG_UDATA.FRAME_TAG contains the received frame tag.
- RX_FRAME_TAG_UDATA.USER_DATA contains the received user data.

If any error conditions occur during reception such as a CRC mismatch, frame error, frame timeout, buffer overrun, or ping watchdog timeout, the corresponding flag is set in the RX_EVT_STS register.

Note

If at any point during operation a frame error occurs, the receiver module must be reset and re-synchronized with the transmitter before the next frame can be successfully received. The follow errors are classified as frame errors:

- Type error
- CRC error
- End of frame error

29.2.2.4 Ping Frame Watchdog

The ping frame watchdog is a hardware-enabled automatic error detection of the connection status to the transmitter. This watchdog monitors the time elapsed between ping frames. If the transmitter has been set up to periodically send out a ping frame, the receiver can be set up to monitor whether this frame has been received within a specified amount of time. If the time between ping frames has exceeded the programmed number of clock cycles, an event is triggered that can generate an interrupt or be monitored by software.

This watchdog has a dedicated counter that is reset and restarted upon the successful reception of a ping frame. The watchdog counter is incremented at the rate of MCLK. Optionally, the watchdog can be configured to be reset upon the successful reception of any frame. This option allows the receiver to monitor for any successful frame to indicate that the connection is still alive and the transmitter is still functioning as expected.

To configure the ping frame watchdog for operation:

1. Reset the ping watchdog counter by setting RX_PING_WD_CTRL.PING_WD_RST to 1 and then subsequently clearing the bit to 0.
2. Set RX_OPER_CTRL.PING_WD_RST_MODE to the desired watchdog reset event, set to 0 for ping frames only or set to 1 for any frame.
3. Set RX_PING_WD_REF to the maximum time between frames. Add 10 additional MCLK cycles to account for clock synchronization.
4. Enable the ping watchdog by setting RX_PING_WD_CTRL.PING_EN to 1.

The ping watchdog is now enabled and can now monitor for ping frames.

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If the RX_PING_WD_CNT value reaches the value programmed in RX_PING_WD_REF, the RX_EVT_STS.PING_WD_TO flag is set. If configured, an interrupt can be generated on this event.

29.2.2.5 Frame Watchdog

The frame watchdog is an additional feature the receiver can use to monitor for any error conditions. This dedicated watchdog monitors the duration for a single frame to be received. The watchdog starts incrementing at the time the receiver detects a proper start of frame condition. If the end of frame condition is not detected within the expected number of MCLK cycles, the frame watchdog is triggered that can generate an interrupt or be monitored by software.

This watchdog is automatically started and stopped at the start-of-frame and end-of-frame conditions, respectively. The frame watchdog is connected to MCLK.

To configure the frame watchdog for operation:

1. Reset the frame watchdog counter by setting RX_FRAME_WD_CTRL. FRAME_WD_CNT_RST to 1 and then subsequently clearing the bit to 0.
2. Set RX_FRAME_WD_REF.FRAME_WD_REF to the maximum number of MCLK cycles expected to be in the longest frame that can be received. Add an additional 10 MCLK cycles to account for clock synchronization.
3. Enable the frame watchdog by setting RX_FRAME_WD_CTRL.FRAME_WD_CNT_EN to 1.

The frame watchdog is now enabled and can detect a failed frame.

If the RX_FRAME_WD_CNT reaches the value programmed in RX_FRAME_WD_REF, the RX_EVT_STS.FRAME_WD_TO flag is set. If enabled, an interrupt can be generated on this event.

If the frame watchdog interrupt ever occurs, the receiver core is in an invalid state to receive a new transmission. The only way to recover from a frame watchdog time out is to undergo a soft reset, and subsequently resynchronizing with the transmitter.

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29.2.2.6 Delay Line Control

The receiver module has a programmable delay line on each of the external signal inputs: RXCLK, RXD0, and RXD1. The delay elements introduce delays on the respective lines. This is to facilitate adjustment for signal delays introduced by system level components such as signal buffers, ferrite beads, isolators, and so on, or board delays such as uneven trace lengths, long cable length, and so on. The length of the delay is controlled by setting the RX_DLY_LINE_CTRL register values for each line. By default, no delay is introduced by the delay line elements. The delay values must only be adjusted while the FSIRX is held in soft reset, making sure that there are no active transmissions during this process. Figure 29-5 shows a representation of the delay line circuitry for the input signals. The implementation for RXCLK, RXD0, and RXD1 are replicas of this diagram. All circuits behave similarly.

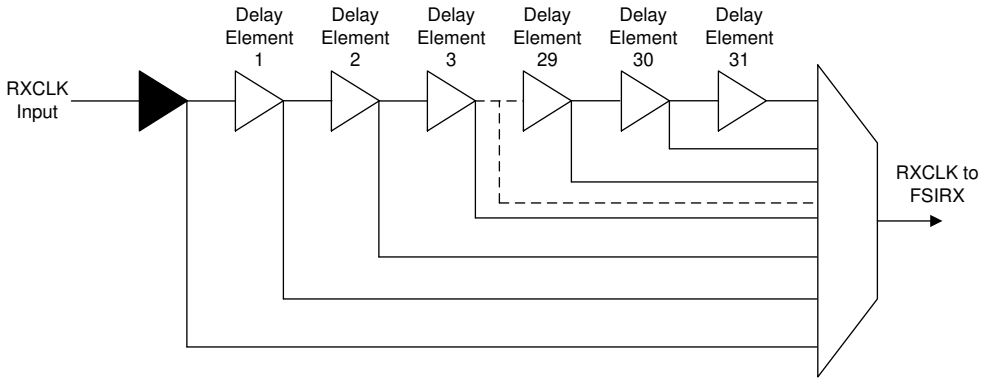


Figure 29-5. Delay Line Control Circuit

For more information on skew compensation, refer to *Fast Serial Interface (FSI) Skew Compensation*.

The FSITX module also has a delay line control circuitry that is placed before the FSITX signals (TXCLK, TXD0, and TXD1) are sent to the TDM signal selection mux (controlled by the SEL_TDM_PATH signal). The TX_DLY_LINE_CTRL register determines the length of the delay for each output line.

29.2.2.7 Buffer Management

The FSI receiver has a 16-word buffer that the data is copied to when the data has been received. This buffer is implemented as a circular buffer, not a FIFO, so some care must be taken to properly interpret buffer overrun and underrun as well as the RX_BUF_PTR_STS register. These flags and pointers work under the assumption that the software or DMA is using the buffer as a circular buffer. If the receiver state machine enters into an erroneous state, there is no way for software to cleanly handle this because there is no specified receive clock. For the receiver to detect a clean resynchronization, the state machine needs to be operational and not in the error state. The only way to recover from the error state is to reset the entire receiver module. For overrun and underrun, the receiver can no longer verify that values in the buffer are valid. As such, the best way to recover is to reset the FSI and resynchronize with the transmitter.

Due to the flexibility of the receive buffer, it is possible for software to implement a simple ping-pong buffer, or to randomly receive and read from any location of the buffer. If the buffer is used in this manner, these flags and status fields can be ignored without adversely affecting the receiver capability. Additionally, the CURR_WORD_CNT is also invalid if used in this way. The application can set the buffer pointer manually by writing the 4-bit index to RX_BUF_PTR_LOAD. This forces the receiver to start storing the received data starting at the indicated location in the buffer.

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29.2.2.8 CRC Submodule

The receive module automatically calculates the CRC on the incoming data. The received CRC value is placed into RX_CRC_INFO.RX_CRC. The CRC value calculated by hardware on the received data is placed into RX_CRC_INFO.CALC_CRC. These values are compared by hardware and RX_EVT_STS.CRC_ERROR is set if there is a mismatch. The receiver can generate an interrupt based on RX_EVT_STS.CRC_ERROR if enabled.

Since the CRC is only used in data frames, the values found in RX_CRC_INFO.RX_CRC and RX_CRC_INFO.CALC_CRC are undefined during ping and error frames.

For more information on how the CRC is calculated, refer to Section 29.2.6 .

If the transmitting module is sending a software-defined CRC value (FSITX.TX_OPER_CTRL_LO.SW_CRC = 1), the receiver module triggers a CRC error event if the received value does not match the hardware-calculated value. As this is an application-level decision, the FSIRX can safely disregard the CRC error event. Application software needs to calculate and verify the incoming CRC using the same custom algorithm used on the transmitter and act appropriately.

The CRC field can also be used as an application-specific value, not a CRC. The application can use the RX_CRC_INFO.RX_CRC as required. All CRC errors and flags can be ignored in this situation.

29.2.2.9 Using the Zero Bits of the Receiver Tag Registers

The receiver tag registers (receiver frame tag and user data (RX_FRAME_TAG_UDATA) register and receiver ping tag (RX_PING_TAG) register)) have the least-significant bit set to 0. The actual received tag is in the bit positions 4:1. The reason for this is to facilitate user software to create a table of functions that can be called depending on the tag value. A function pointer needs a 32-bit storage space and, hence, each successive pointer is offset by 2. If the first pointer is at address x, then the second pointer is at address x + 2, the third at address x + 4, and so on. By keeping the LSB to 0, the five bits of the tag register (bits 4:0) can now be directly used as an index into a table of function pointers.

29.2.2.10 Conditions in Which the Receiver Must Undergo a Soft Reset

The receiver receives data on every clock edge. While there are specific patterns that determine the a start of a frame, and denote the end of a frame, these patterns are able to occur at any point during normal operation inside of the frame. If there ever is a point at which the receiver fails to detect a successful frame, the module must be reset to make sure that subsequent frames are received properly.

When any of the following errors occur in a received frame, the receiver can be required to be reset and resynchronized with the transmitter:

- Frame type error
- End of frame error
- Ping frame watchdog timeout
- Frame watchdog timeout
- Receiver in an invalid state due to noisy clock

The receiver core status (RX_VIS_1.RX_CORE_STS) can be monitored to determine if the receiver core has entered into an error state requiring a soft reset to resume communication. Incorrect frame type and end of frame errors always cause this bit to become set. A soft reset is required in these cases. A frame watchdog timeout always requires a reset due to the fact that the receiver state machine is still expecting more information when the watchdog timed out. RX_CORE_STS can be used to determine if a noise event was the cause of the failed frame. The ping frame watchdog also does not cause RX_CORE_STS to be set. Similar to the frame watchdog, a corrupt receiver can not be the reason for the ping frame to have timed out. The transmitter can have gone offline and never sent a ping frame. Alternately, during idle time, a noise event can have occurred, thereby putting the receiver into a corrupt state. As the receiver is able to detect this during the ping frame watchdog timeout interrupt handler, this type of event is not lost and the application can act appropriately.

As the receiver is clocked by RXCLK, not MCLK, a noisy clock or data line can cause some internal design constraints to be violated, putting the receiver core logic into undefined states. Make sure that the clock and data lines satisfy the Electrical Characteristics and timing requirements of the FSI module found in the device

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data sheet. Failure to do so can cause the receiver state machine to go into an unrecoverable error state. The receiver can only be recovered by undergoing a soft reset. To determine the state of the receiver core after an unexpected frame error, the application must check the receiver core status bit.

In addition to the above errors, buffer overrun or underrun can warrant a soft reset to resynchronize with the local application software. Refer to Section 29.2.2.8 for more information on the receive buffers. The requirement of resetting the receiver due to overrun or underrun is up to the application.

After the receiver has been placed into soft reset, the application must notify the other device's transmitter to begin a new synchronization phase. The simplest way to achieve this is through a ping or error frame sent with a designated tag. If the application is not using the FSITX on the device with the detected error, some other method must be established. The other device must stop transmitting and begin a new synchronization phase.

29.2.2.11 FSI_RX Reset

The receiver module and the registers are reset by SYSRST. The receiver core is reset by SYSRST or by writing a 1 to RX_MAIN_CTRL.CORE_RST.

A module reset causes the registers to be reset to the default state. After a module reset, the receiver module must be re-initialized and the data link re-established.

29.2.3 Frame Format

The FSI module transmits and receives information in frames. Each frame contains multiple phases where different information can be found. The number of phases as well as the total length of the frame varies depending on the frame type being transmitted. Frames can be as short as 16-bits long for a ping or error frame or 288-bits long for a 16-word data frame.

In normal transmission mode, there are four preamble clock edges before the start of the frame and four post-frame clock edges (postamble). Data is transmitted on both edges of the clock (double data rate). The basic frame structure is shown in Table 29-4. Each phase of the frame (such as start-of-frame, frame type, and so on) is transmitted with the most-significant bit first. Table 29-4 describes the basic frame structure used by the FSI and adapted according to which frame type is transmitted.

Table 29-4. Basic Frame Structure

Idle State	Preamble	Start of Frame	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	End of Frame	Postamble	Idle State
	1111	1001	4 bits	8 bits	1-16 words	8 bits	4 bits	0110	1111	

The FSI also supports a FSI-SPI compatibility mode. The SPI compatible frame structure is similar to a standard FSI frame, but there are differences. Refer to Section 29.2.12 for more information on how to configure and use the FSI-SPI compatibility mode.

Note

One word of the FSI refers to 16 bits.

The terms “frame” and “packet” can be used interchangeably to describe the signaling format of the FSI.

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29.2.3.1 FSI Frame Phases

The different phases of the frame structure are described in detail.

- **Idle State:** During the idle state, the clock and data lines are driven high, the inactive state.
- **Preamble:** The preamble phase contains four clock edges (or two complete clock pulses) with the data signals held in the high state. These clock edges serve to flush the receiver logic and prepare the receiver logic for receiving a new frame. This phase is not present in SPI compatibility mode.
- **Start of Frame:** The start of frame phase contains two clock pulses with four bits, 1001, transmitted on the data lines.
- **Frame Type:** The frame type phase contains two clock pulses with the 4-bit frame type code being transmitted on the data lines. The different frame types are described in detail in Section 29.2.3.2 . The transmitter must set the TX_FRAME_CTRL.FRAME_TYPE field before transmitting a frame. The received frame type is stored in the RX_FRAME_INFO.FRAME_TYPE.
- **User Data:** The user data phase contains a fully user-configurable data field. There are no restrictions on how this field is used. This phase is only available in data frames. The user data to be transmitted is set by writing to TX_FRAME_TAG_UDATA.USER_DATA. The received user data is stored in RX_FRAME_TAG_UDATA.USER_DATA.
- **Data:** The data phase contains the data that is being transmitted. The data is pulled from the transmit buffer of the transmitter and is placed in the receive buffer of the receiver. Word 0 is transmitted first. This phase is only present in data frames. Depending on the type of frame transmitted, this can contain anywhere between 1 and 16 words depending on the frame type selected. More information on data frames is found in Section 29.2.3.2.3 .
- **CRC Byte:** The CRC byte contains the CRC of the transmitted data. The value present in this phase can be sourced from either hardware or software based on the TX_OPER_CTRL_LO.SW_CRC bit. Refer to the module-specific section of the CRC Submodule for more information on the CRC is generated or used, for the transmitter and receiver modules respectively. The CRC byte is only present in data frames.
- **Frame Tag:** The frame tag contains the 4-bit user-defined frame tag. There are no restrictions on how this field is used in an application. The transmitter supplies this tag into the TX_FRAME_TAG_UDATA.FRAME_TAG bits for data frames. Ping frames use the tag defined in TX_PING_TAG.TAG. The receiver can access the received frame tag in RX_FRAME_TAG_UDATA.FRAME_TAG.
- **End of Frame:** The end of frame contains four clock edges with four bits, 0110, transmitted on the data lines.
- **Postamble:** The postamble contains four additional clock edges with the data lines held in the high state. After the postamble, the clock and data lines are driven high (inactive state). This phase is not present in FSI-SPI compatibility mode.

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29.2.3.2 Frame Types

The FSI hardware can generate and handle many predefined frame types. The different frame types can be used by the application to signal different types of events or convey different information to the receiver. The different frame types influence which phases and data fields to include in the transmitted frames.

Table 29-5 provides a short overview of the different frame types used by the FSI. Each frame type is described in more detail in the following subsections.

Table 29-5. Frame Types and the 4-bit Codes

Frame Type	4-bit Frame Code	Description
PING	0000	Used typically for checking line integrity. A ping frame can be sent either by software or automatically by hardware.
ERROR	1111	Used typically during error conditions or any condition where one side wants to signal the other side for attention. However, the user software can use an error frame for any purpose.
DATA_1_WORD	0100	1 word data packet (16 bits of data)
DATA_2_WORD	0101	2 word data packet (32 bits of data)
DATA_4_WORD	0110	4 word data packet (64 bits of data)
DATA_6_WORD	0111	6 word data packet (96 bits of data)
DATA_N_WORD	0011	N(1-16) word data packet where software has programmed the number of the data words in a designated register. Both transmitter and receiver modules must have the same value programmed.
Reserved	0001, 0010, and 1000-1110	Reserved

29.2.3.2.1 Ping Frames

Ping frames are one of the most basic frames that can be generated by the FSI. Table 29-6 shows the structure of the ping frames.

Table 29-6. Ping Frame

Idle State	Preamble	SOF	Frame Type	Frame Tag	EOF	Postamble	Idle State
	1111	1001	0000	xxxx	0110	1111	

The ping frame type is always 0000. The frame tag is defined by the application. Separate frame tags exist for timer and software initiated ping frames. No data or CRC is transmitted in a ping frame.

The main purpose of the ping frame is to periodically send a notification to the receiver to make sure an active connection between the transmitter and receiver. The transmitter and receiver cores implement different features to allow the ping frame to operate as a line break detect feature.

On the transmitter, the ping frame is the only frame that can be set up and transmitted without any further software or DMA intervention. Ping frames can be transmitted by any (or all) of the three sources: automatic ping timer, software, or external triggers. See Section 29.2.1.3.3 for information on how the transmitter configures and sends the ping frames.

The receiver has a ping watchdog that can detect if a ping frame has not been received in a predetermined window. This allows the receiver to know if the connection between the receiver and the transmitter has been broken. See Section 29.2.2.4 for information on how the receiver handles ping frames.

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29.2.3.2.2 Error Frames

Error frames are similar to ping frames in that there are no data fields transmitted. Despite the naming of this frame as an “error frame,” the usage of it is up to the application, as no restrictions are placed on how and when this type of frame is transmitted. Table 29-7 shows the structure of an error frame.

Table 29-7. Error Frame

Idle State	Preamble	SOF	Frame Type	Frame Tag	EOF	Postamble	Idle State
	1111	1001	1111	xxxx	0110	1111	

The structure of the error frame is the same as a ping frame. No data or CRC values are transmitted. The frame type is 1111 for all error frames, and the frame tag is defined by software in the TX_FRAME_TAG_UDATA register.

The receiver can detect if an error frame has been received based on the frame type field. Because of this, the receiver can read the incoming frame tag from the RX_FRAME_TAG_UDATA register and act on up to 16 different conditions.

29.2.3.2.3 Data Frames

Data frames are the most complex frames. As the name indicates, these frames are used to transfer data. Table 29-8 shows the general structure of data frames.

Table 29-8. Data Frame

Idle State	Preamble	SOF	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	EOF	Postamble	Idle State
	1111	1001	0xxx	xxxx xxxx	1-16 words	xxxx xxxx	xxxx	0110	1111	

The frame type field reflects the 4-bit code of the frame type. A list of frame types can be seen in Table 29-5. The number of the data words transmitted is determined by the frame type chosen.

There are four fixed-length data frames supported by the frame type: 1 word, 2 words, 4 words, and 6 words.

Additionally, there is a user-defined data length frame type where the number of data words is fixed by software. Anywhere from 1 to 16 words can be transmitted in this frame type. This length must be configured in the N_WORDS field of the transmitter’s TX_FRAME_CTRL register and receiver’s RX_OPER_CTRL register.

29.2.3.3 Multi-Lane Transmission

The FSI is capable of transmitting and receiving data on two parallel data lines. When enabled, data bits are split between the data lines while the start of frame, frame type, frame tag, and end of frame fields are identical and complete on each line. The user data, data, and CRC fields are split between the data lines. Starting with the most-significant bit, the odd-numbered bits appear on D0 and even-numbered bits appear on D1.

In the following example, assume the following:

8-bit user data: u7u6u5u4u3u2u1u0

16-bit data: d15d14d13d12…d1d0

8-bit CRC: c7c6c5c4c3c2c1c0

Table 29-9. Multi-Lane Frame Format

Idle State	Preamble	SOF	Frame Type	User Data	Data Words	CRC Byte	Frame Tag	EOF	Postamble	Idle State
TXD0	1111	1001	0011	$u^7u^5u^3u^1$	$d^{15}d^{13}…d^1$	$c^7c^5c^3c^1$	xxxx	0110	1111	
TXD1	1111	1001	0011	$u^6u^4u^2u^0$	$d^{14}d^{12}…d^0$	$c^6c^4c^2c^0$	xxxx	0110	1111	

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29.2.4 Flush Sequence

Every time there is a soft reset of the receiver, the receiver requires a flush sequence from the transmitter before the receiver can receive and decode frames. The receiver core has an asynchronous reset mechanism that allows the receive module to be reset even in the absence of the receive clocks. However, due to the design, this reset is released synchronous to the receive clock (RXCLK). Thus, the receiver requires five full clock pulses to be able to come out of reset. Sending the flush pattern makes sure that these clock edges are received and any subsequent frames sent to the receiver are correctly interpreted.

The flush sequence consists of a single toggle on both of the data lines as well as five consecutive pulses on the clock line.

If the FSI receiver is receiving data from a standard SPI, a data word of 0xFFFF from the SPI has the same effect as a flush sequence.

Figure 29-6 shows a sample plot of the flush sequence.

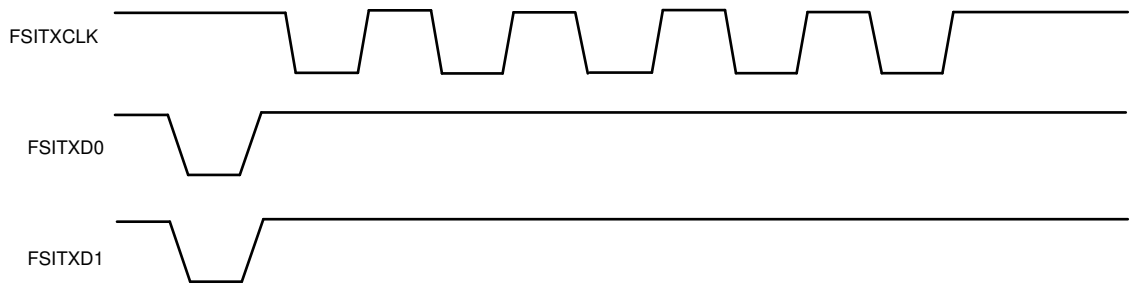


Figure 29-6. Flush Sequence Signals

29.2.5 Internal Loopback

The transmitter and receiver cores can be connected together internally to allow for development and debug. This is achieved by setting RX_MAIN_CTRL.INT_LOOPBACK to 1. Internal loopback routes the signals from the corresponding transmitter to the appropriate receiver pin. No configuration needs to be done in the transmitter. Figure 29-7 shows the signal connections with internal loopback.

In this device, there is one FSI transmitter core, and one receiver core. When using loopback mode, FSI_TX can be used in loopback mode with FSI_RX.

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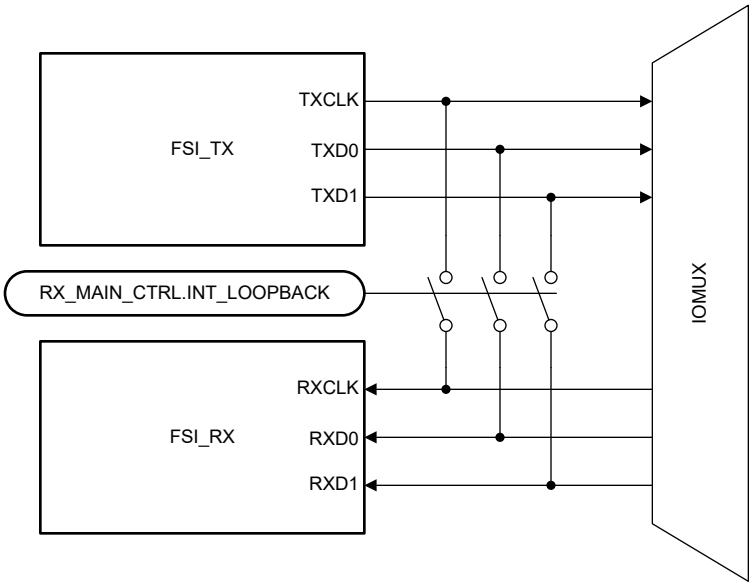


Figure 29-7. FSI with Internal Loopback

29.2.6 CRC Generation

The FSI uses CRC-8 with the polynomial 0x07 for the internal hardware CRC generation. This polynomial is also represented as x^8+x^2+x+1.

For example, for a 2-word data packet the following calculation occurs:

Data-1 = 0x4433

Data-0 = 0x2211

User Data = 0xAA

The CRC is computed with the bytes being taken in the following order (first to last):

0xAA – Byte 0, User Data

0x11 – Byte 1, Data-0, Least-significant byte

0x22 – Byte 2, Data-0, Most-significant byte

0x33 – Byte 3, Data-1, Least-significant byte

0x44 – Byte 4, Data-1, Most-significant byte

29.2.7 ECC Module

The FSI module comes with a 16-bit or 32-bit ECC computation module in both the transmitter and receiver. Use of this module is optional.

Note that the ECC is independent and unrelated to the hardware CRC computation module present in both the transmitter and receiver cores.

The following example shows a scenario in which the application requires ECC be calculated and transmitted on a 2-word data frame.

In the FSITX module:

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1. Configure the ECC module for 32-bit data by setting TX_OPER_CTRL_HI.ECC_SEL to 1.
2. Write the data to the TX_ECC_DATA register as well as the transmit buffer.
3. Read TX_ECC_VAL Register. This register contains the 8-bit ECC value calculated on the data.
4. Copy the 8-bit data from TX_ECC_VAL to TX_FRAME_TAG_UDATA.USER_DATA.
5. Set the Start Condition to begin the transmission.

The reverse process is followed on the FSIRX module. Once the data frame is received, user software can do the following:

1. Copy the data from the receive buffer to the RX_ECC_DATA register.
2. Copy the received user data that contains the transmitted ECC value from RX_FRAME_TAG_UDATA.USER_DATA to the RX_ECC_VAL register.
3. Read the RX_ECC_LOG register. This contains the result of the ECC computation using the RX_ECC_DATA and RX_ECC_VAL registers.
   a. If no ECC errors were detected, RX_ECC_LOG is 0. The correct data is available in RX_ECC_SEC_DATA.
   b. If a single bit error was detected, RX_ECC_LOG.SBE is 1. The autocorrected data is available in RX_ECC_SEC_DATA.
   c. If multiple bit errors occurred, RX_ECC_LOG.MBE is 1. The data in RX_ECC_SEC_DATA is invalid and must not be used.

Using a 2-word data frame plus using the user data for the ECC is one possible implementation for ECC detection. Another option is to use a larger data frame a allocate one of the data words to be the ECC value.

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29.2.8 Tag Matching

The FSI receiver core has the capability of generating an interrupt when the received data or ping frame's tag matches the reference tag in RX_FRAME_TAG_CMP or RX_PING_TAG_CMP, respectively.

Each tag compare register allows the user to not only select a reference tag (TAG_REF) but also set up a mask (TAG_MASK) to ignore specified bits in the reference tag. For tag matching to be enabled, the CMP_EN bit must be set. When the tag compare is enabled and a successful match occurs, the PING_TAG_MATCH, the DATA_TAG_MATCH or the ERROR_TAG_MATCH in RX_EVT_ERR_STATUS is set. The corresponding match register status can be cleared by writing to RX_EVT_ERR_CLEAR. Also, if required to set the match register status in software, the user must do so by writing to the RX_EVT_ERR_SET register.

The tag matching scheme is not a filtering scheme. Tag matching is only a notification scheme to alert the user when a specific tag is detected in a data or ping frame. Both RX_INTR_EVT_CTRL_1 and RX_INTR_EVT_CTRL_2 interrupts can be set up to generate an interrupt when a tag match event occurs.

Another feature used when tag matching is enabled is the broadcast feature. The broadcast feature can be enabled by setting the BRDCST_EN in RX_FRAME_TAG_CMP or RX_PING_TAG_CMP. When broadcast mode is enabled, the third bit of the tag is treated as a broadcast bit. If the received tag has a third bit set, then the tag is treated as a match regardless of the other tag bit comparisons. Note that a match caused by TAG_REF and TAG_MASK is also considered a match.

Note that the tag matching scheme is not a filtering scheme. For example, if tag matching is enabled and a frame is received with a non-matching tag, the frame is still saved in the buffer and the corresponding event status bits (FRAME_DONE, DATA_FRAME_RCVD) is set.

Tag matching is required in multi-peripheral TDM configurations as described in Section 29.2.10 ; however, tag matching can also be used in single-peripheral configurations as needed.

29.2.9 User Data Filtering (UDATA Matching)

The FSI receiver core has the capability of filtering data frames and only receive packets when received data UDATA (user data) matches the reference UDATA in RX_UDATA_FILTER.

The UDATA filter compare register allows you to not only select a reference UDATA (UDATA_REF) but also set up a mask (UDATA_MASK) to ignore specified bits in the reference user data. For user data filtering to be enabled, the RX_MAIN_CTRL.DATA_FILTER_EN bit must be set. When the user data filtering is enabled, only a successful match allows the packet to be received in the FSIRX circular buffer and all non-matching packets are ignored.

The user data matching scheme is a filtering scheme.

User data filtering is used in multi-peripheral configurations as described in Section 29.2.10 ; however, user data filtering can be used in single-peripheral configurations as needed.

29.2.10 TDM Configurations

The FSI module in this device supports multi-node TDM configurations, whereas a single main device can control multiple remote node devices. To use the FSI module in the multi-node TDM configuration described, the remote node device must utilize tag matching and user data filtering.

This multi-node TDM configuration is supported in the FSI module through time-division multiplexing. When TDM is enabled, each remote node device must also have tag matching enabled. Figure 29-8 shows a scheme where a single main device is communicating with multiple remote node devices. All FSI receive modules in the remote node devices are directly connected to the main device transmit module. The transmit modules of the remote node devices are chained serially such that each transmit module is connected to the next remote node device and the last remote node device output connects to the main device receive module. Each remote node device decides, based on the received frame's tag, whether to transmit the data or to enter bypass mode where the previous remote node device transmit module directly connects to the next remote node device. This is done by using the FSI transmit module TDM_IN.

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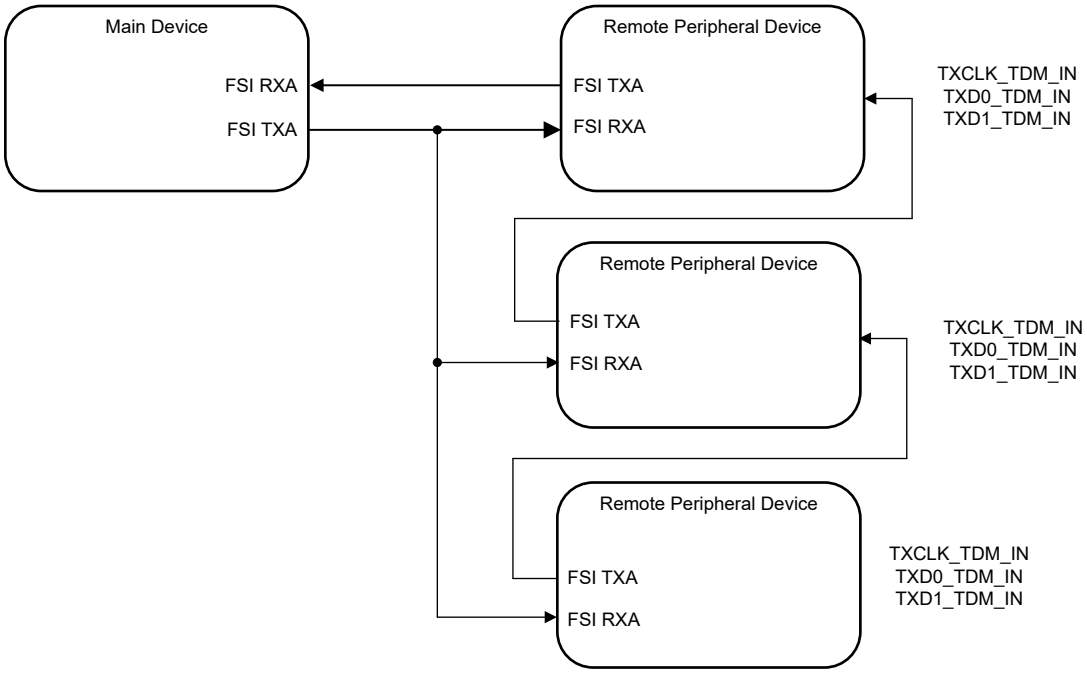


Figure 29-8. FSI Multi-Node TDM Configuration

When an FSI transmitter module is used in TDM mode, TXCLK_TDM_IN, TXD0_TDM_IN and TXD1_TDM_IN pins are used if the transmitter is required to enter bypass mode. Figure 29-9 shows how the FSI module operates when in multi-node TDM mode.

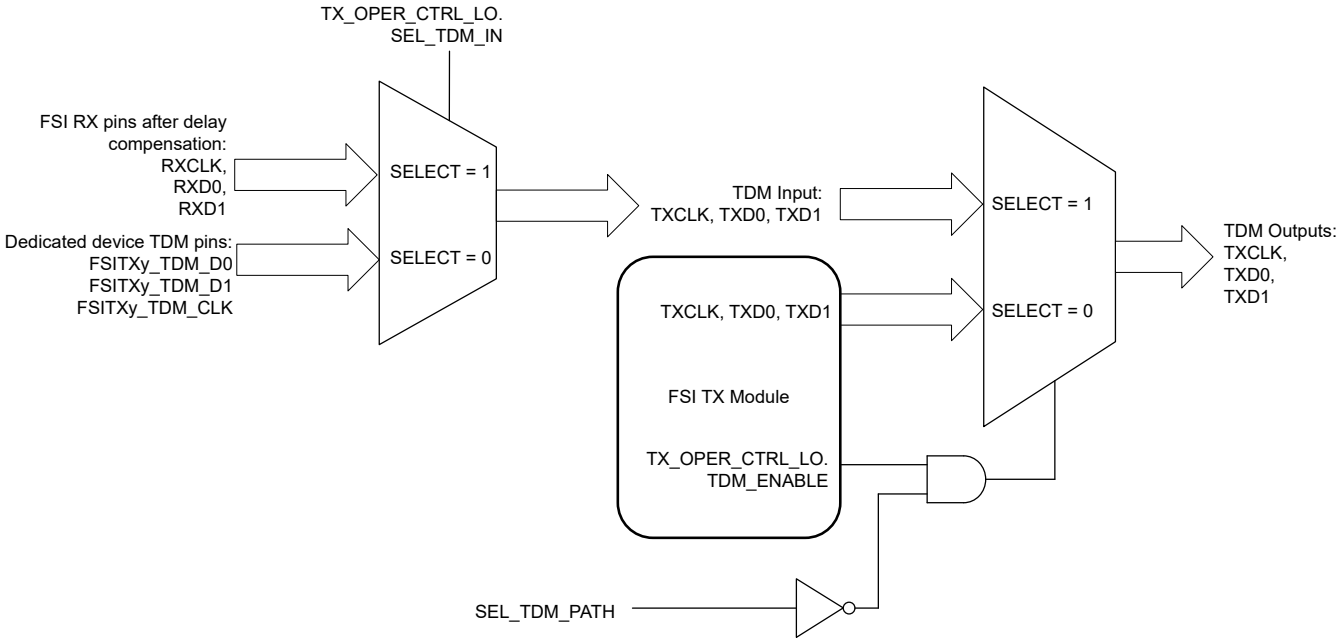


Figure 29-9. FSI Transmitter Multi-Node TDM Multiplexing

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The SEL_TDM_PATH signal is sourced from the RX_TRIG0 signal (after being stretched by the programmable width module). The RX_TRIGx signal also generates the transmit trigger for the FSI transmitter. The RX_TRIGx signal must be configured to decide when to generate the FSI transmit trigger based on the status of the data, ping, and frame tag match generated by the FSI receiver module. The FSITX module must be configured to transmit on an external trigger and the corresponding RX_TRIGx trigger input must be selected. In a broadcast scenario (FSI tag match notifies all remote node devices that a match has occurred), the RX_TRIG0 signal inside each remote node device generates a trigger and SEL_TDM_PATH signal. The main key here is that the trigger and the SEL_TDM_PATH signal must be generated at a different time interval in a non-overlapping manner. Figure 29-10 shows an example of FSI transmit triggers and the multi-node TDM SEL_TDM_PATH signals generated by theRX_TRIGx signal of the remote node devices in a broadcast scenario.

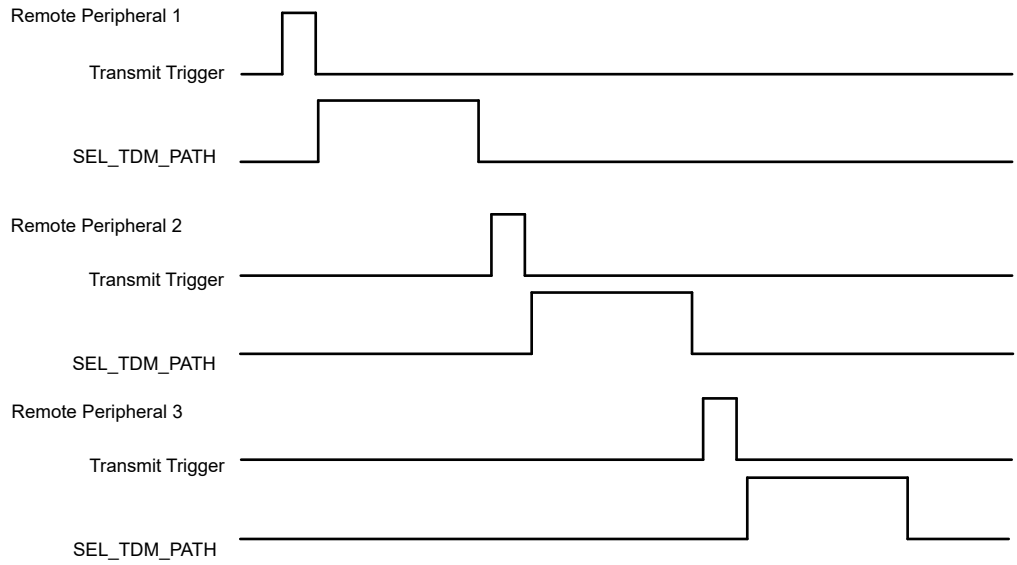


Figure 29-10. Generated Signals for FSI Multi-Node TDM Configuration

When using TDM mode, the user has the option of using the device dedicated TDM_IN pins or FSIRX pins. When the FSITX module is put in bypass mode, the TX_OPER_CTRL.SEL_TDM_IN bit determines which set of signals, FSIRX input signals or TDM_IN signals, is internally connected to the FSITX output signals.

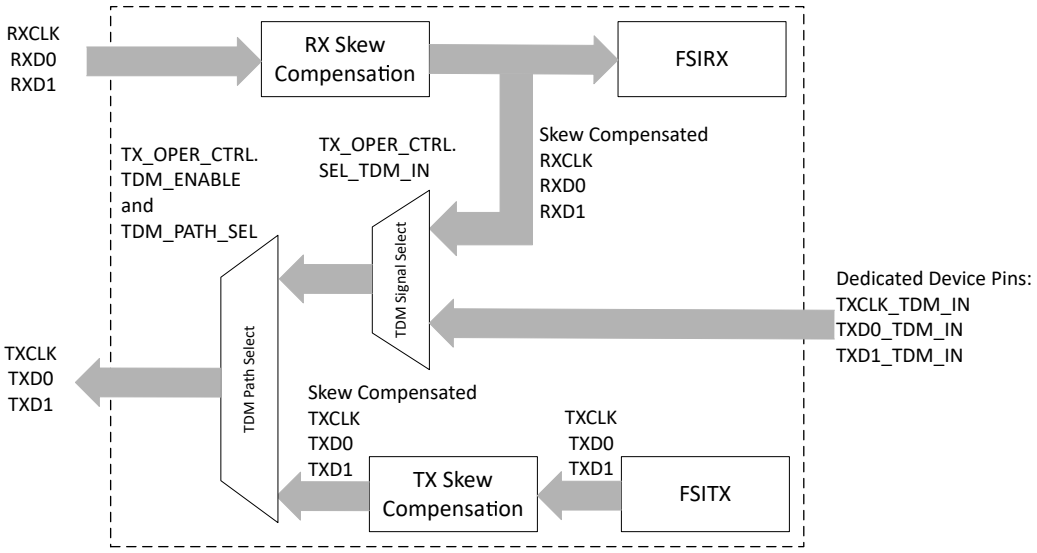


Figure 29-11. TDM Signal Selection

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29.2.11 FSI Trigger Generation

The RX_TRIGx external trigger can be used to initiate FSITX transmission. RX_TRIG0 must be used if TDM mode (multi-node configuration) is required. RX_TRIG0 must be used as the trigger source for start of transmission while the programmable stretch width RX_TRIG0 signal is used as the SEL_TDM_PATH signal (which decides whether the local FSITX is active or put in bypass mode).

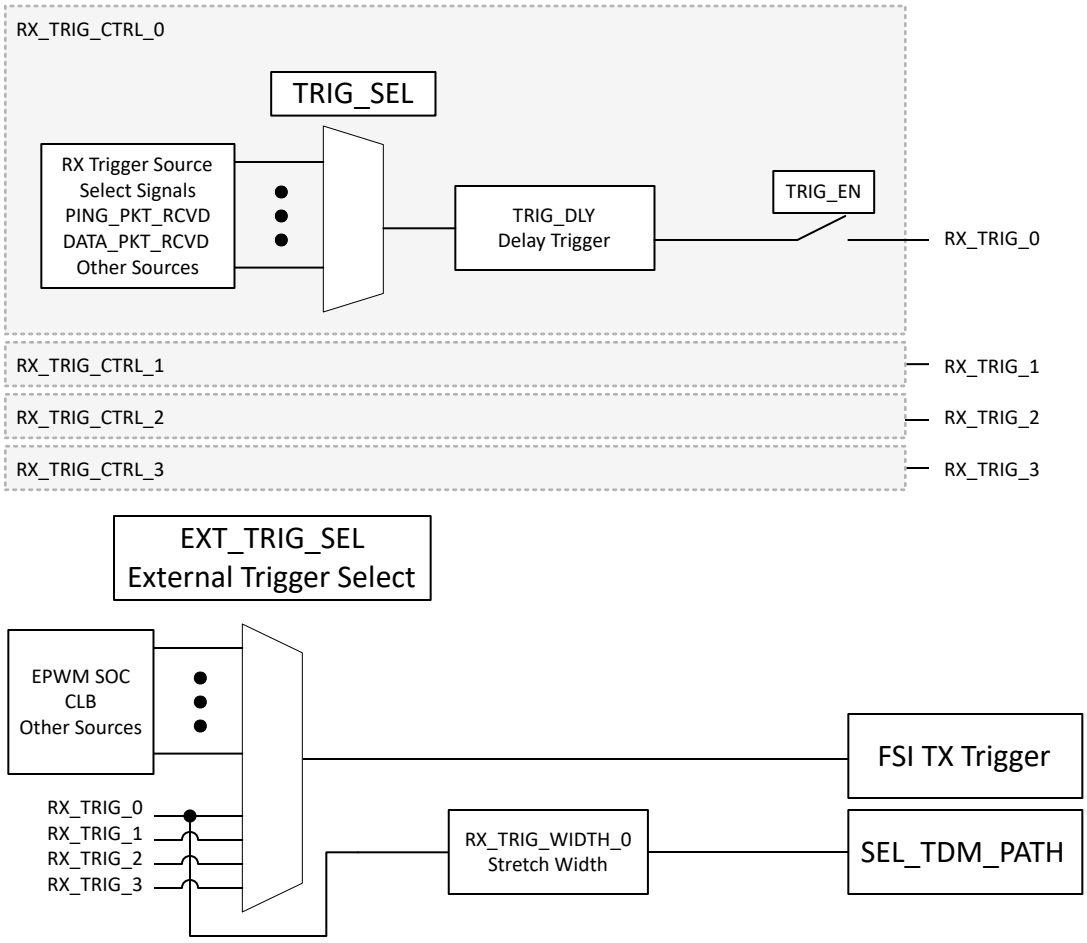


Figure 29-12. RX_TRIGx FSI Trigger

The signal source for the RX_TRIGx signal is selected through the RX_TRIG_CTRL_x.TRIG_SEL bits, as listed in Table 29-10.

Table 29-10. RX_TRIGx Trigger Select Signals

RX_TRIG_CTRLx.TRIG_SEL	Selected Signal
0	Ping Packet Received
1	Data Packet Received
2	Error Packet Received
3	Ping Frame Tag Match Occurred
4	Data Frame Tag Match Occurred
5	Error Frame Tag Match Occurred
6	Frame Done
7	Reserved

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Table 29-10. RX_TRIGx Trigger Select Signals (continued)

RX_TRIG_CTRLx.TRIG_SEL	Selected Signal
8 to 15	Reserved

The RX_TRIGx signals can optionally be delayed (this can be used in TDM scenarios) through the RX_TRIG_CTRL_x.TRIG_DLY.

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29.2.12 FSI-SPI Compatibility Mode

The FSI supports a SPI compatibility mode. While the FSI can communicate with a standard SPI module, the FSI supports a limited configuration. The features of this compatibility mode are:

- Data transmits on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 is driven like an active-low, chip-select signal. The signal is low for the duration for the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks are transmitted. All signals return to the IDLE state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

Table 29-11 lists the frame structure of the FSI-SPI compatibility mode. Each frame phase is present in this mode. If the FSI is transmitting to a standard SPI module, the SPI must decode the frame structure. Similarly, if the FSI is configured as a SPI peripheral, the standard SPI must encode the transmission to be sent.

Table 29-11. FSI-SPI Compatibility Frame Structure

Idle State	Start of Frame	Frame Type	User Data	Data Words	CRC byte(1)	Frame Tag	End of Frame	Idle State
	1001	4 bits	8 bits	1-16 words	8 bits	4 bits	0110	

(1) The CRC byte is present only in data frames.

Because of the requirement that the standard SPI module encodes the various frame data, this limits the type of modules that can be connected to the FSI in SPI mode. The paired SPI module must have enough functionality to encode and decode the frames.

If the FSI is transmitted to a standard 16-bit SPI, the data is arranged in the following manner. The example provided in Table 29-12 assumes a DATA_2_WORD frame has been sent.

Table 29-12. Contents of Data Received by a Standard SPI

SPI Data	Data Contents
SPI word 0	1001, 0100, 8-bit User Data
SPI word 1	Data word 1
SPI word 2	Data word 2
SPI word 3	8-bit CRC, 4-bit Frame Tag, 0110

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29.2.12.1 Available SPI Modes

There are a few wiring schemes available for the FSI to use when communicating with an SPI module.

29.2.12.1.1 FSITX as SPI Controller, Transmit Only

The FSITX can operate as an independent SPI controller module. In this condition, TXCLK is connected to SPICLK, TXD0 is connected to SPIPICO, and TXD1 is connected to $\overline{\text{SPIPTE}}$, the chip select.

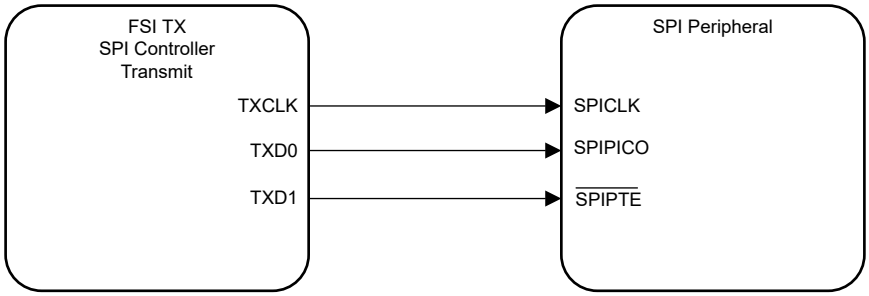


Figure 29-13. FSITX as SPI Controller, Transmit Only

When the FSI is an SPI transmitter, the application has the ability to check for frame errors, line breaks, CRC errors, and ECC checks on data. These are all encoded by hardware in every FSI frame. The SPI receiver requires some software to act upon this information.

Table 29-13. FSI as Controller Transmitter, SPI as Peripheral Receiver

Capability	Availability	Comment
Framing checks on the data frames	Yes	Can be implemented in software on the SPI receiver.
Ability to detect line breaks	Yes	Can be implemented in software on the SPI receiver but requires additional software overhead such as a timer or watchdog.
CRC check	Yes	Can be implemented in software on the SPI receiver. For devices that have , this is more efficient.
ECC on data	Yes	Can be implemented in software on the SPI receiver
Detection of abruptly terminated frames	No	
Double edge data rate	No	
Recovery from glitches on signal lines between frames	No	
Skew adjustment on signal lines	No	

29.2.12.1.1.1 Initialization

To configure the FSITX module to be an SPI controller for transmit only, proceed through the standard FSITX initialization procedure. Before releasing the FSITX from reset, set TX_OPER_CTRL_LO.SPI_MODE to 1. This enables the SPI clocking scheme and signaling structure.

29.2.12.1.1.2 Operation

The operation of the FSITX module in FSI-SPI Compatibility mode is the same as if the module is in standard FSI mode. The application can utilize the frame timer, ping frames, external frame triggers, and so on. Refer to Section 29.2.1 for more information on each of these features.

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29.2.12.1.2 FSIRX as SPI Peripheral, Receive Only

The FSIRX can operate as an independent SPI peripheral module. In this usage, RXCLK is connected to SPICLK and RXD0 is connected to SPIPICO. RXD1 is unused. There is no requirement for a chip select signal to be used when connected to the FSIRX. This is because the FSIRX responds to any incoming clock edge. If there is any noise or unwanted clock transitions, a flush sequence is required to resynchronize the FSIRX module with the controller.

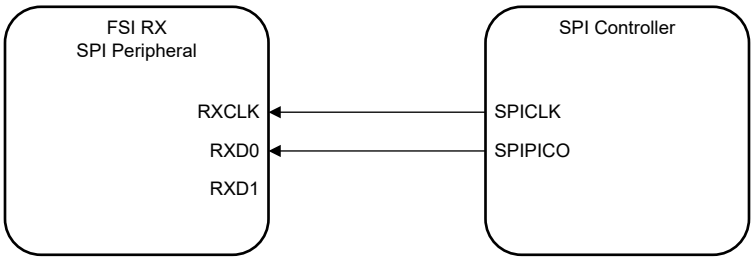


Figure 29-14. FSIRX as SPI Peripheral, Receive Only

When the FSI is an SPI receiver communicating with an SPI transmitter, the application has the ability to detect frame errors, line breaks, CRC errors, ECC checks on data, as well as abruptly terminated frames. Note that the FSI can handle all of this in hardware, but the SPI transmitter must encode the information into the data to be transmitted.

Table 29-14. SPI as Controller Transmitter, FSI as Peripheral Receiver

Capability	Availability	Comment
Framing checks on the data frames	Yes	Standard on FSI
Ability to detect line breaks	Yes	Can be implemented in software on the SPI transmitter but requires the use of a timer or watchdog in the transmitting SPI device.
CRC check	Yes	Can be implemented in software on the SPI transmitter.
ECC on data	Yes	Can be implemented in software on the SPI transmitter.
Detection of abruptly terminated frames	Yes	This is accomplished with the FSI setting up the frame watchdog counter.
Double edge data rate	No	
Recovery from glitches on signal lines between frames	Yes	Whenever glitches occur on either the clock or data lines in between transmissions, the initial flush pattern of a frame discards the effects of these glitches and causes the receiver to resynchronize when the real “start-of-frame” pattern is seen. So, the ability to reject glitches in between frames is very high.
Skew adjustment on signal lines	Yes	The FSI receiver has the ability to add delays to the incoming signal lines.

29.2.12.1.2.1 Initialization

To configure the FSIRX module to be an SPI peripheral for receiving only, proceed through the standard FSIRX initialization procedure. Before releasing the FSIRX from reset, set RX_OPER_CTRL.SPI_MODE to 1. This enables the SPI clocking scheme and signaling structure.

29.2.12.1.2.2 Operation

The operation of the FSIRX module in FSI-SPI compatibility mode is the same as if the module is in standard FSI mode. The application can utilize the Frame and Ping Watchdogs, CRC and ECC checks, and so on. Refer to Section 29.2.2 for more information on each of these features.

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29.2.12.1.3 FSITX and FSIRX Emulating a Full Duplex SPI Controller

In this configuration, the FSITX is the controller clock. The FSITX module drives TXCLK (SPICLK), TXD0 (SPIPICO), and TXD1 (SPISTE/chip select) to the SPI peripheral. The SPIPOCI signal is connected back to the RXD0 signal. RXCLK can be applied either using the internal SPI pairing feature or externally wired, depending on the application requirements. Since the FSITX and RX modules are independent, the FSIRX can also be thought of as an additional SPI peripheral. Some software logic is required for the FSI to emulate an SPI controller fully.

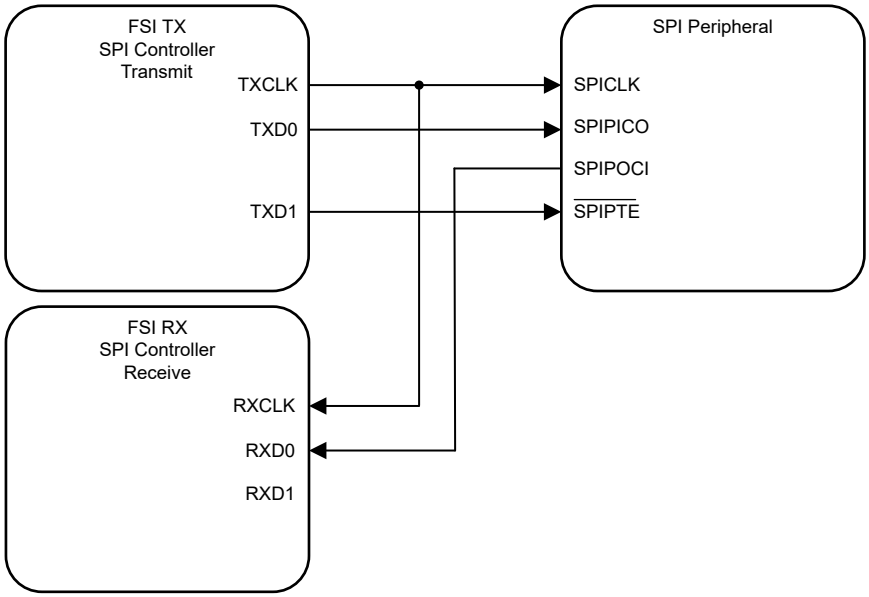


Figure 29-15. FSITX and FSIRX as SPI Controller, Full Duplex

29.2.12.1.3.1 Initialization

To configure both FSITX and RX modules for full duplex SPI controller operation, follow the initialization instructions for each module described in the preceding sections. Both FSITX and RX modules must set the respective SPI_MODE bits. This enables the SPI clocking scheme and signaling structures.

If internal clock loopback is desired, the FSIRX module must also set RX_MAIN_CTRL.SPI_PAIRING to 1. This internally connects TXCLK to RXCLK. If using internal clock loopback, the GPIO used for RXCLK can be reallocated to other application requirements.

If the application requires an external clock loopback, make sure that TXCLK is connected to RXCLK. This is required if the SPI peripheral is across an isolation barrier and there is latency between TXCLK being launched and SPIPOCI data being received on RXD0.

29.2.12.1.3.2 Operation

In this mode of operation, some higher level software must be written to emulate a full SPI controller module. There is no path for the transmit module to determine what the receive module received. Both the TX and RX modules are still able to utilize the various other features available, such as the ping frame timer, ping frame and frame watchdogs, CRC and ECC error checkers, and so on. The procedure for configuring these features is described elsewhere in this document.

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29.3 FSI Programing Guide

This section describes various operational sequences and features for the FSI.

29.3.1 Establishing the Communication Link

Once the transmitter and receiver modules have been configured, some synchronization must occur before the modules exchange data. Since the receiver accepts data on any clock transition, the receiver core logic must be flushed to properly interpret the start of a new, valid frame. This is especially true when the FSI modules reside on separate devices and are possibly isolated.

The following example provides a suggested approach for establishing a clean communication link on two separate devices that power up in an arbitrary order. Note that this is only a sample synchronization. Depending on application requirements, a different approach can be followed. The single, most important aspect of synchronization is to make sure that the receiver is properly flushed and ready to receive a complete frame without error. How to achieve this is up to the application.

Figure 29-16 shows the connection of the devices in this example. While there is no true concept of a main device or a remote device node in the FSI protocol, the example uses this nomenclature as a simple way to describe the data flow.

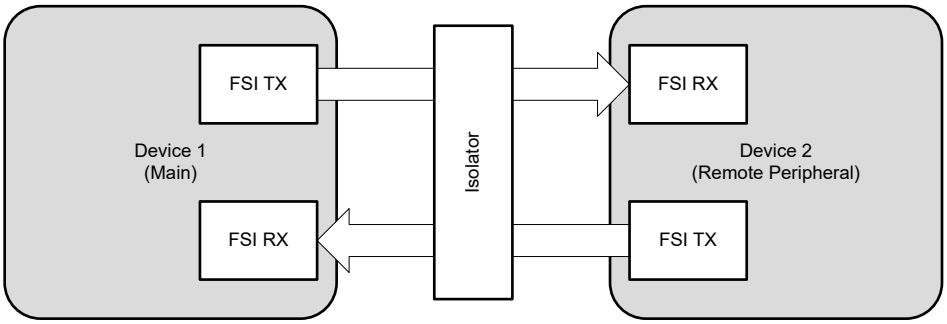


Figure 29-16. Point to Point Connection

Device 1 is the main node; it is the driver of the initialization sequence. Device 2 is the remote node; it responds to the main device commands. In this example, as well as in a real world use-case, neither the main device nor the remote device knows precisely when the other is ready to receive communication.

Sample sequences for both the main device and remote device are provided in the following subsections.

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29.3.1.1 Establishing the Communication Link from the Main Device

The following sequence is an example of how the main device node establishes the communication link with the remote device without external signals outside of the standard communication link.

1. Assert the core reset to both the FSITX and FSIRX modules, and then deassert the resets.
2. Configure the transmitter and receiver for desired operation.
3. Set up the receiver interrupts to detect an incoming transmission.
4. Begin the ping loop:
   - Send the flush sequence.
   - Send a ping frame with the frame tag 0000.
   - Wait for some time. (determined by application)
   - If the FSIRX has received a valid ping frame, continue; else, iterate the loop again.
   - If the received ping frame tag was 0001, continue; else, iterate the loop again.
5. Send a ping frame with the frame tag 0001.

At this point, both the main transmit and receive channels have successfully received a frame from the remote counterparts. The link has been established and standard application communication can begin.

29.3.1.2 Establishing the Communication Link from the Remote Device

The following sequence is an example of how the remote device node establishes the communication link with the main device without external signals outside of the standard communication link.

1. Apply the core reset to both the FSITX and FSIRX modules, and then release the reset.
2. Configure the transmitter and receiver for desired operation.
3. Set up the receiver interrupts to detect an incoming transmission.
4. Wait for a receiver interrupt.
5. If the FSIRX has received a valid ping frame, continue; else, return to step 4.
6. If the received frame tag was 0000, continue; else, discard the transmission and return to step 4.
7. Send the flush sequence.
8. Send a ping frame with the frame tag 0001.
9. Wait for a receiver interrupt.
10. If the FSIRX has received a valid ping frame, continue; else, return to step 4.
11. If the received ping frame tag was 0001, continue; else, if the received frame tag was 0000, return to step 9. This can happen if a second ping frame was already in transit before receiving the remote device response in step 8.

At this point, both the transmit and receive modules have successfully received ping frames from the main counterparts. The link has been established and regular communication can now proceed. The application can configure periodic ping frames from the transmitter, initialize the receiver ping and frame watchdogs, and begin the communication required by the application.

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29.3.2 Register Protection

Both the FSITX and FSIRX modules contain control registers that have embedded write protection. This is accomplished through register keys and a main register lock. These protections make sure that no spurious writes or unintentional modifications to these registers are accepted.

Register Key Protection

Some bits in the FSI registers are protected by a key. To write to these bits, the key must be written at the same time. For example, to put the transmitter core into reset, TX_MAIN_CTRL.CORE_RST must be set. To do this, write 0xA501 to TX_MAIN_CTRL, where 0xA500 is the KEY value, and 0x0001 is the CORE_RST value. Refer to the *Registers* section for more information on which registers have write keys added.

Control Register Lock Protection

There also exists a main lock to prevent any modifications to the control registers. There is an independent lock for each FSI module. For the list of registers that are protected by this control register lock, refer to the *Registers* section. The control register lock prevents any writes to the control registers until the lock is released. To set the control register lock, write 0xA501 to RX_LOCK_CTRL and TX_LOCK_CTRL for the receiver and transmitter, respectively.

The control register lock cannot be disabled by the application until a SYSRST has been asserted. This can occur at the device level, or by writing to the appropriate peripheral soft reset register (DEV_CFG_REGS.SOFTPRESx) for the FSI module.

29.3.3 Emulation Mode

There is no specific emulation mode or configuration supported. The FSI cores are always in free running mode. CPU halts do not have any effect on the operation of the FSI. Reads of registers and data buffers by the debugger do not affect any flags or status of the data buffers.

If you want to stop the operation of either FSI module when the debugger halts, the following steps are required:

1. Set the debugger to real-time emulation mode.
2. Mark the FSI interrupt group as a time-critical interrupt. That is, enable the corresponding bit in the DBGIER register.
3. The ISR can check the DSTAT register and to determine if the ISR was called when the debugger was halted.
4. FSI operations can be disabled and the ISR can branch to a debug-specific halt location.

29.4 FSI Interrupts & Triggers

29.4.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 29-15. CPU Interrupts Triggered by FSI

NVIC Interrupt Name	Peripheral Instance Name	Register Group	FSI Interrupt Configuration Registers	Description
FSITX_INT1	FSI_TX	N/A	TX_INT_CTRL, EVT_STS, EVT_FRC, EVT_CLR	FSI_TX INT1 interrupt. Multiple OR'd, configurable source conditions.
FSITX_INT2	FSI_TX	N/A	TX_INT_CTRL, EVT_STS, EVT_FRC, EVT_CLR	FSI_TX INT2 interrupt. Multiple OR'd, configurable source conditions.

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Table 29-15. CPU Interrupts Triggered by FSI (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	FSI Interrupt Configuration Registers	Description
FSIRX_INT1	FSI_RX	N/A	RX_INT1_CTRL, RX_EVT_STS, RX_EVT_CLR, RX_EVT_FRC	FSI_RX INT1 interrupt. Multiple OR'd, configurable source conditions.
FSIRX_INT2	FSI_RX	N/A	RX_INT2_CTRL, RX_EVT_STS, RX_EVT_CLR, RX_EVT_FRC	FSI_RX INT2 interrupt. Multiple OR'd, configurable source conditions.

29.4.1.1 FSI Interrupts

Each FSI module contains multiple interrupt sources that can be assigned to two different interrupt vectors: INT1 and INT2. Each interrupt source has an associated status flag, force, and clear bits in the EVT_STS, EVT_FRC, and the EVT_CLR registers, respectively.

Each interrupt can be assigned to either interrupt vector, INT1 and INT2, to allow for two priority levels. Alternately, the interrupt source can be prevented from generating any interrupt, though the status flag can still be set and monitored by software. The transmitter events are assigned to either interrupt vector in the TX_INT_CTRL register. The receiver events are assigned an interrupt vector using RX_INT1_CTRL and RX_INT2_CTRL registers. If an interrupt is not required, make sure the bit is not set in the respective INT_CTRL register.

29.4.1.1.1 Transmitter Interrupts

The transmitter can generate the following interrupts:

- **Frame Done (FRAME_DONE):** This event indicates that FSI has completed transmitting a frame.
- **Buffer Underrun (BUF_UNDERRUN):** This event indicates that the transmit buffer has experienced underrun. Buffer underrun occurs when the transmitter tries to read data from a location which has not yet be written to by the CPU, or DMA.
- **Buffer Overrun (BUF_OVERRUN):** The buffer overrun interrupt is generated when the buffer has experienced overrun. Buffer overrun can occur if a piece of data is overwritten before the data has been transmitted.
- **Ping Frame Triggered (PING_TRIGGERED):** The ping frame triggered interrupt is generated when the ping frame has been triggered. This bit is set when the ping counter has timed out or an external ping trigger event has occurred.

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29.4.1.1.2 Receiver Interrupts

The receiver core is capable of generating interrupts from many different events:

- **Ping Watchdog Timeout (PING_WD_TO):** This event indicates that the ping watchdog timer has timed out. The receiver has not received a valid frame within the time period specified in the RX_PING_WD_REF register.
- **Frame Watchdog Timeout (FRAME_WD_TO):** This event indicates that the frame watchdog timer has timed out. The conditions of this timeout are set using the RX_FRAME_WD_CTRL register. As soon as the start of frame phase is detected, the frame watchdog counter starts counting from 0. The end of frame phase must complete by the time the watchdog counter reaches the reference value. If this does not happen, the watchdog times out and this event is generated. If this event occurs, the receiver must undergo a soft reset and subsequent resynchronization to resume proper operation.
- **CRC Error (CRC_ERR):** This error indicates that a CRC error has occurred. A CRC error is generated when the received CRC and the computed CRC do not match.
- **Frame Type Error (TYPE_ERR):** This error indicates that an invalid frame type has been received. If this error occurs, the receiver must undergo a soft reset and subsequent resynchronization to resume proper operation.
- **End-of-Frame Error (EOF_ERR):** This error indicates that an invalid end-of-frame bit pattern has been received. If this error occurs, the receiver must undergo a soft reset and subsequent resynchronization to resume proper operation.
- **Receive Buffer Overrun (BUF_OVERRUN):** This event indicates that an overrun condition has occurred in the receive buffer.
- **Receive Buffer Underrun (BUF_UNDERRUN):** This event indicates that an underrun condition has occurred in the receive buffer. This condition occurs when software reads an empty buffer.
- **Frame Done (FRAME_DONE):** This event indicates that a valid frame has been received without error.
- **Error Frame Received (ERR_FRAME):** This event indicates that an error frame has been received.
- **Ping Frame Received (PING_FRAME):** This event indicates that a ping frame has been received.
- **Frame Overrun (FRAME_OVERRUN):** This event indicates that a new frame has been received while the FRAME_DONE flag was still set.
- **Data Frame Received (DATA_FRAME):** This event indicates that a data frame has been received.
- **Ping Tag Matched (PING_TAG_MATCH):** This event indicates that a ping frame with a matching tag has been received.
- **Data Tag Matched (DATA_TAG_MATCH):** This event indicates that a data frame with a matching tag has been received.
- **Error Tag Matched (ERROR_TAG_MATCH):** This event indicates that an error frame with a matching tag has been received.

29.4.1.1.3 Configuring Interrupts

To configure interrupts on the FSI, the application must select the interrupt vector for each desired event using the TX_INT_CTRL register for the transmitter, and RX_INT1_CTRL and RX_INT2_CTRL registers for the receiver. There is no module-level interrupt enable bit to configure.

Note

If an event is registered for both interrupt vectors, both interrupts fire. There are no hardware checks for overlapping interrupt vector assignments.

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29.4.1.1.4 Handling Interrupts

Inside the interrupt service routine (ISR), the user must clear the event flag using the EVT_CLR register and then acknowledge the CPU interrupt.

If the one event occurs multiple times before the corresponding bit is cleared by software, no new interrupt is generated.

If multiple events occur simultaneously, or very close in time, it is possible to handle multiple conditions within a single interrupt. Each flag is independently set by hardware and must be cleared by application software. If multiple different events occur, the ISR can handle each in whatever order is deemed necessary by the application. It is not advisable to clear the full interrupt status register in every ISR. This can cause the application to miss events that can be detrimental to the application. A sample sequence for handling interrupts on the receiver follows; the transmitter routine is similar.

- On receiving an interrupt, copy the current state of the receive event and error status flag register (RX_EVT_STS) into a local snapshot variable.
- Read all of the bits from the snapshot to determine the events that require action.
- Perform the necessary actions for each of the events seen in the snapshot.
- Write to the receive event and error clear register (RX_EVT_CLR) with the snapshot to clear only those interrupts that were set at the beginning of the ISR.
- Repeat this sequence for every generated ISR.

There is a chance that another event occurred during the just-handled ISR since only the snapshot of events was handled and then cleared; an event flag can still be set at the end of the ISR. As soon as the ISR completes, a new interrupt is generated and this flag is still set and can be handled accordingly.

Software accesses tied to multiple events and handled within the same ISR can cause race conditions that cause the software to not function as desired. For example, it is recommended to use different interrupt lines if the user wants to enable events for both ping and data frames. If both events are handled within the same interrupt line, the software can only respond to one of the events if both events occur close in time.

29.4.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 29-16. DMA Triggers from the FSI

Trigger Name	Peripheral Instance Name	Register Group	FSI DMA Configuration Registers	Description
FSITX_DMA	FSI_TX	N/A	TX_DMA_CTRL, TX_EVT_STS.FRAME_DONE, TX_EVT_CLR.FRAME_DONE, TX_EVT_FRC.FRAME_DONE	FSI_TX DMA trigger. Single, configurable source condition.
FSIRX_DMA	FSI_RX	N/A	RX_DMA_CTRL, RX_EVT_STS.FRAME_DONE, RX_EVT_CLR.FRAME_DONE, RX_EVT_FRC.FRAME_DONE	FSI_RX DMA trigger. Single, configurable source condition.
FSIRX_DATA_TAG_MATCH	FSI_RX	N/A	RX_EVT_STS.DATA_TAG_MATCH, RX_EVT_CLR.DATA_TAG_MATCH, RX_EVT_FRC.DATA_TAG_MATCH	FSI_RX Tag Match DMA trigger. Single, configurable source condition.
FSIRX_PING_TAG_MATCH	FSI_RX	N/A	RX_EVT_STS.PING_TAG_MATCH, RX_EVT_CLR.PING_TAG_MATCH, RX_EVT_FRC.PING_TAG_MATCH	FSI_RX Ping Tag Match DMA trigger. Single, configurable source condition.

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29.4.2.1 DMA Interface

Both the transmitter and receiver are capable of using the DMA for automatic data transfers. The DMA trigger is independent from the interrupt signals. DMA events are only triggered on the completion of a data frame.

The transmitter DMA trigger is enabled by setting TX_DMA_CTRL.DMA_EVT_EN to 1. The transmitter must also set TX_OPER_CTRL_LO.START_MODE to 0x2 to allow either a write to the TX_FRAME_CTRL.START bit or to the TX_FRAME_TAG_UDATA register to start the transmission.

The receiver DMA trigger is enabled by setting RX_DMA_CTRL.DMA_EVT_EN to 1.

Refer to Section 29.2.1 and Section 29.2.2 for more DMA information specific to each FSI Module.

29.4.2.1.1 Transmitting Frames with DMA

The FSI transmitter can send data that is continuously applied with the DMA. A DMA trigger is generated every time a data frame transmission is completed. This is concurrent with the FRAME_DONE signal that sets the TX_EVT_STS.FRAME_DONE flag.

To transmit continuous data with the DMA, some configurations need to be made on the transmitter:

First, set TX_DMA_CTRL.DMA_EVT_EN to 1. This allows the DMA trigger to propagate to the DMA module. Next, TX_OPER_CTRL_LO.START_MODE must be set to 0x2. The transmitter is now able to start a transmission using a software write to TX_FRAME_CTRL.START or TX_FRAME_TAG_UDATA..

The DMA must also be configured properly for the FSI to send the data. One way of using the DMA to continuously feed the transmit buffer is:

- Set up two DMA channels to be triggered by the same FSI transmitter and DMA trigger.
- Configure one channel to fill the transmit buffer.
- Configure the other channel to set the frame tag and user data fields
- Since the FSI transmit buffer is a 16-word circular buffer, make sure the DMA channel servicing the data buffer wraps the after 16 words are copied.

Note

Because the frame tag and user data must be written in to initiate the transmission of the frame, use two consecutive DMA channels. This makes sure that the DMA channels are always executed in sequence. The DMA channel servicing the data buffer must be the lower numbered channel and the tag/user data channel must be the next. For example, configure DMA channel 3 to service the data buffer, and configure DMA channel 4 to service the tag and user data.

29.4.2.1.2 Receiving Frames with DMA

The FSI receiver can continuously receive data and move the data from the receiver buffer with the DMA. A DMA trigger is generated every time a data frame has been received. This is concurrent with the FRAME_DONE signal that sets the RX_EVT_STS.FRAME_DONE flag. To receive continuous data with the DMA, some configurations need to be made on the receiver.

First, set RX_DMA_CTRL.DMA_EVT_EN to 1. This allows the DMA trigger to propagate to the DMA module. The receiver is now able to trigger a DMA event upon the reception of a data frame.

The DMA must also be configured properly for the FSI to receive the data. One way for using the receiver to continuously feed the DMA is:

- Set up two DMA channels to be triggered by the FSI Receiver DMA trigger.
- Configure one DMA channel to copy data from the receive buffer to a larger data buffer.
- Configure the next DMA channel to copy the received frame tag and user data to another data buffer.
- Since the FSI receive buffer is a 16-word circular buffer, make sure the DMA channel servicing the data buffer wraps after 16 words are copied.

Unlike the transmitter, there is no requirement to have the DMA channel that is handling the data buffer execute before the DMA channel handling the received tag and user data.

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29.5 FSI Registers

This Section describes the FSI Registers.

29.5.1 FSI Base Address Table

Table 29-17. FSI Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
FsiTxRegs	FSI_TX_REGS	FSI_TX	0x4050_0000
FsiRxRegs	FSI_RX_REGS	FSI_RX	0x4050_1000

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29.5.2 FSI_TX_REGS Registers

Table 29-18 lists the memory-mapped registers for the FSI_TX_REGS registers. All register offset addresses not listed in Table 29-18 should be considered as reserved locations and the register contents should not be modified.

Table 29-18. FSI_TX_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	TX_MAIN_CTRL	Transmit main control register		Go
4h	TX_CLK_CTRL	Transmit clock control register		Go
8h	TX_OPER_CTRL_LO	Transmit operation control register low		Go
Ah	TX_OPER_CTRL_HI	Transmit operation control register high		Go
Ch	TX_FRAME_CTRL	Transmit frame control register		Go
Eh	TX_FRAME_TAG_UDATA	Transmit frame tag and user data register		Go
10h	TX_BUF_PTR_LOAD	Transmit buffer pointer control load register		Go
12h	TX_BUF_PTR_STS	Transmit buffer pointer control status register		Go
14h	TX_PING_CTRL	Transmit ping control register		Go
16h	TX_PING_TAG	Transmit ping tag register		Go
18h	TX_PING_TO_REF	Transmit ping timeout counter reference		Go
1Ch	TX_PING_TO_CNT	Transmit ping timeout current count		Go
20h	TX_INT_CTRL	Transmit interrupt event control register		Go
22h	TX_DMA_CTRL	Transmit DMA event control register		Go
24h	TX_LOCK_CTRL	Transmit lock control register		Go
28h	TX_EVT_STS	Transmit event and error status flag register		Go
2Ch	TX_EVT_CLR	Transmit event and error clear register		Go
2Eh	TX_EVT_FRC	Transmit event and error flag force register		Go
30h	TX_USER_CRC	Transmit user-defined CRC register		Go
40h	TX_ECC_DATA	Transmit ECC data register		Go
44h	TX_ECC_VAL	Transmit ECC value register		Go
48h	TX_DLYLINE_CTRL	Transmit delay Line control register		Go
80h + formula	TX_BUF_BASE_y	Base address for transmit buffer		Go

Complex bit access types are encoded to fit into small table cells. Table 29-19 shows the codes that are used for access types in this section.

Table 29-19. FSI_TX_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

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Table 29-19. FSI_TX_REGS Access Type Codes (continued)

Access Type	Code	Description
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 TX_MAIN_CTRL Register (Offset = 0h) [Reset = 0000h]

TX_MAIN_CTRL is shown in Figure 29-17 and described in Table 29-20.

Return to the Summary Table.

Transmit main control register

Figure 29-17. TX_MAIN_CTRL Register

15	14	13	12	11	10	9	8
KEY							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						FLUSH	CORE_RST
R-0h						R/W-0h	R/W-0h

Table 29-21. TX_MAIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	W	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset type: SYSRSn
7-2	RESERVED	R	0h	Reserved
1	FLUSH	R/W	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h (R/W) = Clear this bit. 1h (R/W) = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0. Reset type: SYSRSn
0	CORE_RST	R/W	0h	Transmitter Main Core Reset bit This bit controls the transmitter main core reset. In order to send any frame, this bit must be cleared. 0h (R/W) = Transmitter core is not in reset and can transmit frames. 1h (R/W) = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn

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2 TX_CLK_CTRL Register (Offset = 4h) [Reset = 0000h]

TX_CLK_CTRL is shown in Figure 29-18 and described in Table 29-21.

Return to the Summary Table.

Transmit clock control register

Figure 29-18. TX_CLK_CTRL Register

15	14	13	12	11	10	9	8
RESERVED						PRESCALE_VAL	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
PRESCALE_VAL						CLK_EN	CLK_RST
R/W-0h						R/W-0h	R/W-0h

Table 29-23. TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-2	PRESCALE_VAL	R/W	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h (R/W) = Reserved 1h (R/W) = Input clock /1 2h (R/W) = Input clock /2 3h (R/W) = Input clock /3 4h (R/W) = Input clock /4 ... FFh (R/W) = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN Reset type: SYSRSn
1	CLK_EN	R/W	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h (R/W) = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h (R/W) = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled. Reset type: SYSRSn
0	CLK_RST	R/W	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h (R/W) = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h (R/W) = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit. Reset type: SYSRSn

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3 TX_OPER_CTRL_LO Register (Offset = 8h) [Reset = 0000h]

TX_OPER_CTRL_LO is shown in Figure 29-19 and described in Table 29-22.

Return to the Summary Table.

Transmit operation control register low

Figure 29-19. TX_OPER_CTRL_LO Register

15	14	13	12	11	10	9	8
RESERVED					SEL_TDM_IN	TDM_ENABLE	SEL_PLLCLK
R-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PING_TO_MODE	SW_CRC	START_MODE			SPI_MODE	DATA_WIDTH	
R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h	

Table 29-25. TX_OPER_CTRL_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	SEL_TDM_IN	R/W	0h	Input TDM port Select bit This bit selects the input port for the transmitter core between the TDM input pins or the RX module. When this bit is '0', the inputs selected for TDM are from the TDM input pins. When this bit is '1', then inputs selected for TDM are from the RX module. Reset type: SYSRSn
9	TDM_ENABLE	R/W	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-remote TDM operation. 0h (R/W) Transmit TDM Mode is not enabled. 1h (R/W) Transmit TDM Mode is enabled. Reset type: SYSRSn
8	SEL_PLLCLK	R/W	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h (R/W) = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h (R/W) = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler. Reset type: SYSRSn
7	PING_TO_MODE	R/W	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h (R/W) = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h (R/W) = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout Reset type: SYSRSn
6	SW_CRC	R/W	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h (R/W) = The transmitted CRC value is computed by hardware. 1h (R/W) = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register. Reset type: SYSRSn

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Table 29-25. TX_OPER_CTRL_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	START_MODE	R/W	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h (R/W) = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h (R/W) = The configured external trigger will initiate a new transmission. 2h (R/W) = Either writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use. Reset type: SYSRSn
2	SPI_MODE	R/W	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode. Reset type: SYSRSn
1-0	DATA_WIDTH	R/W	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h (R/W) = Data will be transmitted on one data line (TXD0). 1h (R/W) = Data will be transmitted on two data lines (TXD0 and TXD1). The format of the data is described in the preceeding chapter. 2h, 3h (R/W) = Reserved Reset type: SYSRSn

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4 TX_OPER_CTRL_HI Register (Offset = Ah) [Reset = 0000h]

TX_OPER_CTRL_HI is shown in Figure 29-20 and described in Table 29-23.

Return to the Summary Table.

Transmit operation control register high

Figure 29-20. TX_OPER_CTRL_HI Register

15	14	13	12	11	10	9	8
RESERVED		EXT_TRIG_SEL					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
EXT_TRIG_SEL	ECC_SEL	FORCE_ERR	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				

Table 29-27. TX_OPER_CTRL_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-7	EXT_TRIG_SEL	R/W	0h	External Trigger Select bit These bits define which of the 128 external inputs will be used as the source for the external input trigger. 00h (R/W) = Trigger 1 is the source. 01h (R/W) = Trigger 2 is the source. 02h (R/W) = Trigger 3 is the source. ... 7Fh (R/W) = Trigger 128 is the source. Reset type: SYSRSn
6	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used. Reset type: SYSRSn
5	FORCE_ERR	R/W	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode (FSI Transmit). 0h (R/W) = The CRC will not be forced to 0. 1h (R/W) = The CRC will be forced to 0 in a buffer overrun or underrun condition. Reset type: SYSRSn
4-0	RESERVED	R	0h	Reserved

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5 TX_FRAME_CTRL Register (Offset = Ch) [Reset = 0000h]

TX_FRAME_CTRL is shown in Figure 29-21 and described in Table 29-24.

Return to the Summary Table.

Transmit frame control register

Figure 29-21. TX_FRAME_CTRL Register

15	14	13	12	11	10	9	8
START	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
N_WORDS				FRAME_TYPE			
R/W-0h				R/W-0h			

Table 29-29. TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	R/W	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Start the next transmission. This bit will be cleared by hardware. Reset type: SYSRSn
14-8	RESERVED	R	0h	Reserved
7-4	N_WORDS	R/W	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data). Reset type: SYSRSn
3-0	FRAME_TYPE	R/W	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b (R/W) = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b (R/W) = DATA_1_WORD Frame. One word data frame (16-bit data). 0101b (R/W) = DATA_2_WORD Frame. Two word data frame (32-bit data). 0110b (R/W) = DATA_4_WORD Frame. Four word data frame (64-bit data). 0111b (R/W) = DATA_6_WORD Frame. Six word data frame (96-bit data). 0011b (R/W) = DATA_N_WORD Frame. The N_WORDS field will determine the number of words (1 to 16) to be sent. Both the transmitter and receiver must have the same value programmed. 1111b (R/W) = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset type: SYSRSn

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6 TX_FRAME_TAG_UDATA Register (Offset = Eh) [Reset = 0000h]

TX_FRAME_TAG_UDATA is shown in Figure 29-22 and described in Table 29-25.

Return to the Summary Table.

Transmit frame tag and user data register

Figure 29-22. TX_FRAME_TAG_UDATA Register

15	14	13	12	11	10	9	8
USER_DATA							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				FRAME_TAG			
R-0h				R/W-0h			

Table 29-31. TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	USER_DATA	R/W	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior. Reset type: SYSRSn
7-4	RESERVED	R	0h	Reserved
3-0	FRAME_TAG	R/W	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead. Reset type: SYSRSn

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7 TX_BUF_PTR_LOAD Register (Offset = 10h) [Reset = 0000h]

TX_BUF_PTR_LOAD is shown in Figure 29-23 and described in Table 29-26.

Return to the Summary Table.

Transmit buffer pointer control load register

Figure 29-23. TX_BUF_PTR_LOAD Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				BUF_PTR_LOAD			
R-0h				R/W-0h			

Table 29-33. TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior. Reset type: SYSRSn

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8 TX_BUF_PTR_STS Register (Offset = 12h) [Reset = 0000h]

TX_BUF_PTR_STS is shown in Figure 29-24 and described in Table 29-27.

Return to the Summary Table.

Transmit buffer pointer control status register

Figure 29-24. TX_BUF_PTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			CURR_WORD_CNT				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED				CURR_BUF_PTR			
R-0h				R-0h			

Table 29-35. TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	CURR_WORD_CNT	R	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition. Reset type: SYSRSn
7-4	RESERVED	R	0h	Reserved
3-0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset type: SYSRSn

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9 TX_PING_CTRL Register (Offset = 14h) [Reset = 0000h]

TX_PING_CTRL is shown in Figure 29-25 and described in Table 29-28.

Return to the Summary Table.

Transmit ping control register

Figure 29-25. TX_PING_CTRL Register

15	14	13	12	11	10	9	8
RESERVED						EXT_TRIG_SEL	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
EXT_TRIG_SEL					EXT_TRIG_EN	TIMER_EN	CNT_RST
R/W-0h					R/W-0h	R/W-0h	R/W-0h

Table 29-37. TX_PING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-3	EXT_TRIG_SEL	R/W	0h	External Trigger Select bits This bitfield will select one of the 128 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h (R/W) = Trigger 1 will be used to generate a ping frame. 1h (R/W) = Trigger 2 will be used to generate a ping frame. .. 7Fh (R/W) = Trigger 128 will be used to generate a ping frame. Reset type: SYSRSn
2	EXT_TRIG_EN	R/W	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h (R/W) = External triggers will not be used to generate ping frames. 1h (R/W) = The selected external trigger (selected by EXT_TRIG_SEL bits) will be able to generate a ping frame. The ping timer will be ignored if this bit is set. Reset type: SYSRSn
1	TIMER_EN	R/W	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h (R/W) = The ping timer is disabled and will not generate ping frames. 1h (R/W) = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function. Reset type: SYSRSn
0	CNT_RST	R/W	0h	Ping Counter Reset bit Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter. 0h (R/W) = Clear the CNT_RST. 1h (R/W) = The ping counter will be reset to 0. Reset type: SYSRSn

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10 TX_PING_TAG Register (Offset = 16h) [Reset = 0000h]

TX_PING_TAG is shown in Figure 29-26 and described in Table 29-29.

Return to the Summary Table.

Transmit ping tag register

Figure 29-26. TX_PING_TAG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TAG			
R-0h				R/W-0h			

Table 29-39. TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	TAG	R/W	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value. Reset type: SYSRSn

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11 TX_PING_TO_REF Register (Offset = 18h) [Reset = 00000000h]

TX_PING_TO_REF is shown in Figure 29-27 and described in Table 29-30.

Return to the Summary Table.

Transmit ping timeout counter reference

Figure 29-27. TX_PING_TO_REF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_REF																															
R/W-0h																															

Table 29-41. TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TO_REF	R/W	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting. Reset type: SYSRSn

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12 TX_PING_TO_CNT Register (Offset = 1Ch) [Reset = 00000000h]

TX_PING_TO_CNT is shown in Figure 29-28 and described in Table 29-31.

Return to the Summary Table.

Transmit ping timeout current count

Figure 29-28. TX_PING_TO_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO_CNT																															
R-0h																															

Table 29-43. TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TO_CNT	R	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value (TX_PING_TO_REF), at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter Reset type: SYSRSn

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13 TX_INT_CTRL Register (Offset = 20h) [Reset = 0000h]

TX_INT_CTRL is shown in Figure 29-29 and described in Table 29-32.

Return to the Summary Table.

Transmit interrupt event control register

Figure 29-29. TX_INT_CTRL Register

15	14	13	12	11	10	9	8
RESERVED				INT2_EN_PING_TO	INT2_EN_BUF_OVERRUN	INT2_EN_BUF_UNDERRUN	INT2_EN_FRAME_DONE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				INT1_EN_PING_TO	INT1_EN_BUF_OVERRUN	INT1_EN_BUF_UNDERRUN	INT1_EN_FRAME_DONE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 29-45. TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	INT2_EN_PING_TO	R/W	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT2. Reset type: SYSRSn
10	INT2_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT2. Reset type: SYSRSn
9	INT2_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT2. Reset type: SYSRSn
8	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT2. Reset type: SYSRSn
7-4	RESERVED	R	0h	Reserved
3	INT1_EN_PING_TO	R/W	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT1. Reset type: SYSRSn

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Table 29-45. TX_INT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT1_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT1. Reset type: SYSRSn
1	INT1_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT1. Reset type: SYSRSn
0	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT1. Reset type: SYSRSn

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14 TX_DMA_CTRL Register (Offset = 22h) [Reset = 0000h]

TX_DMA_CTRL is shown in Figure 29-30 and described in Table 29-33.

Return to the Summary Table.

Transmit DMA event control register

Figure 29-30. TX_DMA_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMA_EVT_EN
R-0h							R/W-0h

Table 29-47. TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames. Reset type: SYSRSn

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15 TX_LOCK_CTRL Register (Offset = 24h) [Reset = 0000h]

TX_LOCK_CTRL is shown in Figure 29-31 and described in Table 29-34.

Return to the Summary Table.

Transmit lock control register

Figure 29-31. TX_LOCK_CTRL Register

15	14	13	12	11	10	9	8
KEY							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0h							R/W-0h

Table 29-49. TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	W	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset type: SYSRSn
7-1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h (R/W) = Transmit control registers can be modified and are not locked. 1h (R/W) = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn

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16 TX_EVT_STS Register (Offset = 28h) [Reset = 0000h]

TX_EVT_STS is shown in Figure 29-32 and described in Table 29-35.

Return to the Summary Table.

Transmit event and error status flag register

Figure 29-32. TX_EVT_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R-0h				R-0h	R-0h	R-0h	R-0h

Table 29-51. TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	PING_TRIGGERED	R	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = A ping frame has not been triggered. 1h (R) = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset type: SYSRSn
2	BUF_OVERRUN	R	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Overrun has not occured. 1h (R) = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset type: SYSRSn
1	BUF_UNDERRUN	R	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Underrun has not occured. 1h (R) = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset type: SYSRSn
0	FRAME_DONE	R	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Frame Done condition has not occured. 1h (R) = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register. Reset type: SYSRSn

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17 TX_EVT_CLR Register (Offset = 2Ch) [Reset = 0000h]

TX_EVT_CLR is shown in Figure 29-33 and described in Table 29-36.

Return to the Summary Table.

Transmit event and error clear register

Figure 29-33. TX_EVT_CLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R-0h				W-0h	W-0h	W-0h	W-0h

Table 29-53. TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event. Reset type: SYSRSn
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset type: SYSRSn
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset type: SYSRSn
0	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Reset type: SYSRSn

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18 TX_EVT_FRC Register (Offset = 2Eh) [Reset = 0000h]

TX_EVT_FRC is shown in Figure 29-34 and described in Table 29-37.

Return to the Summary Table.

Transmit event and error flag force register

Figure 29-34. TX_EVT_FRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R-0h				W-0h	W-0h	W-0h	W-0h

Table 29-55. TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register. Reset type: SYSRSn
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Force the corresponding flag bit in the TX_EVT_STS Register. Reset type: SYSRSn
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register. Reset type: SYSRSn
0	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register. Reset type: SYSRSn

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19 TX_USER_CRC Register (Offset = 30h) [Reset = 0000h]

TX_USER_CRC is shown in Figure 29-35 and described in Table 29-38.

Return to the Summary Table.

Transmit user-defined CRC register

Figure 29-35. TX_USER_CRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
USER_CRC							
R/W-0h							

Table 29-57. TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	USER_CRC	R/W	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option (TX_OPER_CTRL_LO.SW_CRC = 1). This register is ignored if the hardware CRC generation is enabled. Reset type: SYSRSn

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20 TX_ECC_DATA Register (Offset = 40h) [Reset = 00000000h]

TX_ECC_DATA is shown in Figure 29-36 and described in Table 29-39.

Return to the Summary Table.

Transmit ECC data register

Figure 29-36. TX_ECC_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_HIGH																DATA_LOW															
R/W-0h																R/W-0h															

Table 29-59. TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset type: SYSRSn
15-0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset type: SYSRSn

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21 TX_ECC_VAL Register (Offset = 44h) [Reset = 000Ch]

TX_ECC_VAL is shown in Figure 29-37 and described in Table 29-40.

Return to the Summary Table.

Transmit ECC value register

Figure 29-37. TX_ECC_VAL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ECC_VAL						
R-0h	R-Ch						

Table 29-61. TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-0	ECC_VAL	R	Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register. Reset type: SYSRSn

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22 TX_DLYLINE_CTRL Register (Offset = 48h) [Reset = 0000h]

TX_DLYLINE_CTRL is shown in Figure 29-38 and described in Table 29-41.

Return to the Summary Table.

Transmit delay Line control register

Figure 29-38. TX_DLYLINE_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	TXD1_DLY					TXD0_DLY	
R-0h	R/W-0h					R/W-0h	
7	6	5	4	3	2	1	0
TXD0_DLY			TXCLK_DLY				
R/W-0h			R/W-0h				

Table 29-63. TX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-10	TXD1_DLY	R/W	0h	Delay Line Tap Select for TXD1 This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD1 path. 2h (R/W) Two delay elements are included in the TXD1 path. ... 1Fh (R/W) 31 delay elements are included in the TXD1 path, the maximum. Reset type: SYSRSn
9-5	TXD0_DLY	R/W	0h	Delay Line Tap Select for TXD0 This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD0 path. 2h (R/W) Two delay elements are included in the TXD0 path. ... 1Fh (R/W) 31 delay elements are included in the TXD0 path, the maximum. Reset type: SYSRSn
4-0	TXCLK_DLY	R/W	0h	Delay Line Tap Select for TXCLK This bitfield selects the number of delay elements inserted into the TXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the TXCLK path. 2h (R/W) Two delay elements are included in the TXCLK path. ... 1Fh (R/W) 31 delay elements are included in the TXCLK path, the maximum. Reset type: SYSRSn

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23 TX_BUF_BASE_y Register (Offset = 80h + formula) [Reset = 0000h]

TX_BUF_BASE_y is shown in Figure 29-39 and described in Table 29-42.

Return to the Summary Table.

Base address for transmit buffer

Offset = 80h + (y * 2h); where y = 0h to Fh

Figure 29-39. TX_BUF_BASE_y Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R/W-0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R/W-0h							

Table 29-65. TX_BUF_BASE_y Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BASE_ADDRESS	R/W	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter. Reset type: SYSRSn

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29.5.3 FSI_RX_REGS Registers

Table 29-43 lists the memory-mapped registers for the FSI_RX_REGS registers. All register offset addresses not listed in Table 29-43 should be considered as reserved locations and the register contents should not be modified.

Table 29-66. FSI_RX_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	RX_MAIN_CTRL	Receive main control register		Go
8h	RX_OPER_CTRL	Receive operation control register		Go
Ch	RX_FRAME_INFO	Receive frame control register		Go
Eh	RX_FRAME_TAG_UDATA	Receive frame tag and user data register		Go
10h	RX_DMA_CTRL	Receive DMA event control register		Go
14h	RX_EVT_STS	Receive event and error status flag register		Go
16h	RX_CRC_INFO	Receive CRC info of received and computed CRC		Go
18h	RX_EVT_CLR	Receive event and error clear register		Go
1Ah	RX_EVT_FRC	Receive event and error flag force register		Go
1Ch	RX_BUF_PTR_LOAD	Receive buffer pointer load register		Go
1Eh	RX_BUF_PTR_STS	Receive buffer pointer status register		Go
20h	RX_FRAME_WD_CTRL	Receive frame watchdog control register		Go
24h	RX_FRAME_WD_REF	Receive frame watchdog counter reference		Go
28h	RX_FRAME_WD_CNT	Receive frame watchdog current count		Go
2Ch	RX_PING_WD_CTRL	Receive ping watchdog control register		Go
2Eh	RX_PING_TAG	Receive ping tag register		Go
30h	RX_PING_WD_REF	Receive ping watchdog counter reference		Go
34h	RX_PING_WD_CNT	Receive pingwatchdog current count		Go
38h	RX_INT1_CTRL	Receive interrupt control register for RX_INT1		Go
3Ah	RX_INT2_CTRL	Receive interrupt control register for RX_INT2		Go
3Ch	RX_LOCK_CTRL	Receive lock control register		Go
40h	RX_ECC_DATA	Receive ECC data register		Go
44h	RX_ECC_VAL	Receive ECC value register		Go
48h	RX_ECC_SEC_DATA	Receive ECC corrected data register		Go
4Ch	RX_ECC_LOG	Receive ECC log and status register		Go
50h	RX_FRAME_TAG_CMP	Receive frame tag compare register		Go
52h	RX_PING_TAG_CMP	Receive ping tag compare register		Go
58h	RX_TRIG_CTRL_0	Receive Trigger Control register 0		Go
5Ch	RX_TRIG_WIDTH_0	Receive Trigger Wdith register 0		Go
60h	RX_DLYLINE_CTRL	Receive delay line control register		Go
64h	RX_TRIG_CTRL_1	Receive Trigger Control register 1		Go
68h	RX_TRIG_CTRL_2	Receive Trigger Control register 2		Go
6Ch	RX_TRIG_CTRL_3	Receive Trigger Control register 3		Go
70h	RX_VIS_1	Receive debug visibility register 1		Go
74h	RX_UDATA_FILTER	Receive User Data Filter Control register		Go
80h + formula	RX_BUF_BASE_y	Base address for receive data buffer		Go

Complex bit access types are encoded to fit into small table cells. Table 29-44 shows the codes that are used for access types in this section.

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Table 29-67. FSI_RX_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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1 RX_MAIN_CTRL Register (Offset = 0h) [Reset = 0000h]

RX_MAIN_CTRL is shown in Figure 29-40 and described in Table 29-45.

Return to the Summary Table.

Receive main control register

Figure 29-40. RX_MAIN_CTRL Register

15	14	13	12	11	10	9	8
KEY							
W-0h							
7	6	5	4	3	2	1	0
RESERVED			DATA_FILTER_EN	INPUT_ISOLATE	SPI_PAIRING	INT_LOOPBACK	CORE_RST
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 29-69. RX_MAIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4	DATA_FILTER_EN	R/W	0h	Data Filter Enable Bit. 0h (R/W) = Data filtering is disabled. 1h (R/W) = Data filtering is enabled. Reset type: SYSRSn
3	INPUT_ISOLATE	R/W	0h	When set to 1, the FSI RX inputs (RXCLK, RXD0 and RXD1) will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not affect the RX module itself. Reset type: SYSRSn
2	SPI_PAIRING	R/W	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI controller, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only (RX_OPER_CTRL.SPI_MODE = 1) 0h (R/W) = SPI clock pairing is not enabled. 1h (R/W) = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn

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Table 29-69. RX_MAIN_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_LOOPBACK	R/W	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h (R/W) = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h (R/W) = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn
0	CORE_RST	R/W	0h	Receiver Main Core Reset bit This bit controls the receiver main core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h (R/W) = Receiver core is not in reset and can receive frames. 1h (R/W) = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn

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2 RX_OPER_CTRL Register (Offset = 8h) [Reset = 0000h]

RX_OPER_CTRL is shown in Figure 29-41 and described in Table 29-46.

Return to the Summary Table.

Receive operation control register

Figure 29-41. RX_OPER_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							PING_WD_RST_MODE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
ECC_SEL	N_WORDS				SPI_MODE	DATA_WIDTH	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	

Table 29-71. RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	PING_WD_RST_MODE	R/W	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h (R/W) = The ping watchdog counter will reset and restart only by ping frames. 1h (R/W) = The ping watchdog counter will reset and restart by any received frame. Reset type: SYSRSn
7	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used. Reset type: SYSRSn
6-3	N_WORDS	R/W	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data). Reset type: SYSRSn
2	SPI_MODE	R/W	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode. Reset type: SYSRSn

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Table 29-71. RX_OPER_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	DATA_WIDTH	R/W	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h (R/W) = Data will be received on one data line, RXD0. 1h (R/W) = Data will be received on two data lines, RXD0 and RXD1. 2h, 3h (R/W) = Reserved Reset type: SYSRSn

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3 RX_FRAME_INFO Register (Offset = Ch) [Reset = 0000h]

RX_FRAME_INFO is shown in Figure 29-42 and described in Table 29-47.

Return to the Summary Table.

Receive frame control register

Figure 29-42. RX_FRAME_INFO Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				FRAME_TYPE			
R-0h				R-0h			

Table 29-73. RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	FRAME_TYPE	R	0h	Received Frame Type This field indicates the type of non-ping frame that was successfully received last. Note: Ping frame reception does not update this field, we want to retain the last successful non-ping frame FRAME_TYPE and PING_FRAME_RCVD flag already conveys PING info to the user. 0100b (R/W) = A DATA_1_WORD frame was received (16-bit data). 0101b (R/W) = A DATA_2_WORD frame was received (32-bit data). 0110b (R/W) = A DATA_4_WORD frame was received (64-bit data). 0111b (R/W) = A DATA_6_WORD frame was received (96-bit data). 0011b (R/W) = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words (1 to 16) to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b (R/W) = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used. Reset type: SYSRSn

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4 RX_FRAME_TAG_UDATA Register (Offset = Eh) [Reset = 0000h]

RX_FRAME_TAG_UDATA is shown in Figure 29-43 and described in Table 29-48.

Return to the Summary Table.

Receive frame tag and user data register

Figure 29-43. RX_FRAME_TAG_UDATA Register

15	14	13	12	11	10	9	8
USER_DATA							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			FRAME_TAG				RESERVED
R-0h			R-0h				R-0h

Table 29-75. RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	USER_DATA	R	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4-1	FRAME_TAG	R	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset type: SYSRSn
0	RESERVED	R	0h	Reserved

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5 RX_DMA_CTRL Register (Offset = 10h) [Reset = 0000h]

RX_DMA_CTRL is shown in Figure 29-44 and described in Table 29-49.

Return to the Summary Table.

Receive DMA event control register

Figure 29-44. RX_DMA_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMA_EVT_EN
R-0h							R/W-0h

Table 29-77. RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames. Reset type: SYSRSn

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6 RX_EVT_STS Register (Offset = 14h) [Reset = 0000h]

RX_EVT_STS is shown in Figure 29-45 and described in Table 29-50.

Return to the Summary Table.

Receive event and error status flag register

Figure 29-45. RX_EVT_STS Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 29-79. RX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	ERROR_TAG_MATCH	R	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched error frame received. 1h (R) = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
13	DATA_TAG_MATCH	R	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched data frame received. 1h (R) = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
12	PING_TAG_MATCH	R	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched ping frame received. 1h (R) = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
11	DATA_FRAME	R	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No data frame has been received. 1h (R) = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn

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Table 29-79. RX_EVT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	FRAME_OVERRUN	R	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame overrun has not ocurred. 1h (R) = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
9	PING_FRAME	R	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No ping frame has been received. 1h (R) = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
8	ERR_FRAME	R	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No error frame has been received. 1h (R) = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
7	BUF_UNDERRUN	R	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive Buffer Underrun has not ocurred. 1h (R) = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
6	FRAME_DONE	R	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No frame has been successfully received. 1h (R) = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn

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Table 29-79. RX_EVT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUF_OVERRUN	R	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive buffer overrun has not ocurred. 1h (R) = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
4	EOF_ERR	R	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid end-of-frame has not been received. 1h (R) = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
3	TYPE_ERR	R	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid frame type has not been received. 1h (R) = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
2	CRC_ERR	R	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = CRC error has not occured. 1h (R) = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
1	FRAME_WD_TO	R	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame watchdog timeout has not occured. 1h (R) = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn
0	PING_WD_TO	R	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Ping watchdog timeout has not occured. 1h (R) = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. Reset type: SYSRSn

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7 RX_CRC_INFO Register (Offset = 16h) [Reset = 0000h]

RX_CRC_INFO is shown in Figure 29-46 and described in Table 29-51.

Return to the Summary Table.

Receive CRC info of received and computed CRC

Figure 29-46. RX_CRC_INFO Register

15	14	13	12	11	10	9	8
CALC_CRC							
R-0h							
7	6	5	4	3	2	1	0
RX_CRC							
R-0h							

Table 29-81. RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CALC_CRC	R	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset type: SYSRSn
7-0	RX_CRC	R	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames. Reset type: SYSRSn

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8 RX_EVT_CLR Register (Offset = 18h) [Reset = 0000h]

RX_EVT_CLR is shown in Figure 29-47 and described in Table 29-52.

Return to the Summary Table.

Receive event and error clear register

Figure 29-47. RX_EVT_CLR Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 29-83. RX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
11	DATA_FRAME	W	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn

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Table 29-83. RX_EVT_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PING_FRAME	W	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
8	ERR_FRAME	W	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
6	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
4	EOF_ERR	W	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
3	TYPE_ERR	W	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
2	CRC_ERR	W	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn

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Table 29-83. RX_EVT_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. Reset type: SYSRSn

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9 RX_EVT_FRC Register (Offset = 1Ah) [Reset = 0000h]

RX_EVT_FRC is shown in Figure 29-48 and described in Table 29-53.

Return to the Summary Table.

Receive event and error flag force register

Figure 29-48. RX_EVT_FRC Register

15	14	13	12	11	10	9	8
RESERVED	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 29-85. RX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
11	DATA_FRAME	W	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn

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Table 29-85. RX_EVT_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PING_FRAME	W	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
8	ERR_FRAME	W	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
6	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
4	EOF_ERR	W	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
3	TYPE_ERR	W	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn

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Table 29-85. RX_EVT_FRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CRC_ERR	W	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register. Reset type: SYSRSn

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10 RX_BUF_PTR_LOAD Register (Offset = 1Ch) [Reset = 0000h]

RX_BUF_PTR_LOAD is shown in Figure 29-49 and described in Table 29-54.

Return to the Summary Table.

Receive buffer pointer load register

Figure 29-49. RX_BUF_PTR_LOAD Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				BUF_PTR_LOAD			
R-0h				R/W-0h			

Table 29-87. RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after (3 RXCLK + 3 SYCLK) cycles. Reset type: SYSRSn

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11 RX_BUF_PTR_STS Register (Offset = 1Eh) [Reset = 0000h]

RX_BUF_PTR_STS is shown in Figure 29-50 and described in Table 29-55.

Return to the Summary Table.

Receive buffer pointer status register

Figure 29-50. RX_BUF_PTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			CURR_WORD_CNT				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED				CURR_BUF_PTR			
R-0h				R-0h			

Table 29-89. RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	CURR_WORD_CNT	R	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition. Reset type: SYSRSn
7-4	RESERVED	R	0h	Reserved
3-0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission. Reset type: SYSRSn

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12 RX_FRAME_WD_CTRL Register (Offset = 20h) [Reset = 0000h]

RX_FRAME_WD_CTRL is shown in Figure 29-51 and described in Table 29-56.

Return to the Summary Table.

Receive frame watchdog control register

Figure 29-51. RX_FRAME_WD_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						FRAME_WD_EN	FRAME_WD_CNT_RST
R-0h						R/W-0h	R/W-0h

Table 29-91. RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	FRAME_WD_EN	R/W	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter (RX_FRAME_WD_CNT) will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value (RX_FRAME_WD_REF) is reached, it will generate a frame watchdog timeout event (RX_EVT_STS.FRAME_WD_TO) and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h (R/W) = The frame watchdog counter is disabled and not running. 1h (R/W) = The frame watchdog counter logic is enabled and running. Reset type: SYSRSn
0	FRAME_WD_CNT_RST	R/W	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the FRAME_WD_CNT_RST. 1h (W) = The frame watchdog counter will be reset to 0. Reset type: SYSRSn

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13 RX_FRAME_WD_REF Register (Offset = 24h) [Reset = 00000000h]

RX_FRAME_WD_REF is shown in Figure 29-52 and described in Table 29-57.

Return to the Summary Table.

Receive frame watchdog counter reference

Figure 29-52. RX_FRAME_WD_REF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_REF																															
R/W-0h																															

Table 29-93. RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FRAME_WD_REF	R/W	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached. Reset type: SYSRSn

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14 RX_FRAME_WD_CNT Register (Offset = 28h) [Reset = 00000000h]

RX_FRAME_WD_CNT is shown in Figure 29-53 and described in Table 29-58.

Return to the Summary Table.

Receive frame watchdog current count

Figure 29-53. RX_FRAME_WD_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_WD_CNT																															
R-0h																															

Table 29-95. RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FRAME_WD_CNT	R	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame. Reset type: SYSRSn

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15 RX_PING_WD_CTRL Register (Offset = 2Ch) [Reset = 0000h]

RX_PING_WD_CTRL is shown in Figure 29-54 and described in Table 29-59.

Return to the Summary Table.

Receive ping watchdog control register

Figure 29-54. RX_PING_WD_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PING_WD_EN	PING_WD_RST
R-0h						R/W-0h	R/W-0h

Table 29-97. RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	PING_WD_EN	R/W	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter (RX_PING_WD_CNT) will begin counting from 0 when it is enabled. When the reference value (RX_PING_WD_REF) is reached, it will generate a ping watchdog timeout event (RX_EVT_STS.PING_WD_TO) and the counter value will reset to 0, and resume counting 0h (R/W) = The ping watchdog counter is disabled and not running. 1h (R/W) = The ping watchdog counter logic is enabled and running. Reset type: SYSRSn
0	PING_WD_RST	R/W	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the PING_WD_RST. 1h (W) = The ping watchdog counter will be reset to 0. Reset type: SYSRSn

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16 RX_PING_TAG Register (Offset = 2Eh) [Reset = 0000h]

RX_PING_TAG is shown in Figure 29-55 and described in Table 29-60.

Return to the Summary Table.

Receive ping tag register

Figure 29-55. RX_PING_TAG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			PING_TAG				RESERVED
R-0h			R-0h				R-0h

Table 29-99. RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4-1	PING_TAG	R	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag. Reset type: SYSRSn
0	RESERVED	R	0h	Reserved

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17 RX_PING_WD_REF Register (Offset = 30h) [Reset = 00000000h]

RX_PING_WD_REF is shown in Figure 29-56 and described in Table 29-61.

Return to the Summary Table.

Receive ping watchdog counter reference

Figure 29-56. RX_PING_WD_REF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_REF																															
R/W-0h																															

Table 29-101. RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PING_WD_REF	R/W	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached. Reset type: SYSRSn

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18 RX_PING_WD_CNT Register (Offset = 34h) [Reset = 00000000h]

RX_PING_WD_CNT is shown in Figure 29-57 and described in Table 29-62.

Return to the Summary Table.

Receive pingwatchdog current count

Figure 29-57. RX_PING_WD_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PING_WD_CNT																															
R-0h																															

Table 29-103. RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PING_WD_CNT	R	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame. Reset type: SYSRSn

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19 RX_INT1_CTRL Register (Offset = 38h) [Reset = 0000h]

RX_INT1_CTRL is shown in Figure 29-58 and described in Table 29-63.

Return to the Summary Table.

Receive interrupt control register for RX_INT1

Figure 29-58. RX_INT1_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	INT1_EN_ERROR_TAG_MATCH	INT1_EN_DATA_TAG_MATCH	INT1_EN_PING_TAG_MATCH	INT1_EN_DATA_FRAME	INT1_EN_FRAME_OVERRUN	INT1_EN_PING_FRAME	INT1_EN_ERR_FRAME
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT1_EN_UNDERRUN	INT1_EN_FRAME_DONE	INT1_EN_OVERRUN	INT1_EN_EOF_ERR	INT1_EN_TYPE_ERR	INT1_EN_CRC_ERR	INT1_EN_FRAME_WD_TO	INT1_EN_PING_WD_TO
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 29-105. RX_INT1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	INT1_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
13	INT1_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
12	INT1_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
11	INT1_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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Table 29-105. RX_INT1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT1_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
9	INT1_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
8	INT1_EN_ERR_FRAME	R/W	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
7	INT1_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
6	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
5	INT1_EN_OVERRUN	R/W	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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Table 29-105. RX_INT1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT1_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
3	INT1_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
2	INT1_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
1	INT1_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
0	INT1_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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20 RX_INT2_CTRL Register (Offset = 3Ah) [Reset = 0000h]

RX_INT2_CTRL is shown in Figure 29-59 and described in Table 29-64.

Return to the Summary Table.

Receive interrupt control register for RX_INT2

Figure 29-59. RX_INT2_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	INT2_EN_ERROR_TAG_MATCH	INT2_EN_DATA_TAG_MATCH	INT2_EN_PING_TAG_MATCH	INT2_EN_DATA_FRAME	INT2_EN_FRAME_OVERRUN	INT2_EN_PING_FRAME	INT2_EN_ERR_FRAME
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INT2_EN_UNDERRUN	INT2_EN_FRAME_DONE	INT2_EN_OVERRUN	INT2_EN_EOF_ERR	INT2_EN_TYPE_ERR	INT2_EN_CRC_ERR	INT2_EN_FRAME_WD_TO	INT2_EN_PING_WD_TO
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 29-107. RX_INT2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	INT2_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
13	INT2_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
12	INT2_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
11	INT2_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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Table 29-107. RX_INT2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT2_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
9	INT2_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
8	INT2_EN_ERR_FRAME	R/W	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
7	INT2_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
6	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
5	INT2_EN_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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Table 29-107. RX_INT2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	INT2_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
3	INT2_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
2	INT2_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
1	INT2_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn
0	INT2_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register Reset type: SYSRSn

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21 RX_LOCK_CTRL Register (Offset = 3Ch) [Reset = 0000h]

RX_LOCK_CTRL is shown in Figure 29-60 and described in Table 29-65.

Return to the Summary Table.

Receive lock control register

Figure 29-60. RX_LOCK_CTRL Register

15	14	13	12	11	10	9	8
KEY							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0h							R/W-0h

Table 29-109. RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register. Reset type: SYSRSn
7-1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h (R/W) = Receive control registers can be modified and are not locked. 1h (R/W) = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect. Reset type: SYSRSn

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22 RX_ECC_DATA Register (Offset = 40h) [Reset = 00000000h]

RX_ECC_DATA is shown in Figure 29-61 and described in Table 29-66.

Return to the Summary Table.

Receive ECC data register

Figure 29-61. RX_ECC_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_HIGH																DATA_LOW															
R/W-0h																R/W-0h															

Table 29-111. RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. Reset type: SYSRSn
15-0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits. Reset type: SYSRSn

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23 RX_ECC_VAL Register (Offset = 44h) [Reset = 0000h]

RX_ECC_VAL is shown in Figure 29-62 and described in Table 29-67.

Return to the Summary Table.

Receive ECC value register

Figure 29-62. RX_ECC_VAL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ECC_VAL						
R-0h	R/W-0h						

Table 29-113. RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-0	ECC_VAL	R/W	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register. Reset type: SYSRSn

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24 RX_ECC_SEC_DATA Register (Offset = 48h) [Reset = 00000000h]

RX_ECC_SEC_DATA is shown in Figure 29-63 and described in Table 29-68.

Return to the Summary Table.

Receive ECC corrected data register

Figure 29-63. RX_ECC_SEC_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEC_DATA																															
R-0h																															

Table 29-115. RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEC_DATA	R	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used. Reset type: SYSRSn

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25 RX_ECC_LOG Register (Offset = 4Ch) [Reset = 0003h]

RX_ECC_LOG is shown in Figure 29-64 and described in Table 29-69.

Return to the Summary Table.

Receive ECC log and status register

Figure 29-64. RX_ECC_LOG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MBE	SBE
R-0h						R-1h	R-1h

Table 29-117. RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	MBE	R	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h (R) Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h (R) Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used. Reset type: SYSRSn
0	SBE	R	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h (R) No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h (R) A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA. Reset type: SYSRSn

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26 RX_FRAME_TAG_CMP Register (Offset = 50h) [Reset = 0000h]

RX_FRAME_TAG_CMP is shown in Figure 29-65 and described in Table 29-70.

Return to the Summary Table.

Receive frame tag compare register

Figure 29-65. RX_FRAME_TAG_CMP Register

15	14	13	12	11	10	9	8
RESERVED						BROADCAST_EN	CMP_EN
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
R/W-0h				R/W-0h			

Table 29-119. RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled. Reset type: SYSRSn
8	CMP_EN	R/W	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h (R/W) Frame tag comparison is disabled. 1h (R/W) Frame tag comparison is enabled. Reset type: SYSRSn
7-4	TAG_MASK	R/W	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames. Reset type: SYSRSn
3-0	TAG_REF	R/W	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames. Reset type: SYSRSn

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27 RX_PING_TAG_CMP Register (Offset = 52h) [Reset = 0000h]

RX_PING_TAG_CMP is shown in Figure 29-66 and described in Table 29-71.

Return to the Summary Table.

Receive ping tag compare register

Figure 29-66. RX_PING_TAG_CMP Register

15	14	13	12	11	10	9	8
RESERVED						BROADCAST_EN	CMP_EN
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TAG_MASK				TAG_REF			
R/W-0h				R/W-0h			

Table 29-121. RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled. Reset type: SYSRSn
8	CMP_EN	R/W	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h (R/W) Ping tag comparison is disabled. 1h (R/W) Ping tag comparison is enabled. Reset type: SYSRSn
7-4	TAG_MASK	R/W	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames. Reset type: SYSRSn
3-0	TAG_REF	R/W	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames. Reset type: SYSRSn

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28 RX_TRIG_CTRL_0 Register (Offset = 58h) [Reset = 00000000h]

RX_TRIG_CTRL_0 is shown in Figure 29-67 and described in Table 29-72.

Return to the Summary Table.

Receive Trigger Control register 0

Figure 29-67. RX_TRIG_CTRL_0 Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W-0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W-0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				TRIG_EN
R-0h			R/W-0h				R/W-0h

Table 29-123. RX_TRIG_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4-1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset type: SYSRSn
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset type: SYSRSn

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29 RX_TRIG_WIDTH_0 Register (Offset = 5Ch) [Reset = 00000000h]

RX_TRIG_WIDTH_0 is shown in Figure 29-68 and described in Table 29-73.

Return to the Summary Table.

Receive Trigger Wdith register 0

Figure 29-68. RX_TRIG_WIDTH_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_TRIG_WIDTH															
R-0h																R/W-0h															

Table 29-125. RX_TRIG_WIDTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RX_TRIG_WIDTH	R/W	0h	This register decides the width(in SYSCLK cycles) of wide pulse output of the RX trigger module. Reset type: SYSRSn

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30 RX_DLYLINE_CTRL Register (Offset = 60h) [Reset = 0000h]

RX_DLYLINE_CTRL is shown in Figure 29-69 and described in Table 29-74.

Return to the Summary Table.

Receive delay line control register

Figure 29-69. RX_DLYLINE_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	RXD1_DLY					RXD0_DLY	
R-0h	R/W-0h					R/W-0h	
7	6	5	4	3	2	1	0
RXD0_DLY			RXCLK_DLY				
R/W-0h			R/W-0h				

Table 29-127. RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-10	RXD1_DLY	R/W	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD1 path. 2h (R/W) Two delay elements are included in the RXD1 path. ... 1Fh (R/W) 31 delay elements are included in the RXD1 path, the maximum. Reset type: SYSRSn
9-5	RXD0_DLY	R/W	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD0 path. 2h (R/W) Two delay elements are included in the RXD0 path. ... 1Fh (R/W) 31 delay elements are included in the RXD0 path, the maximum. Reset type: SYSRSn
4-0	RXCLK_DLY	R/W	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the RXCLK path. 2h (R/W) Two delay elements are included in the RXCLK path. ... 1Fh (R/W) 31 delay elements are included in the RXCLK path, the maximum. Reset type: SYSRSn

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31 RX_TRIG_CTRL_1 Register (Offset = 64h) [Reset = 00000000h]

RX_TRIG_CTRL_1 is shown in Figure 29-70 and described in Table 29-75.

Return to the Summary Table.

Receive Trigger Control register 1

Figure 29-70. RX_TRIG_CTRL_1 Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W-0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W-0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				TRIG_EN
R-0h			R/W-0h				R/W-0h

Table 29-129. RX_TRIG_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4-1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset type: SYSRSn
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset type: SYSRSn

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32 RX_TRIG_CTRL_2 Register (Offset = 68h) [Reset = 00000000h]

RX_TRIG_CTRL_2 is shown in Figure 29-71 and described in Table 29-76.

Return to the Summary Table.

Receive Trigger Control register 2

Figure 29-71. RX_TRIG_CTRL_2 Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W-0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W-0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				TRIG_EN
R-0h			R/W-0h				R/W-0h

Table 29-131. RX_TRIG_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4-1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset type: SYSRSn
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset type: SYSRSn

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33 RX_TRIG_CTRL_3 Register (Offset = 6Ch) [Reset = 00000000h]

RX_TRIG_CTRL_3 is shown in Figure 29-72 and described in Table 29-77.

Return to the Summary Table.

Receive Trigger Control register 3

Figure 29-72. RX_TRIG_CTRL_3 Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W-0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W-0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				TRIG_EN
R-0h			R/W-0h				R/W-0h

Table 29-133. RX_TRIG_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. Reset type: SYSRSn
7-5	RESERVED	R	0h	Reserved
4-1	TRIG_SEL	R/W	0h	This is the mux select value which selects which of the inputs will be used as the trigger source. Reset type: SYSRSn
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module. Reset type: SYSRSn

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34 RX_VIS_1 Register (Offset = 70h) [Reset = 00000000h]

RX_VIS_1 is shown in Figure 29-73 and described in Table 29-78.

Return to the Summary Table.

Receive debug visibility register 1

Figure 29-73. RX_VIS_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_CORE_STS	RESERVED		
R-0h				R-0h	R-0h		

Table 29-135. RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RX_CORE_STS	R	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h (R) The receiver core is operating normally. 1h (R) The receiver core has entered into an error state and should be reset. Reset type: SYSRSn
2-0	RESERVED	R	0h	Reserved

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35 RX_UDATA_FILTER Register (Offset = 74h) [Reset = 0000h]

RX_UDATA_FILTER is shown in Figure 29-74 and described in Table 29-79.

Return to the Summary Table.

Receive User Data Filter Control register

Figure 29-74. RX_UDATA_FILTER Register

15	14	13	12	11	10	9	8
UDATA_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
UDATA_REF							
R/W-0h							

Table 29-137. RX_UDATA_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	UDATA_MASK	R/W	0h	Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position. Reset type: SYSRSn
7-0	UDATA_REF	R/W	0h	Reference to be used for comparing the USERDATA field when filtering is enabled. Reset type: SYSRSn

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36 RX_BUF_BASE_y Register (Offset = 80h + formula) [Reset = 0000h]

RX_BUF_BASE_y is shown in Figure 29-75 and described in Table 29-80.

Return to the Summary Table.

Base address for receive data buffer

Offset = 80h + (y * 2h); where y = 0h to Fh

Figure 29-75. RX_BUF_BASE_y Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R-0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R-0h							

Table 29-139. RX_BUF_BASE_y Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	BASE_ADDRESS	R	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver. Reset type: SYSRSn

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Chapter 30

Modular Controller Area Network (MCAN)

The Modular Controller Area Network (MCAN) peripheral supports both communication through classic CAN and CAN-FD protocols.

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30.1 MCAN Overview

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices can coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

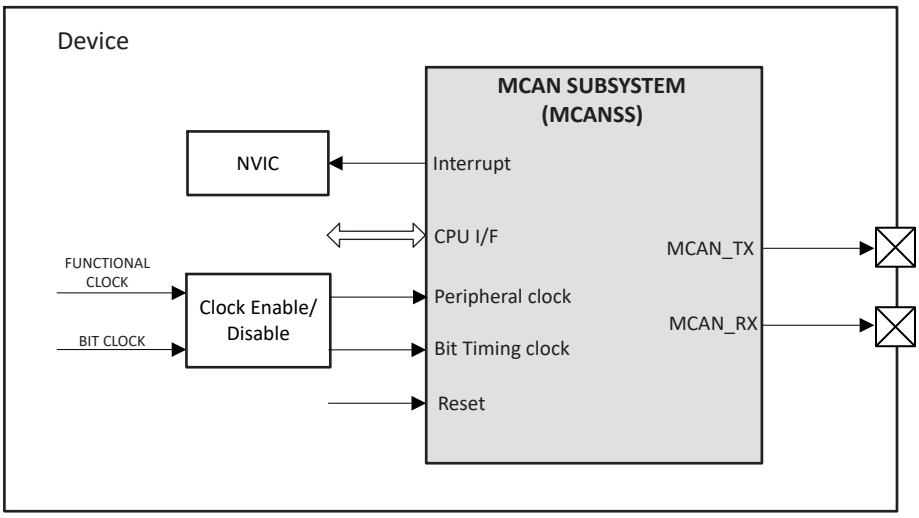


Figure 30-1. MCAN Block Diagram

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30.1.1 MCAN Features

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit Event FIFO, up to 32 elements
- Up to 14 dedicated receive buffers
- Two configurable receive FIFOs, up to 14 elements each with 1kB message RAM.
- Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt
  - 2 configurable interrupt lines
  - Correctable ECC
  - Counter overflow
  - Clock stop or wakeup
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock and host clock)
- ECC check for Message RAM
- Clock stop and wakeup support
- Timestamp counter
- Up to 1-Mbps nominal bit rate, up to 8-Mbps data bit rate

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

30.2 MCAN Environment

The CAN network physical layer consists of a two-wire differential bus, usually twisted pair, and provides a high level of interference immunity. An external CAN transceiver IC is needed to access the bus.

Figure 30-2 shows typical MCAN wiring. Table 30-1 describes the external signals of the MCAN module.

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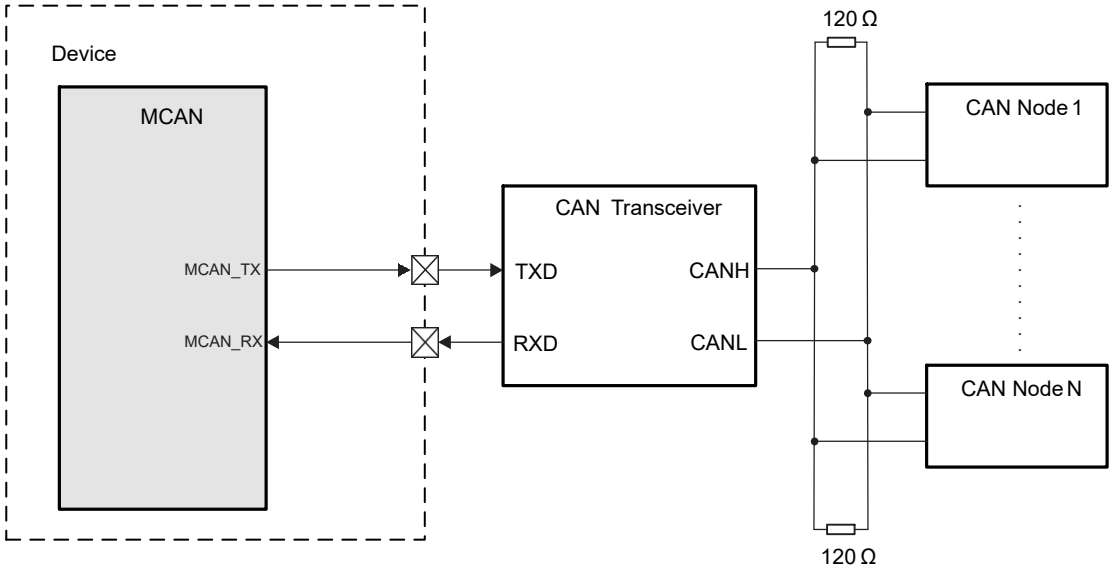


Figure 30-2. MCAN Typical Bus Wiring

Table 30-1. MCAN I/O Description

Module Signal	I/O	Description	Value at Reset
MCAN_RX	Input	Serial data input from external CAN transceiver.	HiZ
MCAN_TX	Output	Serial data output to external CAN transceiver.	HiZ

30.3 CAN Network Basics

The network basics are:

- The CAN bus is a 2-wire differential bus using non-return-to-zero (NRZ) encoding and has two states:
  - Recessive state (logical 1)
  - Dominant state (logical 0)
- When the bus is idle, any node can initiate a transmission to any other node. When two or more nodes (ECUs) attempt to transmit at the same time, a nondestructive arbitration technique sends messages in order of priority so that no messages are lost.
- The message transmission is multicast. Data messages transmitted are identifier-based, not address-based.
- The content of the message is labeled by the identifier that is unique throughout the network (for example: RPM, temperature, position, pressure, and so forth).
- All nodes on the network receive the message and each performs an acceptance test on the identifier. If the message is relevant, it is processed; otherwise, it is ignored.
- The unique identifier also determines the priority of the message (the lower the numerical value of the identifier, the higher the priority).
- Data is transmitted and received using message frames, consisting of the following basic fields:
  - Arbitration field
  - Control field
  - Data field (up to 8 bytes for classical CAN and up to 64 bytes for CAN FD)
  - CRC field
  - ACK field

For more information, see *ISO 11898-1:2015: CAN data link layer and physical signaling*.

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MCAN power up and clock sequence :

1. Select CANCLK from the available clock sources: the HFCLK (XTAL or HFCLK_IN) or the SYSPLL (SYSPLLCLK0).
2. Enable the corresponding clock source.
3. Wait until the clock source is stable (SYSCTL_CLKSTATUS[*GOOD] bit = 1).
4. Enable MCAN power by setting PWREN for MCAN.
5. Wait until MCAN is ready (SYSCTL_SYSSTATUS[MCAN0READY] = 1).

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30.4 MCAN Functional Description

The MCAN module performs CAN protocol communication according to ISO 11898-1:2015. The bit rate can be programmed to values up to 8Mbit/s. Additional transceiver hardware is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message frames can be configured. The message frames and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler.

The register set of the MCAN module can be accessed directly through the module interface. These registers are used to control and configure the CAN core and the Message Handler, and to access the Message RAM.

Figure 30-3 shows the MCAN module block diagram, followed by the description of the MCAN module blocks.

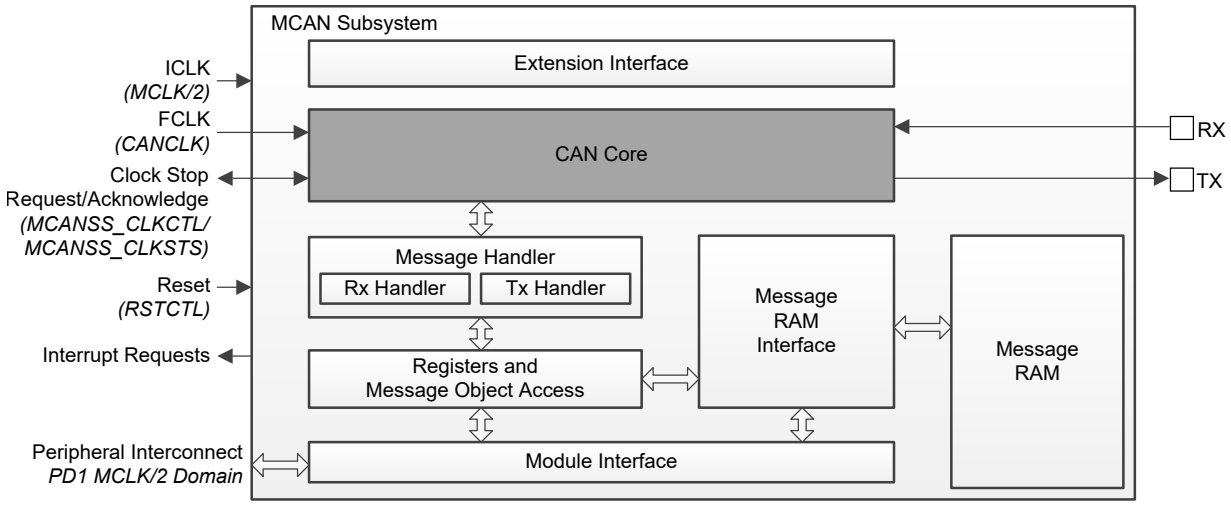


Figure 30-3. MCAN Block Diagram

- **CAN Core**: The CAN core consists of the CAN protocol controller and the Rx/Tx shift register. It handles all ISO 11898-1:2015 protocol functions and supports 11-bit and 29-bit identifiers.
- **Message Handler**: the Message Handler (Rx Handler and Tx Handler) is a state machine that controls the data transfer between the single-ported Message RAM and the CAN core's Rx/Tx shift register. It also handles the acceptance filtering and Interrupt generation as programmed in the control registers.
- **Message RAM**: the main purpose of the Message RAM is to store Rx/Tx messages, Tx Event elements, and Message ID Filter elements (for more information, see Section 30.4.18).
- **Message RAM Interface**: enables a connection between the Message RAM and the other blocks in the MCAN module.
- **Registers and Message Object Access**: Data consistency is ensured by indirect accesses to the message objects. During normal operation, all software and DMA accesses to the Message RAM are done through interface registers. The interface registers have the same word-length as the Message RAM.
- **Module Interface**: The MCAN module registers are accessed by the user's software through a 32-bit peripheral bus interface.
- **Clocking**: Two clocks are provided to the MCAN module: the peripheral synchronous clock (interface clock - MCAN_ICLK sourced from MCLK/2) and the peripheral asynchronous clock (functional clock - MCAN_FCLKsourced from CANCLK).

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- **Extension Interface**: All selected internal status and control signals are routed to this interface (except for the indication signals of configuration change enable bit (MCAN_CCCR.CCE) and Interrupt Register bits (MCAN_IR).

30.4.1 Clock Setup

Peripheral asynchronous clock (MCAN_FCLK) for MCAN can be clocked either through HFXT or SYSPLL. This clock configuration has to be done through SYSCTL REGISTERS. *Refer to CANCLK (CAN-FD Functional Clock) under the Clocks section.*

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30.4.2 Module Clocking Requirements

Two clocks are provided to the MCAN module:

- Host Clock : peripheral synchronous clock (MCAN_ICLK) as the general module clock source, and
- CAN Clock: peripheral asynchronous clock (MCAN_FCLK) provided to the CAN core for generating the CAN bit timing.

Within the MCAN module, there is a synchronization mechanism implemented to make sure there is safe data transfer between the two clock domains. There is synchronization between the signals from the Host clock domain to the CAN clock domain and conversely, and between the reset signal (MCAN_RST) to the Host clock domain and to the CAN clock domain.

Note

MCAN_ICLK must always be higher or equal to MCAN_FCLK to achieve a stable functionality of the MCAN module: $f_{ICLK} \geq f_{FCLK}$

The CAN-FD supports higher speeds of operation and as such has more stringent timing requirements than the classic CAN. For performance, TI recommends using the lowest N-divider value that maintains a working PLL REF_CLK for the system. Lower N-divider values increase the loop bandwidth of the PLL, which in turn improves timing margins for CAN-FD.

The peripheral asynchronous clock (MCAN_FCLK) can be clocked either through HFXT or SYSPLL. The configuration of this has to be done through the SYSCTL registers. Refer to the *Clocks* module for more information

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30.4.3 Operating Modes

The operating modes are discussed in the following sections.

30.4.3.1 Normal Operation

Once the MCAN module is initialized and the MCAN_CCCR.INIT bit is reset to zero, the MCAN module synchronizes itself to the CAN bus and is ready for communication. After passing the acceptance filtering, received messages including Message Identifier (ID) and Data Length Code (DLC) are stored into a dedicated Rx Buffer or into Rx FIFO 0/Rx FIFO 1.

For messages to be transmitted, dedicated Tx buffers, and a Tx FIFO or a Tx queue can be initialized or updated.

Note

Automated transmission upon reception of remote frames is not supported.

30.4.3.2 CAN Classic

CAN supports transmission of data up to 8 bytes with standard (11 bit) or (29 bit) identifier.

30.4.3.3 CAN FD Operation

The CAN FD standard allows extended frames to be sent, up to 64 data bytes in a single frame at a higher bit rate for the data phase of a frame, up to 8 Mbps. The CAN FD standard introduces the ability to switch from one bit rate to another. Extended Data Length (EDL), as shown in Figure 30-4 and described in Table 30-2, sets a data length of up to 8 or 64 data bytes. Bit Rate Switching (BRS) indicates whether two bit rates (the data phase is transmitted at a different bit rate compared to the arbitration phase) are enabled.

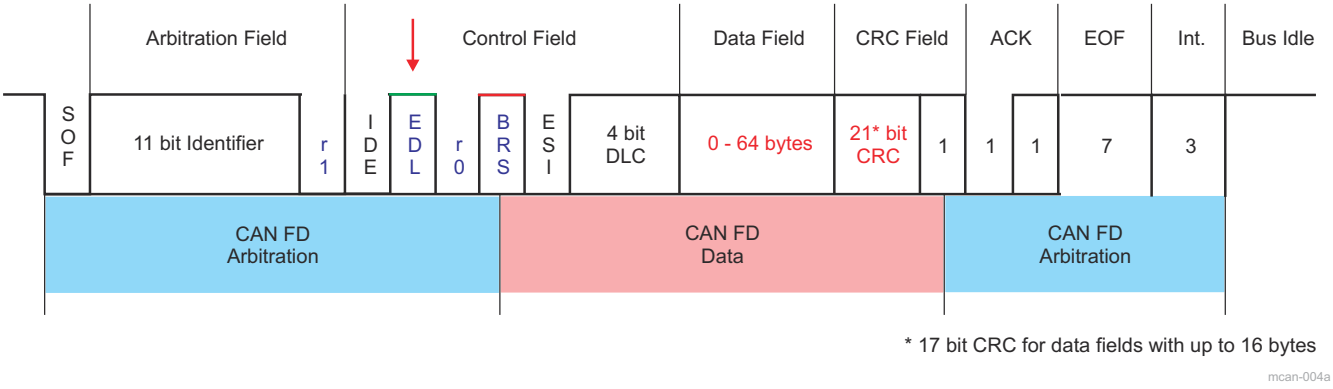


Figure 30-4. CAN FD Frame

Table 30-2. CAN FD Frame Description

Bit/Field	Description
SOF	Start of Frame
Arbitration	Contains the identifier (address) of the message. Used for determining which node gets to transmit.
Control	Contains information about the frame format, including the Data Length Code (DLC, specifies # of data bytes in the frame)
Data	Message data: Up to 8 bytes in classic CAN, up to 64 bytes in CAN-FD
IDE	Identifier extension (for 29 bit extended ID)
FDF	Flexible Data Format
BRS	Bit Rate Switching
ESI	Error Status Indicator

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Table 30-2. CAN FD Frame Description (continued)

Bit/Field	Description
DLC	Data Length Code
CRC	Cyclic Redundancy check
ACK	Acknowledgement bits to indicate successful reception of the frame

There are two variants of CAN FD frame transmission:

- CAN FD frame transmission without bit rate switching
- CAN FD frame transmission where control field, data field, and CRC field are transmitted with a higher bit rate than the beginning and the end of the frame

In the CAN frames, FDF = recessive (logical 1) signifies a CAN FD frame, FDF = dominant (logical 0) signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF - res and BRS, decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by res = dominant and BRS = recessive. Note that the coding of res = recessive is reserved for future expansion of the protocol.
If the MCAN module receives a frame with FDF = recessive and res = recessive, the MCAN signals a Protocol Exception Event by setting the MCAN_PSR.PXE bit. When Protocol Exception Handling is enabled (MCAN_CCCR.PXHD = 0), this causes the operation state to change from Receiver (MCAN_PSR.ACT = 10) to Integrating (MCAN_PSR.ACT = 00) at the next sample point. In case Protocol Exception Handling is disabled (MCAN_CCCR.PXHD = 1), the MCAN treats a recessive bit as an error and responds with an error frame.

CAN FD operation is enabled by programming the MCAN_CCCR.FDOE bit. If MCAN_CCCR.FDOE = 1, transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured using the FDF bit in the respective Tx Buffer element.

With MCAN_CCCR.FDOE = 0, received frames are interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if the FDF bit of a Tx Buffer element is set. The MCAN_CCCR.FDOE and MCAN_CCCR.BRSE bits can only be changed while the MCAN_CCCR.INIT and MCAN_CCCR.CCE bits are both set. With MCAN_CCCR.FDOE = 0, the setting of bits FDF and BRS is ignored and frames are transmitted in Classic CAN format.

With MCAN_CCCR.FDOE = 1 and MCAN_CCCR.BRSE = 0, only FDF bit of a Tx Buffer element is evaluated. With MCAN_CCCR.FDOE = 1 and MCAN_CCCR.BRSE = 1, transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with bits FDF and BRS set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significantly higher than in the CAN FD arbitration phase. In this case, disable the CAN FD bit rate switching option for transmissions.
- During system startup, all nodes are transmitting Classic CAN messages until verified that the nodes are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wakeup messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in Silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

The coding of the DLC in the CAN FD format differs from the standard CAN format. The DLC codes 0 to 8 have the same coding as in standard CAN (0 to 8 data bytes), the codes 9 to 15, which in standard CAN all code a data field of 8 bytes, are coded according to Table 30-3.

Table 30-3. DLC Coding in CAN FD

DLC	9	10	11	12	13	14	15
Number of Data Bytes	12	16	20	24	32	48	64

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CAN-FD Bit Timing

For CAN FD frames, the bit timing is switched inside the frame after the BRS (Bit Rate Switch) bit in case this bit is recessive. In the CAN FD arbitration phase, before the BRS bit, the nominal CAN bit timing (see Figure 30-5) is used as configured by the Nominal Bit Timing and Prescaler Register (MCAN_NBTP). In the following CAN FD data phase, the data phase bit timing is used as configured by the Data Bit Timing and Prescaler Register (MCAN_DBTP). The bit timing is switched back from the data phase timing at the CRC delimiter or when an error is detected, whichever occurs first.

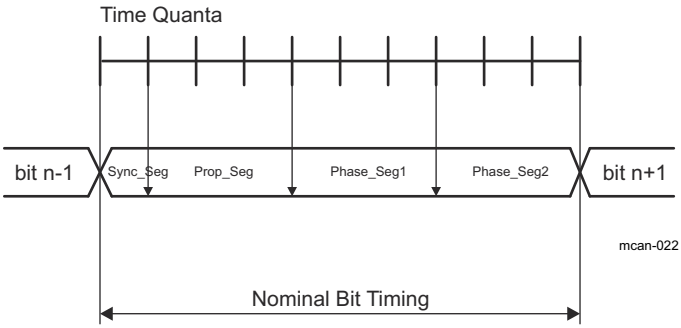


Figure 30-5. CAN Bit Timing

The maximum configurable data phase bit timing depends on the CAN clock frequency (MCAN_FCLK). Example: with MCAN_FCLK = 20MHz and the shortest configurable bit time of 4 t_q (time quanta), the bit rate in the data phase is 5 Mbit/s.

In both data frame formats, CAN FD and CAN FD with bit rate switching, the value of the Error Status Indicator (ESI) bit depends on the transmitter error state (see MCAN_PSR.RESI bit) monitored at the start of the transmission. If the transmitter has an error passive flag, the ESI bit is transmitted recessive; else, the ESI bit is transmitted dominant.

30.4.4 Software Initialization

A software initialization begins when the MCAN_CCCR.INIT bit is set to 1. This is done either by software or by a hardware reset, when an uncorrected bit error is detected in the Message RAM, or by going to a Bus_Off state. While the MCAN_CCCR.INIT bit is set, the message transfer is stopped and the status of the output TX pin is recessive (high). The counters of the Error Management Logic (EML) are unchanged. Setting the MCAN_CCCR.INIT bit does not change any configuration register. Resetting the MCAN_CCCR.INIT bit finishes the software initialization. After waiting for the occurrence of a sequence of 11 consecutive recessive bits (indication for Bus_Idle state) the message transfer starts.

Access to the MCAN configuration registers is only enabled when both MCAN_CCCR.INIT and MCAN_CCCR.CCE bits are set (write protection).

The MCAN_CCCR.CCE bit can only be set/reset while the MCAN_CCCR.INIT = 1. The MCAN_CCCR.CCE bit is automatically reset when the MCAN_CCCR.INIT bit is reset.

The following registers are reset when the MCAN_CCCR.CCE bit is set:

- MCAN_HPMS - High Priority Message Status
- MCAN_RXF0S - Rx FIFO 0 Status
- MCAN_RFX1S - Rx FIFO 1 Status
- MCAN_TXFQS - Tx FIFO/Queue Status
- MCAN_TXBRP - Tx Buffer Request Pending
- MCAN_TXBTO - Tx Buffer Transmission Occurred
- MCAN_TXBCF - Tx Buffer Cancellation Finished
- MCAN_TXEFS - Tx Event FIFO Status

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The Timeout Counter value MCAN_TOCV.TOC field is preset to the value configured by the MCAN_TOCC.TOP field when the MCAN_CCCR.CCE bit is set.

In addition, the Tx Handler and Rx Handler are held in idle state while MCAN_CCCR.CCE = 1.

The following registers are only writable while MCAN_CCCR.CCE = 0

- MCAN_TXBAR - Tx Buffer Add Request
- MCAN_TXBCR - Tx Buffer Cancellation Request

MCAN_CCCR.TEST and MCAN_CCCR.MON bits can only be set by the Host CPU while MCAN_CCCR.INIT = 1 and MCAN_CCCR.CCE = 1. Both bits are reset at any time. The MCAN_CCCR.DAR bit can only be set/reset while MCAN_CCCR.INIT = 1 and MCAN_CCCR.CCE = 1.

Table 30-4 shows the steps to configure the MCAN module.

Table 30-4. Steps to Configure MCAN Module

Step	Operation	Description	Pseudo Code
1	Initialize MCAN_CCCR	Set MCAN_CCCR.INIT bit and check that the bit has been set	INIT = 1; If INIT ≠ 1, wait until set
2	Unlock protected registers	Set MCAN_CCCR.CCE bit	CCE = 1;
3	Configure CAN mode	Set MCAN_CCCR.FDOE bit to CAN FD	FDOE = 1 for CAN FD FDOE = 0 for Classic CAN
4	Configure Bit Rate Switching	Set MCAN_CCCR.BRSE bit	BRSE = 1 for bit rate switching BRSE = 0 for no bit rate switching
5	Set nominal bit timing 1	Set MCAN_NBTP register	
6	Lock protected registers	Clear MCAN_CCCR.CCE bit	CCE = 0;
7	Return MCAN module to normal operation	Clear MCAN_CCCR.INIT bit and check that the bit has been cleared	INIT = 0; If INIT ≠ 0, wait until cleared

30.4.5 Transmitter Delay Compensation

30.4.5.1 Description

When only one CAN FD node is transmitting and all other nodes are receivers, the length of the bus line has no impact. When transmitting using the TX pin, the MCAN module receives the transmitted data from its CAN transceiver using the RX pin. The received data is delayed. If the transmitter delay is greater than TSEG1 (time segment before sample point), a bit error is detected.

The MCAN module provides a delay compensation mechanism to compensate for the transmitter delay. The compensation mechanism enables transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver. Without transmitter delay compensation the bit rate in the data phase is limited by the transmitter delay.

The mechanism enables configurations where the data bit time is shorter than the transmitter delay (it is described in detail in ISO 11898-1:2015). The transmitter delay compensation is enabled by setting the MCAN_DBTP.TDC bit to 1.

The delayed transmit data is compared against the received data at the Secondary Sample Point (SSP) to check for bit errors during the data phase of transmitting nodes. If a bit error is detected, the transmitter reacts on this bit error at the next following regular sample point. During the arbitration phase, the delay compensation is always disabled.

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the MCAN transmit output TX pin through the transceiver to the receive input RX pin plus the transmitter delay compensation offset configured by the MCAN_TDCR.TDCO field (see Figure 30-6). The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (example: half of the bit time in the data phase). The position of the SSP is rounded down to the next integer number of mtq.

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The actual transmitter delay compensation value can be checked by reading the MCAN_PSR.TDCV field. This field is cleared when the MCAN_CCCR_INIT bit is set and is updated at each transmission of CAN FD frame while the MCAN_DBTP.TDC bit is set.

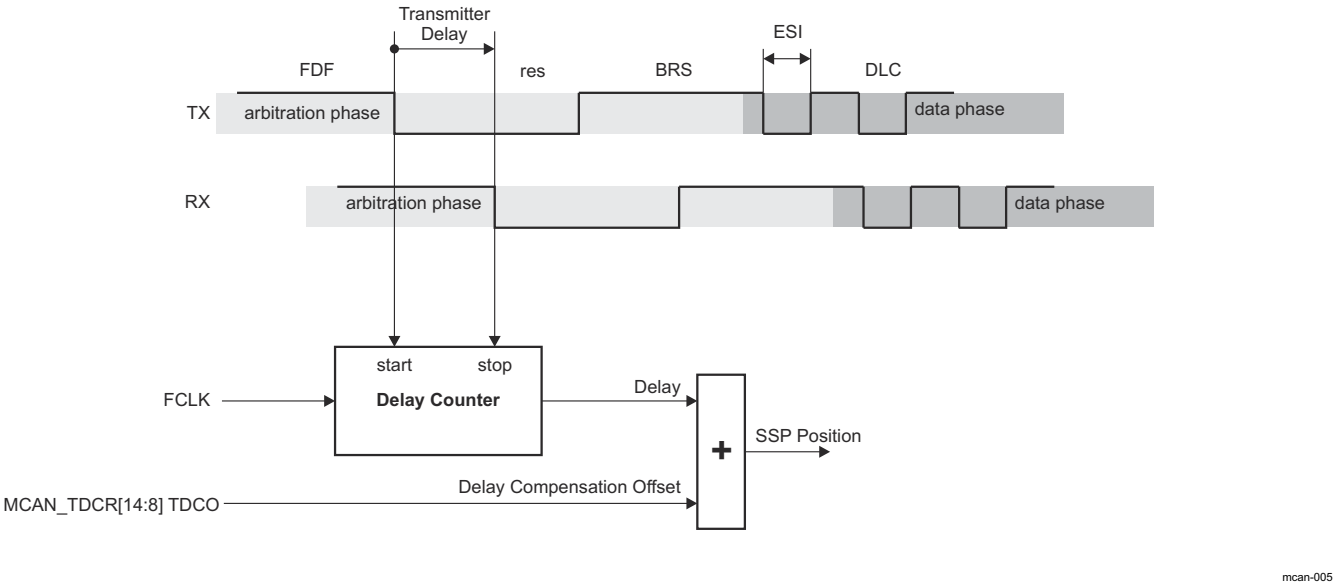


Figure 30-6. Transmitter Delay Measurement

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30.4.5.2 Transmitter Delay Compensation Measurement

When transmitter delay compensation is enabled (by programming MCAN_DBTP.TDC = 1), the measurement is started within each transmitted CAN FD frame at the falling edge of FDF bit to bit r0. The measurement is stopped when this edge is seen at the receive input RX pin of the transmitter. The resolution of this measurement is one mtq (see Section 30.4.5). The mtq (minimum time quantum) dimension is equal to the CAN clock period (MCAN_FCLK).

The use of a transmitter delay compensation filter window can be enabled by programming the MCAN_TDCR.TDCF field. This filter feature defines a minimum value for the SSP position to avoid the case in which a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in an early taken SSP position. Dominant edges on the RX pin that result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR.TDCF field and the RX pin is low.

The following boundary conditions have to be considered:

- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR.TDCO field) has to be less than six bit times in the data phase.
- The sum of the measured delay from the TX pin to the RX pin and the configured transmitter delay compensation offset (MCAN_TDCR.TDCO) field has to be less or equal 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transmitter delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.

30.4.6 Restricted Operation Mode

In restricted operation mode, the CAN node is able to receive data and remote frames and give acknowledgment to valid frames, but the node does not send data frames, remote frames, active error frames, or overload frames. In the case of an error condition or overload condition, the node does not send dominant bits; instead the node waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The receive and transmit error counters (MCAN_ECR.REC and MCAN_ECR.TEC) are frozen while CAN error logging (MCAN_ECR.CEL) is active. The Host CPU can set the MCAN module into Restricted Operation Mode by setting the MCAN_CCCR.ASM bit. The bit can only be set by the Host CPU at any time when both MCAN_CCCR.CCE and MCAN_CCCR.INIT bits are set to 1.

The restricted operation mode is automatically entered when the Tx Handler is not able to read data from the Message RAM in time. To leave restricted operation mode, the Host CPU has to reset the MCAN_CCCR.ASM bit. This mode can be used in applications that adapt themselves to different CAN bit rates. In this case, the application tests different bit rates and leaves the restricted operation mode after the node has received a valid frame.

Note

The Restricted Operation Mode must not be combined with the Loop Back Mode.

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30.4.7 Bus Monitoring Mode

Entering bus monitoring mode is done by setting the MCAN_CCCR.MON bit to 1. In this mode (see ISO 11898-1:2015, *Bus Monitoring* section), the MCAN module is able to receive valid data and remote frames, but cannot start a transmission. The MCAN module sends only recessive bits on the CAN bus. If the MCAN module is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN module monitors this dominant bit, although the CAN bus may remain in recessive state. In bus monitoring mode, the MCAN_TXBRP register is held in reset state. The bus monitoring mode can be used to analyze the traffic on a CAN bus without affecting the bus by the transmission of dominant bits. Figure 30-7 shows the connection of the TX and RX signals to the MCAN module in bus monitoring mode.

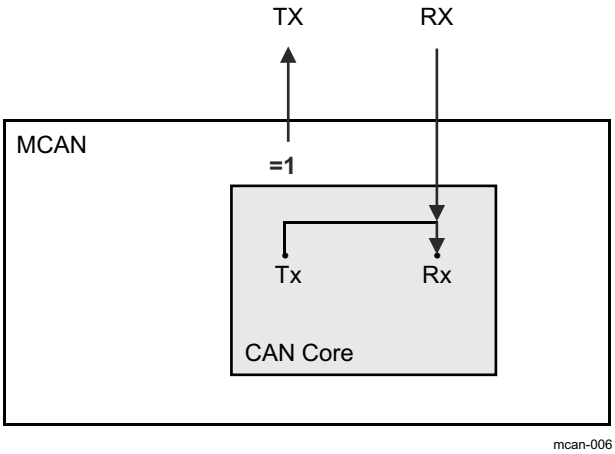


Figure 30-7. Connection of Signals in Bus Monitoring Mode

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30.4.8 Disabled Automatic Retransmission (DAR) Mode

According to the CAN Specification (see ISO11898-1:2015, *Recovery Management* section), the MCAN module provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled (see the MCAN_CCCR.DAR bit).

30.4.8.1 Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically canceled after they have started on the CAN bus. A Tx buffer's Tx Request Pending (MCAN_TXBRP[xx]) TRPx bit is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

Successful transmission:

- Corresponding Tx Buffer Transmission Occurred (MCAN_TXBTO.TOx) TOx bit is set
- Corresponding Tx Buffer Cancellation Finished (MCAN_TXBCF.CFx) CFx bit is not set

Successful transmission in spite of cancellation:

- Corresponding Tx Buffer Transmission Occurred (MCAN_TXBTO.TOx) TOx bit is set
- Corresponding Tx Buffer Cancellation Finished (MCAN_TXBCF.CFx) CFx bit is set

Arbitration lost or frame transmission disturbed:

- Corresponding Tx Buffer Transmission Occurred (MCAN_TXBTO.TOx) TOx bit is not set
- Corresponding Tx Buffer Cancellation Finished (MCAN_TXBCF.CFx) CFx bit is set

In the case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = 10 (transmission in spite of cancellation).

30.4.9 Clock Stop Mode

Entering the clock stop mode can be achieved by programming one of two bits:

- Clock stop request bit in MCAN_IP (MCAN_CCCR.CSR)
- Stop request bit in MCAN_WRAPPER (MCANSS_CLKCTL.STOPREQ)

The register bit within the MCAN_IP (MCAN_CCCR.CSR) reads as 1 as long as the MCAN_WRAPPER bit (MCANSS_CLKCTL.STOPREQ) is asserted.

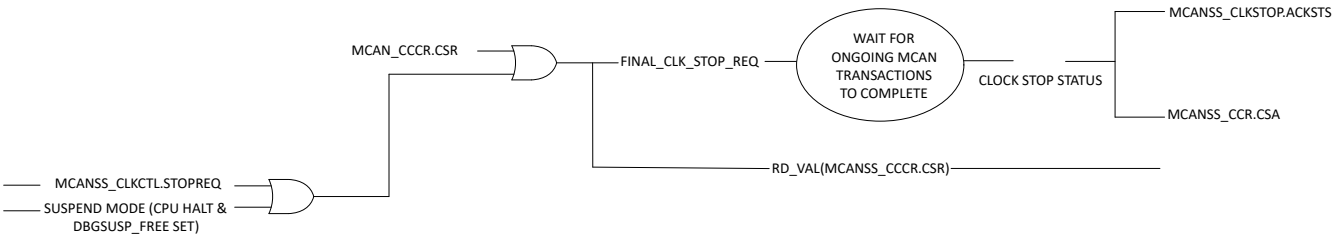


Figure 30-8. Clock Stop Request

After all pending transmission requests have completed, the MCAN module waits until the bus idle state is detected and then sets MCAN_CCCR.INIT to 1 to prevent further CAN transfers. The MCAN module then acknowledges the MCAN is ready for power down by setting the clock stop acknowledge bit MCAN_CCCR.CSA to 1 (MCANSS_CLKSTS.CLKSTOP_ACKSTS reflects the same value as well). In this state, before clocks are switched off, further register accesses can be made. However, a write access to the MCAN_CCCR.INIT bit has no effect. Module clock inputs MCAN_ICLK and MCAN_FCLK can now be switched off using MCANSS_CLKEN.CLK_REQEN.

To exit the power-down mode, the application has to turn on module clocks before clearing the clock stop request bit (make sure both MCAN_CCCR.CSR and MCANSS_CLKCTL.STOPREQ are cleared). MCAN acknowledges removal of the clock request by clearing the MCANSS_CLKSTS.CLKSTOP_ACKSTS

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and MCAN_CCCR.CSA bits. The application can now restart CAN communication by clearing the MCAN_CCCR.INIT bit.

Automatic wakeup from the power-down mode (due to activity on MCAN Rx) is supported through the MCANSS_CTRL.AUTOWAKEUP and MCANSS_CTRL.WAKEUPREQEN bits (for more information, see Section 30.4.9.2).

Clock stop and automatic wakeup is illustrated in Figure 30-8.

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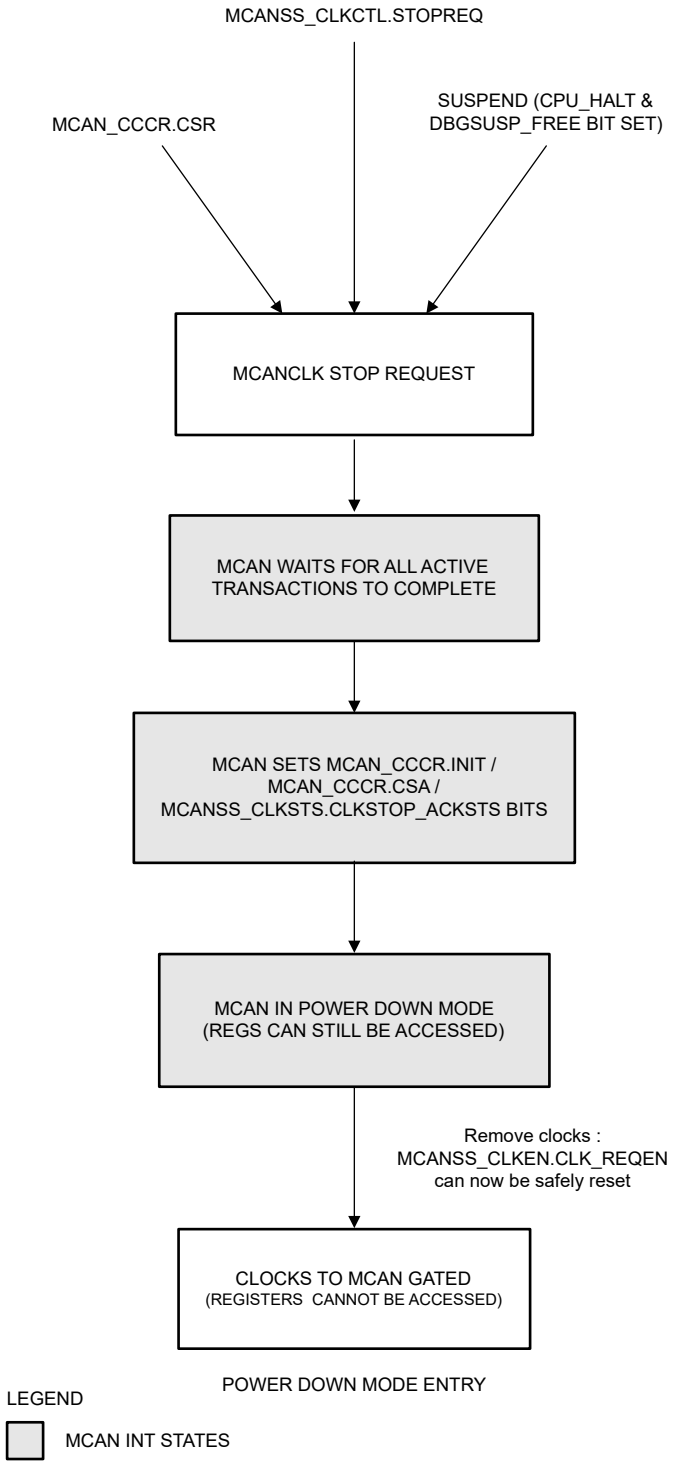


Figure 30-9. Power Down Entry

30.4.9.1 Suspend Mode

The MCAN module supports two suspend modes:

- Immediate
- Graceful

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In a graceful suspend mode (see the MCANSS_CTRL.DBGSUSP_FREE bit) when the suspend request is asserted, a clock stop request to the MCAN core is performed. The MCAN core responds with a clock stop acknowledge when all pending Tx messages have been processed and an Idle line had been detected. At that point, the MCAN_CCCR.INIT bit is set and the MCAN core stays Idle. The suspend state can be verified by reading the MCAN_CCCR.INIT bit.

The automatic wakeup feature is enabled by setting the MCANSS_CTRL.AUTOWAKEUP and MCANSS_CTRL.WAKEUPREQEN bits to 1 (for more information, see Section 30.4.9.2). When suspend request is removed, if no external clock stop request is active, a read-modify-write to the MCAN_CCCR.INIT bit is performed to clear the bit.

During suspend mode the auto-clear feature is disabled. The following register fields have an auto-clear feature:

- MCAN_ECR.CEL
- MCAN_PSR.LEC
- MCAN_PSR.DLEC
- MCAN_PSR.RESI
- MCAN_PSR.RBRS
- MCAN_PSR.RFDF
- MCAN_PSR.PXE

30.4.9.2 Wakeup Request

Issuing a clock stop request puts the MCAN module into power-down mode (Sleep Mode). During transition from IDLE to ACTIVE, if the MCANSS_CTRL.AUTOWAKEUP and MCANSS_CTRL.WAKEUPREQEN bits are enabled, after the MCAN Core respond to the removal of the clock stop request with removing the clock stop acknowledge, a read-modify-write is issued to clear the MCAN_CCCR.INIT bit and the MCAN core resumes operation. Please note that after clock stop request has been removed by the hardware the first frame (wakeup frame) is not received. This is because after the clock stop is issued; there are no active clocks running into the IP. Therefore after removing the clock stop request; the wakeup frame that enables clock has to be re-transmitted.

If the MCANSS_CTRL.WAKEUPREQEN bit is set, the MCAN module provides a wakeup request on the following wakeup event:

- The receive RX pin is dominant (logical 0)

The wakeup request is deasserted when any of the following conditions occur:

- Clock stop request is removed and clock stop acknowledge is deasserted
- A reset is applied to the MCAN module

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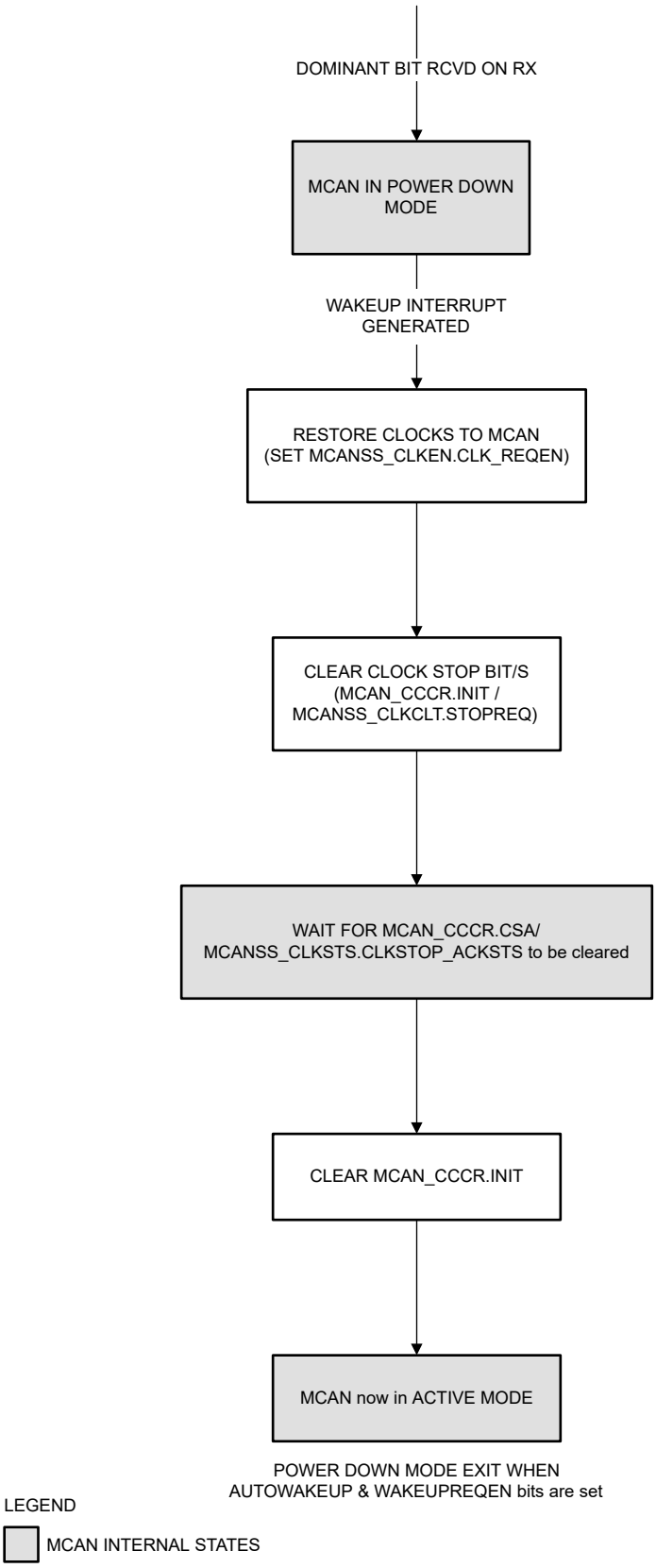


Figure 30-10. Auto Wakeup Enabled Exit from Power Down

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Please note the suggested user notes while issuing a wakeup request.

- If there is a message that is being received on the CAN Bus when a Clock Stop Request (CSR) is issued; it will create a wakeup interrupt at the end of the reception resulting in the MCAN module not entering the clock stop mode. To avoid unnecessary wake ups; the user should check the node activity bit (ACT) in the protocol status register(PSR) ensuring an idle state before setting the request.
- The user should also avoid creating a SW polling loop to only exit with a stop clock acknowledge (CSA) since the timing of the software check and wake up interrupt clearing the CSA could cause an infinite software loop
- If there is excessive noise on the Rx pin, it may cause frequent wake up. To avoid this it is recommended that the user waits for a specified time to see if a wake up was received and if not, assert the clock stop state.
- The wakeup logic can be unexpectedly disabled if MCAN is reset while clock stop request is asserted. Therefore, the user should avoid asserting a soft reset to MCAN while CSR is asserted.

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30.4.10 Test Modes

The MCAN_TEST register write access is enabled by setting the test mode enable MCAN_CCCR.TEST bit to 1. The MCAN_TEST register allows the configuration of the test modes and test functions.

The transmit (TX) pin has four different output functions which can be selected by programming the MCAN_TEST.TX field. The default function is the serial data output. The pin can also be driven with a constant dominant or recessive value. It is also possible to drive the sample-point signal to monitor the bit-timing.

The actual value of the receive (RX) pin can be monitored from MCAN_TEST.RX bit. Both functions can be used to check the physical layer. Due to the synchronization mechanism between the CAN clock (MCANx_FCLK) and Host clock (MCANx_ICLK) domain, there can be a delay of several Host clock periods between writing to the MCAN_TEST.TX field until the new configuration is visible at the output TX pin. This applies also when reading input RX pin by way of the MCAN_TEST.RX bit.

Note

Test modes can be used for self-test only. The software control for TX pin interferes with all CAN protocol functions. It is not recommended to use test modes for an application.

30.4.10.1 External Loop Back Mode

The MCAN module can be set into external loop back mode by programming MCAN_TEST.LBCK to 1. In loop backmode, the MCAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO as shown in below figure. Figure shows the connection of the TX and RX pins to the MCAN module in external loop back mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the MCAN module ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in loop back mode. In this mode, the MCAN module performs an internal feedback from the Tx output to the Rx input. The actual value of the RX input pin is disregarded by the MCAN module. The transmitted messages are monitored at the TX pin.

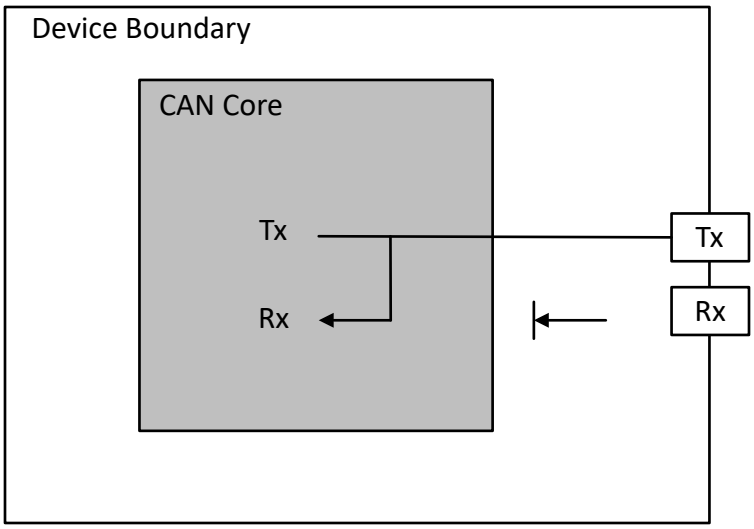


Figure 30-11. External Loop Back Mode

30.4.10.2 Internal Loop Back Mode

The MCAN module can be set into internal loop back mode by programming MCAN_TEST.LBCK and MCAN_CCCR.MON bits to 1. The internal loop back mode is used for a Hot Self-test. The Hot Self-test allows

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the MCAN module to be tested without affecting a running CAN system connected to the TX and RX pins. In this mode, the RX pin is disconnected from the MCAN module and the TX pin is held recessive. Figure 30-12 shows the connection of the TX and RX pins to the MCAN module in internal loop back mode.

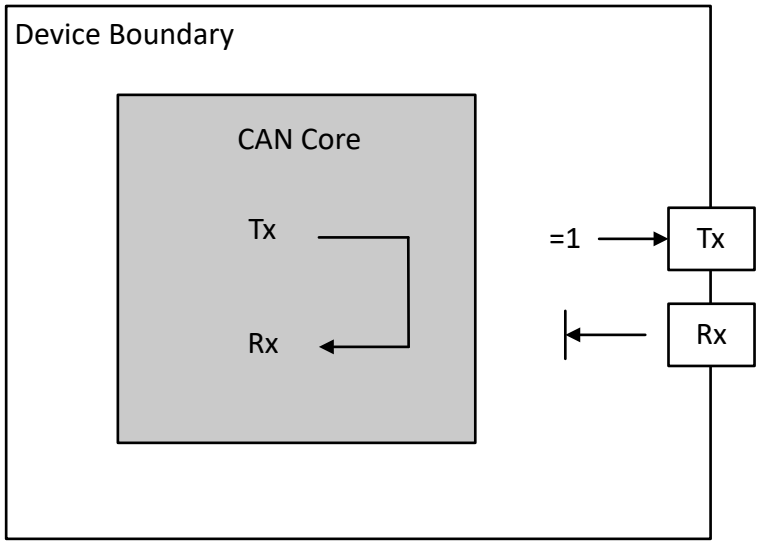


Figure 30-12. Internal Loop Back Mode

30.4.11 Timestamp Generation

The MCAN module has an integrated 16-bit wrap-around counter for timestamp generation. The timestamp counter prescaler MCAN_TSCC.TCP field can be configured to clock the counter in multiples of CAN bit times (1-16). The counter is readable by way of the MCAN_TSCV.TSC field. A write access to the MCAN_TSCV register resets the counter to zero. When the timestamp counter wraps around the interrupt MCAN_IR.TSW flag is set. On start of a frame reception/transmission the counter value is captured and stored into the timestamp section of an Rx Buffer/Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element. For more information regarding FIFO timestamp configuration, see Section 30.4.18 .

30.4.11.1 External Timestamp Counter

For CAN FD operation mode, the MCAN core requires an external timestamp counter. An externally generated 16-bit vector can substitute the integrated 16-bit CAN bit time counter (internal timestamp counter) for receive and transmit timestamp generation. An external 16-bit timestamp counter can be used by programming the MCAN_TSCC.TSS field.

The external timestamp counter uses the interface clock (MCANx_ICLK) as a reference clock. The MCAN core accepts a 16-bit timestamp. A 24-bit prescaler provides a programmable resolution for the timestamp (see MCANSS_EXT_TS_PRESCALER.PRESCALER bit field). The external timestamp counter can be enabled or disabled through the MCANSS_CTRL.EXT_TS_CNTR_EN bit. When disabled, the counter is reset back to zero. While enabled, the counter keeps incrementing. When the timestamp rolls over, the MCAN_IRQ_TS interrupt is generated.

When the timestamp rolls over, the MCANSS_IRS register is set. The MCANSS_IE register can be affected by writing to the MCANSS_IESS register to set or to the MCANSS_IECS register to clear. The MCANSS_IESS register is a shadow register mapped to the same address as the MCANSS_IE register. The level interrupt is a reflection of both MCANSS_IRS and MCANSS_IE being set. The MCANSS_IES register reflects the level interrupt. When a rollover event occurs, the interrupt counter is incremented. Writing to the MCANSS_ICS register to clear the MCANSS_IRS register also decrements the interrupt counter. Writing to the MCANSS_EOI register issues another pulse, if the interrupt counter is not zero.

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The rollover event can be artificially simulated by software through writing to the Interrupt Set Shadow register (MCANSS_ISS). The MCANSS_ISS register is a shadow register mapped to the same address as the MCANSS_IRS register.

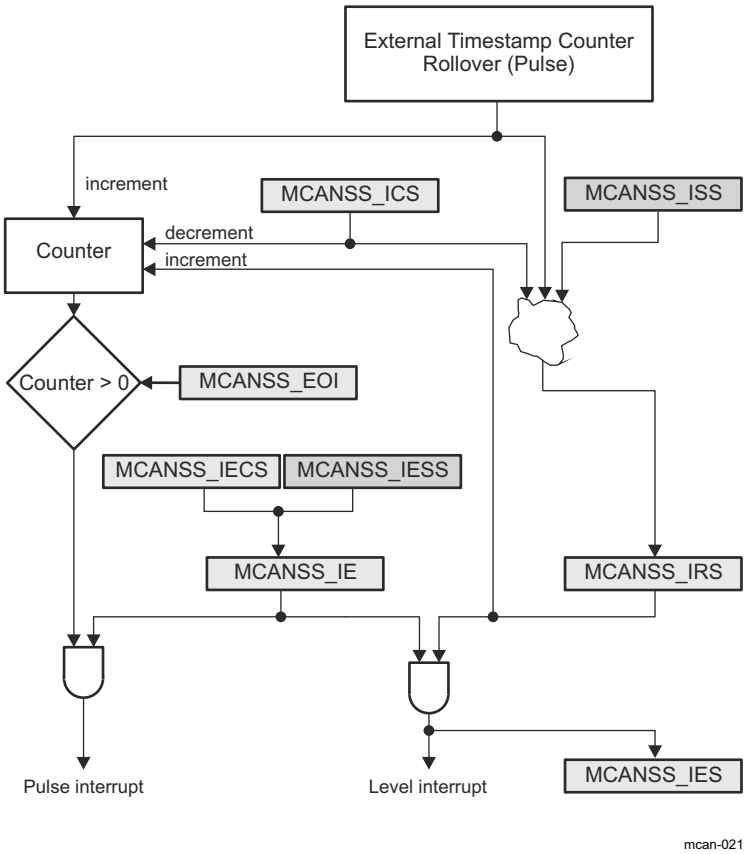


Figure 30-13. External Timestamp Counter Interrupt

30.4.12 Timeout Counter

The MCAN module has an integrated 16-bit timeout counter. The timeout counter is used to signal timeout conditions for the Rx FIFO 0, Rx FIFO 1, and Tx Event FIFO Message RAM elements. The timeout counter is configured using the MCAN_TOCC register and is enabled using the MCAN_TOCC.ETOC bit. The timeout counter operates as down-counter and uses the same prescaler programmed by the MCAN_TSCC.TCP field as the timestamp counter. The actual counter value can be monitored from the MCAN_TOCV.TOC field. The timeout counter can be started only when MCAN_CCCR.INIT = 0 and stopped when MCAN_CCCR.INIT = 1 (example: when the MCAN enters Bus_Off state). The operation mode is selected by the MCAN_TOCC.TOS field. When continuous mode is selected, the counter starts when MCAN_CCCR.INIT = 0, a write to the MCAN_TOCV register presets the counter to the value configured by the MCAN_TOCC.TOP field and continues down-counting.

In case the timeout counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC.TOP field. Down-counting is started when the first FIFO element is stored. Writing to the MCAN_TOCV register has no effect. When the counter reaches zero, the interrupt MCAN_IR.TOO flag is set.

In continuous mode, the counter is immediately restarted at the value configured by the MCAN_TOCC.TOP field.

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Note

The clock signal for the timeout counter is derived from the CAN core sample point signal. Therefore, the point in time where the timeout counter is decremented can vary due to the synchronization/re-synchronization mechanism of the CAN core. If the bit rate switch (BRS) feature in CAN-FD is used, the timeout counter is clocked differently in arbitration and data field.

30.4.13 Safety

The Message RAM (MSG_RAM) is wrapped in an ECC wrapper providing SECDED parity functionality. The MCAN ECC wrapper is controlled by an ECC aggregator.

30.4.13.1 MCAN ECC Wrapper

The ECC wrapper provides single error correction (SEC) and double error detection (DED) parity to the message memory content. The ECC wrapper has side band signals for error notification. The ECC Wrapper implements an error injection test mode.

The error correction is done using a lazy write back. When an error is detected, the error is noted in a FIFO queue that waits for an access gap to write the data back and refresh the memory. If a transaction writes new data to the compromised entry before the lazy write back completes, the write back is discarded.

30.4.13.2 MCAN ECC Aggregator

This section describes the functional details of the MCAN ECC aggregator module.

30.4.13.2.1 MCAN ECC Aggregator Overview

The MCAN ECC aggregator module supports the following general features:

- Provides a mechanism to control and monitor the ECC RAM in the MCAN module.
- Provides software access to all the ECC related registers.
- Supports software readable status of ECC single/double-bit errors and associated info such as RAM address and data bits that are in error.
- Aggregates level pending status from the ECC RAM into a single interrupt to the Host CPU.

The following feature is not supported:

- Statistics such as tracking the number of single and double-bit errors. If needed, these operations can be handled by software.

30.4.13.2.2 MCAN ECC Aggregator Registers

There are three groups of registers in the MCAN ECC aggregator module:

- **Global registers:** Aggregator Revision Register (MCANERR_REV), ECC Vector Register (MCANERR_VECTOR), Misc Status Register (MCANERR_STAT), ECC Control Register (MCANERR_CTRL), and ECC Wrapper Revision Register (MCANERR_WRAP_REV).
- **Control and status registers:** ECC Error Control Registers (MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2) and ECC Error Status Registers (MCANERR_ERR_STAT1, MCANERR_ERR_STAT2, and MCANERR_ERR_STAT3).
- **Interrupt registers:** interrupt status, interrupt enable set, interrupt enable clear, and EOI (End Of Interrupt) registers that are part of a standard interrupt module. For more information, see the following registers:
  - MCANERR_SEC_EOI
  - MCANERR_SEC_STATUS
  - MCANERR_SEC_ENABLE_SET
  - MCANERR_SEC_ENABLE_CLR
  - MCANERR_DED_EOI
  - MCANERR_DED_STATUS
  - MCANERR_DED_ENABLE_SET
  - MCANERR_DED_ENABLE_CLR

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30.4.13.3 Reads to ECC Control and Status Registers

The reads to the ECC control and status registers are triggered by writing a 'read message' to the ECC Vector Register as:

1. Software writes value (the ECC RAM ID) to the MCANERR_VECTOR.ECC_VECTOR field to select the ECC RAM for control or status.
2. Software writes 1 to the MCANERR_VECTOR.RD_SVBUS bit to trigger a read.
3. Software writes read address to the MCANERR_VECTOR.RD_SVBUS_ADDRESS field.
4. Software then polls the MCANERR_VECTOR.RD_SVBUS_DONE bit to check if the bit is 1. This bit indicates that the read operation has completed.
5. Software reads the data from the ECC control or status register. The following clock cycle (MCAN_ICLK) returns the read data.

30.4.13.4 ECC Interrupts

The ECC aggregator module aggregates the level pending status from the ECC RAM into a single EOI-handshake based interrupt to the Host CPU. Software is expected to follow the sequence described:

1. Software enables the interrupts for the ECC RAM by writing to the MCANERR_SEC_ENABLE_SET/ MCANERR_DED_ENABLE_SET register.
2. Software writes the ECC RAM ID in the MCANERR_VECTOR.ECC_VECTOR.
3. Software writes the MCANERR_VECTOR.RD_SVBUS bit to trigger the read.
4. Software writes the MCANERR_ERR_STAT1 register address to the MCANERR_VECTOR.RD_SVBUS_ADDRESS field. Software needs to load the 'read message' in the rMCANERR_VECTOR register again, if the software needs to read the MCANERR_ERR_STAT2 register.
5. Software polls the MCANERR_VECTOR.RD_SVBUS_DONE bit. When this bit is set, a read of the MCANERR_ERR_STAT1/MCANERR_ERR_STAT2 register is performed.
6. After the interrupt has been serviced, software clears the interrupt status by writing to the MCANERR_ERR_STAT1.CLR_ECC_SEC or MCANERR_ERR_STAT1.CLR_ECC_DED bit depending on the type of the ECC error.
7. Software polls the MCANERR_ERR_STAT1 register to verify that the status bit has been cleared.
8. Software writes to the MCANERR_SEC_EOI/MCANERR_DED_EOI register to clear the interrupt.
9. After clearing the ECC interrupt source, the application software must also write 1 to the MCANERR_SEC_EOI.EOI_WR /MCANERR_DED_EOI.EOI_WR bits.

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30.4.14 Tx Handling

The Tx handler is used to handle the Tx requests. It controls the transfer of transmit messages from the dedicated Tx buffers, the Tx FIFO, and the Tx Queue to the CAN Core, the Tx Event FIFO, and the Put and GetIndex operations. The MCAN module supports up to 32 Tx buffers. These Tx buffers can be configured as dedicated Tx buffers, Tx FIFO, or Tx Queue and as combination of dedicated Tx buffers/Tx FIFO or dedicated Tx buffers/Tx Queue. For each Tx Buffer element Classical CAN or CAN FD transmission mode can be configured. Table below shows the possible configurations for message transmission.

Table 30-5. Message Transmission configurations

MCAN_CCCR Register		Buffer Element		Frame Transmission
BRSE	FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	CAN FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	CAN FD without bit rate switching
1	1	1	1	CAN FD with bit rate switching

When the Tx Buffer RequestPending (MCAN_TXBRP) register is updated, or when a transmission has been started the Tx Handler starts scanning to check for the highest priority pending Tx request. The Tx Buffer with the lowest Message ID has highest priority.

Note

AUTOSAR requires at least three Tx Queue buffers and support of transmit cancellation

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30.4.14.1 Transmit Pause

The transmit pause feature is intended for use in CAN networks where the CAN Message IDs are specific and cannot easily be changed. These Message IDs may have a higher priority than other defined Message IDs, while in a specific application their relative priority should be inverse. This allows for a case where one ECU sends a burst of CAN messages that cause CAN messages from another ECU to be delayed (paused).

The transmit pause feature is enabled by the MCAN_CCCR.TXP bit. By default this bit is disabled (MCAN_CCCR.TXP= 0). Each time after successfully transmitted message, a pause for two CAN bit times occurs before the start of the next transmission. This allows the other CAN nodes in the network to transmit messages even if their Message IDs have lower priority.

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30.4.14.2 Dedicated Tx Buffers

Dedicated Tx buffers are intended for message transmission under complete control of the Host CPU. There are two options.

- Each dedicated Tx Buffer is configured with a specific Message ID
- Two or more dedicated Tx buffers are configured with the same Message ID. In this case the Tx Buffer with the lowest buffer number is transmitted first

After the data section has been updated, a transmission is requested by an Add Request. This is done using the MCAN_TXBAR[x]ARn bit (where x = 0 to 31). The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

The following table shows the Tx Buffer, Tx FIFO, and Tx Queue Element Size. A Dedicated Tx Buffer allocates element size 32-bit words in the Message RAM. The start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index from 0 to 31 (MCAN_TXFQS.TFQP) × Element size to the Tx Buffer start address MCAN_TXBC.TBSA field

Table 30-6. Tx Buffer, Tx FIFO, Tx Queue Element Size

MCAN_TXESC.TBDS	DataField [Bytes]	Element Size [RAM Words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

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30.4.14.3 Tx FIFO

Tx FIFO mode is configured by setting bit MCAN_TXBC.TFQM = 0. The data stored in the Tx FIFO messages are transmitted starting with the message referenced by the Get Index MCAN_TXFQS.TFGI field. After each transmission the Get Index is incremented until the Tx FIFO is empty. The Tx FIFO Free Level MCAN_TXFQS.TFFL field indicates the number of the available free Tx FIFO elements. The Tx FIFO allows transmission of messages with the same Message ID from different Tx buffers in the order these messages have been written to the Tx FIFO.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS.TFQP field. After each Add Request (MCAN_TXBAR[x] ARn = 1) the Put Index is incremented to the next free Tx FIFO element. When the Put Index reaches the Get Index (MCAN_TXFQS.TFQP = MCAN_TXFQS.TFGI), Tx FIFO Full condition is signaled by bit MCAN_TXFQS.TFQF = 1. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

The number of requested Tx buffers should not exceed the number of free Tx buffers as indicated by the Tx FIFO Free Level MCAN_TXFQS.TFFL field.

In case a transmission request for the Tx Buffer referenced by the Get Index is canceled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level MCAN_TXFQS.TFFL field is recalculated. In case transmission cancellation is applied to any other Tx Buffer - the Get Index and the FIFO Free Level remain unchanged.

A Tx FIFO element allocates element size 32-bit words in the Message RAM. The start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS.TFQP (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC.TBSA field.

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30.4.14.4 Tx Queue

Tx Queue mode is configured by setting bit MCAN_TXBC.TFQM = 1. The data stored in the Tx Queue messages are transmitted starting with the highest priority message (lowest Message ID). In case two or more Queue buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index MCAN_TXFQS.TFQP field. Each Add Request cyclically increments the Put Index to the next free Tx Buffer. In case of Tx Queue Full condition (MCAN_TXFQS.TFQF = 1), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been canceled.

The application may use the MCAN_TXBRP register instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates element size 32-bit words in the Message RAM. The start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS.TFQP (from 0 to 31) × Element Size to the Tx Buffer Start Address MCAN_TXBC.TBSA field.

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30.4.14.5 Mixed Dedicated Tx Buffers/Tx FIFO

For this combination the Tx buffers section in the Message RAM is separated in two parts:

- Dedicated Tx buffers: the number of dedicated Tx buffers is configured by MCAN_TXBC.NDTB field.
- Tx FIFO: the number of Tx buffers assigned to the Tx FIFO is configured by the MCAN_TXBC.TFQS field. If the MCAN_TXBC.TFQS field is empty(zero)- only dedicated Tx buffers are used.

Tx prioritization:

- Scan Dedicated Tx buffers and oldest pending Tx FIFO Buffer (referenced by the MCAN_TXFQS.TFGI field)
- Buffer with lowest Message ID gets highest priority and is transmitted next
- The following figure shows Mixed Dedicated Tx buffers/Tx FIFO example.

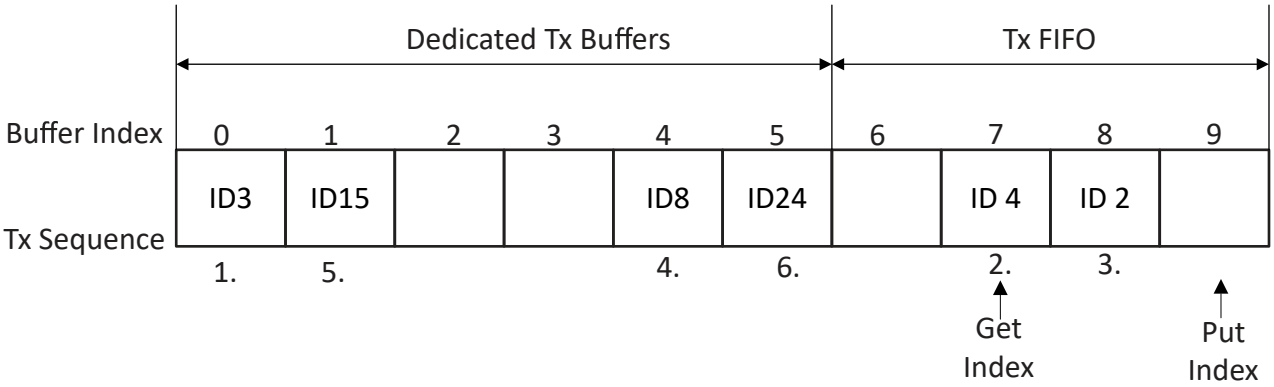


Figure 30-14. Mixed Dedicated Tx Buffers/ Tx FIFO (example)

Note

The SysConfig tool allows for dynamic configuration of MSG_RAM, TX Buffers/FIFO/Queue, and RX Buffers/FIFO/Queue with automatic memory layout/partitioning and auto-generating configuration code. It is strongly recommended to use the SysConfig tool for these configurations.

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30.4.14.6 Mixed Dedicated Tx Buffers/Tx Queue

For this combination the Tx buffers section in the Message RAM is separated in two parts:

- Dedicated Tx buffers: the number of Dedicated Tx buffers is configured by the MCAN_TXBC.NDTB field.
- Tx Queue: the number of Tx buffers assigned to the Tx Queue is configured by the MCAN_TXBC.TFQS field If MCAN_TXBC.TFQS field is empty (zero) - only Dedicated Tx buffers are used.

Tx prioritization:

- Scan all Tx buffers with activated transmission request
- Tx Buffer with lowest Message ID gets highest priority and is transmitted next
- The following figure shows Mixed Dedicated Tx buffers/Tx Queue example.

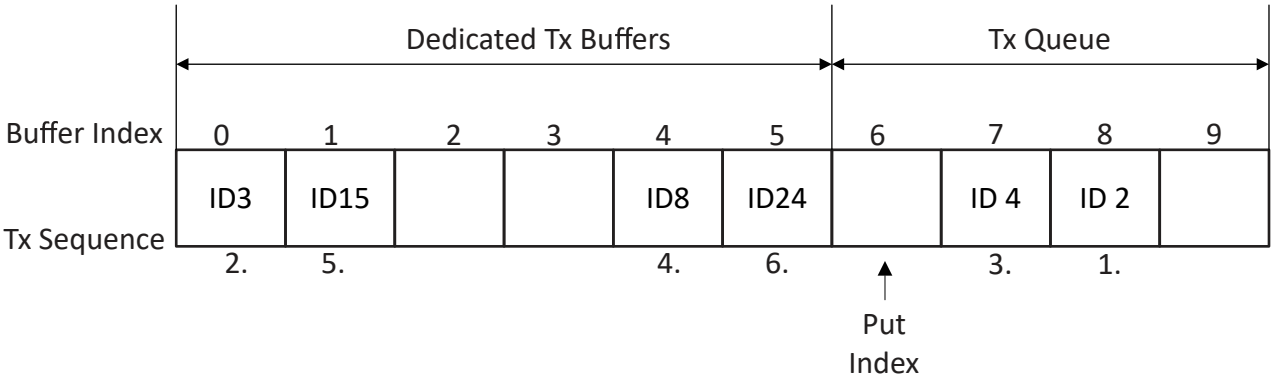


Figure 30-15. Mixed Dedicated Tx Buffers/ Tx FIFO (Example)

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30.4.14.7 Transmit Cancellation

This feature is especially intended for gateway and AUTOSAR based applications. The Host CPU can cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer by setting bit MCAN_TXBCR[n] CRn = 1 (where n = 0 - 31). The corresponding bit position n is equivalent to the number of the Tx buffer.

Transmit cancellation is not intended for Tx FIFO operation.

Successful cancellation is signaled by setting the corresponding bit of the MCAN_TXBCF register (MCAN_TXBCF[n] CFn = 1).

If transmission from a Tx Buffer is already ongoing and a transmit cancellation is requested, the corresponding MCAN_TXBRP[n] TRPn bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding MCAN_TXBTO[n] TOn and MCAN_TXBCF[n] CFn bits are set. If the transmission was not successful, only the corresponding bit MCAN_TXBCF[n] CFn = 1.

Note

If pending transmission is canceled immediately before this transmission could have been started, a short time window occurs where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message that may have a lower priority than the second message in this node.

30.4.14.8 Tx Event Handling

To support Tx Event Handling, the Message RAM has implemented a Tx Event FIFO section. Up to 32 Tx Event FIFO elements can be configured. Section 30.4.18.4 describes the Tx Event FIFO element. After message transmission on the CAN bus, Message ID and Timestamp are stored in a Tx Event FIFO element. To link a Tx Event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

A Tx Event FIFO full condition is signaled by the MCAN_IR.TEFF bit. In this case no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented (MCAN_TXEFS.EFGI). In case a Tx Event occurs while the Tx Event FIFO is full, this event is rejected and interrupt flag MCAN_IR.TEFL bit is set.

The Tx Event FIFO watermark can be configured to avoid a Tx Event FIFO overflow. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by the MCAN_TXEFC.EFWM field, interrupt flag MCAN_IR.TEFW is set. When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index MCAN_TXEFS.EFGI field has to be added to the Tx Event FIFO start address MCAN_TXEFC.EFSA field.

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30.4.14.9 FIFO Acknowledge Handling

The Get Indices of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1) and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (see MCAN_RXF0A, MCAN_RXF1A, and MCAN_TXEFA). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level.

There are two use cases:

- A single element has been read from the FIFO: the Get Index value is written to the FIFO Acknowledge Index.
- A sequence of elements has been read from the FIFO: the Get Index value (Index of the last element read) is written to the FIFO Acknowledge Index at the end of that read sequence.

The Host CPU has free access to the Message RAM. Special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This can be useful when reading a High Priority Message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also changes the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

Note

The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The MCAN module does not check for erroneous values.

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30.4.15 Rx Handling

The Rx Handler controls the following operations:

- Acceptance filtering
- The transfer of received messages to the Rx buffers or to one of the two Rx FIFOs (Rx FIFO 0 or Rx FIFO 1)
- Rx FIFO Put and Get Index operations

30.4.15.1 Acceptance Filtering

The MCAN module employs two sets of acceptance filters - one set for standard and one set for extended identifiers. These filters can be assigned to an Rx Buffer or to one of the two Rx FIFOs.

The main features of the filter elements are:

- Each filter element can be configured as:
  - Range filter (from - to)
  - Filter for specific IDs (for one or two dedicated IDs)
  - Classic bit mask filter
- Each filter element can be enabled/disabled individually
- Each filter element can be configured for acceptance or rejection filtering
- Filters are checked sequentially and execution (acceptance filtering procedure) stops at the first matching filter element or when the end of the filter list is reached

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register
- Extended ID AND Mask (MCAN_XIDAM) register

Depending on the configuration of the filter element (see SFEC/EFEC in Section 30.4.18) if filter matches, one of the following actions is performed:

- Received frame is stored in FIFO 0 or FIFO 1
- Received frame is stored in Rx Buffer
- Received frame is stored in Rx Buffer and generation of pulse at filter event pin is performed. This is high level single MCAN_ICLK pulse.
- Received frame is rejected
- Set High Priority Message interrupt flag MCAN_IR.HPM
- Set High Priority Message interrupt flag MCAN_IR.HPM and store received frame in FIFO 0 or FIFO 1

Acceptance filtering starts when complete Message ID is received. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If a filter element matches - the Rx Handler starts writing the received message data in portions of 32-bit to the matching Rx Buffer or Rx FIFO. If an error condition occurs (for example: CRC error), this message is rejected with the following impact on the affected Rx Buffer or Rx FIFO:

- Rx Buffer: New Data flag (MCAN_NDAT1/MCAN_NDAT2) of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data (for error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC fields,respectively).
- Rx FIFO: Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data (for error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC fields, respectively). If matching Rx FIFO is configured to operate in overwrite mode, the boundary conditions described in Section 30.4.16.2 have to be considered.

Note

When an accepted message is written to one of the two Rx FIFOs, or into an Rx Buffer, the unmodified received identifier is stored independent of the filters used. The result of the acceptance filter process is strongly depending on the sequence of configured filter elements.

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30.4.15.1.1 Range Filter

Each filter element can be configured to operate as Range Filter (Standard Filter Type SFT = 00/Extended Filter Type EFT = 00). The filter matches for all received message frames with IDs in the range from SFID1 to SFID2 (SFID2 ≥ SFID1) respectively in the range from EFID1 to EFID2 (EFID2 ≥ EFID1). For more information see Section 30.4.18.5 and Section 30.4.18.6 .

There are two options for range filtering of extended frames:

- Extended Filter Type EFT = 00: The Extended ID AND Mask (MCAN_XIDAM) is used for Range Filtering. The Message ID of received frames is ANDed with the Extended ID AND Mask (MCAN_XIDAM) before the range filter is applied.
- Extended Filter Type EFT = 11: The Extended ID AND Mask (MCAN_XIDAM) is not used for Range Filtering.

30.4.15.1.2 Filter for Specific IDs

Each filter element can be configured to filter one or two dedicated Message IDs (Standard Filter Type SFT =01/ Extended Filter Type EFT =01). To filter only one specific Message ID, the filter element has to be configured with SFID1 = SFID2 respectively EFID1 = EFID2. For more information, see Section 30.4.18.5 and Section 30.4.18.6 .

30.4.15.1.3 Classic Bit Mask Filter

Classic bit mask filtering can filter groups of Message IDs (Standard Filter Type SFT =10/Extended Filter Type EFT =10). This is done by masking single bits of a received Message ID. In this case SFID1/EFID1 element is used as Message ID filter, while the SFID2/EFID2 element is used as filter mask.

A 0 bit at the filter mask (SFID2/EFID2) masks out the corresponding bit position of the configured Message ID filter (SFID1/EFID1) and the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are 1 are relevant for acceptance filtering.

There are two interesting cases:

- All mask bits are 1: a match occurs only when the received Message ID and the configured Message ID filter are identical.
- All mask bits are 0: all Message IDs match.

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30.4.15.1.4 Standard Message ID Filtering

Section 30.4.18.5 shows the standard Message ID (11-bit ID) filtering flow. Section 30.4.18.6 describes the standard Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Standard ID Filter Configuration (MCAN_SIDFC) register

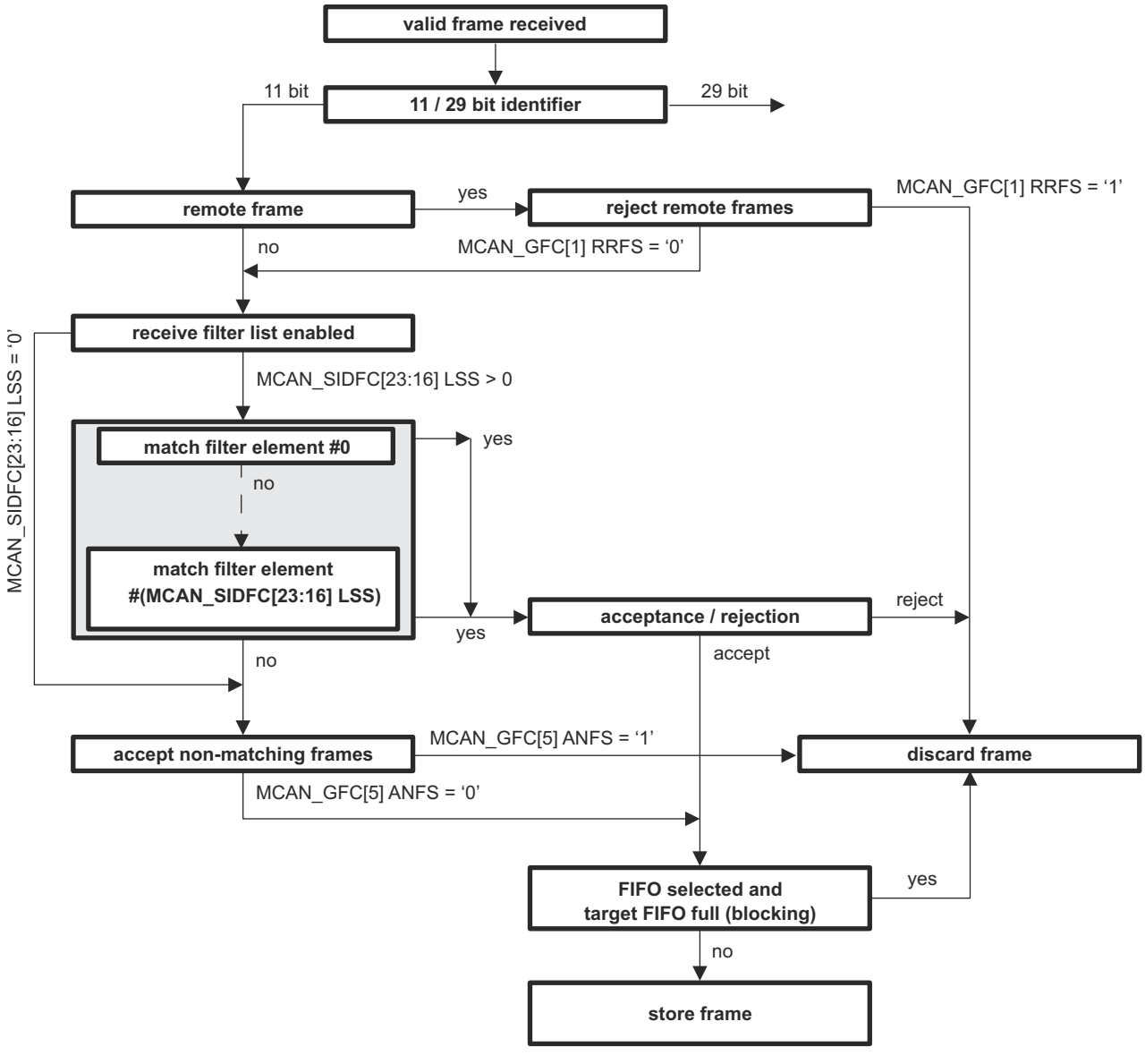


Figure 30-16. Standard Message ID Filter Path

Note

In MCAN_GFC[1]RRFS and MCAN_GFC[5]ANFS; the [1] and [5] denotes the bit position for the RRFS and ANFS bits respectively in the MCAN_GFC register

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30.4.15.1.5 Extended Message ID Filtering

Figure 30-17 shows the extended Message ID (29-bit ID) filtering flow. Section 30.4.18.6 describes the extended Message ID filter element.

The Remote Transmission Request (RTR) and Extended Identifier (XTD) bits of the received frames are compared against the list of configured filter elements. This is controlled by the following registers:

- Global Filter Configuration (MCAN_GFC) register
- Extended ID Filter Configuration (MCAN_XIDFC) register

Note that before the filter list is executed, the received identifier is ANDed with the Extended ID AND Mask (MCAN_XIDAM).

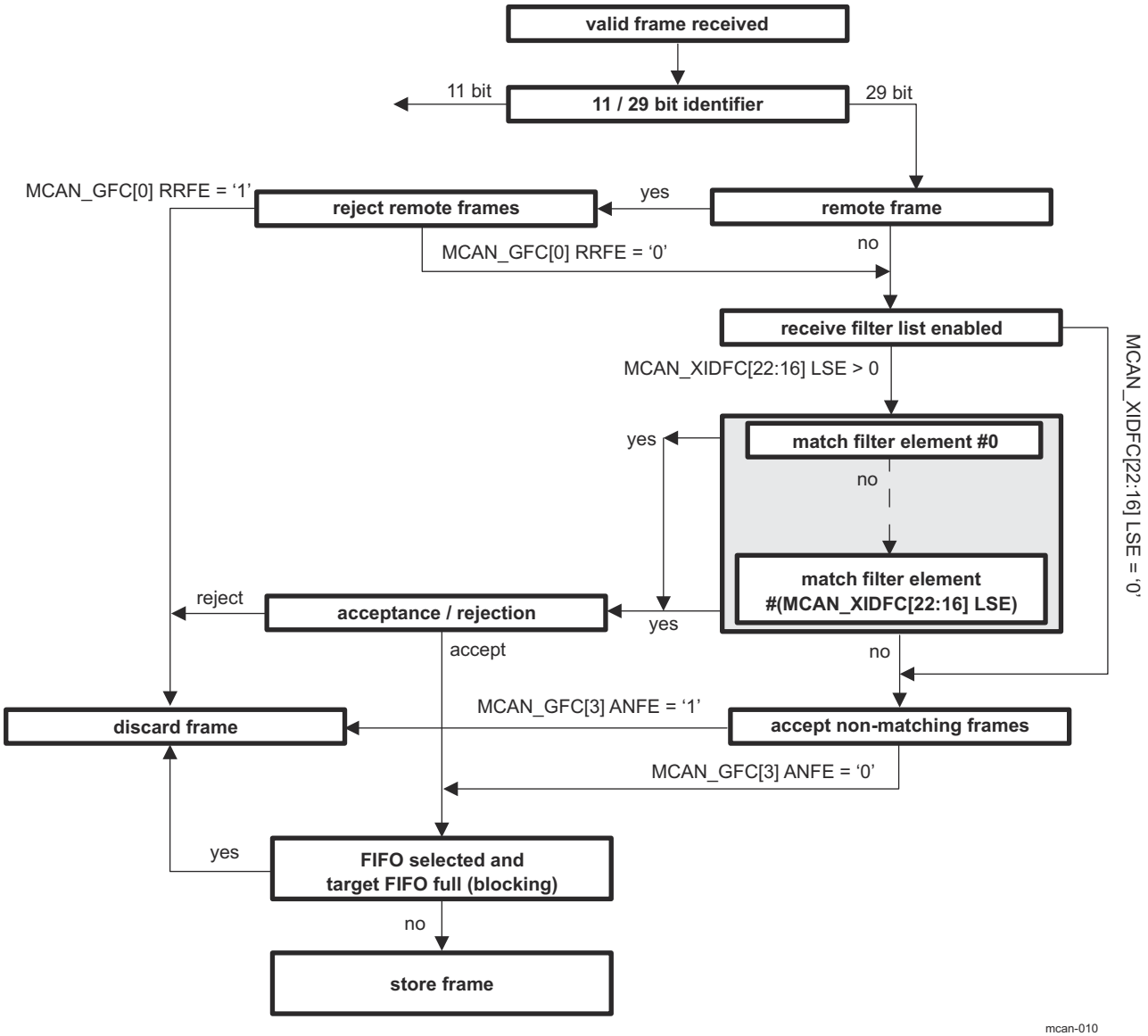


Figure 30-17. Extended Message ID Filter Path

In MCAN_GFC[0]RRFS and MCAN_GFC[3]ANFS; the [0] and [3] denotes the bit position for the RRFS and ANFS bits respectively in the MCAN_GFC register

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30.4.16 Rx FIFOs

The configuration of the Rx FIFOs (Rx FIFO 0 and Rx FIFO 1) can be done by way of the MCAN_RXF0C and MCAN_RXF1C registers. Each Rx FIFO can be configured to store up to 64 received messages.

After acceptance filtering the received messages that passed are transferred to the Rx FIFO. The filter mechanisms available for the Rx FIFO 0 and Rx FIFO 1 are described in Section 30.4.15.1 . The Rx FIFO element is described in Section 30.4.18.2 .

The Rx FIFO watermark can be used to prevent an Rx FIFO overflow. If the Rx FIFO fill level reaches the Rx FIFO watermark configured by the MCAN_RXFnC[30:24] FnWM filed (where: n = 0 or 1), an interrupt flag MCAN_IR.RF0W/MCAN_IR.RF1W is set.

When the Rx FIFO Put Index reaches the Rx FIFO Get Index (MCAN_RXFnS[21:16] FnPI = MCAN_RXFnS[13:8] FnGI), an Rx FIFO Full condition is signaled by the MCAN_RXFnS[24] FnF status bit and interrupt flag MCAN_IR.RF0F/MCAN_IR.RF1F is set. Figure 30-18 shows Rx FIFO Status. The FIFOs fill level is presented in the MCAN_RXFnS[6:0] FnFL field (the number of elements stored in Rx FIFO).

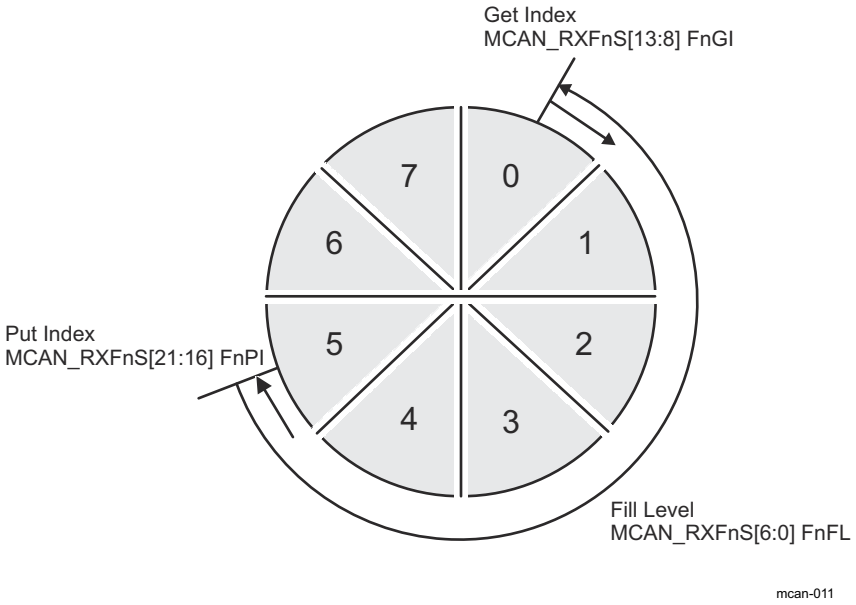


Figure 30-18. Rx FIFO Status

Rx FIFOs start address in the Message RAM (MCAN_RXFnC[15:2]FnSA field) has to be configured when reading from an Rx FIFO (Rx FIFO Get Index - MCAN_RXFnS[13:8] FnGI). Table 30-7 presents Rx Buffer/Rx FIFO Element Size for different Rx Buffer / Rx FIFO Data Field Size which is configured by way of the MCAN_RXESC register.

Table 30-7. Rx Buffer/Rx FIFO Element Size

MCAN_RXESC Register RBDS/F0DS/F1DS Bits	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

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30.4.16.1 Rx FIFO Blocking Mode

The Rx FIFO blocking mode is the default operation mode for the Rx FIFOs and is configured by MCAN_RXFnC[31] FnOM = 0.

If an Rx FIFO full condition is reached (MCAN_RXFnS[21:16] FnPI = MCAN_RXFnS[13:8] FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signaled by the MCAN_RXFnS[24] FnF = 1 and interrupt flag MCAN_IR.RF0F/MCAN_IR.RF1F is set.

In case a message is received while the corresponding Rx FIFO is full, this message is rejected and the message lost condition is signaled by MCAN_RXFnS[25] RFnL = 1 and interrupt flag MCAN_IR.RF0L/ MCAN_IR.RF1L is set.

30.4.16.2 Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by MCAN_RXFnC[31] FnOM = 1. When an Rx FIFO full condition is reached (MCAN_RXFnS[21:16] FnPI = MCAN_RXFnS[13:8] FnGI) signaled by MCAN_RXFnS[24] FnF = 1, the next accepted message for the FIFO overwrites the oldest FIFO message. Put index/Get index are both incremented by one.

In overwrite mode if an Rx FIFO full condition is signaled, reading of the Rx FIFO elements starts at least at get index + 1. The reason for this is a received message is written to the Message RAM (Put index) while the Host CPU is reading from the Message RAM (Get index). In this case, inconsistent data can be read from the respective Rx FIFO element. The problem is solved by adding an offset to the Get index when reading from the Rx FIFO. The offset depends on how fast the Host CPU accesses the Rx FIFO. Figure 30-19 shows an offset of two with respect to the Get index when reading the Rx FIFO. In this case, the two messages stored in element 1 and 2 are lost.

After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index MCAN_RXFnA[5:0] FnAI. This increments the get index to that element number. In case the Put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (MCAN_RXFnS[24] FnF = 0).

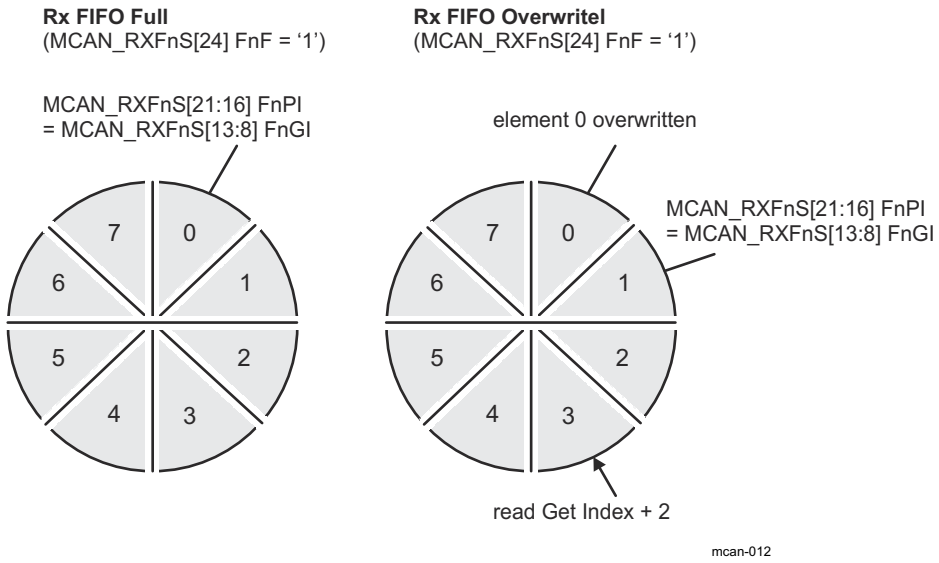


Figure 30-19. Rx FIFO Overflow Handling

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30.4.17 Dedicated Rx Buffers

The MCAN supports up to 64 dedicated Rx buffers. The start address of the Rx buffers section in the Message RAM is configured by way of the MCAN_RXBC.RBSA field. To store in an Rx Buffer a Standard or Extended Message ID Filter Element with SFEC/EFEC = 111 and SFID2/EFID2[10:9] = 00 has to be configured (see Section 30.4.18.5 and Section 30.4.18.6).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element (the format is the same as for an Rx FIFO element). In addition, the flag MCAN_IR.DRX (message stored in Dedicated Rx Buffer) is set.

Table 30-8 shows Example Filter Configuration for Rx buffers.

Table 30-8. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10:0] EFID1[28:0]	SFID2[10:9] EFID2[10:9]	SFID2[5:0] EFID2[5:0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register MCAN_NDAT1/MCAN_NDAT2 is set. As long as the New Data flag is set, the respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the Host CPU by writing a 1 to the respective bit position.

While an Rx buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements can cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message can be rejected, depending on filter configuration.

30.4.17.1 Rx Buffer Handling

Rx Buffer Handling include the following steps:

- Reset interrupt flag MCAN_IR.DRX
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

30.4.18 Message RAM

The MCAN module has a Message RAM. The main purpose of the Message RAM is to store:

- Received Messages
- Transmit Messages
- Tx Event Elements
- Message ID Filter Elements

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30.4.18.1 Message RAM Configuration

The MCAN module can have different Message RAM sizes. The maximum size of the message RAM is 1kB and is offset 0x3FF from the base address. An example of the MCAN module being configured for 1KB size with a width of 32 bits is desribed here.

The Message RAM can include each of the sections listed in Figure 30-20. It is not necessary to configure each of the sections (a section in the Message RAM can be 0) and there is no restriction with respect to the sequence of the sections. For parity checking or ECC, a respective number of bits has to be added to each word. When the MCAN module addresses the Message RAM, it addresses 32-bit words. The start addresses are configurable and they are 32-bit word addresses.

The element size can be configured for:

- Rx FIFO 0, by way of the MCAN_RXESC.F0DS field
- Rx FIFO, 1 by way of the MCAN_RXESC.F1DS field
- Rx buffers, by way of the MCAN_RXESC.RBDS field
- Tx buffers, by way of the MCAN_TXESC.TBDS field

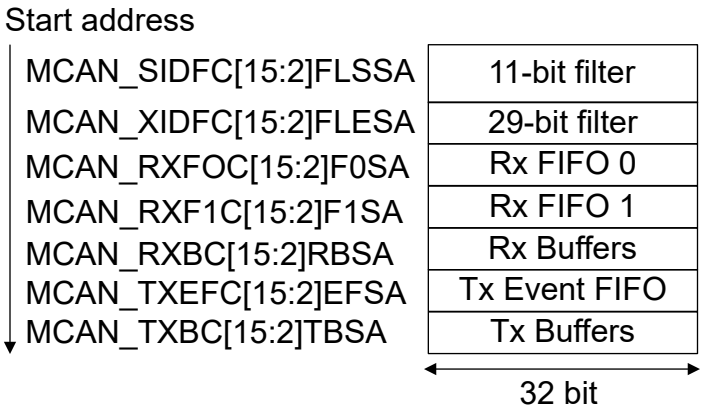


Figure 30-20. Message RAM Configuration

The host CPU configures the following information in the message RAM:

- Start addresses of the memory sections
- Number of elements in each section
- The size of the elements in some sections

Note

The MCAN module does not check for errors in the Message RAM configuration. The configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully. This prevents falsification or loss of data.

An example of the max elements that can be accommodated for each section based on a RAM size of 1kB for the Rx FIFO is provided in Table 30-9 table

Table 30-9. Message Transmission Configurations

Frame Size, DLC Code (Bytes)	Element Size (Words)	Maximum Elements
8	4	64
12	5	51
16	6	43
20	7	37
24	8	32
32	10	26
48	14	18

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Table 30-9. Message Transmission Configurations (continued)

Frame Size, DLC Code (Bytes)	Element Size (Words)	Maximum Elements
64	18	14

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30.4.18.2 Rx Buffer and FIFO Element

Up to 64 Rx buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field by way of the MCAN_RXESC register.

Figure 30-21 shows the Rx Buffer/Rx FIFO element structure. Table 30-10 shows the Rx Buffer/Rx FIFO element field descriptions.

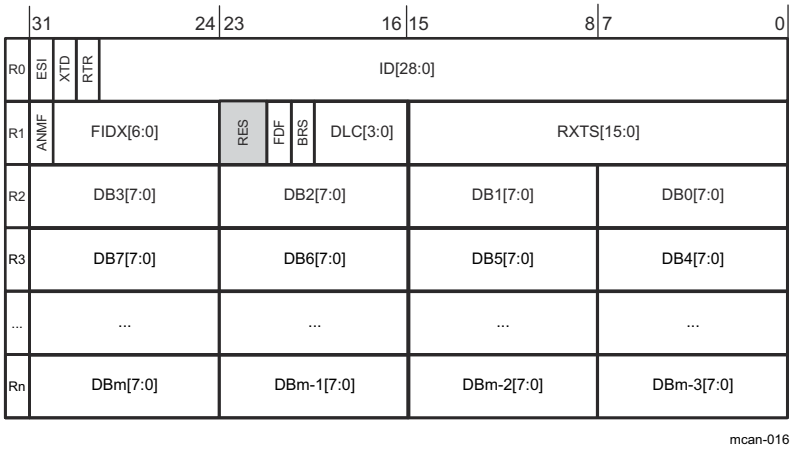


Figure 30-21. Rx Buffer/Rx FIFO Element Structure

Table 30-10. Rx Buffer/Rx FIFO Element Field Descriptions

Word	Bits	Field Name	Description
R0	31	ESI	Error State Indicator • 0x0: Transmitting node is error active • 0x1: Transmitting node is error passive
	30	XTD	Extended Identifier Signals to the Host CPU whether the received frame has a standard or extended identifier. • 0x0: 11-bit standard identifier • 0x1: 29-bit extended identifier
	29	RTR	Remote Transmission Request Signals to the Host CPU whether the received frame is a data frame or a remote frame. • 0x0: Received frame is a data frame • 0x1: Received frame is a remote frame **Note:** There are no remote frames in CAN FD format. In case a CAN FD frame was received (FDF = 1), RTR bit reflects the state of the reserved r1 bit (RES[23]). In CAN FD frames (FDF=1), the dominant RRS (Remote Request Substitution) bit replaces the RTR (Remote Transmission Request) bit.
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier is stored into ID[28:18].

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Table 30-10. Rx Buffer/Rx FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
R1	31	ANMF	Accepted Non-matching Frame Acceptance of non-matching frames can be enabled using the MCAN_GFC.ANFS and MCAN_GFC.ANFE fields. • 0x0: Received frame matching filter index FIDX field • 0x1: Received frame did not match any Rx filter element
	30:24	FIDX[6:0]	Filter Index 0x0-0x7F (0-127): Index of matching Rx acceptance filter element (invalid if ANMF = 1). Range is 0 to MCAN_SIDFC.LSS - 1 respectively MCAN_XIDFC.LSE - 1.
	23:22	RES	Reserved
	21	FDF	FD Format • 0x0: Standard frame format • 0x1: CAN FD frame format (new DLC-coding and CRC)
	20	BRS	Bit Rate Switch • 0x0: Frame received without bit rate switching • 0x1: Frame received with bit rate switching
	19:16	DLC[3:0]	Data Length Code • 0x0-0x8 (0-8): CAN + CAN FD: received frame has 0-8 data bytes • 0x9-0xF (9-15): CAN: received frame has 8 data bytes • 0x9-0xF (9-15): CAN FD: received frame has 12/16/20/24/32/48/64 data bytes
	15:0	RXTS[15:0]	Rx Timestamp Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC.TCP.
R2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0
R3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4
...	...	...	...
Rn	31:24	DBm[7:0]	Data Byte m
	23:16	DBm-1[7:0]	Data Byte m-1
	15:8	DBm-2[7:0]	Data Byte m-2
	7:0	DBm-3[7:0]	Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3-17) are used for storage of a CAN message's data field.

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30.4.18.3 Tx Buffer Element

The Tx buffers section can be configured to hold dedicated Tx buffers as well as a Tx FIFO/Tx Queue. In case that the Tx buffers section is shared by dedicated Tx buffers and a Tx FIFO/Tx Queue, the dedicated Tx buffers start at the beginning of the Tx buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler makes difference between dedicated Tx buffers and Tx FIFO/Tx Queue by way of the MCAN_TXBC.TFQS and MCAN_TXBC.NDTB fields. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field by way of the MCAN_TXESC register.

Figure 30-22 shows the Tx Buffer element structure. Table 30-11 shows the Tx Buffer element field descriptions.

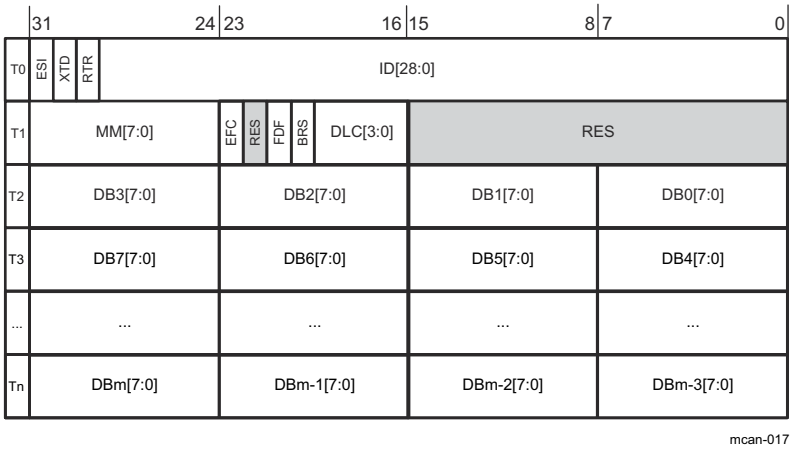


Figure 30-22. Tx Buffer Element Structure

Table 30-11. Tx Buffer Element Field Descriptions

Word	Bits	Field Name	Description
T0	31	ESI	Error State Indicator • 0x0: ESI bit in CAN FD format depends only on error passive flag • 0x1: ESI bit in CAN FD format transmitted recessive **Note:** The ESI bit of the transmit buffer is ORed with the error passive flag to decide the value of the ESI bit in the transmitted CAN FD frame. As required by the CAN FD protocol specification, an error active node can optionally transmit the ESI bit recessive, but an error passive node always transmits the ESI bit recessive.
	30	XTD	Extended Identifier • 0x0: 11-bit standard identifier • 0x1: 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0x0: Transmit data frame • 0x1: Transmit remote frame **Note:** When RTR = 1, the MCAN module transmits a remote frame according to ISO11898-1:2015, even if the MCAN_CCCR.FDOE bit enables the transmission in CAN FD format.
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28:18].

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Table 30-11. Tx Buffer Element Field Descriptions (continued)

Word	Bits	Field Name	Description
T1	31:24	MM[7:0]	Message Marker Written by Host CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status (see also MM[7:0] field in Table 30-11).
	23	EFC	Event FIFO Control • 0x0: Don't store Tx events • 0x1: Store Tx events
	22	RES	Reserved
	21	FDF	FD Format • 0x0: Frame transmitted in Classic CAN format • 0x1: Frame transmitted in CAN FD format
	20	BRS	Bit Rate Switch • 0x0: CAN FD frames transmitted without bit rate switching • 0x1: CAN FD frames transmitted with bit rate switching **Note:** ESI, FDF, and BRS bits are only evaluated when CAN FD operation is enabled using the MCAN_CCCR.FDOE bit. BRS bit is only evaluated when MCAN_CCCR.BRSE = 1.
	19:16	DLC[3:0]	Data Length Code • 0x0-0x8 (0-8): CAN + CAN FD: transmit frame has 0-8 data bytes • 0x9-0xF (9-15): CAN: transmit frame has 8 data bytes • 0x9-0xF (9-15): CAN FD: transmit frame has 12/16/20/24/32/48/64 data bytes
	15:0	RES	Reserved
T2	31:24	DB3[7:0]	Data Byte 3
	23:16	DB2[7:0]	Data Byte 2
	15:8	DB1[7:0]	Data Byte 1
	7:0	DB0[7:0]	Data Byte 0
T3	31:24	DB7[7:0]	Data Byte 7
	23:16	DB6[7:0]	Data Byte 6
	15:8	DB5[7:0]	Data Byte 5
	7:0	DB4[7:0]	Data Byte 4
...	...	...	...
Tn	31:24	DBm[7:0]	Data Byte m
	23:16	DBm-1[7:0]	Data Byte m-1
	15:8	DBm-2[7:0]	Data Byte m-2
	7:0	DBm-3[7:0]	Data Byte m-3

Note

Depending on the configuration of the element size (MCAN_TXESC), between two and sixteen 32-bit words (Tn = 3-17) are used for storage of a CAN message's data field.

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30.4.18.4 Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from the MCAN_TXEFS register.

Figure 30-23 shows the Tx Event FIFO element structure. Table 30-12 shows the Tx Event FIFO element field descriptions.

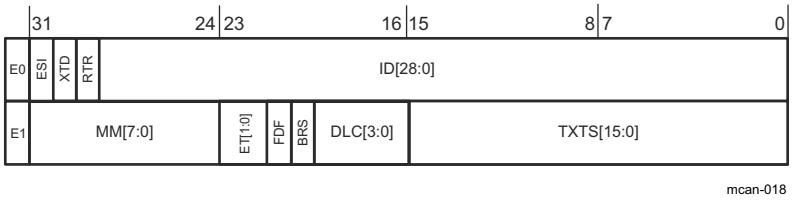


Figure 30-23. Tx Event FIFO Element Structure

Table 30-12. Tx Event FIFO Element Field Descriptions

Word	Bits	Field Name	Description
E0	31	ESI	Error State Indicator • 0x0: Transmitting node is error active • 0x1: Transmitting node is error passive
	30	XTD	Extended Identifier • 0x0: 11-bit standard identifier • 0x1: 29-bit extended identifier
	29	RTR	Remote Transmission Request • 0x0: Data frame transmitted • 0x1: Remote frame transmitted
	28:0	ID[28:0]	Identifier Standard or extended identifier depending on XTD bit. A standard identifier has to be written to ID[28:18].
E1	31:24	MM[7:0]	Message Marker Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status (see also MM[7:0] field in Table 30-12).
	23:22	ET[1:0]	Event Type • 0x0: Reserved • 0x1: Tx event • 0x2: Transmission in spite of cancellation (always set for transmissions in DAR mode) • 0x3: Reserved
	21	FDF	FD Format • 0x0: Standard frame format • 0x1: CAN FD frame format (new DLC-coding and CRC)

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Table 30-12. Tx Event FIFO Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	20	BRS	Bit Rate Switch • 0x0: Frame transmitted without bit rate switching • 0x1: Frame transmitted with bit rate switching
	19:16	DLC[3:0]	Data Length Code • 0x0-0x8 (0-8): CAN + CAN FD: frame with 0-8 data bytes transmitted • 0x9-0xF (9-15): CAN: frame with 8 data bytes transmitted • 0x9-0xF (9-15): CAN FD: frame with 12/16/20/24/32/48/64 data bytes transmitted
	15:0	TXTS[15:0]	Tx Timestamp Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC.TCP filed.

30.4.18.5 Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, the element address is the Filter List Standard Start Address MCAN_SIDFC.FLSSA field plus the index of the filter element (0-127).

Figure 30-24 shows the Standard Message ID Filter element structure. Table 30-13 shows the Standard Message ID Filter element field descriptions.

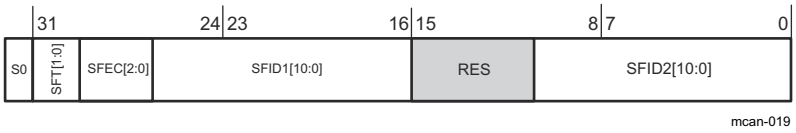


Figure 30-24. Standard Message ID Filter Element Structure

Table 30-13. Standard Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
S0	31:30	SFT[1:0]	Standard Filter Type • 0x0: Range filter from SFID1 to SFID2 (SFID2 ≥ SFID1) • 0x1: Dual ID filter for SFID1 or SFID2 • 0x2: Classic filter: SFID1 = filter; SFID2 = mask • 0x3: Filter element disabled **Note:** With SFT = 11 the filter element is disabled and the acceptance filtering continues (same behavior as with SFEC = 000)

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Table 30-13. Standard Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	29:27	SFEC[2:0]	Standard Filter Element Configuration All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = 100, 101, or 110 match sets interrupt flag MCAN_IR.HPM and, if enabled, an interrupt is generated. In this case, the MCAN_HPMS register is updated with the status of the priority match. • 0x0: Disable filter element • 0x1: Store in Rx FIFO 0 if filter matches • 0x2: Store in Rx FIFO 1 if filter matches • 0x3: Reject ID if filter matches • 0x4: Set priority if filter matches • 0x5: Set priority and store in FIFO 0 if filter matches • 0x6: Set priority and store in FIFO 1 if filter matches • 0x7: Store into Rx Buffer , configuration of SFT[1:0] ignored
	26:16	SFID1[10:0]	Standard Filter ID 1 When filtering for Rx buffers this field defines the ID of a standard message to be stored. The received identifiers must match exactly, no masking mechanism is used.
	15:11	RES	Reserved
	10:0	SFID2[10:0]	Standard Filter ID 2 This bit field has a different meaning depending on the configuration of SFEC: • SFEC = 001 - 110: Second ID of standard ID filter element • SFEC = 111: Filter for Rx buffers
		SFID2[10:9]	This filed is decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0x0: Store message into an Rx Buffer • 0x1: Debug Message A • 0x2: Debug Message B • 0x3: Debug Message C **Note:** Debug feature is not supported.
		SFID2[8:6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only two filter event pins are supported.
		SFID2[5:0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC.RBSA field for storage of a matching message.

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30.4.18.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, the element address is the Filter List Extended Start Address MCAN_XIDFC.FLESA field plus two times the index of the filter element (0-63).

Figure 30-25 shows the Extended Message ID Filter element structure. Table 30-14 shows the Extended Message ID Filter element field descriptions.

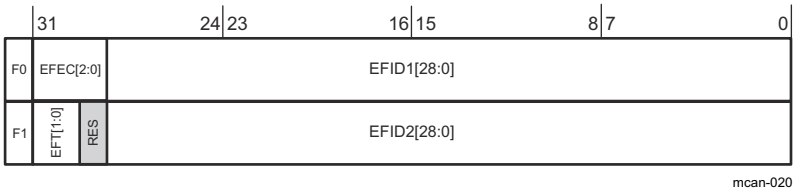


Figure 30-25. Extended Message ID Filter Element Structure

Table 30-14. Extended Message ID Filter Element Field Descriptions

Word	Bits	Field Name	Description
F0	31:29	EFEC[2:0]	Extended Filter Element Configuration All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = 100, 101, or 110 match sets interrupt flag MCAN_IR.HPM and, if enabled, an interrupt is generated. In this case, the MCAN_HPMS register is updated with the status of the priority match. • 0x0: Disable filter element • 0x1: Store in Rx FIFO 0 if filter matches • 0x2: Store in Rx FIFO 1 if filter matches • 0x3: Reject ID if filter matches • 0x4: Set priority if filter matches • 0x5: Set priority and store in FIFO 0 if filter matches • 0x6: Set priority and store in FIFO 1 if filter matches • 0x7: Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored
	28:0	EFID1[28:0]	Extended Filter ID 1 First ID of extended ID filter element. When filtering for Rx buffers this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism (see Table 30-14) is used.
F1	31:30	EFT[1:0]	Extended Filter Type • 0x0: Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1) • 0x1: Dual ID filter for EFID1 or EFID2 • 0x2: Classic filter: EFID1 = filter, EFID2 = mask • 0x3: Range filter from EFID1 to EFID2 (EFID2 ≥ EFID1), XIDAM mask not applied
	29	RES	Reserved

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Table 30-14. Extended Message ID Filter Element Field Descriptions (continued)

Word	Bits	Field Name	Description
	28:0	EFID2[28:0]	Extended Filter ID 2 This bit field has a different meaning depending on the configuration of EFEC: • EFEC = 001 - 110: Second ID of extended ID filter element • EFEC = 111: Filter for Rx buffers
		EFID2[10:9]	This field decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence. • 0x0: Store message into an Rx Buffer • 0x1: Debug Message A • 0x2: Debug Message B • 0x3: Debug Message C **Note:** Debug feature is not supported.
		EFID2[8:6]	This field is used to control the filter event pins at the Extension Interface. A one at the respective bit position enables generation of a pulse at the related filter event pin with the duration of one MCAN_ICKL period in case the filter matches. **Note:** Only two filter event pins are supported.
		EFID2[5:0]	This field defines the offset to the Rx Buffer Start Address MCAN_RXBC.RBSA field for storage of a matching message.

30.5 MCAN Integration

Figure 30-26 shows the integration of the MCAN module in the device.

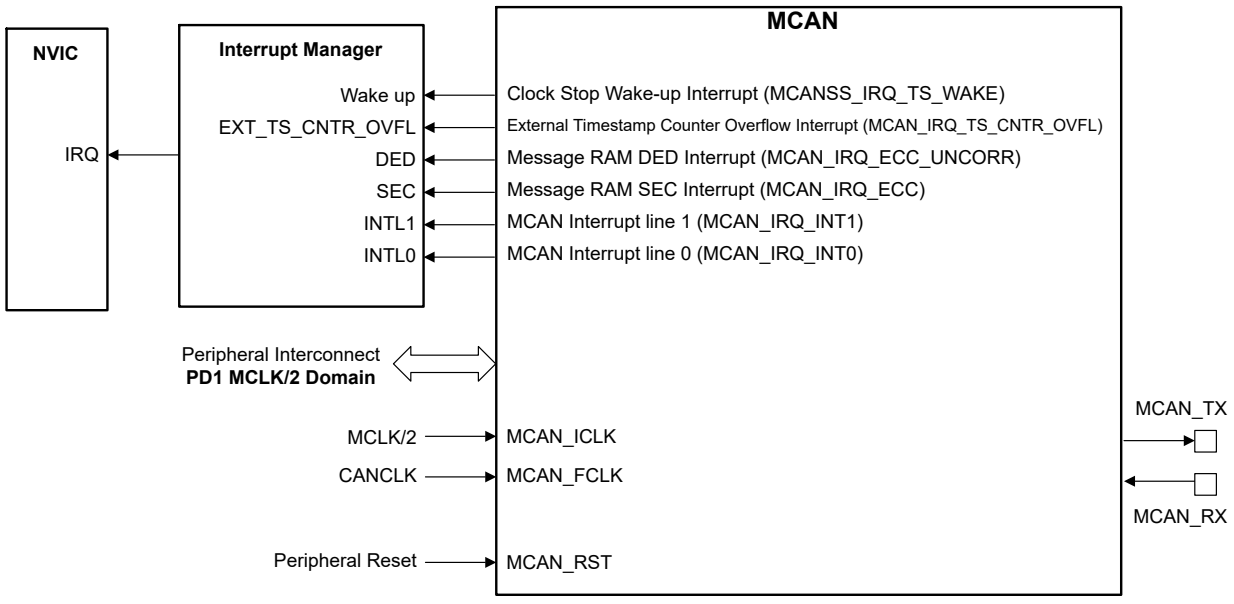


Figure 30-26. MCAN Integration

Table 30-15 summarizes the integration of the MCAN module in the device.

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Table 30-15. MCAN Clocks and Resets

Destination Signal Name	Source Signal Name	Description
Clocks		
MCAN_ICLK	MCLK/2	Interface clock for the MCAN module
MCAN_FCLK	CANCLK	Bit timing clock for MCAN
Resets		
MCAN_RST	Peripheral Reset	Asynchronous reset signal to the MCAN module

Note

For AM13E232x devices, MCLK = 250MHz and the maximum CANCLK speed is 125MHz.

30.6 MCAN Interrupts & Triggers

30.6.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 30-16. CPU Interrupts Triggered by MCAN

NVIC Interrupt Name	Peripheral Instance Name	Register Group	MCAN Interrupt Configuration Registers	Description
MCAN.CPU_INT	MCAN0	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	MCAN0 interrupt. Multiple OR'd, configurable source condition.

30.6.1.1 Interrupt Requests

The MCAN module generates interrupt requests that are configured through the Host CPU. Placing the MCAN module in suspend mode prevents the interrupt requests from propagating to the Host CPU. The MCAN core has two interrupt lines and 30 internal interrupt sources. Each source can be configured to drive one of the two interrupt lines. The interrupts are 'level high' interrupts. The MCAN core provides two interrupt requests (MCANSS_INT0 and MCANSS_INT1).

For more information, see the following registers:

- Interrupt Register (MCAN_IR)
- Interrupt Enable (MCAN_IE)
- Interrupt Line Select (MCAN_ILS)
- Interrupt Line Enable (MCAN_ILE)

The MCAN module supports an External Timestamp Counter. The External Timestamp Counter produces an interrupt when it rolls over (see Section 30.4.11.1).

For more information, see the following registers:

- Interrupt Clear Shadow Register (MCANSS_ICS)
- Interrupt Raw Status Register (MCANSS_IRS)
- Interrupt Enable Clear Shadow Register (MCANSS_IECS)
- Interrupt Enable Register (MCANSS_IE)
- Interrupt Enable Status Register (MCANSS_IES)
- End Of Interrupt Register (MCANSS_EOI)
- External Timestamp Prescaler Register (MCANSS_EXT_TS_PRESCALER)
- External Timestamp Unserviced Interrupts Counter Register (MCANSS_EXT_TS_UNSERVICED_INTR_CNTR)

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To clear IRQ_INT0, IRQ_INT1 and TS_WAKE interrupts, write to the EOI bitfield for the corresponding interrupt number that is described in the MCANSS_EOI register.

After servicing an interrupt (external timestamp, interrupt 0/1), write '1' in the corresponding bit in MCANSS_EOI register to clear the interrupt. In case of an ECC interrupt, after clearing the ECC interrupt source, application software must also write a '1' to the EOI registers (MCANERR_SEC_EOI.EOI_WR/ CANERR_DED_EOI.EOI_WR). For more information see Section 30.4.13.2 .

The IRQ sequence is as follows:

1. Enable one of the interrupt sources by setting corresponding bit in IMASK.
2. Set MCANSS_IE to enable the IRQ, set MCANSS_ILS for line0 or line1.
3. Wait for the interrupt source to be triggered.
4. The interrupt is triggered and the application jumps into IRQ service routine (ISR).
5. In the ISR, check if IRQ is triggered by the expected source by reading IIDX. Reading IIDX clears the IRQ source, so there is no need to write ICLR to clear the IRQ.

   Due to the design of MCAN, step (6) is required in the ISR to clear IRQ. Check the interrupt source to determine if step 7 is needed:
6. Write 1 to MCAN_IR to clear the interrupt.
7. If the source is IRQ_INT0, IRQ_INT1, or TS_WAKE, also clear MCANSS_EOI, otherwise the next IRQ will not be recognized.

30.7 MCAN Registers

This Section describes the MCAN Registers.

30.7.1 MCAN Base Address Table

Table 30-17. MCAN Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Mcan0Regs	MCAN_REGS	MCAN0	0x4011_0000
Mcan1Regs	MCAN_REGS	MCAN1	0x4011_8000

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30.7.2 MCAN_REGS Registers

Table 30-18 lists the memory-mapped registers for the MCAN_REGS registers. All register offset addresses not listed in Table 30-18 should be considered as reserved locations and the register contents should not be modified.

Table 30-18. MCAN_REGS Registers

Offset	Acronym	Register Name	Group	Section
6004h	CANRX	CAN RX IO		Go
6008h	CANTX	CAN TX IO		Go
6204h	CANRX	FUPDATE version of CANRX		Go
6208h	CANTX	FUPDATE version of CANTX		Go
6480h	CPU_CONNECT_0	CPU Connect		Go
6800h	PWREN	Power enable		Go
6804h	RSTCTL	Reset Control		Go
6814h	STAT	Status Register		Go
7000h	MCAN_CREL	MCAN Core Release Register		Go
7004h	MCAN_ENDN	MCAN Endian Register		Go
700Ch	MCAN_DBTP	MCAN Data Bit Timing and Prescaler Register		Go
7010h	MCAN_TEST	MCAN Test Register		Go
7014h	MCAN_RWD	MCAN RAM Watchdog		Go
7018h	MCAN_CCCR	MCAN CC Control Register		Go
701Ch	MCAN_NBTP	MCAN Nominal Bit Timing and Prescaler Register		Go
7020h	MCAN_TSCC	MCAN Timestamp Counter Configuration		Go
7024h	MCAN_TSCV	MCAN Timestamp Counter Value		Go
7028h	MCAN_TOCC	MCAN Timeout Counter Configuration		Go
702Ch	MCAN_TOCV	MCAN Timeout Counter Value		Go
7040h	MCAN_ECR	MCAN Error Counter Register		Go
7044h	MCAN_PSR	MCAN Protocol Status Register		Go
7048h	MCAN_TDCR	MCAN Transmitter Delay Compensation Register		Go
7050h	MCAN_IR	MCAN Interrupt Register		Go
7054h	MCAN_IE	MCAN Interrupt Enable		Go
7058h	MCAN_ILS	MCAN Interrupt Line Select		Go
705Ch	MCAN_ILE	MCAN Interrupt Line Enable		Go
7080h	MCAN_GFC	MCAN Global Filter Configuration		Go
7084h	MCAN_SIDFC	MCAN Standard ID Filter Configuration		Go
7088h	MCAN_XIDFC	MCAN Extended ID Filter Configuration		Go
7090h	MCAN_XIDAM	MCAN Extended ID and Mask		Go
7094h	MCAN_HPMS	MCAN High Priority Message Status		Go
7098h	MCAN_NDAT1	MCAN New Data 1		Go
709Ch	MCAN_NDAT2	MCAN New Data 2		Go
70A0h	MCAN_RXF0C	MCAN Rx FIFO 0 Configuration		Go
70A4h	MCAN_RXF0S	MCAN Rx FIFO 0 Status		Go
70A8h	MCAN_RXF0A	MCAN Rx FIFO 0 Acknowledge		Go
70ACh	MCAN_RXBC	MCAN Rx Buffer Configuration		Go
70B0h	MCAN_RXF1C	MCAN Rx FIFO 1 Configuration		Go
70B4h	MCAN_RXF1S	MCAN Rx FIFO 1 Status		Go
70B8h	MCAN_RXF1A	MCAN Rx FIFO 1 Acknowledge		Go

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Table 30-18. MCAN_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
70BCh	MCAN_RXESC	MCAN Rx Buffer / FIFO Element Size Configuration		Go
70C0h	MCAN_TXBC	MCAN Tx Buffer Configuration		Go
70C4h	MCAN_TXFQS	MCAN Tx FIFO / Queue Status		Go
70C8h	MCAN_TXESC	MCAN Tx Buffer Element Size Configuration		Go
70CCh	MCAN_TXBRP	MCAN Tx Buffer Request Pending		Go
70D0h	MCAN_TXBAR	MCAN Tx Buffer Add Request		Go
70D4h	MCAN_TXBCR	MCAN Tx Buffer Cancellation Request		Go
70D8h	MCAN_TXBTO	MCAN Tx Buffer Transmission Occurred		Go
70DCh	MCAN_TXBCF	MCAN Tx Buffer Cancellation Finished		Go
70E0h	MCAN_TXBTIE	MCAN Tx Buffer Transmission Interrupt Enable		Go
70E4h	MCAN_TXBCIE	MCAN Tx Buffer Cancellation Finished Interrupt Enable		Go
70F0h	MCAN_TXEFC	MCAN Tx Event FIFO Configuration		Go
70F4h	MCAN_TXEFS	MCAN Tx Event FIFO Status		Go
70F8h	MCAN_TXEFA	MCAN Tx Event FIFO Acknowledge		Go
7200h	MCANSS_PID	MCAN Subsystem Revision Register		Go
7204h	MCANSS_CTRL	MCAN Subsystem Control Register		Go
7208h	MCANSS_STAT	MCAN Subsystem Status Register		Go
720Ch	MCANSS_ICS	MCAN Subsystem Interrupt Clear Shadow Register		Go
7210h	MCANSS_IRS	MCAN Subsystem Interrupt Raw Satus Register		Go
7214h	MCANSS_IECS	MCAN Subsystem Interrupt Enable Clear Shadow Register		Go
7218h	MCANSS_IE	MCAN Subsystem Interrupt Enable Register		Go
721Ch	MCANSS_IES	MCAN Subsystem Interrupt Enable Status		Go
7220h	MCANSS_EOI	MCAN Subsystem End of Interrupt		Go
7224h	MCANSS_EXT_TS_PRESCALER	MCAN Subsystem External Timestamp Prescaler 0		Go
7228h	MCANSS_EXT_TS_UNSERVICED_INTR_CNTR	MCAN Subsystem External Timestamp Unserviced Interrupts Counter		Go
7400h	MCANERR_REV	MCAN Error Aggregator Revision Register		Go
7408h	MCANERR_VECTOR	MCAN ECC Vector Register		Go
740Ch	MCANERR_STAT	MCAN Error Misc Status		Go
7410h	MCANERR_WRAP_REV	MCAN ECC Wrapper Revision Register		Go
7414h	MCANERR_CTRL	MCAN ECC Control		Go
7418h	MCANERR_ERR_CTRL1	MCAN ECC Error Control 1 Register		Go
741Ch	MCANERR_ERR_CTRL2	MCAN ECC Error Control 2 Register		Go
7420h	MCANERR_ERR_STAT1	MCAN ECC Error Status 1 Register		Go
7424h	MCANERR_ERR_STAT2	MCAN ECC Error Status 2 Register		Go
7428h	MCANERR_ERR_STAT3	MCAN ECC Error Status 3 Register		Go
743Ch	MCANERR_SEC_EOI	MCAN Single Error Corrected End of Interrupt Register		Go
7440h	MCANERR_SEC_STATUS	MCAN Single Error Corrected Interrupt Status Register		Go
7480h	MCANERR_SEC_ENABLE_SET	MCAN Single Error Corrected Interrupt Enable Set Register		Go

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Table 30-18. MCAN_REGS Registers (continued)

Offset	Acronym	Register Name	Group	Section
74C0h	MCANERR_SEC_ENABLE_CLR	MCAN Single Error Corrected Interrupt Enable Clear Register		Go
753Ch	MCANERR_DED_EOI	MCAN Double Error Detected End of Interrupt Register		Go
7540h	MCANERR_DED_STATUS	MCAN Double Error Detected Interrupt Status Register		Go
7580h	MCANERR_DED_ENABLE_SET	MCAN Double Error Detected Interrupt Enable Set Register		Go
75C0h	MCANERR_DED_ENABLE_CLR	MCAN Double Error Detected Interrupt Enable Clear Register		Go
7600h	MCANERR_AGGR_ENABLE_SET	MCAN Error Aggregator Enable Set Register		Go
7604h	MCANERR_AGGR_ENABLE_CLR	MCAN Error Aggregator Enable Clear Register		Go
7608h	MCANERR_AGGR_STATUS_SET	MCAN Error Aggregator Status Set Register		Go
760Ch	MCANERR_AGGR_STATUS_CLR	MCAN Error Aggregator Status Clear Register		Go
7820h	IIDX	Interrupt Index Register	CPU_INT	Go
7828h	IMASK	Interrupt mask	CPU_INT	Go
7830h	RIS	Raw interrupt status	CPU_INT	Go
7838h	MIS	Masked interrupt status	CPU_INT	Go
7840h	ISET	Interrupt set	CPU_INT	Go
7848h	ICLR	Interrupt clear	CPU_INT	Go
78E0h	EVT_MODE	Event Mode		Go
78FCh	DESC	Module Description		Go
7900h	MCANSS_CLKEN	MCAN module clock enable		Go
7904h	MCANSS_CLKDIV	Clock divider		Go
7908h	MCANSS_CLKCTL	MCAN-SS clock stop control register		Go
790Ch	MCANSS_CLKSTS	MCANSS clock stop status register		Go

Complex bit access types are encoded to fit into small table cells. Table 30-19 shows the codes that are used for access types in this section.

Table 30-19. MCAN_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
RC	R C	Read to Clear
RS	R S	Read to Set
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
W1S	W 1S	Write 1 to set
W1SQ	W 1S Q	Write 1 to set Qualified. A condition must be met for this operation to occur.

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Table 30-19. MCAN_REGS Access Type Codes (continued)

Access Type	Code	Description
WD	W D	Write Decrement. Decrements the specified bit field by the amount written.
WI	W I	Write Increment. Increments the specified bit field by the amount written.
WK	W K	Write Write protected by a key
WQ	W Q	Write Qualified. A condition must be met for this operation to occur.
Reset or Default Value		
-n		Value after reset or the default value

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1 CANRX Register (Offset = 6004h) [Reset = 00000000h]

CANRX is shown in Figure 30-27 and described in Table 30-20.

Return to the Summary Table.

CAN RX IO

Figure 30-27. CANRX Register

31	30	29	28	27	26	25	24
RESERVED	GFLT	SLEW	WCOMP	WUEN	INV	HIGHZ1	HIGHZ0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	DRV			HYSTEN	INENA	PIPU	PIPD
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
GSTATE		RESERVED					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
PSTATE		RESERVED					
R/W-0h		R/W-0h					

Table 30-21. CANRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	GFLT	R/W	0h	Glitch Filter Enable 0h = No internal glitch filter 1h = Use internal glitch filter
29	SLEW	R/W	0h	Reserved Slew Rate Control 0h = No Slew Rate Control 1h = Use Slew Rate Control
28	WCOMP	R/W	0h	Wake up compare value 0h = Match 0 will wake 1h = Match 1 will wake
27	WUEN	R/W	0h	Wake up enable 0h = Wake up not enabled 1h = Wake up enabled
26	INV	R/W	0h	Invert digital input/output relative to peripheral/GPIO 0h = Input and output are non-inverted 1h = Input and output are inverted
25	HIGHZ1	R/W	0h	High-Z instead of high output 0h = Pin can be driven high 1h = Pin is tri-stated instead of driven high
24	HIGHZ0	R/W	0h	High-Z instead of low output 0h = Pin can be driven low 1h = Pin is tri-stated instead of driven low
23	RESERVED	R/W	0h	
22-20	DRV	R/W	0h	Drive strength options 0h = Lowest drive strength 1h = Drive strength 2/8 2h = Drive strength 3/8 3h = Drive strength 4/8 4h = Drive strength 5/8 5h = Drive strength 6/8 6h = Drive strength 7/8 7h = Highest drive strength

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Table 30-21. CANRX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	HYSTEN	R/W	0h	Hysteresis enable 0h = No hysteresis 1h = Hysteresis on
18	INENA	R/W	0h	Input enable 0h = Inputs 0 to connected core 1h = Inputs IO pad value to connected core
17	PIPU	R/W	0h	Pull up enable 0h = No pull up 1h = Pull up
16	PIPD	R/W	0h	Pull down enable 0h = No pull down 1h = Pull down
15-14	GSTATE	R/W	0h	GPIO Channel State 0h = G-Channel is in Unassigned State 1h = G-Channel is in Handover State 2h = G-Channel is in Connected State and not Locked (That is F field is allowed to change without going back through Unassigned state) 3h = G-Channel is in Connected State and Locked (That is F field is not allowed to change to a different non-Zero value until both G and P channels go to Unassigned)
13-8	RESERVED	R/W	0h	
7-6	PSTATE	R/W	0h	Peripheral-Analog Channel State 0h = P-Channel is in Unassigned State 1h = P-Channel is in Handover State 2h = P-Channel is in Connected State and not Locked (That is F field is allowed to change without going back through Unassigned state) 3h = P-Channel is in Connected State and Locked (That is F field is not allowed to change to a different non-Zero value until both G and P channels go to Unassigned)
5-0	RESERVED	R/W	0h	

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2 CANTX Register (Offset = 6008h) [Reset = 00000000h]

CANTX is shown in Figure 30-28 and described in Table 30-21.

Return to the Summary Table.

CAN TX IO

Figure 30-28. CANTX Register

31	30	29	28	27	26	25	24
RESERVED	GFLT	SLEW	WCOMP	WUEN	INV	HIGHZ1	HIGHZ0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	DRV			HYSTEN	INENA	PIPU	PIPD
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
GSTATE		RESERVED					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
PSTATE		RESERVED					
R/W-0h		R/W-0h					

Table 30-23. CANTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	GFLT	R/W	0h	Glitch Filter Enable 0h = No internal glitch filter 1h = Use internal glitch filter
29	SLEW	R/W	0h	Reserved Slew Rate Control 0h = No Slew Rate Control 1h = Use Slew Rate Control
28	WCOMP	R/W	0h	Wake up compare value 0h = Match 0 will wake 1h = Match 1 will wake
27	WUEN	R/W	0h	Wake up enable 0h = Wake up not enabled 1h = Wake up enabled
26	INV	R/W	0h	Invert digital input/output relative to peripheral/GPIO 0h = Input and output are non-inverted 1h = Input and output are inverted
25	HIGHZ1	R/W	0h	High-Z instead of high output 0h = Pin can be driven high 1h = Pin is tri-stated instead of driven high
24	HIGHZ0	R/W	0h	High-Z instead of low output 0h = Pin can be driven low 1h = Pin is tri-stated instead of driven low
23	RESERVED	R/W	0h	
22-20	DRV	R/W	0h	Drive strength options 0h = Lowest drive strength 1h = Drive strength 2/8 2h = Drive strength 3/8 3h = Drive strength 4/8 4h = Drive strength 5/8 5h = Drive strength 6/8 6h = Drive strength 7/8 7h = Highest drive strength

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Table 30-23. CANTX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	HYSTEN	R/W	0h	Hysteresis enable 0h = No hysteresis 1h = Hysteresis on
18	INENA	R/W	0h	Input enable 0h = Inputs 0 to connected core 1h = Inputs IO pad value to connected core
17	PIPU	R/W	0h	Pull up enable 0h = No pull up 1h = Pull up
16	PIPD	R/W	0h	Pull down enable 0h = No pull down 1h = Pull down
15-14	GSTATE	R/W	0h	GPIO Channel State 0h = G-Channel is in Unassigned State 1h = G-Channel is in Handover State 2h = G-Channel is in Connected State and not Locked (That is F field is allowed to change without going back through Unassigned state) 3h = G-Channel is in Connected State and Locked (That is F field is not allowed to change to a different non-Zero value until both G and P channels go to Unassigned)
13-8	RESERVED	R/W	0h	
7-6	PSTATE	R/W	0h	Peripheral-Analog Channel State 0h = P-Channel is in Unassigned State 1h = P-Channel is in Handover State 2h = P-Channel is in Connected State and not Locked (That is F field is allowed to change without going back through Unassigned state) 3h = P-Channel is in Connected State and Locked (That is F field is not allowed to change to a different non-Zero value until both G and P channels go to Unassigned)
5-0	RESERVED	R/W	0h	

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3 CANRX Register (Offset = 6204h) [Reset = 00000000h]

CANRX is shown in Figure 30-29 and described in Table 30-22.

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FUPDATE version of CANRX

Figure 30-29. CANRX Register

31	30	29	28	27	26	25	24
RESERVED				IOADDR			
R/W-0h				W-0h			
23	22	21	20	19	18	17	16
IOADDR							
W-0h							
15	14	13	12	11	10	9	8
IOADDR							
W-0h							
7	6	5	4	3	2	1	0
IOADDR						LOCK	GSEL
W-0h						W-0h	W-0h

Table 30-25. CANRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	
27-2	IOADDR	W	0h	IO Address. This is the address that corresponds to the SOC address[27:2] of the module IP instance specific IO signal in the "Full Write" subregion of the pinmux subregion.
1	LOCK	W	0h	Sets lock bit 0h = Writing this value has no effect 1h = Set channel lock bit
0	GSEL	W	0h	GPIO channel Select 0: Select the P-Channel for the F update 1: Select the G-Channel for the F update 0h = Select the P-Channel for the F update 1h = Select the G-Channel for the F update

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4 CANTX Register (Offset = 6208h) [Reset = 00000000h]

CANTX is shown in Figure 30-30 and described in Table 30-23.

Return to the Summary Table.

FUPDATE version of CANTX

Figure 30-30. CANTX Register

31	30	29	28	27	26	25	24
RESERVED				IOADDR			
R/W-0h				W-0h			
23	22	21	20	19	18	17	16
IOADDR							
W-0h							
15	14	13	12	11	10	9	8
IOADDR							
W-0h							
7	6	5	4	3	2	1	0
IOADDR						LOCK	GSEL
W-0h						W-0h	W-0h

Table 30-27. CANTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	
27-2	IOADDR	W	0h	IO Address. This is the address that corresponds to the SOC address[27:2] of the module IP instance specific IO signal in the "Full Write" subregion of the pinmux subregion.
1	LOCK	W	0h	Sets lock bit 0h = Writing this value has no effect 1h = Set channel lock bit
0	GSEL	W	0h	GPIO channel Select 0: Select the P-Channel for the F update 1: Select the G-Channel for the F update 0h = Select the P-Channel for the F update 1h = Select the G-Channel for the F update

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5 CPU_CONNECT_0 Register (Offset = 6480h) [Reset = 00000000h]

CPU_CONNECT_0 is shown in Figure 30-31 and described in Table 30-24.

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Directly connect peripheral publisher port to application processor

Figure 30-31. CPU_CONNECT_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R/W-0h						R/W-0h	R/W-0h

Table 30-29. CPU_CONNECT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	

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6 PWREN Register (Offset = 6800h) [Reset = 00000000h]

PWREN is shown in Figure 30-32 and described in Table 30-25.

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Register to control the power state

Figure 30-32. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 30-31. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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7 RSTCTL Register (Offset = 6804h) [Reset = 00000000h]

RSTCTL is shown in Figure 30-33 and described in Table 30-26.

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Register to control reset assertion and de-assertion

Figure 30-33. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 30-33. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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8 STAT Register (Offset = 6814h) [Reset = 00000000h]

STAT is shown in Figure 30-34 and described in Table 30-27.

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peripheral enable and reset status

Figure 30-34. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 30-35. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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9 MCAN_CREL Register (Offset = 7000h) [Reset = 32380608h]

MCAN_CREL is shown in Figure 30-35 and described in Table 30-28.

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MCAN Core Release Register

Figure 30-35. MCAN_CREL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
R-3h				R-2h				R-3h				R-8h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
R-6h								R-8h							

Table 30-37. MCAN_CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	REL	R	3h	Core Release. One digit, BCD-coded.
27-24	STEP	R	2h	Step of Core Release. One digit, BCD-coded.
23-20	SUBSTEP	R	3h	Sub-Step of Core Release. One digit, BCD-coded.
19-16	YEAR	R	8h	Time Stamp Year. One digit, BCD-coded.
15-8	MON	R	6h	Time Stamp Month. Two digits, BCD-coded.
7-0	DAY	R	8h	Time Stamp Day. Two digits, BCD-coded.

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10 MCAN_ENDN Register (Offset = 7004h) [Reset = 87654321h]

MCAN_ENDN is shown in Figure 30-36 and described in Table 30-29.

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MCAN Endian Register

Figure 30-36. MCAN_ENDN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV																															
R-87654321h																															

Table 30-39. MCAN_ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ETV	R	87654321h	Endianess Test Value. Reading the constant value maintained in this register allows software to determine the endianess of the host CPU.

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11 MCAN_DBTP Register (Offset = 700Ch) [Reset = 00000A33h]

MCAN_DBTP is shown in Figure 30-37 and described in Table 30-30.

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This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 m_can_cclk periods. tq = (DBRP + 1) mtq.
DTSEG1 is the sum of Prop_Seg and Phase_Seg1. DTSEG2 is Phase_Seg2.
Therefore the length of the bit time is (programmed values) (DTSEG1 + DTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq.
The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Figure 30-37. MCAN_DBTP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
TDC	RESERVED			DBRP			
R/WQ-0h	R/W-0h			R/WQ-0h			
15	14	13	12	11	10	9	8
RESERVED			DTSEG1				
R/W-0h			R/WQ-Ah				
7	6	5	4	3	2	1	0
DTSEG2				DSJW			
R/WQ-3h				R/WQ-3h			

Table 30-41. MCAN_DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23	TDC	R/WQ	0h	Transmitter Delay Compensation 0 Transmitter Delay Compensation disabled 1 Transmitter Delay Compensation enabled
22-21	RESERVED	R/W	0h	
20-16	DBRP	R/WQ	0h	Data Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-13	RESERVED	R/W	0h	
12-8	DTSEG1	R/WQ	Ah	Data Time Segment Before Sample Point. Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7-4	DTSEG2	R/WQ	3h	Data Time Segment After Sample Point. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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Table 30-41. MCAN_DBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	DSJW	R/WQ	3h	Data Resynchronization Jump Width. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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12 MCAN_TEST Register (Offset = 7010h) [Reset = 000000X0h]

MCAN_TEST is shown in Figure 30-38 and described in Table 30-31.

Return to the Summary Table.

Write access to the Test Register has to be enabled by setting bit CCCR.TEST to '1'. All Test Register functions are set to their reset values when bit CCCR.TEST is reset.
Loop Back Mode and software control of the internal CAN TX pin are hardware test modes.

Figure 30-38. MCAN_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RX	TX		LBCK	RESERVED			
R-Xh	R/WQ-0h		R/WQ-0h	R/W-0h			

Table 30-43. MCAN_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	RX	R	Xh	Receive Pin. Monitors the actual value of the CAN receive pin. 0h = DOMINANT : The CAN bus is dominant (CAN RX pin = '0') 1h = RECESSIVE : The CAN bus is recessive (CAN RX pin = '1')
6-5	TX	R/WQ	0h	Control of Transmit Pin 00 CAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at CAN TX pin 10 Dominant ('0') level at CAN TX pin 11 Recessive ('1') at CAN TX pin Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	LBCK	R/WQ	0h	Loop Back Mode. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'. 0h = DISABLE : Reset value, Loop Back Mode is disabled 1h = ENABLE : Loop Back Mode is enabled
3-0	RESERVED	R/W	0h	

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13 MCAN_RWD Register (Offset = 7014h) [Reset = 00000000h]

MCAN_RWD is shown in Figure 30-39 and described in Table 30-32.

Return to the Summary Table.

MCAN RAM Watchdog

Figure 30-39. MCAN_RWD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WDV								WDC							
R/W-0h																R-0h								R/WQ-0h							

Table 30-45. MCAN_RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-8	WDV	R	0h	Watchdog Value. Acutal Message RAM Watchdog Counter Value. The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access via the MCAN's Generic Master Interface starts the Message RAM Watchdog Counter with the value configured by the WDC field. The counter is reloaded with WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag MCAN_IR.WDI is set. The RAM Watchdog Counter is clocked by the host (system) clock.
7-0	WDC	R/WQ	0h	Watchdog Configuration. Start value of the Message RAM Watchdog Counter. With the reset value of "00" the counter is disabled. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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14 MCAN_CCCR Register (Offset = 7018h) [Reset = 00000001h]

MCAN_CCCR is shown in Figure 30-40 and described in Table 30-33.

Return to the Summary Table.

MCAN CC Control Register

Figure 30-40. MCAN_CCCR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
NISO	TXP	EFBI	PXHD	RESERVED		BRSE	FDOE
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/W-0h		R/WQ-0h	R/WQ-0h
7	6	5	4	3	2	1	0
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/W1SQ-0h	R/WQ-0h	R/W1SQ-0h	R/W-0h	R-0h	R/W1SQ-0h	R/WQ-0h	R/W-1h

Table 30-47. MCAN_CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	NISO	R/WQ	0h	Non ISO Operation. If this bit is set, the MCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0 CAN FD frame format according to ISO 11898-1:2015 1 CAN FD frame format according to Bosch CAN FD Specification V1.0
14	TXP	R/WQ	0h	Transmit Pause. If this bit is set, the MCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame. 0 Transmit pause disabled 1 Transmit pause enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
13	EFBI	R/WQ	0h	Edge Filtering during Bus Integration 0 Edge filtering disabled 1 Two consecutive dominant tq required to detect an edge for hard synchronization Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
12	PXHD	R/WQ	0h	Protocol Exception Handling Disable 0 Protocol exception handling enabled 1 Protocol exception handling disabled Note: When protocol exception handling is disabled, the MCAN will transmit an error frame when it detects a protocol exception condition. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
11-10	RESERVED	R/W	0h	

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Table 30-47. MCAN_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BRSE	R/WQ	0h	Bit Rate Switch Enable 0 Bit rate switching for transmissions disabled 1 Bit rate switching for transmissions enabled Note: When CAN FD operation is disabled FDOE = '0', BRSE is not evaluated. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
8	FDOE	R/WQ	0h	Flexible Datarate Operation Enable 0 FD operation disabled 1 FD operation enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	TEST	R/W1SQ	0h	Test Mode Enable 0 Normal operation, register TEST holds reset values 1 Test Mode, write access to register TEST enabled Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
6	DAR	R/WQ	0h	Disable Automatic Retransmission 0 Automatic retransmission of messages not transmitted successfully enabled 1 Automatic retransmission disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
5	MON	R/W1SQ	0h	Bus Monitoring Mode. Bit MON can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time. 0 Bus Monitoring Mode is disabled 1 Bus Monitoring Mode is enabled Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
4	CSR	R/W	0h	Clock Stop Request 0 No clock stop is requested 1 Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge 0 No clock stop acknowledged 1 MCAN may be set in power down by stopping the Host and CAN clocks
2	ASM	R/W1SQ	0h	Restricted Operation Mode. Bit ASM can only be set by SW when both CCE and INIT are set to '1'. The bit can be reset by SW at any time. 0 Normal CAN operation 1 Restricted Operation Mode active Qualified Write 1 to Set is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1	CCE	R/WQ	0h	Configuration Change Enable 0 The CPU has no write access to the protected configuration registers 1 The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	INIT	R/W	1h	Initialization 0 Normal Operation 1 Initialization is started Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to INIT can be read back. Therefore the programmer has to assure that the previous value written to INIT has been accepted by reading INIT before setting INIT to a new value.

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15 MCAN_NBTP Register (Offset = 701Ch) [Reset = 06000A03h]

MCAN_NBTP is shown in Figure 30-41 and described in Table 30-34.

Return to the Summary Table.

This register is only writable if bits CCCR.CCE and CCCR.INIT are set. The CAN bit time may be programed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 m_can_cclk periods. tq = (NBRP + 1) mtq.
NTSEG1 is the sum of Prop_Seg and Phase_Seg1. NTSEG2 is Phase_Seg2.
Therefore the length of the bit time is (programmed values) (NTSEG1 + NTSEG2 + 3) tq or (functional values) (Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2) tq.
The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.
Note: With a CAN clock of 8 MHz, the reset value of 0x06000A03 configures the MCAN for a bit rate of 500 kBit/s.

Figure 30-41. MCAN_NBTP Register

31	30	29	28	27	26	25	24
NSJW							NBRP
R/WQ-3h							R/WQ-0h
23	22	21	20	19	18	17	16
NBRP							
R/WQ-0h							
15	14	13	12	11	10	9	8
NTSEG1							
R/WQ-Ah							
7	6	5	4	3	2	1	0
RESERVED	NTSEG2						
R/W-0h	R/WQ-3h						

Table 30-49. MCAN_NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	NSJW	R/WQ	3h	Nominal (Re)Synchronization Jump Width. Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
24-16	NBRP	R/WQ	0h	Nominal Bit Rate Prescaler. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-8	NTSEG1	R/WQ	Ah	Nominal Time Segment Before Sample Point. Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R/W	0h	

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Table 30-49. MCAN_NBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	NTSEG2	R/WQ	3h	Nominal Time Segment After Sample Point. Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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16 MCAN_TSCC Register (Offset = 7020h) [Reset = 00000000h]

MCAN_TSCC is shown in Figure 30-42 and described in Table 30-35.

Return to the Summary Table.

MCAN Timestamp Counter Configuration

Figure 30-42. MCAN_TSCC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												TCP			
R/W-0h												R/WQ-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TSS	
R/W-0h														R/WQ-0h	

Table 30-51. MCAN_TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19-16	TCP	R/WQ	0h	Timestamp Counter Prescaler. Configures the timestamp and timeout counters time unit in multiples of CAN bit times. Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation (TSS = "10"). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	RESERVED	R/W	0h	
1-0	TSS	R/WQ	0h	Timestamp Select 00 Timestamp counter value always 0x0000 01 Timestamp counter value incremented according to TCP 10 External timestamp counter value used 11 Same as "00" Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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17 MCAN_TSCV Register (Offset = 7024h) [Reset = 00000000h]

MCAN_TSCV is shown in Figure 30-43 and described in Table 30-36.

Return to the Summary Table.

MCAN Timestamp Counter Value

Figure 30-43. MCAN_TSCV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TSC															
R/W-0h																R/W-0h															

Table 30-53. MCAN_TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	TSC	R/W	0h	Timestamp Counter. The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = "01", the Timestamp Counter is incremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = "10", TSC reflects the External Timestamp Counter value, and a write access has no impact. Note: A "wrap around" is a change of the Timestamp Counter value from non-zero to zero not caused by write access to MCAN_TSCV.

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18 MCAN_TOCC Register (Offset = 7028h) [Reset = FFFF0000h]

MCAN_TOCC is shown in Figure 30-44 and described in Table 30-37.

Return to the Summary Table.

MCAN Timeout Counter Configuration

Figure 30-44. MCAN_TOCC Register

31	30	29	28	27	26	25	24
TOP							
R/WQ-FFFFh							
23	22	21	20	19	18	17	16
TOP							
R/WQ-FFFFh							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					TOS		ETOC
R/W-0h					R/WQ-0h		R/WQ-0h

Table 30-55. MCAN_TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TOP	R/WQ	FFFFh	Timeout Period. Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-3	RESERVED	R/W	0h	
2-1	TOS	R/WQ	0h	Timeout Select. When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00 Continuous operation 01 Timeout controlled by Tx Event FIFO 10 Timeout controlled by Rx FIFO 0 11 Timeout controlled by Rx FIFO 1 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	ETOC	R/WQ	0h	Enable Timeout Counter 0 Timeout Counter disabled 1 Timeout Counter enabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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19 MCAN_TOCV Register (Offset = 702Ch) [Reset = 0000FFFFh]

MCAN_TOCV is shown in Figure 30-45 and described in Table 30-38.

Return to the Summary Table.

MCAN Timeout Counter Value

Figure 30-45. MCAN_TOCV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TOC															
R/W-0h																R/W-FFFFh															

Table 30-57. MCAN_TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	TOC	R/W	FFFFh	Timeout Counter. The Timeout Counter is decremented in multiples of CAN bit times, (1...16), depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS.

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20 MCAN_ECR Register (Offset = 7040h) [Reset = 00000000h]

MCAN_ECR is shown in Figure 30-46 and described in Table 30-39.

Return to the Summary Table.

MCAN Error Counter Register

Figure 30-46. MCAN_ECR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								CEL							
R-0h								RC-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
R-0h	R-0h							R-0h							

Table 30-59. MCAN_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23-16	CEL	RC	0h	CAN Error Logging. The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF the next increment of TEC or REC sets interrupt flag IR.ELO. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
15	RP	R	0h	Receive Error Passive 0 The Receive Error Counter is below the error passive level of 128 1 The Receive Error Counter has reached the error passive level of 128
14-8	REC	R	0h	Receive Error Counter. Actual state of the Receive Error Counter, values between 0 and 127. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.
7-0	TEC	R	0h	Transmit Error Counter. Actual state of the Transmit Error Counter, values between 0 and 255. Note: When CCCR.ASM is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.

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21 MCAN_PSR Register (Offset = 7044h) [Reset = 00000707h]

MCAN_PSR is shown in Figure 30-47 and described in Table 30-40.

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MCAN Protocol Status Register

Figure 30-47. MCAN_PSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	TDCV						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RESERVED	PXE	RFDF	RBRS	RESI	DLEC		
R-0h	RC-0h	RC-0h	RC-0h	RC-0h	RS-7h		
7	6	5	4	3	2	1	0
BO	EW	EP	ACT		LEC		
R-0h	R-0h	R-0h	R-0h		RS-7h		

Table 30-61. MCAN_PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	
22-16	TDCV	R	0h	Transmitter Delay Compensation Value. Position of the secondary sample point, defined by the sum of the measured delay from the internal CAN TX signal to the internal CAN RX signal and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.
15	RESERVED	R	0h	
14	PXE	RC	0h	Protocol Exception Event 0 No protocol exception event occurred since last read access 1 Protocol exception event occurred
13	RFDF	RC	0h	Received a CAN FD Message. This bit is set independent of acceptance filtering. 0 Since this bit was reset by the CPU, no CAN FD message has been received 1 Message in CAN FD format with FDF flag set has been received
12	RBRS	RC	0h	BRS Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering. 0 Last received CAN FD message did not have its BRS flag set 1 Last received CAN FD message had its BRS flag set
11	RESI	RC	0h	ESI Flag of Last Received CAN FD Message. This bit is set together with RFDF, independent of acceptance filtering. 0 Last received CAN FD message did not have its ESI flag set 1 Last received CAN FD message had its ESI flag set
10-8	DLEC	RS	7h	Data Phase Last Error Code. Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	BO	R	0h	Bus_Off Status 0 The M_CAN is not Bus_Off 1 The M_CAN is in Bus_Off state

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Table 30-61. MCAN_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EW	R	0h	Warning Status 0 Both error counters are below the Error_Warning limit of 96 1 At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive 0 The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1 The M_CAN is in the Error_Passive state
4-3	ACT	R	0h	Node Activity. Monitors the module's CAN communication state. 00 Synchronizing - node is synchronizing on CAN communication 01 Idle - node is neither receiver nor transmitter 10 Receiver - node is operating as receiver 11 Transmitter - node is operating as transmitter Note: ACT is set to "00" by a Protocol Exception Event.
2-0	LEC	RS	7h	Last Error Code. The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0 No Error: No error occurred since LEC has been reset by successful reception or transmission. 1 Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2 Form Error: A fixed format part of a received frame has the wrong format. 3 AckError: The message transmitted by the MCAN was not acknowledged by another node. 4 Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5 Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6 CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7 NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in DLEC instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error. Note: The Bus_Off recovery sequence (see ISO 11898-1:2015) cannot be shortened by setting or resetting CCCR.INIT. If the device goes Bus_Off, it will set CCCR.INIT of its own accord, stopping all bus activities. Once CCCR.INIT has been cleared by the CPU, the device will then wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the Bus_Off recovery sequence, the Error Management Counters will be reset. During the waiting time after the resetting of CCCR.INIT, each time a sequence of 11 recessive bits has been monitored, a Bit0Error code is written to PSR.LEC, enabling the CPU to readily check up whether the CAN bus is stuck at dominant or continuously disturbed and to monitor the Bus_Off recovery sequence. ECR.REC is used to count these sequences.

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22 MCAN_TDCR Register (Offset = 7048h) [Reset = 00000000h]

MCAN_TDCR is shown in Figure 30-48 and described in Table 30-41.

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MCAN Transmitter Delay Compensation Register

Figure 30-48. MCAN_TDCR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	TDCO						
R/W-0h	R/WQ-0h						
7	6	5	4	3	2	1	0
RESERVED	TDCF						
R/W-0h	R/WQ-0h						

Table 30-63. MCAN_TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	0h	
14-8	TDCO	R/WQ	0h	Transmitter Delay Compensation Offset. Offset value defining the distance between the measured delay from the internal CAN TX signal to the internal CAN RX signal and the secondary sample point. Valid values are 0 to 127 mtq. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R/W	0h	
6-0	TDCF	R/WQ	0h	Transmitter Delay Compensation Filter Window Length. Defines the minimum value for the SSP position, dominant edges on the internal CAN RX signal that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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23 MCAN_IR Register (Offset = 7050h) [Reset = 80000000h]

MCAN_IR is shown in Figure 30-49 and described in Table 30-42.

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The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. The configuration of IE controls whether an interrupt is generated. The configuration of ILS controls on which interrupt line an interrupt is signalled.

Figure 30-49. MCAN_IR Register

31	30	29	28	27	26	25	24
RESERVED		ARA	PED	PEA	WDI	BO	EW
R/W-2h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
EP	ELO	BEU	RESERVED	DRX	TOO	MRAF	TSW
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 30-65. MCAN_IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	2h	
29	ARA	R/W1C	0h	Access to Reserved Address 0 No access to reserved address occurred 1 Access to reserved address occurred
28	PED	R/W1C	0h	Protocol Error in Data Phase (Data Bit Time is used) 0 No protocol error in data phase 1 Protocol error in data phase detected (PSR.DLEC ? 0,7)
27	PEA	R/W1C	0h	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0 No protocol error in arbitration phase 1 Protocol error in arbitration phase detected (PSR.LEC ? 0,7)
26	WDI	R/W1C	0h	Watchdog Interrupt 0 No Message RAM Watchdog event occurred 1 Message RAM Watchdog event due to missing READY
25	BO	R/W1C	0h	Bus_Off Status 0 Bus_Off status unchanged 1 Bus_Off status changed
24	EW	R/W1C	0h	Warning Status 0 Error_Warning status unchanged 1 Error_Warning status changed
23	EP	R/W1C	0h	Error Passive 0 Error_Passive status unchanged 1 Error_Passive status changed
22	ELO	R/W1C	0h	Error Logging Overflow 0 CAN Error Logging Counter did not overflow 1 Overflow of CAN Error Logging Counter occurred

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Table 30-65. MCAN_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	BEU	R/W1C	0h	Bit Error Uncorrected. Message RAM bit error detected, uncorrected. This bit is set when a double bit error is detected by the ECC aggregator attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0 No bit error detected when reading from Message RAM 1 Bit error detected, uncorrected (e.g. parity logic)
20	RESERVED	R/W	0h	
19	DRX	R/W1C	0h	Message Stored to Dedicated Rx Buffer. The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0 No Rx Buffer updated 1 At least one received message stored into an Rx Buffer
18	TOO	R/W1C	0h	Timeout Occurred 0 No timeout 1 Timeout reached
17	MRAF	R/W1C	0h	Message RAM Access Failure. The flag is set, when the Rx Handler: - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0 No Message RAM access failure occurred 1 Message RAM access failure occurred
16	TSW	R/W1C	0h	Timestamp Wraparound 0 No timestamp counter wrap-around 1 Timestamp counter wrapped around
15	TEFL	R/W1C	0h	Tx Event FIFO Element Lost 0 No Tx Event FIFO element lost 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero
14	TEFF	R/W1C	0h	Tx Event FIFO Full 0 Tx Event FIFO not full 1 Tx Event FIFO full
13	TEFW	R/W1C	0h	Tx Event FIFO Watermark Reached 0 Tx Event FIFO fill level below watermark 1 Tx Event FIFO fill level reached watermark
12	TEFN	R/W1C	0h	Tx Event FIFO New Entry 0 Tx Event FIFO unchanged 1 Tx Handler wrote Tx Event FIFO element
11	TFE	R/W1C	0h	Tx FIFO Empty 0 Tx FIFO non-empty 1 Tx FIFO empty
10	TCF	R/W1C	0h	Transmission Cancellation Finished 0 No transmission cancellation finished 1 Transmission cancellation finished
9	TC	R/W1C	0h	Transmission Completed 0 No transmission completed 1 Transmission completed

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Table 30-65. MCAN_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HPM	R/W1C	0h	High Priority Message 0 No high priority message received 1 High priority message received
7	RF1L	R/W1C	0h	Rx FIFO 1 Message Lost 0 No Rx FIFO 1 message lost 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero
6	RF1F	R/W1C	0h	Rx FIFO 1 Full 0 Rx FIFO 1 not full 1 Rx FIFO 1 full
5	RF1W	R/W1C	0h	Rx FIFO 1 Watermark Reached 0 Rx FIFO 1 fill level below watermark 1 Rx FIFO 1 fill level reached watermark
4	RF1N	R/W1C	0h	Rx FIFO 1 New Message 0 No new message written to Rx FIFO 1 1 New message written to Rx FIFO 1
3	RF0L	R/W1C	0h	Rx FIFO 0 Message Lost 0 No Rx FIFO 0 message lost 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero
2	RF0F	R/W1C	0h	Rx FIFO 0 Full 0 Rx FIFO 0 not full 1 Rx FIFO 0 full
1	RF0W	R/W1C	0h	Rx FIFO 0 Watermark Reached 0 Rx FIFO 0 fill level below watermark 1 Rx FIFO 0 fill level reached watermark
0	RF0N	R/W1C	0h	Rx FIFO 0 New Message 0 No new message written to Rx FIFO 0 1 New message written to Rx FIFO 0

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24 MCAN_IE Register (Offset = 7054h) [Reset = 00000000h]

MCAN_IE is shown in Figure 30-50 and described in Table 30-43.

Return to the Summary Table.

MCAN Interrupt Enable

Figure 30-50. MCAN_IE Register

31	30	29	28	27	26	25	24
RESERVED		ARAE	PEDE	PEAE	WDIE	BOE	EWE
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30-67. MCAN_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29	ARAE	R/W	0h	Access to Reserved Address Enable
28	PEDE	R/W	0h	Protocol Error in Data Phase Enable
27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Enable
26	WDIE	R/W	0h	Watchdog Interrupt Enable
25	BOE	R/W	0h	Bus_Off Status Enable
24	EWE	R/W	0h	Warning Status Enable
23	EPE	R/W	0h	Error Passive Enable
22	ELOE	R/W	0h	Error Logging Overflow Enable
21	BEUE	R/W	0h	Bit Error Uncorrected Enable
20	BECE	R/W	0h	Bit Error Corrected Enable A separate interrupt line reserved for corrected bit errors is provided via the MCAN_ERROR_REGS. It advised for the user to use these registers and leave this bit cleared to '0'.
19	DRXE	R/W	0h	Message Stored to Dedicated Rx Buffer Enable
18	TOOE	R/W	0h	Timeout Occurred Enable
17	MRAFE	R/W	0h	Message RAM Access Failure Enable
16	TSWE	R/W	0h	Timestamp Wraparound Enable
15	TEFLE	R/W	0h	Tx Event FIFO Element Lost Enable
14	TEFFE	R/W	0h	Tx Event FIFO Full Enable
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Enable
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Enable
11	TFEE	R/W	0h	Tx FIFO Empty Enable
10	TCFE	R/W	0h	Transmission Cancellation Finished Enable
9	TCE	R/W	0h	Transmission Completed Enable
8	HPME	R/W	0h	High Priority Message Enable

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Table 30-67. MCAN_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Enable
6	RF1FE	R/W	0h	Rx FIFO 1 Full Enable
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Enable
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Enable
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Enable
2	RF0FE	R/W	0h	Rx FIFO 0 Full Enable
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Enable
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Enable

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25 MCAN_ILS Register (Offset = 7058h) [Reset = 00000000h]

MCAN_ILS is shown in Figure 30-51 and described in Table 30-44.

Return to the Summary Table.

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via ILE.EINT0 and ILE.EINT1.

Figure 30-51. MCAN_ILS Register

31	30	29	28	27	26	25	24
RESERVED		ARAL	PEDL	PEAL	WDIL	BOL	EWL
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30-69. MCAN_ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29	ARAL	R/W	0h	Access to Reserved Address Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
28	PEDL	R/W	0h	Protocol Error in Data Phase Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
26	WDIL	R/W	0h	Watchdog Interrupt Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
25	BOL	R/W	0h	Bus_Off Status Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
24	EWL	R/W	0h	Warning Status Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
23	EPL	R/W	0h	Error Passive Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
22	ELOL	R/W	0h	Error Logging Overflow Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
21	BEUL	R/W	0h	Bit Error Uncorrected Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1

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Table 30-69. MCAN_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	BECL	R/W	0h	Bit Error Corrected Line A separate interrupt line reserved for corrected bit errors is provided via the MCAN_ERROR_REGS. It advised for the user to use these registers and leave the MCAN_IE.BECE bit cleared to '0' (disabled), thereby relegating this bit to not applicable.
19	DRXL	R/W	0h	Message Stored to Dedicated Rx Buffer Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
18	TOOL	R/W	0h	Timeout Occurred Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
17	MRAFL	R/W	0h	Message RAM Access Failure Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
16	TSWL	R/W	0h	Timestamp Wraparound Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
15	TEFLL	R/W	0h	Tx Event FIFO Element Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
14	TEFFL	R/W	0h	Tx Event FIFO Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
11	TFEL	R/W	0h	Tx FIFO Empty Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
10	TCFL	R/W	0h	Transmission Cancellation Finished Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
9	TCL	R/W	0h	Transmission Completed Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
8	HPML	R/W	0h	High Priority Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
6	RF1FL	R/W	0h	Rx FIFO 1 Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1

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Table 30-69. MCAN_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RF0FL	R/W	0h	Rx FIFO 0 Full Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Line 0 Interrupt source is assigned to Interrupt Line 0 1 Interrupt source is assigned to Interrupt Line 1

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26 MCAN_ILE Register (Offset = 705Ch) [Reset = 00000000h]

MCAN_ILE is shown in Figure 30-52 and described in Table 30-45.

Return to the Summary Table.

MCAN Interrupt Line Enable

Figure 30-52. MCAN_ILE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						EINT1	EINT0
R/W-0h						R/W-0h	R/W-0h

Table 30-71. MCAN_ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	EINT1	R/W	0h	Enable Interrupt Line 1 0 Interrupt Line 1 is disabled 1 Interrupt Line 1 is enabled
0	EINT0	R/W	0h	Enable Interrupt Line 0 0 Interrupt Line 0 is disabled 1 Interrupt Line 0 is enabled

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27 MCAN_GFC Register (Offset = 7080h) [Reset = 00000000h]

MCAN_GFC is shown in Figure 30-53 and described in Table 30-46.

Return to the Summary Table.

MCAN Global Filter Configuration

Figure 30-53. MCAN_GFC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		ANFS		ANFE		RRFS	RRFE
R/W-0h		R/WQ-0h		R/WQ-0h		R/WQ-0h	R/WQ-0h

Table 30-73. MCAN_GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-4	ANFS	R/WQ	0h	Accept Non-matching Frames Standard. Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00 Accept in Rx FIFO 0 01 Accept in Rx FIFO 1 10 Reject 11 Reject Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
3-2	ANFE	R/WQ	0h	Accept Non-matching Frames Extended. Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00 Accept in Rx FIFO 0 01 Accept in Rx FIFO 1 10 Reject 11 Reject Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1	RRFS	R/WQ	0h	Reject Remote Frames Standard 0 Filter remote frames with 11-bit standard IDs 1 Reject all remote frames with 11-bit standard IDs Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
0	RRFE	R/WQ	0h	Reject Remote Frames Extended 0 Filter remote frames with 29-bit extended IDs 1 Reject all remote frames with 29-bit extended IDs Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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28 MCAN_SIDFC Register (Offset = 7084h) [Reset = 00000000h]

MCAN_SIDFC is shown in Figure 30-54 and described in Table 30-47.

Return to the Summary Table.

MCAN Standard ID Filter Configuration

Figure 30-54. MCAN_SIDFC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
LSS							
R/WQ-0h							
15	14	13	12	11	10	9	8
FLSSA							
R/WQ-0h							
7	6	5	4	3	2	1	0
FLSSA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-75. MCAN_SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23-16	LSS	R/WQ	0h	List Size Standard 0 No standard Message ID filter 1-128 Number of standard Message ID filter elements >128 Values greater than 128 are interpreted as 128
15-2	FLSSA	R/WQ	0h	Filter List Standard Start Address. Start address of standard Message ID filter list (32-bit word address).
1-0	RESERVED	R/W	0h	

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29 MCAN_XIDFC Register (Offset = 7088h) [Reset = 00000000h]

MCAN_XIDFC is shown in Figure 30-55 and described in Table 30-48.

Return to the Summary Table.

MCAN Extended ID Filter Configuration

Figure 30-55. MCAN_XIDFC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED	LSE						
R/W-0h	R/WQ-0h						
15	14	13	12	11	10	9	8
FLESA							
R/WQ-0h							
7	6	5	4	3	2	1	0
FLESA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-77. MCAN_XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	0h	
22-16	LSE	R/WQ	0h	Filter List Extended Start Address. Start address of extended Message ID filter list (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	FLESA	R/WQ	0h	List Size Extended 0 No extended Message ID filter 1-64 Number of extended Message ID filter elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R/W	0h	

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30 MCAN_XIDAM Register (Offset = 7090h) [Reset = 1FFFFFFFh]

MCAN_XIDAM is shown in Figure 30-56 and described in Table 30-49.

Return to the Summary Table.

MCAN Extended ID and Mask

Figure 30-56. MCAN_XIDAM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			EIDM																												
R/W-0h			R/WQ-1FFFFFFFh																												

Table 30-79. MCAN_XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28-0	EIDM	R/WQ	1FFFFFFFh	Extended ID Mask. For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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31 MCAN_HPMS Register (Offset = 7094h) [Reset = 00000000h]

MCAN_HPMS is shown in Figure 30-57 and described in Table 30-50.

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This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Figure 30-57. MCAN_HPMS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
FLST	FIDX						
R-0h	R-0h						
7	6	5	4	3	2	1	0
MSI		BIDX					
R-0h		R-0h					

Table 30-81. MCAN_HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15	FLST	R	0h	Filter List. Indicates the filter list of the matching filter element. 0 Standard Filter List 1 Extended Filter List
14-8	FIDX	R	0h	Filter Index. Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1.
7-6	MSI	R	0h	Message Storage Indicator 00 No FIFO selected 01 FIFO message lost 10 Message stored in FIFO 0 11 Message stored in FIFO 1
5-0	BIDX	R	0h	Buffer Index. Index of Rx FIFO element to which the message was stored. Only valid when MSI(1) = '1'.

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32 MCAN_NDAT1 Register (Offset = 7098h) [Reset = 00000000h]

MCAN_NDAT1 is shown in Figure 30-58 and described in Table 30-51.

Return to the Summary Table.

MCAN New Data 1

Figure 30-58. MCAN_NDAT1 Register

31	30	29	28	27	26	25	24
ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 30-83. MCAN_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND31	R/W1C	0h	New Data RX Buffer 31 0 Rx Buffer not updated 1 Rx Buffer updated from new message
30	ND30	R/W1C	0h	New Data RX Buffer 30 0 Rx Buffer not updated 1 Rx Buffer updated from new message
29	ND29	R/W1C	0h	New Data RX Buffer 29 0 Rx Buffer not updated 1 Rx Buffer updated from new message
28	ND28	R/W1C	0h	New Data RX Buffer 28 0 Rx Buffer not updated 1 Rx Buffer updated from new message
27	ND27	R/W1C	0h	New Data RX Buffer 27 0 Rx Buffer not updated 1 Rx Buffer updated from new message
26	ND26	R/W1C	0h	New Data RX Buffer 26 0 Rx Buffer not updated 1 Rx Buffer updated from new message
25	ND25	R/W1C	0h	New Data RX Buffer 25 0 Rx Buffer not updated 1 Rx Buffer updated from new message
24	ND24	R/W1C	0h	New Data RX Buffer 24 0 Rx Buffer not updated 1 Rx Buffer updated from new message
23	ND23	R/W1C	0h	New Data RX Buffer 23 0 Rx Buffer not updated 1 Rx Buffer updated from new message
22	ND22	R/W1C	0h	New Data RX Buffer 22 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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Table 30-83. MCAN_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ND21	R/W1C	0h	New Data RX Buffer 21 0 Rx Buffer not updated 1 Rx Buffer updated from new message
20	ND20	R/W1C	0h	New Data RX Buffer 20 0 Rx Buffer not updated 1 Rx Buffer updated from new message
19	ND19	R/W1C	0h	New Data RX Buffer 19 0 Rx Buffer not updated 1 Rx Buffer updated from new message
18	ND18	R/W1C	0h	New Data RX Buffer 18 0 Rx Buffer not updated 1 Rx Buffer updated from new message
17	ND17	R/W1C	0h	New Data RX Buffer 17 0 Rx Buffer not updated 1 Rx Buffer updated from new message
16	ND16	R/W1C	0h	New Data RX Buffer 16 0 Rx Buffer not updated 1 Rx Buffer updated from new message
15	ND15	R/W1C	0h	New Data RX Buffer 15 0 Rx Buffer not updated 1 Rx Buffer updated from new message
14	ND14	R/W1C	0h	New Data RX Buffer 14 0 Rx Buffer not updated 1 Rx Buffer updated from new message
13	ND13	R/W1C	0h	New Data RX Buffer 13 0 Rx Buffer not updated 1 Rx Buffer updated from new message
12	ND12	R/W1C	0h	New Data RX Buffer 12 0 Rx Buffer not updated 1 Rx Buffer updated from new message
11	ND11	R/W1C	0h	New Data RX Buffer 11 0 Rx Buffer not updated 1 Rx Buffer updated from new message
10	ND10	R/W1C	0h	New Data RX Buffer 10 0 Rx Buffer not updated 1 Rx Buffer updated from new message
9	ND9	R/W1C	0h	New Data RX Buffer 9 0 Rx Buffer not updated 1 Rx Buffer updated from new message
8	ND8	R/W1C	0h	New Data RX Buffer 8 0 Rx Buffer not updated 1 Rx Buffer updated from new message
7	ND7	R/W1C	0h	New Data RX Buffer 7 0 Rx Buffer not updated 1 Rx Buffer updated from new message
6	ND6	R/W1C	0h	New Data RX Buffer 6 0 Rx Buffer not updated 1 Rx Buffer updated from new message
5	ND5	R/W1C	0h	New Data RX Buffer 5 0 Rx Buffer not updated 1 Rx Buffer updated from new message
4	ND4	R/W1C	0h	New Data RX Buffer 4 0 Rx Buffer not updated 1 Rx Buffer updated from new message
3	ND3	R/W1C	0h	New Data RX Buffer 3 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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Table 30-83. MCAN_NDAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ND2	R/W1C	0h	New Data RX Buffer 2 0 Rx Buffer not updated 1 Rx Buffer updated from new message
1	ND1	R/W1C	0h	New Data RX Buffer 1 0 Rx Buffer not updated 1 Rx Buffer updated from new message
0	ND0	R/W1C	0h	New Data RX Buffer 0 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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33 MCAN_NDAT2 Register (Offset = 709Ch) [Reset = 00000000h]

MCAN_NDAT2 is shown in Figure 30-59 and described in Table 30-52.

Return to the Summary Table.

MCAN New Data 2

Figure 30-59. MCAN_NDAT2 Register

31	30	29	28	27	26	25	24
ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 30-85. MCAN_NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ND63	R/W1C	0h	New Data RX Buffer 63 0 Rx Buffer not updated 1 Rx Buffer updated from new message
30	ND62	R/W1C	0h	New Data RX Buffer 62 0 Rx Buffer not updated 1 Rx Buffer updated from new message
29	ND61	R/W1C	0h	New Data RX Buffer 61 0 Rx Buffer not updated 1 Rx Buffer updated from new message
28	ND60	R/W1C	0h	New Data RX Buffer 60 0 Rx Buffer not updated 1 Rx Buffer updated from new message
27	ND59	R/W1C	0h	New Data RX Buffer 59 0 Rx Buffer not updated 1 Rx Buffer updated from new message
26	ND58	R/W1C	0h	New Data RX Buffer 58 0 Rx Buffer not updated 1 Rx Buffer updated from new message
25	ND57	R/W1C	0h	New Data RX Buffer 57 0 Rx Buffer not updated 1 Rx Buffer updated from new message
24	ND56	R/W1C	0h	New Data RX Buffer 56 0 Rx Buffer not updated 1 Rx Buffer updated from new message
23	ND55	R/W1C	0h	New Data RX Buffer 55 0 Rx Buffer not updated 1 Rx Buffer updated from new message
22	ND54	R/W1C	0h	New Data RX Buffer 54 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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Table 30-85. MCAN_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ND53	R/W1C	0h	New Data RX Buffer 53 0 Rx Buffer not updated 1 Rx Buffer updated from new message
20	ND52	R/W1C	0h	New Data RX Buffer 52 0 Rx Buffer not updated 1 Rx Buffer updated from new message
19	ND51	R/W1C	0h	New Data RX Buffer 51 0 Rx Buffer not updated 1 Rx Buffer updated from new message
18	ND50	R/W1C	0h	New Data RX Buffer 50 0 Rx Buffer not updated 1 Rx Buffer updated from new message
17	ND49	R/W1C	0h	New Data RX Buffer 49 0 Rx Buffer not updated 1 Rx Buffer updated from new message
16	ND48	R/W1C	0h	New Data RX Buffer 48 0 Rx Buffer not updated 1 Rx Buffer updated from new message
15	ND47	R/W1C	0h	New Data RX Buffer 47 0 Rx Buffer not updated 1 Rx Buffer updated from new message
14	ND46	R/W1C	0h	New Data RX Buffer 46 0 Rx Buffer not updated 1 Rx Buffer updated from new message
13	ND45	R/W1C	0h	New Data RX Buffer 45 0 Rx Buffer not updated 1 Rx Buffer updated from new message
12	ND44	R/W1C	0h	New Data RX Buffer 44 0 Rx Buffer not updated 1 Rx Buffer updated from new message
11	ND43	R/W1C	0h	New Data RX Buffer 43 0 Rx Buffer not updated 1 Rx Buffer updated from new message
10	ND42	R/W1C	0h	New Data RX Buffer 42 0 Rx Buffer not updated 1 Rx Buffer updated from new message
9	ND41	R/W1C	0h	New Data RX Buffer 41 0 Rx Buffer not updated 1 Rx Buffer updated from new message
8	ND40	R/W1C	0h	New Data RX Buffer 40 0 Rx Buffer not updated 1 Rx Buffer updated from new message
7	ND39	R/W1C	0h	New Data RX Buffer 39 0 Rx Buffer not updated 1 Rx Buffer updated from new message
6	ND38	R/W1C	0h	New Data RX Buffer 38 0 Rx Buffer not updated 1 Rx Buffer updated from new message
5	ND37	R/W1C	0h	New Data RX Buffer 37 0 Rx Buffer not updated 1 Rx Buffer updated from new message
4	ND36	R/W1C	0h	New Data RX Buffer 36 0 Rx Buffer not updated 1 Rx Buffer updated from new message
3	ND35	R/W1C	0h	New Data RX Buffer 35 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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Table 30-85. MCAN_NDAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ND34	R/W1C	0h	New Data RX Buffer 34 0 Rx Buffer not updated 1 Rx Buffer updated from new message
1	ND33	R/W1C	0h	New Data RX Buffer 33 0 Rx Buffer not updated 1 Rx Buffer updated from new message
0	ND32	R/W1C	0h	New Data RX Buffer 32 0 Rx Buffer not updated 1 Rx Buffer updated from new message

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34 MCAN_RXF0C Register (Offset = 70A0h) [Reset = 00000000h]

MCAN_RXF0C is shown in Figure 30-60 and described in Table 30-53.

Return to the Summary Table.

MCAN Rx FIFO 0 Configuration

Figure 30-60. MCAN_RXF0C Register

31	30	29	28	27	26	25	24
F0OM	F0WM						
R/WQ-0h	R/WQ-0h						
23	22	21	20	19	18	17	16
RESERVED	F0S						
R/W-0h	R/WQ-0h						
15	14	13	12	11	10	9	8
F0SA							
R/WQ-0h							
7	6	5	4	3	2	1	0
F0SA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-87. MCAN_RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/WQ	0h	FIFO 0 Operation Mode. FIFO 0 can be operated in blocking or in overwrite mode. 0 FIFO 0 blocking mode 1 FIFO 0 overwrite mode Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F0WM	R/WQ	0h	Rx FIFO 0 Watermark 0 Watermark interrupt disabled 1-64 Level for Rx FIFO 0 watermark interrupt (IR.RF0W) >64 Watermark interrupt disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R/W	0h	
22-16	F0S	R/WQ	0h	Rx FIFO 0 Size. The Rx FIFO 0 elements are indexed from 0 to F0S-1. 0 No Rx FIFO 0 1-64 Number of Rx FIFO 0 elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F0SA	R/WQ	0h	Rx FIFO 0 Start Address. Start address of Rx FIFO 0 in Message RAM (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
1-0	RESERVED	R/W	0h	

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35 MCAN_RXF0S Register (Offset = 70A4h) [Reset = 00000000h]

MCAN_RXF0S is shown in Figure 30-61 and described in Table 30-54.

Return to the Summary Table.

MCAN Rx FIFO 0 Status

Figure 30-61. MCAN_RXF0S Register

31	30	29	28	27	26	25	24
RESERVED						RF0L	F0F
R-0h						R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED		F0PI					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESERVED		F0GI					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RESERVED	F0FL						
R-0h	R-0h						

Table 30-89. MCAN_RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25	RF0L	R	0h	Rx FIFO 0 Message Lost. This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0 No Rx FIFO 0 message lost 1 Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Note: Overwriting the oldest message when RXF0C.F0OM = '1' will not set this flag.
24	F0F	R	0h	Rx FIFO 0 Full 0 Rx FIFO 0 not full 1 Rx FIFO 0 full
23-22	RESERVED	R	0h	
21-16	F0PI	R	0h	Rx FIFO 0 Put Index. Rx FIFO 0 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	
13-8	F0GI	R	0h	Rx FIFO 0 Get Index. Rx FIFO 0 read index pointer, range 0 to 63.
7	RESERVED	R	0h	
6-0	F0FL	R	0h	Rx FIFO 0 Fill Level. Number of elements stored in Rx FIFO 0, range 0 to 64.

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36 MCAN_RXF0A Register (Offset = 70A8h) [Reset = 00000000h]

MCAN_RXF0A is shown in Figure 30-62 and described in Table 30-55.

Return to the Summary Table.

MCAN Rx FIFO 0 Acknowledge

Figure 30-62. MCAN_RXF0A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										F0AI					
R/W-0h																										R/W-0h					

Table 30-91. MCAN_RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL.

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37 MCAN_RXBC Register (Offset = 70ACh) [Reset = 00000000h]

MCAN_RXBC is shown in Figure 30-63 and described in Table 30-56.

Return to the Summary Table.

MCAN Rx Buffer Configuration

Figure 30-63. MCAN_RXBC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RBSA														RESERVED	
R/W-0h																R/WQ-0h														R/W-0h	

Table 30-93. MCAN_RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-2	RBSA	R/WQ	0h	Rx Buffer Start Address. Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address).
1-0	RESERVED	R/W	0h	

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38 MCAN_RXF1C Register (Offset = 70B0h) [Reset = 00000000h]

MCAN_RXF1C is shown in Figure 30-64 and described in Table 30-57.

Return to the Summary Table.

MCAN Rx FIFO 1 Configuration

Figure 30-64. MCAN_RXF1C Register

31	30	29	28	27	26	25	24
F1OM	F1WM						
R/WQ-0h	R/WQ-0h						
23	22	21	20	19	18	17	16
RESERVED	F1S						
R/W-0h	R/WQ-0h						
15	14	13	12	11	10	9	8
F1SA							
R/WQ-0h							
7	6	5	4	3	2	1	0
F1SA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-95. MCAN_RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/WQ	0h	FIFO 1 Operation Mode. FIFO 1 can be operated in blocking or in overwrite mode. 0 FIFO 1 blocking mode 1 FIFO 1 overwrite mode Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
30-24	F1WM	R/WQ	0h	Rx FIFO 1 Watermark 0 Watermark interrupt disabled 1-64 Level for Rx FIFO 1 watermark interrupt (IR.RF1W) >64 Watermark interrupt disabled Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23	RESERVED	R/W	0h	
22-16	F1S	R/WQ	0h	Rx FIFO 1 Size. The Rx FIFO 1 elements are indexed from 0 to F1S - 1. 0 No Rx FIFO 1 1-64 Number of Rx FIFO 1 elements >64 Values greater than 64 are interpreted as 64 Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	F1SA	R/WQ	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address).
1-0	RESERVED	R/W	0h	

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39 MCAN_RXF1S Register (Offset = 70B4h) [Reset = 00000000h]

MCAN_RXF1S is shown in Figure 30-65 and described in Table 30-58.

Return to the Summary Table.

MCAN Rx FIFO 1 Status

Figure 30-65. MCAN_RXF1S Register

31	30	29	28	27	26	25	24
DMS		RESERVED				RF1L	F1F
R-0h		R-0h				R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED		F1PI					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESERVED		F1GI					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RESERVED	F1FL						
R-0h	R-0h						

Table 30-97. MCAN_RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DMS	R	0h	Debug Message Status 00 Idle state, wait for reception of debug messages 01 Debug message A received 10 Debug messages A, B received 11 Debug messages A, B, C received
29-26	RESERVED	R	0h	
25	RF1L	R	0h	Rx FIFO 1 Message Lost. This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0 No Rx FIFO 1 message lost 1 Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: Overwriting the oldest message when RXF1C.F1OM = '1' will not set this flag.
24	F1F	R	0h	Rx FIFO 1 Full 0 Rx FIFO 1 not full 1 Rx FIFO 1 full
23-22	RESERVED	R	0h	
21-16	F1PI	R	0h	Rx FIFO 1 Put Index. Rx FIFO 1 write index pointer, range 0 to 63.
15-14	RESERVED	R	0h	
13-8	F1GI	R	0h	Rx FIFO 1 Get Index. Rx FIFO 1 read index pointer, range 0 to 63.
7	RESERVED	R	0h	
6-0	F1FL	R	0h	Rx FIFO 1 Fill Level. Number of elements stored in Rx FIFO 1, range 0 to 64.

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40 MCAN_RXF1A Register (Offset = 70B8h) [Reset = 00000000h]

MCAN_RXF1A is shown in Figure 30-66 and described in Table 30-59.

Return to the Summary Table.

MCAN Rx FIFO 1 Acknowledge

Figure 30-66. MCAN_RXF1A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										F1AI					
R/W-0h																										R/W-0h					

Table 30-99. MCAN_RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index. After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL.

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41 MCAN_RXESC Register (Offset = 70BCh) [Reset = 00000000h]

MCAN_RXESC is shown in Figure 30-67 and described in Table 30-60.

Return to the Summary Table.

Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Figure 30-67. MCAN_RXESC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					RBDS		
R/W-0h					R/WQ-0h		
7	6	5	4	3	2	1	0
RESERVED	F1DS			RESERVED	F0DS		
R/W-0h	R/WQ-0h			R/W-0h	R/WQ-0h		

Table 30-101. MCAN_RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	0h	
10-8	RBDS	R/WQ	0h	Rx Buffer Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
7	RESERVED	R/W	0h	
6-4	F1DS	R/WQ	0h	Rx FIFO 1 Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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Table 30-101. MCAN_RXESC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	0h	
2-0	F0DS	R/WQ	0h	Rx FIFO 0 Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by RXESC are stored to the Rx Buffer resp. Rx FIFO element. The rest of the frame's data field is ignored. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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42 MCAN_TXBC Register (Offset = 70C0h) [Reset = 00000000h]

MCAN_TXBC is shown in Figure 30-68 and described in Table 30-61.

Return to the Summary Table.

MCAN Tx Buffer Configuration

Figure 30-68. MCAN_TXBC Register

31	30	29	28	27	26	25	24
RESERVED	TFQM	TFQS					
R/W-0h	R/WQ-0h	R/WQ-0h					
23	22	21	20	19	18	17	16
RESERVED		NDTB					
R/W-0h		R/WQ-0h					
15	14	13	12	11	10	9	8
TBSA							
R/WQ-0h							
7	6	5	4	3	2	1	0
TBSA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-103. MCAN_TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	
30	TFQM	R/WQ	0h	Tx FIFO/Queue Mode 0 Tx FIFO operation 1 Tx Queue operation Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
29-24	TFQS	R/WQ	0h	Transmit FIFO/Queue Size 0 No Tx FIFO/Queue 1-32 Number of Tx Buffers used for Tx FIFO/Queue >32 Values greater than 32 are interpreted as 32 Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
23-22	RESERVED	R/W	0h	
21-16	NDTB	R/WQ	0h	Number of Dedicated Transmit Buffers 0 No Dedicated Tx Buffers 1-32 Number of Dedicated Tx Buffers >32 Values greater than 32 are interpreted as 32 Note: Be aware that the sum of TFQS and NDTB may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.
15-2	TBSA	R/WQ	0h	Tx Buffers Start Address. Start address of Tx Buffers section in Message RAM (32-bit word address). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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Table 30-103. MCAN_TXBC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RESERVED	R/W	0h	

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43 MCAN_TXFQS Register (Offset = 70C4h) [Reset = 00000000h]

MCAN_TXFQS is shown in Figure 30-69 and described in Table 30-62.

Return to the Summary Table.

The Tx FIFO/Queue status is related to the pending Tx requests listed in register TXBRP. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (TXBRP not yet updated).

Figure 30-69. MCAN_TXFQS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED		TFQF	TFQP				
R-0h		R-0h	R-0h				
15	14	13	12	11	10	9	8
RESERVED			TFGI				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED		TFFL					
R-0h		R-0h					

Table 30-105. MCAN_TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	
21	TFQF	R	0h	Tx FIFO/Queue Full 0 Tx FIFO/Queue not full 1 Tx FIFO/Queue full
20-16	TFQP	R	0h	Tx FIFO/Queue Put Index. Tx FIFO/Queue write index pointer, range 0 to 31. Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
15-13	RESERVED	R	0h	
12-8	TFGI	R	0h	Tx FIFO Get Index. Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1'). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.
7-6	RESERVED	R	0h	
5-0	TFFL	R	0h	Tx FIFO Free Level. Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1').

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44 MCAN_TXESC Register (Offset = 70C8h) [Reset = 00000000h]

MCAN_TXESC is shown in Figure 30-70 and described in Table 30-63.

Return to the Summary Table.

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Figure 30-70. MCAN_TXESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													TBDS		
R/W-0h													R/WQ-0h		

Table 30-107. MCAN_TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	TBDS	R/WQ	0h	Tx Buffer Data Field Size 000 8 byte data field 001 12 byte data field 010 16 byte data field 011 20 byte data field 100 24 byte data field 101 32 byte data field 110 48 byte data field 111 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as "0xCC" (padding bytes). Qualified Write is possible only with CCCR.CCE='1' and CCCR.INIT='1'.

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45 MCAN_TXBRP Register (Offset = 70CCh) [Reset = 00000000h]

MCAN_TXBRP is shown in Figure 30-71 and described in Table 30-64.

Return to the Summary Table.

MCAN Tx Buffer Request Pending

Figure 30-71. MCAN_TXBRP Register

31	30	29	28	27	26	25	24
TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 30-109. MCAN_TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRP31	R	0h	Transmission Request Pending 31. See description for bit 0.
30	TRP30	R	0h	Transmission Request Pending 30. See description for bit 0.
29	TRP29	R	0h	Transmission Request Pending 29. See description for bit 0.
28	TRP28	R	0h	Transmission Request Pending 28. See description for bit 0.
27	TRP27	R	0h	Transmission Request Pending 27. See description for bit 0.
26	TRP26	R	0h	Transmission Request Pending 26. See description for bit 0.
25	TRP25	R	0h	Transmission Request Pending 25. See description for bit 0.
24	TRP24	R	0h	Transmission Request Pending 24. See description for bit 0.
23	TRP23	R	0h	Transmission Request Pending 23. See description for bit 0.
22	TRP22	R	0h	Transmission Request Pending 22. See description for bit 0.
21	TRP21	R	0h	Transmission Request Pending 21. See description for bit 0.
20	TRP20	R	0h	Transmission Request Pending 20. See description for bit 0.
19	TRP19	R	0h	Transmission Request Pending 19. See description for bit 0.
18	TRP18	R	0h	Transmission Request Pending 18. See description for bit 0.
17	TRP17	R	0h	Transmission Request Pending 17. See description for bit 0.
16	TRP16	R	0h	Transmission Request Pending 16. See description for bit 0.
15	TRP15	R	0h	Transmission Request Pending 15. See description for bit 0.
14	TRP14	R	0h	Transmission Request Pending 14. See description for bit 0.
13	TRP13	R	0h	Transmission Request Pending 13. See description for bit 0.
12	TRP12	R	0h	Transmission Request Pending 12. See description for bit 0.
11	TRP11	R	0h	Transmission Request Pending 11. See description for bit 0.
10	TRP10	R	0h	Transmission Request Pending 10. See description for bit 0.
9	TRP9	R	0h	Transmission Request Pending 9. See description for bit 0.
8	TRP8	R	0h	Transmission Request Pending 8. See description for bit 0.
7	TRP7	R	0h	Transmission Request Pending 7. See description for bit 0.

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Table 30-109. MCAN_TXBRP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TRP6	R	0h	Transmission Request Pending 6. See description for bit 0.
5	TRP5	R	0h	Transmission Request Pending 5. See description for bit 0.
4	TRP4	R	0h	Transmission Request Pending 4. See description for bit 0.
3	TRP3	R	0h	Transmission Request Pending 3. See description for bit 0.
2	TRP2	R	0h	Transmission Request Pending 2. See description for bit 0.
1	TRP1	R	0h	Transmission Request Pending 1. See description for bit 0.
0	TRP0	R	0h	Transmission Request Pending 0. Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TXBAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signalled via TXBCF - after successful transmission together with the corresponding TXBTO bit - when the transmission has not yet been started at the point of cancellation - when the transmission has been aborted due to lost arbitration - when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0 No transmission request pending 1 Transmission request pending Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding TXBRP bit is reset.

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46 MCAN_TXBAR Register (Offset = 70D0h) [Reset = 00000000h]

MCAN_TXBAR is shown in Figure 30-72 and described in Table 30-65.

Return to the Summary Table.

MCAN Tx Buffer Add Request

Figure 30-72. MCAN_TXBAR Register

31	30	29	28	27	26	25	24
AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
23	22	21	20	19	18	17	16
AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
15	14	13	12	11	10	9	8
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h

Table 30-111. MCAN_TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AR31	R/WQ	0h	Add Request 31. See description for bit 0.
30	AR30	R/WQ	0h	Add Request 30. See description for bit 0.
29	AR29	R/WQ	0h	Add Request 29. See description for bit 0.
28	AR28	R/WQ	0h	Add Request 28. See description for bit 0.
27	AR27	R/WQ	0h	Add Request 27. See description for bit 0.
26	AR26	R/WQ	0h	Add Request 26. See description for bit 0.
25	AR25	R/WQ	0h	Add Request 25. See description for bit 0.
24	AR24	R/WQ	0h	Add Request 24. See description for bit 0.
23	AR23	R/WQ	0h	Add Request 23. See description for bit 0.
22	AR22	R/WQ	0h	Add Request 22. See description for bit 0.
21	AR21	R/WQ	0h	Add Request 21. See description for bit 0.
20	AR20	R/WQ	0h	Add Request 20. See description for bit 0.
19	AR19	R/WQ	0h	Add Request 19. See description for bit 0.
18	AR18	R/WQ	0h	Add Request 18. See description for bit 0.
17	AR17	R/WQ	0h	Add Request 17. See description for bit 0.
16	AR16	R/WQ	0h	Add Request 16. See description for bit 0.
15	AR15	R/WQ	0h	Add Request 15. See description for bit 0.
14	AR14	R/WQ	0h	Add Request 14. See description for bit 0.
13	AR13	R/WQ	0h	Add Request 13. See description for bit 0.
12	AR12	R/WQ	0h	Add Request 12. See description for bit 0.
11	AR11	R/WQ	0h	Add Request 11. See description for bit 0.
10	AR10	R/WQ	0h	Add Request 10. See description for bit 0.
9	AR9	R/WQ	0h	Add Request 9. See description for bit 0.
8	AR8	R/WQ	0h	Add Request 8. See description for bit 0.
7	AR7	R/WQ	0h	Add Request 7. See description for bit 0.

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Table 30-111. MCAN_TXBAR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AR6	R/WQ	0h	Add Request 6. See description for bit 0.
5	AR5	R/WQ	0h	Add Request 5. See description for bit 0.
4	AR4	R/WQ	0h	Add Request 4. See description for bit 0.
3	AR3	R/WQ	0h	Add Request 3. See description for bit 0.
2	AR2	R/WQ	0h	Add Request 2. See description for bit 0.
1	AR1	R/WQ	0h	Add Request 1. See description for bit 0.
0	AR0	R/WQ	0h	Add Request 0. Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0 No transmission request added 1 Transmission requested added Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit already set), this add request is ignored. Qualified Write is possible only with CCCR.CCE='0'

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47 MCAN_TXBCR Register (Offset = 70D4h) [Reset = 00000000h]

MCAN_TXBCR is shown in Figure 30-73 and described in Table 30-66.

Return to the Summary Table.

MCAN Tx Buffer Cancellation Request

Figure 30-73. MCAN_TXBCR Register

31	30	29	28	27	26	25	24
CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
23	22	21	20	19	18	17	16
CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
15	14	13	12	11	10	9	8
CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h
7	6	5	4	3	2	1	0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h	R/WQ-0h

Table 30-113. MCAN_TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CR31	R/WQ	0h	Cancellation Request 31. See description for bit 0.
30	CR30	R/WQ	0h	Cancellation Request 30. See description for bit 0.
29	CR29	R/WQ	0h	Cancellation Request 29. See description for bit 0.
28	CR28	R/WQ	0h	Cancellation Request 28. See description for bit 0.
27	CR27	R/WQ	0h	Cancellation Request 27. See description for bit 0.
26	CR26	R/WQ	0h	Cancellation Request 26. See description for bit 0.
25	CR25	R/WQ	0h	Cancellation Request 25. See description for bit 0.
24	CR24	R/WQ	0h	Cancellation Request 24. See description for bit 0.
23	CR23	R/WQ	0h	Cancellation Request 23. See description for bit 0.
22	CR22	R/WQ	0h	Cancellation Request 22. See description for bit 0.
21	CR21	R/WQ	0h	Cancellation Request 21. See description for bit 0.
20	CR20	R/WQ	0h	Cancellation Request 20. See description for bit 0.
19	CR19	R/WQ	0h	Cancellation Request 19. See description for bit 0.
18	CR18	R/WQ	0h	Cancellation Request 18. See description for bit 0.
17	CR17	R/WQ	0h	Cancellation Request 17. See description for bit 0.
16	CR16	R/WQ	0h	Cancellation Request 16. See description for bit 0.
15	CR15	R/WQ	0h	Cancellation Request 15. See description for bit 0.
14	CR14	R/WQ	0h	Cancellation Request 14. See description for bit 0.
13	CR13	R/WQ	0h	Cancellation Request 13. See description for bit 0.
12	CR12	R/WQ	0h	Cancellation Request 12. See description for bit 0.
11	CR11	R/WQ	0h	Cancellation Request 11. See description for bit 0.
10	CR10	R/WQ	0h	Cancellation Request 10. See description for bit 0.
9	CR9	R/WQ	0h	Cancellation Request 9. See description for bit 0.
8	CR8	R/WQ	0h	Cancellation Request 8. See description for bit 0.
7	CR7	R/WQ	0h	Cancellation Request 7. See description for bit 0.

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Table 30-113. MCAN_TXBCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CR6	R/WQ	0h	Cancellation Request 6. See description for bit 0.
5	CR5	R/WQ	0h	Cancellation Request 5. See description for bit 0.
4	CR4	R/WQ	0h	Cancellation Request 4. See description for bit 0.
3	CR3	R/WQ	0h	Cancellation Request 3. See description for bit 0.
2	CR2	R/WQ	0h	Cancellation Request 2. See description for bit 0.
1	CR1	R/WQ	0h	Cancellation Request 1. See description for bit 0.
0	CR0	R/WQ	0h	Cancellation Request 0. Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0 No cancellation pending 1 Cancellation pending Qualified Write is possible only with CCCR.CCE='0'

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48 MCAN_TXBTO Register (Offset = 70D8h) [Reset = 00000000h]

MCAN_TXBTO is shown in Figure 30-74 and described in Table 30-67.

Return to the Summary Table.

MCAN Tx Buffer Transmission Occurred

Figure 30-74. MCAN_TXBTO Register

31	30	29	28	27	26	25	24
TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 30-115. MCAN_TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TO31	R	0h	Transmission Occurred 31. See description for bit 0.
30	TO30	R	0h	Transmission Occurred 30. See description for bit 0.
29	TO29	R	0h	Transmission Occurred 29. See description for bit 0.
28	TO28	R	0h	Transmission Occurred 28. See description for bit 0.
27	TO27	R	0h	Transmission Occurred 27. See description for bit 0.
26	TO26	R	0h	Transmission Occurred 26. See description for bit 0.
25	TO25	R	0h	Transmission Occurred 25. See description for bit 0.
24	TO24	R	0h	Transmission Occurred 24. See description for bit 0.
23	TO23	R	0h	Transmission Occurred 23. See description for bit 0.
22	TO22	R	0h	Transmission Occurred 22. See description for bit 0.
21	TO21	R	0h	Transmission Occurred 21. See description for bit 0.
20	TO20	R	0h	Transmission Occurred 20. See description for bit 0.
19	TO19	R	0h	Transmission Occurred 19. See description for bit 0.
18	TO18	R	0h	Transmission Occurred 18. See description for bit 0.
17	TO17	R	0h	Transmission Occurred 17. See description for bit 0.
16	TO16	R	0h	Transmission Occurred 16. See description for bit 0.
15	TO15	R	0h	Transmission Occurred 15. See description for bit 0.
14	TO14	R	0h	Transmission Occurred 14. See description for bit 0.
13	TO13	R	0h	Transmission Occurred 13. See description for bit 0.
12	TO12	R	0h	Transmission Occurred 12. See description for bit 0.
11	TO11	R	0h	Transmission Occurred 11. See description for bit 0.
10	TO10	R	0h	Transmission Occurred 10. See description for bit 0.
9	TO9	R	0h	Transmission Occurred 9. See description for bit 0.
8	TO8	R	0h	Transmission Occurred 8. See description for bit 0.
7	TO7	R	0h	Transmission Occurred 7. See description for bit 0.

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Table 30-115. MCAN_TXBTO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TO6	R	0h	Transmission Occurred 6. See description for bit 0.
5	TO5	R	0h	Transmission Occurred 5. See description for bit 0.
4	TO4	R	0h	Transmission Occurred 4. See description for bit 0.
3	TO3	R	0h	Transmission Occurred 3. See description for bit 0.
2	TO2	R	0h	Transmission Occurred 2. See description for bit 0.
1	TO1	R	0h	Transmission Occurred 1. See description for bit 0.
0	TO0	R	0h	Transmission Occurred 0. Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0 No transmission occurred 1 Transmission occurred

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49 MCAN_TXBCF Register (Offset = 70DCh) [Reset = 00000000h]

MCAN_TXBCF is shown in Figure 30-75 and described in Table 30-68.

Return to the Summary Table.

MCAN Tx Buffer Cancellation Finished

Figure 30-75. MCAN_TXBCF Register

31	30	29	28	27	26	25	24
CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 30-117. MCAN_TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CF31	R	0h	Cancellation Finished 31. See description for bit 0.
30	CF30	R	0h	Cancellation Finished 30. See description for bit 0.
29	CF29	R	0h	Cancellation Finished 29. See description for bit 0.
28	CF28	R	0h	Cancellation Finished 28. See description for bit 0.
27	CF27	R	0h	Cancellation Finished 27. See description for bit 0.
26	CF26	R	0h	Cancellation Finished 26. See description for bit 0.
25	CF25	R	0h	Cancellation Finished 25. See description for bit 0.
24	CF24	R	0h	Cancellation Finished 24. See description for bit 0.
23	CF23	R	0h	Cancellation Finished 23. See description for bit 0.
22	CF22	R	0h	Cancellation Finished 22. See description for bit 0.
21	CF21	R	0h	Cancellation Finished 21. See description for bit 0.
20	CF20	R	0h	Cancellation Finished 20. See description for bit 0.
19	CF19	R	0h	Cancellation Finished 19. See description for bit 0.
18	CF18	R	0h	Cancellation Finished 18. See description for bit 0.
17	CF17	R	0h	Cancellation Finished 17. See description for bit 0.
16	CF16	R	0h	Cancellation Finished 16. See description for bit 0.
15	CF15	R	0h	Cancellation Finished 15. See description for bit 0.
14	CF14	R	0h	Cancellation Finished 14. See description for bit 0.
13	CF13	R	0h	Cancellation Finished 13. See description for bit 0.
12	CF12	R	0h	Cancellation Finished 12. See description for bit 0.
11	CF11	R	0h	Cancellation Finished 11. See description for bit 0.
10	CF10	R	0h	Cancellation Finished 10. See description for bit 0.
9	CF9	R	0h	Cancellation Finished 9. See description for bit 0.
8	CF8	R	0h	Cancellation Finished 8. See description for bit 0.
7	CF7	R	0h	Cancellation Finished 7. See description for bit 0.

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Table 30-117. MCAN_TXBCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CF6	R	0h	Cancellation Finished 6. See description for bit 0.
5	CF5	R	0h	Cancellation Finished 5. See description for bit 0.
4	CF4	R	0h	Cancellation Finished 4. See description for bit 0.
3	CF3	R	0h	Cancellation Finished 3. See description for bit 0.
2	CF2	R	0h	Cancellation Finished 2. See description for bit 0.
1	CF1	R	0h	Cancellation Finished 1. See description for bit 0.
0	CF0	R	0h	Cancellation Finished 0. Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0 No transmit buffer cancellation 1 Transmit buffer cancellation finished

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50 MCAN_TXBTIE Register (Offset = 70E0h) [Reset = 00000000h]

MCAN_TXBTIE is shown in Figure 30-76 and described in Table 30-69.

Return to the Summary Table.

MCAN Tx Buffer Transmission Interrupt Enable

Figure 30-76. MCAN_TXBTIE Register

31	30	29	28	27	26	25	24
TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30-119. MCAN_TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TIE31	R/W	0h	Transmission Interrupt Enable 31. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
30	TIE30	R/W	0h	Transmission Interrupt Enable 30. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
29	TIE29	R/W	0h	Transmission Interrupt Enable 29. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
28	TIE28	R/W	0h	Transmission Interrupt Enable 28. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
27	TIE27	R/W	0h	Transmission Interrupt Enable 27. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
26	TIE26	R/W	0h	Transmission Interrupt Enable 26. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
25	TIE25	R/W	0h	Transmission Interrupt Enable 25. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
24	TIE24	R/W	0h	Transmission Interrupt Enable 24. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable

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Table 30-119. MCAN_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	TIE23	R/W	0h	Transmission Interrupt Enable 23. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
22	TIE22	R/W	0h	Transmission Interrupt Enable 22. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
21	TIE21	R/W	0h	Transmission Interrupt Enable 21. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
20	TIE20	R/W	0h	Transmission Interrupt Enable 20. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
19	TIE19	R/W	0h	Transmission Interrupt Enable 19. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
18	TIE18	R/W	0h	Transmission Interrupt Enable 18. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
17	TIE17	R/W	0h	Transmission Interrupt Enable 17. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
16	TIE16	R/W	0h	Transmission Interrupt Enable 16. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
15	TIE15	R/W	0h	Transmission Interrupt Enable 15. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
14	TIE14	R/W	0h	Transmission Interrupt Enable 14. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
13	TIE13	R/W	0h	Transmission Interrupt Enable 13. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
12	TIE12	R/W	0h	Transmission Interrupt Enable 12. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
11	TIE11	R/W	0h	Transmission Interrupt Enable 11. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
10	TIE10	R/W	0h	Transmission Interrupt Enable 10. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable

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Table 30-119. MCAN_TXBTIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TIE9	R/W	0h	Transmission Interrupt Enable 9. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
8	TIE8	R/W	0h	Transmission Interrupt Enable 8. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
7	TIE7	R/W	0h	Transmission Interrupt Enable 7. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
6	TIE6	R/W	0h	Transmission Interrupt Enable 6. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
5	TIE5	R/W	0h	Transmission Interrupt Enable 5. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
4	TIE4	R/W	0h	Transmission Interrupt Enable 4. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
3	TIE3	R/W	0h	Transmission Interrupt Enable 3. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
2	TIE2	R/W	0h	Transmission Interrupt Enable 2. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
1	TIE1	R/W	0h	Transmission Interrupt Enable 1. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable
0	TIE0	R/W	0h	Transmission Interrupt Enable 0. Each Tx Buffer has its own Transmission Interrupt Enable bit. 0 Transmission interrupt disabled 1 Transmission interrupt enable

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51 MCAN_TXBCIE Register (Offset = 70E4h) [Reset = 00000000h]

MCAN_TXBCIE is shown in Figure 30-77 and described in Table 30-70.

Return to the Summary Table.

MCAN Tx Buffer Cancellation Finished Interrupt Enable

Figure 30-77. MCAN_TXBCIE Register

31	30	29	28	27	26	25	24
CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30-121. MCAN_TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFIE31	R/W	0h	Cancellation Finished Interrupt Enable 31. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
30	CFIE30	R/W	0h	Cancellation Finished Interrupt Enable 30. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
29	CFIE29	R/W	0h	Cancellation Finished Interrupt Enable 29. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
28	CFIE28	R/W	0h	Cancellation Finished Interrupt Enable 28. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
27	CFIE27	R/W	0h	Cancellation Finished Interrupt Enable 27. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
26	CFIE26	R/W	0h	Cancellation Finished Interrupt Enable 26. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
25	CFIE25	R/W	0h	Cancellation Finished Interrupt Enable 25. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
24	CFIE24	R/W	0h	Cancellation Finished Interrupt Enable 24. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled

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Table 30-121. MCAN_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	CFIE23	R/W	0h	Cancellation Finished Interrupt Enable 23. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
22	CFIE22	R/W	0h	Cancellation Finished Interrupt Enable 22. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
21	CFIE21	R/W	0h	Cancellation Finished Interrupt Enable 21. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
20	CFIE20	R/W	0h	Cancellation Finished Interrupt Enable 20. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
19	CFIE19	R/W	0h	Cancellation Finished Interrupt Enable 19. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
18	CFIE18	R/W	0h	Cancellation Finished Interrupt Enable 18. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
17	CFIE17	R/W	0h	Cancellation Finished Interrupt Enable 17. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
16	CFIE16	R/W	0h	Cancellation Finished Interrupt Enable 16. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
15	CFIE15	R/W	0h	Cancellation Finished Interrupt Enable 15. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
14	CFIE14	R/W	0h	Cancellation Finished Interrupt Enable 14. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
13	CFIE13	R/W	0h	Cancellation Finished Interrupt Enable 13. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
12	CFIE12	R/W	0h	Cancellation Finished Interrupt Enable 12. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
11	CFIE11	R/W	0h	Cancellation Finished Interrupt Enable 11. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
10	CFIE10	R/W	0h	Cancellation Finished Interrupt Enable 10. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled

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Table 30-121. MCAN_TXBCIE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CFIE9	R/W	0h	Cancellation Finished Interrupt Enable 9. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
8	CFIE8	R/W	0h	Cancellation Finished Interrupt Enable 8. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
7	CFIE7	R/W	0h	Cancellation Finished Interrupt Enable 7. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
6	CFIE6	R/W	0h	Cancellation Finished Interrupt Enable 6. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
5	CFIE5	R/W	0h	Cancellation Finished Interrupt Enable 5. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
4	CFIE4	R/W	0h	Cancellation Finished Interrupt Enable 4. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
3	CFIE3	R/W	0h	Cancellation Finished Interrupt Enable 3. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
2	CFIE2	R/W	0h	Cancellation Finished Interrupt Enable 2. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
1	CFIE1	R/W	0h	Cancellation Finished Interrupt Enable 1. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled
0	CFIE0	R/W	0h	Cancellation Finished Interrupt Enable 0. Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0 Cancellation finished interrupt disabled 1 Cancellation finished interrupt enabled

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52 MCAN_TXEFC Register (Offset = 70F0h) [Reset = 00000000h]

MCAN_TXEFC is shown in Figure 30-78 and described in Table 30-71.

Return to the Summary Table.

MCAN Tx Event FIFO Configuration

Figure 30-78. MCAN_TXEFC Register

31	30	29	28	27	26	25	24
RESERVED		EFWM					
R/W-0h		R/WQ-0h					
23	22	21	20	19	18	17	16
RESERVED		EFS					
R/W-0h		R/WQ-0h					
15	14	13	12	11	10	9	8
EFSA							
R/WQ-0h							
7	6	5	4	3	2	1	0
EFSA						RESERVED	
R/WQ-0h						R/W-0h	

Table 30-123. MCAN_TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	0h	
29-24	EFWM	R/WQ	0h	Event FIFO Watermark 0 Watermark interrupt disabled 1-32 Level for Tx Event FIFO watermark interrupt (IR.TEFW) >32 Watermark interrupt disabled
23-22	RESERVED	R/W	0h	
21-16	EFS	R/WQ	0h	Event FIFO Size. The Tx Event FIFO elements are indexed from 0 to EFS - 1. 0 Tx Event FIFO disabled 1-32 Number of Tx Event FIFO elements >32 Values greater than 32 are interpreted as 32
15-2	EFSA	R/WQ	0h	Event FIFO Start Address. Start address of Tx Event FIFO in Message RAM (32-bit word address).
1-0	RESERVED	R/W	0h	

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53 MCAN_TXEFS Register (Offset = 70F4h) [Reset = 00000000h]

MCAN_TXEFS is shown in Figure 30-79 and described in Table 30-72.

Return to the Summary Table.

MCAN Tx Event FIFO Status

Figure 30-79. MCAN_TXEFS Register

31	30	29	28	27	26	25	24
RESERVED						TEFL	EFF
R-0h						R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED			EFPI				
R-0h			R-0h				
15	14	13	12	11	10	9	8
RESERVED			EFGI				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED		EFFL					
R-0h		R-0h					

Table 30-125. MCAN_TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25	TEFL	R	0h	Tx Event FIFO Element Lost. This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0 No Tx Event FIFO element lost 1 Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	EFF	R	0h	Event FIFO Full 0 Tx Event FIFO not full 1 Tx Event FIFO full
23-21	RESERVED	R	0h	
20-16	EFPI	R	0h	Event FIFO Put Index.Tx Event FIFO write index pointer, range 0 to 31.
15-13	RESERVED	R	0h	
12-8	EFGI	R	0h	Event FIFO Get Index. Tx Event FIFO read index pointer, range 0 to 31.
7-6	RESERVED	R	0h	
5-0	EFFL	R	0h	Event FIFO Fill Level. Number of elements stored in Tx Event FIFO, range 0 to 32.

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54 MCAN_TXEFA Register (Offset = 70F8h) [Reset = 00000000h]

MCAN_TXEFA is shown in Figure 30-80 and described in Table 30-73.

Return to the Summary Table.

MCAN Tx Event FIFO Acknowledge

Figure 30-80. MCAN_TXEFA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											EFAI				
R/W-0h																											R/W-0h				

Table 30-127. MCAN_TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4-0	EFAI	R/W	0h	Event FIFO Acknowledge Index. After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL.

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55 MCANSS_PID Register (Offset = 7200h) [Reset = 68E04901h]

MCANSS_PID is shown in Figure 30-81 and described in Table 30-74.

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MCAN Subsystem Revision Register

Figure 30-81. MCANSS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		MODULE_ID											
R-1h		R-2h		R-8E0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MAJOR			RESERVED		MINOR					
R-9h					R-1h			R-0h		R-1h					

Table 30-129. MCANSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	RESERVED	R	2h	Reserved
27-16	MODULE_ID	R	8E0h	Module Identification Number
15-11	RESERVED	R	9h	Reserved
10-8	MAJOR	R	1h	Major Revision of the MCAN Subsystem
7-6	RESERVED	R	0h	Reserved
5-0	MINOR	R	1h	Minor Revision of the MCAN Subsystem

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56 MCANSS_CTRL Register (Offset = 7204h) [Reset = 00000008h]

MCANSS_CTRL is shown in Figure 30-82 and described in Table 30-75.

Return to the Summary Table.

MCAN Subsystem Control Register

Figure 30-82. MCANSS_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREQEN	DBGSUSP_FREE	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h		

Table 30-131. MCANSS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6	EXT_TS_CNTR_EN	R/W	0h	External Timestamp Counter Enable. 0 External timestamp counter disabled 1 External timestamp counter enabled
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable. Enables the MCANSS to automatically clear the MCAN CCCR.INIT bit, fully waking the MCAN up, on an enabled wakeup request. 0 Disable the automatic write to CCCR.INIT 1 Enable the automatic write to CCCR.INIT
4	WAKEUPREQEN	R/W	0h	Wakeup Request Enable. Enables the MCANSS to wakeup on CAN RXD activity. 0 Disable wakeup request 1 Enables wakeup request
3	DBGSUSP_FREE	R/W	1h	Debug Suspend Free Bit. Enables debug suspend. 0 Honor debug suspend 1 Disregard debug suspend
2-0	RESERVED	R/W	0h	

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57 MCANSS_STAT Register (Offset = 7208h) [Reset = 0000000Xh]

MCANSS_STAT is shown in Figure 30-83 and described in Table 30-76.

Return to the Summary Table.

MCAN Subsystem Status Register

Figure 30-83. MCANSS_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_FDOE	MEM_INIT_DONE	RESET
R-0h					R-Xh	R-0h	R-0h

Table 30-133. MCANSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	ENABLE_FDOE	R	Xh	Reflects the value of mcanss_enable_fdoe configuration port
1	MEM_INIT_DONE	R	0h	Memory Initialization Done. 0 Message RAM initialization is in progress 1 Message RAM is initialized for use
0	RESET	R	0h	Soft Reset Status. 0 Not in reset 1 Reset is in progress

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58 MCANSS_ICS Register (Offset = 720Ch) [Reset = 00000000h]

MCANSS_ICS is shown in Figure 30-84 and described in Table 30-77.

Return to the Summary Table.

MCAN Subsystem Interrupt Clear Shadow Register

Figure 30-84. MCANSS_ICS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
R/W-0h							R-0/W1C-0h

Table 30-135. MCANSS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EXT_TS_CNTR_OVFL	R-0/W1C	0h	External Timestamp Counter Overflow Interrupt Status Clear. Reads always return a 0. 0 Write of '0' has no effect 1 Write of '1' clears the MCANSS_IRS.EXT_TS_CNTR_OVFL bit

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59 MCANSS_IRS Register (Offset = 7210h) [Reset = 00000000h]

MCANSS_IRS is shown in Figure 30-85 and described in Table 30-78.

Return to the Summary Table.

MCAN Subsystem Interrupt Raw Satus Register

Figure 30-85. MCANSS_IRS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
R/W-0h							R/W1S-0h

Table 30-137. MCANSS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EXT_TS_CNTR_OVFL	R/W1S	0h	External Timestamp Counter Overflow Interrupt Status. This bit is set by HW or by a SW write of '1'. To clear, use the MCANSS_ICS.EXT_TS_CNTR_OVFL bit. 0 External timestamp counter has not overflowed 1 External timestamp counter has overflowed When this bit is set to '1' by HW or SW, the MCANSS_EXT_TS_UNSERVICED_INTR_CNTR.EXT_TS_INTR_CNTR bit field will increment by 1.

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60 MCANSS_IECS Register (Offset = 7214h) [Reset = 00000000h]

MCANSS_IECS is shown in Figure 30-86 and described in Table 30-79.

Return to the Summary Table.

MCAN Subsystem Interrupt Enable Clear Shadow Register

Figure 30-86. MCANSS_IECS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
R/W-0h							R-0/W1C-0h

Table 30-139. MCANSS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EXT_TS_CNTR_OVFL	R-0/W1C	0h	External Timestamp Counter Overflow Interrupt Enable Clear. Reads always return a 0. 0 Write of '0' has no effect 1 Write of '1' clears the MCANSS_IES.EXT_TS_CNTR_OVFL bit

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61 MCANSS_IE Register (Offset = 7218h) [Reset = 00000000h]

MCANSS_IE is shown in Figure 30-87 and described in Table 30-80.

Return to the Summary Table.

MCAN Subsystem Interrupt Enable Register

Figure 30-87. MCANSS_IE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
R/W-0h							R/W1S-0h

Table 30-141. MCANSS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EXT_TS_CNTR_OVFL	R/W1S	0h	External Timestamp Counter Overflow Interrupt Enable. A write of '0' has no effect. A write of '1' sets the MCANSS_IES.EXT_TS_CNTR_OVFL bit.

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62 MCANSS_IES Register (Offset = 721Ch) [Reset = 00000000h]

MCANSS_IES is shown in Figure 30-88 and described in Table 30-81.

Return to the Summary Table.

MCAN Subsystem Interrupt Enable Status

Figure 30-88. MCANSS_IES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_TS_CNTR_OVFL
R-0h							R-0h

Table 30-143. MCANSS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow Interrupt Enable Status. To set, use the CANSS_IE.EXT_TS_CNTR_OVFL bit. To clear, use the MCANSS_IECS.EXT_TS_CNTR_OVFL bit. 0 External timestamp counter overflow interrupt is not enabled 1 External timestamp counter overflow interrupt is enabled

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63 MCANSS_EOI Register (Offset = 7220h) [Reset = 00000000h]

MCANSS_EOI is shown in Figure 30-89 and described in Table 30-82.

Return to the Summary Table.

MCAN Subsystem End of Interrupt

Figure 30-89. MCANSS_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOI							
R/W-0h																								R-0/W1S-0h							

Table 30-145. MCANSS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	EOI	R-0/W1S	0h	End of Interrupt. A write to this register will clear the associated interrupt. If the unserviced interrupt counter is > 1, another interrupt is generated. 0x00 External TS Interrupt is cleared 0x01 MCAN(0) interrupt is cleared 0x02 MCAN(1) interrupt is cleared Other writes are ignored.

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64 MCANSS_EXT_TS_PRESCALER Register (Offset = 7224h) [Reset = 00000000h]

MCANSS_EXT_TS_PRESCALER is shown in Figure 30-90 and described in Table 30-83.

Return to the Summary Table.

MCAN Subsystem External Timestamp Prescaler 0

Figure 30-90. MCANSS_EXT_TS_PRESCALER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRESCALER																							
R/W-0h								R/W-0h																							

Table 30-147. MCANSS_EXT_TS_PRESCALER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	
23-0	PRESCALER	R/W	0h	External Timestamp Prescaler Reload Value. The external timestamp count rate is the host (system) clock rate divided by this value, except in the case of 0. A zero value in this bit field will act identically to a value of 0x000001.

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65 MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 7228h) [Reset = 00000000h]

MCANSS_EXT_TS_UNSERVICED_INTR_CNTR is shown in Figure 30-91 and described in Table 30-84.

Return to the Summary Table.

MCAN Subsystem External Timestamp Unserviced Interrupts Counter

Figure 30-91. MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EXT_TS_INTR_CNTR				
R-0h			R-0h				

Table 30-149. MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	EXT_TS_INTR_CNTR	R	0h	External Timestamp Counter Unserviced Rollover Interrupts. If this value is > 1, an MCANSS_EOI write of '1' to bit 0 will issue another interrupt. The status of this bit field is affected by the MCANSS_IRS.EXT_TS_CNTR_OVFL bit field.

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66 MCANERR_REV Register (Offset = 7400h) [Reset = 66A0EA00h]

MCANERR_REV is shown in Figure 30-92 and described in Table 30-85.

Return to the Summary Table.

MCAN Error Aggregator Revision Register

Figure 30-92. MCANERR_REV Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		MODULE_ID			
R-1h		R-2h		R-6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R-6A0h							
15	14	13	12	11	10	9	8
RESERVED					REVMAJ		
R-1Dh					R-2h		
7	6	5	4	3	2	1	0
RESERVED		REVMIN					
R-0h		R-0h					

Table 30-151. MCANERR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	RESERVED	R	2h	Reserved
27-16	MODULE_ID	R	6A0h	Module Identification Number
15-11	RESERVED	R	1Dh	Reserved
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	RESERVED	R	0h	Reserved
5-0	REVMIN	R	0h	Minor Revision of the Error Aggregator

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67 MCANERR_VECTOR Register (Offset = 7408h) [Reset = 00000000h]

MCANERR_VECTOR is shown in Figure 30-93 and described in Table 30-86.

Return to the Summary Table.

Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address.

Figure 30-93. MCANERR_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-0h							R-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R-0/W1S-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

Table 30-153. MCANERR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	0h	
24	RD_SVBUS_DONE	R	0h	Read Completion Flag
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address Offset
15	RD_SVBUS	R-0/W1S	0h	Read Trigger
14-11	RESERVED	R/W	0h	
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID. Each error detection and correction (EDC) controller has a bank of error registers (offsets 0x10 - 0x3B) associated with it. These registers are accessed via an internal serial bus (SVBUS). To access them through the ECC aggregator the controller ID desired must be written to the ECC_VECTOR field, together with the RD_SVBUS trigger and RD_SVBUS_ADDRESS bit field. This initiates the serial read which consummates by setting the RD_SVBUS_DONE bit. At this point the addressed register may be read by a normal CPU read of the appropriate offset address. 0x000 Message RAM ECC controller is selected Others Reserved (do not use) Subsequent writes through the SVBUS (offsets 0x10 - 0x3B) have a delayed completion. To avoid conflicts, perform a read back of a register within this range after writing.

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68 MCANERR_STAT Register (Offset = 740Ch) [Reset = 00000002h]

MCANERR_STAT is shown in Figure 30-94 and described in Table 30-87.

Return to the Summary Table.

MCAN Error Misc Status

Figure 30-94. MCANERR_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-2h										

Table 30-155. MCANERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	
10-0	NUM_RAMS	R	2h	Number of RAMs. Number of ECC RAMs serviced by the aggregator.

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69 MCANERR_WRAP_REV Register (Offset = 7410h) [Reset = 66A46A02h]

MCANERR_WRAP_REV is shown in Figure 30-95 and described in Table 30-88.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-95. MCANERR_WRAP_REV Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		MODULE_ID			
R-1h		R-2h		R-6A4h			
23	22	21	20	19	18	17	16
MODULE_ID							
R-6A4h							
15	14	13	12	11	10	9	8
RESERVED					REVMAJ		
R-Dh					R-2h		
7	6	5	4	3	2	1	0
RESERVED		REVMIN					
R-0h		R-2h					

Table 30-157. MCANERR_WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID Register Scheme
29-28	RESERVED	R	2h	Reserved
27-16	MODULE_ID	R	6A4h	Module Identification Number
15-11	RESERVED	R	Dh	Reserved
10-8	REVMAJ	R	2h	Major Revision of the Error Aggregator
7-6	RESERVED	R	0h	Reserved
5-0	REVMIN	R	2h	Minor Revision of the Error Aggregator

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70 MCANERR_CTRL Register (Offset = 7414h) [Reset = 00000187h]

MCANERR_CTRL is shown in Figure 30-96 and described in Table 30-89.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-96. MCANERR_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							CHECK_SVBUS_TIMEOUT
R/W-0h							R/W-1h
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

Table 30-159. MCANERR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	CHECK_SVBUS_TIMEOUT	R/W	1h	Enables Serial VBUS timeout mechanism
7	RESERVED	R/W	1h	
6	ERROR_ONCE	R/W	0h	If this bit is set, the FORCE_SEC/FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent reads will not force an error.
5	FORCE_N_ROW	R/W	0h	Enable single/double-bit error on the next RAM read, regardless of the MCANERR_ERR_CTRL1.ECC_ROW setting. For write through mode, this applies to writes as well as reads.
4	FORCE_DED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
3	FORCE_SEC	R/W	0h	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted. For write through mode, this applies to writes as well as reads. MCANERR_ERR_CTRL1 and MCANERR_ERR_CTRL2 should be configured prior to setting this bit.
2	ENABLE_RMW	R/W	1h	Enable read-modify-write on partial word writes
1	ECC_CHECK	R/W	1h	Enable ECC Check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are '0'.
0	ECC_ENABLE	R/W	1h	Enable ECC Generation

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71 MCANERR_ERR_CTRL1 Register (Offset = 7418h) [Reset = 00000000h]

MCANERR_ERR_CTRL1 is shown in Figure 30-97 and described in Table 30-90.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-97. MCANERR_ERR_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW																															
R/W-0h																															

Table 30-161. MCANERR_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R/W	0h	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.

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72 MCANERR_ERR_CTRL2 Register (Offset = 741Ch) [Reset = 00000000h]

MCANERR_ERR_CTRL2 is shown in Figure 30-98 and described in Table 30-91.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-98. MCANERR_ERR_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT2																ECC_BIT1															
R/W-0h																R/W-0h															

Table 30-163. MCANERR_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT2	R/W	0h	Second column/data bit that needs to be flipped when FORCE_DED is set
15-0	ECC_BIT1	R/W	0h	Column/Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set

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73 MCANERR_ERR_STAT1 Register (Offset = 7420h) [Reset = 00000000h]

MCANERR_ERR_STAT1 is shown in Figure 30-99 and described in Table 30-92.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-99. MCANERR_ERR_STAT1 Register

31	30	29	28	27	26	25	24
ECC_BIT1							
R-0h							
23	22	21	20	19	18	17	16
ECC_BIT1							
R-0h							
15	14	13	12	11	10	9	8
CLR_CTRL_REG_ERROR	RESERVED		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC	
R/W1S-0h	R/W-0h		R/W1C-0h	R/WD-0h		R/WD-0h	
7	6	5	4	3	2	1	0
CTRL_REG_ERROR	RESERVED		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1S-0h	R/W-0h		R/W1S-0h	R/WI-0h		R/WI-0h	

Table 30-165. MCANERR_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R	0h	ECC Error Bit Position. Indicates the bit position in the RAM data that is in error on an SEC error. Only valid on an SEC error. 0 Bit 0 is in error 1 Bit 1 is in error 2 Bit 2 is in error 3 Bit 3 is in error ... 31 Bit 31 is in error >32 Invalid
15	CLR_CTRL_REG_ERROR	R/W1S	0h	Writing a '1' clears the CTRL_REG_ERROR bit
14-13	RESERVED	R/W	0h	
12	CLR_ECC_OTHER	R/W1C	0h	Writing a '1' clears the ECC_OTHER bit.
11-10	CLR_ECC_DED	R/WD	0h	Clear ECC_DED. A write of a non-zero value to this bit field decrements the ECC_DED bit field by the value provided.
9-8	CLR_ECC_SEC	R/WD	0h	Clear ECC_SEC. A write of a non-zero value to this bit field decrements the ECC_SEC bit field by the value provided.
7	CTRL_REG_ERROR	R/W1S	0h	Control Register Error. A bit field in the control register is in an ambiguous state. This means that the redundancy registers have detected a state where not all values are the same and has defaulted to the reset state. S/W needs to re-write these registers to a known state. A write of 1 will set this interrupt flag.
6-5	RESERVED	R/W	0h	
4	ECC_OTHER	R/W1S	0h	SEC While Writeback Error Status 0 No SEC error while writeback pending 1 Indicates that successive single-bit errors have occurred while a writeback is still pending

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Table 30-165. MCANERR_ERR_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	ECC_DED	R/WI	0h	Double Bit Error Detected Status. A 2-bit saturating counter of the number of DED errors that have occurred since last cleared. 0 No double-bit error detected 1 One double-bit error was detected 2 Two double-bit errors were detected 3 Three double-bit errors were detected A write of a non-zero value to this bit field increments it by the value provided.
1-0	ECC_SEC	R/WI	0h	Single Bit Error Corrected Status. A 2-bit saturating counter of the number of SEC errors that have occurred since last cleared. 0 No single-bit error detected 1 One single-bit error was detected and corrected 2 Two single-bit errors were detected and corrected 3 Three single-bit errors were detected and corrected A write of a non-zero value to this bit field increments it by the value provided.

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74 MCANERR_ERR_STAT2 Register (Offset = 7424h) [Reset = 00000000h]

MCANERR_ERR_STAT2 is shown in Figure 30-100 and described in Table 30-93.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-100. MCANERR_ERR_STAT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW																															
R-0h																															

Table 30-167. MCANERR_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R	0h	Indicates the row address where the single or double-bit error occurred. This value is address offset/4.

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75 MCANERR_ERR_STAT3 Register (Offset = 7428h) [Reset = 00000000h]

MCANERR_ERR_STAT3 is shown in Figure 30-101 and described in Table 30-94.

Return to the Summary Table.

This register is accessed through the ECC aggregator via an internal serial bus. To access, the appropriate procedure must be first followed in the MCAN ECC Vector Register.

Figure 30-101. MCANERR_ERR_STAT3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT	RESERVED
R/W-0h						R-0/W1C-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT	WB_PEND
R/W-0h						R-0/W1S-0h	R-0h

Table 30-169. MCANERR_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	CLR_SVBUS_TIMEOUT	R-0/W1C	0h	Write 1 to clear the Serial VBUS Timeout Flag
8-2	RESERVED	R/W	0h	
1	SVBUS_TIMEOUT	R-0/W1S	0h	Serial VBUS Timeout Flag. Write 1 to set.
0	WB_PEND	R	0h	Delayed Write Back Pending Status 0 No write back pending 1 An ECC data correction write back is pending

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76 MCANERR_SEC_EOI Register (Offset = 743Ch) [Reset = 00000000h]

MCANERR_SEC_EOI is shown in Figure 30-102 and described in Table 30-95.

Return to the Summary Table.

MCAN Single Error Corrected End of Interrupt Register

Figure 30-102. MCANERR_SEC_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-0h							R-0/W1S-0h

Table 30-171. MCANERR_SEC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EOI_WR	R-0/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_SEC goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

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77 MCANERR_SEC_STATUS Register (Offset = 7440h) [Reset = 00000000h]

MCANERR_SEC_STATUS is shown in Figure 30-103 and described in Table 30-96.

Return to the Summary Table.

MCAN Single Error Corrected Interrupt Status Register

Figure 30-103. MCANERR_SEC_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_PEND
R/W-0h							R-0-0h

Table 30-173. MCANERR_SEC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_PEND	R-0	0h	Message RAM SEC Interrupt Pending 0 No SEC interrupt is pending 1 SEC interrupt is pending

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78 MCANERR_SEC_ENABLE_SET Register (Offset = 7480h) [Reset = 00000000h]

MCANERR_SEC_ENABLE_SET is shown in Figure 30-104 and described in Table 30-97.

Return to the Summary Table.

MCAN Single Error Corrected Interrupt Enable Set Register

Figure 30-104. MCANERR_SEC_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_ENABLE_SET
R/W-0h							R/W1S-0h

Table 30-175. MCANERR_SEC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_ENABLE_SET	R/W1S	0h	Message RAM SEC Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

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79 MCANERR_SEC_ENABLE_CLR Register (Offset = 74C0h) [Reset = 00000000h]

MCANERR_SEC_ENABLE_CLR is shown in Figure 30-105 and described in Table 30-98.

Return to the Summary Table.

MCAN Single Error Corrected Interrupt Enable Clear Register

Figure 30-105. MCANERR_SEC_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_ENABLE_CLR
R/W-0h							R/W1C-0h

Table 30-177. MCANERR_SEC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_ENABLE_CLR	R/W1C	0h	Message RAM SEC Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM SEC error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

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80 MCANERR_DED_EOI Register (Offset = 753Ch) [Reset = 00000000h]

MCANERR_DED_EOI is shown in Figure 30-106 and described in Table 30-99.

Return to the Summary Table.

MCAN Double Error Detected End of Interrupt Register

Figure 30-106. MCANERR_DED_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-0h							R-0/W1S-0h

Table 30-179. MCANERR_DED_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	EOI_WR	R-0/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. Note that a write to the MCANERR_ERR_STAT1.CLR_ECC_DED goes through the SVBUS and has a delayed completion. To avoid an additional interrupt, read the MCANERR_ERR_STAT1 register back prior to writing to this bit field.

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81 MCANERR_DED_STATUS Register (Offset = 7540h) [Reset = 00000000h]

MCANERR_DED_STATUS is shown in Figure 30-107 and described in Table 30-100.

Return to the Summary Table.

MCAN Double Error Detected Interrupt Status Register

Figure 30-107. MCANERR_DED_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_PEND
R/W-0h							R-0-0h

Table 30-181. MCANERR_DED_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_PEND	R-0	0h	Message RAM DED Interrupt Pending 0 No DED interrupt is pending 1 DED interrupt is pending

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82 MCANERR_DED_ENABLE_SET Register (Offset = 7580h) [Reset = 00000000h]

MCANERR_DED_ENABLE_SET is shown in Figure 30-108 and described in Table 30-101.

Return to the Summary Table.

MCAN Double Error Detected Interrupt Enable Set Register

Figure 30-108. MCANERR_DED_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_ENABLE_SET
R/W-0h							R/W1S-0h

Table 30-183. MCANERR_DED_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_ENABLE_SET	R/W1S	0h	Message RAM DED Interrupt Pending Enable Set. Writing a 1 to this bit enables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

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83 MCANERR_DED_ENABLE_CLR Register (Offset = 75C0h) [Reset = 00000000h]

MCANERR_DED_ENABLE_CLR is shown in Figure 30-109 and described in Table 30-102.

Return to the Summary Table.

MCAN Double Error Detected Interrupt Enable Clear Register

Figure 30-109. MCANERR_DED_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MSGMEM_ENABLE_CLR
R/W-0h							R/W1C-0h

Table 30-185. MCANERR_DED_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	
0	MSGMEM_ENABLE_CLR	R/W1C	0h	Message RAM DED Interrupt Pending Enable Clear. Writing a 1 to this bit disables the Message RAM DED error interrupts. Writing a 0 has no effect. Reads return the corresponding enable bit's current value.

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84 MCANERR_AGGR_ENABLE_SET Register (Offset = 7600h) [Reset = 00000000h]

MCANERR_AGGR_ENABLE_SET is shown in Figure 30-110 and described in Table 30-103.

Return to the Summary Table.

MCAN Error Aggregator Enable Set Register

Figure 30-110. MCANERR_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLE_TIMEOUT_SET	ENABLE_PARITY_SET
R/W-0h						R/W1S-0h	R/W1S-0h

Table 30-187. MCANERR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	ENABLE_TIMEOUT_SET	R/W1S	0h	Write 1 to enable timeout errors. Reads return the corresponding enable bit's current value.
0	ENABLE_PARITY_SET	R/W1S	0h	Write 1 to enable parity errors. Reads return the corresponding enable bit's current value.

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85 MCANERR_AGGR_ENABLE_CLR Register (Offset = 7604h) [Reset = 00000000h]

MCANERR_AGGR_ENABLE_CLR is shown in Figure 30-111 and described in Table 30-104.

Return to the Summary Table.

MCAN Error Aggregator Enable Clear Register

Figure 30-111. MCANERR_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLE_TIMEOUT_CLR	ENABLE_PARITY_CLR
R/W-0h						R/W1C-0h	R/W1C-0h

Table 30-189. MCANERR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	ENABLE_TIMEOUT_CLR	R/W1C	0h	Write 1 to disable timeout errors. Reads return the corresponding enable bit's current value.
0	ENABLE_PARITY_CLR	R/W1C	0h	Write 1 to disable parity errors. Reads return the corresponding enable bit's current value.

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86 MCANERR_AGGR_STATUS_SET Register (Offset = 7608h) [Reset = 00000000h]

MCANERR_AGGR_STATUS_SET is shown in Figure 30-112 and described in Table 30-105.

Return to the Summary Table.

MCAN Error Aggregator Status Set Register

Figure 30-112. MCANERR_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				SVBUS_TIMEOUT		AGGR_PARITY_ERR	
R/W-0h				R/WI-0h		R/WI-0h	

Table 30-191. MCANERR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3-2	SVBUS_TIMEOUT	R/WI	0h	Aggregator Serial VBUS Timeout Error Status 2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared. 0 No timeout errors have occurred 1 One timeout error has occurred 2 Two timeout errors have occurred 3 Three timeout errors have occurred A write of a non-zero value to this bit field increments it by the value provided.
1-0	AGGR_PARITY_ERR	R/WI	0h	Aggregator Parity Error Status 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0 No parity errors have occurred 1 One parity error has occurred 2 Two parity errors have occurred 3 Three parity errors have occurred A write of a non-zero value to this bit field increments it by the value provided.

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87 MCANERR_AGGR_STATUS_CLR Register (Offset = 760Ch) [Reset = 00000000h]

MCANERR_AGGR_STATUS_CLR is shown in Figure 30-113 and described in Table 30-106.

Return to the Summary Table.

MCAN Error Aggregator Status Clear Register

Figure 30-113. MCANERR_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				SVBUS_TIMEOUT		AGGR_PARITY_ERR	
R/W-0h				R/WD-0h		R/WD-0h	

Table 30-193. MCANERR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3-2	SVBUS_TIMEOUT	R/WD	0h	Aggregator Serial VBUS Timeout Error Status 2-bit saturating counter of the number of SVBUS timeout errors that have occurred since last cleared. 0 No timeout errors have occurred 1 One timeout error has occurred 2 Two timeout errors have occurred 3 Three timeout errors have occurred A write of a non-zero value to this bit field decrements it by the value provided.
1-0	AGGR_PARITY_ERR	R/WD	0h	Aggregator Parity Error Status 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0 No parity errors have occurred 1 One parity error has occurred 2 Two parity errors have occurred 3 Three parity errors have occurred A write of a non-zero value to this bit field decrements it by the value provided.

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88 IIDX Register (Offset = 7820h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 30-114 and described in Table 30-107.

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This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 30-114. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 30-195. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending. 1h = MCAN Interrupt Line 0 interrupt pending. 2h = MCAN Interrupt Line 1 interrupt pending. 3h = Message RAM SEC (Single Error Correction) interrupt pending. 4h = Message RAM DED (Double Error Detection) interrupt pending. 5h = External Timestamp Counter Overflow interrupt pending. 6h = Clock Stop Wake Up interrupt pending.

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89 IMASK Register (Offset = 7828h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 30-115 and described in Table 30-108.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 30-115. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		WAKEUP	EXT_TS_CNTR_OVFL	DED	SEC	INTL1	INTL0
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 30-197. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	WAKEUP	R/W	0h	Clock Stop Wake Up interrupt mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
4	EXT_TS_CNTR_OVFL	R/W	0h	External Timestamp Counter Overflow interrupt mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
3	DED	R/W	0h	Massage RAM DED interrupt mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
2	SEC	R/W	0h	Message RAM SEC interrupt mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
1	INTL1	R/W	0h	MCAN Interrupt Line 1 mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask
0	INTL0	R/W	0h	MCAN Interrupt Line 0 mask. 0h = Clear Interrupt Mask 1h = Set Interrrupt Mask

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90 RIS Register (Offset = 7830h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 30-116 and described in Table 30-109.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 30-116. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		WAKEUP	EXT_TS_CNTR_OVFL	DED	SEC	INTL1	INTL0
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 30-199. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	
5	WAKEUP	R	0h	Clock Stop Wake Up interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_CNTR_OVFL	R	0h	External Timestamp Counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

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91 MIS Register (Offset = 7838h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 30-117 and described in Table 30-110.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 30-117. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		WAKEUP	EXT_TS_CNTR_OVFL	DED	SEC	INTL1	INTL0
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 30-201. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	
5	WAKEUP	R	0h	Masked Clock Stop Wake Up interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
4	EXT_TS_CNTR_OVFL	R	0h	Masked External Timestamp Counter Overflow interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
3	DED	R	0h	Masked Message RAM DED interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
2	SEC	R	0h	Masked Message RAM SEC interrupt. 0h = Interrupt did not occur 1h = Interrupt occured
1	INTL1	R	0h	Masked MCAN Interrupt Line 1. 0h = Interrupt did not occur 1h = Interrupt occured
0	INTL0	R	0h	Masked MCAN Interrupt Line 0. 0h = Interrupt did not occur 1h = Interrupt occured

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92 ISET Register (Offset = 7840h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 30-118 and described in Table 30-111.

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Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 30-118. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED		WAKEUP	EXT_TS_CNTR_OVFL	DED	SEC	INTL1	INTL0
W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 30-203. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	W	0h	
5	WAKEUP	W	0h	Set Clock Stop Wake Up interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
4	EXT_TS_CNTR_OVFL	W	0h	Set External Timestamp Counter Overflow interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
3	DED	W	0h	Set Message RAM DED interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
2	SEC	W	0h	Set Message RAM SEC interrupt. 0h = Writing 0 has no effect 1h = Set Interrupt
1	INTL1	W	0h	Set MCAN Interrupt Line 1. 0h = Writing 0 has no effect 1h = Set Interrupt
0	INTL0	W	0h	Set MCAN Interrupt Line 0. 0h = Writing 0 has no effect 1h = Set Interrupt

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93 ICLR Register (Offset = 7848h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 30-119 and described in Table 30-112.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 30-119. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED		WAKEUP	EXT_TS_CNTR_OVFL	DED	SEC	INTL1	INTL0
W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 30-205. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	W	0h	
5	WAKEUP	W	0h	Clear Clock Stop Wake Up interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	EXT_TS_CNTR_OVFL	W	0h	Clear External Timestamp Counter Overflow interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	DED	W	0h	Clear Message RAM DED interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
2	SEC	W	0h	Clear Message RAM SEC interrupt. 0h = Writing 0 has no effect 1h = Clear Interrupt
1	INTL1	W	0h	Clear MCAN Interrupt Line 1. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	INTL0	W	0h	Clear MCAN Interrupt Line 0. 0h = Writing 0 has no effect 1h = Clear Interrupt

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94 EVT_MODE Register (Offset = 78E0h) [Reset = 00000000h]

EVT_MODE is shown in Figure 30-120 and described in Table 30-113.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 30-120. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						INT0_CFG	
R/W-0h						R-0h	

Table 30-207. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	INT0_CFG	R	1h	Event line mode select for event corresponding to [IPSTANDARD.CPU_INT] 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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95 DESC Register (Offset = 78FCh) [Reset = 00000000h]

DESC is shown in Figure 30-121 and described in Table 30-114.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 30-121. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				RESERVED				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 30-209. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	940h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness. 0h = Smallest value FFFFh = Highest possible value
15-12	FEATUREVER	R	0h	Feature Set for the module *instance* 0h = MCAN module with CAN-FD mode enabled 1h = MCAN module with CAN-FD mode disabled
11-8	RESERVED	R	0h	
7-4	MAJREV	R	0h	Major rev of the IP 0h = Smallest value Fh = Highest possible value
3-0	MINREV	R	0h	Minor rev of the IP 0h = Smallest value Fh = Highest possible value

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96 MCANSS_CLKEN Register (Offset = 7900h) [Reset = 00000000h]

MCANSS_CLKEN is shown in Figure 30-122 and described in Table 30-115.

Return to the Summary Table.

MCAN module clock (functional clock and Vbusp to access MCAN module MMRs) enable register

Figure 30-122. MCANSS_CLKEN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_REQEN
R-0h							-0

Table 30-211. MCANSS_CLKEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	
0	CLK_REQEN	0h	MCAN functional and MCAN/ MCANSS MMR clock request enable bit 0h = MCAN module functional clock and Vbusp is not requested. These clocks are gated to the MCAN module. 1h = Setting this bit requests MCAN module functional clock and Vbusp. These clocks are not gated to MCAN module.	

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97 MCANSS_CLKDIV Register (Offset = 7904h) [Reset = 00000000h]

MCANSS_CLKDIV is shown in Figure 30-123 and described in Table 30-116.

Return to the Summary Table.

Needs to go to the Management apperture once available

Figure 30-123. MCANSS_CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														RATIO	
R/W-0h														R/W-0h	

Table 30-213. MCANSS_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	RATIO	R/W	0h	Clock divide ratio specification. Enables configuring clock divide settings for the MCAN functional clock input to the MCAN-SS. 0h (R/W) = Divides input clock by 1 1h (R/W) = Divides input clock by 2 2h (R/W) = Divides input clock by 4 3h (R/W) = Divides input clock by 1

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98 MCANSS_CLKCTL Register (Offset = 7908h) [Reset = 00000000h]

MCANSS_CLKCTL is shown in Figure 30-124 and described in Table 30-117.

Return to the Summary Table.

MCANSS clock stop control MMR.
Bus clock for the wrapper MMRs (including this MMR) is not gated by this register settings.

Figure 30-124. MCANSS_CLKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							WKUP_GLTFLT_EN
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED			WAKEUP_INT_EN	RESERVED			STOPREQ
R/W-0h			R/W-0h	R/W-0h			R/W-0h

Table 30-215. MCANSS_CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	WKUP_GLTFLT_EN	R/W	0h	Setting this bit enables the glitch filter on MCAN RXD input, which wakes up the MCAN controller to exit clock gating. 0h = Disable glitch filter enable on RXD input when MCAN is in clock stop mode (waiting for event on RXD input for clock stop wakeup). 1h = Enable glitch filter enable on RXD input when MCAN is in clock stop mode (waiting for event on RXD input for clock stop wakeup).
7-5	RESERVED	R/W	0h	
4	WAKEUP_INT_EN	R/W	0h	This bit contols enabling or disabling the MCAN IP clock stop wakeup interrupt (when MCANSS_CTRL.WAKEUPREQEN wakeup request is enabled to wakeup MCAN IP upon CAN RXD activity) 0h = Disable MCAN IP clock stop wakeup interrupt 1h = Enable MCAN IP clock stop wakeup interrupt
3-1	RESERVED	R/W	0h	
0	STOPREQ	R/W	0h	This bit is used to enable/disable MCAN clock (both host clock and functional clock) gating request. Note: This bit can be reset by HW by Clock-Stop Wake-up via CAN RX Activity. See spec for more details. 0h = Disable MCAN-SS clock stop request 1h = Enable MCAN-SS clock stop request

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99 MCANSS_CLKSTS Register (Offset = 790Ch) [Reset = 00000000h]

MCANSS_CLKSTS is shown in Figure 30-125 and described in Table 30-118.

Return to the Summary Table.

MCANSS clock stop status register to indicate status of clock stop mechanism

Figure 30-125. MCANSS_CLKSTS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CCLKDONE
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED			STOPREQ_HW_OVR	RESERVED			CLKSTOP_ACKSTS
R-0h			R-0h	R-0h			R-0h

Table 30-217. MCANSS_CLKSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	CCLKDONE	R	0h	This bit indicates the status of MCAN contoller clock request from GPRCM. 0h = MCAN controller clock is not available to the MCAN IP. 1h = MCAN controller clock is enabled and available to the MCAN IP.
7-5	RESERVED	R	0h	
4	STOPREQ_HW_OVR	R	0h	MCANSS clock stop HW override status bit. This bit indicates when the MCANSS_CLKCTL.STOPREQ bit has been cleared by HW when a clock-stop wake-up event via CAN RX activity is triggered. 0h = MCANSS_CLKCTL.STOPREQ bit has not been cleared by HW. 1h = MCANSS_CLKCTL.STOPREQ bit has been cleared by HW.
3-1	RESERVED	R	0h	
0	CLKSTOP_ACKSTS	R	0h	Clock stop acknowledge status from MCAN IP 0h = No clock stop acknowledged. 1h = Clock stop has been acknowledged by MCAN IP MCAN-SS may be clock gated by stopping both the CAN host and functional clocks.

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Chapter 31

Unified Communication Peripheral (UNICOMM)

UNICOMM is a run-time configurable unified communications module capable of supporting either a UART, I^2C or SPI protocol. Certain UNICOMM variants provide extended support for LIN and SMBus protocols.

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31.1 Overview

UNICOMM is a unified serial communication peripheral capable of operating in multiple different standard serial protocols including UART, SPI, and I2C. Register settings configure which protocol is selected for a given UNICOMM peripheral instance via the IPMODE field. A UNICOMM instance can only be configured for one protocol mode at a time.

Each UNICOMM instance can be configured to operate in one of the following protocol modes:

- UART - Universal Asychronous Receiver/Transmitter
- SPI - Serial Peripheral Interface
- I2CC - Inter Integrated Circuit Controller
- I2CT - Inter Integrated Circuit Target

This document commonly uses the abbreviation UCx to refer to a specific UNICOMM instance, with x being the instance number (for example, UC3 refers to the 3rd UNICOMM instance.) Individual UNICOMM instances are grouped together into designated Scalable Peripheral Groupings (SPGs) for high level configurations such as loopback modes and I2C pairings. Each grouping uses the naming scheme SPGx (or Sx in the UNICOMM register blocks) where x represents the group number the UNICOMM instance belongs to.

There are six UNICOMM instances grouped in two SPG instances present on this device. Below are the configuration options and peripheral types available for each UNICOMM instance. UNICOMM instances UC0, UC1 and UC2 are grouped into SPG0/S0 and instances UC3, UC4, and UC5 are grouped together in SPG1/S1.

Table 31-1. Available UNICOMM Configurations Per Instance

SPG Instance	UNICOMM Instance	Supported Serial Protocols	Available Peripheral Types
SPG0	UC0	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC1	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC2	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target
SPG1	UC3	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC4	UART, SPI, I2C	Basic UART, Basic SPI, Basic I2C Controller/Target
	UC5	UART, LIN, I2C, SMBUS	Basic+ UART, Advanced I2C Controller/Target

This chapter describes all the features and configurations that are common across all UNICOMM instances regardless of the IPMODE configured. This includes FIFO operation, enabling and resetting a UNICOMM instance, the generic transmit and receive sequence, and generic initialization sequence for UNICOMM.

There are also two test mode features, loopback and I2C pairing, that involve interaction between two or more UNICOMM instances. This chapter begins by describing these top-level test features, and their dependance on the UNICOMM's SPG (Scalable Peripheral Group).

The detailed and protocol-specific operation of each UNICOMM protocol mode is described in each of the below dedicated chapters:

- UART - Section 32
- SPI - Section 34
- I2CC / I2CT - Section 33

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31.1.1 Block Diagram

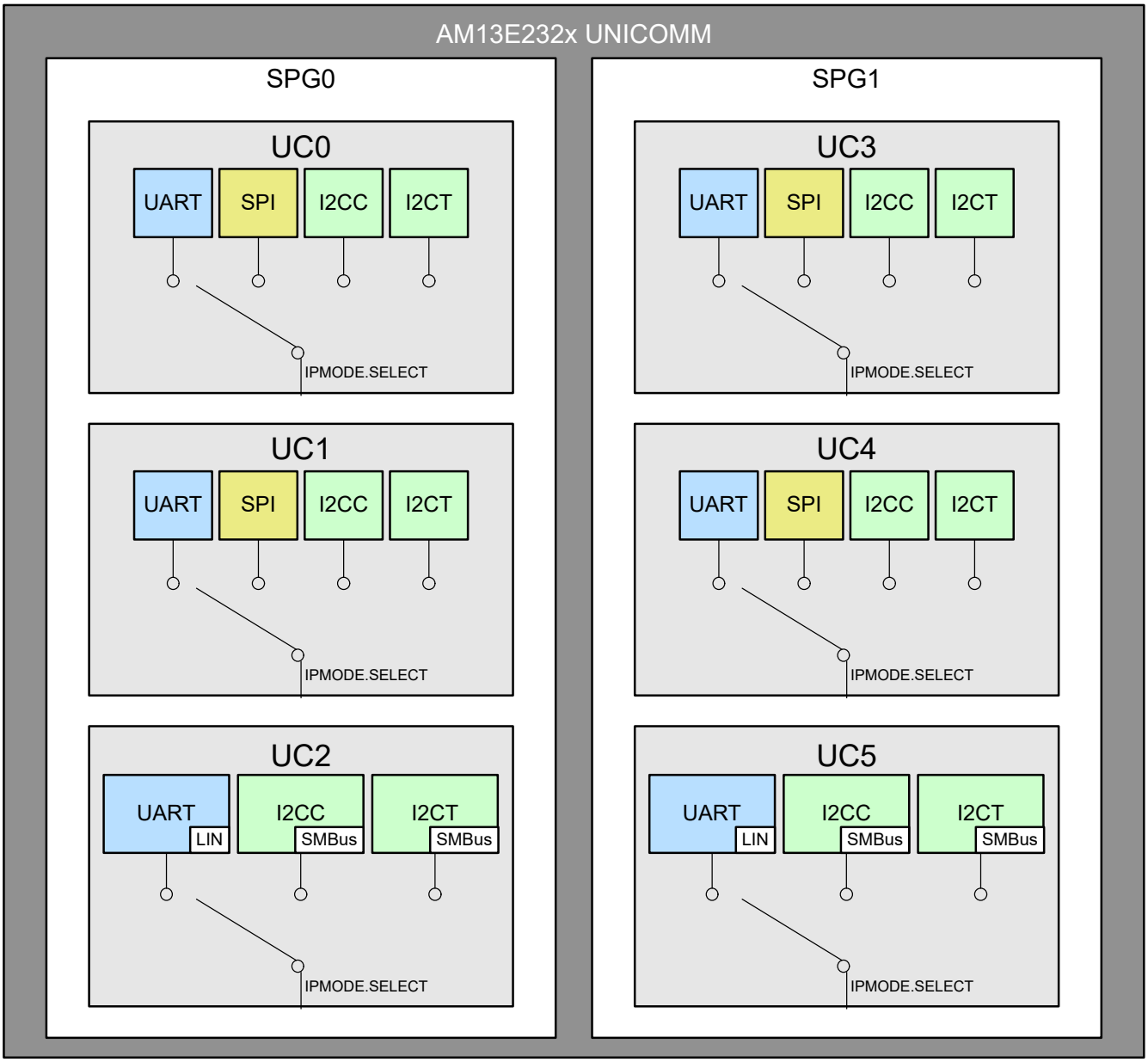


Figure 31-1. Unicomm Block Diagram

31.2 Unicomm Architecture

31.2.1 Scalable Peripheral Group (SPG) Configurations

The Scalable Peripheral Group (SPG) level configurations consist internal loopback operation and I2C pairing operation in compliance with the SMBUS protocol.

Note

Users not employing either of the loopback or I2C pairing test fetures can skip to Section 31.2.2 .

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31.2.1.1 Loopback Operation

UNICOMM supports a multiple self-test modes which internally connect the output UNICOMM signals to the input UNICOMM signals. This mode is helpful for initial code development and debugging. There are two types of internal loopback modes in UNICOMM, internal loopback and inter-module internal loopback. Figure 31-2 shows an example of these two loopback setups with UNICOMM UART, as well as an external loopback hardware setup example.

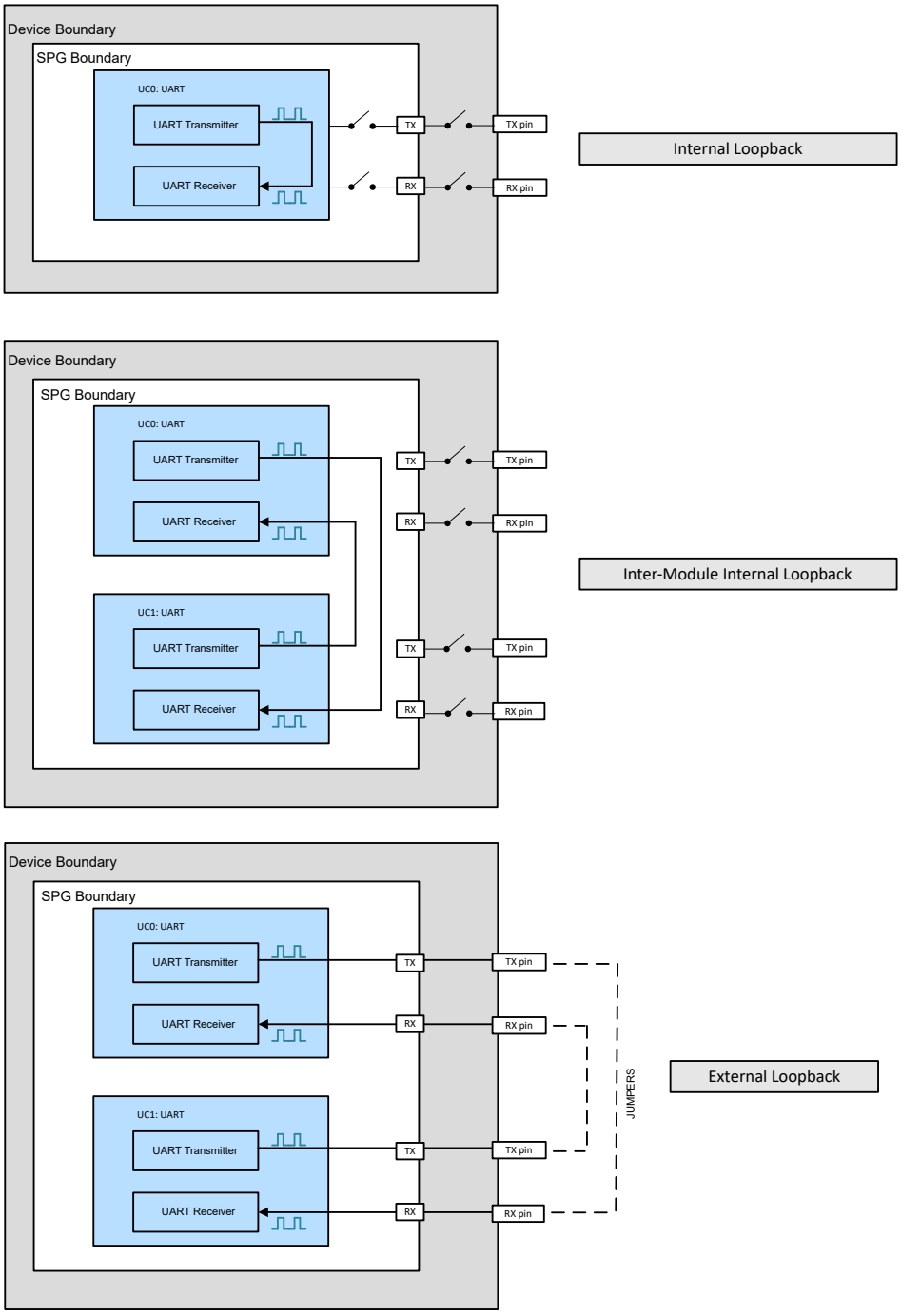


Figure 31-2. UNICOMM Loopback Types

Internal Loopback

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For UNICOMM instances configured as UART or SPI, internal loopback within a *single* UNICOMM instance is available. The configuration for this mode is done in the UNICOMMUART_REGS and the UNICOMMSPI_REGS; see UART Internal Loopback and SPI Internal Loopback sections in the corresponding peripheral chapters.

- UART
  - UCi TX signal / UCi RX signal
- SPI
  - UCi SCLK signal / UCi SCLK signal
  - UCi SDO signal / UCi SDI signal
  - UCi SDI signal / UCi SDO signal

Inter-Module Internal Loopback

Inter-module internal loopback is available between *two different* UNICOMM instances configured for the same communication type that are in the same SPG group. The Figure 31-1 shows which UC instances belong in each SPG grouping. In this loopback method, the following signals are connected between two different UC instances, represented as "i" and "j" below. Inter-module internal loopback is configured in the LPBKx.CONTROLLER and LPBKx.PERIPHERAL fields of the LPBKx registers. Then, enable the loopback pair by setting the EN bit in the LPBKx register. There is one configurable loopback pair available for each UNICOMM group on this device.

- UART
  - UCi TX signal / UCj RX signal
- SPI
  - UCi CS0 signal / UCj CS0 signal
  - UCi SCLK signal / UCj SCLK signal
  - UCi SDO signal / UCj SDI signal
  - UCi SDI signal / UCj SDO signal
- I2C
  - UCi SCL signal / UCj SCL signal
  - UCi SDA signal / UCj SDA signal

External Loopback

Additionally, users can configure any two UNICOMM instances in the UART IPMODE and connect the signals externally to validate the hardware setup. This requires no specific loopback configurations in any of the UNICOMM registers since the loopback is done external to the device.

UART

- UCi TX signal / UCj RX signal

Note

When two UC instances are configured as an internal loopback pair (internal or inter-module internal), the associated signals are not brought out to device pins.

31.2.1.2 I2C Pairings

I2C paring supports specialized I2C modes where multiple controllers or a I2CC/I2CT pair are connected to a single external bus. Multi-controller configurations and protocols like SMBus/PMBus require this setup. I2C pairing is available between two UNICOMM instances when both of the below are true:

1. Both UNICOMM modules are configured for I2C communication in the IPMODE register. Controller-Controller and Controller-Target pairing are supported.
2. Both UNICOMM modules belong to the same SPG instance. Check the Figure 31-1 to see which SPG instance the UNICOMM instance belongs to.

I2C pairing connects the SDA line to the SDA line and the SCL line to the SCL line between two different UNICOMM instances inside the same scalable peripheral group (SPG). The I2C pairing control is set through the PAIRx registers.

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To create an I2C pair within an SPG:

1. Select the UNICOMM to be used as the first I2C (I2CC) in the pair and find the index number of the SPG the UNICOMM instance belongs to.
2. Select the UNICOMM to be used as the second I2C (I2CC or I2CT) in the pair and verify that the index number of the SPG for the UNICOMM matches that of the SPG index from number 1 (for example: both from SPG0).
3. Write the local UNICOMM index (relative to each SPG) of the *first* instance to PAIRx.CTL.
    a. The local index of UC0 and UC3 is 0x0
    b. The local index of UC1 and UC4 is 0x1
    c. The local index of UC2 and UC5 is 0x2
4. Write the local UNICOMM index (relative to each SPG) of the *second* instance to PAIRx.TARGET.
    a. The local index of UC0 and UC3 is 0x0
    b. The local index of UC1 and UC4 is 0x1
    c. The local index of UC2 and UC5 is 0x2
5. Enable the loopback by writing a '1' to PAIRx.EN.

I2C pairing functions similar to a loopback, except for that the SDA/SCL signals propogate to the device pins. When an I2C pair is enabled, the SDA/SCL signals associated with the UNICOMM module defined in PAIR.TARGET propogates and the UNICOMM module defined in PAIR.CTL is driven IDLE.

31.2.2 FIFO Operation

Each UNICOMM peripheral has two dedicated 16-level FIFOs, one for receive operations and one for transmit operations. The FIFOs reduce service overhead by effeciently storing data to be sent while the transmitter is busy or storing received data to be processed while the CPU is busy. The TXDATA and RXDATA registers are used to interface with the transmit and receive FIFOs respectively.

The FIFO level for each UNICOMM instance is configured in the IFLS register within the peripheral-specific interface registers, even though the configuration options are the same across all IP modes.

31.2.2.1 Receive FIFO Levels

The configurable FIFO condition options for the Receive (RX) FIFO are:

- FIFO is full
- FIFO is at least 1/16 full - "not empty"
- FIFO is ¼ full
- FIFO is ½ full
- FIFO is ¾ full
- FIFO is 15/16 full - "almost full"
- FIFO is 1/16 full - "almost empty"

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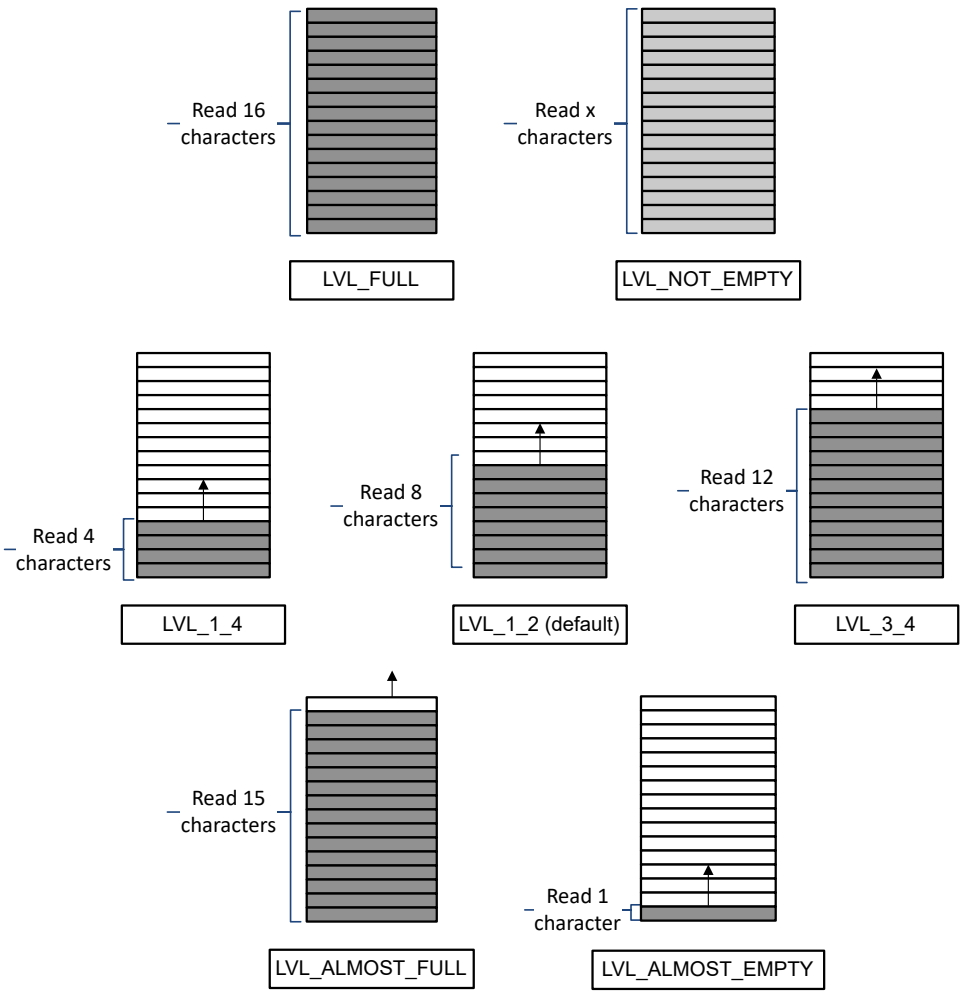


Figure 31-3. UNICOMM Receive FIFO Levels

These various conditions are typically used to generate a CPU_INT or DMA_TRIG_RX event where the CPU/RX subsequently reads a specific number of characters into memory from RXDATA. The number of characters read in each Interrupt Service Routine (ISR) equals how many are ensured present in the FIFO as indicated by the flag. Typically, the FIFO level is selected so that the CPU reads the largest number of characters possible in each ISR which is the highest possible even factor of the number of characters sent by the transmitting device in each frame. For the "not empty" condition, the application can read one element at a time while the condition is satisfied.

Note

Debugger reads of RXDATA have no effect on the contents in the RX FIFO.

31.2.2.2 Transmitter FIFO Levels

The configurable FIFO condition options for the Transmit (TX) FIFO are:

- FIFO is empty
- FIFO is at least 1/16 empty - "not full"
- FIFO is ¼ full
- FIFO is ½ full
- FIFO is ¾ full
- FIFO is 15/16 full - "almost full"
- FIFO is 1/16 full - "almost empty"

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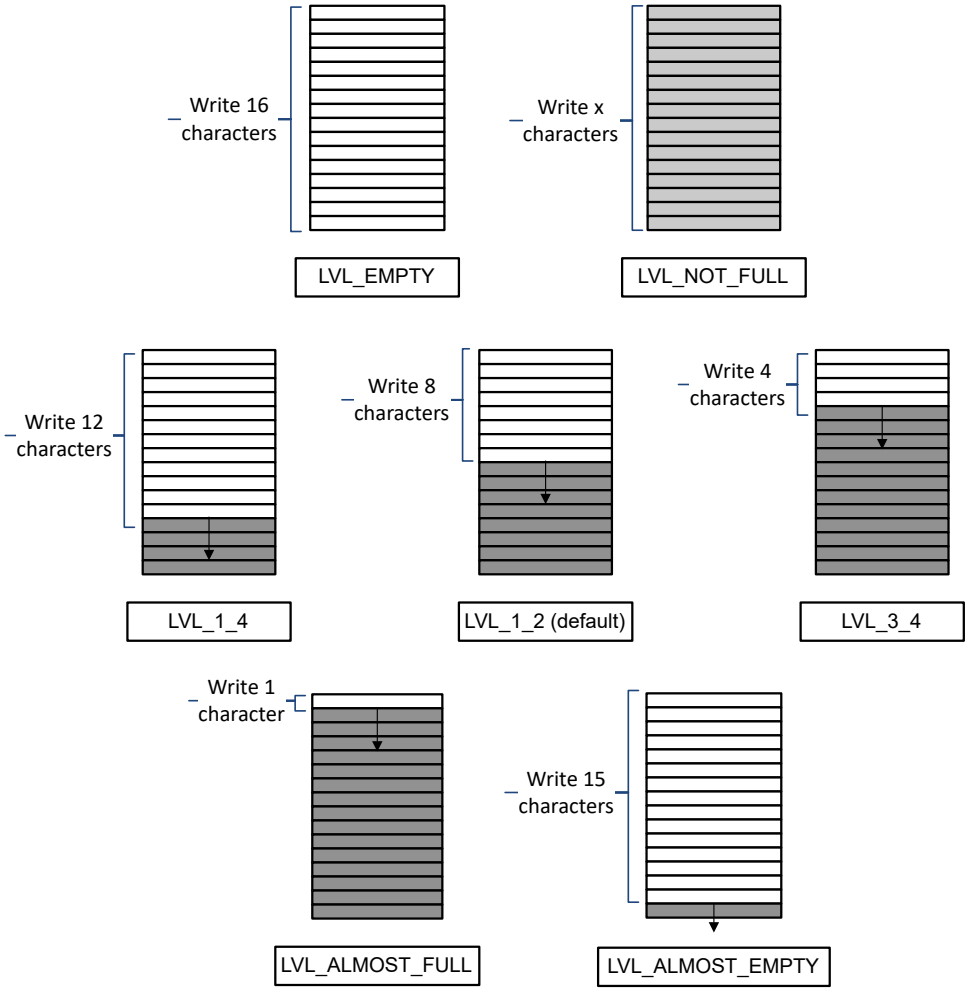


Figure 31-4. UNICOMM Transmit FIFO Levels

These various conditions are typically used to generate a CPU_INT or DMA_TRIG_TX event where the CPU/DMA subsequently writes a specific number of characters into the TXDATA register. The number of characters written in each Interrupt Service Routine (ISR) equals how many spots are ensured empty in the FIFO as indicated by the flag. Typically, the FIFO level is selected so that the CPU writes the largest number of characters possible in each ISR. Often this value is the highest possible even factor of the number of characters that are sent in each frame. For the "not full" condition, the application can write one element at a time while the condition is satisfied.

Note

Debugger writes of TXDATA will add elements to the TX FIFO the same as a CPU write.

31.2.2.3 Clearing FIFO Contents

Setting the IFLS.RXCLR and IFLS.TXCLR register bits clears the contents of each of the respective FIFOs. Follow the below sequence:

1. Write a 1 to the RXCLR or TXCLR bit in the IFLS peripheral-specific register.
2. Wait until the RXCLR or TXCLR status bit in the STAT register is set to 1.
3. Write a 0 to the RXCLR or TXCLR bit in the IFLS peripheral-specific register.

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Note

Performing the above clear sequence before changing the FIFO level configuration in the RXIFSEL or TXIFSEL fields is recommended.

Note

Avoid performing step 1 repeatedly before full sequence is complete.

31.2.2.4 FIFO Status Flags

Each of the common available FIFO status bits are explained in the table below. All status bits are included in the below registers for each UNICOMM peripheral and can be used by application software to poll the FIFO status as needed.

- UART - STAT register
- SPI - STAT register
- I2CC - SR register
- I2CT - SR register

Table 31-2. UNICOMM FIFO Status Bits

Status Bit	Description
RXFE	This bit is set when the RX FIFO is empty.
RXFF	This bit is set when the RX FIFO is full.
RXCLR	This bit is set when a clear of the RX FIFO, started by setting the IFLS.RXCLR bit, is complete.
TXFE	This bit is set when TX FIFO is empty.
TXFF	This bit is set when TX FIFO is full.
TXCLR	This bit is set when a clear of the TX FIFO, started by setting the IFLS.TXCLR bit, is complete.

31.2.3 Interrupts

Each UNICOMM peripheral contains standard interrupt registers: IIDX, IMASK, RIS, MIS, ISET and ICLR in the CPU_INT register group. These configuration, control, and status registers dictate how the UNICOMM module interfaces with the device interrupt controller module. Unique conditional flags are available in these registers to generate CPU interrupts for each specific peripheral mode (UART, SPI, I2CC, or I2CT). Each UNICOMM instance has one interrupt line connected to the interrupt controller.

31.2.3.1 Receive Interrupt Sequence

The receive interrupt flags for each peripheral specific UNICOMM instance are described below. These flags are raised when there is data present in the RX FIFO that is ready to be read by the CPU or DMA.

- UART - RXINT flag
- SPI - RX flag
- I2CC - RXTRG flag
- I2CT - RXTRG flag

Below is the high-level sequence for receiving a fixed amount of data with interrupts.

1. The RX FIFO contains greater than or equal to the number of bytes/words designated by the programmed trigger level in IFLS.RXIFSEL.
2. The interrupt flag for the configured peripheral mode is set and an interrupt is triggered on the CPU.
3. In the Interrupt Service Routine (ISR), the CPU reads the fixed amount of data from the RXDATA register (repeated reads). This data is then read from the RX FIFO automatically by hardware.

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Depending on the peripheral mode configured, additional steps before and/or after this sequence may be required to receive the data using the corresponding protocol. See the peripheral-specific UNICOMM chapters for more details about the software steps needed for each IP.

31.2.3.2 Transmit Interrupt Sequence

The transmit interrupt flags for each peripheral specific UNICOMM instance are described below. These flags are raised when there is space present in the TX FIFO for the CPU or DMA to write data.

- UART - TXINT flag
- SPI - TX flag
- I2CC - TXTRG flag
- I2CT - TXTRG flag

Below is the high-level sequence for transmitting a fixed amount of data with interrupts.

1. The TX FIFO contains less than or equal to the number of bytes/words designated by the programmed trigger level in IFLS.TXIFSEL.
2. The interrupt flag for the configured peripheral mode is set and an interrupt is triggered on the CPU.
3. In the Interrupt Service Routine (ISR), the CPU writes the fixed amount of data to the TXDATA register. This data is then written to the TX FIFO automatically by hardware.

Depending on the peripheral mode configured, additional steps before and/or after this sequence may be required to transmit the data using the corresponding protocol. See the peripheral-specific UNICOMM chapters for more details about the software steps needed for each IP.

31.2.4 DMA Operation

Each UNICOMM peripheral has access to the DMA module on the device and can be configured to trigger DMA channels. From the UNICOMM point-of-view, DMA triggers are setup through the registers in the DMA_TRIG_RX and DMA_TRIG_TX register groups. Different conditionals are available to trigger the DMA_TRIG_RX line and the DMA_TRIG_TX line depending on the IPMODE configured. See the below sections from the peripheral-specific chapters for the options available.

- UART mode DMA conditionals: UART DMA Event Support
- SPI mode DMA conditionals: SPI DMA Event Support
- I2CC/I2CT mode DMA conditionals: I2C DMA Event Support

Note

Some modules only have one available conditional per DMA line.

See Section 11.2.3 for how to configure one of the UNICOMM signals as the trigger source for a DMA channel in the DMA registers.

31.3 High-Level Initialization

Below are the generic intialization steps to configure a UNICOMM instance and the recommended order for software to execute these steps. Peripheral specific initializations are listed in the respective sections.

1. Put the UNICOMM instance into reset by setting the RSCTL.RESETASSERT register bit from the UNICOMM Registers.
2. Enable power to the UNICOMM instance by writing "0h26" to the KEY field and setting the EN bit for the PWREN register in the UNICOMM_REGS registers. Wait four or more cycles after this is set before writing to the individual peripheral registers.
3. Configure the peripheral mode for the UCx instance in the IPMODE.SELECT field from the UNICOMM_REGS registers to operate as a UART, SPI, I2C Controller, or I2C Target.
4. Enable the pin functionality for each GPIO being used in the peripheral configuration in the IOMUX_REGS registers. See the Section 16 section for more information.

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Note

IOMUX configurations must be done after the peripheral mode (IPMODE.SELECT) is configured (previous step).

5. (Optionally) Configure the inter-module internal loopback/pairing settings in the SPG_REGS registers between two UCx modules in the same SPG. See Figure 31-1 to determine which UCx pairings are available on this device.
   a. Configure the loopback pairs (maximum of one pair per SPG module) in the LPBKx register field.
   b. Configure the I2C pairs (maximum of one pair per SPG module) in the PAIRx register field.
6. Configure the below settings in the UNICOMMUART_REGS / UNICOMMSPI_REGS / UNICOMMI2CC_REGS / UNICOMMI2CT_REGS registers .
   a. To enable clocking of the UNICOMM module, configure the clock source in the CLKSEL register to be MCLKDIV2, the functional clock of UNICOMM.
   b. Configure the clock divider for the UNICOMM instance's peripheral-specific functional clock in the CLKDIV.RATIO register field. This decides how much to divide down the overall UNICOMM clock source for each specific UNICOMM instance clock.
   c. Perform peripheral-specific initializations (example: SPI peripheral vs. controller mode, UART baud rate etc.) Follow the detailed steps in in the UART Initialization, SPI Initialization, I2C Controller Initialization, and I2C Target Initialization chapters.

31.4 Enables & Resets

Each UNICOMM instance (UCx) has a dedicated reset and enable bitfield in the UNICOMM_REGS register group.

The UNICOMM instance can be reset by writing a 1 to the RSTCTL.RESETASSERT bit. Writing this field resets the internal state of the UCx module, all configuration registers for the UC instance and the UC peripheral, and clears all of the FIFOs. The STAT.RESETKY bit is set once the UCx module has undergone a reset. To clear the RESETKY bit, write to RSTCTL.RESETSTKYCLR bit and the RESETKY bit won't be set until the next reset is performed.

A UNICOMM instance can be enabled at the UCx level by setting the PWREN.ENABLE bit. Clocking of the UC peripheral-specific registers is not enabled until this PWREN.ENABLE bit is set. If no IPMODE has been selected, a write to these registers has no effect.

Software Reset Considerations

A software reset can be executed with setting the RESETASSERT together with the KEY in the RSTCTL register. An ongoing transfer is terminated immediately and can leave the software in an undefined state. Therefore, before requesting a reset, an ongoing transfer must be terminated.

Hardware Reset Considerations

A hardware reset also initializes the IO configuration. This sets the IOs to a high impedance state. If pull-up resistors are connected externally (for example in the case of UNICOMM-I2C), the IOs are pulled high on reset. If there are no pull-up resistors connected externally, the IOs float after a UNICOMM reset.

31.5 Suspending Communication

Each UNICOMM peripheral contains a SUSPEND bitfield, see the below registers for each module. When this bit is set, the module returns to an idle state and stops further communication on the external pins. The transmit line/lines are driven to the idle state and any further toggles on the receives line/lines are not processed. To suspend the module, follow the below steps.

1. Check that the UNICOMM module is in an IDLE state
   a. UNICOMM-UART
      i. STAT.BUSY needs to read '0'.
      ii. In LIN mode, if transmitting, the checksum needs to be loaded into the TX FIFO.

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iii. In LIN mode, if receiving, the checksum needs to be received from the RX FIFO.
iv. In idleline multiprocessor mode, if transmitting, all address and data bytes for the current frame need to be loaded into the TX FIFO
v. In idleline multiprocessor mode, if receiving, SR.IDLE needs to read '1'.
vi. If using RTS/CTS flow control, if transmitting, pull nRTS line high after TX FIFO is empty.
vii. If using RTS/CTS flow control, if receiving, pull nCTS line high after receiving the current byte.

b. UNICOMM-SPI
   - In Controller mode, CS needs to be idle.
   - In Peripheral mode, CS needs to read back as idle.

c. UNICOMM-I2CC
   - SR.BUSY needs to read '0'.
   - If transmitting, the receiving target must send a NACK
   - If receiving, NACK must be sent on the line
   - In multi-controller mode, STOP condition needs to be sent on the line

d. UNICOMM-I2CT
   - SR.BUSY needs to read '0'.
   - If transmitting, receiving controller must send a NACK
   - If receiving and clock stretching is enabled, NACK must be sent on the line
   - If receiving and clock stetching is disabled, transmitting controller must send a STOP or address a different target

2. Set the SUSPEND bit
   a. UNICOMM-UART: LCRH.SUSPEND=1
   b. UNICOMM-SPI: CTL1.SUSPEND=1
   c. UNICOMM-I2CC: CTR.SUSPEND=1
   d. UNICOMM-I2CT: CTR.SUSPEND=1
3. Clear the RX FIFO
4. Disable the module
   a. UNICOMM-UART: CTL0.ENABLE=0
   b. UNICOMM-SPI: CTL1.ENABLE=0
   c. UNICOMM-I2CC: CTR.ENABLE=0
   d. UNICOMM-I2CT: CR.ENABLE=0

Note

Before re-enabling the UNICOMM module, the SUSPEND bit needs to be cleared.

31.6 UNICOMM Interrupts & Triggers

31.6.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 31-3. CPU Interrupts Triggered by UNICOMM

NVIC Interrupt Name	Peripheral Instance Name	Register Group	UNICOMM Interrupt Configuration Registers	Description
UNICOMM0.CPU_INT	UNICOMM0	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM0 interrupt. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.

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Table 31-3. CPU Interrupts Triggered by UNICOMM (continued)

NVIC Interrupt Name	Peripheral Instance Name	Register Group	UNICOMM Interrupt Configuration Registers	Description
UNICOMM1.CPU_INT	UNICOMM1	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM1 interrupt. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.
UNICOMM2.CPU_INT	UNICOMM2	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM2 interrupt. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.
UNICOMM3.CPU_INT	UNICOMM3	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM3 interrupt. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.
UNICOMM4.CPU_INT	UNICOMM4	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM4 interrupt. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.
UNICOMM5.CPU_INT	UNICOMM5	CPU_INT	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET, [IPMODE.SELECT].ICLR	UNICOMM5 interrupt. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. Multiple OR'd, configurable source conditions.

31.6.2 DMA Triggers

See the Section 11.2.3 section for more details about how to configure DMA triggers for individual DMA channels.

Table 31-4. DMA Triggers from the UNICOMM

Trigger Name	Peripheral Instance Name	Register Group	UNICOMM DMA Configuration Registers	Description
UNICOMM0.DMA_TRIG_TX	UNICOMM0	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM0 Transmit DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.

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Table 31-4. DMA Triggers from the UNICOMM (continued)

Trigger Name	Peripheral Instance Name	Register Group	UNICOMM DMA Configuration Registers	Description
UNICOMM0.DMA_TRIG_RX	UNICOMM0	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM0 Receive DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of SPI, I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.
UNICOMM1.DMA_TRIG_TX	UNICOMM1	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM1 Transmit DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.
UNICOMM1.DMA_TRIG_RX	UNICOMM1	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM1 Receive DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of SPI, I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.
UNICOMM2.DMA_TRIG_TX	UNICOMM2	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM2 Transmit DMA trigger. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.
UNICOMM2.DMA_TRIG_RX	UNICOMM2	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM2 Receive DMA trigger. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.

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Table 31-4. DMA Triggers from the UNICOMM (continued)

Trigger Name	Peripheral Instance Name	Register Group	UNICOMM DMA Configuration Registers	Description
UNICOMM3.DMA_TRIG_TX	UNICOMM3	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM3 Transmit DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.
UNICOMM3.DMA_TRIG_RX	UNICOMM3	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM3 Receive DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of SPI, I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.
UNICOMM4.DMA_TRIG_TX	UNICOMM4	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM4 Transmit DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.
UNICOMM4.DMA_TRIG_RX	UNICOMM4	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM4 Receive DMA trigger. Can come from the embedded UART, SPI, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of SPI, I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.
UNICOMM5.DMA_TRIG_TX	UNICOMM5	DMA_TRIG_TX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM5 Transmit DMA trigger. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. Single, configurable source condition.

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Table 31-4. DMA Triggers from the UNICOMM (continued)

Trigger Name	Peripheral Instance Name	Register Group	UNICOMM DMA Configuration Registers	Description
UNICOMM5.DMA_TRIG_RX	UNICOMM5	DMA_TRIG_RX	[IPMODE.SELECT].IIDX, [IPMODE.SELECT].IMASK, [IPMODE.SELECT].RIS, [IPMODE.SELECT].MIS, [IPMODE.SELECT].ISET	UNICOMM5 Receive DMA trigger. Can come from the embedded UART, I2CC or I2CT depending on the IPMODE.SELECT configured. For IPMODE of I2CC, and I2CT: Single, configurable source condition. For IPMODE of UART: Multiple OR'd, configurable source conditions.

31.7 UNICOMM Registers

This Section describes the UNICOMM Registers.

31.7.1 UNICOMM Base Address Table

Table 31-5. UNICOMM Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Unicomm0Regs	UNICOMM_REGS	UNICOMM0	0x4063_0000
Unicomm1Regs	UNICOMM_REGS	UNICOMM1	0x4063_2000
Unicomm2Regs	UNICOMM_REGS	UNICOMM2	0x4063_4000
Unicomm3Regs	UNICOMM_REGS	UNICOMM3	0x4067_0000
Unicomm4Regs	UNICOMM_REGS	UNICOMM4	0x4067_2000
Unicomm5Regs	UNICOMM_REGS	UNICOMM5	0x4067_4000

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31.7.2 UNICOMM_REGS Registers

Table 31-6 lists the memory-mapped registers for the UNICOMM_REGS registers. All register offset addresses not listed in Table 31-6 should be considered as reserved locations and the register contents should not be modified.

Table 31-6. UNICOMM_REGS Registers

Offset	Acronym	Register Name	Group	Section
800h	PWREN	Power enable		Go
804h	RSTCTL	Reset Control		Go
814h	STAT	Status Register		Go
1100h	IPMODE	Mode Selection Register		Go

Complex bit access types are encoded to fit into small table cells. Table 31-7 shows the codes that are used for access types in this section.

Table 31-7. UNICOMM_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value

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1 PWREN Register (Offset = 800h) [Reset = 00000000h]

PWREN is shown in Figure 31-5 and described in Table 31-8.

Return to the Summary Table.

Register to control the power state

Figure 31-5. PWREN Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE
R/W-0h							R/WK-0h

Table 31-9. PWREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	KEY to allow Power State Change 26h = KEY to allow write access to this register
23-1	RESERVED	R/W	0h	
0	ENABLE	R/WK	0h	Enable the power [EXT_GPRCM.GPRCM.PWREN.KEY] must be set to 26h to write to this bit. 0h = Disable Power 1h = Enable Power

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2 RSTCTL Register (Offset = 804h) [Reset = 00000000h]

RSTCTL is shown in Figure 31-6 and described in Table 31-9.

Return to the Summary Table.

Register to control reset assertion and de-assertion

Figure 31-6. RSTCTL Register

31	30	29	28	27	26	25	24
KEY							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						RESETSTKYCLR	RESETASSERT
W-0h						WK-0h	WK-0h

Table 31-11. RSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	KEY	W	0h	Unlock key B1h = KEY to allow write access to this register
23-2	RESERVED	W	0h	
1	RESETSTKYCLR	WK	0h	Clear the RESETSTKY bit in the STAT register [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Clear reset sticky bit
0	RESETASSERT	WK	0h	Assert reset to the peripheral [EXT_GPRCM.GPRCM.RSTCTL.KEY] must be set to B1h to write to this bit. 0h = Writing 0 has no effect 1h = Assert reset

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3 STAT Register (Offset = 814h) [Reset = 00000000h]

STAT is shown in Figure 31-7 and described in Table 31-10.

Return to the Summary Table.

peripheral enable and reset status

Figure 31-7. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							RESETSTKY
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 31-13. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	RESETSTKY	R	0h	This bit indicates, if the peripheral was reset, since this bit was cleared by RESETSTKYCLR in the RSTCTL register 0h = The peripheral has not been reset since this bit was last cleared by RESETSTKYCLR in the RSTCTL register 1h = The peripheral was reset since the last bit clear
15-0	RESERVED	R	0h	

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4 IPMODE Register (Offset = 1100h) [Reset = 00000000h]

IPMODE is shown in Figure 31-8 and described in Table 31-11.

Return to the Summary Table.

Used for selecting mode - UART / I2C Controller / I2C Target / SPI

Figure 31-8. IPMODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SELECT	
R/W-0h														R/W-0h	

Table 31-15. IPMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	SELECT	R/W	0h	Free run control 0h = UNICOMM is in UART Mode 1h = UNICOMM is in SPI Mode. Selection only valid for UC0, UC1, UC3, and UC4. 2h = UNICOMM is in I2C Controller Mode 3h = UNICOMM is in I2C Target Mode

31.8 SPG Registers

This section describes the SPG Registers.

31.8.1 SPG Base Address Table

Table 31-16. SPG Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Spg0Regs	SPG_REGS	SPG0	0x4063_F000
Spg1Regs	SPG_REGS	SPG1	0x4067_F000

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31.8.2 SPG_REGS Registers

Table 31-13 lists the memory-mapped registers for the SPG_REGS registers. All register offset addresses not listed in Table 31-13 should be considered as reserved locations and the register contents should not be modified.

Table 31-17. SPG_REGS Registers

Offset	Acronym	Register Name	Group	Section
120h	LPBK0	Loopback across multiple UNICOMM instances. User has to ensure that the UNICOMMs looped back are contained in the same SPG and have the same underlying IP instantiated (i.e. both UART, both SPI, both I2C, etc.)		Go
1C0h	PAIR0	Pairing of UNICOMM I2C-configured instances for Multi-Master/SMBUS applications. User has to ensure that the UNICOMMs looped back are contained in the same SPG and are both in I2C modes.		Go

Complex bit access types are encoded to fit into small table cells. Table 31-14 shows the codes that are used for access types in this section.

Table 31-18. SPG_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 LPBK0 Register (Offset = 120h) [Reset = 00000000h]

LPBK0 is shown in Figure 31-9 and described in Table 31-15.

Return to the Summary Table.

Loopback across multiple UNICOMM instances. User has to ensure that the UNICOMMs looped back are contained in the same SPG and have the same underlying IP instantiated (i.e. both UART, both SPI, both I2C, etc.)

Figure 31-9. LPBK0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERIPHERAL				CONTROLLER				RESERVED							EN
R/W-0h				R/W-0h				R/W-0h							R/W-0h

Table 31-20. LPBK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-12	PERIPHERAL	R/W	0h	UNICOMM instance selected for loopback. The selected instance will be treated as the LPBK0 peripheral. 0h = UNICOMM0_3 : Select UNICOMM0(SPG0) or UNICOMM3(SPG1). 1h = UNICOMM1_4 : Select UNICOMM1(SPG0) or UNICOMM4(SPG1). 2h = UNICOMM2_5 : Select UNICOMM2(SPG0) or UNICOMM5(SPG1).
11-8	CONTROLLER	R/W	0h	UNICOMM instance selected for loopback. The selected instance will be treated as the LPBK0 controller. 0h = UNICOMM0_3 : Select UNICOMM0(SPG0) or UNICOMM3(SPG1). 1h = UNICOMM1_4 : Select UNICOMM1(SPG0) or UNICOMM4(SPG1). 2h = UNICOMM2_5 : Select UNICOMM2(SPG0) or UNICOMM5(SPG1).
7-1	RESERVED	R/W	0h	
0	EN	R/W	0h	Loopback enable 0h = Disable 1h = Enable

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2 PAIR0 Register (Offset = 1C0h) [Reset = 00000000h]

PAIR0 is shown in Figure 31-10 and described in Table 31-16.

Return to the Summary Table.

Pairing of UNICOMM I2C-configured instances for Multi-Master/SMBUS applications. User has to ensure that the UNICOMMs looped back are contained in the same SPG and are both in I2C modes.

Figure 31-10. PAIR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TARGET				CTL				RESERVED							EN
R/W-0h				R/W-0h				R/W-0h							R/W-0h

Table 31-22. PAIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-12	TARGET	R/W	0h	UNICOMM instance selected for I2C pairing. The selected instance will be treated as the I2C PAIR0 target. 0h = UNICOMM0_3 : Select UNICOMM0(SPG0) or UNICOMM3(SPG1). 1h = UNICOMM1_4 : Select UNICOMM1(SPG0) or UNICOMM4(SPG1). 2h = UNICOMM2_5 : Select UNICOMM2(SPG0) or UNICOMM5(SPG1).
11-8	CTL	R/W	0h	UNICOMM instance selected for I2C pairing. The selected instance will be treated as the I2C PAIR0 controller. 0h = UNICOMM0_3 : Select UNICOMM0(SPG0) or UNICOMM3(SPG1). 1h = UNICOMM1_4 : Select UNICOMM1(SPG0) or UNICOMM4(SPG1). 2h = UNICOMM2_5 : Select UNICOMM2(SPG0) or UNICOMM5(SPG1).
7-1	RESERVED	R/W	0h	
0	EN	R/W	0h	Enable 0h = Disable 1h = Enable

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Chapter 32

Universal Asynchronous Receiver/Transmitter (UART)

The functionality of a UNICOMM module when configured to operate as a UART is described in this section. The protocol mode of a given UNICOMM instance is decided by the programmed SELECT field of the IPMODE register. If a UNICOMM instance is configured for another peripheral mode, the UART functionality on that UNICOMM instance is disabled and unusable.

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32.1 Overview

32.1.1 Purpose of the Peripheral

The Universal Asynchronous Receiver/Transmitter (UART) interface is a single-ended, asynchronous serial communication port that transmits (TX) and receives (RX) a programmable length serial bit stream into and out of the device at a programmable baud rate. The UNICOMM UART module can be used to communicate with another device supporting the standard UART protocol.

The **Basic** UNICOMM UART module features include additional support for:

- ISO7816 Smart Card

The **Basic+** UNICOMM UART module features include additional support for:

- LIN (Local Interconnect Network)

This device has both Basic and Basic+ implementations of the UART UNICOMM module on different UNICOMM instances. The *Available UNICOMM Configurations Per Instance* table lists which UNICOMM UART mode is present for each UCx instance inside each SPG. This document outlines the functionality of each feature.

32.1.2 Features

The UNICOMM-UART peripheral mode of the UNICOMM module includes the following features:

- Fully programmable serial interface:
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - LSB-first or MSB-first data transmit and receive
  - Line-break detection
  - Programmable baud-rate generation with oversampling by 16, 8 or 3
- Separate transmit (TX) and receive (RX) buffers/first-in first-out buffers (FIFOs)
- Direct Memory Access (DMA) support
- Available Interrupts:
  - Transmit (TX) and receive (RX) FIFO levels
  - End of transmission (EOT)
  - Receive timeout
  - Line timeout
  - Break, frame, parity, noise, and overrun error
  - Receive positive and negative edge conditions
  - Address matching
  - CTS condition
  - LIN counter capture, match, and overflow events
  - DMA done conditions
- Local Interconnect Network (LIN) hardware support (Basic+ instances)
- Hardware Flow Control (CTS/RTS)
- RS485 Flow Control support
- Idle-line Multiprocessor Mode
- 9-Bit UART Mode
- ISO7816 Smartcard support (Basic instances)
- Internal loopback test mode

To support UART protocol, a UNICOMM module must be configured as a UART in the UNICOMM top level IPMODE register.

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32.1.3 Functional Block Diagram

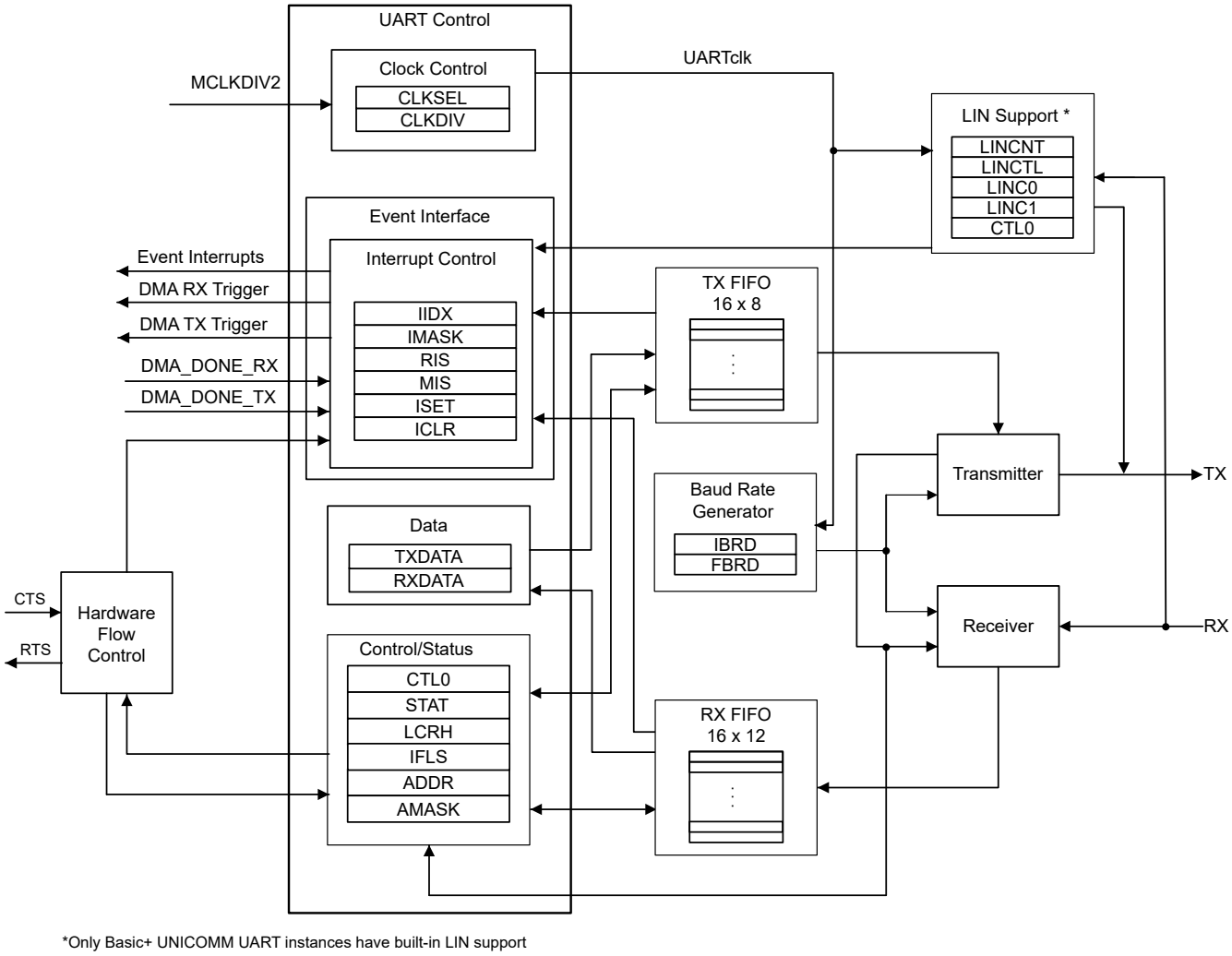


Figure 32-1. UART Functional Block Diagram

32.2 Peripheral Functional Description

32.2.1 Clock Control

The UART internal functional clock is selected and divided from the functional clock of the IP.

- Use the CLKSEL register to enable MCLKDIV2 as the functional clock source for the UNICOMM UART module.
- Use the CLKDIV register to select the divide ratio of the UART functional clock. The options available are divide by 1 through divide by 64.

The selected source clock is always available and the frequency depends on the power mode, for more information, see the *Clock Module (CKM)* section. After enabling the UART module by setting the CTL0.ENABLE bit, the module is ready to start receiving and transmitting data.

32.2.2 General Architecture and Protocol

The UART protocol transmits and receives characters at a programmable bit rate, called a baud rate, shared between the two communicating devices. This is done asychronously, meaning there is no connected clock pin

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for this protocol. The configured baud rate is generated by each device's functional clock and is used by both the UNICOMM UART transmitter and receiver submodules.

In general, configuration registers can only be programmed when the UNICOMM UART module is disabled (the ENABLE bit in the CTL0 register is cleared). One exception is the baud-rate divisor registers (IBRD and FBRD), which can be modified without disabling the UART. If the UNICOMM UART is disabled during an ongoing transmit or receive operation, the current transaction completes before the UART halts operation.

32.2.2.1 Signal Descriptions

UART communications require two pins: Receive Data (RX) and Transmit Data (TX):

- RX (Receive Data): The serial data input. Oversampling techniques are used on the receive signal for accuracy of incoming data.
- TX (Transmit Data): The serial data output. When the transmitter is enabled and no data needs to be transmitted, the TX pin is held high (idle). In some bidirectional protocols like ISO7816 Smart card, this pin is also used to receive data.

In hardware flow control mode, the following pins are also used.

- CTS (Clear To Send): The flow control input. When driven high by an external signal, this signal blocks the data transmission at the end of the current transfer.
- RTS (Request To Send): The flow control output. When held low, this signal indicates that the UART is ready to receive data.

32.2.2.2 Transmit and Receive Logic

The transmit logic performs parallel-to-serial conversion on the data written to the TXDATA register. The UNICOMM-UART transmitter automatically buffers the data written to the TXDATA register into the TX FIFO. The control logic outputs the serial bit stream beginning with a start bit and followed by the data bits (LSB first), parity bit, and the stop bits according to the programmed configuration.

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line-break detection are also performed, and this status accompanies the data that is written to the receive FIFO. Each RX FIFO element is 12-bits wide to include the data bits and all status information.

In the UNICOMMUART Registers, the CTL0.ENABLE bit is used to enable and disable the UNICOMM-UART module, the CTL0.TXE and CTL0.RXE bits are used to enable the UART transmitter and UART receiver, the LCRH.WLEN bit is used to configure the number of data bits transmitted or received in each frame, the LCRH.PEN is used to enable parity mode, and the LCRH.STP2 is used to send two stop bits (rather than the default one bit).

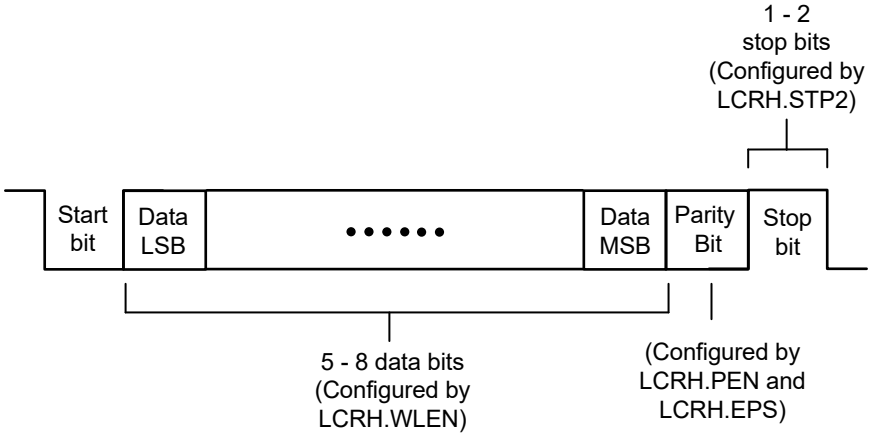


Figure 32-2. UART Character Frame

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32.2.2.3 Bit Sampling

UNICOMM UART supports oversampling at 3x, 8x, and 16x the UART bus baud-rate.

- By default, CTL0.HSE is set to 0, i.e.16X oversampling is selected. The center sample (sample 8) is used for sampling data on RX line.
- CTL0.HSE set to '1', selects 8X oversampling. The center sample (sample 4) is used for sampling data on RX line.
- CTL0.HSE set to '2' selects 3X oversampling. The center sample (sample 2) is used for sampling data on RX line.

The aforementioned scenarios assume an IBRD =1 and FBRD =0.

Depending on the application:

- Select oversampling by 3 or 8 to achieve higher speed with UARTclk/8 or UARTclk/3. In this case the receiver tolerance to clock deviation is reduced.
- Select oversampling by 16 to increase the tolerance of the receiver to clock deviations. The maximum speed is limited to UARTclk/16.

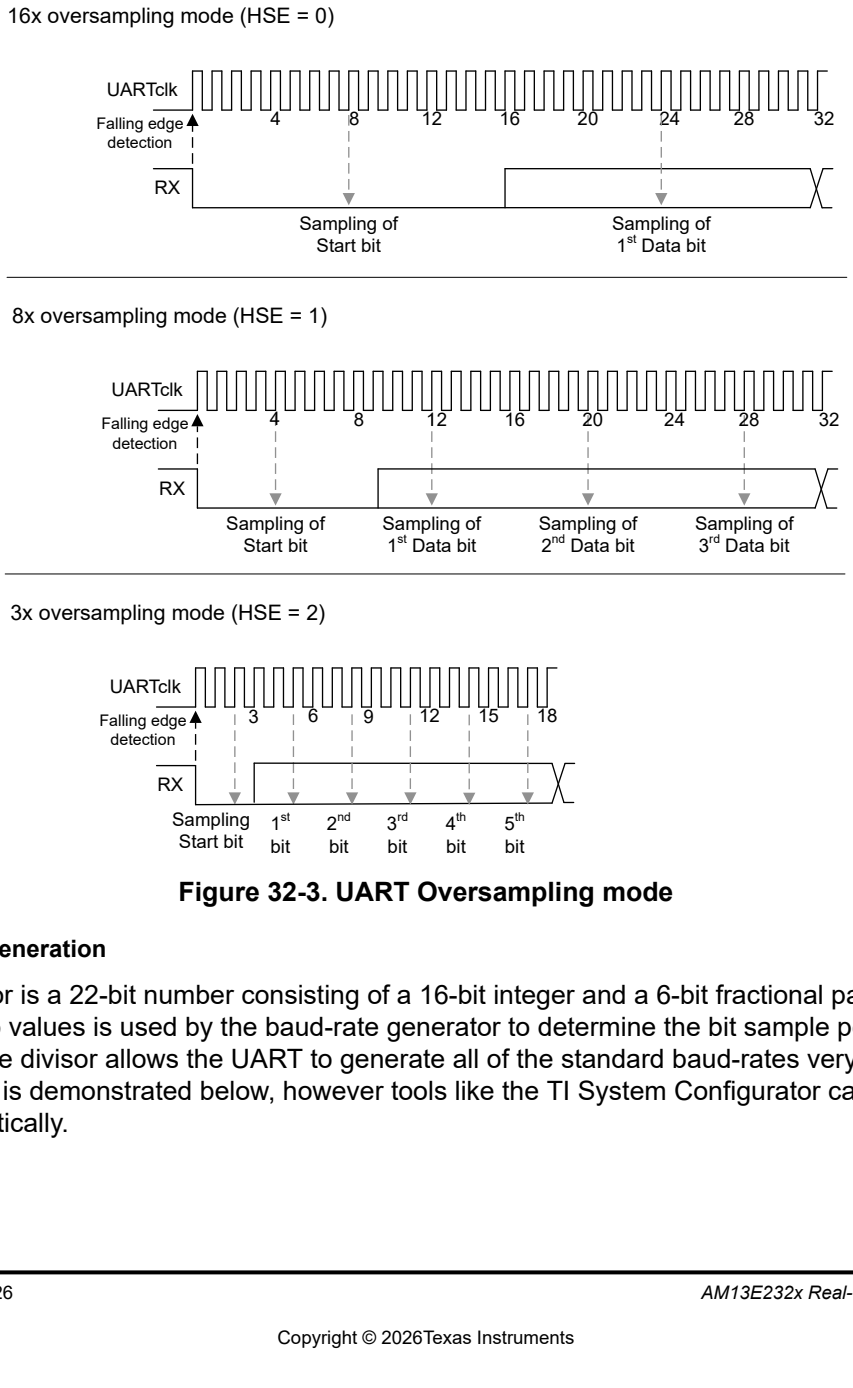


Figure 32-3. UART Oversampling mode

32.2.2.4 Baud Rate Generation

The baud-rate divisor is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. The number formed by these two values is used by the baud-rate generator to determine the bit sample period. Having a fractional baud-rate divisor allows the UART to generate all of the standard baud-rates very accurately. An example calculation is demonstrated below, however tools like the TI System Configurator can perform these calculations automatically.

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The 16-bit integer is loaded through the UART Integer Baud-Rate Divisor IBRD register and the 6-bit fractional part is loaded with the UART Fractional Baud-Rate Divisor FBRD register.

The baud-rate divisor can be calculated by using the following formula:

BRD = UART Clock / (Oversampling x Baud rate) (47)

UART Clock (UARTclk) is the clock output of the UART clock control logic, configured by CLKSEL and CLKDIV. Oversampling is selected by the HSE bit in the CTL0 register and can be configured to 16, 8 or 3.

- IBRD = INT(BRD), integer portion of the BRD
- FBRD = BRD % 64 , fractional portion of the BRD

The integer portion of the BRD is loaded into IBRD register. The 6-bit fractional number must be loaded into the FBRD register.

Note

When IBRD = 0, FBRD is ignored and no data gets transmitted or received by the UART. Similarly, when IBRD = 65535 (that is 0xFFFF), then FBRD must not be greater than zero. The ongoing transmission or reception is aborted if these requirements are not met.

The following example shows a simple method to calculate IBRD.DIVINT and FBRD.DIVFRAC for a baud rate of 19200 bit/s:

UART Clock = MCLKDIV2 / CLKDIV.RATIO = 40 MHz
CTL0.HSE Oversampling = 16
Baud Rate = 19200 bit/s

$$BRD = \frac{UARTclk}{Oversampling \times Baud\ Rate} = \frac{40MHz}{16 \times 19200\ bit/s} = 130.2083333$$

IBRD.DIVINT= 130 (=82h)

FBRRD.DIFRAC
= INT((.2083333 x 64) + 0.5)
= INT(13.833333)
= 13d (= Dh)

Note: The adder '+0.5' ensures rounding to the closest integer value to keep the rounding error as small as possible

Figure 32-4. Baud Rate Configuration

When updating the baud-rate divisor (IBRD or IFRD), the LCRH register must also be written, so any changes to the baud rate divisor must be followed by a write to the LCRH register for the changes to take effect. The contents of the IBRD and FBRD registers are not updated until transmission or reception of the current character is complete.

32.2.2.5 Data Transmission

Data received or transmitted is stored in two 16-element FIFOs, where the receive FIFO has an extra four bits per character for status information.

Transmit data:

For transmission, data is written into the TXDATA register. If the UART is enabled, a write to TXDATA causes a data frame to start transmitting with the parameters indicated in the LCRH register. Data continues to be transmitted until there is no data left in the transmit FIFO. The BUSY bit in the STAT register is asserted as soon as data is written to the transmit FIFO (that is, if the FIFO is non-empty) and remains asserted while data is being transmitted. The BUSY bit goes low only when the transmit FIFO is empty, and the last character has been

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transmitted to the shift register, including the stop bits. STAT.BUSY also is set during the generation of a BREAK signal.

Receive data:

When the UART receiver is in an idle state and data input transitions to a low level (i.e. START condition detect), the receive counter starts running and data is sampled as per the oversampling settings in CTL0.HSE, except for the START/STOP bits. During the START bit, the receiver checks that every sampled value reads '0', and if not, the receiver state machine transitions back to the IDLE state. During the STOP bit/s, the receiver checks that every sampled value reads '1'. If not, the framing error flag (RXDATA.FRMERR) is set. When a full word is received, data is stored in the receive FIFO along with any associated error bits. The STAT.BUSY flag is set to high when a START condition is detected and set to low after a STOP bit has been received (i.e. after the entire duration of STOP bit).

32.2.2.6 Error and Status

For received data, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive buffer/FIFO. The error and status can be can be retrieved by reading RXDATA register as showing in Table 32-1. Each of the four below conditions can also set the interrupt flag RXINT if the corresponding interrupt bit is enabled in the IMASK register.

Table 32-1. UART Error and Conditions

Error Condition(1)	Bit Field	Description
Framing error	FRMERR	A framing error occurs when a low stop bit is detected. When two stop bits are used, both stop bits are checked for a framing error. When a framing error is detected, the FRMERR bit is set.
Parity error	PARERR	A parity error is a mismatch between the number of 1s in a character and the value of the parity bit. Address bits are included in the parity calculation if included in the character. When a parity error is detected, the PARERR bit is set.
Receive overrun	OVRERR	An overrun error occurs when a character is loaded into RXDATA/FIFO before the prior character has been read. When an overrun occurs, the OVRERR bit is set.
Break condition	BRKERR	A break is detected when the receive input is held low for longer than a full character transmission time, meaning the start bit, all received data, parity bit, and stop bit/bits are 0. When a break condition is detected, the BRKERR bit is set.

(1) Framing error and break condition are not set when LIN mode is enabled, this pattern is used to signal a Sync frame for LIN.

The UART module flag status can also be checked by reading the STAT register, as shown in Table 32-2.

Table 32-2. UART Flag Status

Bit Field	Description
BUSY	This bit is set as soon as the transmit FIFO becomes non-empty (regardless of whether UART is enabled). In IDLELINE mode (when the CTL0.MODE field is configured for IDLELINE), the BUSY signal also stays set during the idle time generation.
RXFE	This bit is set when the receive FIFO is empty.
RXFF	This bit is set when the receive FIFO is full.
TXFE	This bit is set when transmit FIFO is empty.
TXFF	This bit is set when transmit FIFO is full.
CTS	This bit is set when CTS signal is asserted (low) and cleared when CTS signal is not asserted (high).
IDLE	This bit is set when an IDLE line has been detected in idle-line multiprocessor mode. The IDLE bit is used as an address tag for each block of characters. In idle line multiprocessor format, this bit is set when a received character is an address.

32.2.2.7 DMA Operation

The UNICOMM-UART provides an interface to the DMA module with separate channels for transmit and receive. The DMA operation of the UART is enabled through the UART Event and DMA registers. When DMA operation

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is enabled, the UART asserts a DMA request on the receive or transmit channel when the associated FIFO can transfer data. The DMA transfer requests are handled automatically by the DMA controller based on how the DMA channel is configured (burst size, transfer size, source address etc.).

For more information about the DMA module and DMA-specific configurations, see the Direct Memory Access (DMA) chapter.

- For the receive channel, a DMA transfer request is asserted when the amount of data in the receive FIFO is at or above the FIFO trigger level configured using the RXIFLSEL bit in IFLS register or if the receive timeout has triggered. In the receive timeout trigger case, the amount of data received up to that point is transferred.

Note

The DMA moves all data present in the RX FIFO once triggered, not just the amount configured by the RXIFLSEL field.

- For the transmit channel, a DMA transfer request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level configured using the TXIFLSEL bit in IFLS register.

32.2.2.8 Internal Loopback Operation

The UNICOMM-UART can be placed into an internal loopback mode for diagnostic or debug work by setting the LBE bit in the CTL0 register. In loopback mode, the UART operates with the following behavior:

- Data transmitted on the TX output is received on the RX input
- Data transmitted on the TX output is not propagated to the TX IO pin
- Data received on the RX IO pin is ignored

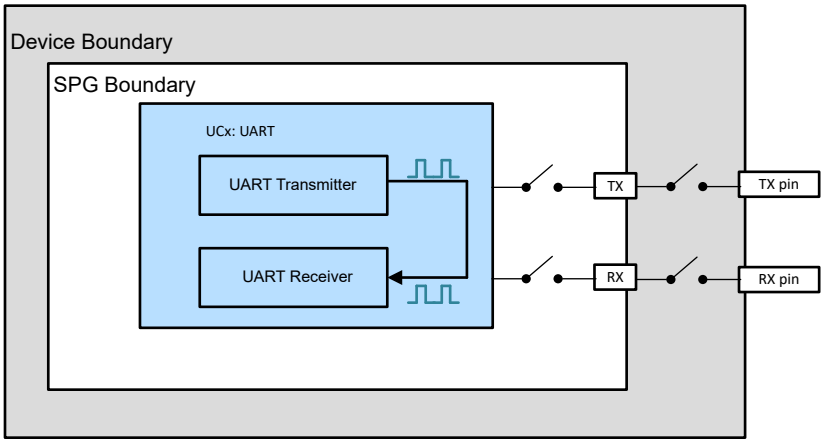


Figure 32-5. UART Internal Loopback

32.2.3 Additional Protocol and Feature Support

32.2.3.1 Local Interconnect Network (LIN) Support

LIN hardware support is only available for Basic+ UNICOMM-UART instances.

The Local Interconnect Network (LIN) protocol standard is based on the UART serial data link format. The LIN communication protocol is a single-commander/multiple-responder topology with message identification for multicast transmission between network nodes.

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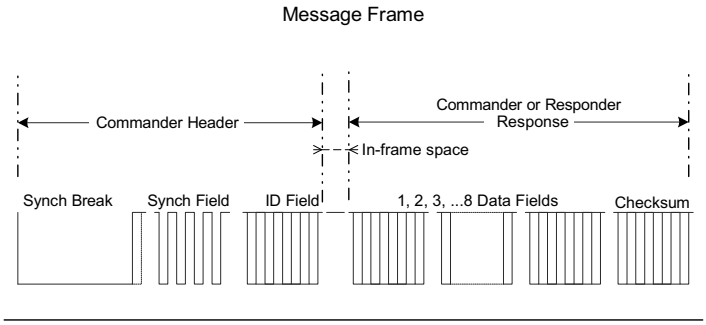


Figure 32-6. LIN Protocol Message Structure

The LIN commander issues a BREAK field, SYNC field, and PID (Protected Identifier) field at the start of every frame. The four LIN registers are used so that the LIN responder software driver can reasonably detect BREAK and SYNC fields and measure the necessary timing parameters to adjust the baud rate or detect an error.

See the *LIN Standards and Specifications* page for more information about the LIN protocol standards. The UNICOMM-UART module in LIN mode can operate as a LIN commander or a LIN responder when configured properly. To support the LIN protocol while reducing the number of interrupts needed in software, the following hardware enhancements are included in the UNICOMM-UART module in the Basic+ module variants:

- **LIN Control** - LINCTL
  - Configuration of LIN mode behavior.
- **LIN Counter** - LINCNT
  - 16-bit up-counter clocked by the UARTclk.
  - CPU_INT.IMASK.LINOVF flag - Interrupt capability on counter overflow.
- **LIN Capture 0** - LINC0
  - 16-bit Capture 0 with two configurable modes:
    - If LINCTL.LIN0CAP is set - Capture of the LINCNT value on RX pin falling edge. Interrupt capability on capture (CPU_INT.IMASK.LINC0).
    - If LINCTL.LIN0_MATCH is set - Compare of the LINCNT with interrupt capability on match (CPU_INT.IMASK.LINC0).
- **LIN Capture 1** - LINC1: 16-bit Capture 1.
  - Capture LINCNT value on RX pin rising edge. Interrupt capability on capture (CPU_INT.IMASK.LINC0).

Additionally, software can manually control the logic level output of the UNICOMM-UART TXD pin by writing the CTL0.TXD_OUT bit when the CTL0.TXD_OUT_EN is set to 1 with CTL0.TXE set to 0 (transmits disabled). This feature is also needed to achieve a LIN protocol on UNICOMM-UART.

Note

Full hardware support of the LIN protocol is not available in UNICOMM-UART. The above registers are used to aid in a software LIN implementation of the LIN-specific features added on top of the UART protocol.

32.2.3.1.1 LIN Commander Transmit

The below highlights how a UNICOMM-UART can implement each portion of the LIN Commander transmission using the registers available in the module.

Transmitting the Break Field

The break signal can be sent automatically by the UNICOMM-UART by setting the BRK bit in LCRH register for greater than 13*Tbits. This bit needs to be set before any data is written into the transmit data register TXDATA.

Transmitting the Sync Field

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The sync field can be sent by writing 0x55 to the TXDATA register to be transmitted using the standard UNICOMM-UART transmitter.

Transmitting the PID Field

Write the ID byte to the TXDATA register to be transmitted using the standard UNICOMM-UART transmitter. Make sure CTL0.TXE is set.

Transmitting the Data Fields

Write the data bytes to TXDATA register to be transmitted using the standard UNICOMM-UART transmitter. Make sure CTL0.TXE is set.

Transmitting the Checksum

Calculate and write the checksum byte to the TXDATA register to be transmitted using the standard UNICOMM-UART transmitter. Make sure CTL0.TXE is set.

32.2.3.1.2 LIN Responder Receive

Receiving the Break Field

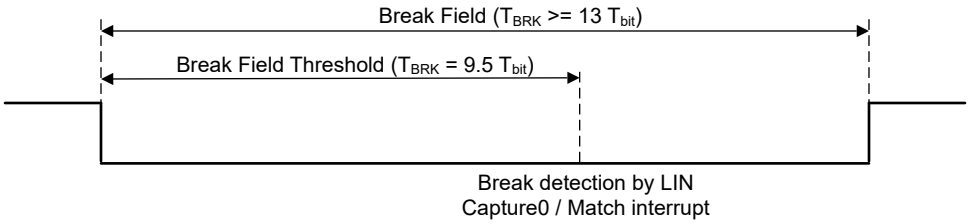


Figure 32-7. LIN Break Field Detection

Use the break field detection and compare modes to receive and validate the BREAK field of a LIN message. The following configurations are needed:

1. Initialize the LIN counter register to 0 (LINCNT = 0)
2. Enable counter compare match mode (LINCTL.LINC0_MATCH = 1)
3. Load LINC0 (Counter Capture 0 register) with the counter value corresponding to 9.5 x T_{bit} (refer to the *LIN Standards and Specifications* for details on this timing).
4. Enable the LINC0 match interrupt (CPU_INT.IMASK.LINC0 = 1)
5. Setup LIN count control (configure the LINCTL register):
   - Enable count while low signal on RXD pin (LINCTL.CNTRXLOW = 1)
   - Enable LIN counter clearing on RXD pin falling edge (LINCTL.ZERONE = 1)
   - Enable LIN counter (LINCTL.CTRENA = 1)

   Optional:
   - Enable the rising edge on UART TX signal interrupt (CPU_INT.IMASK.RXPE = 1), when the RXPE interrupt fires, the software can read the LINCNT directly to see the BREAK field timing.
   - Enable the LIN counter overflow interrupt (CPU_INT.IMASK.LINOVF = 1) to detect the BREAK field is too long and overflows 16-bit counter. The timeout can be calculated as $t_{Timeout}$= 2^{16}/ UARTclk.

Receiving the Sync Field

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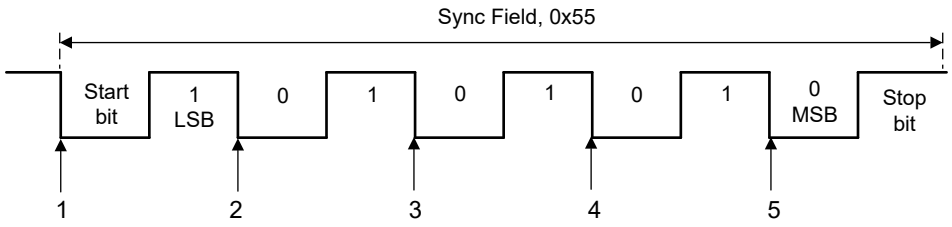


Figure 32-8. LIN Sync Field Detection

Sync field validation is required to verify accuracy of the LIN header and to calculate the commander baud rate. The sync field consists of the data 0x55 inside a byte field (see Figure 32-8). After software detects a valid BREAK field, the counter can be set to measure the SYNC field. Figure 32-8 shows the SYNC byte format. The LINCNT is set to 0 on the start bit falling edge and counts continuously. The LINC0 capture or RX falling edge interrupt fires at the falling edges of the RX line. During interrupt processing, software can measure the individual HIGH/LOW times of the bits themselves with the values in the LINC0 and LINC1 registers to verify that all of the timings are valid.

The following flow describes a LIN sync field validation procedure:

1. Initialize LIN counter to 0 (LINCNT = 0) after detecting a valid break field.
2. Enable interrupt on RX falling edge (CPU_INT.IMASK.RXNE = 1)
3. Setup LIN count control (LINCTL):
   - Enable LIN counter capture on raising RX edge (LINCTL.LINC1CAP = 1)
   - Enable LIN counter capture on falling RX edge (LINCTL.LINC0CAP = 1)
   - Enable LIN counter clearing on RX falling edge (LINCTL.ZERONE = 1)
   - Enable LIN counter (LINCTL.CTRENA = 1)

Actions at each falling edge of the RX line for the sync field as showing below:

1. LIN counter is set to 0 and start counting on the falling RX edge. (LINCTL.ZERONE = 1)
2. RX falling edge interrupt trigger (RXNE):
   - Read capture register LINC0 (falling edge) and LINC1 (rising edge) values
   - Verify bit times
3. RX falling edge interrupt trigger (RXNE):
   - Read capture register LINC0 (falling edge) and LINC1 (rising edge) values
   - Verify bit times
4. RX falling edge interrupt trigger (RXNE):
   - Read capture register LINC0 (falling edge) and LINC1 (rising edge) values
   - Verify bit times
5. RX falling edge interrupt trigger (RXNE):
   - Read capture register LINC0 (falling edge) and LINC1 (rising edge) values
   - Verify bit times
   - Calculate the proper baud rate to set. Software must set the baud rate before the start bit of the PID field after sync field.

On each interrupt occurrence, the capture registers must be read and the bit times need to be validated by the application software. In case of a bit time verification error, the sync field analysis process must be aborted and the application software must switch back to break detection.

In case of errors like a breaking commander communication during sync field detection, a timeout interrupt can be generated by enabling the LIN counter overflow (IMASK.LINOVF = 1). When the counter overflows, the interrupt handler can abort the sync field analysis and switch back to break detection. The time the counter overflow interrupt occurs can be calculated as $t_{Timeout} = 2^{16}$/ UART clock.

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Note

The sync field is automatically stored in the RX FIFO and can be misread as the PID. Therefore, flush the RX FIFO after the sync field is received and before the PID is received.

Receiving the PID Field

Read the PID byte from the RXDATA register using the standard UNICOMM-UART receiver. Make sure CTL0.RXE is set.

Receiving the Data Fields

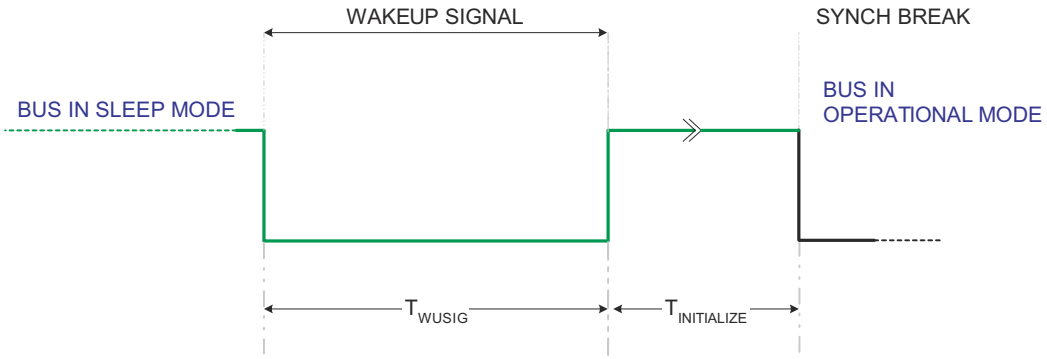
Read the data fields from the RXDATA register using the standard UNICOMM-UART receiver. Make sure CTL0.RXE is set.

Receiving the Checksum Field

Read the checksum byte from the RXDATA register using the standard UNICOMM-UART receiver and decode the value in software. Make sure CTL0.RXE is set.

32.2.3.1.3 LIN Wakeup

Per the LIN specification, any node in a sleeping LIN cluster can request a wake up by transmitting a wake up signal. This signal type is shown in Figure 32-9.



Note

$0.25ms \leq T_{WUSIG} \leq 5ms$

Figure 32-9. LIN Wakeup

To generate a wake signal on the TX pin with the UNICOMM-UART as a LIN controller, the application must use the CTL0.TXD_CTL_EN and CTL0.TXD_OUT bits. Set the TXD_CTL_EN bit to enable register control of the TXD pin, then clear the TXD_OUT bit for the duration of T_{WUSIG} .

32.2.3.2 Flow Control

In the default UART mode (CTL0.MODE set to 0), hardware flow control between two devices is accomplished by connecting the RTS output to the CTS input on the receiving device, and connecting the RTS output on the receiving device to the CTS input. The RTS output signal is active low, the CTS input expects a low signal on a send request as shown in Figure 32-10.

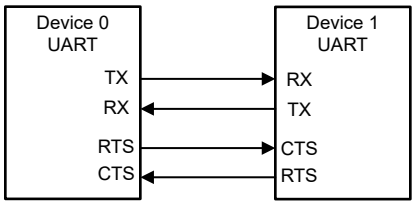


Figure 32-10. Flow Control

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The CTS input controls the transmitter. The transmitter can only transmit data when the CTS input is asserted low. When RTS flow control is enabled, the RTS output signal indicates the state of the RX FIFO. CTS of the transmitting device remains asserted low until, the preprogrammed watermark level is reached, indicating that the receiver has no space to store additional characters.

The CTSEN and RTSEN bits in the CTL0 register specify the flow control mode as shown in Table 32-3.

Table 32-3. Flow Control Enable

CTSEN	RTSEN	Description
1	1	RTS and CTS flow control enabled
1	0	Only CTS flow control enabled
0	1	Only RTS flow control enabled
0	0	Both RTS and CTS flow control disabled

The RTS bit can be driven by hardware or software. When RTSEN is 1 (i.e. hardware-controlled mode), the value of CTL0.RTS bit is ignored and RTS output signal is generated by hardware trigger levels as described below.

RTS flow control:

The RTS flow control logic is linked to the programmable RX FIFO watermark levels, which can be configured using the IFLS register. When RTS flow control is enabled, the RTS is asserted (low) until the RX FIFO is filled up to the watermark level. When the RX FIFO watermark level is reached, the RTS signal is de-asserted (high), indicating that there is no more room to receive any more data. The other device's transmission of data is expected to cease after the current character has been transmitted. The RTS signal is reasserted (low) when data has been read out of the RX FIFO until the FIFO is filled to less than the watermark level. If RTS flow control is disabled and the UNICOMM-UART is still enabled, then data is received until the RX FIFO is full, or there is no more data transmitted.

The RTS signal is de-asserted when the FIFO watermark level is reached by putting the last received character into the FIFO. This means on a back to back transmit, another character transfer could already have been started by the other device. In this case, the watermark level must be set to one level lower so that all data can be received and put into the FIFO.

CTS flow control:

If CTS flow control is disabled and the UNICOMM-UART is enabled, data is continuously transmitted until the TX FIFO is empty.

If CTS flow control is enabled, then the transmitter checks that the CTS signal is asserted low before transmitting each byte. The data continues to be transmitted while CTS is asserted (low), and the TX FIFO is not empty. If the TX FIFO is empty and the CTS signal is asserted (low) no data is transmitted. If the CTS signal is de-asserted (high), then the current character transmission is completed before the transmission is halted.

32.2.3.3 RS485 Support

RS485 is a standard used in serial communications systems. This standard can be used effectively over long distances and in electrically noisy environments. Multiple receivers can be connected to a RS-485 network. These characteristics make RS-485 useful in industrial control systems and other similar applications.

The RS485 direction signal controls the external RS485 PHY. The RTS I/O is used in this mode as the direction signal. The signal is set automatically to high once a data transmit is started. This siganl stays high between back to back byte transmits. If a data receive operation is ongoing, a new transmit must be delayed until this data has been received and the direction signal has been set to transmit.

The data exchange sequence is show in Figure 32-11:

- Wait until an ongoing receive has been finished.
- Activate direction signal to transmit on RTS Pin
- Send data (one or more bytes)

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- Wait till an ongoing receive has been finished.
- Deactivate direction signal to transmit on RTS Pin

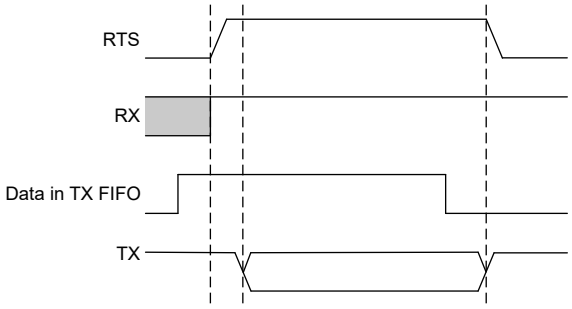


Figure 32-11. RS485 Data Exchange

Two bit fields to the LCRH register define the setup and hold time of the external driver direction control:

- EXTDIR_SETUP bits define number of functional clocks between RTS assertion and beginning of START bit
- EXTDIR_HOLD bits define number of functional clocks between STOP (entire bit duration) and RTS de-assertion

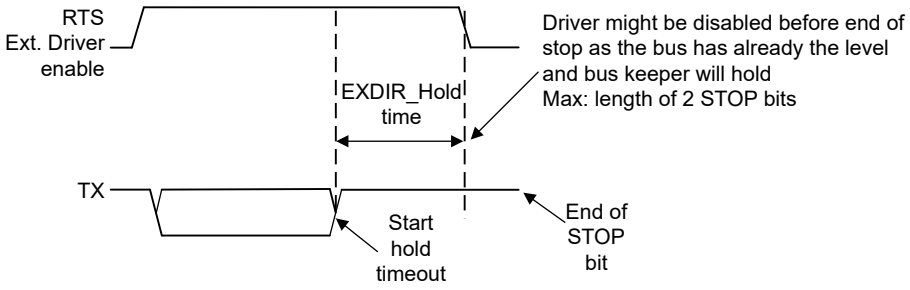


Figure 32-12. RS485 external driver control

32.2.3.4 Idle-Line Multiprocessor

This section applies to UNICOMM-UART configurations which support the UART-IDLELINE-MULTIPROC feature.

When IDLELINE is set in the CTL0.MODE register bits, the idle-line multiprocessor format is selected. Blocks of data are separated by an idle time on the transmit or receive lines (Figure 32-13). An idle receive line is detected when ten or more continuous ones (marks) are received after the one or two stop bits of a character. The baud-rate generator is switched off after reception of an idle line until the next start edge is detected. When an idle line is detected, the IDLE bit in UARTx.STAT is set. In Idle-Line mode the UART receiver operates in no parity mode and the UART word length (UARTx.LCRH.WLEN) must be set to 8bit.

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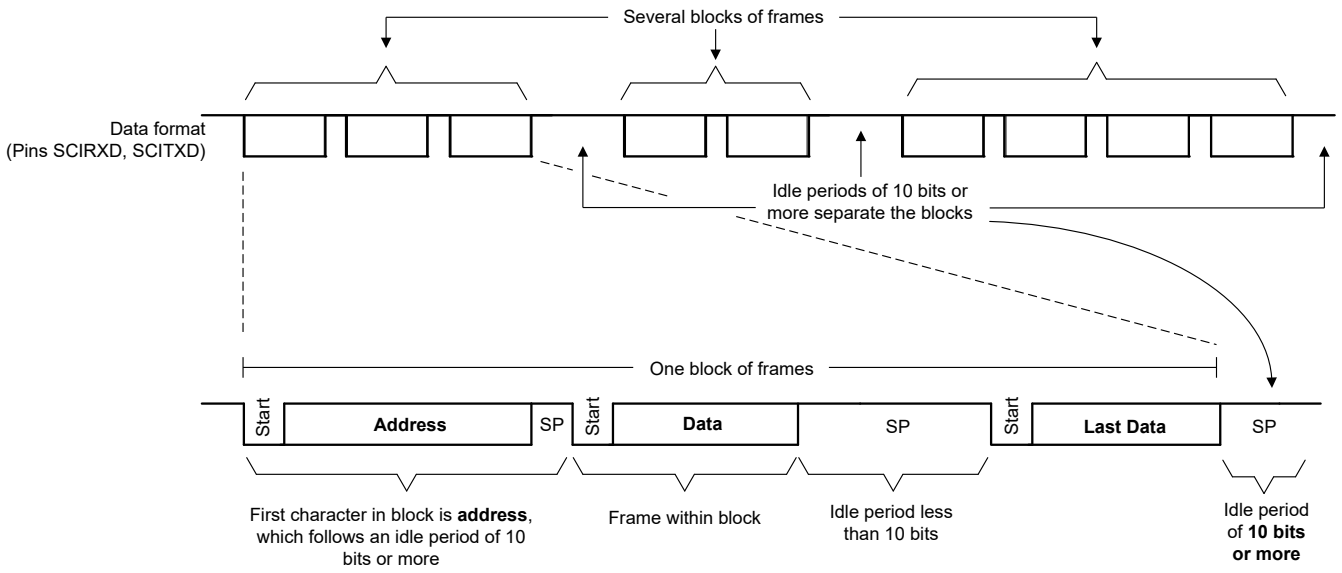


Figure 32-13. Idle-Line Multiprocessor

The first character received after an idle period is an address character. The IDLE bit in UARTx.STAT register is used as an address tag for each block of characters.

If an address character is received it is compared against the ADDR register with the AMASK applied. If the received character matches, the address character and all following received characters are transferred into the RXDATA buffer/FIFO and interrupts are generated until the next address without a match is received. The IDLE bit in STAT register is automatically cleared when the address does match; otherwise the IDLE bit is set until the address is matched.

When SENDIDLE control bit is set, the UART inserts an idle period of 11 bit times on the bus. Application has to ensure that there are no active transactions on the transmit line prior to setting SENDIDLE bit.

Once SENDIDLE bit is set, application has to wait for SENDIDLE status bit to be asserted and then clear the SENDIDLE control bit to proceed. The next transfer can then begin with an address character.

The following procedure sends out an idle frame to indicate an address character followed by associated data:

1. Set SENDIDLE then write the address character to TXDATA. TXDATA must be ready for new data (TXINT interrupt must be 1). This generates an idle period of exactly 11 bits followed by the address character. SENDIDLE is reset automatically when the address character has been transferred (all bits are sent out of shift register).
2. Write desired data characters to TXDATA. TXDATA must be ready for new data (TXINT interrupt must be 1). The data written to TXDATA is transferred to the shift register and transmitted as soon as the shift register is ready for new data.

The idle-line time (10 bit periods) must not be exceeded between address and data transmission or between data transmissions. Otherwise, the transmitted data is misinterpreted as an address.

When using IDLELINE mode, the UART Word Length in the LCRH register must be set to:

- 8-bit word length (WLEN bits 6:5 configured to 0x3)

BUSY bit in IDLELINE:

- TX: BUSY is set during the generation of an IDLELINE signal and while the address and data bytes are sent.
- RX: The BUSY signal while receiving data and till first 10 idle bits are received.

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32.2.3.5 9-Bit UART Mode

9-bit mode is enabled by setting the MODE field to ADDR9BIT in the CTL0 register. This feature is useful in a multi-drop configuration where a single controller connected to multiple peripherals can communicate with a particular peripheral through the peripheral's programmed address or a set of addresses, along with a qualifier for an address byte. In 9-bit UART mode, the parity enable/mode bits are ignored and the UART word length (LCRH.WLEN) must be set to 8 bits.

Receive Transaction:

In 9-bit mode, a UNICOMM-UART peripheral checks for the address qualifier at the location of the parity bit. If set, the received byte is compared with the preprogrammed address in ADDR register:

- If the address matches, a 9-bit mode address match interrupt (ADDR_MATCH) is generated, if enabled, and further data is received into the RX FIFO.
- If the address does not match, the address byte and the subsequent data bytes are not received into the RX FIFO.

The address is predefined in the ADDR register to match with the received byte. Matching can be extended to a set of addresses using the address mask in the AMASK register. By default, the AMASK is 0xFF, meaning that only the specified address can generate a match.

Transmit Transaction:

All the transmits in 9-bit UART mode are interpreted as:

- Address bytes, if the 9th bit is set
- Data bytes, if the 9th bit is cleared

In 9-bit mode, the 9th bit can be controlled by software. The value set in the EPS bit of the LCRH register determines the value of the 9th bit for transmit transactions. To indicate an address byte, the application must set the EPS bit before the byte transmission. To indicate a data byte, the EPS bit must be cleared before the byte transmission. For a complete transmit transaction, the address byte must be transmitted as a single byte transaction with EPS bit set, followed by a data byte burst where the EPS bit is cleared.

Table 32-4. 9th Bit Handling

PEN	EPS	9th Bit (Transmitted or Verified)
0	X	Not transmitted or verified
1	0	0 (= Data)
1	1	1 (= Address)

32.2.3.6 ISO7816 Smart Card Support

ISO7816 Smart Card support is only available for Basic UNICOMM-UART instances.

The UNICOMM-UART Smart Card support feature enables basic communication with an ISO7816 smart card. When configuring the CTL0.MODE field, select the smart card option, the TXD signal is used as a bit clock, and the RXD signal is used as the half-duplex communication line connected to the smart card. Further smart card signals are not supported by UNICOMM-UART.

The clock rate of the UART clock in ISO7816 mode must be in the range of 1 MHz to 5 MHz when using ISO7816 mode, the LCRH register must be set to:

- 8-bit word length (WLEN bits configured to 0x3)
- Even parity (PEN set and EPS set)
- No stick parity (SPS cleared)

In ISO7816 mode, the UART automatically uses 2 stop bits and oversampling of 16 is used; LCRH.STP2 & CTL0.HSE bits are ignored.

If a parity error is detected during a transmission, the RX line is pulled low during the second stop bit. In this case, the UNICOMM-UART aborts the transmission and flushes the TX FIFO. Additionally,the module raises a

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parity error interrupt, allowing the software to detect the problem and initiate retransmission of the affected data, as the UART does not support automatic retransmission in this case. The UART does not support automatic retransmission on parity errors. If a parity error is detected on transmission, all further transmit operations are aborted and software must handle retransmission of the affected byte or message.

In Smartcard Mode, the receiver in case of parity error drives the line low and a parity interrupt flag is asserted. The transmitter responds based on the value of this bit.

32.2.3.7 Address Detection

This section applies when a UNICOMM-UART module is configured for Idle-line multiprocessor mode or 9-Bit UART mode in the CTL0.MODE register field.

The ADDR register is used to set the specific address that is matched to the received address byte. This register is used in conjunction with AMASK register to form a match for address-byte received. Only bits where the AMASK is set to '1' are considered. So for full address the AMASK register is set to 0xFF.

Table 32-5. Address Detection

Condition	Idle Line Mode	9-Bit Mode
Address match	Address and Data is moved to RXDATA	Address and Data is moved to RXDATA
Address mismatch	Address and Data get dropped	Address and Data get dropped

32.2.4 Initialization

Follow the high-level UNICOMM configurations in Section 31.3 before executing the below UART-specific configurations.

To enable and initialize the UART, perform the following initialization steps:

1. Clear the ENABLE bit in the CTL0 register before making any of the below configuration changes.
2. Use the baud-rate equation in Figure 32-4 to calculate the IBRD and FBRD registers.
3. Write the integer portion of the BRD to the IBRD register.
4. Write the fractional portion of the BRD to the FBRD register.
5. Write the desired communication mode settings to the CTL0 register (all CTL0 fields other than ENABLE).
6. Write the desired serial parameter configurations to the LCRH register.
7. Configure the desired FIFO trigger levels in the IFLS register.
8. Enable desired interrupts and/or DMA event by using CPU_INT, DMA_TRIG_RX, DMA_TRIG_TX group IMASK registers.
9. (Optionally) Configure the emulation mode for the peripheral in the PDBGCTL register.
10. Enable the UART by setting the CTL0.ENABLE bit.

Note

Before UNICOMM-UART is setup or configuration changes, the CTL0.ENABLE bit must be cleared to avoid unpredictable behavior during the updates or for the first data receive or transmitted afterward.

32.2.5 Emulation Modes

The module behavior while the device is in debug mode is controlled by the FREE and SOFT bits in PDBGCTL register.

When the device is in debug mode and set into halt mode below behavior can be configured.

Table 32-6. Debug Mode Peripheral Behavior

PDBGCTL.FREE	PDBGCTL.SOFT	Function
1	**x**	Modules continues operation
0	**0**	Module stops immediately
0	**1**	Module stops after the next transfer has been finished

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32.3 UART Interrupts & Triggers

32.3.1 CPU Interrupts (IRQs)

The UNICOMM-UART interrupts are fed through the UNICOMM instance interrupt line when that UNICOMM's IPMODE is configured as UART. See Section 31.6.1 for more information on the UNICOMM CPU interrupts.

32.3.2 DMA Triggers

The UNICOMM-UART DMA triggers (TX and RX) are fed through the UNICOMM instance trigger lines when that UNICOMM's IPMODE is configured as UART. See Section 31.6.2 for more information on the TX and RX UNICOMM DMA triggers.

32.4 UNICOMM-UART Registers

This Section describes the UNICOMM-UART Registers.

32.4.1 UNICOMM-UART Base Address Table

Table 32-7. UNICOMM-UART Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Uc0uartRegs	UNICOMMUART_REGS	UC0_UART	0x4060_0000
Uc1uartRegs	UNICOMMUART_REGS	UC1_UART	0x4060_1000
Uc2uartRegs	UNICOMMUART_REGS	UC2_UART	0x4060_2000
Uc3uartRegs	UNICOMMUART_REGS	UC3_UART	0x4064_0000
Uc4uartRegs	UNICOMMUART_REGS	UC4_UART	0x4064_1000
Uc5uartRegs	UNICOMMUART_REGS	UC5_UART	0x4064_2000

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32.4.2 UNICOMMUART_REGS Registers

Table 32-8 lists the memory-mapped registers for the UNICOMMUART_REGS registers. All register offset addresses not listed in Table 32-8 should be considered as reserved locations and the register contents should not be modified.

Table 32-8. UNICOMMUART_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	CLKDIV	Clock Divider		Go
8h	CLKSEL	Clock Source Selection/Enable.		Go
18h	PDBGCTL	Peripheral Debug Control		Go
20h	IIDX	Interrupt index	CPU_INT	Go
28h	IMASK	Interrupt mask	CPU_INT	Go
30h	RIS	Raw interrupt status	CPU_INT	Go
38h	MIS	Masked interrupt status	CPU_INT	Go
40h	ISET	Interrupt set	CPU_INT	Go
48h	ICLR	Interrupt clear	CPU_INT	Go
58h	IMASK	Interrupt mask	DMA_TRIG_RX	Go
60h	RIS	Raw interrupt status	DMA_TRIG_RX	Go
68h	MIS	Masked interrupt status	DMA_TRIG_RX	Go
70h	ISET	Interrupt set	DMA_TRIG_RX	Go
88h	IMASK	Interrupt mask	DMA_TRIG_TX	Go
90h	RIS	Raw interrupt status	DMA_TRIG_TX	Go
98h	MIS	Masked interrupt status	DMA_TRIG_TX	Go
A0h	ISET	Interrupt set	DMA_TRIG_TX	Go
E4h	INTCTL	Interrupt control register		Go
100h	CTL0	UART Control Register 0		Go
104h	LCRH	UART Line Control Register		Go
108h	STAT	UART Status Register		Go
10Ch	IFLS	UART Interrupt FIFO Level Select Register		Go
110h	IBRD	UART Integer Baud-Rate Divisor Register		Go
114h	FBRD	UART Fractional Baud-Rate Divisor Register		Go
120h	TXDATA	UART Transmit Data Register		Go
124h	RXDATA	UART Receive Data Register		Go
130h	LINCNT	UART LIN Mode Counter Register		Go
134h	LINCTL	UART LIN Mode Control Register		Go
138h	LINC0	UART LIN Mode Capture 0 Register		Go
13Ch	LINC1	UART LIN Mode Capture 1 Register		Go
148h	AMASK	Self Address Mask Register		Go
14Ch	ADDR	Self Address Register		Go

Complex bit access types are encoded to fit into small table cells. Table 32-9 shows the codes that are used for access types in this section.

Table 32-9. UNICOMMUART_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

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Table 32-9. UNICOMMUART_REGS Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 CLKDIV Register (Offset = 0h) [Reset = 00000000h]

CLKDIV is shown in Figure 32-14 and described in Table 32-10.

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This register is used to specify the module-specific divide ratio of the UART functional clock (UARTclk).

Figure 32-14. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 32-11. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock. Division factor 0 : DIV_BY_1 1 : DIV_BY_2 .... 63: DIV_BY_64 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8 3Ch = Divide clock source by 61 3Dh = Divide clock source by 62 3Eh = Divide clock source by 63 3Fh = Divide clock source by 64

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2 CLKSEL Register (Offset = 8h) [Reset = 00000000h]

CLKSEL is shown in Figure 32-15 and described in Table 32-11.

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UART Clock Source Selection.

Figure 32-15. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				MCLKDIV2	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 32-13. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	MCLKDIV2	R/W	0h	Enables MCLKDIV2 as the UNICOMM UART clock source. 0h = Does not select this clock as a source 1h = Select this clock as a source
2-0	RESERVED	R/W	0h	

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3 PDBGCTL Register (Offset = 18h) [Reset = 00000000h]

PDBGCTL is shown in Figure 32-16 and described in Table 32-12.

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UART Debug Control. This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 32-16. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 32-15. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft halt boundary control. This function is only available, if [FREE] is set to 'STOP' 0h = Not supported 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free run control 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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4 IIDX Register (Offset = 20h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 32-17 and described in Table 32-13.

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This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 32-17. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 32-17. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	

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Table 32-17. IIDX Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	STAT	R	0h	UART Module Interrupt Vector Value. This register provides the highest priority interrupt index. A read clears the corresponding interrupt flag in RIS and MIS registers. 15h-1Fh = Reserved 00h = No interrupt pending 01h = UART receive time-out interrupt Interrupt Flag: RT Interrupt Priority: Highest 02h = UART framing error interrupt Interrupt Flag: FE 03h = UART parity error interrupt Interrupt Flag: PE 04h = UART break error interrupt Interrupt Flag: BE 05h = UART receive overrun error interrupt Interrupt Flag: OE 06h = Negative edge on UARTxRXD interrupt Interrupt Flag: RXNE 07h = Positive edge on UARTxRXD interrupt Interrupt Flag: RXPE 08h = LIN capture 0 / match interrupt Interrupt Flag: LINC0 09h = LIN capture 1 interrupt Interrupt Flag: LINC1 0Ah = LIN hardware counter overflow interrupt Interrupt Flag: LINOVF 0Bh = UART receive interrupt Interrupt Flag: RX 0Ch = UART transmit interrupt Interrupt Flag: TX 0Dh = UART end of transmission interrupt (transmit serializer empty) Interrupt Flag: EOT 0Eh = 9-bit mode address match interrupt Interrupt Flag: ADDR_MATCH Fh = UART Clear to Send Modem interrupt Interrupt Flag: CTS 10h = DMA DONE on RX 11h = DMA DONE on TX 12h = Noise Error Event 15h = UART line time-out interrupt Interrupt Flag

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5 IMASK Register (Offset = 28h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 32-18 and described in Table 32-14.

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Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 32-18. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED			LTOUT	RESERVED		NERR	DMA_DONE_TX
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	CTS	ADDR_MATCH	EOT	TXINT	RXINT	LINOVF	LINC1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
LINC0	RXPE	RXNE	OVRERR	BRKERR	PARERR	FRMERR	RTOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 32-19. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	0h	
20	LTOUT	R/W	0h	UART Line Time-Out Interrupt Mask. This interrupt is raised when no start edge has been detected for at least one character period when the UNICOMM-UART is receiving data. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
19-18	RESERVED	R/W	0h	
17	NERR	R/W	0h	UART Noise Error Interrupt Mask. This interrupt is raised when the 3 samples of majority voting are not equal. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
16	DMA_DONE_TX	R/W	0h	UART DMA Done on TX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the UART from a DMA configured with a DMA_TRIG_TX trigger publisher. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
15	DMA_DONE_RX	R/W	0h	UART DMA Done on RX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	CTS	R/W	0h	UART Clear to Send Modem Interrupt Mask. This interrupt is raised when the CTS input has been asserted low and data is ready to be transmitted on the TX line. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 32-19. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADDR_MATCH	R/W	0h	UART Address Match Interrupt Mask. This interrupt is raised when a match between the received address character (address bit set to '1') and the masked address configured by the ADDR and AMASK registers. Used in 9-bit UART mode, configured by the CTL0.MODE field. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	EOT	R/W	0h	UART End of Transmission Interrupt Mask. This interrupt is raised when the last bit of all transmitted data and flags, including the STOP bit, has left the serializer without any further data in the TX FIFO. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
11	TXINT	R/W	0h	UART Transmit Interrupt Mask. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10	RXINT	R/W	0h	UART Receive Interrupt Mask. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	LINOVF	R/W	0h	UART LIN Hardware Counter Overflow Interrupt Mask. This interrupt is raised when the 16-bit LINCNT register has overflowed. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	LINC1	R/W	0h	UART LIN Capture 1 Interrupt Mask. If LINCTL.LINC1_CAP=1: the interrupt is raised on each falling edge of RXD, indicating that the LINC1 captured the LINCNT value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	LINC0	R/W	0h	UART LIN Capture 0 / Match Interrupt Mask. If LINCTL.LINC0_CAP=1: the interrupt is raised on each rising edge of RXD, indicating that the LINC0 captured the LINCNT value. If LINCTL.LINC0_MATCH=1: the interrupt is raised when the LINCNT value is equal to the LINC0 value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	RXPE	R/W	0h	UART Positive Edge on UARTxRXD Interrupt Mask. This interrupt is raised when there is a rising edge on the receive line (generally used for LIN break field detection). 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	RXNE	R/W	0h	UART Negative Edge on UARTxRXD Interrupt Mask. This interrupt is raised when there is a falling edge on the receive line (generally used for LIN sync field detection). 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	OVRERR	R/W	0h	UART Receive Overrun Error Interrupt Mask. This interrupt is raised when the RX FIFO is full and a new character has been received. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3	BRKERR	R/W	0h	UART Break Error Interrupt Mask. This interrupt is raised when all data bits, parity bit and stop bits are '0' in the received character. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 32-19. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PARERR	R/W	0h	UART Parity Error Interrupt Mask. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	FRMERR	R/W	0h	UART Framing Error Interrupt Mask. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	RTOUT	R/W	0h	UART Receive Time-Out Interrupt Mask. This interrupt is raised when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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6 RIS Register (Offset = 30h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 32-19 and described in Table 32-15.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 32-19. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			LTOUT	RESERVED		NERR	DMA_DONE_TX
R-0h			R-0h	R-0h		R-0h	R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	CTS	ADDR_MATCH	EOT	TXINT	RXINT	LINOVF	LINC1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
LINC0	RXPE	RXNE	OVRERR	BRKERR	PARERR	FRMERR	RTOUT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 32-21. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	
20	LTOUT	R	0h	UART Line Time-Out Interrupt Raw Status. This interrupt is raised when no start edge has been detected for at least one character period when the UNICOMM-UART is receiving data. 0h = Interrupt did not occur 1h = Interrupt occurred
19-18	RESERVED	R	0h	
17	NERR	R	0h	UART Noise Error Interrupt Raw Status. This interrupt is raised when the 3 samples of majority voting are not equal. 0h = Interrupt did not occur 1h = Interrupt occurred
16	DMA_DONE_TX	R	0h	UART DMA Done on TX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Interrrupt did not occur 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	UART DMA Done on RX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Interrrupt did not occur 1h = Interrupt occurred
14	CTS	R	0h	UART Clear to Send Modem Interrupt Raw Status. This interrupt is raised when the CTS input has been asserted low and data is ready to be transmitted on the TX line. 0h = Interrrupt did not occur 1h = Interrupt occurred

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Table 32-21. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADDR_MATCH	R	0h	UART Address Match Interrupt Raw Status. This interrupt is raised when a match between the received address character (address bit set to '1') and the masked address configured by the ADDR and AMASK registers. Used in 9-bit UART mode, configured by the CTL0.MODE field. 0h = Interrupt did not occur 1h = Interrupt occurred
12	EOT	R	0h	UART End of Transmission Interrupt Raw Status. This interrupt is raised when the last bit of all transmitted data and flags, including the STOP bit, has left the serializer without any further data in the TX FIFO. 0h = Interrupt did not occur 1h = Interrupt occurred
11	TXINT	R	0h	UART Transmit Interrupt Raw Status. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur 1h = Interrupt occurred
10	RXINT	R	0h	UART Receive Interrupt Raw Status. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur 1h = Interrupt occurred
9	LINOVF	R	0h	UART LIN Hardware Counter Overflow Interrupt Raw Status. This interrupt is raised when the 16-bit LINCNT register has overflowed. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur 1h = Interrupt occurred
8	LINC1	R	0h	UART LIN Capture 1 Interrupt Raw Status. If LINCTL.LINC1_CAP=1: the interrupt is raised on each falling edge of RXD, indicating that the LINC1 captured the LINCNT value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur 1h = Interrupt occurred
7	LINC0	R	0h	UART LIN Capture 0 / Match Interrupt Raw Status. If LINCTL.LINC0_CAP=1: the interrupt is raised on each rising edge of RXD, indicating that the LINC0 captured the LINCNT value. If LINCTL.LINC0_MATCH=1: the interrupt is raised when the LINCNT value is equal to the LINC0 value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur 1h = Interrupt occurred
6	RXPE	R	0h	UART Positive Edge on UARTxRXD Interrupt Raw Status. This interrupt is raised when there is a rising edge on the receive line (generally used for LIN break field detection). 0h = Interrupt did not occur 1h = Interrupt occurred
5	RXNE	R	0h	UART Negative Edge on UARTxRXD Interrupt Raw Status. This interrupt is raised when there is a falling edge on the receive line (generally used for LIN sync field detection). 0h = Interrupt did not occur 1h = Interrupt occurred
4	OVRERR	R	0h	UART Receive Overrun Error Interrupt Raw Status. This interrupt is raised when the RX FIFO is full and a new character has been received. 0h = Interrupt did not occur 1h = Interrupt occurred
3	BRKERR	R	0h	UART Break Error Interrupt Raw Status. This interrupt is raised when all data bits, parity bit and stop bits are '0' in the received character. 0h = Interrupt did not occur 1h = Interrupt occurred

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Table 32-21. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PARERR	R	0h	UART Parity Error Interrupt Raw Status. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Interrupt did not occur 1h = Interrupt occurred
1	FRMERR	R	0h	UART Framing Error Interrupt Raw Status. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Interrupt did not occur 1h = Interrupt occurred
0	RTOUT	R	0h	UART Receive Time-Out Interrupt Raw Status. This interrupt is raised when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Interrupt did not occur 1h = Interrupt occurred

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7 MIS Register (Offset = 38h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 32-20 and described in Table 32-16.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 32-20. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			LTOUT	RESERVED		NERR	DMA_DONE_TX
R-0h			R-0h	R-0h		R-0h	R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	CTS	ADDR_MATCH	EOT	TXINT	RXINT	LINOVF	LINC1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
LINC0	RXPE	RXNE	OVRERR	BRKERR	PARERR	FRMERR	RTOUT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 32-23. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	
20	LTOUT	R	0h	UART Line Time-Out Interrupt Masked Status. This interrupt is raised when no start edge has been detected for at least one character period when the UNICOMM-UART is receiving data. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
19-18	RESERVED	R	0h	
17	NERR	R	0h	UART Noise Error Interrupt Masked Status. This interrupt is raised when the 3 samples of majority voting are not equal. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
16	DMA_DONE_TX	R	0h	UART DMA Done on TX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	UART DMA Done on RX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
14	CTS	R	0h	UART Clear to Send Modem Interrupt Masked Status. This interrupt is raised when the CTS input has been asserted low and data is ready to be transmitted on the TX line. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred

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Table 32-23. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADDR_MATCH	R	0h	UART Address Match Interrupt Masked Status. This interrupt is raised when a match between the received address character (address bit set to '1') and the masked address configured by the ADDR and AMASK registers. Used in 9-bit UART mode, configured by the CTL0.MODE field. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
12	EOT	R	0h	UART End of Transmission Interrupt Raw Status. This interrupt is raised when the last bit of all transmitted data and flags, including the STOP bit, has left the serializer without any further data in the TX FIFO. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
11	TXINT	R	0h	UART Transmit Interrupt Raw Status. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
10	RXINT	R	0h	UART Receive Interrupt Raw Status. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
9	LINOVF	R	0h	UART LIN Hardware Counter Overflow Interrupt Masked Status. This interrupt is raised when the 16-bit LINCNT register has overflowed. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
8	LINC1	R	0h	UART LIN Capture 1 Interrupt Masked Status. If LINCTL.LINC1_CAP=1: the interrupt is raised on each falling edge of RXD, indicating that the LINC1 captured the LINCNT value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
7	LINC0	R	0h	UART LIN Capture 0 / Match Interrupt Masked Status. If LINCTL.LINC0_CAP=1: the interrupt is raised on each rising edge of RXD, indicating that the LINC0 captured the LINCNT value. If LINCTL.LINC0_MATCH=1: the interrupt is raised when the LINCNT value is equal to the LINC0 value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
6	RXPE	R	0h	UART Positive Edge on UARTxRXD Interrupt Masked Status. This interrupt is raised when there is a rising edge on the receive line (generally used for LIN break field detection). 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
5	RXNE	R	0h	UART Negative Edge on UARTxRXD Interrupt Masked Status. This interrupt is raised when there is a falling edge on the receive line (generally used for LIN sync field detection). 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
4	OVRERR	R	0h	UART Receive Overrun Error Interrupt Masked Status. This interrupt is raised when the RX FIFO is full and a new character has been received. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred

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Table 32-23. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BRKERR	R	0h	UART Break Error Interrupt Masked Status. This interrupt is raised when all data bits, parity bit and stop bits are '0' in the received character. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
2	PARERR	R	0h	UART Parity Error Interrupt Masked Status. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
1	FRMERR	R	0h	UART Framing Error Interrupt Masked Status. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred
0	RTOUT	R	0h	UART Receive Time-Out Interrupt Masked Status. This interrupt is raised when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Interrupt did not occur or mask was disabled 1h = Interrupt occurred

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8 ISET Register (Offset = 40h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 32-21 and described in Table 32-17.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 32-21. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED			LTOUT	RESERVED		NERR	DMA_DONE_TX
W-0h			W-0h	W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	CTS	ADDR_MATCH	EOT	TXINT	RXINT	LINOVF	LINC1
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
LINC0	RXPE	RXNE	OVRERR	BRKERR	PARERR	FRMERR	RTOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 32-25. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	W	0h	
20	LTOUT	W	0h	Set UART Line Time-Out Interrupt. This interrupt is raised when no start edge has been detected for at least one character period when the UNICOMM-UART is receiving data. 0h = Writing 0 has no effect 1h = Set Interrupt
19-18	RESERVED	W	0h	
17	NERR	W	0h	Set UART Noise Error Interrupt. This interrupt is raised when the 3 samples of majority voting are not equal. 0h = Writing 0 has no effect 1h = Set the interrupt
16	DMA_DONE_TX	W	0h	Set UART DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt
15	DMA_DONE_RX	W	0h	Set UART DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt
14	CTS	W	0h	Set UART Clear to Send Modem Interrupt. This interrupt is raised when the CTS input has been asserted low and data is ready to be transmitted on the TX line. 0h = Writing 0 has no effect 1h = Set Interrupt

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Table 32-25. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADDR_MATCH	W	0h	Set UART Address Match Interrupt. This interrupt is raised when a match between the received address character (address bit set to '1') and the masked address configured by the ADDR and AMASK registers. Used in 9-bit UART mode, configured by the CTL0.MODE field. 0h = Writing 0 has no effect 1h = Set Interrupt
12	EOT	W	0h	Set UART End of Transmission Interrupt. This interrupt is raised when the last bit of all transmitted data and flags, including the STOP bit, has left the serializer without any further data in the TX FIFO. 0h = Writing 0 has no effect 1h = Set Interrupt
11	TXINT	W	0h	Set UART Transmit Interrupt. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Set Interrupt
10	RXINT	W	0h	Set UART Receive Interrupt. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Set Interrupt
9	LINOVF	W	0h	Set UART LIN Hardware Counter Overflow Interrupt. This interrupt is raised when the 16-bit LINCNT register has overflowed. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Set Interrupt
8	LINC1	W	0h	Set UART LIN Capture 1 Interrupt. If LINCTL.LINC1_CAP=1: the interrupt is raised on each falling edge of RXD, indicating that the LINC1 captured the LINCNT value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Set Interrupt
7	LINC0	W	0h	Set UART LIN Capture 0 / Match Interrupt. If LINCTL.LINC0_CAP=1: the interrupt is raised on each rising edge of RXD, indicating that the LINC0 captured the LINCNT value. If LINCTL.LINC0_MATCH=1: the interrupt is raised when the LINCNT value is equal to the LINC0 value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Set Interrupt
6	RXPE	W	0h	Set UART Positive Edge on UARTxRXD Interrupt. This interrupt is raised when there is a rising edge on the receive line (generally used for LIN break field detection). 0h = Writing 0 has no effect 1h = Set Interrupt
5	RXNE	W	0h	Set UART Negative Edge on UARTxRXD Interrupt. This interrupt is raised when there is a falling edge on the receive line (generally used for LIN sync field detection). 0h = Writing 0 has no effect 1h = Set Interrupt
4	OVRERR	W	0h	Set UART Receive Overrun Error Interrupt. This interrupt is raised when the RX FIFO is full and a new character has been received. 0h = Writing 0 has no effect 1h = Set Interrupt
3	BRKERR	W	0h	Set UART Break Error Interrupt. This interrupt is raised when all data bits, parity bit and stop bits are '0' in the received character. 0h = Writing 0 has no effect 1h = Set Interrupt

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Table 32-25. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PARERR	W	0h	Set UART Parity Error Interrupt. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Writing 0 has no effect 1h = Set Interrupt
1	FRMERR	W	0h	Set UART Framing Error Interrupt. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Writing 0 has no effect 1h = Set Interrupt
0	RTOUT	W	0h	Set UART Receive Time-Out Interrupt. This interrupt is raised when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Writing 0 has no effect 1h = Set Interrupt

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9 ICLR Register (Offset = 48h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 32-22 and described in Table 32-18.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 32-22. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED			LTOUT	RESERVED		NERR	DMA_DONE_TX
W-0h			W-0h	W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	CTS	ADDR_MATCH	EOT	TXINT	RXINT	LINOVF	LINC1
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
LINC0	RXPE	RXNE	OVRERR	BRKERR	PARERR	FRMERR	RTOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 32-27. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	W	0h	
20	LTOUT	W	0h	Clear UART Line Time-Out Interrupt. This interrupt is raised when no start edge has been detected for at least one character period when the UNICOMM-UART is receiving data. 0h = Writing 0 has no effect 1h = Clear Interrupt
19-18	RESERVED	W	0h	
17	NERR	W	0h	Clear UART Noise Error Interrupt. This interrupt is raised when the 3 samples of majority voting are not equal. 0h = Writing 0 has no effect 1h = Clear Interrupt
16	DMA_DONE_TX	W	0h	Clear UART DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the UART from a DMA configured with a DMA_TRIG_TX trigger publisher. 0h = Writing 0 has no effect 1h = Clear Interrupt
15	DMA_DONE_RX	W	0h	Clear UART DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the UART from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Clear Interrupt
14	CTS	W	0h	Clear UART Clear to Send Modem Interrupt. This interrupt is raised when the CTS input has been asserted low and data is ready to be transmitted on the TX line. 0h = Writing 0 has no effect 1h = Clear Interrupt

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Table 32-27. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ADDR_MATCH	W	0h	Clear UART Address Match Interrupt. This interrupt is raised when a match between the received address character (address bit set to '1') and the masked address configured by the ADDR and AMASK registers. Used in 9-bit UART mode, configured by the CTL0.MODE field. 0h = Writing 0 has no effect 1h = Clear Interrupt
12	EOT	W	0h	Clear UART End of Transmission Interrupt. This interrupt is raised when the last bit of all transmitted data and flags, including the STOP bit, has left the serializer without any further data in the TX FIFO. 0h = Writing 0 has no effect 1h = Clear Interrupt
11	TXINT	W	0h	Clear UART Transmit Interrupt. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Clear Interrupt
10	RXINT	W	0h	Clear UART Receive Interrupt. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Clear Interrupt
9	LINOVF	W	0h	Clear UART LIN Hardware Counter Overflow Interrupt. This interrupt is raised when the 16-bit LINCNT register has overflowed. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Clear Interrupt
8	LINC1	W	0h	Clear UART LIN Capture 1 Interrupt. If LINCTL.LINC1_CAP=1: the interrupt is raised on each falling edge of RXD, indicating that the LINC1 captured the LINCNT value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Clear Interrupt
7	LINC0	W	0h	Clear UART LIN Capture 0 / Match Interrupt. If LINCTL.LINC0_CAP=1: the interrupt is raised on each rising edge of RXD, indicating that the LINC0 captured the LINCNT value. If LINCTL.LINC0_MATCH=1: the interrupt is raised when the LINCNT value is equal to the LINC0 value. Interrupt only valid for Basic+ UNICOMM UART instances. 0h = Writing 0 has no effect 1h = Clear Interrupt
6	RXPE	W	0h	Clear UART Positive Edge on UARTxRXD Interrupt. This interrupt is raised when there is a rising edge on the receive line (generally used for LIN break field detection). 0h = Writing 0 has no effect 1h = Clear Interrupt
5	RXNE	W	0h	Clear UART Negative Edge on UARTxRXD Interrupt. This interrupt is raised when there is a falling edge on the receive line (generally used for LIN sync field detection). 0h = Writing 0 has no effect 1h = Clear Interrupt
4	OVRERR	W	0h	Clear UART Receive Overrun Error Interrupt. This interrupt is raised when the RX FIFO is full and a new character has been received. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	BRKERR	W	0h	Clear UART Break Error Interrupt. This interrupt is raised when all data bits, parity bit and stop bits are '0' in the received character. 0h = Writing 0 has no effect 1h = Clear Interrupt

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Table 32-27. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PARERR	W	0h	Clear UART Framing Error Interrupt. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Writing 0 has no effect 1h = Clear Interrupt
1	FRMERR	W	0h	Clear UART Framing Error Interrupt. This interrupt is raised when an expected stop bit is not found, meaning synchronization with the start bit has been lost and that the character is incorrectly framed. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	RTOUT	W	0h	Clear UART Receive Time-Out Interrupt. This interrupt is raised when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Writing 0 has no effect 1h = Clear Interrupt

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10 IMASK Register (Offset = 58h) [Reset = 00000000h] (DMA_TRIG_RX)

IMASK is shown in Figure 32-23 and described in Table 32-19.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 32-23. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					RXINT	RESERVED	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							RTOUT
R/W-0h							R/W-0h

Table 32-29. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	0h	
10	RXINT	R/W	0h	UART Receive DMA Trigger Interrupt Mask. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9-1	RESERVED	R/W	0h	
0	RTOUT	R/W	0h	UART Receive Timeout DMA Trigger Mask. This DMA is triggered when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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11 RIS Register (Offset = 60h) [Reset = 00000000h] (DMA_TRIG_RX)

RIS is shown in Figure 32-24 and described in Table 32-20.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme.

Figure 32-24. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					RXINT	RESERVED	
R-0h					R-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED							RTOUT
R-0h							R-0h

Table 32-31. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	
10	RXINT	R	0h	UART Receive DMA Trigger Interrupt Raw Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
9-1	RESERVED	R	0h	
0	RTOUT	R	0h	UART Receive Timeout DMA Trigger Raw Status. This DMA is triggered when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Interrupt did not occur 1h = Interrupt occurred

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12 MIS Register (Offset = 68h) [Reset = 00000000h] (DMA_TRIG_RX)

MIS is shown in Figure 32-25 and described in Table 32-21.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 32-25. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					RXINT	RESERVED	
R-0h					R-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED							RTOUT
R-0h							R-0h

Table 32-33. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	
10	RXINT	R	0h	UART Receive DMA Trigger Interrupt Raw Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
9-1	RESERVED	R	0h	
0	RTOUT	R	0h	UART Receive Timeout DMA Trigger Masked Status. This DMA is triggered when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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13 ISET Register (Offset = 70h) [Reset = 00000000h] (DMA_TRIG_RX)

ISET is shown in Figure 32-26 and described in Table 32-22.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 32-26. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED					RXINT	RESERVED	
W-0h					W-0h	W-0h	
7	6	5	4	3	2	1	0
RESERVED							RTOUT
W-0h							W-0h

Table 32-35. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	W	0h	
10	RXINT	W	0h	Set UART Receive DMA Trigger Interrupt. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
9-1	RESERVED	W	0h	
0	RTOUT	W	0h	Set UART Receive Timeout DMA Trigger. This DMA is triggered when receiving data if there is at least one element in the RX FIFO and there is no start edge detected for an additional character period (frame period: calculated as per clock and baud rate settings), regardless of if the RX FIFO level configured in the IFLS register has been reached. 0h = Writing 0 has no effect 1h = Set Interrupt

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14 IMASK Register (Offset = 88h) [Reset = 00000000h] (DMA_TRIG_TX)

IMASK is shown in Figure 32-27 and described in Table 32-23.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 32-27. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				TXINT	RESERVED		
R/W-0h				R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

Table 32-37. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	0h	
11	TXINT	R/W	0h	UART Transmit DMA Trigger Interrupt Mask. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
10-0	RESERVED	R/W	0h	

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15 RIS Register (Offset = 90h) [Reset = 00000000h] (DMA_TRIG_TX)

RIS is shown in Figure 32-28 and described in Table 32-24.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking.

Figure 32-28. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				TXINT	RESERVED		
R-0h				R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 32-39. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	
11	TXINT	R	0h	UART Transmit DMA Trigger Interrupt Raw Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
10-0	RESERVED	R	0h	

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16 MIS Register (Offset = 98h) [Reset = 00000000h] (DMA_TRIG_TX)

MIS is shown in Figure 32-29 and described in Table 32-25.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 32-29. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				TXINT	RESERVED		
R-0h				R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 32-41. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	
11	TXINT	R	0h	UART Transmit DMA Trigger Interrupt Raw Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
10-0	RESERVED	R	0h	

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17 ISET Register (Offset = A0h) [Reset = 00000000h] (DMA_TRIG_TX)

ISET is shown in Figure 32-30 and described in Table 32-26.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 32-30. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED				TXINT	RESERVED		
W-0h				W-0h	W-0h		
7	6	5	4	3	2	1	0
RESERVED							
W-0h							

Table 32-43. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	W	0h	
11	TXINT	W	0h	Set UART Transmit DMA Trigger Interrupt. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
10-0	RESERVED	W	0h	

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18 INTCTL Register (Offset = E4h) [Reset = 00000000h]

INTCTL is shown in Figure 32-31 and described in Table 32-27.

Return to the Summary Table.

Interrupt Control Register.

Figure 32-31. INTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTEVAL
W-0h							W-0h

Table 32-45. INTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTEVAL	W	0h	Writing a 1 to this field re-evaluates the interrupt sources. 0h = Writing 0 has no effect 1h = Interrupt Eval

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19 CTL0 Register (Offset = 100h) [Reset = 00000038h]

CTL0 is shown in Figure 32-32 and described in Table 32-28.

Return to the Summary Table.

UART Control Register. All the bits are cleared on reset except for the Transmit Enable (TXE) and Receive Enable (RXE) bits, which are set. To enable the UART module, the CTL0.ENABLE bit must be set. If software requires a configuration change in the module, the ENABLE bit must be cleared before the configuration changes are written. If the UART is disabled during a transmit or receive operation, the current transaction is completed prior to the UART stopping. NOTE: The CTL0 register should not be changed while the UART is enabled or else the results are unpredictable. The following sequence is recommended for making changes to the CTL0 register. 1. Disable the UART (CTL0.ENABLE=0). 2. Wait for the end of transmission or reception of the current character. 3. Clear transmit FIFO (set IFLS.TXCLR=1, wait for STAT.TXCLR=1, IFLS.TXCLR=0) 4. Reprogram the CTL0 register. 5. Enable the UART (CTL0.ENABLE=1).

Figure 32-32. CTL0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				MSBFIRST	MAJVOTE	RESERVED	HSE
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
HSE	CTSEN	RTSEN	RTS	RESERVED	MODE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	TXD_OUT	TXD_OUT_EN	TXE	RXE	LBE	RESERVED	ENABLE
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 32-47. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	0h	
19	MSBFIRST	R/W	0h	Most Significant Bit First. This bit has effect both on the way protocol byte is transmitted and received. Notes: User needs to match the protocol to the correct value of this bit to send MSb or LSb first. The hardware engine will send the byte entirely based on this bit. 0h = Least significant bit is sent first in the protocol packet 1h = Most significant bit is sent first in the protocol packet
18	MAJVOTE	R/W	0h	Majority Vote Enable. When Majority Voting is enabled, the three center bits are used to determine received sample value. In case of error (i.e. all 3 bits are not the same), noise error is detected and bits RIS.NERR and register RXDATA.NERR are set. Oversampling of 16 : bits 7, 8, 9 are used Oversampling of 8 : bits 3, 4, 5 are used Disabled : Single sample value (center value) used 0h = Majority voting is disabled 1h = Majority voting is enabled
17	RESERVED	R/W	0h	

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Table 32-47. CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-15	HSE	R/W	0h	High-Speed Bit Oversampling Enable. **NOTE:** The bit oversampling setting influences the UART baud rate configuration. The state of this bit has no effect on clock generation in ISO7816 smart card mode (when the CTL0.MODE is set to SMART in Basic UNICOMM instances). 0h = 16x oversampling. 1h = 8x oversampling. 2h = 3x oversampling. ISO7816 Smartcard mode (CTL0.MODE=4h) is not supported when 3x oversampling is enabled.
14	CTSEN	R/W	0h	Clear To Send (CTS) Enable. 0h = CTS hardware flow control is disabled. 1h = CTS hardware flow control is enabled. Data is only transmitted when the UARTxCTS signal is asserted.
13	RTSEN	R/W	0h	Request to Send (RTS) Enable. Enable hardware controlled Request to Send. 0h = RTS hardware flow control is disabled. 1h = RTS hardware flow control is enabled. Data is only requested (by asserting CTL0.RTS) when the RX FIFO has available entries.
12	RTS	R/W	0h	Request to Send. If RTSEN is set, the RTS output signals is controlled by the hardware logic using the programmed IFLS FIFO fill level. If RTSEN is cleared, the RTS output is controlled by the RTS bit. The bit is the complement of the UART request to send, RTS modem status output. 0h = Signal not RTS 1h = Signal RTS
11	RESERVED	R/W	0h	
10-8	MODE	R/W	0h	UART Communication Mode. Set the communication mode and protocol used. (Undefined settings uses the default setting: 0) 0h = Normal operation. 1h = RS485 Mode: UART needs to be IDLE with receiving data for the in LCRH.EXTDIR_HOLD set time. EXTDIR_SETUP defines the time the RTS line is set to high before sending. When the RX FIFO is empty, the RTS line is set low again. A transmit will be delayed as long the UART is receiving data. 2h = The UART operates in IDLE Line Mode. 3h = The UART operates in 9 Bit Address mode. 4h = ISO7816 Smart Card Mode. Only valid for Basic UNICOMM instances. The application must ensure that it sets 8-bit word length (WLEN set to 3h) and even parity (PEN set to 1, EPS set to 1, SPS set to 0) in the LCRH register when using ISO7816 mode. The value of the STP2 bit in UARTLCRH is ignored and the number of stop bits is forced to 2.
7	RESERVED	R/W	0h	
6	TXD_OUT	R/W	0h	TXD Pin Control Controls the TXD pin when TXD_OUT_EN = 1 and TXE = 0. 0h = TXD pin is low 1h = TXD pin is high
5	TXD_OUT_EN	R/W	1h	TXD Pin Control Enable. When the transmit section of the UART is disabled (TXE = 0), the TXD pin can be controlled by the TXD_OUT bit. 0h = TXD pin can not be controlled by TXD_OUT 1h = TXD pin can be controlled by TXD_OUT
4	TXE	R/W	1h	UART Transmit Enable. If the UART is disabled in the middle of a transmission, it completes the current character before stopping. **NOTE:** To enable transmission, the CTL0.ENABLE bit must be set. 0h = The transmit section of the UART is disabled. The UARTxTXD pin of the UART can be controlled by the TXD_CTL bit when enabled. 1h = The transmit section of the UART is enabled.

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Table 32-47. CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RXE	R/W	1h	UART Receive Enable. If the UART is disabled in the middle of a receive, it completes the current character before stopping. **NOTE:** To enable reception, the CTL0.ENABLE bit must be set. 0h = The receive section of the UART is disabled. 1h = The receive section of the UART is enabled.
2	LBE	R/W	0h	UART Internal Loopback Mode Enable. 0h = Normal operation. 1h = The UARTxTX path is fed through the UARTxRX path internally.
1	RESERVED	R/W	0h	
0	ENABLE	R/W	0h	UART Module Enable. If the UART is disabled in the middle of transmission or reception, it completes the current character before stopping. If the ENABLE bit is not set, all registers can still be accessed and updated. It is recommended to setup and change the UART operation mode with having the ENABLE bit cleared to avoid unpredictable behavior during the setup or update. If disabled the UART module will not send or receive any data and the logic is held in reset state. 0h = Disable Module 1h = Enable module

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20 LCRH Register (Offset = 104h) [Reset = 00000000h]

LCRH is shown in Figure 32-33 and described in Table 32-29.

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UART Line Control Register. The LCRH register is the line control register. Serial parameters such as data length, parity, and stop bit selection are implemented in this register.

Figure 32-33. LCRH Register

31	30	29	28	27	26	25	24
RESERVED					SUSPEND	EXTDIR_HOLD	
R/W-0h					R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
EXTDIR_HOLD			EXTDIR_SETUP				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
SENDIDLE	SPS	WLEN		STP2	EPS	PEN	BRK
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 32-49. LCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	0h	
26	SUSPEND	R/W	0h	Suspend External Communication. When this bit is set, UART communication on the external line is suspended after the UART TX FIFO is drained and the UART FSM goes idle (SR.BUSY reads '0'). 0h = Functional mode resumed 1h = External communication suspended
25-21	EXTDIR_HOLD	R/W	0h	Defines the number of UARTclk ticks the signal to control the external driver for the RS485 will be reset after the beginning of the stop bit. (If 2 STOP bits are enabled the beginning of the 2nd STOP bit.) 0h = Smallest value 1Fh = Highest possible value
20-16	EXTDIR_SETUP	R/W	0h	Defines the number of UARTclk ticks the signal to control the external driver for the RS485 will be set before the START bit is send 0h = Smallest value 1Fh = Highest possible value
15-8	RESERVED	R/W	0h	
7	SENDIDLE	R/W	0h	UART send IDLE pattern. When this bit is set, an IDLE period of 11 bits is sent on the TX line. Used in idle-line multiprocessor mode (CTL0.MODE=IDLELINE). Read the STAT.SENDIDLE bit to read back the current status of the SENDIDLE operation. 0h = Normal operation 1h = Send Idle Pattern

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Table 32-49. LCRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SPS	R/W	0h	UART Stick Parity Select. The Stick Parity Select (SPS) bit is used to set either a permanent '1' or a permanent '0' as parity when transmitting or receiving data. Its purpose is to typically indicate the first byte of a package or to mark an address byte, for example in a multi-drop RS-485 network. When bits PEN, EPS, and SPS of UARTLCRH are set, the parity bit is transmitted and checked as a 0. When bits PEN and SPS are set and EPS is cleared, the parity bit is transmitted and checked as a 1. 0h = Disable Stick Parity 1h = Enable Stick Parity
5-4	WLEN	R/W	0h	UART Word Length. The bits indicate the number of data bits transmitted or received in a frame as follows: 0h = 5 bits (default) 1h = 6 bits 2h = 7 bits 3h = 8 bits
3	STP2	R/W	0h	UART Two Stop Bits Select. When in 7816 smart card mode (the SMART bit is set in the UARTCTL register), the number of stop bits is forced to 2. 0h = One stop bit is transmitted at the end of a frame. 1h = Two stop bits are transmitted at the end of a frame. The receive logic checks for two stop bits being received and provide Frame Error if either is invalid.
2	EPS	R/W	0h	UART Even Parity Select. This bit has no effect when parity is disabled by the PEN bit. For 9-Bit UART Mode transmissions, this bit controls the address byte and data byte indication (9th bit). 0 = The transferred byte is a data byte 1 = The transferred byte is an address byte 0h = Odd parity is performed, which checks for an odd number of 1s. 1h = Even parity generation and checking is performed during transmission and reception, which checks for an even number of 1s in data and parity bits.
1	PEN	R/W	0h	UART Parity Enable. 0h = Parity is disabled and no parity bit is added to the data frame. 1h = Parity checking and generation is enabled.
0	BRK	R/W	0h	UART Send Break (for LIN Protocol). 1. Break condition is sent on the line for as long as this bit is set 0h = Normal operation 1h = A low level is continually output on the UARTxTXD signal, after completing transmission of the current character. For the proper execution of the break command, software must set this bit for at least two frames (character periods).

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21 STAT Register (Offset = 108h) [Reset = 00000000h]

STAT is shown in Figure 32-34 and described in Table 32-30.

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UART Status Register.

Figure 32-34. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					SENDIDLE	IDLE	CTS
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TXCLR	TXFF	TXFE	RXCLR	RXFF	RXFE	RESERVED	BUSY
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 32-51. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	
10	SENDIDLE	R	0h	Send Idle Operation Status. Used in idle-line multiprocessor mode (CTL0.MODE=IDLELINE). 0h = IDLE condition has not yet been sent on the line 1h = IDLE condition has been sent on the line
9	IDLE	R	0h	UART Idle-line status. IDLE mode has been detected in Idleline-Multiprocessor-Mode. The IDLE bit is used as an address tag for each block of characters. In idle-line multiprocessor format, this bit is set when a received character is an address. 0h = IDLE has not been detected before last received character. (In idle-line multiprocessor mode). 1h = IDLE has been detected before last received character. (In idle-line multiprocessor mode).
8	CTS	R	1h	UART Clear To Send Status. If CTS flow control is enabled (CTL0.CTSEN), the UNICOMM-UART transmitter checks that this bit is low before sending the next byte. 0h = The CTS signal is not asserted (high). 1h = The CTS signal is asserted (low).
7	TXCLR	R	0h	UART TX FIFO Clear Status. 0h = TX FIFO is not cleared 1h = TX FIFO clear is complete
6	TXFF	R	0h	UART TX FIFO Full Status. 0h = TX FIFO is not full 1h = TX FIFO is full
5	TXFE	R	1h	UART TX FIFO Empty Status. 0h = TX FIFO is empty 1h = TX FIFO is empty
4	RXCLR	R	0h	UART RX FIFO Clear Status. 0h = RX FIFO is not cleared 1h = RX FIFO clear is complete
3	RXFF	R	0h	UART RX FIFO Full Status. 0h = RX FIFO is not full 1h = RX FIFO is full

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Table 32-51. STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RXFE	R	1h	UART RX FIFO Empty Status. 0h = RX FIFO is not empty 1h = RX FIFO is empty
1	RESERVED	R	0h	
0	BUSY	R	0h	UART Busy Status. This bit is set as soon as the TX FIFO becomes non-empty or if a receive data is currently ongoing (after the start edge have been detected until a complete byte, including all stop bits, has been received by the shift register). In IDLE_Line mode, the BUSY signal also stays set during the idle time generation. This bit is set only when the module in enabled. 0h = The UART is not busy. 1h = The UART is busy transmitting data. This bit remains set until the complete byte, including all stop bits, has been sent/received from/into the shift register.

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22 IFLS Register (Offset = 10Ch) [Reset = 00000022h]

IFLS is shown in Figure 32-35 and described in Table 32-31.

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Interrupt FIFO Level Select. Use this register to define the levels at which the TX, RX and timeout interrupt flags are triggered. The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered when the RX FIFO is filled with two or more characters. Out of reset, the TXIFLSEL and RXIFLSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Figure 32-35. IFLS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				RXTOSEL			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RXCLR	RXIFLSEL			TXCLR	TXIFLSEL		
R/W-0h	R/W-2h			R/W-0h	R/W-2h		

Table 32-53. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	0h	
11-8	RXTOSEL	R/W	0h	UART Receive Interrupt Timeout Select. Configures the number of bits (at the programmed baud rate), used by the UART when there is no start edge received, to flag/trigger a timeout condition (RTOUT or LTOUT). A value of 0 disables the timeout functions. 0h = Smallest value Fh = Highest possible value
7	RXCLR	R/W	0h	RX FIFO Clear. Setting this bit will clear the RX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
6-4	RXIFLSEL	R/W	2h	RX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Opposite of empty 5h = RX FIFO is full 6h = RX_FIFO >= (MAX_FIFO_LEN -1) 7h = RX_FIFO <= 1
3	TXCLR	R/W	0h	TX FIFO Clear. Setting this bit will clear the TX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear

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Table 32-53. IFLS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	TXIFLSEL	R/W	2h	TX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Opposite of full 5h = TX FIFO is empty 6h = TX FIFO <= 1 7h = TX_FIFO >= (MAX_FIFO_LEN -1)

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23 IBRD Register (Offset = 110h) [Reset = 00000000h]

IBRD is shown in Figure 32-36 and described in Table 32-32.

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UART Integer Baud-Rate Divisor Register. When changing the IBRD register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register. See Baud-Rate Generation chapter for configuration details.

Figure 32-36. IBRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DIVINT															
R/W-0h																R/W-0h															

Table 32-55. IBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	DIVINT	R/W	0h	Integer Baud-Rate Divisor BRD = UARTclk / ((HSE Oversampling)*(Baud rate)). Program the integer portion of BRD to this register field. 0h = Smallest value FFFFh = Highest possible value

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24 FBRD Register (Offset = 114h) [Reset = 00000000h]

FBRD is shown in Figure 32-37 and described in Table 32-33.

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UART Fractional Baud-Rate Divisor Register. The FBRD register is the fractional part of the baud-rate divisor value. All the bits are cleared on reset. When changing the FBRD register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register. See Baud-Rate Generation chapter for configuration details.

Figure 32-37. FBRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										DIVFRAC					
R/W-0h										R/W-0h					

Table 32-57. FBRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5-0	DIVFRAC	R/W	0h	Fractional Baud-Rate Divisor BRD = UARTclk / ((HSE Oversampling)*(Baud rate)). Program the (fractional portion of BRD*64 + 0.5) rounded up to the nearest integer to this register field. 0h = Smallest value 3Fh = Highest possible value

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25 TXDATA Register (Offset = 120h) [Reset = 00000000h]

TXDATA is shown in Figure 32-38 and described in Table 32-34.

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UART Transmit Data Register. This register is the transmit data register (the interface to the FIFOs). For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the TX FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the TX FIFO). A write to this register initiates a transmission from the UART.

Figure 32-38. TXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
W-0h																								W-0h							

Table 32-59. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	W	0h	
7-0	DATA	W	0h	Data Transmitted or Received Data that is to be transmitted via the UART is written to this field. When read, this field contains the data that was received by the UART. 0h = Smallest value FFh = Highest possible value

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26 RXDATA Register (Offset = 124h) [Reset = 00000000h]

RXDATA is shown in Figure 32-39 and described in Table 32-35.

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UART Receive Data Register. This register is the data receive register (the interface to the FIFOs). For received data, if the FIFO is enabled, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide RX FIFO. If the FIFO is disabled, the data byte and status are stored in the receiving holding register (the bottom word of the RX FIFO). The received data can be retrieved by reading this register.

Figure 32-39. RXDATA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				NERR	BRKERR	PARERR	FRMERR
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DATA							
R-0h							

Table 32-61. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	
11	NERR	R	0h	Noise Error. Writing to this bit has no effect. The flag is cleared by writing 1 to the NERR bit in the UART EVENT ICLR register. 0h = No noise error occurred 1h = Noise error occurred during majority voting
10	BRKERR	R	0h	UART Break Error. Writing to this bit has no effect. The flag is cleared by writing 1 to the BRKERR bit in the UART EVENT ICLR register. This error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state) and the next valid start bit is received. 0h = No break condition has occurred 1h = A break condition has been detected, indicating that the receive data input was held low for longer than a full-word transmission time (defined as start, data, parity, and stop bits).
9	PARERR	R	0h	UART Parity Error. Writing to this bit has no effect. The flag is cleared by writing 1 to the PARERR bit in the UART EVENT ICLR register. 0h = No parity error has occurred 1h = The parity of the received data character does not match the parity defined by bits 2 and 7 of the UARTLCRH register.
8	FRMERR	R	0h	UART Framing Error. Writing to this bit has no effect. The flag is cleared by writing 1 to the FRMERR bit in the UART EVENT ICLR register. This error is associated with the character at the top of the FIFO. 0h = No framing error has occurred 1h = The received character does not have a valid stop bit sequence, which is one or two stop bits depending on the UARTLCRH.STP2 setting (a valid stop bit is 1).

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Table 32-61. RXDATA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DATA	R	0h	Received Data. When read, this field contains the data that was received by the UART. 0h = Smallest value FFh = Highest possible value

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27 LINCNT Register (Offset = 130h) [Reset = 00000000h]

LINCNT is shown in Figure 32-40 and described in Table 32-36.

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UART LIN Mode Counter Register. Only applies to Basic+ instances of UNICOMM.

Figure 32-40. LINCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VALUE															
R/W-0h																R/W-0h															

Table 32-63. LINCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	VALUE	R/W	0h	16-bit up counter clocked by UARTclk. 0h = Smallest value FFFFh = Highest possible value

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28 LINCTL Register (Offset = 134h) [Reset = 00000000h]

LINCTL is shown in Figure 32-41 and described in Table 32-37.

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UART LIN Mode Control Register. Only applies to Basic+ instances of UNICOMM.

Figure 32-41. LINCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
EN_FRM_ERR	LINC0_MATCH	LINC1CAP	LINC0CAP	RESERVED	CNTRXLOW	ZERONE	CTRENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 32-65. LINCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	EN_FRM_ERR	R/W	0h	Enable LIN Frame Error. 0h = Disable Frame Error Generation If STOP bit of '0' is received, then, FRAME ERROR is not generated 1h = Enable Frame Error Generation If STOP bit of '0' is received, then, FRAME ERROR is generated
6	LINC0_MATCH	R/W	0h	Counter Compare Match Mode. When this bit is set to 1 a counter compare match with LINC0 register triggers an LINC0 interrupt when enabled. 0h = Counter compare match mode disabled (capture mode enabled) 1h = Counter compare match enabled (capture mode disabled)
5	LINC1CAP	R/W	0h	Capture Counter on positive RXD Edge. When enabled the counter value is captured to LINC1 register on each positive RXD edge. A LINC1 interrupt is triggered when enabled. 0h = Capture counter on positive UARTxRXD edge disabled 1h = Capture counter on positive UARTxRXD edge enabled
4	LINC0CAP	R/W	0h	Capture Counter on negative RXD Edge. When enabled the counter value is captured to LINC0 register on each negative RXD edge. A LINC0 interrupt is triggered when enabled. 0h = Capture counter on negative UARTxRXD edge disabled 1h = Capture counter on negative UARTxRXD edge enabled
3	RESERVED	R/W	0h	
2	CNTRXLOW	R/W	0h	Count while low Signal on RXD. When counter is enabled and the signal on RXD is low, the counter increments. 0h = Count while low Signal on UARTxRXD disabled 1h = Count while low Signal on UARTxRXD enabled
1	ZERONE	R/W	0h	Zero on negative Edge of RXD. When enabled the counter is set to 0 and starts counting on a negative edge of RXD 0h = Zero on negative edge disabled 1h = Zero on negative edge enabled

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Table 32-65. LINCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CTRENA	R/W	0h	LIN Counter Enable. LIN counter will only count when enabled. 0h = Counter disabled 1h = Counter enabled

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29 LINC0 Register (Offset = 138h) [Reset = 00000000h]

LINC0 is shown in Figure 32-42 and described in Table 32-38.

Return to the Summary Table.

UART LIN Mode Capture 0 Register. Only applies to Basic+ instances of UNICOMM.

Figure 32-42. LINC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DATA															
R/W-0h																R/W-0h															

Table 32-67. LINC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	DATA	R/W	0h	16 Bit Capture / Compare Register. Captures current LINCNT value on RXD falling edge and can generate a LINC0 interrupt when capture is enabled (LINC0CAP = 1). If compare mode is enabled (LINC0_MATCH = 1), a counter match can generate a LINC0 interrupt. 0h = Smallest value FFFFh = Highest possible value

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30 LINC1 Register (Offset = 13Ch) [Reset = 00000000h]

LINC1 is shown in Figure 32-43 and described in Table 32-39.

Return to the Summary Table.

UART LIN Mode Capture 1 Register. Only applies to Basic+ instances of UNICOMM.

Figure 32-43. LINC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DATA															
R/W-0h																R/W-0h															

Table 32-69. LINC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15-0	DATA	R/W	0h	16 Bit Capture / Compare Register. Captures current LINCNT value on RXD rising edge and can generate a LINC1 interrupt when capture is enabled (LINC1CAP = 1) 0h = Smallest value FFFFh = Highest possible value

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31 AMASK Register (Offset = 148h) [Reset = 00000000h]

AMASK is shown in Figure 32-44 and described in Table 32-40.

Return to the Summary Table.

Self Address Mask Register. The address bits are masked to create a set of addresses to be matched with the received address byte for various UART operating modes.

Figure 32-44. AMASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VALUE							
R/W-0h																								R/W-0h							

Table 32-71. AMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	VALUE	R/W	0h	Self Address Mask. This field contains the address mask used to create a set of addresses that can be matched. A '0' bit in the MSK bitfield configures that the corresponding bit in the ADDR bitfield of the ADDR register is a don't care. A '1' bit in the MSK bitfield configures that the corresponding bit in the ADDR bitfield of the ADDR register must match. 0h = Smallest value FFh = Highest possible value

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32 ADDR Register (Offset = 14Ch) [Reset = 00000000h]

ADDR is shown in Figure 32-45 and described in Table 32-41.

Return to the Summary Table.

Self Address Register. The ADDR register is used to write the specific address that should be matched with the receiving byte when the Address Mask (AMASK) is set to FFh. This register is used in conjunction with AMASK to form a match for address-byte received. Used in UART 9-Bit or Idle-Line mode.

Figure 32-45. ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VALUE							
R/W-0h																								R/W-0h							

Table 32-73. ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-0	VALUE	R/W	0h	Self Address Register. This field contains the address that should be matched when AMASK is FFh. 0h = Smallest value FFh = Highest possible value

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Chapter 33

Inter-Integrated Circuit (I2C)

The functionality of a UNICOMM module when configured to operate as an I2C (either I2C Controller or I2C Target) is described in this section. The protocol mode of a given UNICOMM instance is decided by the programmed SELECT field of the IPMODE register. If a UNICOMM instance is configured for another peripheral mode, the I2CT/I2CC functionality on that UNICOMM instance is disabled and unusable.

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33.4 UNICOMM-I2C Registers 2490

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33.1 Overview

The UNICOMM-I2CC (Controller) and UNICOMM-I2CT (Target) modules provides a standardized serial interface to transfer data between AM13E230x devices and other external I^2C devices (such as a sensors, memory, DACs, other MCUs).

33.1.1 Purpose of the Peripheral

The UNICOMM-I2CC and UNICOMM-I2CT peripherals provides bidirectional data transfer through a two-wire serial bus consisting of a data (SDA) and clock (SCL) line. The I^2C bus is widely used to interface with devices such as battery management ICs, sensors, other MCUs and so on. This I^2C peripheral provides the ability to both transmit to and receive from other I^2C devices on the bus.

The **Basic UNICOMM-I2CC** module features include additional support for:

- Digital Glitch Supression

The **Advanced UNICOMM-I2CC** module features include additional support for:

- Analog Glitch Supression
- Burst Mode
- SMBus Support (PEC, Timeout Detection)

The **Basic UNICOMM-I2CT** module features include additional support for:

- Digital Glitch Supression

The **Advanced UNICOMM-I2CT** module features include additional support for:

- Analog glitch Supression
- SMBus Support (PEC, Timeout Detection, Enhanced Acknowledgement features, Default Device/Host/Alert Response Addresses, Target Arbitration)
- Secondary Target Address & Mask

33.1.2 Features

The UNICOMM-I2CC (Controller) and UNICOMM-I2CT (Target) peripheral modes of the UNICOMM module includes the following features:

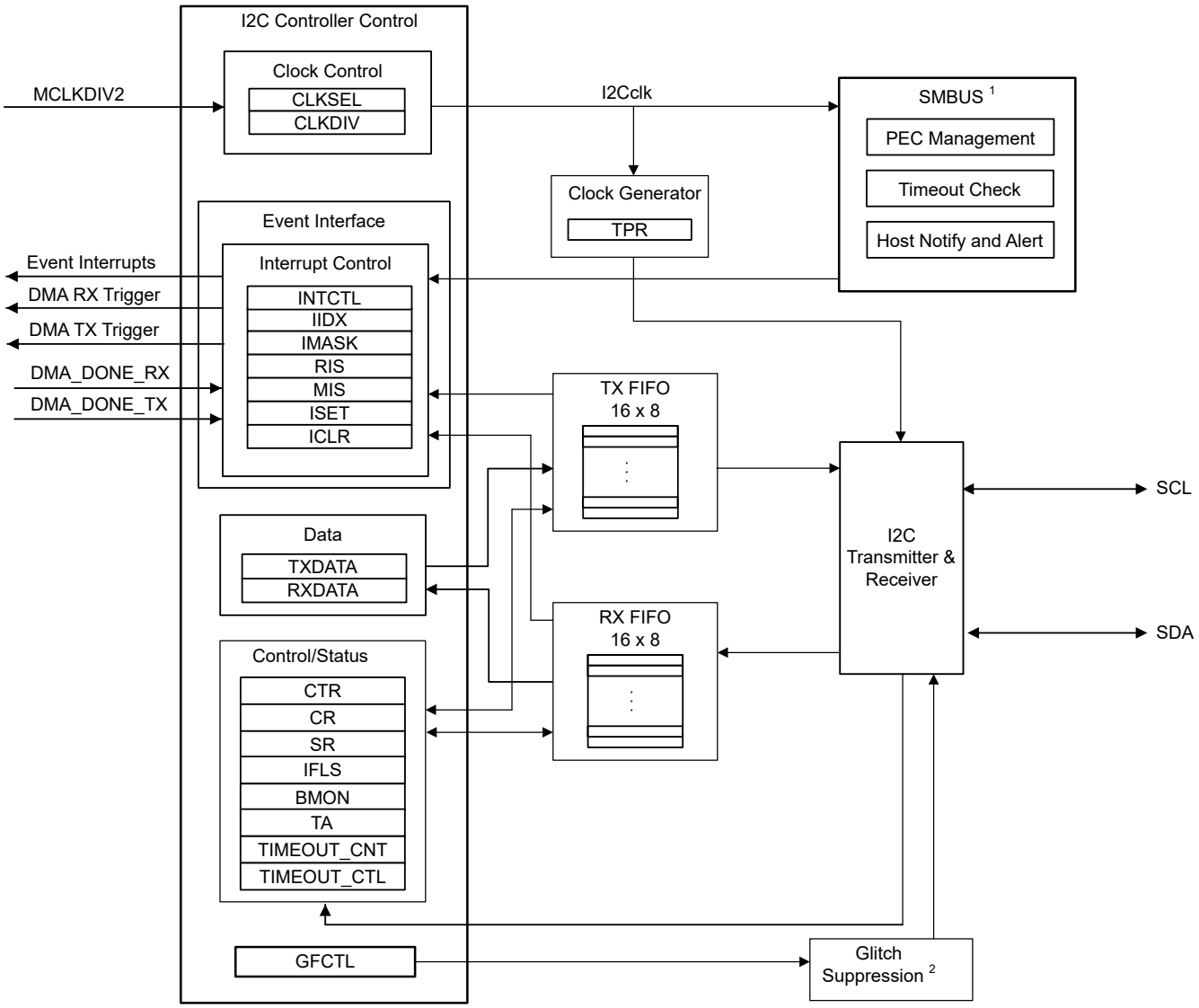
- 7-bit and 10-bit addressing
- Separate transmit (TX) and receive (RX) buffers/first-in first-out buffers (FIFOs)
- Supported transmission speeds:
  - Standard-mode (Sm) with a bit rate up to 100 kbps
  - Fast-mode (Fm) with a bit rate up to 400 kbps
  - Fast-mode Plus (Fm+) with a bit rate up to 1 Mbps
- Direct Memory Access (DMA) support
- Clock stretching (optional)
- Controller arbitration
- Multiple controller mode
- Glitch suppresion: analog (Advanced instances) and digital (Basic instances)
- Burst mode (Advanced instances)
- Dual addressing (Advanced instances)
- Available Interrupts:
  - Transmit (TX) and receive (RX) FIFO levels and empty/full conditions
  - START and STOP conditions
  - Transmit and receive done events
  - Target timeout events
  - Overrun, underrun, arbitration lost, PEC receive, and NACK error
  - DMA done conditions
- SMBus 3.0 hardware support (Advanced instances)
  - Enhanced ACK control

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- Quick command
- General call interrupt
- Clock low and high timeout
- Packet error checking (PEC)
- Host notify protocol
- Alert Response Protocol
- Address Resolution Protocol (ARP)

To support I2C protocol, a UNICOMM module must be configured as either UNICOMM-I2CC (Controller) or UNICOMM-I2CT (Target) in the UNICOMM top level IPMODE register.

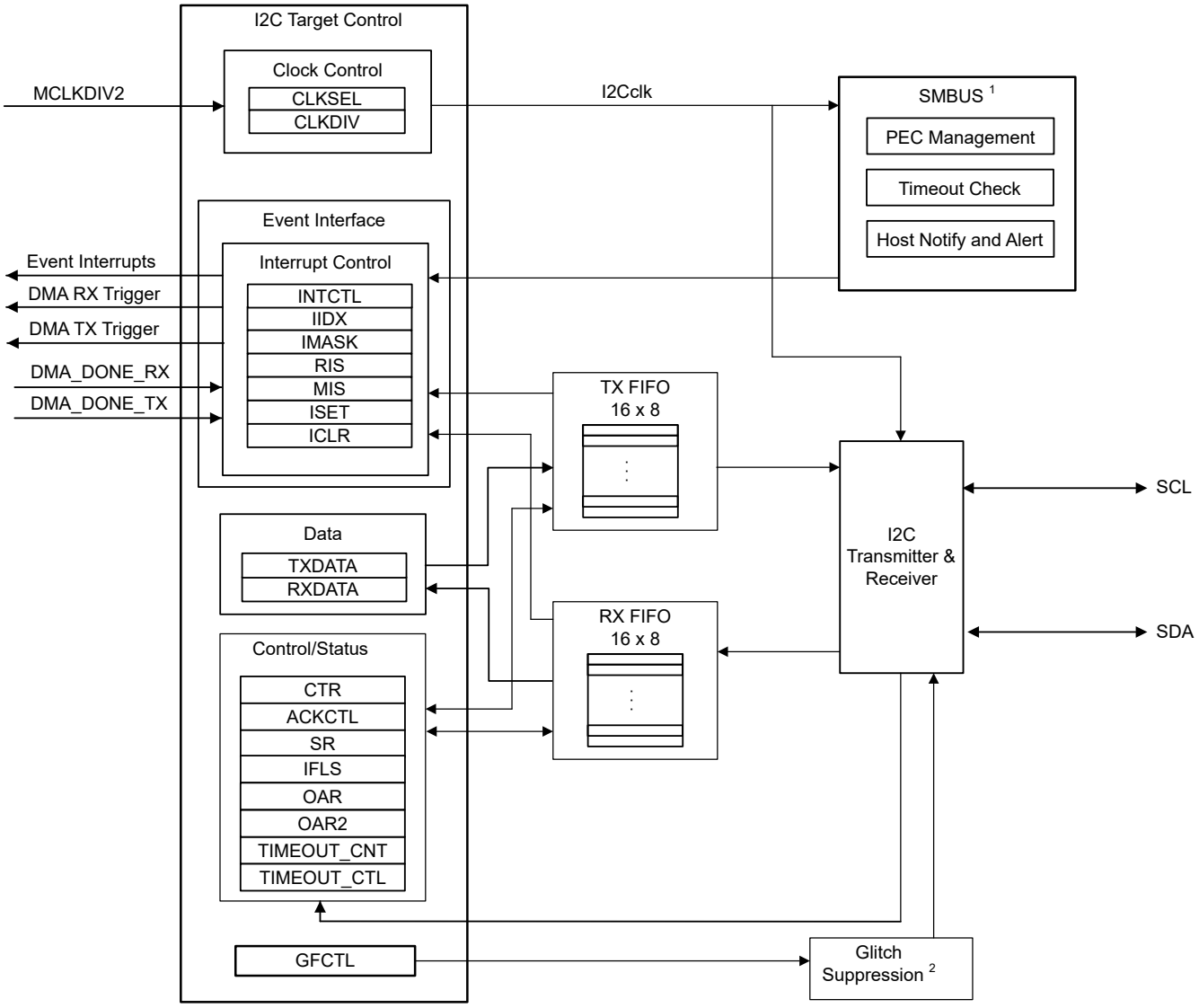
33.1.3 Functional Block Diagram



[1] Only Advanced I2CC instances have built-in SMBUS support
[2] Basic I2CC instances have only digital glitch support and Advanced I2CC instances have only analog glitch support

Figure 33-1. I2C Controller (I2CC) Functional Block Diagram

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[1] Only Advanced I2CT instances have built-in SMBUS support
[2] Basic I2CT instances have only digital glitch support and Advanced I2CT instances have only analog glitch support

Figure 33-2. I2C Target (I2CT) Functional Block Diagram

33.2 Peripheral Functional Description

33.2.1 Clock Control

33.2.1.1 Clock Select and I²C Speed

Standard, Fast, and Fast Plus modes are selected using a value in the I²C Controller Timer Period (TPR) register that results in a maximum SCL frequency of:

- 100 kbps for Standard mode
- 400 kbps for Fast mode
- 1 Mbps for Fast mode Plus

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The I²C frequency I2C_FREQ is determined by the I2Cclk functional clock frequency and the TPR field, as well as the fixed SCL_LP , and SCL_HP values where:

- I2Cclk is the functional clock frequency to the I²C module. Note that the I²C internal functional clock is first divided from the source clock:
  - Use the CLKSEL register to enable MCLKDIV2 as the functional clock source for the UNICOMM I²C module.
  - Use the CLKDIV.RATIO register field to select divide ratio of I²C functional clock, options are from divide by 1 to 8.
- SCL_LP is the low phase of SCL: This is fixed at a value of 6
- SCL_HP is the high phase of SCL: This is fixed at a value of 4
- TPR is the programmed value of the TPR field of the TPR register. This value is determined by replacing the known variables in the equation below and solving for TPR.

The I²C freqency is calculated as follows:

$$I2C_FREQ = I2Cclk/(((1 + TPR) * (SCL_LP + SCL_HP)) + (2/I2Cclk)) \quad (48)$$

For example, if the I²C functional clock (I2Cclk) frequency is 32 MHz and target SCL frequency is 400 kHz:

I2Cclk = 32 MHz

I2C_FREQ = 400 kHz

SCL_LP = 6 , SCL_HP = 4

TPR = ((1 / (4+6))*((I2Cclk / I2C_FREQ) - (2 / I2Cclk)) - 1)

TPR = 6.999 ≈ 7 (0x07)

Note

The I2CC can only achieve frequencies (I2C_FREQ) resulting from integers values written to the TPR register and the set I2Cclk frequency. When the solved equation results in a TPR value that is not a whole number (like the above example), there will be error associated with the generated SCL clock frequency when compared to the expected I2C_FREQ.

Table 33-1. Examples of Controller Clock Setting for Typical Clock Configurations

I2Cclk	TPR Bits Standard Mode 100-kHz SCL	TPR Bits Fast Mode 400-kHz SCL	TPR Bits Fast Mode Plus 1000-kHz SCL
4 MHz	0x03	0x01	-
8 MHz	0x07	0x03	-
20 MHz	0x13	0x06	0x01
32 MHz	0x1F	0x07	0x02
40 MHz	0x27	0x09	0x03

The I²C functional clock must be greater than or equal to 20 times the SCL frequency, I2Cclk ≥ 20 × I2C_FREQ.

The following minimum functional clock frequencies are required when running certain I2C_FREQ speeds:

- I2Cclk ≥ 2 MHz when working with I²C speed 0 to 100 kHz
- I2Cclk ≥ 8 MHz when working with I²C speed 100 to 400 kHz
- I2Cclk ≥ 20 MHz when working with I²C speed 400 kHz to 1 MHz

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33.2.1.2 Clock Startup

The module clock source is always available once setup in the CLKSEL register. After enabling the I²C module by setting the PWREN.ENABLE bit from the UNICOMM top level, the module is ready to start receiving and transmitting data.

33.2.2 Signal Descriptions

The I²C bus consists of a clock signal and a data signal. The clock signal can be generated either internally (during controller operation) or externally (during target operation).

Table 33-2. I²C signal descriptions

Device Pin	Function
I2Cx_SCL	I²C clock signal
I2Cx_SDA	I²C data signal

33.2.3 General Architecture

33.2.3.1 I²C Bus Functional Overview

The I²C bus uses only two signals: SDA and SCL. SDA is the bidirectional serial data line and SCL is the bidirectional serial clock line. The bus is considered idle when both lines are in high state and no transfer is ongoing.

Every transaction on the I²C bus is 9-bits long, consisting of 8 data bits and 1 acknowledge bit. A transaction is defined as the time between a valid START and STOP condition—as described in Figure 33-3. The number of bytes per transaction is unrestricted; however, each data byte must be followed by an acknowledge bit and data must be transferred MSB first. When a receiving device cannot receive another complete byte, it can hold the clock line SCL Low and force the transmitting device into a wait state.This process is commonly known as clock stretching. The data transaction continues when the receiver releases the clock SCL.

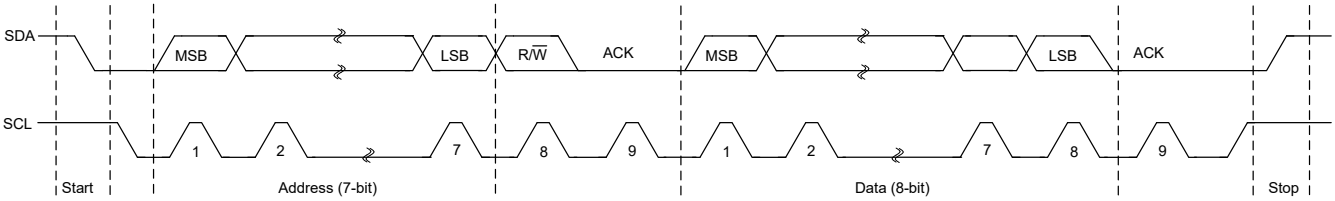


Figure 33-3. Module Data Transfer

The data on the SDA line must be stable during the high period of the clock, and the data line can only change when SCL is low (see Figure 33-4), otherwise START or STOP conditions are generated.

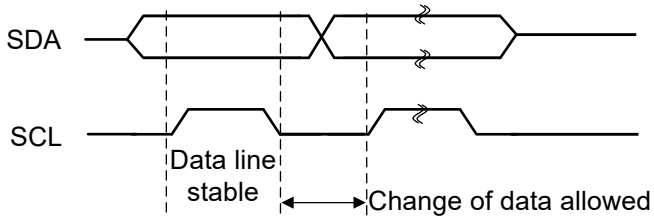


Figure 33-4. Data Change Period

33.2.3.2 START and STOP Conditions

The protocol of the I²C bus defines two states to begin and end a transaction: START and STOP. A high-to-low transition on the SDA line while the SCL is high is defined as a START condition, and a low-to-high transition on the SDA line while SCL is high is defined as a STOP condition. START and STOP conditions are always

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generated by the controller. The bus is considered busy after a START condition and free after a STOP condition.

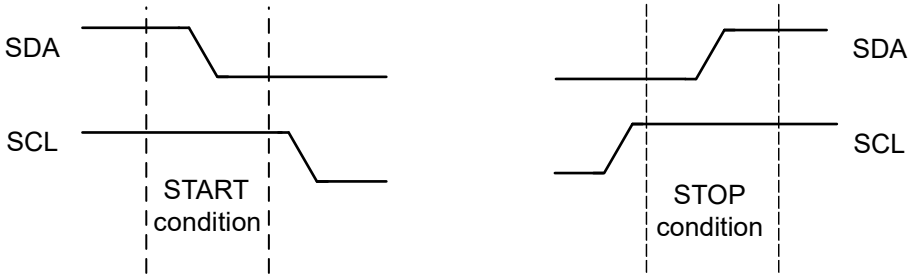


Figure 33-5. START and STOP Conditions

The STOP bit determines if the transaction stops at the end of the data cycle or continues on to a repeated START condition.

To generate a single transaction, the I^2C controller target address TA.ADDR register is written with the desired address, the TA.DIR bit should be set to 1 to start a receive operation and 0 to start a transmit operation , and the control register (CTR) is written with ACK = X (0 or 1), STOP = 1, START = 1, and FRM_START = 1 to perform the operation and generate a STOP at the end. When the operation is completed (or aborted due an error) the interrupt flags are set. When the I^2C module operates in Controller receiver mode, the ACK bit is normally (in case of no error) set causing the I^2C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I^2C bus controller requires no further data to be transmitted from the target transmitter. For more information on I^2C controller mode configuration please refer to Section 33.2.4.1 .

When operating in target mode, the START and STOP bits in the CPU_INT.RIS register indicate detection of start and stop conditions on the bus and the CPU_INT.IMASK can be configured to allow START and STOP to be promoted to controller interrupts (when interrupts are enabled). For more information on I^2C target mode configuration please refer to Section 33.2.4.2 .

Bus Status Flags:

- BUSBSY is set when a START condition is detected on the bus and cleared when a STOP condition is detected on the bus.
- BUSY is also set after a START/Repeated START, and cleared after CTR.BLEN bytes of data is transferred. It is also cleared after data is NACK ‘d or a STOP.
- IDLE is set when the Controller I^2C state machine is in the IDLE state indicating there is no ongoing transfer.

33.2.3.3 7-Bit Address Format

Standard 7-bit addressing I^2C data transfers follow the format shown in Figure 33-6. To transmit/receive using a 7-bit addressing mode, set TA.MODE=0 for UNICOMM-I2CC devices and OAR.MODE=0 for UNICOMM-I2CT devices.

The I^2C controller initiates the START condition, then a target address is transmitted. This address is 7-bits long, followed by an eighth bit, which is a data direction bit, set by TA.DIR for UNICOMM-I2CC modules. A TA.DIR bit set to '0' indicates a transmit operation (send) a TA.DIR bit set to '1' indicates a request to receive data (receive). A data transfer is always terminated by a STOP condition generated by the controller. However, a controller can initiate communications with another device on the bus by generating a Repeated START condition and addressing another target without first generating a STOP condition, see section Figure 33-8. Various combinations of receive/transmit formats are then possible within a single transfer. The ninth bit is the Acknowledge bit, which is described in Section 33.2.3.7 .

The target address sent in the I^2C frame matches the unique target address of a target device on the bus. For UNICOMM-I2CT devices, this unique address is programmed in the OAR.OAR register field, where the top 3 bits are "don't care" in for 7-bit addressing mode. If the UNICOMM-I2CT device receives an address byte on the bus

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matching the address programmed in OAR.OAR with a read bit, it shifts the data bytes that follow into the RX FIFO. If the UNICOMM-I2CT device receives an address byte on the bus matching the address programmed in OAR.OAR with a write bit, it shifts out the data bytes in the TX FIFO and onto the SDA line.

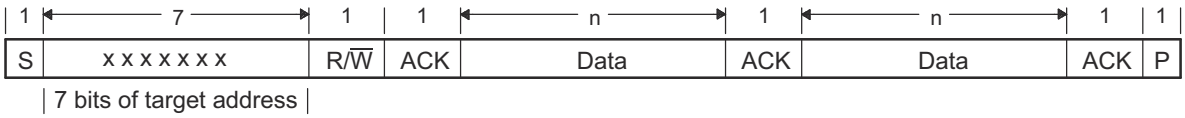


Figure 33-6. Data Format with 7-Bit Address

33.2.3.4 10-Bit Address Format

To transmit/receive using a 10-bit addressing mode, set TA.MODE=1 for UNICOMM-I2CC devices and OAR.MODE=1 for UNICOMM-I2CT devices.

Standard 10-bit addressing I^2C data transfers follow the format shown in Data Format with 10-Bit Address. The 10-bit addressing format is similar to the 7-bit addressing format, except the controller sends the target address in two separate byte transfers. After the START condition, the first byte consists of 11110b, the two MSBs of the 10-bit target address, and the R/W bit. The second byte contains the remaining 8 bits of the 10-bit target address. A data transfer is always terminated by a STOP condition or repeated START condition generated by the controller.

The target side matching is also similar to 7-bit addressing mode, except that the UNICOMM-I2CT address matches the full 10-bits of the programmed OAR.OAR field.

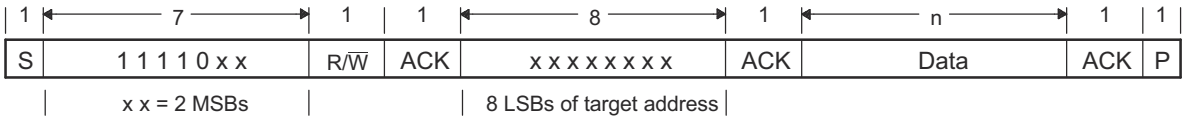


Figure 33-7. Data Format with 10-Bit Address

33.2.3.5 General Call

The general call feature is available UNICOMM-I2CT's and is enabled by setting the CTR.GENCALL bit. The General Call is identified by an address of 0x00 and R/W bit set to '0'. With this feature, the I2CT module responds to a General Call on the I^2C bus, as well as any frames with addresses matching the programmed OAR (and OAR2 if applicable and enabled) addresses. The General Call interrupt is flagged upon receiving a general call frame from the I2C controller. This interrupt can be enabled by setting the CPU_INT.IMASK.GENCALL bit.

33.2.3.6 Dual Address

The dual addresses feature is only available for Advanced UNICOMM-I2CT instances.

An additional programmable UNICOMM-I2CT Own Address Register called OAR2 is provided and can be used for matching in a 7-bit addressing format, if enabled. When the secondary address is disabled (OAR2.OAR2EN=0), the I2CT provides an ACK on the bus if the address matches the OAR field in the OAR register.

In dual address mode (OAR2.OAR2EN=1), the UNICOMM-I2CT provides an ACK on the bus if either the OAR field in the OAR register or the OAR2 field in the OAR2 register is matched. The OAR2SEL bit in the SR register indicates whether the address that was ACK'ed is the alternate address or the primary address. A cleared OAR2SEL bit indicates that either the primary address matched, or there was no OAR2 address match.

33.2.3.7 Acknowledge

All bus transactions have a required acknowledge clock cycle that is generated by the controller. During the acknowledge cycle, the transmitter (which can be the controller or target) releases the SDA line. To acknowledge the transaction, the receiver must pull down SDA during the acknowledge clock cycle. The acknowledge cycle must comply with the data validity requirements.

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When a target receiver does not acknowledge the target address, SDA must be left high by the target so that the controller can generate a STOP condition and abort the current transfer or generate a repeated START condition to start a new transfer. If the controller device is acting as a receiver during a transaction, it is responsible for acknowledging each transfer made by the target. Because the controller decides the number of bytes in the transaction, it signals the end of data to the target transmitter by not generating an acknowledge on the last data byte. The target transmitter must then release SDA to allow the controller to generate the STOP or a repeated START condition.

A target can generate an ACK/NACK manually or automatically.

- When ACKCTL.ACKOEN=0, the target will send automatic acknowledgements. The I2CT will receive and ACK all bytes automatically until the RX FIFO is full.
- When ACKCTL.ACKOEN =1, manual acknowledgments are enabled. Manual ACK override can be used to evaluate each received byte or to slow down the communication when automatic FIFO reception is not desired. When manual ACK override operation is enabled, the I^2C target module's clock is pulled low after the last data bit until this ACKCTL.ACKOVAL is written with the indicated response. The reception of new data is indicated by the RXDONE interrupt flag.

If the I^2C controller receives a NACK while transmitting data, the NACK and TXDONE bit will be set in the RIS registers. If there is still data in the TX FIFO, the TXEMPTY bit will remain clear to inform software that a TX FIFO flush may be required.

33.2.3.8 Repeated Start

The direction of data flow on SDA can be changed by the controller, without first stopping a transfer, by issuing a repeated START condition. This is called a RESTART, see data format in Figure 33-8. After a RESTART is issued, the target address is again sent out with the new data direction specified by the R/W bit.

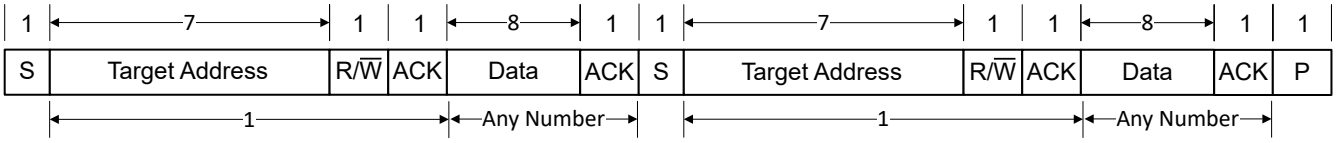


Figure 33-8. Data Format with Repeated Start

A repeated start sequence for a controller transmit or receive is as follows:

1. When the device is in the idle state, the Controller writes the target address to the TA register and configures the DIR bit for the desired transfer type.
2. Data is written to the TXDATA register (for transmit) or RXDATA register (for receive).
3. When SR.BUSY status reads back as '0', FRM_START and START bits in the CTR register are set to initiate a transfer.
4. Software waits till BUSY bit in the SR register reads back as '0'.
5. The controller can now change direction of transfer or address another target, by generating a restart condition. Software updates TA register and then, sets FRM_START. This initiates a repeated start on the line.

   Note: if there is a NACK for address, a STOP condition will be automatically generated. RESTART cannot be sent in that case.

33.2.3.9 Clock Low Timeout

Timeout Counter A

An UNICOMM-I2CT can extend the transaction by pulling the SCL line low to slow down communication. Both the UNICOMM-I2CC and UNICOMM-I2CT modules have a counter called TCNTA, which is a 12-bit programmable counter that tracks how long the clock has been held **low**. The upper 8-bits of the count value are software programmable through the TIMEOUT_CTL register. The value programmed in the TIMEOUT_CTL.TCNTLA register field must be greater than 0x01 to enable the timeout A feature.

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The application can program the eight most significant bits of the counter to reflect the acceptable cumulative low period in a transaction. Each count is equal to a timeout period of ((1 + TPR) × 12) I2Cclk's where the TPR is the programmable timer period. TIMEOUT_CNT.TCNTA counts continuously for the entire time SCL is held in a low state. When SCL goes back high, TIMEOUT_CNT.TCNTA is reloaded with the value in the TIMEOUT_CTL.TCNTLA register, and begins counting down from this value at the falling edge of SCL.

The internal I2Cclk keeps running even if SCL is held low on the bus.

The I^2C clock low timeout period is calculated as follows:

- Cumulative SCL low period = Timeout counter * One timeout period
- One timeout period = (I2Cclk period) * (1 + TPR) * (12)
- Timeout counter = TIMEOUT_CTL.TCNTLA register (this register contains the upper 8-bits of a 12-bit counter value, the lower 4-bits are set to 0)

As an example, if the I2Cclk is configured to 20 MHz and the I^2C module is operating at a 100-kHz speed, the TPR would be equal to 19. See Section 33.2.1.1 on how TPR is calculated. One timeout period is equal to (1 / 20 MHz) × (1 + 19) × 12 or 12 µs. Programming the TIMEOUT_CTL.TCNTLA register to 0xDA would translate to the value 0xDA0, because the lower 4-bits are set to 0x0. This translates to a decimal value of 3488 clocks or a cumulative clock low period of 3488 × 12 µs, or 41.856 ms at 100 kHz.

The TIMEOUTA bit in the UNICOMM-I2CC RIS register is set when the clock timeout period is reached, allowing the controller to start corrective action to resolve the remote target state. This bit is cleared after I^2C goes to idle or during the I^2C controller reset. The status of the raw SDA and SCL signals are readable by software through the SDA and SCL bits in the BMON register to help determine the state of the remote target. In the event of a timeout condition, application software must choose how it intends to attempt bus recovery. If a timeout is detected before the end of a transfer (receive or transmit), software needs to flush the FIFOs before initiating the next transfer. This timeout feature is needed for SMBus and PMBus implementation.

A UNICOMM-I2CT module can also trigger an interrupt on a configured clock timeout low condition using the same registers and fields.

Timeout Counter B

Timeout Counter B is only available for Advanced UNICOMM-I2CC and UNICOMM-I2CT instances.

Both the UNICOMM-I2CC and UNICOMM-I2CT modules have a secondary counter called TCNTB, which is a 12-bit programmable counter that tracks how long the clock has been held **high**. This counter is configured similarly to the TCNTA, where the upper 8-bits of the count value are software programmable through the TIMEOUT_CTL.TCNTLB register. The value programmed in the TIMEOUT_CTL.TCNTLB register field must be greater than 0x01 to enable the timeout B feature. There is an interrupt flag available for the TCNTB counter for UNICOMM I2CC and UNICOMM-I2CT in the event that the clock timeout period is reached, the TIMEOUTB bit in the RIS register is set.

Note

All timeout configurations must only be modified while the UNICOMM-I2C module is disabled - CR.ENABLE=0 for I2CC and CTR.ENABLE=0 for I2CT.

33.2.3.10 Clock Stretching

For a UNICOMM-I2CC, clock stretching can be disabled if none of the targets on the bus support clock stretching, allowing the controller to reach the maximum speed on the bus. Otherwise, the clock can be slowed by a target keeping the clock low or due to the clock status detection delay within the I^2C module.

For a UNICOMM-I2CT, clock stretching is activated automatically when either the RX FIFO full or TX FIFO empty is set. Clock stretching support can be enabled or disabled by configuring the CTR.CLKSTRETCH bit, where the feature is enabled by default. Clock stretching status is indicated by the TREQ and RREQ bits from the SR register described below.

- TREQ

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  - When this bit is set, the I^2C target has been addressed as a target transmitter and is using clock stretching to delay the controller until data has been written to TXDATA.
- RREQ
  - When this bit is set, the I^2C controller has outstanding receive data from the I2C controller and is using clock stretching to delay the controller until the data has been read from RXDATA.

33.2.3.11 Arbitration

A controller can start a transfer only if the bus is idle. It's possible for two or more controllers to generate a START condition within minimum hold time of the START condition. In these situations, an arbitration scheme takes place on the SDA line, while SCL is high (see Figure 33-9) . The first controller transmitter that generates a logic high is overruled by the opposing controller generating a logic low and the losing controller releases the bus until the bus is idle again.

Arbitration can take place over several bits. Its first stage is a comparison of address bits, and if both controllers are trying to address the same device, arbitration continues on to the comparison of data bits.

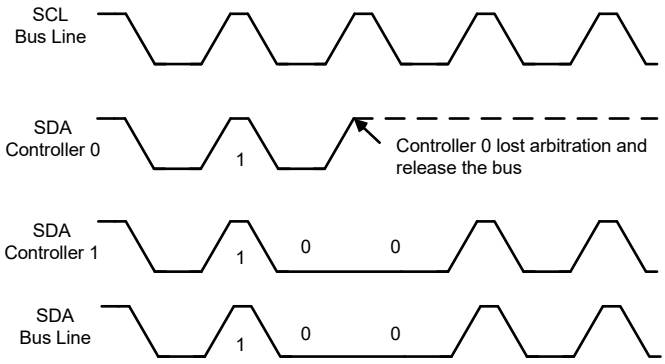


Figure 33-9. Arbitration Procedure Between Two Controller Transmitters

When an arbitration lost error occurs, the SR.ARBLST flag is set. It will be reset by the hardware with the next STOP condition is detected on the bus. Additionally the ARBLOST flags in RIS registers are set.

If arbitration is lost when the I2CC has initiated a transfer, the application should execute the following steps to correctly handle the arbitration loss:

- Clear the TX FIFO
- Once the bus is IDLE, the TXFIFO can be filled and enabled, the TXEMPTY bit can be unmasked and a new transaction can be initiated.

33.2.3.12 Multiple Controller Mode

To enable multiple I2C controllers on the bus, the CR.CTL bit must be set to enable multi-controller mode. During the arbitration procedure, the clocks from all the different controllers must be synchronized. A device that first generates a low period on SCL overrules the other devices, forcing them to start their own low periods. SCL is then held low by the device with the longest low period. The other devices must wait for SCL to be released before starting their high periods.

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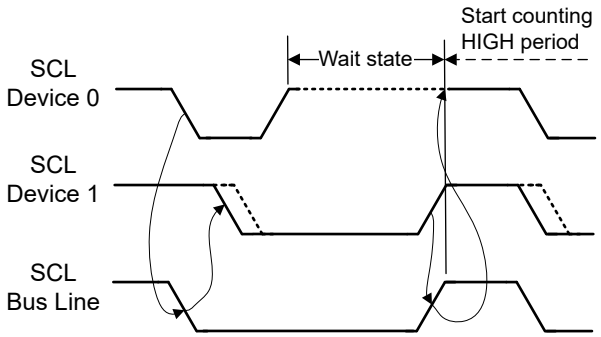


Figure 33-10. Clock Synchronization

33.2.3.13 Glitch Suppression

The UNICOMM I2CC and I2CT modules supports glitch suppression on the SCL and SDA lines up to 50ns, as specified in the I^2C specification.

Analog Glitch Filter

The analog glitch filter feature is only available for Advanced UNICOMM-I2CC and UNICOMM-I2CT instances.

In Advanced UNICOMM-I2C instances, by default, an analog glitch filter is enabled and configured to suppress spikes with a pulse width up to 50ns, configurable via the GFCTL.AGFEN field. The I^2C specification advises to suppress noise spikes of less than 50ns. This filter is disabled by clearing the GFCTL.AGFEN bit.

Digital Glitch Filter

The digital glitch filter feature is only available for Basic UNICOMM-I2CC and UNICOMM-I2CT instances.

In Basic UNICOMM-I2C instances, a digital glitch filter is available. The DGFSEL bits in the GFCTL register can be programmed to provide glitch suppression on the SCL and SDA lines and provide proper signal values. The glitch suppression value is in terms of I2Cclk cycles. To disable the digital glitch filter, set the DGFSEL field to zero. All signals are delayed internally when glitch suppression is nonzero. For example, if the DGFSEL field is set to 0x7, 31 clocks are added onto the calculation for the expected transaction time.

Table 33-3. Glitch Suppression Filter Types

	Analog Glitch Filter	Digital Glitch Filter
Default	Default enabled with 50ns	Default bypassed
UNICOMM Instances	UC2, UC5	UC0, UC1, UC3, UC4
Pulse width of suppressed spikes	Configurable periods: 5ns, 10ns, 25ns, 50ns	Configurable I2Cclk cycles: 1, 2, 3, 4, 8, 16, 31
Benefits	Filter does not depend on the I2Cclk	Programmable length provides extra filtering options and a stable filtering length
Limitation	Variation with temperature and voltage	Only enabled 3 clock cycles after the start of I^2C packet.

Note

Modifications to the GFCTL register must only be done while the CR.ENABLE bit is cleared.

33.2.3.14 Burst Mode

Burst mode is only available for Advanced UNICOMM-I2CC instances.

The UNICOMM-I2CC burst mode allows a sequence of data transfers using DMA or software to transmit or receive the data in the FIFOs. Burst mode is enabled by setting the CTR.BLEN bits in the I2CC CTR register to a value 'N', where 'N' must be greater then '1'. This field sets the number of bytes transferred by a burst. A copy of this value is automatically written to the SR.BCNT bits in the I2CC status register to be used as a down-counter

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during burst transfer. The RXDONE and TXDONE interrupt flags are set after a burst of 'N' data bytes has been sent.

In the event that one of the data bytes is NACK'd during an I2CC burst sequence:

- If the CTR.STOP bit *is* set, the frame transfer is terminated. Upon receiving a not acknowledge condition, the I2CC NACK interrupt bit is set in the RIS register and the I2CC automatically sends out a STOP condition on the bus and terminates transfer.
- If the CTR.STOP bit *is not* set, hardware waits for software to proceed further. Upon receiving a not acknowledge condition, the I2CC NACK interrupt bit is set in the RIS register. Software can read the SR.BCNT field to determine the amount of data that was transferred prior to the termination of the burst if desired. Then, software can send out a STOP condition by setting CTR.STOP or a RESTART condition by setting CTR.FRM_START.

33.2.3.15 DMA Operation

The UNICOMM I^2C modules, I2CC and I2CT, each provide an interface to the DMA module with seperate channels for transmit and receive. The DMA operation of the I^2C is enabled through the I^2C DMA Event and DMA module registers. When the DMA functionality is enabled, the I^2C asserts a DMA request on the selected channel when the associated FIFO can transfer or receive data. The DMA transfer requests are handled automatically by the DMA controller based on how the DMA channel is configured (burst size, transfer size, source address etc.).

For more information about the DMA module and DMA-specific configurations, see Direct Memory Access (DMA).

- For the receive channel, a DMA transfer request is asserted when the amount of data in the receive FIFO is at or above the FIFO trigger level configured using the RXIFLSEL bit in IFLS register.
- For the transmit channel, a DMA transfer request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level configured using the TXIFLSEL bit in IFLS register.

33.2.3.16 SMBus 3.0 Support

The System Management Bus (SMBus) protocol is a standard two-wire interface used for industrial applications like battery management, memory SSD and several other use cases. See the *System Management Bus (SMBus) Specification* for more information about the SMBus protocol standards. Since the SMBus protocol reuses a number of features from the standard I^2C protocol, UNICOMM-I2CC peripherals can be used to support the SMBus protocol as well. The additional registers and features supporting the SMBus protocol are only present on UNICOMM instances with Advanced I2CC and I2CT capabilities.

33.2.3.16.1 Quick Command

Quick Command is a simple, compact SMBus transaction that sends an address and 1-bit of data in the DIR bit of the I2C header byte to communicate a command to the target, typically a "turn off" or "turn on". The controller has the ability to send a Quick Command by writing the target address and direction value into the TA register, followed by setting the START, STOP, and FRM_START bits in the CTR register and clearing the BLEN field to 0. The target logic also has quick command support built in.

In UNICOMM-I2C Target mode, the TX FIFO must be empty upon receiving a Quick Command and can only be loaded after decoding the received message. Follow the steps below to receive a Quick Command from an I2CT:

1. TX FIFO must be empty
2. Receive and decode a Quick Command message using the SR.QCMDST and SR.QCMDRW bits.
3. If clock stretching is enabled, software must load the TX FIFO with 0xFF to stop clock stretching and allow the I2C Controller to generate a STOP condition.

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Figure 33-11. Quick Command Message

33.2.3.16.2 Acknowledge Control

I2C Target Enhanced ACK Control

The below additonal bits in the ACKCTL register provide enhanced acknowledgement functionality. The status bit SR.ACKOEN is updated automatically when the ACKOEN_ON_PECDONE, ACKOEN_ON_PECNEXT, or ACKOEN_ON_START bits in ACKCTL are set. Software has to write ACKCTL.ACKOEN to '0' to clear the acknowledge override condition generated by hardware.

- **ACKOEN_ON_PECDONE**
  - When set, this bit automatically turns on the target override mechanism following the ACK/NACK of the received PEC byte. This allows software to manually handle data bytes received after the PEC byte. The sequence is as follows:
    1. Set ACKCTL.ACKOEN_ON_PECDONE
    2. SR.ACKOEN bit is automatically set after the PEC byte has been ACK/NACK'd
    3. Receive "n" bytes using manual software ACK
    4. Clear SR.ACKOEN after "n" bytes have been received
    5. Receive next "m" bytes using the automatic hardware ACK
- **ACKOEN_ON_PECNEXT**
  - When set, this bit automatically turns on the target override mechanism following the ACK/NACK of the byte received prior to the PEC byte. Software must clear the SR.ACKOEN after ACKing/NACKing the PEC byte. Using this option, software can effectively get the synchronization point by getting an interrupt here (TREQ/RREQ condition with TXEMPTY_ONTREQ/RXFLL_ON_RREQ set), and then manually send the ACK/NACK of the PEC. In other words, the software doesn't need to rely on byte granularity RXMODE and TXMODE interrupts and get an interrupt after the entire frame has been TX/RX. The sequence is as follows:
    1. Set ACKCTL.ACKOEN_ON_PECNEXT
    2. SR.ACKOEN bit is automatically set before the PEC bytes
    3. Receive the PEC byte and manually ACK/NACK using software
    4. Clear SR.ACKOEN
    5. Receive the entire next frame using automatic hardware ACK until the next PEC byte is received
- **ACKOEN_ON_START**
  - When set, this bit automatically turns on the target override mechanism following a START condition. The sequence is as follows:
    1. Set ACKCTL.ACKOEN_ON_START
    2. SR.ACKOEN bit is automatically set when the START condition is detected
    3. Continue receiving bytes with software until remaining bytes are known
    4. Clear SR.ACKOEN
    5. Receive the rest of the frame using automatic hardware ACK until the next START condition is received

Note

The I2CT software must wait a bit duration between generating a NACK and disabling the SR.ACKOEN. These operations cannot happen in the same cycle.

I2C Controller Enhanced ACK Control

The I2CC, when in receive mode, can ACK/NACK after "n" number of bytes are received. When CTR.ACKOEN is set and the number of bytes configured by CTR.BLEN are received, an RXDONE interrupt is generated and

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the transaction is either ACK'd or NACK'd depending on the value of CTR.ACK. To stop the transaction, the CTR.STOP can be set. Otherwise, software can update the CTR.BLEN field to a new value to continue with the transaction.

33.2.3.16.3 Clock Low Timeout Detection

Clock **low** timeout detection is done by setting the TIMEOUT_CTL.TCNTAEN and configuring the timeout period in the TIMEOUT_CNT.TCNTLA (the upper 8-bits of a 12-bit period) register field. The TIMEOUT_CNT.TCNTA register contains the current count value.

Example counter calculations for low SCL timeout detection is shown below.

- For SCL low detect, each count is equal to 520 cycles of the I2Cclk period.
- A pre-multiplier of 520 is used to make the total timeout period greater than 35ms (tTIMEOUT,MAX specified by SMBus 3.0), even at the highest clock frequency of 40MHz.
- At 40MHz, 1 count = 520 * 25ns = 13us
- Max count value = 12'b1111_1111_0000 = 12'd4080
- Total time configurable = 4080 * 13us = 53.04ms

33.2.3.16.4 Clock High Timeout Detection

Clock **high** timeout detection is done by setting the TIMEOUT_CTL.TCNTBEN and configuring the timeout period in the TIMEOUT_CNT.TCNTLB (the upper 8-bits of a 12-bit period) register field. The TIMEOUT_CNT.TCNTB register contains the current count value.

Example counter calculations for high SCL timeout detection is shown below.

- For SCL high detection, each count is equal to 1 * I2Cclk period.
- A pre-multiplier of 1 is used to make the accuracy of the counter remain high for 50 µs ($t_{HIGH,MAX}$) even for low frequency I2Cclk's.
- At 10MHz, 1 count = 100ns
- Total I2Cclk counts required to count 50 µs = 500
- Value of TIMEOUT_CNT.CNTLB for 50µs bus idle timeout = 500/16 = 32

33.2.3.16.5 Cumulative clock low extended timeout for controller and target

The below two cumulative timeout event specifications come from SMBus 3.0 for targets and controllers.

- $t_{LOW:SEXT}$
  - This value is defined as the cummulative time a given target device is allowed to extend the clock cycles in one message from the initial START to the STOP. Another target device, or the controller, can also extend the clock causing the combined clock low extend time to be greater than $t_{LOW:SEXT}$. Therefore, this parameter is measured with the target device as the sole target of a full-speed controller.
- $t_{LOW:MEXT}$
  - This value is defined as the cumulative time a controller device is allowed to extend the clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. A target device or another controller can also extend the clock causing the combined clock low time to be greater than $t_{LOW:MEXT}$ on a given byte. Therefore, this parameter is measured with a full speed target device as the sole target of the controller.

Cumulative timeout events need to be monitored in software for I2CC and I2CT. In most cases, a single clock stretch SCL timeout can act as a sufficient safeguard against cumulative events.

In controller mode, the UNICOMM-I2CC only clock stretches on byte boundaries. This aligns with the definition of $t_{LOW:MEXT}$ and the Counter A low timeout method outlined in Section 33.2.3.16.3 can be used.

In target mode, since clock stretch events can happen at different byte boundaries within a transaction for UNICOMM-I2CT, software must use DMA and FIFO capabilities to avoid exceeding $t_{LOW:SEXT}$. Typically, software takes a longer time to process the first command byte of an SMBUS frame, so the Counter A method can safeguard against software latencies. The rest of the transaction contains byte transfers that must not have software delays.

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33.2.3.16.6 Packet Error Checking (PEC)

PEC is a CRC-8 error checking byte which is calculated using all the message bytes of a transaction, including addresses and read/write bits. The ACK/NACK, START, and STOP bits do not contribute to the PEC calculation. The PEC is appended to the message by the device that supplied the last data byte.

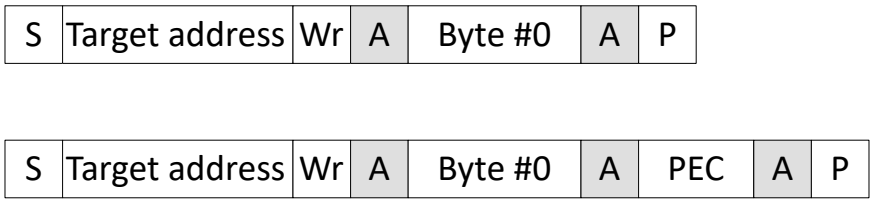


Figure 33-12. Send Byte Message with and without PEC

The PEC Polynomial calculation is the below.

$$x^8 + x^2 + x^1 + 1$$

The PECCTL register on Advanced UNICOMM-I2CC and UNICOMM-I2CT instancessupports PEC transmission and checking for both controller and target modes. Each of the fields from the PECCTL register are described below.

- PECEN
  - This bit enables the SMB Packet Error Checking (PEC) mechanism. When enabled, the PEC is calculated on all bits except the START, STOP, and ACK/NACK.
- PECCNT
  - When this field is set to a non-zero value, the number of I2C data bytes are counted and compared against this value to keep track of each PEC byte in a transmission/reception.

Note

For a I2C Target, dynamic changes made to PECCNT must be done while the SCL is being stretched and only if the previous PECCNT= 0.

Note

For a I2C Controller, dynamic changes made to PECCNT must be done only if the previous PECCNT=0. A PECCNT value of 1 is an invalid configuration as this indicates one PEC byte and zero data bytes in the transaction, which is not possible per the SMBus standard.

For transmitting, an extra byte needs to be inserted into the transmit sequence for each transaction by writing a dummy byte to the TXDATA register. If PECEN is set, I2CC/I2CT calculates the PEC and replaces this dummy byte with the PEC value during transmission when the data byte count reaches the value in PECCNT. For reception, a PEC byte is received the same as a data byte through the RX FIFO. If PECEN is set and the data byte count is equal to the value programmed in PECCNT, the I2CC/I2CT checks the next received byte since that is the PEC. If the PEC byte is non-zero, the PEC_RX_ERR flag in RIS is set and a NACK is transmitted on the line automatically.

The PECSR register is also added to provide status flags relating to PEC operation and functionality for both UNICOMM-I2CC and UNICOMM-I2CT. Each of the fields from the PECSR register are described below.

- PECBYTECNT
  - This is the current PEC Byte Count of the I2C controller or target.
- PECSTS_CHECK
  - This status bit indicates if the PEC was checked in the transaction that occurred before the last STOP. The flag is updated on a STOP condition.
- PECSTS_ERROR

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– This status bit indicates if a PEC check error has occurred in the transaction before the last STOP condition. The flag is updated on a STOP condition.

In a typical I2C Target use case, software can set PECEN=1 and PECCNT=0 and enabled the manual ACK override feature, by setting the ACKOEN bit, until the remaining packet length is known. Software then can set the PECCNT to the remaining packet length (including the PEC byte). Once transmission/reception of the packet is complete, manual ACK override mode can be disabled by clearing ACKOEN.

33.2.3.16.7 Host Notify Protocol

To support the SMBus host notify protocol specifications, UNICOMM-I2CT Advanced instances contain a default host address. When the CTR.EN_DEFHOSTADR bit is set, the default host address of **7'b000_1000** is always used by the Target address match logic for comparison. When this bit is cleared, the default host address is not used for matching.

33.2.3.16.8 Alert Response Protocol

To support the SMBus host notify protocol specifications, UNICOMM-I2CT Advanced instances contain an alert response address. When the CTR.EN_ALRESPADR bit is set, the alert response address of **7'b000_1100** is always matched by the Target address match logic. When this bit is cleared, the alert response address is not matched. GPIO signaling for alarm situations must be handled in software.

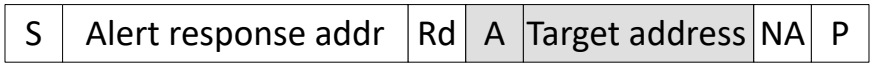


Figure 33-13. Alert Response Message

33.2.3.16.9 Address Resolution Protocol

SMBus target address conflicts can be resolved by dynamically assigning a new unique address to each target device. The Address Resolution Protocol (ARP) outlined below is used by the UNICOMM-I2CC in this event.

1. Prepare to ARP
   a. Controller sends a **Prepare to ARP** command to all the targets on the bus by using the default device address. All targets must ACK this command and clear own addresses.
2. Get UDID
   a. Controller sends the **Get UDID** command to all the targets on the bus. All targets return the unique UDID back to the controller.
   b. Target arbitration happens since all targets are trying to send a UDID to the controller.
3. Assign address
   a. Controller sends the **Assign Address** command to all the target UDID's to assign each device with a new unique address. The controller needs to keep track of the used address pool and corresponding UDID's in software during this process. All targets need to monitor the UDID bytes and change the own address to the assigned address in the event of a UDID match. For UNICOMM-I2CT instances, this can be done in software. The commander can repeat Step 2 and 3, until there are no ACK's from a target after sending a **Get UDID** command, meaning all ARP-capable targets now have valid target addresses assigned.

Additionally to support the ARP process, UNICOMM-I2CT Advanced instances contain a default device address. When the CTR.EN_DEFDEVADR bit is set, a default device address of **7'b110_0001** is always used by the target address match logic. When this bit is cleared, the default device address is not matched. If arbitration is lost, the RIS.ARBLOST interrupt is set, similar to the arbitration logic of the UNICOMM-I2CC module.

33.2.4 Protocol Descriptions

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33.2.4.1 I²C Controller Mode

33.2.4.1.1 I2C Controller Initialization

Follow the high-level UNICOMM configurations in Section 31.3 before executing the below I2CC-specific configurations.

1. Clear the ENABLE bit in the CR register before making any of the below configuration changes.
2. Set the desired SCL clock speed by writing the TPR bit in TPR register with the correct value. For example, with a 20MHz I2Cclk and 100kbps desired SCL clock, a TPR value of 19 (0x13) needs to be written to TPR. For more information about how to calculate the TPR value, refer to *Clock Control*.
3. Configure the desired FIFO trigger levels in the IFLS register.
4. Enable/Disable clock stretching in the CR register.
5. Specify the target address, initial direction of transfer, and addressing mode (7-bit or 10-bit) by writing the TA register.
6. Enable desired interrupts and/or DMA event by using CPU_INT, DMA_TRIG_RX, DMA_TRIG_TX group IMASK registers.
7. (Optionally) Configure the emulation mode for the peripheral in the PDBGCTL register.
8. Enable the I2CC by setting the CR.ENABLE bit.
9. Specify the initial length of transfer, acknowledgement settings, and START/STOP conditions through the CTR register. If operating in controller-transmitter mode, TXDATA can be written with data to be transmitted. Start a frame by writing to the FRM_START bit.

33.2.4.1.2 I2C Controller Status

The application can read the SR register to check the current state of the UNICOMM-I2CC. Status bits that are common across all UNICOMM peripherals and relate to the TX and RX FIFOs are explained in Section 31.2.2.4 from the top-level SPGSS chapter.

33.2.4.1.3 I2C Controller Receive Mode

For an UNICOMM-I2CC to start receiving data out of the idle mode, the user needs to set the START bit in CTR register to generate the START condition. Then the controller automatically sends the START condition followed by the target address as soon as the bus is free.

First, set TA.DIR to 1 to enable receive mode and set CTR.START to 1 to enable the START condition. CTR.BLEN can then be programmed to indicate the number of bytes (n) for the receive operation on Advanced I2CC instances (for Basic UNICOMM-I2CC instances, this length is hardcoded to 1). The CTR.ACK and CTR.STOP bit can then be set or cleared based on user configuration. CTR.FRM_START is set to begin the transaction on the line. The packet format is: START + ADDR + R + (DATA*n) +(ACK/NACK) + STOP. The last data ACK/NACK depends on the ACK bit and an additional STOP condition depends on STOP bit.

After last byte is received, the RXDONE interrupt in the CPU_INT.IIDX register is set to indicate that Controller-Receive transaction is complete. User can use the RXTRG interrupt in CPU_INT.IIDX register to read the data from the RX FIFO. This interrupt triggers when the controller RX FIFO contains >= defined bytes, the trigger level can be defined by using the RXIFSEL bit in IFLS register. The flow chart of controller receiver mode is shown in Figure 33-14.

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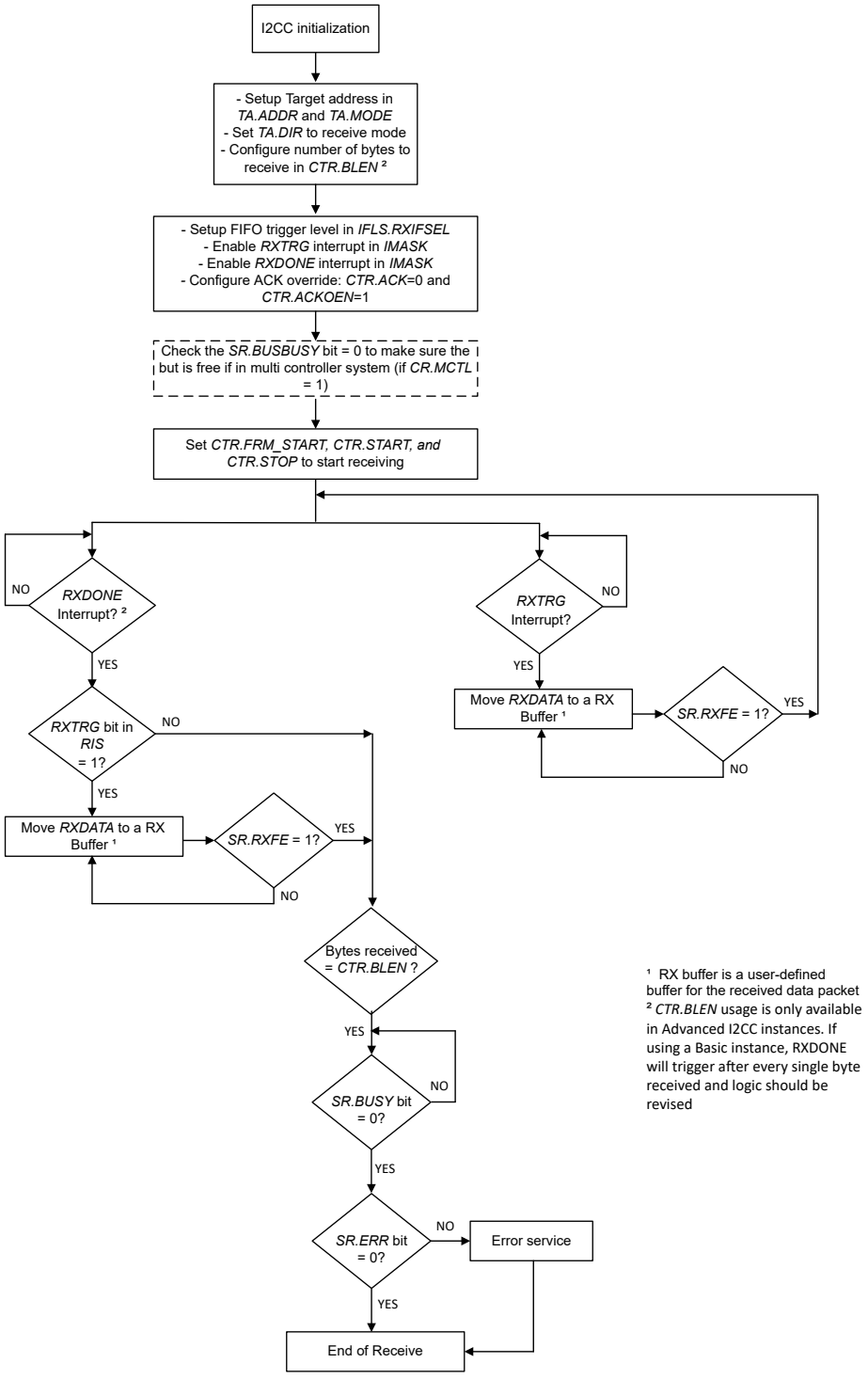


Figure 33-14. Controller Receive Mode

33.2.4.1.4 I2C Controller Transmitter Mode

For a controller to start transmitting data out of idle mode, the user needs to set the START bit in the CTR register to generate the START condition. Then the controller automatically sends the START condition followed by the target address as soon as the bus is free. The data written into TXDATA is transmitted if arbitration is not lost during transmission of the target address.

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First, clear TA.DIR to 0 to enable transmit mode and set CTR.START to 1 to enable the START condition. CTR.BLEN can then be programmed to indicate the number of bytes (n) for the transmit operation on Advanced I2CC instances (for Basic instances this length is hardcoded to 1). The CTR.STOP bit can then be set or cleared based on user configuration. CTR.FRM_START is then set to begin the transaction on the line. The packet format is START + ADDR + W + (DATA*n) + STOP, where transmission of the STOP condition depends on the STOP bit.

After the last byte is transmitted, the TXDONE interrupt in the CPU_INT.IIDX register is set to indicate that the controller transmit transaction is completed. The user can also use the TXEMPTY interrupt from the CPU_INT.IIDX register to see if the TX FIFO is empty and ready to load more data. This interrupt triggers if all data in the transmit FIFO has been shifted out. The flow chart with the nexessary software steps for controller-transmitter mode is shown in Figure 33-15.

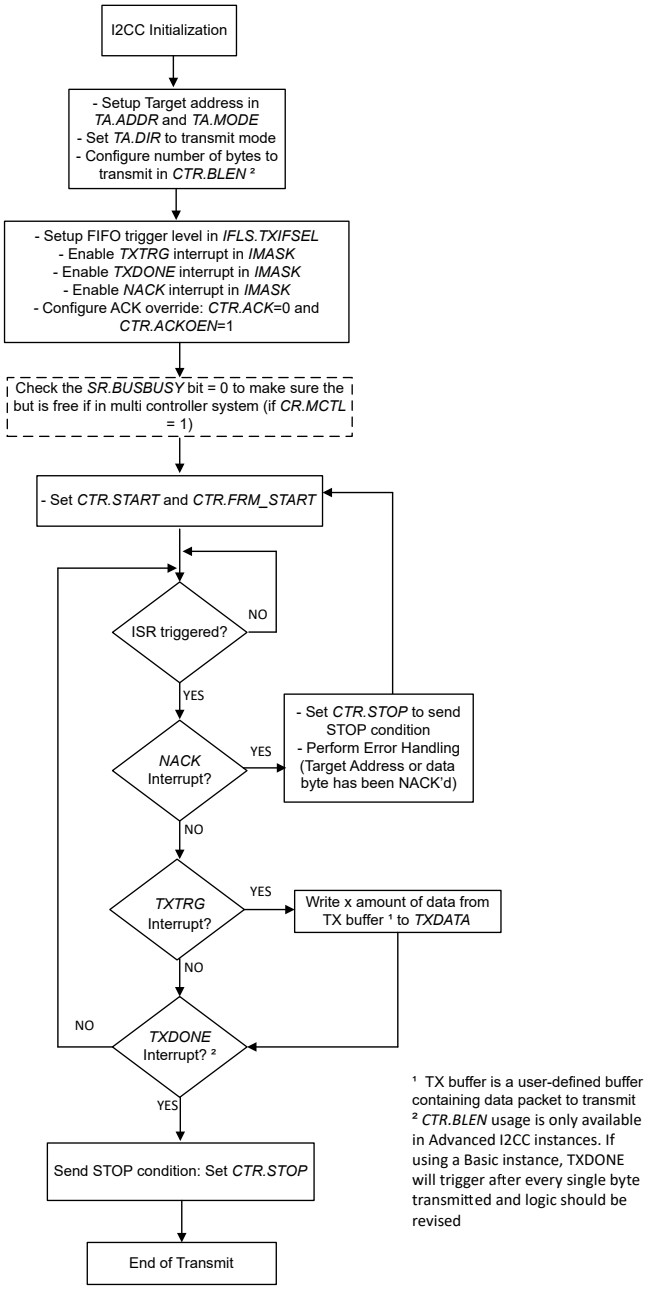


Figure 33-15. Controller Transmitter Mode

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33.2.4.1.5 Controller Configuration

The UNICOMM-I2CC control register (CTR) and UNICOMM-I2CC target address register (TA) are used during the application run to setup controller transmit and receive transactions. The following settings can be used to control each transaction before software reads/writes TXDATA and RXDATA.

- Length indicates the number of bytes for the transaction and is configured by CTR.BLEN bits (Only available in Advanced UNICOMM I2CC instances. In Basic I2CC instances, transaction length is fixed at one.)
- Direction (transmit or receive) is configured by TA.DIR bit
- ACK generation is configured by CTR.ACK and CTR.ACKOEN bit.
- STOP condition generation is configured by CTR.STOP bit.
- START or Repeated START condition generation is configured by the CTR.START bit.
- Start of transmission is enabled by the CTR.FRM_START bit.
- Transmit/Receive status and Error status can be checked with the SR.BUSY and SR.ERR bits respectively.

Controller Transmit Data Transactions

Table 33-4. Start Transmit From Idle Mode

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	0	X	0 or 1	1	1	START+ADDR+R/W+ DATA*n+STOP	Sending of STOP conndition depends on the CTR.STOP bit.

Table 33-5. Continue Transmit when Last Transmission Finished without STOP

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	0	X	0 or 1	0	1	DATA*n+ ACK/ NACK+STOP	Sending of STOP conndition depends on the CTR.STOP bit.

If there is a NACK response from the target, the controller automatically sends out a STOP condition to finish the transmit. The Controller is unable to send a RESTART after a ADDR or DATA NACK.

Controller Receive Data Transactions

Table 33-6. Start Receive from Idle Mode

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	1	0 or 1	0 or 1	1	1	START+ADDR +R/ W+DATA *n +ACK/NACK +STOP	The last data ACK or NACK depends on the CTR.ACK bit; additional sending of STOP condition depends on CTR.STOP bit.

Table 33-7. Continue Receive when Last Receive Finished without STOP or NACK

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	1	0 or 1	0 or 1	0	1	DATA*n+ ACK/NACK +STOP	The last data ACK or NACK depends on the CTR.ACK bit; additional sending of STOP condition depends on CTR.STOP bit.

This configuration is not allowed if last transaction ended with NACK, since NACK can only be followed by a STOP or RESTART condition. The ACK and STOP bits must not be set to 1 at the same time, as the target needs to be informed to release bus lines before sending out STOP.

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Controller Repeated START Transactions

If the last transmit or receive finished without a STOP, a Repeated START can be generated to initiate a new transaction

Table 33-8. Repeated Start Transmit

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	0	0 or 1	0 or 1	1	1	Restart+ADDR +R/ W+DATA*n +STOP	Additional sending of STOP depends on CTR.STOP bit.

If there is a NACK response from the target, the controller automatically sends out a STOP condition to finish the transmit. The Controller is unable to send a RESTART after an ADDR or DATA NACK.

Table 33-9. Repeated Start Receive

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	1	0 or 1	0 or 1	1	1	Restart+ADDR +R/ W+DATA*n +ACK/ NACK+STOP	The last data followed by ACK or NACK depend on CTR.ACK bit; additional sending of STOP depends on CTR.STOP bit.

The ACK and STOP bits must not be set to 1 at the same time, as the target needs to be informed to release bus lines before sending out STOP.

Controller Transmit STOP-only Transaction

Table 33-10. Send STOP only

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
n (n>0)	X	X	1	0	1	STOP	STOP command

Only send this transaction after the previous transaction successfully finishes, The STOP condition can't be sent without a NACK to the target if the controller is currently in receive mode.

Controller Quick Command Transaction

The Quick command can only be sent at the beginning of a transaction, not following other transactions (without a STOP) or repeatted start.

Table 33-11. Controller Quick Command

Length	Direction	ACK	STOP	START	FRM_START	Frame Format	Notes
0	0/1	X	1	1	1	START+ADDR +R/ W+STOP	Quick command

33.2.4.2 I²C Target Mode

33.2.4.2.1 I2C Target Initialization

Follow the high-level UNICOMM configurations in Section 31.3 before executing the below I2CT-specific configurations.

1. Clear the ENABLE bit in the CTR register before making any of the below configuration changes.
2. Configure at least one target address by writing the OAR register. An additional target address can be enabled and configured for Advanced I2CT UNICOMM instances using the OAR2 register.

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3. Configure the desired FIFO trigger levels in the IFLS register.
4. Configure acknowledgement settings in the ACKCTL register.
5. Configure clock stretching, TXTRG/RXTRG interrupt modes, default device addresses, and SMBUS feature settings (only available on Advanced I2CT instances) in the CTR register.
6. Enable desired interrupts and/or DMA event by using CPU_INT, DMA_TRIG_RX, DMA_TRIG_TX group IMASK registers.
7. (Optionally) Configure the emulation mode for the peripheral in the PDBGCTL register.
8. Enable the I2CT by setting the CTR.ENABLE bit.

33.2.4.2.2 I2C Target Status

The application can read the SR register to check the current state of the UNICOMM-I2CT. Status bits that are common across all UNICOMM peripherals and relate to the TX and RX FIFOs are explained in Section 31.2.2.4 from the top-level SPGSS chapter.

33.2.4.2.3 I2C Target Receiver Mode

Target receiver mode is entered when the target address transmitted by the controller matches the I2CT's own address and a **low** R/W bit is received. In target receiver mode, serial data bits received on SDA are shifted in with the clock pulses that are generated by the controller device. The target device does not generate the clock, but can hold SCL low if intervention of the CPU is required after a byte has been received.

After the a data byte is received, the RXDONE interrupt in CPU_INT.IIDX register is set. The I^2C module automatically acknowledges the received data or the user can manually send an acknowledge after each byte received by configuring the ACKCTL register.

When the controller generates a START condition, the START interrupt flag from the CPU_INT.IIDX register is set. When the controller generates a STOP condition, the STOP interrupt flag from the CPU_INT.IIDX register is set.

The user can also use the RXTRG interrupt in CPU_INT.IIDX register to read the data from the receive FIFO. This interrupt triggers when the receive FIFO contains >= defined bytes. The FIFO trigger level can be defined in the RXIFSEL bit in the IFLS register.

The RXDONE approach can be used if the target wants to slow down communication to evaluate reception of every byte, while the RXTRG approach is used to maximize throughput and avoid clock stretching.

The flow chart of using RXDONE and RXFIFOTRG interrupt to read the receive data are shown in Figure 33-16and Figure 33-17 respectively.

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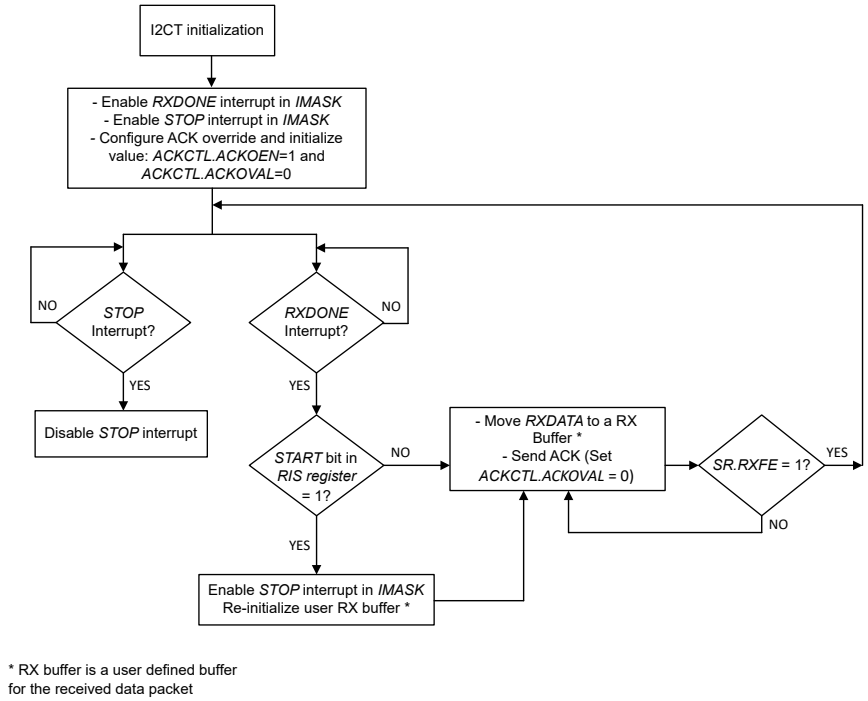


Figure 33-16. Target Receiver Mode using RXDONE and ACK Override

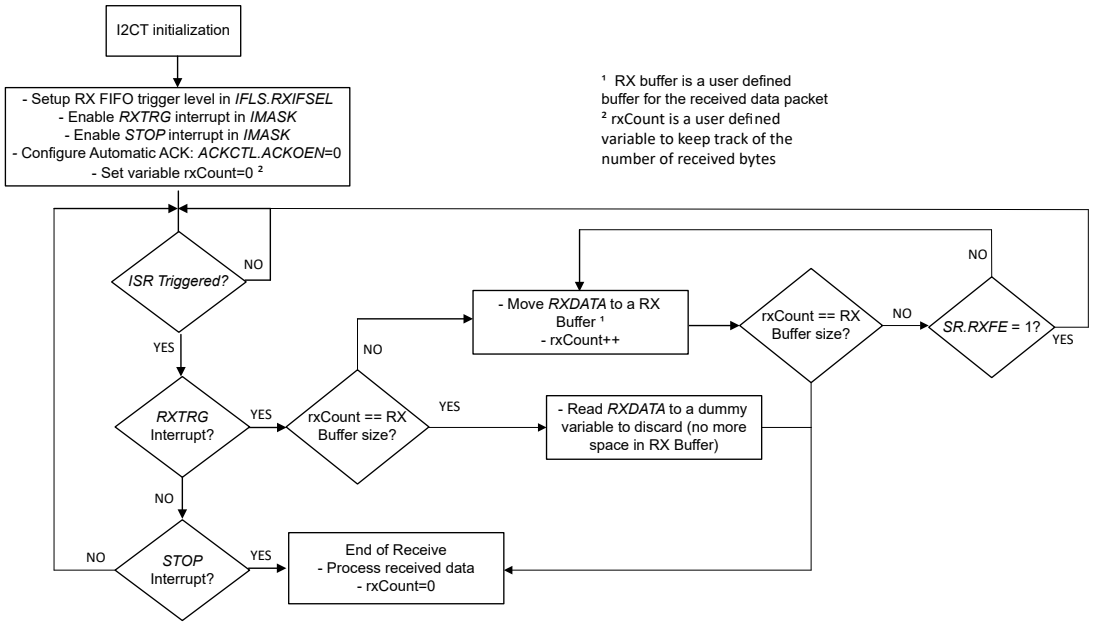


Figure 33-17. Target Receiver Mode using RXTRG and Automatic ACK

33.2.4.2.4 I2C Target Transmitter Mode

Target transmitter mode is entered when the target address transmitted by the controller matches the I2CT's own address with a **high** R/W bit. The target transmitter shifts the serial data out on SDA with the clock pulses that are generated by the controller device. The target device does not generate the clock, but can hold SCL low if intervention of the CPU is required after a byte has been transmitted.

After a data byte is transmitted, the TXDONE interrupt in CPU_INT.IIDX register is set to indicate that a byte has been transmitted.

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When the controller generates a START condition, the START interrupt in CPU_INT.IIDX register is set. When the controller generates a STOP condition, the STOP interrupt in CPU_INT.IIDX register is set.

The user can also use the TXTRG interrupt from the CPU_INT.IIDX register to load data to the transmit FIFO. This interrupt triggers when the transmit FIFO contains <= defined bytes. The FIFO trigger level can be defined by using TXIFSEL field in the IFLS register.

The TXDONE approach is used if the target wants to slow down communication to evaluate the transmission of every byte, while the TXTRG approach is used to maximize throughput and avoid clock stretching.

The flow chat of using TXDONE and TXFIFOTRG interrupt to transmit data are shown in Figure 33-18and Figure 33-19.

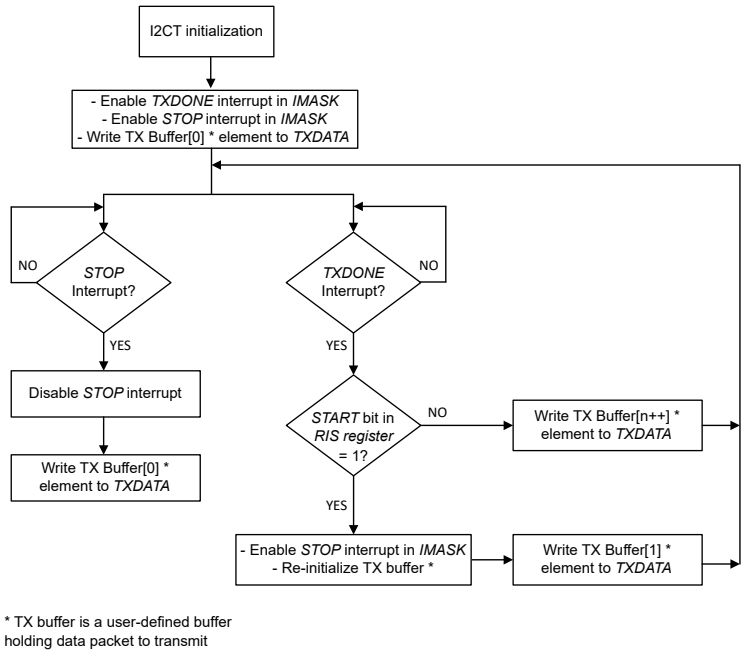


Figure 33-18. Target Transmitter Mode using TXDONE

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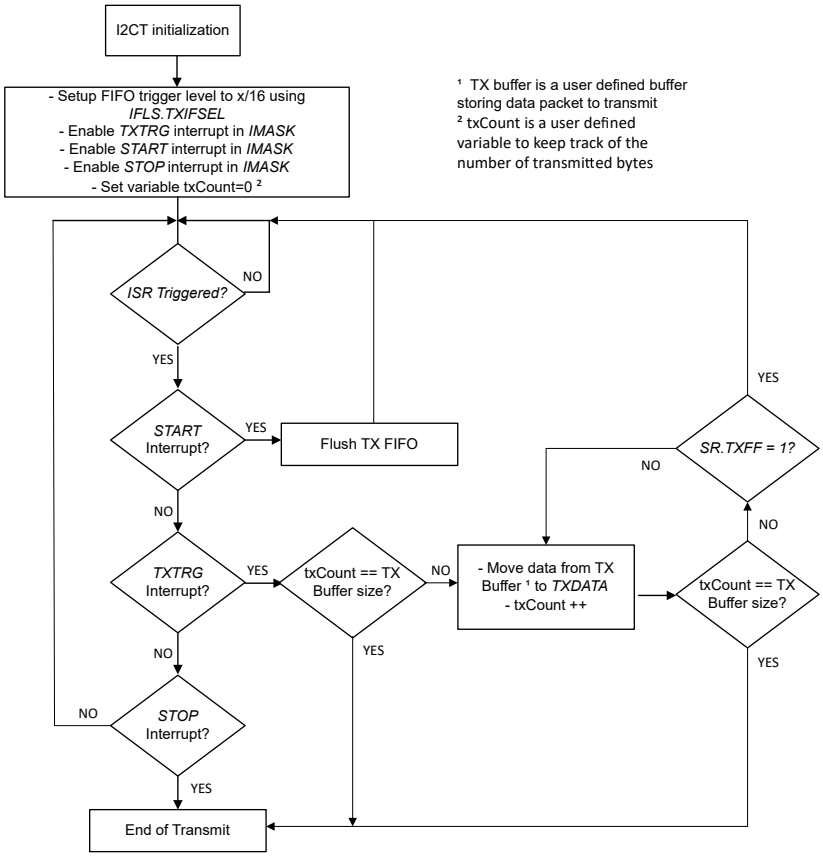


Figure 33-19. Target Transmitter Mode using TXTRG

33.2.5 Reset Considerations

Software Reset Considerations

A Software reset can be executed by setting the RESETASSERT bit together with the KEY bit in the RSTCTL register. Resets must only be issued after terminating a transaction.

Hardware Reset Considerations

A hardware reset also re-initializes the IO configuration. This sets the IOs to a high-impedance state and with the external pullup resistors for I^2C, the lines are pulled high.

Table 33-12 and Table 33-13 shows the behavior of status bits when Controller or Target gets disabled.

Table 33-12. Status Bits when Controller is Disabled

Register	Bit	Behavior when Controller is Disabled	Behavior when Target Disabled	Behavior after Controller/Target is Enabled
SR	BUSY	Reset State	Don't care	Updates START condition sending
	ERR	Reset State	Don't care	Updates on next event detected
	ADRACK	Reset State	Don't care	Updates on next event detected
	DATACK	Reset State	Don't care	Updates on next event detected
	ARBLST	Reset State	Don't care	Updates on next event detected
	IDLE	Reset State	Don't care	Updates on next event detected
	BUSBSY	Reset State	Don't care	Updates on next START detected on bus (or SDA or SCL is low)
	BCNT	Reset State	Don't care	Updates on next event detected
BMON	SCL	Reset State	Don't care	Updates with Controller enable

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Table 33-12. Status Bits when Controller is Disabled (continued)

Register	Bit	Behavior when Controller is Disabled	Behavior when Target Disabled	Behavior after Controller/Target is Enabled
	SDA	Reset State	Don't care	Updates with Controller enable

Table 33-13. Status Bits when Target is Disabled

Register	Bit	Behavior When Controller Disabled	Behavior When Target Disabled	Behavior After Controller/Target Enabled
SR	RREQ	Don't care	Reset State	Updates on next event detected
	TREQ	Don't care	Reset State	Updates on next event detected
	OAR2SEL	Don't care	Reset State	Updates on next event detected
	QCMDST	Don't care	Reset State	Updates on next event detected
	QCMDRW	Don't care	Reset State	Updates on next event detected

33.2.6 Emulation Modes

The module behavior while the device is in debug mode is controlled by the FREE and SOFT bits in PDBGCTL register.

When the device is in debug mode and set into halt mode below behavior can be configured.

Table 33-14. Debug Mode Peripheral Behavior

PDBGCTL.FREE	PDBGCTL.SOFT	Function
1	**x**	Modules continues operation
0	**0**	Module stops immediately
0	**1**	Module stops after the next transfer has been finished

33.3 I2C Interrupts & Triggers

33.3.1 CPU Interrupts (IRQs)

The UNICOMM-I2CC interrupts are fed through the UNICOMM instance interrupt line if that UNICOMM's IPMODE is configured as I2CC. The UNICOMM-I2CT interrupts are fed through the UNICOMM instance interrupt line if that UNICOMM's IPMODE is configured as I2CT. See Section 31.6.1 for more information on the UNICOMM CPU interrupts.

33.3.2 DMA Triggers

The UNICOMM-I2CC DMA triggers (TX and RX) are fed through the UNICOMM instance trigger lines if that UNICOMM's IPMODE is configured as I2CC. The UNICOMM-I2CT DMA triggers (TX and RX) are fed through the UNICOMM instance trigger lines if that UNICOMM's IPMODE is configured as I2CT. See Section 31.6.2 for more information on the TX and RX UNICOMM DMA triggers.

33.4 UNICOMM-I2C Registers

This Section describes the UNICOMM-I2C Registers.

33.4.1 UNICOMM-I2C Base Address Table

Table 33-15. UNICOMM-I2C Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Uc0i2ccRegs	UNICOMMI2CC_REGS	UC0_I2CC	0x4060_8000
Uc1i2ccRegs	UNICOMMI2CC_REGS	UC1_I2CC	0x4060_9000
Uc2i2ccRegs	UNICOMMI2CC_REGS	UC2_I2CC	0x4060_A000

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Table 33-15. UNICOMM-I2C Base Address Table (continued)

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Uc0i2ctRegs	UNICOMMI2CT_REGS	UC0_I2CT	0x4061_0000
Uc1i2ctRegs	UNICOMMI2CT_REGS	UC1_I2CT	0x4061_1000
Uc2i2ctRegs	UNICOMMI2CT_REGS	UC2_I2CT	0x4061_2000
Uc3i2ccRegs	UNICOMMI2CC_REGS	UC3_I2CC	0x4064_8000
Uc4i2ccRegs	UNICOMMI2CC_REGS	UC4_I2CC	0x4064_9000
Uc5i2ccRegs	UNICOMMI2CC_REGS	UC5_I2CC	0x4064_A000
Uc3i2ctRegs	UNICOMMI2CT_REGS	UC3_I2CT	0x4065_0000
Uc4i2ctRegs	UNICOMMI2CT_REGS	UC4_I2CT	0x4065_1000
Uc5i2ctRegs	UNICOMMI2CT_REGS	UC5_I2CT	0x4065_2000

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33.4.2 UNICOMMI2CC_REGS Registers

Table 33-16 lists the memory-mapped registers for the UNICOMMI2CC_REGS registers. All register offset addresses not listed in Table 33-16 should be considered as reserved locations and the register contents should not be modified.

Table 33-16. UNICOMMI2CC_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	CLKDIV	Clock Divider		Go
8h	CLKSEL	Clock Source Selection/Enable.		Go
18h	PDBGCTL	Peripheral Debug Control		Go
20h	IIDX	Interrupt index	CPU_INT	Go
28h	IMASK	Interrupt mask	CPU_INT	Go
30h	RIS	Raw interrupt status	CPU_INT	Go
38h	MIS	Masked interrupt status	CPU_INT	Go
40h	ISET	Interrupt set	CPU_INT	Go
48h	ICLR	Interrupt clear	CPU_INT	Go
58h	IMASK	Interrupt mask	DMA_TRIG_RX	Go
60h	RIS	Raw interrupt status	DMA_TRIG_RX	Go
68h	MIS	Masked interrupt status	DMA_TRIG_RX	Go
70h	ISET	Interrupt set	DMA_TRIG_RX	Go
88h	IMASK	Interrupt mask	DMA_TRIG_TX	Go
90h	RIS	Raw interrupt status	DMA_TRIG_TX	Go
98h	MIS	Masked interrupt status	DMA_TRIG_TX	Go
A0h	ISET	Interrupt set	DMA_TRIG_TX	Go
E4h	INTCTL	Interrupt control register		Go
100h	CTR	Control Register		Go
104h	CR	Configuration		Go
108h	SR	Status Register		Go
10Ch	IFLS	Interrupt FIFO Level Select Register		Go
110h	TPR	Timer Period		Go
118h	GFCTL	I2C Glitch Filter Control		Go
11Ch	BMON	Bus Monitor		Go
120h	TXDATA	TXData		Go
124h	RXDATA	RXData		Go
128h	PECSR	PEC status register		Go
14Ch	TA	Target Address Register		Go
150h	TIMEOUT_CNT	I2C Timeout Count Register		Go
154h	TIMEOUT_CTL	I2C Timeout Count Control Register		Go
158h	PECCTL	I2C PEC control register		Go

Complex bit access types are encoded to fit into small table cells. Table 33-17 shows the codes that are used for access types in this section.

Table 33-17. UNICOMMI2CC_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

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Table 33-17. UNICOMMI2CC_REGS Access Type Codes (continued)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 CLKDIV Register (Offset = 0h) [Reset = 00000000h]

CLKDIV is shown in Figure 33-20 and described in Table 33-18.

Return to the Summary Table.

This register is used to specify the module-specific divide ratio of the I2CC functional clock (I2Cclk).

Figure 33-20. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 33-19. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock Division factor 0 : DIV_BY_1 1 : DIV_BY_2 .... 63: DIV_BY_64 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

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2 CLKSEL Register (Offset = 8h) [Reset = 00000000h]

CLKSEL is shown in Figure 33-21 and described in Table 33-19.

Return to the Summary Table.

I2CC Clock Source Selection.

Figure 33-21. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				MCLKDIV2	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 33-21. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	MCLKDIV2	R/W	0h	Enables MCLKDIV2 as the UNICOMM I2CC clock source. 0h = Does not select this clock as a source 1h = Select this clock as a source
2-0	RESERVED	R/W	0h	

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3 PDBGCTL Register (Offset = 18h) [Reset = 00000000h]

PDBGCTL is shown in Figure 33-22 and described in Table 33-20.

Return to the Summary Table.

I2CC Debug Control. This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input.

Figure 33-22. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 33-23. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft Halt Boundary Control. This function is only available, if [FREE] is set to 'STOP' 0h = Not supported 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free Run Control. 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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4 IIDX Register (Offset = 20h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 33-23 and described in Table 33-21.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index.

Figure 33-23. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 33-25. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	I2CC Interrupt Vector Value. This field provides the highest priority interrupt index. A read clears the corresponding interrupt flag in RIS and MIS. 15h-1Fh = Reserved. 00h = No Interrupt Pending. 01h = Receive Done Flag. 02h = Transmit Done Flag. 03h = Receive FIFO Event. 04h = Transmit FIFO Event. 5h = RX FIFO Full Event/Interrupt Pending. 6h = TX FIFO Empty Event/Interrupt Pending. 08h = Address/Data NACK. 09h = START Event. 0Ah = STOP Event. 0Bh = Arbitration Lost. Ch = PEC Receive Error Event. This event is only available on Advanced I2CC instances. Dh = Timeout Counter A Event. Eh = Timeout Counter B Event. 10h = DMA DONE on Channel RX. 11h = DMA DONE on Channel TX.

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5 IMASK Register (Offset = 28h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 33-24 and described in Table 33-22.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-24. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	ARBLOST	STOP	START
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
NACK	RESERVED	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 33-27. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	0h	
16	DMA_DONE_TX	R/W	0h	I2CC DMA Done on TX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA, indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
15	DMA_DONE_RX	R/W	0h	I2CC DMA Done on RX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	RESERVED	R/W	0h	
13	TIMEOUTB	R/W	0h	I2CC Timeout Counter B Interrupt Mask. This interrupt is raised when the SCL line is continously high for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLB register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	TIMEOUTA	R/W	0h	I2CC Timeout Counter A Interrupt Mask. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
11	PEC_RX_ERR	R/W	0h	I2CC Receive PEC Error Interrupt Mask. This interrupt is raised when the PEC calculated by the I2CC does not match received PEC. This interrupt is only available on Advanced I2CC instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 33-27. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ARBLOST	R/W	0h	I2CC Arbitration Lost Interrupt Mask. This flag indicates that the I2CC has lost an arbitration contest with another Controller in a multi-controller system. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	STOP	R/W	0h	I2CC STOP Detection Interrupt Mask. This interrupt is raised when a STOP condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	START	R/W	0h	I2CC START Detection Interrupt Mask. This interrupt is raised when a START condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	NACK	R/W	0h	I2CC Address/Data NACK Interrupt Mask. This interrupt is raised when an address or data NACK is received by the I2CC. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	RESERVED	R/W	0h	
5	TXEMPTY	R/W	0h	I2CC TX FIFO Empty Interrupt Mask. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CC transmitter goes idle. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	RXFULL	R/W	0h	I2CC RX FIFO Full Interrupt Mask. This interrupt is raised when the RX FIFO is full. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3	TXTRG	R/W	0h	I2CC Transmit Trigger Interrupt Mask. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RXTRG	R/W	0h	I2CC Receive Trigger Interrupt Mask. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	TXDONE	R/W	0h	I2CC Transmit Done Interrupt Mask. This interrupt is raised when a burst length of CTR.BLEN bytes is transmitted. For variants where the BLEN register is not available, it is raised after each byte is transmitted. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '0'. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	RXDONE	R/W	0h	I2CC Receive Done Interrupt Mask. This interrupt is raised when a burst length of CTR.BLEN bytes is received. For variants where the BLEN register is not available, it is raised after each byte is received. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '1'. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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6 RIS Register (Offset = 30h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 33-25 and described in Table 33-23.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-25. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R-0h							R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	ARBLOST	STOP	START
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
NACK	RESERVED	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-29. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	DMA_DONE_TX	R	0h	I2CC DMA Done on TX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	I2CC DMA Done on RX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
14	RESERVED	R	0h	
13	TIMEOUTB	R	0h	I2CC Timeout Counter B Interrupt Raw Status. This interrupt is raised when the SCL line is continously high for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLB register. 0h = Interrupt did not occur 1h = Interrupt occurred
12	TIMEOUTA	R	0h	I2CC Timeout Counter A Interrupt Raw Status. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Interrupt did not occur 1h = Interrupt occurred
11	PEC_RX_ERR	R	0h	I2CC Receive PEC Error Interrupt Raw Status. This interrupt is raised when the PEC calculated by the I2CC does not match received PEC. This interrupt is only available on Advanced I2CC instances. 0h = Interrupt did not occur 1h = Interrupt Occured

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Table 33-29. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ARBLOST	R	0h	I2CC Arbitration Lost Interrupt Raw Status. This flag indicates that the I2CC has lost an arbitration contest with another Controller in a multi-controller system. 0h = Interrupt did not occur 1h = Interrupt occurred
9	STOP	R	0h	I2CC STOP Detection Interrupt Raw Status. This interrupt is raised when a STOP condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Interrupt did not occur 1h = Interrupt occurred
8	START	R	0h	I2CC START Detection Interrupt Raw Status. This interrupt is raised when a START condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Interrupt did not occur 1h = Interrupt occurred
7	NACK	R	0h	I2CC Address/Data NACK Interrupt Raw Status. This interrupt is raised when an address or data NACK is received by the I2CC. 0h = Interrupt did not occur 1h = Interrupt occurred
6	RESERVED	R	0h	
5	TXEMPTY	R	0h	I2CC TX FIFO Empty Interrupt Raw Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CC transmitter goes idle. 0h = Interrupt did not occur 1h = Interrupt occurred
4	RXFULL	R	0h	I2CC RX FIFO Full Interrupt Raw Status. This interrupt is raised when the RX FIFO is full. 0h = Interrupt did not occur 1h = Interrupt occurred
3	TXTRG	R	0h	I2CC Transmit Trigger Interrupt Raw Status. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Interrupt occurred
2	RXTRG	R	0h	I2CC Receive Trigger Interrupt Raw Status. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Interrupt occurred
1	TXDONE	R	0h	I2CC Transmit Done Interrupt Raw Status. This interrupt is raised when a burst length of CTR.BLEN bytes is transmitted. For variants where the BLEN register is not available, it is raised after each byte is transmitted. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '0'. 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXDONE	R	0h	I2CC Receive Done Interrupt Raw Status. This interrupt is raised when a burst length of CTR.BLEN bytes is received. For variants where the BLEN register is not available, it is raised after each byte is received. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '1'. 0h = Interrupt did not occur 1h = Interrupt occurred

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7 MIS Register (Offset = 38h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 33-26 and described in Table 33-24.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 33-26. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R-0h							R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	ARBLOST	STOP	START
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
NACK	RESERVED	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-31. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	DMA_DONE_TX	R	0h	I2CC DMA Done on TX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	I2CC DMA Done on RX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
14	RESERVED	R	0h	
13	TIMEOUTB	R	0h	I2CC Timeout Counter B Interrupt Masked Status. This interrupt is raised when the SCL line is continously high for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLB register. 0h = Clear interrupt mask 1h = Set interrupt mask
12	TIMEOUTA	R	0h	I2CC Timeout Counter A Interrupt Masked Status. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
11	PEC_RX_ERR	R	0h	I2CC Receive PEC Error Interrupt Masked Status. This interrupt is raised when the PEC calculated by the I2CC does not match received PEC. This interrupt is only available on Advanced I2CC instances. 0h = Clear interrupt mask 1h = Set interrupt mask

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Table 33-31. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ARBLOST	R	0h	I2CC Arbitration Lost Interrupt Masked Status. This flag indicates that the I2CC has lost an arbitration contest with another Controller in a multi-controller system. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
9	STOP	R	0h	I2CC STOP Detection Interrupt Masked Status. This interrupt is raised when a STOP condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
8	START	R	0h	I2CC START Detection Interrupt Masked Status. This interrupt is raised when a START condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
7	NACK	R	0h	I2CC Address/Data NACK Interrupt Masked Status. This interrupt is raised when an address or data NACK is received by the I2CC. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
6	RESERVED	R	0h	
5	TXEMPTY	R	0h	I2CC TX FIFO Empty Interrupt Masked Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CC transmitter goes idle. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
4	RXFULL	R	0h	I2CC RX FIFO Full Interrupt Masked Status. This interrupt is raised when the RX FIFO is full. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
3	TXTRG	R	0h	I2CC Transmit Trigger Interrupt Masked Status. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
2	RXTRG	R	0h	I2CC Receive Trigger Interrupt Masked Status. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
1	TXDONE	R	0h	I2CC Transmit Done Interrupt Masked Status. This interrupt is raised when a burst length of CTR.BLEN bytes is transmitted. For variants where the BLEN register is not available, it is raised after each byte is transmitted. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '0'. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
0	RXDONE	R	0h	I2CC Receive Done Interrupt Masked Status. This interrupt is raised when a burst length of CTR.BLEN bytes is received. For variants where the BLEN register is not available, it is raised after each byte is received. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '1'. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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8 ISET Register (Offset = 40h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 33-27 and described in Table 33-25.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-27. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
W-0h							W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	ARBLOST	STOP	START
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
NACK	RESERVED	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 33-33. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	W	0h	
16	DMA_DONE_TX	W	0h	Set I2CC DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
15	DMA_DONE_RX	W	0h	Set I2CC DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
14	RESERVED	W	0h	
13	TIMEOUTB	W	0h	Set I2CC Timeout Counter B Interrupt. This interrupt is raised when the SCL line is continously high for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLB register. 0h = Writing 0 has no effect 1h = Set interrupt
12	TIMEOUTA	W	0h	Set I2CC Timeout Counter A Interrupt. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
11	PEC_RX_ERR	W	0h	Set I2CC Receive PEC Error Interrupt. This interrupt is raised when the PEC calculated by the I2CC does not match received PEC. This interrupt is only available on Advanced I2CC instances. 0h = Writing 0 has no effect 1h = Set interrupt

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Table 33-33. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ARBLOST	W	0h	Set I2CC Arbitration Lost Interrupt. This flag indicates that the I2CC has lost an arbitration contest with another Controller in a multi-controller system. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
9	STOP	W	0h	Set I2CC STOP Detection Interrupt. This interrupt is raised when a STOP condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
8	START	W	0h	Set I2CC START Detection Interrupt. This interrupt is raised when a START condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
7	NACK	W	0h	Set I2CC Address/Data NACK Interrupt. This interrupt is raised when an address or data NACK is received by the I2CC. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
6	RESERVED	W	0h	
5	TXEMPTY	W	0h	Set I2CC TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CC transmitter goes idle. 0h = Writing 0 has no effect 1h = Set Interrupt
4	RXFULL	W	0h	Set I2CC RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Writing 0 has no effect 1h = Set Interrupt
3	TXTRG	W	0h	Set I2CC Transmit Trigger Interrupt. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RXTRG	W	0h	Set I2CC Receive Trigger Interrupt. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	TXDONE	W	0h	Set I2CC Transmit Done Interrupt. This interrupt is raised when a burst length of CTR.BLEN bytes is transmitted. For variants where the BLEN register is not available, it is raised after each byte is transmitted. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '0'. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
0	RXDONE	W	0h	Set I2CC Receive Done Interrupt. This interrupt is raised when a burst length of CTR.BLEN bytes is received. For variants where the BLEN register is not available, it is raised after each byte is received. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '1'. 0h = Writing 0 has no effect 1h = Set Interrupt Mask

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9 ICLR Register (Offset = 48h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 33-28 and described in Table 33-26.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 33-28. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
W-0h							W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	ARBLOST	STOP	START
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
NACK	RESERVED	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 33-35. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	W	0h	
16	DMA_DONE_TX	W	0h	Clear I2CC DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
15	DMA_DONE_RX	W	0h	Clear I2CC DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CC from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
14	RESERVED	W	0h	
13	TIMEOUTB	W	0h	Clear I2CC Timeout Counter B Interrupt. This interrupt is raised when the SCL line is continously high for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLB register. 0h = Writing 0 has no effect 1h = Clear Interrupt
12	TIMEOUTA	W	0h	Clear I2CC Timeout Counter A Interrupt. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
11	PEC_RX_ERR	W	0h	Clear I2CC Receive PEC Error Interrupt. This interrupt is raised when the PEC calculated by the I2CC does not match received PEC. This interrupt is only available on Advanced I2CC instances. 0h = Writing 0 has no effect 1h = Clear Interrupt

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Table 33-35. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ARBLOST	W	0h	Clear I2CC Arbitration Lost Interrupt. This flag indicates that the I2CC has lost an arbitration contest with another Controller in a multi-controller system. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
9	STOP	W	0h	Clear I2CC STOP Detection Interrupt. This interrupt is raised when a STOP condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
8	START	W	0h	Clear I2CC START Detection Interrupt. This interrupt is raised when a START condition is detected on the bus, either generated by the current I2CC or another I2C Controller when in multi-master mode. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
7	NACK	W	0h	Clear I2CC Address/Data NACK Interrupt. This interrupt is raised when an address or data NACK is received by the I2CC. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
6	RESERVED	W	0h	
5	TXEMPTY	W	0h	Clear I2CC TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CC transmitter goes idle. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	RXFULL	W	0h	Clear I2CC RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	TXTRG	W	0h	Clear I2CC Transmit Trigger Interrupt Mask. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RXTRG	W	0h	Clear I2CC Receive Trigger Interrupt Mask. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	TXDONE	W	0h	Clear I2CC Transmit Done Interrupt. This interrupt is raised when a burst length of CTR.BLEN bytes is transmitted. For variants where the BLEN register is not available, it is raised after each byte is transmitted. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '0'. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
0	RXDONE	W	0h	Clear I2CC Receive Done Interrupt. This interrupt is raised when a burst length of CTR.BLEN bytes is received. For variants where the BLEN register is not available, it is raised after each byte is received. In the case of a quick command, the interrupt is raised when a quick command with R/Wn bit set to '1'. 0h = Writing 0 has no effect 1h = Set Interrupt Mask

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10 IMASK Register (Offset = 58h) [Reset = 00000000h] (DMA_TRIG_RX)

IMASK is shown in Figure 33-29 and described in Table 33-27.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-29. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R/W-0h					R/W-0h	R/W-0h	

Table 33-37. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2	RXTRG	R/W	0h	I2CC Receive DMA Trigger Mask. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1-0	RESERVED	R/W	0h	

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11 RIS Register (Offset = 60h) [Reset = 00000000h] (DMA_TRIG_RX)

RIS is shown in Figure 33-30 and described in Table 33-28.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-30. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R-0h					R-0h	R-0h	

Table 33-39. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RXTRG	R	0h	I2CC Receive DMA Trigger Raw Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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12 MIS Register (Offset = 68h) [Reset = 00000000h] (DMA_TRIG_RX)

MIS is shown in Figure 33-31 and described in Table 33-29.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers. A flag set in this register can be cleared by writing 1 to the ICLR register bit.

Figure 33-31. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R-0h					R-0h	R-0h	

Table 33-41. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RXTRG	R	0h	I2CC Receive DMA Trigger Masked Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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13 ISET Register (Offset = 70h) [Reset = 00000000h] (DMA_TRIG_RX)

ISET is shown in Figure 33-32 and described in Table 33-30.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-32. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
W-0h					W-0h	W-0h	

Table 33-43. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	W	0h	
2	RXTRG	W	0h	Set I2CC Receive DMA Trigger. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
1-0	RESERVED	W	0h	

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14 IMASK Register (Offset = 88h) [Reset = 00000000h] (DMA_TRIG_TX)

IMASK is shown in Figure 33-33 and described in Table 33-31.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-33. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 33-45. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	TXTRG	R/W	0h	I2CC Transmit DMA Trigger Mask. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2-0	RESERVED	R/W	0h	

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15 RIS Register (Offset = 90h) [Reset = 00000000h] (DMA_TRIG_TX)

RIS is shown in Figure 33-34 and described in Table 33-32.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-34. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R-0h				R-0h	R-0h		

Table 33-47. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	TXTRG	R	0h	I2CC Transmit DMA Trigger Raw Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
2-0	RESERVED	R	0h	

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16 MIS Register (Offset = 98h) [Reset = 00000000h] (DMA_TRIG_TX)

MIS is shown in Figure 33-35 and described in Table 33-33.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 33-35. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R-0h				R-0h	R-0h		

Table 33-49. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	TXTRG	R	0h	I2CC Transmit DMA Trigger Masked Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
2-0	RESERVED	R	0h	

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17 ISET Register (Offset = A0h) [Reset = 00000000h] (DMA_TRIG_TX)

ISET is shown in Figure 33-36 and described in Table 33-34.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-36. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
W-0h				W-0h	W-0h		

Table 33-51. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	TXTRG	W	0h	Set I2CC Transmit DMA Trigger. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
2-0	RESERVED	W	0h	

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18 INTCTL Register (Offset = E4h) [Reset = 00000000h]

INTCTL is shown in Figure 33-37 and described in Table 33-35.

Return to the Summary Table.

Interrupt Control Register.

Figure 33-37. INTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTEVAL
W-0h							W-0h

Table 33-53. INTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTEVAL	W	0h	Writing a 1 to this field re-evaluates the interrupt sources. 0h = Writing 0 has no effect 1h = Interrupt Eval

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19 CTR Register (Offset = 100h) [Reset = 00000000h]

CTR is shown in Figure 33-38 and described in Table 33-36.

Return to the Summary Table.

I2CC Control Register. Configures the I2CC operation.

Figure 33-38. CTR Register

31	30	29	28	27	26	25	24
RESERVED				BLEN			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
BLEN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	SUSPEND	RD_ON_TXEMPTY	ACKOEN	ACK	STOP	START	FRM_START
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 33-55. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	
27-16	BLEN	R/W	0h	I2CC Transaction Length. This field contains the programmed length of bytes of the next transaction. For variants that don't have the BLEN register, the BLEN is hardcoded to a value of 1. 0h = Smallest value FFFh = Highest possible value
15-7	RESERVED	R/W	0h	
6	SUSPEND	R/W	0h	Suspend External Communication. When this bit is set, I2CC communication on the external bus is suspended after the I2CC FSM goes idle (SR.BUSY reads '0'). 0h = Normal communication 1h = External communication suspended
5	RD_ON_TXEMPTY	R/W	0h	Read on TX EMPTY Enable/Disable. This feature initiates an I2CC write followed by a I2CC read without needing application intervention. 0h = No special behavior 1h = The I2CC will transmit all the bytes from TX FIFO, issue a RESTART and receive data as per programmed burst length (BLEN). This bit is ignored if DIR bit is not set to READ.

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Table 33-55. CTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ACKOEN	R/W	0h	ACK Override Enable When ACKOEN is enabled: 1. I2CC receives data according to the configured burst length (BLEN). 2. Upon receiving the complete data burst, I2CC generates a RXDONE interrupt. 3. The I2CC then holds SCL line low (clock stretching) during the acknowledge phase. 4. This pause gives the application time to update the ACKOVAL register. At this point, application has two options: Option 1: Terminate transaction 1. Set ACKOVAL to send a NACK. 2. The I2CC will automatically generate a STOP condition after the NACK. Option 2: Continue transaction 1. Clear ACKOVAL to send an ACK. 2. Update any other settings as needed. 3. The transaction will proceed based on the new configuration. This mechanism allows the application to control the transaction flow after each data burst is received. Note: In some variants, when BLEN register is not available, the design implements a hardcoded BLEN value of '1'. Consult your device datasheet. 0h = No special behavior 1h = Acknowledge Override Feature Enabled
3	ACK	R/W	0h	Final Data Acknowledge Value. Determines whether a ACK or NACK is automatically sent by the I2CC after the last byte, of length 'N', are received from the target. This setting is used when CTR.ACKOEN=0. 0h = The last received data byte of a transaction is not acknowledged automatically. 1h = The last received data byte of a transaction is acknowledged automatically.
2	STOP	R/W	0h	Enable STOP Condition Generation. I2CC is enabled to send the STOP condition on the bus at the end of the current transaction, per the I2C protocol. 0h = The controller does not generate the STOP condition. 1h = The controller generates the STOP condition.
1	START	R/W	0h	Enable START Condition Generation. I2CC is enabled to send the START condition on the bus per the I2C protocol, when CTR.FRM_START is also set. 0h = The controller does not generate the START condition. 1h = The controller generates the START or repeated START condition.
0	FRM_START	R/W	0h	Frame Start. Start the transaction on the I2C bus according to the programmed settings. 0h = Write of '0' has no effect. Reads back '0' when there is no ongoing transaction 1h = When written to '1', a new transaction is started. Has no effect if there is an ongoing transaction. Reads back as '1' if the transaction is ongoing

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20 CR Register (Offset = 104h) [Reset = 00000000h]

CR is shown in Figure 33-39 and described in Table 33-37.

Return to the Summary Table.

I2CC Configuration Register. Configures and enables the I2CC.

Figure 33-39. CR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					CLKSTRETCH	MCTL	ENABLE
R/W-0h					R/W-0h	R/W-0h	R/W-0h

Table 33-57. CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2	CLKSTRETCH	R/W	0h	Clock Stretching Enable. This bit enables/disables clock stretching detection of the I2CC. 0h = Disables the clock stretching detection. This can be disabled if no Target on the bus does support clock stretching, so that the maximum speed on the bus can be reached. 1h = Enables the clock stretching detection. Enabling the clock stretching ensures compliance to the I2C standard but could limit the speed due the clock stretching.
1	MCTL	R/W	0h	Multi-Controller Mode Enable/Disable. In Multi-Controller mode, the SCL high time begins counting once the SCL line has been detected high. If this bit is not set, the SCL high time begins counting as soon as the SCL line has been set high by the I2CC. 0h = Disable MultiController mode. 1h = Enable MultiController mode.
0	ENABLE	R/W	0h	Enable I2CC module. After this bit has been set, it should not be set again unless it has been cleared by writing a 0 or by a reset, otherwise transfer failures may occur. 0h = Disables operation. 1h = Enables operation.

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21 SR Register (Offset = 108h) [Reset = 00000000h]

SR is shown in Figure 33-40 and described in Table 33-38.

Return to the Summary Table.

I2CC Status Register. This status register indicates the current state of the I2CC.

Figure 33-40. SR Register

31	30	29	28	27	26	25	24
RESERVED				BCNT			
R-0h				R-0h			
23	22	21	20	19	18	17	16
BCNT							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	TXFF	TXFE	RXFF	RXFE	TXCLR	RXCLR	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	BUSBSY	IDLE	ARBLST	DATACK	ADRACK	ERR	BUSY
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-59. SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27-16	BCNT	R	0h	Burst Transaction Count Status. This field contains the current count-down value of the transaction. This field is only available on Advanced I2CC instances. 0h = Smallest value FFFh = Highest possible value
15	RESERVED	R	0h	
14	TXFF	R	0h	TX FIFO Full Status. 0h = TX FIFO is not full 1h = TX FIFO is full
13	TXFE	R	1h	TX FIFO Empty Status. 0h = TX FIFO is not empty 1h = TX FIFO is empty
12	RXFF	R	0h	RX FIFO Full Status. 0h = RX FIFO is not full 1h = RX FIFO is full
11	RXFE	R	1h	RX FIFO Empty Status. 0h = RX FIFO is not empty 1h = RX FIFO is empty
10	TXCLR	R	0h	TX FIFO Clear Status. 0h = TX FIFO is not cleared 1h = TX FIFO clear is complete
9	RXCLR	R	0h	RX FIFO Clear Status. 0h = RX FIFO is not cleared 1h = RX FIFO clear is complete
8-7	RESERVED	R	0h	

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Table 33-59. SR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BUSBSY	R	0h	I2C Bus Busy Status. Indicates when the external line is busy 1. It is set when there is an ongoing transaction on the bus (i.e. if there is a START condition observed) or if SCL toggles. 2. It is cleared upon a STOP condition or when HIGH TIMEOUT occurs & SCL/SDA are both at their IDLE state. This bit reads back '0' when ACTIVE is cleared. The I2CC will wait until this bit is cleared before starting an I2C transaction. When enabling the controller initially, the application should wait for one I2C clock period, poll BUSBSY and start a transaction. 0h = The I2C bus is idle. 1h = SET
5	IDLE	R	1h	I2CC FSM Idle Status. This bit is set when the internal I2CC state machine, rather than when the external bus, is not busy with an ongoing transaction i.e. there is no transmit/receive of data bytes, START, RESTART, Address or STOP signal generation occuring. 0h = The I2C controller is not idle. 1h = The I2C controller is idle.
4	ARBLST	R	0h	Arbitration Lost Status. This status bit indicates whether or not the I2CC won arbitration on the bus. 0h = The I2C controller won arbitration. 1h = The I2C controller lost arbitration.
3	DATACK	R	0h	Data Acknowledge Status. This status bit indicates the acknowledgement status of the previously transmitted data byte. 0h = The transmitted data was acknowledged 1h = The transmitted data was not acknowledged.
2	ADRACK	R	0h	Acknowledge Address 0h = The transmitted address was acknowledged 1h = The transmitted address was not acknowledged.
1	ERR	R	0h	NACK Error Status. This status bit indicates the acknowledgement status of the previously transmitted target address or data byte. 0h = No error was detected on the last operation. 1h = An error occurred on the last operation.
0	BUSY	R	0h	I2CC FSM Busy Status. This bit is set when the internal I2CC state machine, rather than when the external bus, is busy with an ongoing transaction i.e. during transmit/receive of data bytes configured as per BLEN including START, RESTART, Address and STOP signal generation. In variants where the BLEN register is not available, the design implements a hardcoded BLEN value of '1'. 0h = The controller is idle. 1h = The controller is busy.

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22 IFLS Register (Offset = 10Ch) [Reset = 00000022h]

IFLS is shown in Figure 33-41 and described in Table 33-39.

Return to the Summary Table.

I2CC Interrupt FIFO Level Select Register. The IFLS register is the interrupt FIFO level select register. Use this register to define the levels at which the TX, RX, and Receive timeout interrupt flags are triggered. The interrupts are generated based on a transition through a level rather than being based on the level itself. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered when the receive FIFO is filled with two or more characters. Out of reset, the TXIFLSEL and RXIFLSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Figure 33-41. IFLS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RXCLR	RXIFLSEL			TXCLR	TXIFLSEL		
R/W-0h	R/W-2h			R/W-0h	R/W-2h		

Table 33-61. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	RXCLR	R/W	0h	RX FIFO Clear. Setting this bit will clear the RX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
6-4	RXIFLSEL	R/W	2h	RX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Opposite of empty 5h = RX FIFO is full 6h = RX_FIFO >= (MAX_FIFO_LEN -1) 7h = RX_FIFO <= 1
3	TXCLR	R/W	0h	TX FIFO Clear. Setting this bit will clear the TX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
2-0	TXIFLSEL	R/W	2h	TX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Opposite of full 5h = TX FIFO is empty 6h = TX FIFO <= 1 7h = TX_FIFO >= (MAX_FIFO_LEN -1)

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23 TPR Register (Offset = 110h) [Reset = 00000001h]

TPR is shown in Figure 33-42 and described in Table 33-40.

Return to the Summary Table.

I2CC Timer Period Register. This register programs the clock period of the SCL line. Transmission speeds of Standard mode (100kbps), Fast mode (400 kbps), or Fast mode plus (1Mbps) are supported.

Figure 33-42. TPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																									TPR						
R/W-0h																									R/W-1h						

Table 33-63. TPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	0h	
6-0	TPR	R/W	1h	Timer Period. This field is used in the equation to configure SCL_PERIOD SCL_PERIOD = (((1 + TPR) x (SCL_LP + SCL_HP)) + (2 x CLK_PRD)) x CLK_PRD Where: - SCL_PRD is the SCL line period (I2C clock). - TPR is the Timer Period register value (range of 1 to 127). - SCL_LP is the SCL Low period (fixed at 6). - SCL_HP is the SCL High period (fixed at 4). - CLK_PRD is the functional clock period in ns. 1h = Smallest value 7Fh = Highest possible value

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24 GFCTL Register (Offset = 118h) [Reset = 00000000h]

GFCTL is shown in Figure 33-43 and described in Table 33-41.

Return to the Summary Table.

I2CC Glitch Filter Control Register. This register configures the glitch filter on the SCL and SDA lines.

Figure 33-43. GFCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							AGFEN
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						DGFSEL	
R/W-0h						R/W-0h	

Table 33-65. GFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	AGFEN	R/W	0h	Analog Glitch Suppression Enable. 0h = Analog Glitch Filter disable 1h = Analog Glitch Filter enable
7-3	RESERVED	R/W	0h	
2-0	DGFSEL	R/W	0h	Digital Glitch Suppression Pulse Width. The digital glitch filter is only available on Basic I2CC instances. This field controls the pulse width select for glitch suppression on the SCL and SDA lines. The following glitch suppression values are in terms of I2Cclk cycles. 0h = Bypass 1h = 1 clock 2h = 2 clocks 3h = 3 clocks 4h = 4 clocks 5h = 8 clocks 6h = 16 clocks 7h = 31 clocks

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25 BMON Register (Offset = 11Ch) [Reset = 00000003h]

BMON is shown in Figure 33-44 and described in Table 33-42.

Return to the Summary Table.

I2CC Bus Monitor Register. This register is used to read the current SCL and SDA signal logic levels.

Figure 33-44. BMON Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SDA	SCL
R-0h														R-1h	R-1h

Table 33-67. BMON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1	SDA	R	1h	I2C SDA Status. 0h = The I2CSDA signal is low. 1h = The I2CSDA signal is high. Note: During and right after reset, the SDA pin is in GPIO input mode without the internal pull enabled. For proper I2C operation, the user should have the external pull-up resistor in place before starting any I2C operations.
0	SCL	R	1h	I2C SCL Status. 0h = The I2CSCL signal is low. 1h = The I2CSCL signal is high. Note: During and right after reset, the SCL pin is in GPIO input mode without the internal pull enabled. For proper I2C operation, the user should have the external pull-up resistor in place before starting any I2C operations.

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26 TXDATA Register (Offset = 120h) [Reset = 00000000h]

TXDATA is shown in Figure 33-45 and described in Table 33-43.

Return to the Summary Table.

I2CC Transmit Data Register. This register is the transmit data register (the interface to the TX FIFO). For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the TX FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the TX FIFO).

Figure 33-45. TXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
W-0h																								W-0h							

Table 33-69. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	W	0h	
7-0	DATA	W	0h	Transmit Data. This byte contains the data to be transferred during the next transaction. 0h = Smallest value FFh = Highest possible value

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27 RXDATA Register (Offset = 124h) [Reset = 00000000h]

RXDATA is shown in Figure 33-46 and described in Table 33-44.

Return to the Summary Table.

I2CC Receive Data Register. This field contains the current byte being read in the RX FIFO If the FIFO is not present, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO). The received data can be retrieved by reading this register.

Figure 33-46. RXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								R-0h							

Table 33-71. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	DATA	R	0h	Received Data. This field contains the last received data. 0h = Smallest value FFh = Highest possible value

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28 PECSR Register (Offset = 128h) [Reset = 00000000h]

PECSR is shown in Figure 33-47 and described in Table 33-45.

Return to the Summary Table.

I2CC PEC Status Register. This status register can be used to read the current status of the packet error checking mechanism.

Figure 33-47. PECSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						PECSTS_ERROR	PECSTS_CHECK
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							PECBYTECNT
R-0h							R-0h
7	6	5	4	3	2	1	0
PECBYTECNT							
R-0h							

Table 33-73. PECSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17	PECSTS_ERROR	R	0h	PEC Status Error. This status bit indicates if a PEC check error occurred in the transaction that occurred before the last STOP. This bit is cleared automatically when the next STOP condition is observed on the bus. 0h = Indicates PEC check error did not occur in the transaction that occurred before the last STOP 1h = Indicates if a PEC check error occurred in the transaction that occurred before the last STOP
16	PECSTS_CHECK	R	0h	PEC Status Check. This status bit indicates if the PEC was checked in the transaction that occurred before the last STOP. This bit is cleared automatically when the next STOP condition is observed on the bus. 0h = Indicates PEC was not checked in the transaction that occurred before the last STOP 1h = Indicates if the PEC was checked in the transaction that occurred before the last STOP
15-9	RESERVED	R	0h	
8-0	PECBYTECNT	R	0h	PEC Byte Count. This is the current PEC Byte Count of the Controller State Machine. 0h = Minimum Value 1FFh = Maximum Value

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29 TA Register (Offset = 14Ch) [Reset = 00000000h]

TA is shown in Figure 33-48 and described in Table 33-46.

Return to the Summary Table.

I2CC Target Address Register. This register configures the target address, addressing mode, and direction (controller-transmit or controller-receive) of the next transaction.

Figure 33-48. TA Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
MODE	RESERVED				ADDR		
R/W-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
ADDR							DIR
R/W-0h							R/W-0h

Table 33-75. TA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	MODE	R/W	0h	Address Mode Select. This bit selects the addressing mode to be used. When 0, 7-bit addressing is used. When 1, 10-bit addressing is used. 0h = 7-bit addressing mode 1h = 10-bit addressing mode
14-11	RESERVED	R/W	0h	
10-1	ADDR	R/W	0h	I2C Target Address. This field specifies bits A9 through A0 of the Target address. In 7-bit addressing mode, as selected by TA.MODE bit, the top 3 bits are don't care. 0h = Smallest value 3FFh = Highest possible value
0	DIR	R/W	0h	Receive/Transmit Direction. The DIR bit specifies if the next operation is a Receive (High) or Transmit (Low). 0h = Transmit 1h = Receive 0h = in transmit mode. 1h = is in receive mode.

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30 TIMEOUT_CNT Register (Offset = 150h) [Reset = 00020002h]

TIMEOUT_CNT is shown in Figure 33-49 and described in Table 33-47.

Return to the Summary Table.

I2CC Timeout Count Register. This register contains the upper 8 bits of a 12-bit current counter values for Timeout Counter A and Timeout Counter B. The lower four bits of the counter are not user visible and are always 0h.

Figure 33-49. TIMEOUT_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TCNTB								RESERVED								TCNTA							
R-0h								R-2h								R-0h								R-2h							

Table 33-77. TIMEOUT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23-16	TCNTB	R	2h	Timeout Count B Current Count. This field contains the upper 8 bits of a 12-bit current counter for Timeout Counter B. This field is only available on Advanced I2CC instances. 0h = Smallest Value FFh = Highest possible value
15-8	RESERVED	R	0h	
7-0	TCNTA	R	2h	Timeout Count A Current Count. This field contains the upper 8 bits of a 12-bit current counter for Timeout Counter A. 0h = Smallest Value FFh = Highest possible value

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31 TIMEOUT_CTL Register (Offset = 154h) [Reset = 00020002h]

TIMEOUT_CTL is shown in Figure 33-50 and described in Table 33-48.

Return to the Summary Table.

I2CC Timeout Control Register. This register configures Timeout Counter A and Timeout Counter B.

Figure 33-50. TIMEOUT_CTL Register

31	30	29	28	27	26	25	24
TCNTBEN	RESERVED						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
TCNTLB							
R/W-2h							
15	14	13	12	11	10	9	8
TCNTAEN	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
TCNTLA							
R/W-2h							

Table 33-79. TIMEOUT_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCNTBEN	R/W	0h	Timeout Counter B Enable. This field is only available on Advanced I2CC instances. 0h = Disable Timeout Counter B 1h = Enable Timeout Counter B
30-24	RESERVED	R/W	0h	
23-16	TCNTLB	R/W	2h	Timeout Count B Load. Counter B is used for SCL High Detection. This field contains the upper 8 bits of a 12-bit pre-load value for the Timeout Counter B. NOTE: The value of CNTLB must be greater than 1h. Each count is equal to 1* clock period. For example, with 10MHz functional clock one timeout period will be equal to1*100ns. 0h = Smallest possible value FFh = Highest possible value
15	TCNTAEN	R/W	0h	Timeout Counter A Enable. 0h = Disable Timeout Counter A 1h = Enable Timeout Counter A
14-8	RESERVED	R/W	0h	
7-0	TCNTLA	R/W	2h	Timeout Counter A Load Value. Counter A is used for SCL low detection. This field contains the upper 8 bits of a 12-bit pre-load value for the Timeout Counter A. NOTE: The value of CNTLA must be greater than 1h. Each count is equal to 520 times the timeout period of functional clock. For example, with 8MHz functional clock and a 100KHz operating I2C clock, one timeout period will be equal to (1 / 8MHz) * 520 or 65 us. 0h = Smallest Value FFh = Highest possible value

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32 PECCTL Register (Offset = 158h) [Reset = 00000000h]

PECCTL is shown in Figure 33-51 and described in Table 33-49.

Return to the Summary Table.

I2CC PEC Control Register. This register configures the packet error checking (PEC) feature. This register is only available on Advanced I2CC instances.

Figure 33-51. PECCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			PECEN	RESERVED			PECCNT
R/W-0h			R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PECCNT							
R/W-0h							

Table 33-81. PECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	PECEN	R/W	0h	PEC Enable. This bit enables the SMB Packet Error Checking (PEC). When enabled, the PEC is calculated on all bits except the START, STOP, and ACK/NACK. The PEC LSFR and the Byte Counter is set to 0 when the State Machine is in the IDLE state, which occur following a STOP or when a timeout occurs. The Counter is also set to 0 after the PEC byte is sent or received. Note that the NACK is automatically send following a PEC byte that results in a PEC error. The PEC Polynomial is x^8 + x^2 + x^1 + 1. 0h = PEC is disabled 1h = PEC is enabled
11-9	RESERVED	R/W	0h	

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Table 33-81. PECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	PECCNT	R/W	0h	PEC Count. When this field is non zero, the number of I2C bytes are counted (Note that although the PEC is calculated on the I2C address it is not counted at a byte). When the byte count = PECCNT and the I2CC is transmitting, the contents of the LSFR is loaded into the shift register instead of the byte received from the TX FIFO. When the state machine is receiving, after the last bit of this byte is received the LSFR is checked and if it is non-zero, a PEC RX Error interrupt is generated. The I2C packet must be padded to include the PEC byte for both transmit and receive. In transmit mode, the FIFO must be loaded with a dummy PEC byte. In receive mode, the PEC byte will be passed to the RX FIFO. In the a typical controller use case, the application would set PECEN=1 and PECCNT=SMB packet length (not including the Target Address byte, but including the PEC byte). The I2CC application would then configure the DMA to allow the packet to complete unassisted and write CTR to initiate the transaction. Note that when the byte count = PECCNT, the byte count is reset to 0 and multiple PEC calculations can automatically occur within a single I2C transaction. Note that any write to the PECCTL register will clear the current PEC byte count in the I2CC state machine. 0h = Minimum Value 1FFh = Maximum Value

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33.4.3 UNICOMMI2CT_REGS Registers

Table 33-50 lists the memory-mapped registers for the UNICOMMI2CT_REGS registers. All register offset addresses not listed in Table 33-50 should be considered as reserved locations and the register contents should not be modified.

Table 33-82. UNICOMMI2CT_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	CLKDIV	Clock Divider		Go
8h	CLKSEL	Clock Source Selection/Enable.		Go
18h	PDBGCTL	Peripheral Debug Control		Go
20h	IIDX	Interrupt index	CPU_INT	Go
28h	IMASK	Interrupt mask	CPU_INT	Go
30h	RIS	Raw interrupt status	CPU_INT	Go
38h	MIS	Masked interrupt status	CPU_INT	Go
40h	ISET	Interrupt set	CPU_INT	Go
48h	ICLR	Interrupt clear	CPU_INT	Go
58h	IMASK	Interrupt mask	DMA_TRIG_RX	Go
60h	RIS	Raw interrupt status	DMA_TRIG_RX	Go
68h	MIS	Masked interrupt status	DMA_TRIG_RX	Go
70h	ISET	Interrupt set	DMA_TRIG_RX	Go
88h	IMASK	Interrupt mask	DMA_TRIG_TX	Go
90h	RIS	Raw interrupt status	DMA_TRIG_TX	Go
98h	MIS	Masked interrupt status	DMA_TRIG_TX	Go
A0h	ISET	Interrupt set	DMA_TRIG_TX	Go
E4h	INTCTL	Interrupt control register		Go
100h	CTR	I2C Target Control Register		Go
104h	ACKCTL	I2C Target ACK Control		Go
108h	SR	Status Register		Go
10Ch	IFLS	Interrupt FIFO Level Select Register		Go
118h	GFCTL	I2C Glitch Filter Control		Go
120h	TXDATA	I2C TXData		Go
124h	RXDATA	I2C RXData		Go
128h	PECSR	PEC status register		Go
148h	OAR2	Own Address 2		Go
14Ch	OAR	I2C Own Address		Go
150h	TIMEOUT_CNT	I2C Timeout Count Register		Go
154h	TIMEOUT_CTL	I2C Timeout Count Control Register		Go
158h	PECCTL	I2C PEC control register		Go

Complex bit access types are encoded to fit into small table cells. Table 33-51 shows the codes that are used for access types in this section.

Table 33-83. UNICOMMI2CT_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

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Table 33-83. UNICOMMI2CT_REGS Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 CLKDIV Register (Offset = 0h) [Reset = 00000000h]

CLKDIV is shown in Figure 33-52 and described in Table 33-52.

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I2CT Clock Divider. This register is used to specify the module-specific divide ratio of the I2CT functional clock (I2Cclk).

Figure 33-52. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 33-85. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock Division factor 0 : DIV_BY_1 1 : DIV_BY_2 .... 63: DIV_BY_64 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

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2 CLKSEL Register (Offset = 8h) [Reset = 00000000h]

CLKSEL is shown in Figure 33-53 and described in Table 33-53.

Return to the Summary Table.

I2CT Clock Source Selection.

Figure 33-53. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				MCLKDIV2	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 33-87. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	MCLKDIV2	R/W	0h	Enables MCLKDIV2 as the UNICOMM I2CT clock source. 0h = Does not select this clock as a source 1h = Select this clock as a source
2-0	RESERVED	R/W	0h	

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3 PDBGCTL Register (Offset = 18h) [Reset = 00000000h]

PDBGCTL is shown in Figure 33-54 and described in Table 33-54.

Return to the Summary Table.

I2CT Debug Control. This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input.

Figure 33-54. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 33-89. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft Halt Boundary Control. This function is only available, if [FREE] is set to 'STOP' 0h = Not supported 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free Run Control. 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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4 IIDX Register (Offset = 20h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 33-55 and described in Table 33-55.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index.

Figure 33-55. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 33-91. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	I2CT Interrupt Vector Value. This field provides the highest priority interrupt index. A read clears the corresponding interrupt flag in RIS and MIS. 15h-1Fh = Reserved. 00h = No Interrupt Pending. 1h = Receive Done Flag. 2h = Transmit Done Flag. 3h = RX FIFO Trigger Level. 4h = TX FIFO Trigger level 5h = RX FIFO Full Event/Interrupt Pending. 6h = TX FIFO Empty Event/Interrupt Pending. 7h = I2CT TX FIFO Underflow Event. 8h = I2CT RX FIFO Overflow Event. 9h = General Call Event. Ah = START Event. Bh = STOP Event. Ch = PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. Dh = Timeout Counter A Event. Eh = Timeout Counter B Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 10h = DMA DONE on Channel RX. 11h = DMA DONE on Channel TX. 12h = Arbitration Lost.

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5 IMASK Register (Offset = 28h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 33-56 and described in Table 33-56.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-56. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						ARBLOST	DMA_DONE_TX
R/W-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	STOP	START	GENCALL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_OVFL	TX_UNFL	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 33-93. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	0h	
17	ARBLOST	R/W	0h	Arbitration Lost Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
16	DMA_DONE_TX	R/W	0h	I2CT DMA Done on TX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
15	DMA_DONE_RX	R/W	0h	I2CT DMA Done on RX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14	RESERVED	R/W	0h	
13	TIMEOUTB	R/W	0h	Timeout Counter B Interrupt. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
12	TIMEOUTA	R/W	0h	I2CT Timeout Counter A Interrupt Mask. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
11	PEC_RX_ERR	R/W	0h	PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 33-93. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STOP	R/W	0h	I2CT STOP Condition Interrupt Mask. This interrupt is raised when a STOP condition is detected on the bus. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
9	START	R/W	0h	I2CT START Condition Interrupt Mask. This interrupt is raised when a START or repeated START condition is detected on the bus. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
8	GENCALL	R/W	0h	I2CT General Call Interrupt Mask. This interrupt is raised when a general call frame, with an address of 0x00 and R/W bit of '0', is received. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	RX_OVFL	R/W	0h	I2CT RX FIFO Overflow Interrupt Mask. This interrupt is raised when the I2CT receiver tries to receive data, as a result of receiving an address match with a R/W bit of '0', but the I2CT RX FIFO is full. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
6	TX_UNFL	R/W	0h	I2CT TX FIFO Underflow Interrupt Mask. This interrupt is raised when the I2CT transmitter tries to send data, as a result of having received an address match with a R/W bit of '1', but the I2CT TX FIFO is empty. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	TXEMPTY	R/W	0h	I2CT TX FIFO Empty Interrupt Mask. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CT transmitter goes idle. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4	RXFULL	R/W	0h	I2CT RX FIFO Full Interrupt Mask. This interrupt is raised when the RX FIFO is full. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3	TXTRG	R/W	0h	I2CT Transmit Trigger Interrupt Mask. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RXTRG	R/W	0h	I2CT Receive Trigger Interrupt Mask. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	TXDONE	R/W	0h	I2CT Transmit Done Interrupt Mask. This interrupt is raised after each byte is transmitted. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	RXDONE	R/W	0h	I2CT Receive Done Interrupt Mask. This interrupt is raised after each byte is received. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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6 RIS Register (Offset = 30h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 33-57 and described in Table 33-57.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-57. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						ARBLOST	DMA_DONE_TX
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	STOP	START	GENCALL
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RX_OVFL	TX_UNFL	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-95. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17	ARBLOST	R	0h	Arbitration Lost Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur 1h = Interrupt occurred
16	DMA_DONE_TX	R	0h	I2CT DMA Done on TX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	I2CT DMA Done on RX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
14	RESERVED	R	0h	
13	TIMEOUTB	R	0h	Timeout Counter B Interrupt. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur 1h = Interrupt occurred
12	TIMEOUTA	R	0h	I2CT Timeout Counter A Interrupt Raw Status. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Interrupt did not occur 1h = Interrupt occurred
11	PEC_RX_ERR	R	0h	PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur 1h = Interrupt occurred

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Table 33-95. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STOP	R	0h	I2CT STOP Condition Interrupt Raw Status. This interrupt is raised when a STOP condition is detected on the bus. 0h = Interrupt did not occur 1h = Interrupt occurred
9	START	R	0h	I2CT START Condition Interrupt Raw Status. This interrupt is raised when a START or repeated START condition is detected on the bus. 0h = Interrupt did not occur 1h = Interrupt occurred
8	GENCALL	R	0h	I2CT General Call Interrupt Raw Status. This interrupt is raised when a general call frame, with an address of 0x00 and R/W bit of '0', is received. 0h = Interrupt did not occur 1h = Interrupt occurred
7	RX_OVFL	R	0h	I2CT RX FIFO Overflow Interrupt Raw Status. This interrupt is raised when the I2CT receiver tries to receive data, as a result of receiving an address match with a R/W bit of '0', but the I2CT RX FIFO is full. 0h = Interrupt did not occur 1h = Interrupt occurred
6	TX_UNFL	R	0h	I2CT TX FIFO Underflow Interrupt Raw Status. This interrupt is raised when the I2CT transmitter tries to send data, as a result of having received an address match with a R/W bit of '1', but the I2CT TX FIFO is empty. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TXEMPTY	R	0h	I2CT TX FIFO Empty Interrupt Raw Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CT transmitter goes idle. 0h = Interrupt did not occur 1h = Interrupt occurred
4	RXFULL	R	0h	I2CT RX FIFO Full Interrupt Raw Status. This interrupt is raised when the RX FIFO is full. 0h = Interrupt did not occur 1h = Interrupt occurred
3	TXTRG	R	0h	I2CT Transmit Trigger Interrupt Raw Status. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
2	RXTRG	R	0h	I2CT Receive Trigger Interrupt Raw Status. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
1	TXDONE	R	0h	I2CT Transmit Done Interrupt Raw Status. This interrupt is raised after each byte is transmitted. 0h = Interrupt did not occur 1h = Interrupt occurred
0	RXDONE	R	0h	I2CT Receive Done Interrupt Raw Status. This interrupt is raised after each byte is received. 0h = Interrupt did not occur 1h = Interrupt occurred

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7 MIS Register (Offset = 38h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 33-58 and described in Table 33-58.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 33-58. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						ARBLOST	DMA_DONE_TX
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	STOP	START	GENCALL
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RX_OVFL	TX_UNFL	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-97. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17	ARBLOST	R	0h	Arbitration Lost Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
16	DMA_DONE_TX	R	0h	I2CT DMA Done on TX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	I2CT DMA Done on RX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
14	RESERVED	R	0h	
13	TIMEOUTB	R	0h	Timeout Counter B Interrupt. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
12	TIMEOUTA	R	0h	I2CT Timeout Counter A Interrupt Masked Status. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
11	PEC_RX_ERR	R	0h	PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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Table 33-97. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STOP	R	0h	I2CT STOP Condition Interrupt Masked Status. This interrupt is raised when a STOP condition is detected on the bus. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
9	START	R	0h	I2CT START Condition Interrupt Masked Status. This interrupt is raised when a START or repeated START condition is detected on the bus. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
8	GENCALL	R	0h	I2CT General Call Interrupt Masked Status. This interrupt is raised when a general call frame, with an address of 0x00 and R/W bit of '0', is received. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
7	RX_OVFL	R	0h	I2CT RX FIFO Overflow Interrupt Masked Status. This interrupt is raised when the I2CT receiver tries to receive data, as a result of receiving an address match with a R/W bit of '0', but the I2CT RX FIFO is full. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
6	TX_UNFL	R	0h	I2CT TX FIFO Underflow Interrupt Masked Status. This interrupt is raised when the I2CT transmitter tries to send data, as a result of having received an address match with a R/W bit of '1', but the I2CT TX FIFO is empty. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
5	TXEMPTY	R	0h	I2CT TX FIFO Empty Interrupt Masked Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CT transmitter goes idle. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
4	RXFULL	R	0h	I2CT RX FIFO Full Interrupt Masked Status. This interrupt is raised when the RX FIFO is full. 0h = Clear Interrupt Mask 1h = Interrupt occurred
3	TXTRG	R	0h	I2CT Transmit Trigger Interrupt Masked Status. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
2	RXTRG	R	0h	I2CT Receive Trigger Interrupt Masked Status. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
1	TXDONE	R	0h	I2CT Transmit Done Interrupt Masked Status. This interrupt is raised after each byte is transmitted. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
0	RXDONE	R	0h	I2CT Receive Done Interrupt Masked Status. This interrupt is raised after each byte is received. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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8 ISET Register (Offset = 40h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 33-59 and described in Table 33-59.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-59. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED						ARBLOST	DMA_DONE_TX
W-0h						W-0h	W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	STOP	START	GENCALL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RX_OVFL	TX_UNFL	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 33-99. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	W	0h	
17	ARBLOST	W	0h	Arbitration Lost Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Set Interrupt
16	DMA_DONE_TX	W	0h	Set I2CT DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set interrupt
15	DMA_DONE_RX	W	0h	Set I2CT DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set interrupt
14	RESERVED	W	0h	
13	TIMEOUTB	W	0h	Timeout Counter B Interrupt. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Set interrupt
12	TIMEOUTA	W	0h	Set I2CT Timeout Counter A Interrupt. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Writing 0 has no effect 1h = Set Interrupt
11	PEC_RX_ERR	W	0h	PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Set interrupt

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Table 33-99. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STOP	W	0h	Set I2CT STOP Condition Interrupt. This interrupt is raised when a STOP condition is detected on the bus. 0h = Writing 0 has no effect 1h = Set interrupt
9	START	W	0h	Set I2CT START Condition Interrupt. This interrupt is raised when a START or repeated START condition is detected on the bus. 0h = Writing 0 has no effect 1h = Set interrupt
8	GENCALL	W	0h	Set I2CT General Call Interrupt. This interrupt is raised when a general call frame, with an address of 0x00 and R/W bit of '0', is received. 0h = Writing 0 has no effect 1h = Set Interrupt
7	RX_OVFL	W	0h	Set I2CT RX FIFO Overflow Interrupt. This interrupt is raised when the I2CT receiver tries to receive data, as a result of receiving an address match with a R/W bit of '0', but the I2CT RX FIFO is full. 0h = Writing 0 has no effect 1h = Set interrupt
6	TX_UNFL	W	0h	Set I2CT TX FIFO Underflow Interrupt. This interrupt is raised when the I2CT transmitter tries to send data, as a result of having received an address match with a R/W bit of '1', but the I2CT TX FIFO is empty. 0h = Writing 0 has no effect 1h = Set interrupt
5	TXEMPTY	W	0h	Set I2CT TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CT transmitter goes idle. 0h = Writing 0 has no effect 1h = Set Interrupt
4	RXFULL	W	0h	Set I2CT RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Clear Interrupt Mask 1h = Set Interrupt
3	TXTRG	W	0h	Set I2CT Transmit Trigger Interrupt. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt
2	RXTRG	W	0h	Set I2CT Receive Trigger Interrupt. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt
1	TXDONE	W	0h	Set I2CT Transmit Done Interrupt. This interrupt is raised after each byte is transmitted. 0h = Writing 0 has no effect 1h = Set Interrupt
0	RXDONE	W	0h	Set I2CT Receive Done Interrupt. This interrupt is raised after each byte is received. 0h = Writing 0 has no effect 1h = Set Interrupt

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9 ICLR Register (Offset = 48h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 33-60 and described in Table 33-60.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 33-60. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED						ARBLOST	DMA_DONE_TX
W-0h						W-0h	W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED	TIMEOUTB	TIMEOUTA	PEC_RX_ERR	STOP	START	GENCALL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RX_OVFL	TX_UNFL	TXEMPTY	RXFULL	TXTRG	RXTRG	TXDONE	RXDONE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 33-101. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	W	0h	
17	ARBLOST	W	0h	Arbitration Lost Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Set Interrupt
16	DMA_DONE_TX	W	0h	Clear I2CT DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Clear interrupt
15	DMA_DONE_RX	W	0h	Clear I2CT DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the I2CT from a DMA, indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Clear interrupt
14	RESERVED	W	0h	
13	TIMEOUTB	W	0h	Timeout Counter B Interrupt. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Clear Interrupt
12	TIMEOUTA	W	0h	Clear I2CT Timeout Counter A Interrupt. This interrupt is raised when the SCL line is continously low for longer than the clock timeout period programmed by the TIMEOUT_CTL.TCNTLA register. 0h = Writing 0 has no effect 1h = Set Interrupt
11	PEC_RX_ERR	W	0h	PEC Receive Error Event. Interrupt only valid for Advanced UNICOMM I2CT instances. 0h = Writing 0 has no effect 1h = Clear Interrupt

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Table 33-101. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STOP	W	0h	Clear I2CT STOP Condition Interrupt. This interrupt is raised when a STOP condition is detected on the bus. 0h = Writing 0 has no effect 1h = Clear interrupt
9	START	W	0h	Clear I2CT START Condition Interrupt. This interrupt is raised when a START or repeated START condition is detected on the bus. 0h = Writing 0 has no effect 1h = Clear interrupt
8	GENCALL	W	0h	Clear I2CT General Call Interrupt. This interrupt is raised when a general call frame, with an address of 0x00 and R/W bit of '0', is received. 0h = Writing 0 has no effect 1h = Set Interrupt
7	RX_OVFL	W	0h	Clear I2CT RX FIFO Overflow Interrupt. This interrupt is raised when the I2CT receiver tries to receive data, as a result of receiving an address match with a R/W bit of '0', but the I2CT RX FIFO is full. 0h = Writing 0 has no effect 1h = Clear Interrupt
6	TX_UNFL	W	0h	Clear I2CT TX FIFO Underflow Interrupt. This interrupt is raised when the I2CT transmitter tries to send data, as a result of having received an address match with a R/W bit of '1', but the I2CT TX FIFO is empty. 0h = Writing 0 has no effect 1h = Clear Interrupt
5	TXEMPTY	W	0h	Clear I2CT TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the I2CT transmitter goes idle. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	RXFULL	W	0h	Clear I2CT RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Writing 0 has no effect 1h = Clear Interrupt
3	TXTRG	W	0h	Clear I2CT Transmit Trigger Interrupt Mask. This interrupt is raised when the TX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
2	RXTRG	W	0h	Clear I2CT Receive Trigger Interrupt Mask. This interrupt is raised when the RX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
1	TXDONE	W	0h	Clear I2CT Transmit Done Interrupt. This interrupt is raised after each byte is transmitted. 0h = Writing 0 has no effect 1h = Set Interrupt
0	RXDONE	W	0h	Clear I2CT Receive Done Interrupt. This interrupt is raised after each byte is received. 0h = Writing 0 has no effect 1h = Set Interrupt

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10 IMASK Register (Offset = 58h) [Reset = 00000000h] (DMA_TRIG_RX)

IMASK is shown in Figure 33-61 and described in Table 33-61.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-61. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R/W-0h					R/W-0h	R/W-0h	

Table 33-103. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2	RXTRG	R/W	0h	I2CT Receive DMA Trigger Mask. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1-0	RESERVED	R/W	0h	

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11 RIS Register (Offset = 60h) [Reset = 00000000h] (DMA_TRIG_RX)

RIS is shown in Figure 33-62 and described in Table 33-62.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-62. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R-0h					R-0h	R-0h	

Table 33-105. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RXTRG	R	0h	I2CT Receive DMA Trigger Raw Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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12 MIS Register (Offset = 68h) [Reset = 00000000h] (DMA_TRIG_RX)

MIS is shown in Figure 33-63 and described in Table 33-63.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 33-63. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
R-0h					R-0h	R-0h	

Table 33-107. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RXTRG	R	0h	I2CT Receive DMA Trigger Masked Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabledk 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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13 ISET Register (Offset = 70h) [Reset = 00000000h] (DMA_TRIG_RX)

ISET is shown in Figure 33-64 and described in Table 33-64.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-64. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED					RXTRG	RESERVED	
W-0h					W-0h	W-0h	

Table 33-109. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	W	0h	
2	RXTRG	W	0h	Set I2CT Receive DMA Trigger. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt Mask
1-0	RESERVED	W	0h	

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14 IMASK Register (Offset = 88h) [Reset = 00000000h] (DMA_TRIG_TX)

IMASK is shown in Figure 33-65 and described in Table 33-65.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 33-65. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 33-111. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	TXTRG	R/W	0h	I2CT Transmit DMA Trigger Mask. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2-0	RESERVED	R/W	0h	

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15 RIS Register (Offset = 90h) [Reset = 00000000h] (DMA_TRIG_TX)

RIS is shown in Figure 33-66 and described in Table 33-66.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 33-66. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R-0h				R-0h	R-0h		

Table 33-113. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	TXTRG	R	0h	I2CT Transmit DMA Trigger Raw Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2-0	RESERVED	R	0h	

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16 MIS Register (Offset = 98h) [Reset = 00000000h] (DMA_TRIG_TX)

MIS is shown in Figure 33-67 and described in Table 33-67.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 33-67. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
R-0h				R-0h	R-0h		

Table 33-115. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	TXTRG	R	0h	I2CT Transmit DMA Trigger Masked Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2-0	RESERVED	R	0h	

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17 ISET Register (Offset = A0h) [Reset = 00000000h] (DMA_TRIG_TX)

ISET is shown in Figure 33-68 and described in Table 33-68.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 33-68. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				TXTRG	RESERVED		
W-0h				W-0h	W-0h		

Table 33-117. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	TXTRG	W	0h	Set I2CT Transmit DMA Trigger. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2-0	RESERVED	W	0h	

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18 INTCTL Register (Offset = E4h) [Reset = 00000000h]

INTCTL is shown in Figure 33-69 and described in Table 33-69.

Return to the Summary Table.

Interrupt Control Register.

Figure 33-69. INTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTEVAL
W-0h							W-0h

Table 33-119. INTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTEVAL	W	0h	Writing a 1 to this field re-evaluates the interrupt sources. 0h = Writing 0 has no effect 1h = Interrupt Eval

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19 CTR Register (Offset = 100h) [Reset = 00300404h]

CTR is shown in Figure 33-70 and described in Table 33-70.

Return to the Summary Table.

I2CT Control Register.

Figure 33-70. CTR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED		WUEN	CLKSTRETCH	RESERVED			
R/W-0h		R/W-1h	R/W-1h	R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				SUSPEND	RESERVED	EN_DEFDEVADR	EN_ALRESPADR
R/W-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
EN_DEFHOSTADR	RXFULL_ON_REQ	TXWAIT_STALE_TXFIFO	TXTRIG_TXMODE	TXEMPTY_ON_TREQ	RESERVED	GENCALL	ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 33-121. CTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	0h	
21	WUEN	R/W	1h	Target Wakeup Enable. 0h = When 0, the Target is not allowed to clock stretch on START detection 1h = When 1, the Target is allowed to clock stretch on START detection and wait for faster clock to be available. This allows clean wake up support for I2C in low power mode use cases
20	CLKSTRETCH	R/W	1h	Clock Stretching Enable. The I2CT will automatically clock stretch on the SCL line if the TX FIFO is empty in transmit mode or the RX FIFO is full in receive mode. 0h = clock stretching is disabled 1h = clock stretching is enabled
19-12	RESERVED	R/W	0h	
11	SUSPEND	R/W	0h	Suspend External Communication. When this bit is set, I2CT communication on the external bus is suspended after the I2CT FSM goes idle (SR.BUSY reads '0'). 0h = Functional mode resumed 1h = External communication suspended
10	RESERVED	R/W	1h	
9	EN_DEFDEVADR	R/W	0h	Enable Default device address. This field is only available on Advanced I2CT instances. 0h = When this bit is 0, the default device address is not matched. NOTE: it may still be matched if programmed inside OAR/OAR2. 1h = When this bit is 1, default device address of 7'h110_0001 is always matched by the Target address match logic.
8	EN_ALRESPADR	R/W	0h	Enable Alert Response Address. This field is only available on Advanced I2CT instances. 0h = When this bit is 0, the alert response address is not matched. NOTE: it may still be matched if programmed inside OAR/OAR2 1h = When this bit is 1, alert response address of 7'h000_1100 is always matched by the Target address match logic.

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Table 33-121. CTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	EN_DEFHOSTADR	R/W	0h	Enable Default Host Address. This field is only available on Advanced I2CT instances. 0h = When this bit is 0, the default host address is not matched NOTE: it may still be matched if programmed inside OAR/OAR2 1h = When this bit is 1, default host address of 7'h000_1000 is always matched by the Target address match logic.
6	RXFULL_ON_RREQ	R/W	0h	RX Full Interrupt on RREQ. This bit setting determines the behavior of the RXFULL interrupt. 0h = When 0, RIS.RXFULL will be set when only the Target RX FIFO is full. This allows the RXFULL interrupt to be used to indicate that the I2C bus is being clock stretched and that the FW must either read the RX FIFO or ACK/NACK the current RX byte. 1h = When 1, RIS.RXFULL will be set when the I2CT FSM is in the RX_WAIT or RX_ACK_WAIT states which occurs when the I2C transaction is clock stretched because the RX FIFO is full or the ACKOEN has been set and the FSM is waiting for FW to ACK/NACK the current byte.
5	TXWAIT_STALE_TXFIFO	R/W	0h	TX Transfer Wait Configuration. This bit setting determines the behavior of the I2CT transmitter, specifically whether or not the transmitter waits when there is stale data in the TX FIFO. This prevents stale bytes left in the TX FIFO from automatically being sent on the next I2C packet. Note: This setting should only be enabled when TXEMPTY_ON_TREQ is set to prevent the I2CT FSM from waiting for TX FIFO data without an interrupt notification when there is stale FIFO data. 0h = When 0, the TX FIFO empty signal to the Target State Machine indicates that the TX FIFO is empty. 1h = When 1, the TX FIFO empty signal to the Target State Machine will indicate that the TX FIFO is empty or that the TX FIFO data is stale. The TX FIFO data is determined to be stale when there is data in the TX FIFO when the Target State Machine leaves the TXMODE as defined in the SR register. A stale TX FIFO occurs if a Stop or timeout condition occurs when there are bytes left in the TX FIFO.
4	TXTRIG_TXMODE	R/W	0h	TX Trigger when I2CT FSM is in TX Mode. This bit setting determines the behavior of the TXTRG DMA trigger. 0h = No special behavior 1h = When 1, RIS.TXTRG is set when the I2CT TX FIFO has reached the trigger level AND the I2CT FSM is in the TX mode, as defined in the SR register. When cleared, RIS.TXTRG is set when the I2CT TX FIFO is at or above the trigger level. This setting can be used to hold off the TX DMA until a transaction starts. This allows the DMA to be configured when the I2CT is idle but have it wait until the transaction starts to load the I2CT TX FIFO, so it can load from a memory buffer that might be changing over time.
3	TXEMPTY_ON_TREQ	R/W	0h	TX Empty Interrupt on TREQ. This bit setting determines the behavior of the TXEMPTY interrupt. 0h = When 0, RIS.TXEMPTY will be set when only the I2CT TX FIFO is empty. This allows the TXEMPTY interrupt to be used to indicate that the I2C bus is being clock stretched and that I2CT TX data is required. 1h = When 1, RIS.TXEMPTY will be set when the I2CT FSM is in the TX_WAIT state which occurs when the TX FIFO is empty AND the I2C transaction is being clock stretched waiting for data to be written to the TX FIFO.
2	RESERVED	R/W	1h	
1	GENCALL	R/W	0h	General Call/Response Enable. 0b = Do not respond to a general call 1b = Respond to a general call 0h = Do not respond to a general call 1h = Respond to a general call

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Table 33-121. CTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ENABLE	R/W	0h	I2CT Enable. Setting this bit enables the module. 0h = Disables module operation. 1h = Enables module operation.

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20 ACKCTL Register (Offset = 104h) [Reset = 00000000h]

ACKCTL is shown in Figure 33-71 and described in Table 33-71.

Return to the Summary Table.

I2CT Acknowledge Control Register. This register enables the I2CT to Not Acknowledge (NACK) for invalid data/commands or Acknowledge (ACK) for valid data/commands. The I2C SCL is pulled low after the last data bit until this register is written.

Figure 33-71. ACKCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED			ACKOEN_ON_PECDONE	ACKOEN_ON_PECNEXT	ACKOEN_ON_START	ACKOVAL	ACKOEN
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 33-123. ACKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	0h	
4	ACKOEN_ON_PECDONE	R/W	0h	Acknowledge Override Enable on PEC Done. When set, this bit will automatically turn on target acknowledge enable field following the ACK/NACK of the received PEC byte. Status bit ACKOEN will reflect a value of '1' when automatic override enable is used. This field is only available on Advanced I2CT instances. 0h = No special behavior 1h = When set this bit will automatically turn on the Target ACKOEN field following the ACK/NACK of the received PEC byte.
3	ACKOEN_ON_PECNEXT	R/W	0h	Acknowledge Override Enable on PEC Next. When set, this bit will automatically turn on the I2CT acknowledge override following a ACK/NACK of the byte received just prior to the PEC byte. However, setting ACKCTL.ACKOEN bit will not automatically be ACKed/NACKed by the FSM and firmware must perform this function by writing the I2CT ACKCTL register. Status bit ACKOEN will reflect a value of '1' when automatic override enable is used. This field is only available on Advanced I2CT instances. 0h = No special behavior 1h = When set this bit will automatically turn on the Target ACKOEN field following the ACK/NACK of the byte received just prior to the PEC byte. Note that when ACKOEN is set the PEC byte will not automatically be ACKed/NACKed by the State Machine and FW must perform this function by writing ACKCTL.
2	ACKOEN_ON_START	R/W	0h	Acknowledge Override Enable on START. When set this bit will automatically enable target override acknowledge following a Start Condition. Status bit ACKOEN will reflect a value of '1' when automatic override enable is used. This field is only available on Advanced I2CT instances. 0h = No special behavior 1h = When set this bit will automatically turn on the Target ACKOEN field following a Start Condition.

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Table 33-123. ACKCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ACKOVAL	R/W	0h	ACK Override Value. Note: Override control is not applicable to Address frame. Bytes following address frame can be acknowledged using ACKOVAL. 0h = An ACK is sent indicating valid data or command. 1h = A NACK is sent indicating invalid data or command.
0	ACKOEN	R/W	0h	I2CT ACK Override Enable. Determines if the I2CT clock stretches and waits for the application to manually ACK/NACK each received byte using the ACKCTL.ACKOVAL bit, or if the ACK/NACK is done automatically. Read SR.ACKOEN to check current status of this bit. 0h = A response in not provided. 1h = An ACK or NACK is sent according to the value written to the ACKOVAL bit.

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21 SR Register (Offset = 108h) [Reset = 00000000h]

SR is shown in Figure 33-72 and described in Table 33-72.

Return to the Summary Table.

I2CT Status Register. This status register indicates the current state of the I2CT.

Figure 33-72. SR Register

31	30	29	28	27	26	25	24
RESERVED						ADDRMATCH	
R-0h						R-0h	
23	22	21	20	19	18	17	16
ADDRMATCH							
R-0h							
15	14	13	12	11	10	9	8
ACKOEN	TXFF	TXFE	RXFF	RXFE	TXCLR	RXCLR	STALE_TXFIFO
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TXMODE	BUSBSY	QCMDRW	QCMDST	OAR2SEL	RXMODE	TREQ	RREQ
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 33-125. SR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	
25-16	ADDRMATCH	R	0h	Address Match Status. Indicates the address for which Target address match happened. 0h = Minimum Value 3FFh = Maximum Value
15	ACKOEN	R	0h	ACK Override Enable Status. 0h = ACK override is disabled 1h = ACK override was enabled in design
14	TXFF	R	0h	TX FIFO Full Status. 0h = Transmit FIFO is not full 1h = Transmit FIFO is full
13	TXFE	R	1h	TX FIFO Empty Status. 0h = TX FIFO is not empty. 1h = TX FIFO is empty
12	RXFF	R	0h	RX FIFO Full Status. 0h = RX FIFO is not full 1h = RX FIFO is full
11	RXFE	R	1h	RX FIFO Empty Status. 0h = RX FIFO is not empty. 1h = RX FIFO is empty
10	TXCLR	R	0h	TX FIFO Clear Status. 0h = FIFO is not cleared 1h = FIFO clear is complete
9	RXCLR	R	0h	RX FIFO Clear Status. 0h = FIFO is not cleared 1h = FIFO clear is complete
8	STALE_TXFIFO	R	0h	Stale TX FIFO Status. 0h = TX FIFO is not stale 1h = The TX FIFO is stale. This occurs when the TX FIFO was not emptied during the previous I2C transaction.

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Table 33-125. SR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TXMODE	R	0h	I2CT FSM is in TX Mode. 0h = State Machine is not in TX_DATA, TX_WAIT, TX_ACK or ADDR_ACK state with the bus direction set to read. 1h = State Machine is in TX_DATA, TX_WAIT, TX_ACK or ADDR_ACK state with the bus direction set to read.
6	BUSBSY	R	0h	I2C Bus Busy Status. 0h = The I2C Bus is not busy 1h = The I2C Bus is busy. This is cleared on a timeout.
5	QCMDRW	R	0h	Quick Command Read / Write Status. This bit only has meaning when the QCMDST bit is set. Value Description: 0: Quick command was a write 1: Quick command was a read 0h = Quick command was a write 1h = Quick command was a read
4	QCMDST	R	0h	Quick Command Status. Value Description: 0: The last transaction was a normal transaction or a transaction has not occurred. 1: The last transaction was a Quick Command transaction 0h = The last transaction was a normal transaction or a transaction has not occurred. 1h = The last transaction was a Quick Command transaction.
3	OAR2SEL	R	0h	OAR2 Address Matched Status. This bit gets reevaluated after every address comparison. This field is only available on Advanced I2CT instances. 0h = Either the OAR2 address is not matched or the match is in legacy mode. 1h = OAR2 address matched and ACKed by the Target.
2	RXMODE	R	0h	I2CT FSM is in RX Mode. 0h = The Target State Machine is not in the RX_DATA, RX_ACK, RX_WAIT, RX_ACK_WAIT or ADDR_ACK state with the bus direction set to write. 1h = The Target State Machine is in the RX_DATA, RX_ACK, RX_WAIT, RX_ACK_WAIT or ADDR_ACK state with the bus direction set to write.
1	TREQ	R	0h	Transmit Request Status. 0h = No outstanding transmit request. 1h = I2C Target is addressed as a transmitter and is using clock stretching to delay the Controller until data has been written to the TXDATA FIFO (TX FIFO is empty).
0	RREQ	R	0h	Receive Request Status. 0h = No outstanding receive data. 1h = Module has outstanding receive data and is using clock stretching to delay the Controller until the data has been read from the RXDATA FIFO (RX FIFO is full).

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22 IFLS Register (Offset = 10Ch) [Reset = 00000022h]

IFLS is shown in Figure 33-73 and described in Table 33-73.

Return to the Summary Table.

I2CT Interrupt FIFO Level Select Register. The IFLS register is the interrupt FIFO level select register. You can use this register to define the levels at which the TX, RX and timeout interrupt flags are triggered. The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered when the RX FIFO is filled with two or more characters. Out of reset, the TXIFLSEL and RXIFLSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Figure 33-73. IFLS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RXCLR	RXIFLSEL			TXCLR	TXIFLSEL		
R/W-0h	R/W-2h			R/W-0h	R/W-2h		

Table 33-127. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	RXCLR	R/W	0h	RX FIFO Clear. Setting this bit will clear the RX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
6-4	RXIFLSEL	R/W	2h	RX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Opposite of empty 5h = RX FIFO is full 6h = RX_FIFO >= (MAX_FIFO_LEN -1) 7h = RX_FIFO <= 1
3	TXCLR	R/W	0h	TX FIFO Clear. Setting this bit will clear the TX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
2-0	TXIFLSEL	R/W	2h	TX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Opposite of full 5h = TX FIFO is empty 6h = TX FIFO <= 1 7h = TX_FIFO >= (MAX_FIFO_LEN -1)

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23 GFCTL Register (Offset = 118h) [Reset = 00000000h]

GFCTL is shown in Figure 33-74 and described in Table 33-74.

Return to the Summary Table.

I2CT Glitch Filter Control Register. This register controls the glitch filter on the SCL and SDA lines

Figure 33-74. GFCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							AGFEN
R/W-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						DGFSEL	
R/W-0h						R/W-0h	

Table 33-129. GFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	0h	
8	AGFEN	R/W	0h	Analog Glitch Suppression Enable. 0h = Analog Glitch Filter disable 1h = Analog Glitch Filter enable
7-3	RESERVED	R/W	0h	
2-0	DGFSEL	R/W	0h	Digital Glitch Suppression Pulse Width. The digital glitch filter is only available on Basic I2CT instances. This field controls the pulse width select for glitch suppression on the SCL and SDA lines. The following glitch suppression values are in terms of I2Cclk cycles. 0h = Bypass 1h = 1 clock 2h = 2 clocks 3h = 3 clocks 4h = 4 clocks 5h = 8 clocks 6h = 16 clocks 7h = 31 clocks

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24 TXDATA Register (Offset = 120h) [Reset = 00000000h]

TXDATA is shown in Figure 33-75 and described in Table 33-75.

Return to the Summary Table.

I2CT Transmit Data Register. This register is the transmit data register (the interface to the FIFOs). For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the TX FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the TX FIFO).

Figure 33-75. TXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
W-0h																								W-0h							

Table 33-131. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	W	0h	
7-0	DATA	W	0h	Transmit Data. This byte contains the data to be transferred during the next transaction. 0h = Smallest value FFh = Highest possible value

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25 RXDATA Register (Offset = 124h) [Reset = 00000000h]

RXDATA is shown in Figure 33-76 and described in Table 33-76.

Return to the Summary Table.

I2CT Receive Data Register. This field contains the current byte being read in the RX FIFO stack. If the FIFO is disabled, the data byte and status are stored in the receiving holding register (the bottom word of the RX FIFO). The received data can be retrieved by reading this register.

Figure 33-76. RXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								R-0h							

Table 33-133. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	DATA	R	0h	Received Data. This field contains the last received data. 0h = Smallest value FFh = Highest possible value

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26 PECSR Register (Offset = 128h) [Reset = 00000000h]

PECSR is shown in Figure 33-77 and described in Table 33-77.

Return to the Summary Table.

PEC Status Register. This register is only available on Advanced I2CT instances.

Figure 33-77. PECSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						PECSTS_ERROR	PECSTS_CHECK
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							PECBYTECNT
R-0h							R-0h
7	6	5	4	3	2	1	0
PECBYTECNT							
R-0h							

Table 33-135. PECSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	
17	PECSTS_ERROR	R	0h	PEC Status Error. This status bit indicates if a PEC check error occurred in the transaction that occurred before the last STOP. This bit is cleared automatically by hardware when the next STOP observed on the line. 0h = Indicates PEC check error did not occur in the transaction that occurred before the last Stop 1h = Indicates PEC check error occurred in the transaction that occurred before the last Stop
16	PECSTS_CHECK	R	0h	PEC Status Check. This status bit indicates if the PEC was checked in the transaction that occurred before the last STOP. This bit is cleared automatically by hardware when the next STOP observed on the line. 0h = Indicates PEC was not checked in the transaction that occurred before the last Stop 1h = Indicates PEC was checked in the transaction that occurred before the last Stop
15-9	RESERVED	R	0h	
8-0	PECBYTECNT	R	0h	PEC Byte Count. This is the current PEC Byte Count of the I2CT FSM. 0h = Minimum Value 1FFh = Maximum Value

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27 OAR2 Register (Offset = 148h) [Reset = 00000000h]

OAR2 is shown in Figure 33-78 and described in Table 33-78.

Return to the Summary Table.

I2CT Own Address 2 Register. This register consists of seven address bits that identify the alternate address for the I2C device on the I2C bus. This register is only available on Advanced I2CT instances.

Figure 33-78. OAR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED	OAR2_MASK						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
OAR2EN	OAR2						
R/W-0h	R/W-0h						

Table 33-137. OAR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	0h	
22-16	OAR2_MASK	R/W	0h	Own Address 2 Mask. This field specifies bits A6 through A0 of the Target address. The bits with value '1' in OAR2.OAR2_MASK field will make the corresponding incoming address bits to match by default regardless of the value inside OAR2.OAR2 i.e. corresponding OAR2.OAR2 bit is a don't care. 0h = Minimum Value 7Fh = Maximum Value
15-8	RESERVED	R/W	0h	
7	OAR2EN	R/W	0h	Own Address 2 Enable. 0h = The alternate address is disabled. 1h = Enables the use of the alternate address in the OAR2 field.
6-0	OAR2	R/W	0h	Own Address 2. This field specifies the alternate OAR2 address. 0h = Smallest value 7Fh = Highest possible value

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28 OAR Register (Offset = 14Ch) [Reset = 00004000h]

OAR is shown in Figure 33-79 and described in Table 33-79.

Return to the Summary Table.

I2CT Own Address Register. This register consists of seven address bits that identify the I2C device on the I2C bus.

Figure 33-79. OAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
MODE	OAREN	RESERVED				OAR	
R/W-0h	R/W-1h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
OAR							
R/W-0h							

Table 33-139. OAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	MODE	R/W	0h	Addressing Mode Select. This bit selects the addressing mode to be used. When 0, 7-bit addressing is used. When 1, 10-bit addressing is used. 0h = Enable 7-bit addressing 1h = Enable 10-bit addressing
14	OAREN	R/W	1h	Own Address Enable. 0h = Disable OAR address 1h = Enable OAR address
13-10	RESERVED	R/W	0h	
9-0	OAR	R/W	0h	Own Address. This field specifies bits A9 through A0 of the Target address. In 7-bit addressing mode as selected by OAR.MODE bit, the top 3 bits are don't care 0h = Smallest value 3FFh = Highest possible value

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29 TIMEOUT_CNT Register (Offset = 150h) [Reset = 00020002h]

TIMEOUT_CNT is shown in Figure 33-80 and described in Table 33-80.

Return to the Summary Table.

I2CT Timeout Counter. This register contains the upper 8 bits of a 12-bit current counter values for Timeout Counter A and B. The lower four bits of the counter are not user visible and are always 0h.

Figure 33-80. TIMEOUT_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TCNTB								RESERVED								TCNTA							
R-0h								R-2h								R-0h								R-2h							

Table 33-141. TIMEOUT_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	
23-16	TCNTB	R	2h	Timeout Counter B Current Count. This field contains the upper 8 bits of a 12-bit current counter for timeout counter B. This field is only available on Advanced I2CT instances. 0h = Smallest Value FFh = Highest possible value
15-8	RESERVED	R	0h	
7-0	TCNTA	R	2h	Timeout Count A Current Count: This field contains the upper 8 bits of a 12-bit current counter for timeout counter A. Each count is equal to 520 times the timeout period of I2Cclk. For example, with 8MHz I2Cclk and a 100KHz operating I2C clock, one timeout period will be equal to (1 / 8MHz) * 520 or 65 us. 0h = Smallest Value FFh = Highest possible value

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30 TIMEOUT_CTL Register (Offset = 154h) [Reset = 00020002h]

TIMEOUT_CTL is shown in Figure 33-81 and described in Table 33-81.

Return to the Summary Table.

I2CT Timeout Control. This register contains controls for Timeout Counters A and B.

Figure 33-81. TIMEOUT_CTL Register

31	30	29	28	27	26	25	24
TCNTBEN	RESERVED						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
TCNTLB							
R/W-2h							
15	14	13	12	11	10	9	8
TCNTAEN	RESERVED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
TCNTLA							
R/W-2h							

Table 33-143. TIMEOUT_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCNTBEN	R/W	0h	Timeout Counter B Enable. This field is only available on Advanced I2CT instances. 0h = Disable Timeout Counter B 1h = Enable Timeout Counter B
30-24	RESERVED	R/W	0h	
23-16	TCNTLB	R/W	2h	Timeout Count B Load: Counter B is used for SCL High Detection. Each count is equal to 1* clock period. For example, with 10MHz I2Cclk frequency, one timeout period will be equal to 1*100ns. 0h = Smallest possible value FFh = Highest possible value
15	TCNTAEN	R/W	0h	Timeout Counter A Enable. 0h = Disable Timeout Counter B 1h = Enable Timeout Counter B
14-8	RESERVED	R/W	0h	
7-0	TCNTLA	R/W	2h	Timeout Counter A Load Value. Counter A is used for SCL low detection. This field contains the upper 8 bits of a 12-bit pre-load value for the Timeout A count. NOTE: The value of CNTLA must be greater than 1h. Each count is equal to 520 times the timeout period of functional clock. For example, with 8MHz functional clock and a 100KHz operating I2C clock, one timeout period will be equal to (1 / 8MHz) * 520 or 65 us. 0h = Smallest Value FFh = Highest possible value

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31 PECCTL Register (Offset = 158h) [Reset = 00000000h]

PECCTL is shown in Figure 33-82 and described in Table 33-82.

Return to the Summary Table.

PEC Control Register. This register is only available on Advanced I2CT instances.

Figure 33-82. PECCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED			PECEN	RESERVED			PECCNT
R/W-0h			R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
PECCNT							
R/W-0h							

Table 33-145. PECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	0h	
12	PECEN	R/W	0h	PEC Enable. This bit enables the SMB Packet Error Checking (PEC). When enabled, the PEC is calculated on all bits except the START, STOP, ACK and NACK. The PEC internal LSFR and the PECCNT are set to 0 when the I2CT FSM is in the IDLE state, which occurs following a STOP or timeout condition. The PECCNT is also set to 0 after the PEC byte is transmitted or received. Note that the NACK is automatically sent following a PEC byte that results in a PEC error. The PEC polynomial is x^8 + x^2 + x^1 + 1. 0h = PEC transmission and check is disabled 1h = PEC transmission and check is enabled
11-9	RESERVED	R/W	0h	
8-0	PECCNT	R/W	0h	PEC Counter. When this field is non zero, the number of I2C data bytes are counted. When the byte count = PECCNT and the I2CT FSM is transmitting, the contents of the internal LSFR is loaded into the shift register instead of the byte received from the TX FIFO. When the FSM is receiving, after the last bit of this byte is received into the LSFR and the FSM checks that it is non-zero, a PEC RX Error interrupt is generated. The I2C packet must be padded to include the PEC byte for both transmit and receive. In transmit mode, the FIFO must be loaded with a dummy PEC byte. In receive mode, the PEC byte will be passed to the RX FIFO. In the normal use case, FW would set PECEN=1 and PECCNT=0 and use the ACKOEN until the remaining SMBus packet length is known. FW would then set the PECCNT to the remaining packet length (including the PEC bye). FW would then configure the DMA to allow the packet to complete unassisted and exit the NACK mode. Note that when the byte count = PECCNT, the byte count is reset to 0 and multiple PEC calculation can automatically occur within a single I2C transaction. 0h = Minimum Value 1FFh = Maximum Value

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Chapter 34

Serial Peripheral Interface (SPI)

The functionality of a UNICOMM module when configured to operate as a SPI is described in this section. The protocol mode of a given UNICOMM instance is decided by the programmed SELECT field of the IPMODE register. If a UNICOMM instance is configured for another peripheral mode, the SPI functionality on that UNICOMM instance is disabled and unusable.

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34.2 Peripheral Functional Description 2578
34.3 SPI Interrupts & Triggers 2588
34.4 UNICOMM-SPI Registers 2588

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34.1 Overview

The UNICOMM-SPI module provides a standardized serial interface for transferring data between AM13E230x devices and external devices (such as Sensors, Memory, ADCs, DACs, or other MCUs) using the SPI protocol.

34.1.1 Purpose of the Peripheral

The SPI module acts as a controller or peripheral interface for synchronous serial communication with peripheral devices and other controllers. The transmit and receive paths are buffered with internal, independent FIFO memories allowing up to 16 entries with 16-bit width. A DMA interface is also provided to allow the data exchange with the transmit and receive FIFOs.

34.1.2 Features

The UNICOMM-SPI peripheral mode of the UNICOMM module includes the following features:

- Configurable as a controller or a peripheral
- Programmable clock bit rate and prescaler
- Separate transmit (TX) and receive (RX) buffers/first-in first-out buffers (FIFOs)
- Programmable 4 -16 bit data frame size (Controller Mode)
- Programmable 7-16 bit data frame size (Peripheral Mode)
- One chip select (CS) pin
- Direct Memory Access (DMA) support
- Available Interrupts:
  - Transmit (TX) and receive (RX) FIFO levels and empty/full conditions
  - Parity and overrun error
  - Idle condition
  - Receive positive and negative edge conditions
  - DMA done conditions
- Programmable SPI mode support for:
  - Motorola SPI frame format: four phase + polarity combinations
    - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
    - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
    - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
    - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal
  - Texas Instruments frame format
- Single-bit parity is supported in both transmit and receive paths
- Internal loopback test mode

To support SPI protocol, a UNICOMM module must be configured as a SPI in the UNICOMM top level IPMODE register.

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34.1.3 Functional Block Diagram

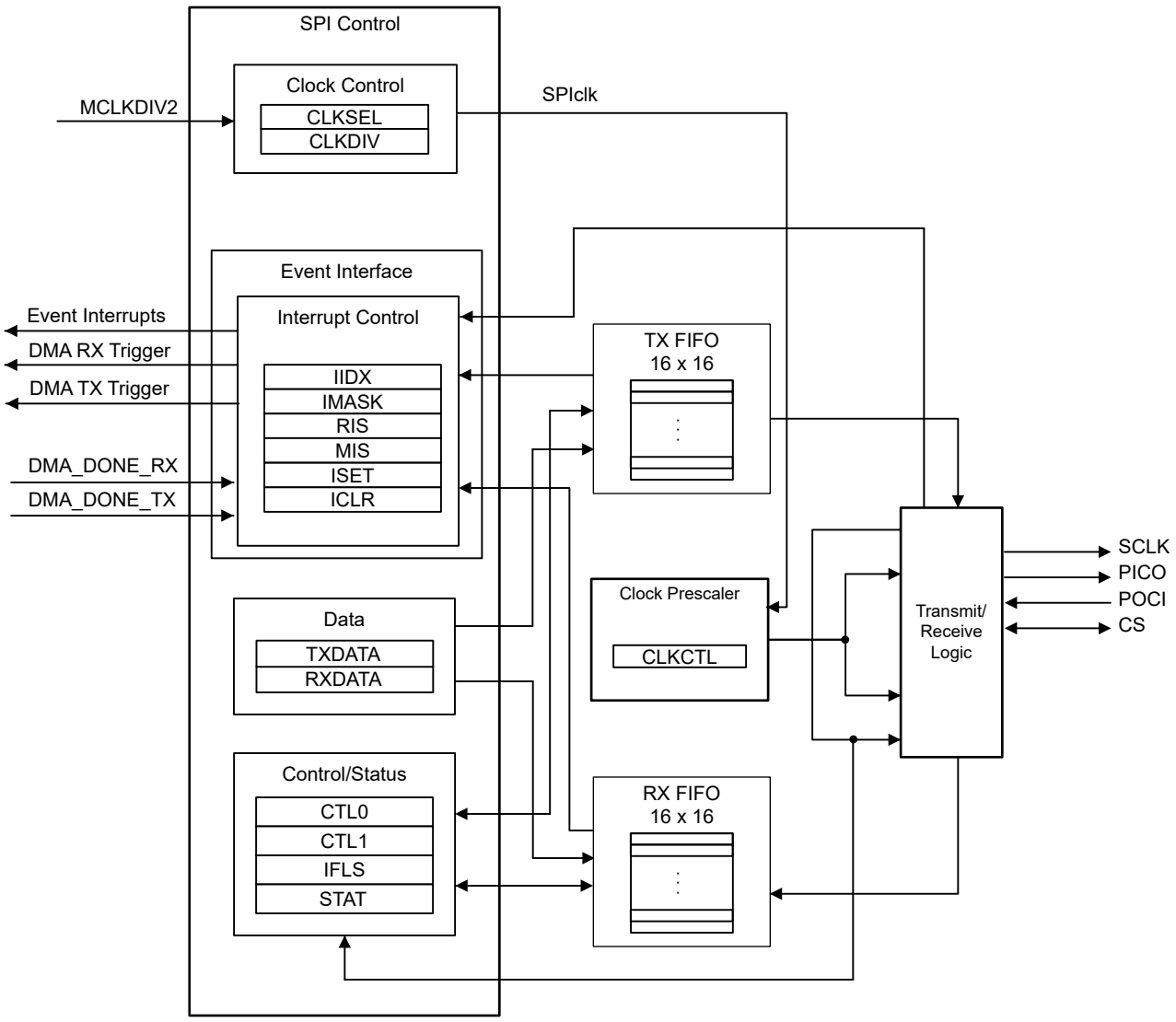


Figure 34-1. SPI Functional Block Diagram

34.2 Peripheral Functional Description

34.2.1 Clock Control

The SPI functional clock SPIclk is selected and divided from the clock sourced to this module.

- Use the CLKSEL register to enable MCLKDIV2 as the functional clock source for the UNICOMM SPI module.
- Use CLKDIV register to select the divide ratio of the SPI functional clock. Options are from divide by 1 to 8.

The SPI module must be enabled before being configured for use by using the ENABLE bit in the UNICOMM_REGS PWREN register. When the SPI is being setup or the configuration is being changed, the ENABLE bit needs to be cleared to avoid unpredictable behavior during the updates or the first data received or transmitted following an update.

The maximum SPI frequency supported with controller and peripheral mode depends on the device clock option and IO option. Please refer to specific device data sheet spec for more information.

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34.2.2 General Architecture

In SPI communication, the controller transfers data by toggling the SPICLK signal. For both the peripheral and the controller, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. As a result, both devices send and receive data simultaneously. The application determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Controller sends data; peripheral sends dummy data.
- Controller sends data; peripheral sends data.
- Controller sends dummy data; peripheral sends data.

The controller can initiate data transfer at any time because the controller controls the SPICLK signal. The application, however, determines how the controller detects when the peripheral is ready to broadcast data. The UNICOMM-SPI operates in either controller or peripheral mode. The CTL1.CP bit selects the operating mode and the source of the SPICLK signal.

34.2.2.1 Chip Select Control

UNICOMM-SPI can be configured to be controller mode by setting the CTL1.CP bit to 1, or in peripheral mode by clearing the CTL1.CP bit. The chip select signal needs to be provided by the controller in four-wire mode and the chip select polarity can be inverted by configuring the PINCM.CSx.INV register. In UNICOMM-SPI peripheral mode, the clock is provided by the controller and used by the peripheral to capture the data. The peripheral has the option to operate in 3-wire or 4-wire mode by configuring the CTL0.FRF field. 4-wire mode only accepts data transfers if the CS is activated.

The CTL0.CSCLR register field determines the behavior of the internal bit counter of the UNICOMM-SPI in peripheral mode when the controller de-asserts the CS signal. This bit is only relevant when the UNICOMM-SPI is configured as a SPI peripheral (CTL1.CP = 0).

- CTL0.CSCLR = 0: The transmit/receive bit counter state is retained when the CS signal disables the peripheral.
- CTL0.CSCLR = 1: The transmit/receive bit counter is cleared when the CS signal disables the peripheral.

When using the Motorola 4-wire mode as a UNICOMM-SPI peripheral with the CTL0.CSCLR = 1 setting, the SPI controller device must follow the below constraints for proper communication. Following these constraints helps the UNICOMM-SPI peripheral to synchronize to the controller during initialization or in the case of a disturbance or glitch on the clock line.

- The CS disable period must be longer than 2 SPIclk cycles before the CS pin is re-asserted
- The CS lead time (CS active to the first bit clock edge) must be at least 2 SPIclk clock cycles

34.2.2.2 Data Format

The control bit CTL1.MSB defines the direction of the data input and output with the most-significant-bit (MSB) or least-significant-bit (LSB) first. If the parity is enabled, the parity bit is always received last.

The CTL0.DSS control register bits determine the bit length per transfer. This can be configured to be between 4-16 bits for UNICOMM-SPI Controller mode and 7-16 bits for UNICOMM-SPI Peripheral mode.

A transfer is triggered by writing to the TXDATA register. The data write must have at least the number of bits of the transfer. For example, if only a byte is written to TXDATA, but the length of the transfer is > 8, the missing bits are filled with 0s. On the receive path, the received data is moved to the RX FIFO after the number of bits defined by the CTL0.DSS register have been received.

The RXDATA and TXDATA registers must be accessed with at least the bits covering one transfer.

- 4-8 bits : byte access (Peripheral mode: 7-8 Bits)
- 9-16 bits : 16 bit access

The clock polarity register field (CTL0.SPO) controls the clock polarity of SPICLK when data is not being transferred and is only valid in the Motorola SPI frame mode.

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- 0h = Peripheral produces a steady state LOW value on the SPICLK pin when data is not being transferred.
- 1h = Peripheral produces a steady state HIGH value on the SPICLK pin when data is not being transferred.

The clock phase register field (CTL0.SPH) selects the clock edge that captures data and allows the module to change state. This setting has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture edge. Please refer to Motorola SPI frame mode section to check the diagrams.

- 0h = Data is captured on the first SPICLK edge transition.
- 1h = Data is captured on the second SPICLK edge transition.

The UNICOMM-SPI can be configured to work in peripheral mode with CTL1.CP bit = 0. In peripheral mode, the clock is provided by the controller and available for the peripheral on the CLK pins which needs to be configured for input. The Clock Select and divider control bits are not used. The CS input signal is used to select/enable the data receive path of the peripheral in 4 wire mode.

The SPI can be configured to work as Controller with CTL1.CP bit = 1. In controller mode, the SPICLK signal needs to be generated by selecting the available clock sources with the clock select bits. The SPI controller also needs to control the CS signal depending on the selected protocol.

Parity checking is a feature in UNICOMM-SPI used to improve the robustness of the communication. The parity transmit enable (CTL1.PTEN) and parity receive enable (CTL1.PREN) register bits add a parity bit to the UNICOMM-SPI transmission or reception respectively.When the CTL1.PTEN bit is set, each data transfer includes an additional parity bit calculated by the previously transmitted data bits. If CTL1.PTEN is cleared, there is no additional bit added to the transmission. When the CTL1.PREN bit is set, the last received bit is used as parity to evaluate the integrity of the previous bits that were received. The CTL1.PES bit selects whether the parity mode is even or odd for both transmit and receive parity operations. When a parity error is detected on a received character, the interrupt flag RIS.PER is set to mark the data as invalid.

34.2.2.3 Delayed Data Sampling

In some circumstances, the data inputted to a UNICOMM-SPI controller on the POCI pin has some delay due to runtime conditions. At high SPICLK speeds, the setup and hold requirements of the UNICOMM-SPI become very strict. As a result, when a data frame is delayed on the POCI pin, the UNICOMM-SPI controller can incorrectly sample the previous data value at the SPICLK sampling edge.

To compensate for this, the delayed sampling feature can be enabled with the CLKCTL.DSAMPLE bits. Delayed sampling is only available when the UNICOMM-SPI is configured for controller mode. The delay configuration of CLKCTL.DSAMPLE is adjusted in steps of SPIclk clock cycles. The maximum allowed delay must not exceed the length of one data frame. If CLKCTL.DSAMPLE is set to zero, delayed sampling is not applied.

See the device data sheet for the minimum and maximum SPICLK speeds with and without the delay sampling feature enabled.

34.2.2.4 Clock Generation

The SPI includes a programmable bit rate clock divider and prescaler to generate the serial output clock (SCLK).

The module supports bit rates up to the clock source (MCLKDIV2) divided by 2.

SPIclk is the output after clock division is performed according to ratio selected by the CLKDIV register.

SPIclk = MCLKDIV2 Frequency / (1 + CLKDIV)

SPI Sampling Clock (SCLK) is the output after dividing the SPIclk by the prescalar value. SCLK = SPIclk / ((1 + SCR)*2)

Note

The input clock frequency must be at least 2 times the desired SPIclk frequency when using the minimum CLKDIV value.

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34.2.2.5 SPI FIFO Operation

See Section 31.2.2 first for an overview of the FIFO operation and status flags available to every UNICOMM instance. The below details FIFO considerations specific to the SPI module.

Transmit FIFO

The CPU or DMA writes data to the TX FIFO by writing the TXDATA register. Data is stored in the FIFO until read out by the SPI transmitter logic. When configured as a controller or a peripheral, parallel data is written into the TX FIFO before serial conversion and transmission to the attached peripheral or controller, respectively, through the PICO or POCI pin.

In peripheral mode, the SPI transmits data each time the controller initiates a transaction. If the TX FIFO is empty and the controller initiates a transfer, the peripheral transmits the most-recent value written to the transmit FIFO. User software is responsible to make valid data available to the FIFO as needed. The SPI can be configured to generate an interrupt or a DMA request when the FIFO reaches a threshold level empty. There is also an interrupt flag called TXFIFO_UNF that indicates if a TX FIFO underflow condition has occurred in when the UNICOMM-SPI is in peripheral mode.

Receive FIFO

Received data from the serial interface is stored in the RX FIFO until read out by the CPU or DMA, which accesses the RX FIFO by reading the RXDATA register.

When configured as a controller or peripheral, serial data is received through the POCI or PICO pin. If the RX FIFO is full and new data is written into the FIFO without reading data the RXFIFO overflow event is set. The receive FIFO has a RXFULL interrupt to indicate a FIFO full condition.

34.2.2.6 DMA Operation

The UNICOMM-SPI provides an interface to the DMA module, with separate transmit and receive lines. The DMA operation of the SPI is enabled through the SPI DMA Event and DMA module registers. When DMA operation is enabled, the SPI asserts a DMA request on the receive or transmit channel when the associated FIFO can transfer data. The DMA transfer requests are handled automatically by the DMA controller based on the DMA channel configurations (burst size, transfer size, source address, etc).

For more information about the DMA module and DMA-specific configurations, see Direct Memory Access (DMA).

- For the receive channel, a DMA transfer request is asserted when the RX FIFO contains at least the FIFO trigger level configured by the RXIFLSEL bit in the IFLS register.
- For the transmit channel, a DMA transfer request is asserted whenever the TX FIFO contains fewer characters than the FIFO trigger level configured using the TXIFLSEL bit in the IFLS register.

34.2.3 Internal Loopback Operation

The SPI module can be placed into an internal loopback mode for diagnostic or debug work by setting the LBM bit in the CTL1 register. In loopback mode, the data from the TX FIFO can serially transmitted into the RX FIFO. Thedata from the RX FIFO can be read to check whether correct transmission has occurred or not. The external toggling of the IOs has no effect when the module is set in the internal loopback mode.

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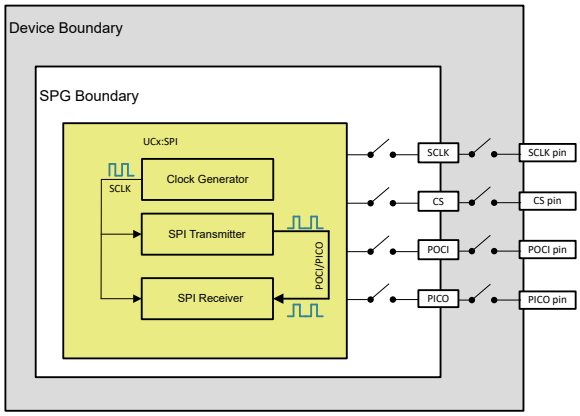


Figure 34-2. SPI Internal Loopback

34.2.4 Protocol Descriptions

The protocol format mode can be selected by using CTL0.FRF register. The supported options include Motorola 3-wire, Motorola 4-wire, and Texas Instruments Synchronous.

34.2.4.1 Motorola SPI Frame Format

The Motorola SPI interface is a 4-wire interface where the CS signal behaves as a peripheral select. In the 3-wire mode, the CS signal is not required and the module behaves as if always selected. The main feature of the Motorola SPI format is that the inactive state and phase of the SCLK signal can be programmed through the SPO and SPH bits in the CTL0 control register.

SPO Clock Polarity Bit

If the CTL0.SPO clock polarity control bit is clear, the bit produces a steady-state low value on the SCLK pin when data is not being transferred. If the CTL0.SPO bit is set, the bit places a steady-state high value on the SCLK pin when data is not being transferred.

SPH Phase-Control Bit

The CTL0.SPH phase-control bit selects the clock edge that captures data, and allows it to change state. The state of this bit has the most impact on the first bit transmitted, by either allowing or not allowing a clock transition before the first data capture edge. If the CTL0.SPH phase-control bit is clear, data is captured on the first clock edge transition. If the SPH bit is set, data is captured on the second clock edge transition.

The serial clock (SCLK) is held inactive while the SPI is IDLE. SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive timeout indication that occurs when the RX FIFO still contains data after a timeout period.

Motorola SPI Frame Format with SPO = 0 and SPH = 0

Figure 34-3 shows signal sequences for Motorola SPI format with SPO = 0 and SPH = 0.

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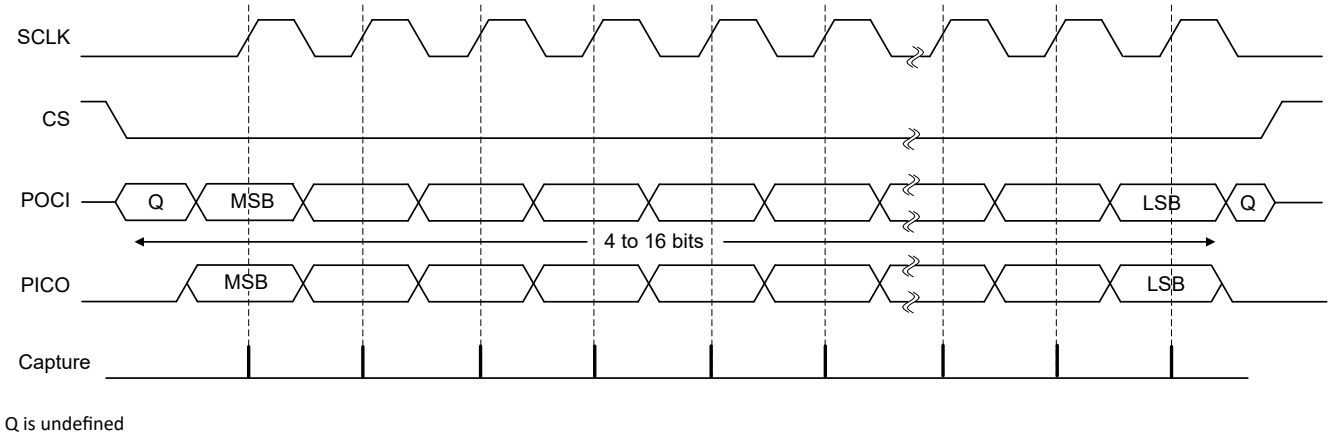


Figure 34-3. Motorola SPI Format With SPO = 0 and SPH = 0

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line PICO is forced low
- The UNICOMM-SPI *enables* the SCLK pin when configured as a controller
- The UNICOMM-SPI *disables* the SCLK pin when configured as a peripheral

If the SPI is enabled and the TX FIFO contains valid data, the CS controller signal is driven low at the start of transmission, enabling peripheral data onto the POCI input line of the controller. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO pin. Once both the controller and peripheral data are set, the SCLK controller clock pin goes high after an additional one-half SCLK period. The data is now captured on the rising edges and propagated on the falling edges of the SCLK signal.

For a single-word transmission, after all bits of the data word are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data-word transfer because the peripheral-select pin freezes the data in the serial peripheral register and prevents altering the data if the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. When the continuous transfer completes, the CS pin is returned to the IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 0 and SPH = 1

Figure 34-4 shows the signal sequence for Motorola SPI format with SPO = 0 and SPH = 1.

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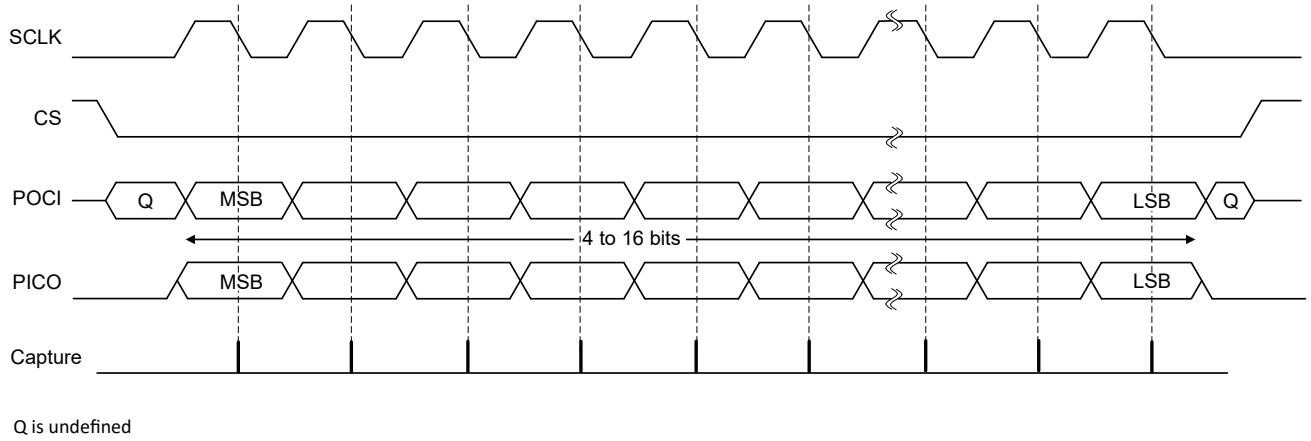


Figure 34-4. Motorola SPI Frame Format With SPO = 0 and SPH = 1

In this configuration, the following occurs during idle periods:

- SCLK is forced low
- CS is forced high
- The transmit data line PICO is forced low
- The UNICOMM-SPI *enables* the SCLK pin when configured as a controller
- The UNICOMM-SPI *disables* the SCLK pin when configured as a peripheral

If the SPI is enabled and valid data is present in the TX FIFO, CS controller signal goes low at the start of transmission.The controller PICO output is enabled. After an additional one-half SCLK period, both controller and peripheral valid data are enabled onto the respective transmission lines. At the same time, SCLK is enabled with a rising-edge transition. Data is then captured on the falling edges and propagated on the rising edges of the SCLK signal.

Fora single-word transfer, after all bits are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

Motorola SPI Frame Format with SPO = 1 and SPH = 0

Figure 34-5 shows signal sequences for Motorola SPI format with SPO = 1 and SPH = 0.

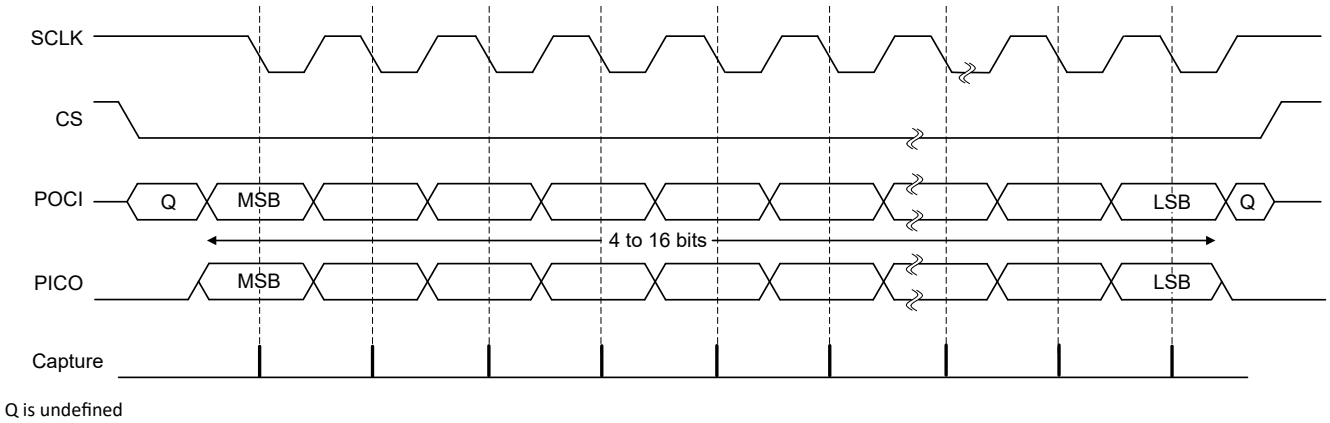


Figure 34-5. Motorola SPI Frame Format With SPO = 1 and SPH = 0

In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is arbitrarily forced low

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- The UNICOMM-SPI *enables* the SCLK pin when configured as a controller
- The UNICOMM-SPI *disables* the SCLK pin when configured as a peripheral

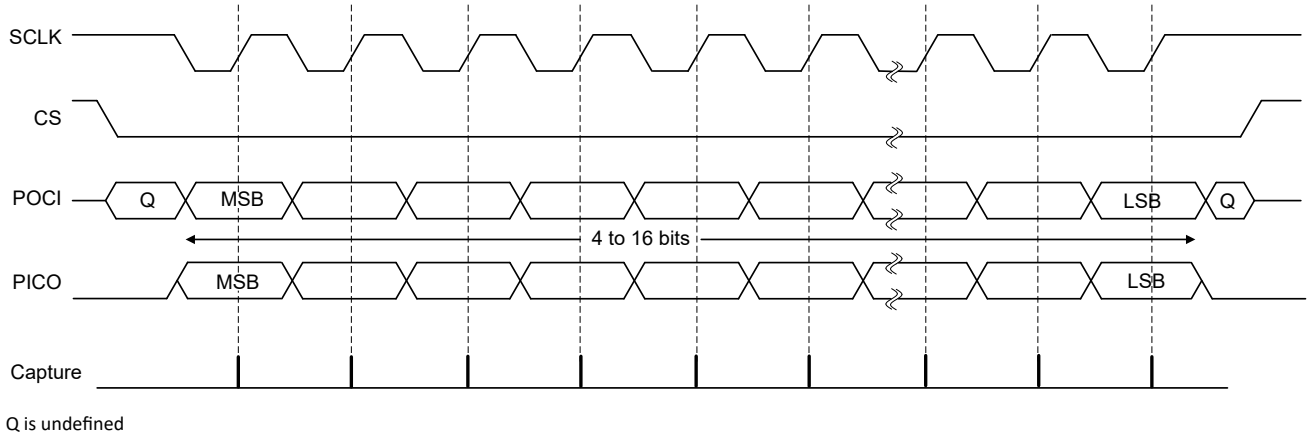
If the SPI is enabled and valid data is in the TX FIFO, the SPI CS controller signal goes low at the start of transmission and transfers the peripheral data to the controller's POCI line immediately. The controller PICO output pin is enabled.

One-half SCLK period later, valid controller data is transferred to the PICO line. When both the controller and peripheral data have been set, the SCLK controller clock pin becomes low after one additional half SCLK period. Data is captured on the falling edges and propagated on the rising edges of the SCLK signal.

For a single-word transmission after all bits of the data word are transferred, the CS line is returned to the IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS signal must pulse high between each data-word transfer, as the peripheral-select pin freezes the data in the serial peripheral register and prevents the data from being altered when the SPH bit is clear. The controller device must raise the CS pin of the peripheral device between each data transfer to enable the serial peripheral data write. When the continuous transfer completes, the CS pin returns to the IDLE state one SCLK period after the last bit is captured.

Motorola SPI Frame Format with SPO = 1 and SPH = 1

Figure 34-6 shows the signal sequence for Motorola SPI format with SPO = 1 and SPH = 1.



In this configuration, the following occurs during idle periods:

- SCLK is forced high
- CS is forced high
- The transmit data line PICO is arbitrarily forced low
- The UNICOMM-SPI *enables* the SCLK pin when configured as a controller
- The UNICOMM-SPI *disables* the SCLK pin when configured as a peripheral

If the SPI is enabled and valid data is in the TX FIFO, the start of transmission is signified by the CS controller signal going low. The controller PICO output pin is enabled. After an additional one-half SCLK period, both controller and peripheral data is transmitted onto their respective transmission lines. At the same time, SCLK is enabled with a falling-edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SCLK signal.

For a single word transmission, after all bits are transferred, the CS line returns to its IDLE high state one SCLK period after the last bit is captured. For continuous back-to-back transmissions, the CS pin remains in its active low state until the final bit of the last word is captured and then returns to its IDLE state. For continuous back-to-back transfers, the CS pin is held low between successive data words and terminates like a single-word transfer.

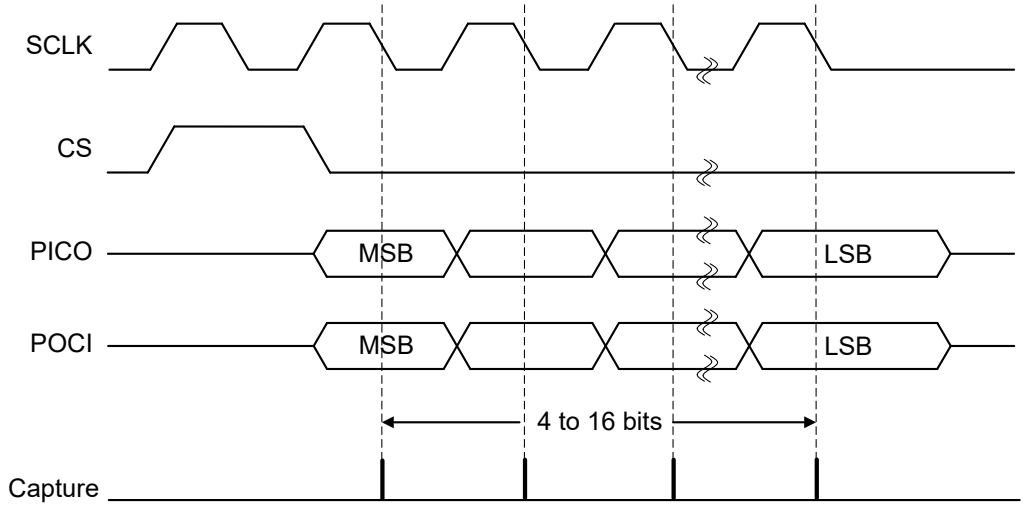
Figure 34-6. Motorola SPI Frame Format With SPO = 1 and SPH = 1

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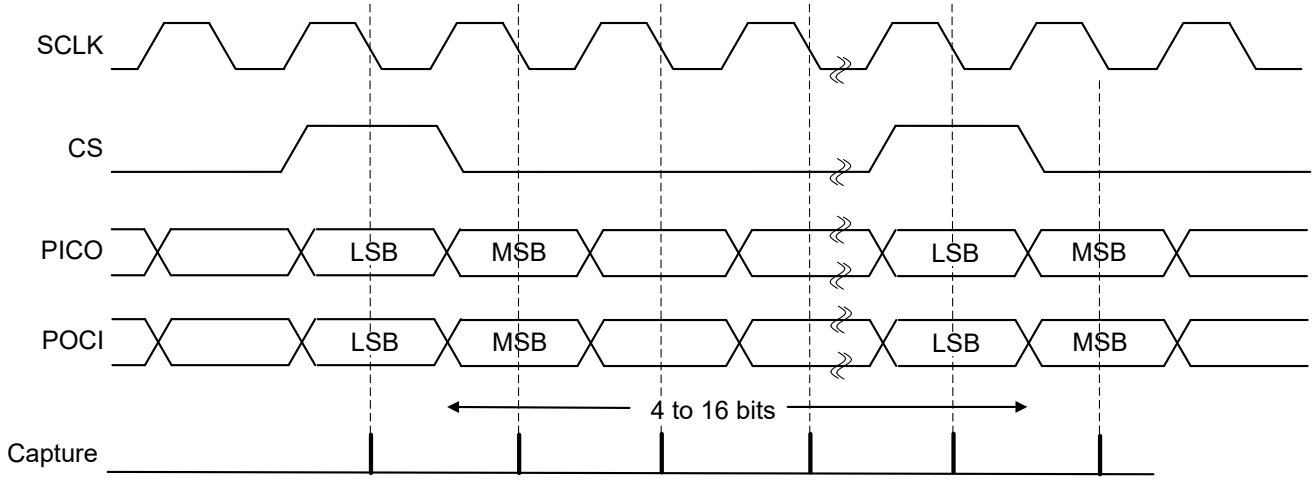
34.2.4.2 Texas Instruments Synchronous Serial Frame Format

The SPI peripheral is compatible with Texas Instruments Synchronous Serial frame format.

Figure 34-7 shows the TI synchronous serial frame format for a single and continuous transmitted frame.



Single Transmission Signal Sequences



Continuous Transmission Signal Sequences

Figure 34-7. TI Synchronous Serial Frame Format

SCLK and CS are forced low and the transmit data line PICO is put in tristate whenever the SPI is idle. When the bottom entry of the TX FIFO contains data, CS is pulsed high for one SCLK period. The transmitted value is also transferred from the TX FIFO to the serial shift register of the transmit logic. On the next rising edge of SCLK, the MSB of the 4- to 16-bit data frame is shifted out on the PICO pin. Likewise, the MSB of the received data is shifted onto the POCI pin by the off-chip serial peripheral device. Both the SPI and the off-chip serial peripheral device then clock each data bit into the respective serial shifters on each falling edge of SCLK. The received data is transferred from the serial shifter to the RX FIFO on the first rising edge of SCLK after the least significant bit (LSB) is latched.

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The serial clock (SCLK) is held inactive while the SPI is idle and SCLK transitions at the programmed frequency only during active transmission or reception of data. The IDLE state of SCLK provides a receive time-out indication that occurs when the RX FIFO still contains data after a time-out period.

34.2.5 Status Flags

The table below lists the behavior of the status bits in the STAT register. Status bits that are common across all UNICOMM peripherals and relate to the TX and RX FIFOs are explained in Section 31.2.2.4 from the top-level SPGSS chapter.

Table 34-1. UNICOMM-SPI Status Bits

Status Bit	Description
BUSY	1. BUSY bit is set (“ACTIVE”) when there is an ongoing transmission and reception. If in peripheral mode and CTL1.POD is set, i.e. the peripheral cannot transmit data on the POCI line, the BUSY bit is set during reception. 2. BUSY bit is cleared (“IDLE”) when there is no ongoing transaction (receive or transmit)

34.2.6 Initialization

Follow the high-level UNICOMM configurations in Section 31.3 before executing the below SPI-specific configurations.

Note

Pull-ups can be used to avoid unnecessary toggles on the SPI pins, which can take the peripheral to a wrong state. In addition, if the SCLK signal is programmed to steady state High through the SPO bit in the CTL0 register, then software must also configure the GPIO port pin corresponding to the SCLK signal as a pull-up.

To enable and initialize the SPI, perform the following initialization steps:

1. Clear the ENABLE bit in the CTL1 register before making any of the below configuration changes.
2. Select whether the SPI is a controller or peripheral:
   - For controller mode, set the CP bit in the CTL1 register.
   - For peripheral mode, clear the CP bit in the CTL1 register.
3. Configure the CTL0 and CTL1 registers based on the desired protocol, data width and other SPI-specific configurations.
4. Configure the desired FIFO trigger levels in the IFLS register.
5. Enable desired interrupts and/or DMA event by using CPU_INT, DMA_TRIG_RX, DMA_TRIG_TX group IMASK registers.
6. (Optionally) Configure the emulation mode for the peripheral in the PDBGCTL register.
7. Enable the SPI by setting the ENABLE bit in the CTL1 register.

34.2.7 Emulation Modes

The module behavior while the device is in debug mode is controlled by the FREE and SOFT bits in PDBGCTL register.

When the device is in debug mode and set into halt mode below behavior can be configured.

Table 34-2. Debug Mode Peripheral Behavior

PDBGCTL.FREE	PDBGCTL.SOFT	Function
1	**x**	Modules continues operation
0	**0**	Module stops immediately

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Table 34-2. Debug Mode Peripheral Behavior (continued)

PDBGCTL.FREE	PDBGCTL.SOFT	Function
0	1	Module stops after the next transfer has been finished

34.3 SPI Interrupts & Triggers

34.3.1 CPU Interrupts (IRQs)

The UNICOMM-SPI interrupts are fed through the UNICOMM instance interrupt line when that UNICOMM's IPMODE is configured as SPI. See Section 31.6.1 for more information on the UNICOMM CPU interrupts.

34.3.2 DMA Triggers

The UNICOMM-SPI DMA triggers (TX and RX) are fed through the UNICOMM instance trigger lines when that UNICOMM's IPMODE is configured as SPI. See Section 31.6.2 for more information on the TX and RX UNICOMM DMA triggers.

34.4 UNICOMM-SPI Registers

This Section describes the UNICOMM-SPI Registers.

34.4.1 UNICOMM-SPI Base Address Table

Table 34-3. UNICOMM-SPI Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
Uc0spiRegs	UNICOMMSPI_REGS	UC0_SPI	0x4061_8000
Uc1spiRegs	UNICOMMSPI_REGS	UC1_SPI	0x4061_9000
Uc3spiRegs	UNICOMMSPI_REGS	UC3_SPI	0x4065_8000
Uc4spiRegs	UNICOMMSPI_REGS	UC4_SPI	0x4065_9000

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34.4.2 UNICOMMSPI_REGS Registers

Table 34-4 lists the memory-mapped registers for the UNICOMMSPI_REGS registers. All register offset addresses not listed in Table 34-4 should be considered as reserved locations and the register contents should not be modified.

Table 34-4. UNICOMMSPI_REGS Registers

Offset	Acronym	Register Name	Group	Section
0h	CLKDIV	Clock Divider		Go
8h	CLKSEL	Clock Source Selection/Enable.		Go
18h	PDBGCTL	Peripheral Debug Control		Go
20h	IIDX	Interrupt Index Register	CPU_INT	Go
28h	IMASK	Interrupt mask	CPU_INT	Go
30h	RIS	Raw interrupt status	CPU_INT	Go
38h	MIS	Masked interrupt status	CPU_INT	Go
40h	ISET	Interrupt set	CPU_INT	Go
48h	ICLR	Interrupt clear	CPU_INT	Go
58h	IMASK	Interrupt mask	DMA_TRIG_RX	Go
60h	RIS	Raw interrupt status	DMA_TRIG_RX	Go
68h	MIS	Masked interrupt status	DMA_TRIG_RX	Go
70h	ISET	Interrupt set	DMA_TRIG_RX	Go
88h	IMASK	Interrupt mask	DMA_TRIG_TX	Go
90h	RIS	Raw interrupt status	DMA_TRIG_TX	Go
98h	MIS	Masked interrupt status	DMA_TRIG_TX	Go
A0h	ISET	Interrupt set	DMA_TRIG_TX	Go
E4h	INTCTL	Interrupt control register		Go
100h	CTL0	SPI control register 0		Go
108h	STAT	Status Register		Go
10Ch	IFLS	Interrupt FIFO Level Select Register		Go
110h	CLKCTL	Clock prescaler and divider register.		Go
120h	TXDATA	TXDATA Register		Go
124h	RXDATA	RXDATA Register		Go
14Ch	CTL1	SPI control register 1		Go

Complex bit access types are encoded to fit into small table cells. Table 34-5 shows the codes that are used for access types in this section.

Table 34-5. UNICOMMSPI_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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1 CLKDIV Register (Offset = 0h) [Reset = 00000000h]

CLKDIV is shown in Figure 34-8 and described in Table 34-6.

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This register is used to specify the module-specific divide ratio of the SPI functional clock (SPIclk).

Figure 34-8. CLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RATIO		
R/W-0h													R/W-0h		

Table 34-7. CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2-0	RATIO	R/W	0h	Selects divide ratio of module clock 0h = Do not divide clock source 1h = Divide clock source by 2 2h = Divide clock source by 3 3h = Divide clock source by 4 4h = Divide clock source by 5 5h = Divide clock source by 6 6h = Divide clock source by 7 7h = Divide clock source by 8

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2 CLKSEL Register (Offset = 8h) [Reset = 00000000h]

CLKSEL is shown in Figure 34-9 and described in Table 34-7.

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SPI Source Clock Selection.

Figure 34-9. CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				MCLKDIV2	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

Table 34-9. CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	MCLKDIV2	R/W	0h	Enables MCLKDIV2 as the UNICOMM SPI clock source. 0h = Does not select this clock as a source 1h = Select this clock as a source
2-0	RESERVED	R/W	0h	

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3 PDBGCTL Register (Offset = 18h) [Reset = 00000000h]

PDBGCTL is shown in Figure 34-10 and described in Table 34-8.

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SPI Debug Control. This register can be used by the software developer to control the behavior of the peripheral relative to the 'Core Halted' input

Figure 34-10. PDBGCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-0h						R/W-0h	R/W-0h

Table 34-11. PDBGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1	SOFT	R/W	1h	Soft Halt Boundary Control. This function is only available, if [FREE] is set to 'STOP' 0h = Not supported 1h = The peripheral blocks the debug freeze until it has reached a boundary where it can resume without corruption
0	FREE	R/W	1h	Free Run Control. 0h = The peripheral freezes functionality while the Core Halted input is asserted and resumes when it is deasserted. 1h = The peripheral ignores the state of the Core Halted input

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4 IIDX Register (Offset = 20h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 34-11 and described in Table 34-9.

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This register provides the highest priority enabled interrupt index. Value 0x00 means no event pending. Interrupt 1 is the highest priority, IIDX next highest, 4, 8, ... IIDX^31 is the least priority. That is, the least bit position that is set to 1 denotes the highest priority pending interrupt. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred. On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in [RIS] and [MIS] are cleared as well. After a read from the CPU (not from the debug interface), the register is updated with the next highest priority interrupt, if none are pending, then it should display 0x0.

Figure 34-11. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 34-13. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 00h = No interrupt pending 1h = Transmit Parity Event/interrupt pending 2h = RX FIFO Overflow Event/interrupt pending 3h = Receive FIFO Event 4h = RX FIFO Full Interrupt 5h = TX FIFO underflow interrupt 6h = Transmit FIFO Event 7h = Transmit FIFO Empty Event/interrupt pending 9h = End of Transmit Event/interrupt pending Ah = SPI receive time-out interrupt 10h = DMA DONE on RX 11h = DMA DONE on TX

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5 IMASK Register (Offset = 28h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 34-12 and described in Table 34-10.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 34-12. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED						IDLE
R/W-0h	R/W-0h						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	TXEMPTY	TX	TXFIFO_UNF	RXFULL	RX	RXFIFO_OVF	PER
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 34-15. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	0h	
16	DMA_DONE_TX	R/W	0h	SPI DMA Done on TX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
15	DMA_DONE_RX	R/W	0h	SPI DMA Done on RX Event Channel Interrupt Mask. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
14-9	RESERVED	R/W	0h	
8	IDLE	R/W	0h	SPI Idle Interrupt Mask. This interrupt is raised when the SPI has finished transfers and gone into an idle state. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
7	RESERVED	R/W	0h	
6	TXEMPTY	R/W	0h	SPI TX FIFO Empty Interrupt Mask. This interrupt is raised when all data has been shifted out of the TX FIFO and the SPI transmitter goes idle. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
5	TX	R/W	0h	SPI Transmit Interrupt Mask. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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Table 34-15. IMASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TXFIFO_UNF	R/W	0h	SPI TX FIFO Underflow Interrupt Mask. This interrupt is raised when the UNICOMM-SPI (in peripheral mode) gets clock edges on the SCLK line from the SPI controller, but the TX FIFO is empty. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
3	RXFULL	R/W	0h	SPI RX FIFO Full Interrupt Mask. This interrupt is raised when the RX FIFO is full. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
2	RX	R/W	0h	SPI Receive Interrupt Mask. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1	RXFIFO_OVF	R/W	0h	SPI RX FIFO Overflow Interrupt Mask. This interrupt is raised when the SPI receiver tries to receive data, but the SPI RX FIFO is full. In this case, new data will be discarded/lost by the SPI receiver. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
0	PER	R/W	0h	SPI Parity Error Interrupt Mask. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask

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6 RIS Register (Offset = 30h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 34-13 and described in Table 34-11.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 34-13. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R-0h							R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED						IDLE
R-0h	R-0h						R-0h
7	6	5	4	3	2	1	0
RESERVED	TXEMPTY	TX	TXFIFO_UNF	RXFULL	RX	RXFIFO_OVF	PER
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 34-17. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	DMA_DONE_TX	R	0h	SPI DMA Done on TX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	SPI DMA Done on RX Event Channel Interrupt Raw Status. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur 1h = Interrupt occurred
14-9	RESERVED	R	0h	
8	IDLE	R	0h	SPI Idle Interrupt Raw Status. This interrupt is raised when the SPI has finished transfers and gone into an idle state. 0h = Interrupt did not occur 1h = Interrupt occurred
7	RESERVED	R	0h	
6	TXEMPTY	R	0h	SPI TX FIFO Empty Interrupt Raw Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the SPI transmitter goes idle. 0h = Interrupt did not occur 1h = Interrupt occurred
5	TX	R	0h	SPI Transmit Interrupt Raw Status. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur 1h = Interrupt occurred

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Table 34-17. RIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TXFIFO_UNF	R	0h	SPI TX FIFO Underflow Interrupt Raw Status. This interrupt is raised when the UNICOMM-SPI (in peripheral mode) gets clock edges on the SCLK line from the SPI controller, but the TX FIFO is empty. 0h = Interrupt did not occur 1h = Interrupt occurred
3	RXFULL	R	0h	SPI RX FIFO Full Interrupt Raw Status. This interrupt is raised when the RX FIFO is full. 0h = Interrupt did not occur 1h = Interrupt occurred
2	RX	R	0h	SPI Receive Interrupt Raw Status. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur 1h = Interrupt occurred
1	RXFIFO_OVF	R	0h	SPI RX FIFO Overflow Interrupt Raw Status. This interrupt is raised when the SPI receiver tries to receive data, but the SPI RX FIFO is full. In this case, new data will be discarded/lost by the SPI receiver. 0h = Interrupt did not occur 1h = Interrupt occurred
0	PER	R	0h	SPI Parity Error Interrupt Raw Status. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Interrupt did not occur 1h = Interrupt occurred

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7 MIS Register (Offset = 38h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 34-14 and described in Table 34-12.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 34-14. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
R-0h							R-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED						IDLE
R-0h	R-0h						R-0h
7	6	5	4	3	2	1	0
RESERVED	TXEMPTY	TX	TXFIFO_UNF	RXFULL	RX	RXFIFO_OVF	PER
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 34-19. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	
16	DMA_DONE_TX	R	0h	SPI DMA Done on TX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
15	DMA_DONE_RX	R	0h	SPI DMA Done on RX Event Channel Interrupt Masked Status. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
14-9	RESERVED	R	0h	
8	IDLE	R	0h	SPI Idle Interrupt Masked Status. This interrupt is raised when the SPI has finished transfers and gone into an idle state. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
7	RESERVED	R	0h	
6	TXEMPTY	R	0h	SPI TX FIFO Empty Interrupt Masked Status. This interrupt is raised when all data has been shifted out of the TX FIFO and the SPI transmitter goes idle. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
5	TX	R	0h	SPI Transmit Interrupt Masked Status. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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Table 34-19. MIS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TXFIFO_UNF	R	0h	SPI TX FIFO Underflow Interrupt Masked Status. This interrupt is raised when the UNICOMM-SPI (in peripheral mode) gets clock edges on the SCLK line from the SPI controller, but the TX FIFO is empty. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
3	RXFULL	R	0h	SPI RX FIFO Full Interrupt Masked Status. This interrupt is raised when the RX FIFO is full. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
2	RX	R	0h	SPI Receive Interrupt Masked Status. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
1	RXFIFO_OVF	R	0h	SPI RX FIFO Overflow Interrupt Masked Status. This interrupt is raised when the SPI receiver tries to receive data, but the SPI RX FIFO is full. In this case, new data will be discarded/lost by the SPI receiver. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
0	PER	R	0h	SPI Parity Error Interrupt Masked Status. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred

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8 ISET Register (Offset = 40h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 34-15 and described in Table 34-13.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 34-15. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
W-0h							W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED						IDLE
W-0h	W-0h						W-0h
7	6	5	4	3	2	1	0
RESERVED	TXEMPTY	TX	TXFIFO_UNF	RXFULL	RX	RXFIFO_OVF	PER
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 34-21. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	W	0h	
16	DMA_DONE_TX	W	0h	Set SPI DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt
15	DMA_DONE_RX	W	0h	Set SPI DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Set Interrupt
14-9	RESERVED	W	0h	
8	IDLE	W	0h	Set SPI Idle Interrupt. This interrupt is raised when the SPI has finished transfers and gone into an idle state. 0h = Writing 0 has no effect 1h = Set Interrupt
7	RESERVED	W	0h	
6	TXEMPTY	W	0h	Set SPI TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the SPI transmitter goes idle. 0h = Writing 0 has no effect 1h = Set Interrupt
5	TX	W	0h	Set SPI Transmit Interrupt. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Set Interrupt

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Table 34-21. ISET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TXFIFO_UNF	W	0h	Set SPI TX FIFO Underflow Interrupt. This interrupt is raised when the UNICOMM-SPI (in peripheral mode) gets clock edges on the SCLK line from the SPI controller, but the TX FIFO is empty. 0h = Writing has no effect 1h = Set interrupt
3	RXFULL	W	0h	Set SPI RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Writing has no effect 1h = Set Interrupt
2	RX	W	0h	Set SPI Receive Interrupt. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Set Interrupt
1	RXFIFO_OVF	W	0h	Set SPI RX FIFO Overflow Interrupt. This interrupt is raised when the SPI receiver tries to receive data, but the SPI RX FIFO is full. In this case, new data will be discarded/lost by the SPI receiver. 0h = Writing 0 has no effect 1h = Set Interrupt
0	PER	W	0h	Set SPI Parity Error Interrupt. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Writing 0 has no effect 1h = Set Interrupt

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9 ICLR Register (Offset = 48h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 34-16 and described in Table 34-14.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 34-16. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							DMA_DONE_TX
W-0h							W-0h
15	14	13	12	11	10	9	8
DMA_DONE_RX	RESERVED						IDLE
W-0h	W-0h						W-0h
7	6	5	4	3	2	1	0
RESERVED	TXEMPTY	TX	TXFIFO_UNF	RXFULL	RX	RXFIFO_OVF	PER
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 34-23. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	W	0h	
16	DMA_DONE_TX	W	0h	Clear SPI DMA Done on TX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Clear Interrupt
15	DMA_DONE_RX	W	0h	Clear SPI DMA Done on RX Event Channel Interrupt. This interrupt is raised when the DONE signal is sent to the SPI from a DMA indicating all the transactions have completed. 0h = Writing 0 has no effect 1h = Clear Interrupt
14-9	RESERVED	W	0h	
8	IDLE	W	0h	Clear SPI Idle Interrupt. This interrupt is raised when the SPI has finished transfers and gone into an idle state. 0h = Writing 0 has no effect 1h = Clear Interrupt
7	RESERVED	W	0h	
6	TXEMPTY	W	0h	Clear SPI TX FIFO Empty Interrupt. This interrupt is raised when all data has been shifted out of the TX FIFO and the SPI transmitter goes idle. 0h = Writing 0 has no effect 1h = Clear Interrupt
5	TX	W	0h	Clear SPI Transmit Interrupt. This interrupt is raised when the TX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Clear Interrupt
4	TXFIFO_UNF	W	0h	Clear SPI TX FIFO Underflow Interrupt. This interrupt is raised when the UNICOMM-SPI (in peripheral mode) gets clock edges on the SCLK line from the SPI controller, but the TX FIFO is empty. 0h = Writing has no effect 1h = Clear interrupt

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Table 34-23. ICLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RXFULL	W	0h	Clear SPI RX FIFO Full Interrupt. This interrupt is raised when the RX FIFO is full. 0h = Writing has no effect 1h = Clear interrupt
2	RX	W	0h	Clear SPI Receive Interrupt. This interrupt is raised when the RX FIFO level has met the condition configured in the IFLS register. 0h = Writing 0 has no effect 1h = Clear Interrupt
1	RXFIFO_OVF	W	0h	Clear SPI RX FIFO Overflow Interrupt. This interrupt is raised when the SPI receiver tries to receive data, but the SPI RX FIFO is full. In this case, new data will be discarded/lost by the SPI receiver. 0h = Writing 0 has no effect 1h = Clear Interrupt
0	PER	W	0h	Clear SPI Parity Error Interrupt. This interrupt is raised when a character is received with a mismatch between the calculated parity and the received parity. 0h = Writing 0 has no effect 1h = Clear Interrupt

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10 IMASK Register (Offset = 58h) [Reset = 00000000h] (DMA_TRIG_RX)

IMASK is shown in Figure 34-17 and described in Table 34-15.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 34-17. IMASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RX	RESERVED	
R/W-0h													R/W-0h	R/W-0h	

Table 34-25. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	0h	
2	RX	R/W	0h	SPI Receive DMA Trigger Mask. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
1-0	RESERVED	R/W	0h	

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11 RIS Register (Offset = 60h) [Reset = 00000000h] (DMA_TRIG_RX)

RIS is shown in Figure 34-18 and described in Table 34-16.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 34-18. RIS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RX	RESERVED	
R-0h													R-0h	R-0h	

Table 34-27. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RX	R	0h	SPI Receive DMA Trigger Raw Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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12 MIS Register (Offset = 68h) [Reset = 00000000h] (DMA_TRIG_RX)

MIS is shown in Figure 34-19 and described in Table 34-17.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 34-19. MIS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RX	RESERVED	
R-0h													R-0h	R-0h	

Table 34-29. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	
2	RX	R	0h	SPI Receive DMA Trigger Masked Status. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled 1h = Interrupt occurred
1-0	RESERVED	R	0h	

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13 ISET Register (Offset = 70h) [Reset = 00000000h] (DMA_TRIG_RX)

ISET is shown in Figure 34-20 and described in Table 34-18.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 34-20. ISET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RX	RESERVED	
W-0h													W-0h	W-0h	

Table 34-31. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	W	0h	
2	RX	W	0h	Set SPI Receive DMA Trigger. The DMA is triggered when the RX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
1-0	RESERVED	W	0h	

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14 IMASK Register (Offset = 88h) [Reset = 00000000h] (DMA_TRIG_TX)

IMASK is shown in Figure 34-21 and described in Table 34-19.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 34-21. IMASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX	RESERVED				
R/W-0h										R/W-0h	R/W-0h				

Table 34-33. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	0h	
5	TX	R/W	0h	SPI Transmit DMA Trigger Mask. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Clear Interrupt Mask 1h = Set Interrupt Mask
4-0	RESERVED	R/W	0h	

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15 RIS Register (Offset = 90h) [Reset = 00000000h] (DMA_TRIG_TX)

RIS is shown in Figure 34-22 and described in Table 34-20.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 34-22. RIS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX	RESERVED				
R-0h										R-0h	R-0h				

Table 34-35. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	
5	TX	R	0h	SPI Transmit DMA Trigger Raw Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur 1h = Interrupt occurred
4-0	RESERVED	R	0h	

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16 MIS Register (Offset = 98h) [Reset = 00000000h] (DMA_TRIG_TX)

MIS is shown in Figure 34-23 and described in Table 34-21.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 34-23. MIS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX	RESERVED				
R-0h										R-0h	R-0h				

Table 34-37. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	
5	TX	R	0h	SPI Transmit DMA Trigger Masked Status. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Interrupt did not occur or mask was not enabled. 1h = Interrupt occurred
4-0	RESERVED	R	0h	

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17 ISET Register (Offset = A0h) [Reset = 00000000h] (DMA_TRIG_TX)

ISET is shown in Figure 34-24 and described in Table 34-22.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 34-24. ISET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX	RESERVED				
W-0h										W-0h	W-0h				

Table 34-39. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	W	0h	
5	TX	W	0h	Set SPI Receive DMA Trigger. The DMA is triggered when the TX FIFO condition programmed by the IFLS register is met. 0h = Writing 0 has no effect 1h = Set Interrupt
4-0	RESERVED	W	0h	

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18 INTCTL Register (Offset = E4h) [Reset = 00000000h]

INTCTL is shown in Figure 34-25 and described in Table 34-23.

Return to the Summary Table.

Interrupt Control Register.

Figure 34-25. INTCTL Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED							INTEVAL
W-0h							W-0h

Table 34-41. INTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	0h	
0	INTEVAL	W	0h	Writing a 1 to this field re-evaluates the interrupt sources. 0h = Writing 0 has no effect 1h = Interrupt Eval

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19 CTL0 Register (Offset = 100h) [Reset = 00000000h]

CTL0 is shown in Figure 34-26 and described in Table 34-24.

Return to the Summary Table.

SPI Control Register 0.

Figure 34-26. CTL0 Register

31	30	29	28	27	26	25	24
RESERVED			CS_MASK_ROTATE_EN	CS3_ROTATE_MASK	CS2_ROTATE_MASK	CS1_ROTATE_MASK	CS0_ROTATE_MASK
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	CSCLR	RESERVED				SPH	SPO
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	FRF		DSS				
R/W-0h	R/W-0h		R/W-0h				

Table 34-43. CTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	0h	
28	CS_MASK_ROTATE_EN	R/W	0h	Chip select rotate mask enable 0h = No additional delay 1h = Enable
27	CS3_ROTATE_MASK	R/W	0h	Chip select rotate mask 0h = Disable 1h = Enable
26	CS2_ROTATE_MASK	R/W	0h	Chip select rotate mask 0h = Disable 1h = Enable
25	CS1_ROTATE_MASK	R/W	0h	Chip select rotate mask 0h = Disable 1h = Enable
24	CS0_ROTATE_MASK	R/W	0h	Chip select rotate mask 0h = Disable 1h = Enable
23-15	RESERVED	R/W	0h	
14	CSCLR	R/W	0h	Clear shift register counter on CS inactive This bit is relevant only in the peripheral, CTL1.CP=0. 0h = Disable automatic clear of shift register when CS goes to disable. 1h = Enable automatic clear of shift register when CS goes to disable.
13-10	RESERVED	R/W	0h	
9	SPH	R/W	0h	CLKOUT phase (Motorola SPI frame format only) This bit selects the clock edge that captures data and enables it to change state. It has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture edge. 0h = Data is captured on the first clock edge transition. 1h = Data is captured on the second clock edge transition.

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Table 34-43. CTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SPO	R/W	0h	CLKOUT polarity (Motorola SPI frame format only) 0h = SPI produces a steady state LOW value on the CLKOUT 1h = SPI produces a steady state HIGH value on the CLKOUT
7	RESERVED	R/W	0h	
6-5	FRF	R/W	0h	Frame format Select 0h = Motorola SPI frame format (3 wire mode) 1h = Motorola SPI frame format (4 wire mode) 2h = TI synchronous serial frame format 3h = Reserved - not to be selected
4-0	DSS	R/W	0h	Data Size Select. Values 0 - 2 are reserved and shall not be used. 3h = 4_BIT : 4-bit data SPI allows only values up to 16 Bit 3h (R/W) = Data Size Select bits: 4 4h (R/W) = Data Size Select bits: 5 5h (R/W) = Data Size Select bits: 6 6h (R/W) = Data Size Select bits: 7 7h (R/W) = Data Size Select bits: 8 8h (R/W) = Data Size Select bits: 9 9h (R/W) = Data Size Select bits: 10 Ah (R/W) = Data Size Select bits: 11 Bh (R/W) = Data Size Select bits: 12 Ch (R/W) = Data Size Select bits: 13 Dh (R/W) = Data Size Select bits: 14 Eh (R/W) = Data Size Select bits: 15 Fh (R/W) = Data Size Select bits: 16

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20 STAT Register (Offset = 108h) [Reset = 00000000h]

STAT is shown in Figure 34-27 and described in Table 34-25.

Return to the Summary Table.

SPI Status Register.

Figure 34-27. STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							BUSY
R-0h							R-0h
7	6	5	4	3	2	1	0
TXCLR	TXFF	TXFE	RXCLR	RXFF	RXFE	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 34-45. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8	BUSY	R	0h	SPI Busy Status. 0h = SPI is in idle mode. 1h = SPI is currently transmitting and/or receiving data
7	TXCLR	R	0h	SPI TX FIFO Clear Status. 0h = TX FIFO is not cleared 1h = TX FIFO clear is complete
6	TXFF	R	0h	SPI TX FIFO Full Status. 0h = TX FIFO is not full 1h = TX FIFO is full
5	TXFE	R	1h	TX FIFO Empty Status. 0h = TX FIFO is not empty 1h = TX FIFO is empty
4	RXCLR	R	0h	SPI RX FIFO Clear Status. 0h = FIFO is not cleared 1h = FIFO clear is complete
3	RXFF	R	0h	SPI RX FIFO Full Status. 0h = RX FIFO is not full 1h = RX FIFO is full
2	RXFE	R	1h	RX FIFO Empty Status. 0h = RX FIFO is not empty 1h = RX FIFO is empty
1-0	RESERVED	R	0h	

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21 IFLS Register (Offset = 10Ch) [Reset = 00000022h]

IFLS is shown in Figure 34-28 and described in Table 34-26.

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Interrupt FIFO Level Select. The IFLS register is the interrupt FIFO level select register. You can use this register to define the levels at which the TX, RX and timeout interrupt flags are triggered. The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered when the RX FIFO is filled with two or more characters. Out of reset, the TXIFLSEL and RXIFLSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

Figure 34-28. IFLS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RXCLR	RXIFLSEL			TXCLR	TXIFLSEL		
R/W-0h	R/W-2h			R/W-0h	R/W-2h		

Table 34-47. IFLS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7	RXCLR	R/W	0h	RX FIFO Clear. Setting this bit will clear the RX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
6-4	RXIFLSEL	R/W	2h	RX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = RX FIFO >= 1/4 full 2h = RX FIFO >= 1/2 full (default) 3h = RX FIFO >= 3/4 full 4h = Opposite of empty 5h = RX FIFO is full 6h = RX_FIFO >= (MAX_FIFO_LEN -1) 7h = RX_FIFO <= 1
3	TXCLR	R/W	0h	TX FIFO Clear. Setting this bit will clear the TX FIFO contents. 0h = Disable FIFO clear 1h = Enable FIFO Clear
2-0	TXIFLSEL	R/W	2h	TX FIFO Level Select for generating events (interrupt/DMA). Note: for undefined settings the default configuration is used. 1h = TX FIFO <= 3/4 empty 2h = TX FIFO <= 1/2 empty (default) 3h = TX FIFO <= 1/4 empty 4h = Opposite of full 5h = TX FIFO is empty 6h = TX FIFO <= 1 7h = TX_FIFO >= (MAX_FIFO_LEN -1)

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22 CLKCTL Register (Offset = 110h) [Reset = 00000000h]

CLKCTL is shown in Figure 34-29 and described in Table 34-27.

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Clock prescaler and divider register. This register contains the settings for the Clock prescaler and divider settings.

Figure 34-29. CLKCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DSAMPLE				RESERVED											
R/W-0h				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SCR									
R/W-0h						R/W-0h									

Table 34-49. CLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	DSAMPLE	R/W	0h	Delayed Sampling Value. In controller mode, data on input pin will be delayed sampled by the defined clock cycles of internal functional clock (SPIclk) hence relaxing the setup time of input data. This setting is useful in systems where the board delays and external peripheral delays are more than the input setup time of the controller. Please refer to the datasheet for values of controller input setup time and assess what DSAMPLE value meets the requirement of the system. Note: High values of DSAMPLE can cause HOLD time violations and must be factored in the calculations. 0h = Delayed sampling is not used Fh = Highest possible value
27-10	RESERVED	R/W	0h	
9-0	SCR	R/W	0h	Serial Clock Divider. This is used to generate the transmit and receive bit rate of the SPI. The SPI bit rate is (SPIclk)/((SCR+1)*2). SCR is a value from 0-1023. 0h = Smallest value 3FFh = Highest possible value

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23 TXDATA Register (Offset = 120h) [Reset = 00000000h]

TXDATA is shown in Figure 34-30 and described in Table 34-28.

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Transmit Data Register. Writing puts the data into the TX FIFO. Reading this register returns the last written value. Only the lower 16-bits of data written into the register is transferred to one 16-bits wide TX FIFO entry.

Figure 34-30. TXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DATA															
W-0h																W-0h															

Table 34-51. TXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	W	0h	
15-0	DATA	W	0h	Transmit Data. When read, last written 16-bits will be returned. When written, one FIFO entry will be written. Data values are removed from the TX FIFO one value at a time by the transmit logic. They are loaded into the transmit serial shifter, then serially shifted out onto the TXD output pin at the programmed bit rate. When a data size of less than 16 bits is selected, the user must right-justify data written to the TX FIFO. The transmit logic ignores the unused bits. 0h = Smallest value FFFFh = Highest possible value

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24 RXDATA Register (Offset = 124h) [Reset = 00000000h]

RXDATA is shown in Figure 34-31 and described in Table 34-29.

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Receive Data Register. Reading this register returns one 16-bit value from the RX FIFO. If the FIFO is empty, the last read value is returned. Writing has not effect and is ignored.

Figure 34-31. RXDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DATA															
R-0h																R-0h															

Table 34-53. RXDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-0	DATA	R	0h	Received Data. When read, 1 entry of the RX FIFO is returned as a 16-bit value. As data values are removed by the receive logic from the incoming data frame, they are placed into an entry in the RX FIFO, pointed to by the current FIFO write pointer. Received data less than 16 bits is automatically right justified. 0h = Smallest value FFFFh = Highest possible value

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25 CTL1 Register (Offset = 14Ch) [Reset = 00000004h]

CTL1 is shown in Figure 34-32 and described in Table 34-30.

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SPI Control Register 1.

Figure 34-32. CTL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						SUSPEND	PTEN
R/W-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	PES	PREN	MSB	POD	CP	LBM	ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 34-55. CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	0h	
9	SUSPEND	R/W	0h	Suspend External Communication. When this bit is set, SPI communication on the external bus is suspended after the CS has returned to the idle state in controller mode, and after the CS is read as an idle state in peripheral mode. 0h = Functional mode resumed 1h = External communication suspended
8	PTEN	R/W	0h	Parity Transmit Enable. If enabled, parity transmission will be done for both controller and peripheral modes. 0h = Parity transmission is disabled 1h = Parity transmission is enabled
7	RESERVED	R/W	0h	
6	PES	R/W	0h	Even Parity Select. 0h = Odd Parity mode 1h = Even Parity mode
5	PREN	R/W	0h	Parity Receive Enable. If enabled, parity reception check will be done for both controller and peripheral modes In case of a parity miss-match the parity error flag RIS.PER will be set. 0h = Disable Parity receive function 1h = Enable Parity receive function
4	MSB	R/W	0h	MSB First Select. Controls the direction of the receive and transmit shift register. 0h = LSB first 1h = MSB first
3	POD	R/W	0h	Peripheral-mode: Data output disabled. This bit is relevant only in Peripheral mode. In multiple-peripheral system topologies, SPI controller can broadcast a message to all peripherals, while only one peripheral drives the line. POD can be used by the SPI peripheral to disable driving data on the line. 0h = SPI can drive the POCI output in peripheral mode. 1h = SPI cannot drive the POCI output in peripheral mode.

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Table 34-55. CTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CP	R/W	1h	Controller or Peripheral Mode Select. This bit can be modified only when SPI is disabled, CTL1.ENABLE=0. 0h = Select Peripheral mode 1h = Select Controller Mode
1	LBM	R/W	0h	Loopback Mode Enable. 0h = Disable loopback mode 1h = Enable loopback mode
0	ENABLE	R/W	0h	SPI Enable. 0h = Disable module function 1h = Enable module function

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Chapter 35

Debug Subsystem (DEBUGSS)

The Debug Subsystem (DEBUGSS) is implemented in all AM13E232x devices. The DEBUGSS enables comprehensive debug of application software running on the processor during development by interfacing an external debug probe to the device systems through a Serial Wire Debug (SWD) and JTAG interface.

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35.4 DEBUGSS Registers 2635

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35.1 DEBUGSS Overview

The Debug Subsystem (DEBUGSS) interfaces the ARM Serial Wire Debug (SWD) two-wire or JTAG four-wire physical interface to multiple debug functions within the device. AM13E232x devices support debugging of processor execution, the device state, and the power state (through EnergyTrace technology). The DEBUGSS also provides a mailbox system for communicating with software through SWD/JTAG.

Key features provided by the debug subsystem include:

- The ARM Serial Wire Debug (SWD) two-wire (SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pullup and pulldown resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as GPIOs
  - Support for debug on all low power modes
- The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) four-wire (TMS, TCK, TDO, TDI) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pullup and pulldown resistors for TMS, TCK, TDI, TDO, enabled by default
  - Support for disabling JTAG functions to use JTAG pins as GPIOs
  - Support for debug on all low power modes
- Debug of the processor
  - Run, halt, and step debug support
  - Up to 8 hardware breakpoints (BPU)
  - Up to 4 hardware watchpoints (DWT)
  - Instruction trace of up to 4 branches through the ARM Micro Trace Buffer (MTB)
  - Non-intrusive program-flow trace through the ARM Embedded Trace Macrocell (ETM)
  - Software breakpoints supported
- Software-configurable peripheral behavior during processor debug
  - Ability to free run select peripherals through debug halt
  - Ability to halt select peripherals on a debug halt
  - Ability to request reset and mode changes to the PMCU
- Monitoring of CPU state through EnergyTrace technology
- Mailbox (DSSM) for passing data and control signals between the SWD interface and Boot ROM (as well as application software)
- Support for various security features, including SWD/JTAG lockout and password authenticated debugging

35.1.1 Debug Interconnect

The DEBUGSS architecture is given in Figure 35-1.

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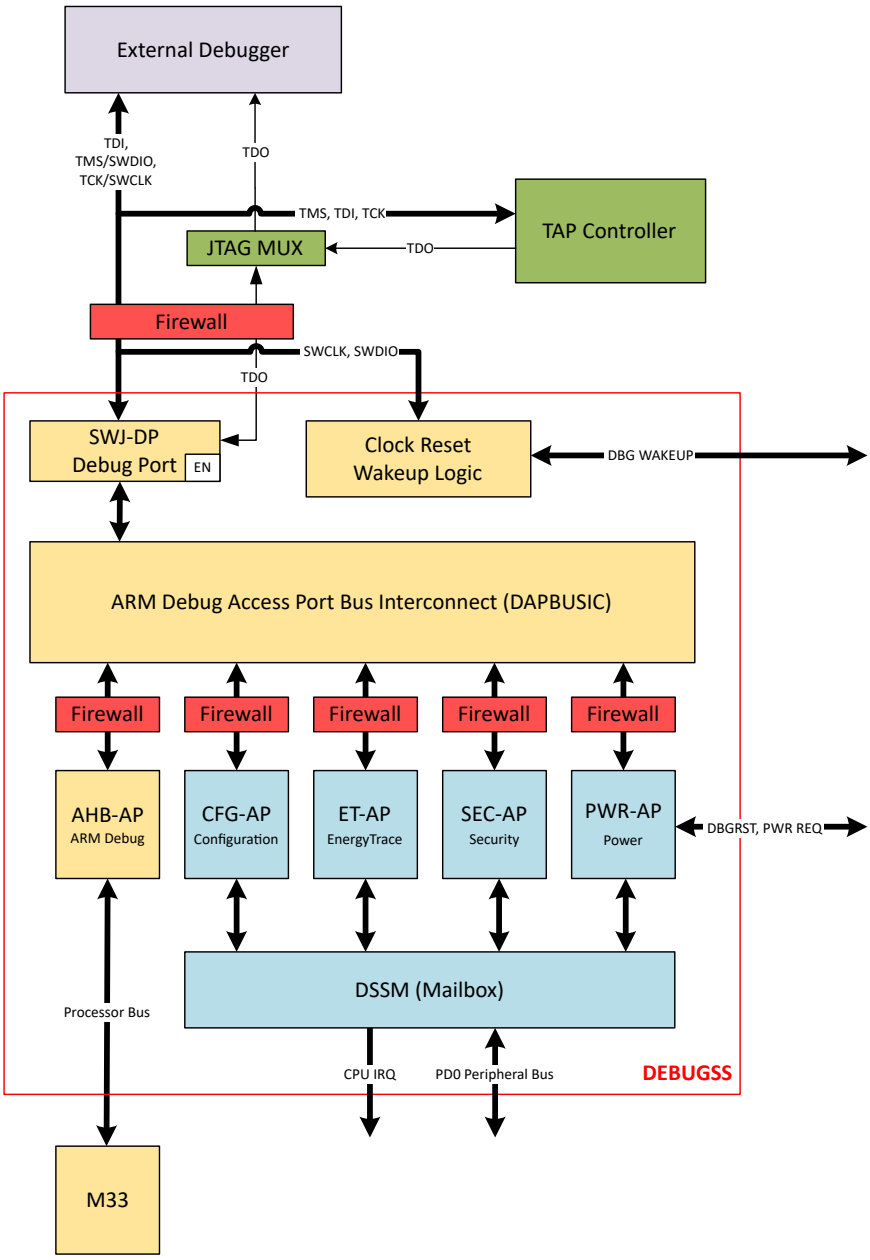


Figure 35-1. Debug Subsystem Block Diagram

The debug probe's physical interface interacts with the Arm Serial Wire Debug and JTAG Debug Port (SWJ-DP) to gain access to the debug access port bus interconnect (DAPBUSIC) when the SWJ-DP is enabled. The

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SWJ-DP is a combined JTAG-DP and SW-DP, enabling access to either a SWD or JTAG probe to a target. From TI, devices ship with the SWJ-DP enabled to allow debug access to the device for development and production programming, but the SWJ-DP can be configured to be permanently disabled through the boot configuration policy (see Section 35.2.3).

The DAPBUSIC enables a debug probe to access one or more debug Access Ports (APs). For a debug probe to be able to communicate with an access port, the SWJ-DP debug port must not be disabled by the device boot configuration policy, and the target access port must also not be disabled by the boot configuration policy. The available access ports are given in Section 35.1.3 .

The SWD/JTAG and SWJ-DP also contain signaling to the PMCU module to support debug-generated resets and operating mode changes (see Section 35.2.2).

35.1.2 Physical Interfaces

The debug port is the physical interface to access the DEBUGSS. This interface controls any access ports provided within the DEBUGSS. The DEBUGSS supports a combined debug port (SWJ-DP) which includes both JTAG and Serial Wire Debug (SWD), with a mechanism that supports switching between them:

1. The JTAG-DP is based on the IEEE 1149.1 Test Access Port (TAP) and Boundary Scan Architecture, widely referred to as JTAG, and provides a JTAG interface to the DEBUGSS. For more information, see JTAG-DP
2. The SW-DP provides a two-pin (clock + data) interface to the DEBUGSS. For more information, see SW-DP

The SWJ-DP provides the auto-detect logic that selects between JTAG and SWD. This enables the JTAG-DP and SW-DP to share the same pins. For more information, see SWJ-DP.

Note

Only one debug port can be used at once. Switching between the two debug ports must only be performed when neither debug port is in use.

35.1.2.1 JTAG Debug Port (JTAG-DP)

By default on POR, debug connections are routed to a JTAG compliant interface known as JTAG-DP. The JTAG-DP interface requires four connections:

- Test Data In (TDI) input to target device which provides a stream of serial data from debug probe
  - TDI must be pulled high on the target to keep the signal inactive when no debug probe is connected
- Test Mode Select (TMS) input to target device which controls the JTAG state-machine
  - TMS must be pulled high on the target to keep the signal inactive when no debug probe is connected
- Test Clock (TCK) input to target device which synchronizes the JTAG state-machine on each rising edge of the TCK signal, sampling the TDI and TMS signals
  - TCK can be pulled high on the target, however, to maintain full compatibility with other JTAG equipment, Arm recommends TCK is pulled low
- Test Data Out (TDO) output from target device which returns a stream of serial data to the debug unit
  - TDO can be left floating on the target, however, to maintain full compatibility with other JTAG equipment, Arm recommends TDO is pulled high

The JTAG interface uses the standard logic levels of the device for JTAG communication. See the device-specific data sheet for input and output logic levels for a given supply voltage (VDD). A TCK frequency of up to 40MHz is supported by the DEBUGSS.

During JTAG operation, the TMS/TDI/TCK line can be driven high or low by the debug probe while the TDO line can be driven high or low by the target device. The primary purpose of the pullup resistors on the TMS/TDI/TDO pins and the pulldown on TCK is to put the signals into a known state when no debug probe is attached. A minimum resistance of 100kΩ is recommended by Arm. The internal pullup/pulldown resistors fulfill this requirement and external resistors are not required for correct operation of the JTAG interface.

After a power-on reset (POR), AM13E232x devices configure the JTAG pins in JTAG mode with an internal pullup resistor enabled on the TMS/TDI/TDO lines and internal pullup enabled on the TCK line. If the device

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configuration has not permanently disabled all JTAG access, then the JTAG interface is enabled during the boot process and a debug probe can be connected to the DEBUGSS.

35.1.2.2 Serial Wire Debug (SWD) Debug Port (SW-DP)

Debug connections to the device are also supported through an Arm Serial Wire Debug (SWD) compliant interface known as the SW-DP. The SW-DP interface requires two connections:

- A bidirectional data line (SWDIO) used to send data to, and receive data from, the device
- A unidirectional clock line (SWCLK) driven by the debug probe connecting to the device

The SWD interface uses the standard logic levels of the device for SWD communication. See the device-specific data sheet for input and output logic levels for a given supply voltage (VDD). A SWCLK frequency of up to 40MHz is supported by the DEBUGSS.

During SWD operation, the SWDIO line can be driven high or driven low by either the target device or the debug probe. As either device can drive the line, when ownership of the shared SWDIO line is switched between the device and the debug probe, undriven time slots are inserted as a part of the SWD protocol. The primary purpose of the pullup resistor on the SWDIO line, and the pulldown resistor on the SWCLK line, is to place the SWD pins into a known state when no debug probe is attached. A minimum resistance of 100kΩ is recommended by Arm. The internal pullup/pulldown resistors fulfill this requirement and external resistors are not required for correct operation of the SWD interface.

After a power-on reset (POR), AM13E232x devices configure the SWD pins in SWD mode with an internal pullup resistor enabled on the SWDIO line and an internal pulldown resistor enabled on the SWCLK line. If the device configuration has not permanently disabled all SWD access, then the SWD interface is enabled during the boot process and a debug probe can be connected to the DEBUGSS.

Upon physical connection of a debug probe, a valid JTAG-to-SWD sequence must be sent from the debug probe to the SWJ-DP on SWDIOTMS to initiate a SWD connection with the SW-DP. Once the sequence is applied and the SWD connection is established, communication with enabled debug access points is possible.

35.1.2.3 Serial Wire Debug and JTAG Debug Port (SWJ-DP)

The SWJ-DP is a combined JTAG-DP and SW-DP that interfaces directly with a SWD or JTAG probe to connect to a target by enabling access to the SW-DP or JTAG-DP blocks. The SWJ-DP interface requires four connections:

1. TDO: used for JTAG mode only
2. TDI: used for JTAG mode only
3. SWDIOTMS: used as SWDIO for SWD mode and TMS for JTAG mode
4. SWCLKTCK: used as clock signal for both SWD and JTAG modes

To make efficient use of package pins, serial wire shares, and overlays, the JTAG pins use an autodetect mechanism that switches between JTAG-DP and SW-DP depending on which probe is connected. By default on POR, the JTAG-DP is used to enable JTAG debug access. A special sequence on the SWDIOTMS pin is used to switch between JTAG-DP and SW-DP. When the switching sequence has been transmitted to the SWJ-DP, the interface behaves as a dedicated JTAG-DP or SW-DP depending upon which sequence had been performed.

35.1.2.4 Debug Wake Up and Interrupts

In the event that a device was configured by software to enter SHUTDOWN mode, and a debug probe is then connected to the SWJ-DP pins with SWCLKTCK active, wakeup logic triggers an exit from SHUTDOWN mode and cause a BOR. A debug connection can then be established to the DEBUGSS after the BOR completes. Please refer to Section 35.2.2 for additional details.

For secure applications, the software can be made aware of a debug connection by utilizing the DEBUGSS *PWRUPIFG* interrupt. When the debug probe is disconnected and the connection is lost, the *PWRDWNIFG* interrupt is asserted.

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Application software can disable the SWJ-DP interface in SYSCTL, freeing the IO to be used for GPIO functionality. Review Section 3.6.4 in SYSCTL for using the debug pins for additional functionality other than JTAG/SWD. Once software disables debug functionality, it is not possible to re-enable it other than by triggering a POR. A POR will automatically re-enable the debug functionality and put the debug pins into JTAG/SWD mode with internal pullup/pulldown resistors enabled. To re-gain debug access to a device which contains software that disables the JTAG/SWD pins at startup, the device needs to be held in a reset state with the NRST pin during a POR. This will prevent the application software from starting and will allow the debug probe to gain access to the device, at which point a mass erase DSSM command can be sent from the integrated development environment to the device by the debug probe to remove the application software which is disabling the JTAG/SWD pins.

Note

BOR, BOOTRST, and SYSRST levels do reset the IOMUX logic, which will re-enable the pullup/pulldown resistors on the JTAG/SWD pins. However, the JTAG/SWD functionality remains disabled until the next POR. Because the device always powers up with the pullup and pulldown resistors enabled, the hardware design must accommodate this when using the JTAG/SWD pins for functions other than JTAG/SWD after startup. After reset, application software may disable the pullup/pulldown resistors in the IOMUX to free the JTAG/SWD pins for other purposes.

35.1.3 Debug Access Ports

The debug access ports in the DEBUGSS are given in Table 35-1.

Table 35-1. DEBUGSS Access Port Listing

APSEL	AP	Port Description	Purpose
0x0	AHB-AP	CPUSS debug access port	Debug of the processor and peripherals
0x1	CFG-AP	Configuration access port	Access device type information
0x2	SEC-AP	Security access port	Communicate with boot code and access device security information
0x3	ET-AP	EnergyTrace™ technology access port	Read the power state data from EnergyTrace technology for power aware debug
0x4	PWR-AP	Power access port	Configure the device power states (interfaces with PMCU/SYSCTL)

The AHB-AP, PWR-AP, and ET-AP provide the complete device debug functionality (processor debug, peripheral and memory bus access, power state control, and processor state). See Section 35.2.1 for more information.

The CFG-AP provides device information to the debug probe so that the debug probe can identify device characteristics, including the device part number and the device revision.

The SEC-AP provides access to the mailbox for communicating with software running on the device through JTAG/SWD. See Section 35.2.4 for more information.

35.2 DEBUGSS Operation

The features and behaviors of the DEBUGSS module is discussed in the following sections.

35.2.1 Debug Features

The DEBUGSS supports processor debug, processor trace, peripheral debug, and energy state debug.

35.2.1.1 Processor Debug

The Arm Cortex-M33 processor supports a wide range of features to simplify debugging of application software during development. Key features supported by AM13E230x MCUs include:

- Ability to halt the processor through a assertion of a halt signal, a configured debug event (such as a hard fault entry or reset), or a BKPT instruction (for software breakpoints)
- Ability to step through instructions (with or without peripheral interrupts enabled)
- Ability to run through instructions (with or without peripheral interrupts enabled)
- Ability to read and write CPU registers when halted

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- Ability to read exception information through the Cortex-M33 System Control Space (SCS)
- Support for up to 8 hardware breakpoints
- Support for up to 4 hardware watchpoints
- Support for accessing the device memory map
- Support for Micro Trace Buffer (MTB) up to 4 jump locations

35.2.1.1.1 Breakpoint Unit (BPU)

The breakpoint unit (BPU) provides up to 8 comparators which can be used to generate a debug event when the address of an instruction fetch matches the address programmed into the respective BPU comparator.

The BPU does not generate a debug event upon an address match for a data read or data write access.

Address matching is possible for half-word (16-bit) instructions and word (32-bit) instructions fetched from the CODE region (0x0000_0000 to 0x1FFF_FFFF).

If a debug scenario requires more than the supported hardware breakpoints, software breakpoints can be used together with hardware breakpoints using the BKPT instruction. If debugging of code in the SRAM region is desired, hardware breakpoints are not available and software breakpoints must be inserted by the debug probe instead.

```
// Example of a breakpoint function in C (TI Arm CLANG compiler)
__BKPT(0);
```

Note

For more information, please refer to the ARM Cortex-M33 Processor Technical Reference Manual.

35.2.1.1.2 Data Watchpoint and Trace Unit (DWT)

The data watchpoint and trace unit (DWT) provides up to 4 comparators which both support generating an event upon a data address match (watchpoint event) or an instruction address match (PC watchpoint event).

The DWT comparators support masking of the address, enabling an event to be generated when the processor attempts to access an address within a specified address range.

Note

For more information, please refer to the ARM Cortex-M33 Processor Technical Reference Manual.

35.2.1.1.3 Processor Trace (MTB)

AM13E230x devices support basic instruction execution trace to obtain context for the sequence of execution which led to a certain state of the processor. The processor trace engine is based on the Arm CoreSight MTB-M33 Micro Trace Buffer (MTB).

The MTB captures the processor's program counter (PC) state when the PC changes in a nonsequential way due to a branch instruction or an exception. Load and store activity is not captured by the MTB. When nonsequential execution is detected by the MTB, the change is captured and stored into a small buffer memory (described in Table 35-2) which can be read out later by application software or the debug probe.

Note

For more information, please refer to the ARM CoreSight MTB-M33 Technical Reference Manual.

Table 35-2. MTB Buffer Memory

Start Address	End Address	Length
0x4040_3000	0x4040_301F	32B (4 trace packets)

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35.2.1.1.4 External Trace (ETM)

AM13E230x devices integrate a single Embedded Trace Macrocell (ETM) that streams a full-instruction program-counter trace together with a 64-bit cycle-accurate timestamp counter. The ETM can be enabled by unlocking the debug registers, setting the ETM control register to enable instruction tracing (and optionally the TSCR bit for timestamps), optionally applying address-range filters to limit bandwidth, and then routing the trace pins or the on-chip Trace Port Interface Unit (TPIU) output to a CoreSight-compatible external debugger, which captures the PC-plus-timestamp stream for precise execution-time reconstruction.

Note

For more information, please refer to the ARM CoreSight ETM-M33 Technical Reference Manual.

Table 35-3. ETM Memory

Base Address	Aperture Size	Notes
0x4004_1000	0x1000	Contains control, status, filter, and the 64-bit timestamp registers; accessed via the standard programmer's model for configuration and run-time

35.2.1.2 Peripheral Debug

In addition to processor debug, the DEBUGSS can be used to access the device memory map from the perspective of the processor. Thus, a connected debug probe can be used to read and write memory-mapped peripheral registers, the system SRAM, and the flash memory.

Certain peripherals support advanced debug configuration options. These options are configured by application software (or optionally, the debug probe) by setting/clearing various debug control bits in the memory map of a given peripheral. In general, the debug behavior of a particular peripheral is specified in the PDBGCTL register of each peripheral. Many peripherals offer the option of halting the functional clock to the peripheral when the processor is halted for debug, thus pausing the peripheral together with the processor (default configuration), or letting the peripheral run even when the processor is halted for debug.

For example, the WWDT peripheral supports the FREE bit in the PDBGCTL register. Setting the FREE bit in PDBGCTL for a WWDT causes the WWDT counter to run even if the processor is halted for debug. This results in the watchdog not being serviced (causing an interrupt or reset).

35.2.1.3 EnergyTrace Technology

The DEBUGSS in AM13E230x devices support EnergyTrace technology. EnergyTrace technology enables power profiling of MCU devices running application code. This is very useful when developing an application which must be optimized for low-power operation.

Development tools from Texas Instruments, including the AM13E230x LaunchPad development tools, support hardware energy measurement of the target AM13E230x over time through EnergyTrace charge counting. This mechanism enables a developer to obtain an energy usage profile for an application, based on real current measurements with a wide dynamic range.

To give context to the energy measurements made by the hardware development tools supporting EnergyTrace technology, AM13E230x MCUs also enable EnergyTrace+. EnergyTrace+ is a component of the DEBUGSS that lets the debug probe log the state of the processor (RUN, SLEEP) and the current program counter value while the device is running. This state information can be then overlaid with energy measurements to determine if the cause of high current is the processor running or some other activity on the device.

TI's Code Composer Studio integrated development environment provides out-of-the-box support for EnergyTrace energy measurement and EnergyTrace+ processor state logging with AM13E230x devices.

Note

EnergyTrace+ state logging is not supported in SHUTDOWN mode, however the energy profiling function of EnergyTrace is still functional

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35.2.2 Behavior in Low Power Modes

The DEBUGSS supports maintaining a debug connection through SWD/JTAG in all operating modes except SHUTDOWN. In SHUTDOWN mode, the DEBUGSS supports wakeup of the device to regain full access only via SWD connection.

By default access to device memory and peripherals is possible in RUN mode and SLEEP mode, in which a debug probe can be actively connected to the AHB-AP access port to interface with the processor. In STOP and STANDBY modes, a debug connection can be established and/or maintained with the DEBUGSS, but not with the CPU debug access port. The PWR-AP of the DEBUGSS allows an overwrite of the default behavior to keep access to the processor interface established while being in STOP or STANDBY mode.

In SHUTDOWN mode, any active debug connection is terminated as the debug logic is powered down with the device VCORE. While a debug connection to the DEBUGSS is not possible while the device is in SHUTDOWN mode, a debug probe can cause the device to exit SHUTDOWN mode by attempting to communicate with the SWD pins. The device detects any attempted SWD debug requests even when the device is in SHUTDOWN. If activity is detected, a SHUTDOWN exit is initiated and the device transitions through a BOR state, after which a debug connection can be made to the DEBUGSS through SWD/JTAG.

The DEBUGSS functionality by operating mode is given in Table 35-4.

Table 35-4. DEBUGSS Functionality by Operating Mode

Capability	RUN	SLEEP	STOP	STANDBY	SHUTDOWN	NRST HOLD
Processor debug	Y	Y	N	N	N	N
Memory map access	Y	Y	N	N	N	N
Debug status through SWJ-DP	Y	Y	Y	Y	N	Y
Debug state maintained	Y	Y	Y	Y	N	N
Wake from SWD	-	-	-	-	Y	-

35.2.3 Restricting Debug Access

The DEBUGSS supports several methods for restricting access to the device through the SWD/JTAG interface. The debug access policy is determined by the user configuration specified in the NONMAIN flash region.

There are 4 levels of access control, given in Table 35-5. By default, products shipped from TI arrive in a "Debug Enabled" state where the device is fully open. This state is not recommended for production. For production, TI recommends changing the debug configuration to password protected, debug disabled, or SWD/JTAG disabled.

Table 35-5. Debug Access Control

DEBUGSS Function	Debug Configuration			
	Debug Enabled (default)	Debug Enabled with Password	Debug Disabled	SWD/JTAG Disabled
SWJ-DP (debug port)	EN	EN	EN	DIS
CFG-AP	EN	EN	EN	DIS
SEC-AP	EN	EN	EN	DIS
ET-AP	EN	EN w/ Password	DIS	DIS
AHB-AP (CPU Debug)	EN	EN w/ Password	DIS	DIS

The debug access control can be configured by writing predefined values into the NONMAIN BOOTCFG0.

Table 35-6. Debug Access Control Settings for BOOTCFG0

Debug Configuration	SWJDP_MODE	DEBUGACCESS
Debug Enabled (default)	AABBh	AABBh
Debug Enabled with Password	AABBh	CCDDh
Debug Disabled	AABBh	5566h

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Table 35-6. Debug Access Control Settings for BOOTCFG0 (continued)

Debug Configuration	SWJDP_MODE	DEBUGACCESS
SWD Disabled	5566h	5566h

When debug is set to enabled with password, the debug access command together with the user-specified debug access password must be provided to the DEBUGSS mailbox, and a BOOTRST must be issued. The password for access control is stored in NONMAIN utilizing the PWDDEBUGLOCK registers. On AM13E232x devices, the password can either be:

1. 128-bit plain text
   a. Simple password match flow, common for all devices
2. 128-bit AES encryption of the DEVICE_UID
   a. Unique password for each device
3. 128-bit CMAC signature of the DEVICE_UID
   a. Unique password for each device

When debug is disabled, the SWJ-DP is disabled during the boot process and any commands previously sent to the mailbox are ignored during boot. Following boot, any attempt to connect to the SWJ-DP is ignored.

Permanently lock debug access to the device by configuring the NONMAIN flash region to disable debug access while also configuring the NONMAIN flash region as statically write protected (locked). Locking the NONMAIN configuration has the added security of preventing the bootstrap loader (BSL) and application code from changing the debug security policy.

Table 35-7. Debug related password registers

Debug Function	Debug Access Control	Factory Reset	Mass Erase
Register Name	PWDDEBUGLOCK	PWDFACTORYRESET	PWDMASSERASE

Example: 128-bit plain text password

To enable a password on a debug function write a 128-bit hex value split into four 32-bit words into the respective password register.

Example: Factory Reset Password Configuration

1. Create 128-bit hex value
   a. 0xCAFECAFE12345678A5A5C3C30000FFFF
2. Split the 128-bit value into four 32-bit words and write the value into the respective registers
   a. PWDFACTORYRESET[0]←0x0000FFFF
   b. PWDFACTORYRESET[1]←0xA5A5C3C3
   c. PWDFACTORYRESET[2]←0x12345678
   d. PWDFACTORYRESET[3]←0xCAFECAFE
3. Repeat the same steps for any function that needs password protection

35.2.4 Mailbox (DSSM)

The Debug Subsystem Mailbox (DSSM) enables a debug probe to pass messages to the target device through the SWJ-DP interface, as well as making it possible for the target device to return data to the debug probe.

The DSSM supports the following functions:

- Transmission of commands to the device during boot, including authenticating the debug probe for password-protected debug, mass erase, and factory reset operations

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- Communicating with application software running on the target device when no other communication interface is present

Two 32-bit word data buffers are provided for TX data (debug probe to target device) and RX data (target device to debug probe). These data buffers are implemented as 32-bit memory-mapped registers in the DEBUGSS. In addition, TXCTL and RXCTL registers are provided for enabling flow control and indicating status of the mailbox.

Table 35-8. DSSM Register Functions

DSSM Register	Description	Debug Probe	Target Device	Actions
TX_DATA	Data buffer	RW	R	TXCTL.TRANSMIT is set on write by the debug probe, and cleared on a read by the target device; TXIFG is also set on a write by the debug probe
TXCTL	Flow control and status	RW	R	None
RX_DATA	Data buffer	R	RW	RXCTL.RECEIVE is set on write by the target device, and cleared on a read by the debug probe; RXIFG is also set on a write by the target device
RXCTL	Flow control and status	R	RW	None

The TXCTL and RXCTL registers provide generic transmit and receive flags. BIT0 of the TXCTL and RXCTL registers provide a specific TRANSMIT and RECEIVE flag which indicate the status of the TX_DATA and RX_DATA. The TRANSMIT bit is set in the TXCTL register when a debug probe writes data to the TX_DATA buffer register. The TRANSMIT flag will then remain set until the CPU in the target device reads TX_DATA or a POR occurs. The RECEIVE flag is set in the RXCTL register when the CPU in the target device writes data to the RX_DATA buffer register. The RECEIVE flag will then remain set until the debug probe reads the data from RX_DATA.

It is not possible for software running on the target device to write to TX_DATA, and it is also not possible for target software to clear the TRANSMIT flag other than by reading TX_DATA.

The upper 31 bits of the TXCTL register, TRANSMIT_FLAGS, contain generic flag bits which can be set or cleared by the debug probe to implement a protocol if desired. Only the debug probe can write to the TRANSMIT_FLAGS field in TXCTL. The Table 35-10 is an example of a protocol to communicate with the target device. Also refer to Boot Configuration (TBD: M33 chapter) for security level control related to the DSSM commands.

In a similar way, only the target device software can write to RX_DATA and RXCTL. The debug probe cannot write to RX_DATA and it can only clear the RECEIVE flag in RXCTL by reading RX_DATA. BIT1 through BIT7 (0xFE) of RXCTL contains the RECEIVE_FLAGS field. Software on the target device can set or clear bits in the RECEIVE_FLAGS field to implement a protocol if desired. These flags can be read by the debug probe but can not be modified by the debug probe.

Table 35-9. DEBUGSS SEC-AP Register Definition

AP SEL	ADDR	BANK	INDEX	REGISTER NAME	BIT 31 - 8	BIT 7 - 1	BIT 0
2	0x00	0	0	TXDATA	TX DATA		
	0x04	0	1	TXCTL	TRANSMIT_FLAGS		TRANSMIT
	0x08	0	2	RXDATA	RX Data		
	0x0C	0	3	RXCTL	Reserved	RECEIVE_FLAGS	RECEIVE
	0x0FC	15	3	IDR	Access point ID		

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35.2.4.1 DSSM Commands

DSSM commands are serviced by the bootcode upon a BOOTRST. If passwords are enabled for DSSM commands, the commands do not execute until the correct password sequence is entered. Refer to Table 35-10for possible DSSM commands and values.

Table 35-10. DSSM Commands

DSSM Command	Command ID
Wait For Debug	0x03
Invoke BSL	0x04
Factory Reset	0x05
Mass Erase	0x06
Command Debug	0x07
Get Lifecycle	0x0A
Get Device ID	0x0B
Key Provisioning	0x0E
Convert Bad Device	0x15
Update Active Key Revision	0x16
Update Application Revision	0x17
Data Exchange	0x77

Invoke BSL

The "Invoke BSL" command invokes the BSL instead of using GPIO.

Factory Reset

The "Factory Reset" command erases all contents within MAIN and NONMAIN flash memory. Then NONMAIN memory is re-populated with default contents. This command is useful in the cases of:

- NONMAIN misconfiguration
- Disabled debug access
- Peripheral/device misconfiguration

Factory reset has requires a configuration and password, please refer to Section 5.3.1.1 for security level details.

Note

The factory reset restores the NONMAIN configuration memory and therefore all previous security level settings are lost.

Mass Erase

The "Mass Erase" command erases all contents within the MAIN memory but NONMAIN remains untouched. This command is useful in the case of:

- Peripheral/device misconfiguration

Command Debug

The "Command Debug" command allows debugger access for a session when debug is locked.

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Data Exchange

Data exchange is the only DSSM command that does not require a BOOTRST to process the command. This command is used in combination with factory reset, mass erase, or password authentication which do require a password. After sending the initial command to the mailbox and performing a reset, the user must begin sending the password to the TXDATA register. After each word 0x77 must be written to the TXCTL register.

Wait for Debug

The "Wait for Debug" command resets the peripherals defined by the reset level and then forces the device into the reset handler.

Get Lifecycle

The "Get Lifecycle" command returns the current lifecycle of the device.

Get Device ID

The "Get Device ID" command returns the unique ID of the device.

Key Provisioning

The "Key Provisioning" command provisions AES keys into NONMAIN memory.

Convert Bad Device

The "Convert Bad Device" command designates a device as decommissioned.

Update Active Key Revision

The "Update Active Key Revision" command updates the key revision and changes the active key.

Update Application Revision

The "Update Application Revision" command updates the application revision.

Custom DSSM Command

The user can also create a custom DSSM command and perform actions defined by the user. This is done by having the debugger communicate to the M33 core through the TXDATA and TXCTL registers. The core can then receive messages from the debugger and send responses back by using the RXDATA and RXCTL registers for the debugger to read. CPU interrupt events can be configured for activity seen in the TX_DATA buffer, RX_DATA buffer, and DAP connection.

35.3 DEBUGSS Interrupts & Triggers

35.3.1 CPU Interrupts (IRQs)

See the Section 4.3.1 section for more details about how to configure interrupts at the CPU level.

Table 35-11. CPU Interrupts Triggered by DEBUGSS

NVIC Interrupt Name	Peripheral Instance Name	Register Group	DEBUGSS Interrupt Configuration Registers	Description
DEBUGSS	DEBUGSS	CPU_INT	IIDX, IMASK, RIS, MIS, ISET, ICLR	DEBUGSS interrupt. Multiple OR'd, configurable source conditions.

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35.4 DEBUGSS Registers

This Section describes the DEBUGSS Registers.

35.4.1 DEBUGSS Base Address Table

Table 35-12. DEBUGSS Base Address Table

Bit Field Name		DriverLib Name	Base Address
Instance	Structure		
DebugssRegs	DEBUGSS_REGS	DEBUGSS	0x400C_7000

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35.4.2 DEBUGSS_REGS Registers

Table 35-13 lists the memory-mapped registers for the DEBUGSS_REGS registers. All register offset addresses not listed in Table 35-13 should be considered as reserved locations and the register contents should not be modified.

Table 35-13. DEBUGSS_REGS Registers

Offset	Acronym	Register Name	Group	Section
1020h	IIDX	Interrupt index	CPU_INT	Go
1028h	IMASK	Interrupt mask	CPU_INT	Go
1030h	RIS	Raw interrupt status	CPU_INT	Go
1038h	MIS	Masked interrupt status	CPU_INT	Go
1040h	ISET	Interrupt set	CPU_INT	Go
1048h	ICLR	Interrupt clear	CPU_INT	Go
10E0h	EVT_MODE	Event Mode		Go
10FCh	DESC	Module Description		Go
1100h	TXD	Transmit data register		Go
1104h	TXCTL	Transmit control register		Go
1108h	RXD	Receive data register		Go
110Ch	RXCTL	Receive control register		Go
1200h	SPECIAL_AUTH	Special enable authorization register		Go
1210h	APP_AUTH	Application CPU0 authorization register		Go

Complex bit access types are encoded to fit into small table cells. Table 35-14 shows the codes that are used for access types in this section.

Table 35-14. DEBUGSS_REGS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
WK	W K	Write Write protected by a key
Reset or Default Value		
-n		Value after reset or the default value

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1 IIDX Register (Offset = 1020h) [Reset = 00000000h] (CPU_INT)

IIDX is shown in Figure 35-2 and described in Table 35-15.

Return to the Summary Table.

This register provides the highest priority enabled interrupt index. 0xFF means no event pending. Interrupt 0x0 is the highest priority, 0x1 next highest, and 0xFE is the least priority. The priority order is fixed. However, users can implement their own prioritization schemes using other registers that expose the full set of interrupts that have occurred.
On each read, only one interrupt is indicated. On a read, the current interrupt (highest priority) is automatically cleared by the hardware and the corresponding interrupt flag in the RIS and MIS are cleared as well. After a read from the CPU (not from the debug interface), the register must be updated with the next highest priority interrupt, if none are pending, then it displays 0xFF.

Figure 35-2. IIDX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STAT							
R-0h																								R-0h							

Table 35-16. IIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	STAT	R	0h	Interrupt index status 0h = No pending interrupt request 1h = TX interrupt 2h = RX interrupt 3h = Power-up interrupt. A debug session has started. 4h = Power-up interrupt. A debug session has started.

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2 IMASK Register (Offset = 1028h) [Reset = 00000000h] (CPU_INT)

IMASK is shown in Figure 35-3 and described in Table 35-16.

Return to the Summary Table.

Interrupt Mask. If a bit is set, then corresponding interrupt is un-masked. Un-masking the interrupt causes the raw interrupt to be visible in IIDX, as well as MIS.

Figure 35-3. IMASK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PWRDWNIFG	PWRUPIFG	RXIFG	TXIFG
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 35-18. IMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	
3	PWRDWNIFG	R/W	0h	Masks PWRDWNIFG in MIS register 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
2	PWRUPIFG	R/W	0h	Masks PWRUPIFG in MIS register 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
1	RXIFG	R/W	0h	Masks RXIFG in MIS register 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set
0	TXIFG	R/W	0h	Masks TXIFG in MIS register 0h = Interrupt is masked out 1h = Interrupt will request an interrupt service routine and corresponding bit in MIS will be set

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3 RIS Register (Offset = 1030h) [Reset = 00000000h] (CPU_INT)

RIS is shown in Figure 35-4 and described in Table 35-17.

Return to the Summary Table.

Raw interrupt status. Reflects all pending interrupts, regardless of masking. The RIS register allows the user to implement a poll scheme. A flag set in this register can be cleared by writing 1 to the ICLR register bit even if the corresponding IMASK bit is not enabled.

Figure 35-4. RIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PWRDWNIFG	PWRUPIFG	RXIFG	TXIFG
R-0h				R-0h	R-0h	R-0h	R-0h

Table 35-20. RIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	PWRDWNIFG	R	0h	Raw interrupt status for PWRDWNIFG 0h = PWRUPIFG did not occur 1h = PWRUPIFG occurred
2	PWRUPIFG	R	0h	Raw interrupt status for PWRUPIFG 0h = PWRUPIFG did not occur 1h = PWRUPIFG occurred
1	RXIFG	R	0h	Raw interrupt status for RXIFG 0h = RXIFG did not occur 1h = RXIFG occurred
0	TXIFG	R	0h	Raw interrupt status for TXIFG 0h = TXIFG did not occur 1h = TXIFG occurred

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4 MIS Register (Offset = 1038h) [Reset = 00000000h] (CPU_INT)

MIS is shown in Figure 35-5 and described in Table 35-18.

Return to the Summary Table.

Masked interrupt status. This is an AND of the IMASK and RIS registers.

Figure 35-5. MIS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PWRDWNIFG	PWRUPIFG	RXIFG	TXIFG
R-0h				R-0h	R-0h	R-0h	R-0h

Table 35-22. MIS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	PWRDWNIFG	R	0h	Masked interrupt status for PWRDWNIFG 0h = PWRUPIFG did not request an interrupt service routine 1h = PWRUPIFG requests an interrupt service routine
2	PWRUPIFG	R	0h	Masked interrupt status for PWRUPIFG 0h = PWRUPIFG did not request an interrupt service routine 1h = PWRUPIFG requests an interrupt service routine
1	RXIFG	R	0h	Masked interrupt status for RXIFG 0h = RXIFG did not request an interrupt service routine 1h = RXIFG requests an interrupt service routine
0	TXIFG	R	0h	Masked interrupt status for TXIFG 0h = TXIFG did not request an interrupt service routine 1h = TXIFG requests an interrupt service routine

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5 ISET Register (Offset = 1040h) [Reset = 00000000h] (CPU_INT)

ISET is shown in Figure 35-6 and described in Table 35-19.

Return to the Summary Table.

Interrupt set. Allows interrupts to be set by software (useful in diagnostics and safety checks). Writing a 1 to a bit in ISET will set the event and therefore the related RIS bit also gets set. If the interrupt is enabled through the mask, then the corresponding MIS bit is also set.

Figure 35-6. ISET Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				PWRDWNIFG	PWRUPIFG	RXIFG	TXIFG
W-0h				W-0h	W-0h	W-0h	W-0h

Table 35-24. ISET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	PWRDWNIFG	W	0h	Sets PWRDWNIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to PWRUPIFG is set
2	PWRUPIFG	W	0h	Sets PWRUPIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to PWRUPIFG is set
1	RXIFG	W	0h	Sets RXIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to RXIFG is set
0	TXIFG	W	0h	Sets TXIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to TXIFG is set

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6 ICLR Register (Offset = 1048h) [Reset = 00000000h] (CPU_INT)

ICLR is shown in Figure 35-7 and described in Table 35-20.

Return to the Summary Table.

Interrupt clear. Write a 1 to clear corresponding Interrupt.

Figure 35-7. ICLR Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED				PWRDWNIFG	PWRUPIFG	RXIFG	TXIFG
W-0h				W-0h	W-0h	W-0h	W-0h

Table 35-26. ICLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	0h	
3	PWRDWNIFG	W	0h	Clears PWRDWNIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to PWRUPIFG is cleared
2	PWRUPIFG	W	0h	Clears PWRUPIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to PWRUPIFG is cleared
1	RXIFG	W	0h	Clears RXIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to RXIFG is cleared
0	TXIFG	W	0h	Clears TXIFG in RIS register 0h = Writing a 0 has no effect 1h = RIS bit corresponding to TXIFG is cleared

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7 EVT_MODE Register (Offset = 10E0h) [Reset = 00000000h]

EVT_MODE is shown in Figure 35-8 and described in Table 35-21.

Return to the Summary Table.

Event mode register. It is used to select whether each line is disabled, in software mode (software clears the RIS) or in hardware mode (hardware clears the RIS)

Figure 35-8. EVT_MODE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						INT0_CFG	
R-0h						R-0h	

Table 35-28. EVT_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	
1-0	INT0_CFG	R	1h	Event line mode select for peripheral events 0h = The interrupt or event line is disabled. 1h = The interrupt or event line is in software mode. Software must clear the RIS. 2h = The interrupt or event line is in hardware mode. The hardware (another module) clears automatically the associated RIS flag.

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8 DESC Register (Offset = 10FCh) [Reset = 00000000h]

DESC is shown in Figure 35-9 and described in Table 35-22.

Return to the Summary Table.

This register identifies the peripheral and its exact version.

Figure 35-9. DESC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULEID															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEATUREVER				INSTNUM				MAJREV				MINREV			
R-0h				R-0h				R-0h				R-0h			

Table 35-30. DESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULEID	R	340h	Module identification contains a unique peripheral identification number. The assignments are maintained in a central database for all of the platform modules to ensure uniqueness.
15-12	FEATUREVER	R	0h	Feature Set for the module *instance*
11-8	INSTNUM	R	0h	Instance Number within the device. This will be a parameter to the RTL for modules that can have multiple instances
7-4	MAJREV	R	0h	Major rev of the IP
3-0	MINREV	R	0h	Minor rev of the IP

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9 TXD Register (Offset = 1100h) [Reset = 00000000h]

TXD is shown in Figure 35-10 and described in Table 35-23.

Return to the Summary Table.

This register is used for data transfers from external debug tools to the DSSM module. The register is written by the debug tool and read by the CPU.

Figure 35-10. TXD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_DATA																															
R-0h																															

Table 35-32. TXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_DATA	R	0h	Contains data written by an external debug tool to the SEC-AP TXDATA register

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10 TXCTL Register (Offset = 1104h) [Reset = 00000000h]

TXCTL is shown in Figure 35-11 and described in Table 35-24.

Return to the Summary Table.

Transmit control register

Figure 35-11. TXCTL Register

31	30	29	28	27	26	25	24
TRANSMIT_FLAGS							
R-0h							
23	22	21	20	19	18	17	16
TRANSMIT_FLAGS							
R-0h							
15	14	13	12	11	10	9	8
TRANSMIT_FLAGS							
R-0h							
7	6	5	4	3	2	1	0
TRANSMIT_FLAGS							TRANSMIT
R-0h							R-0h

Table 35-34. TXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	TRANSMIT_FLAGS	R	0h	Generic TX flags that can be set by external debug tool. Functionality is defined by SW.
0	TRANSMIT	R	0h	Indicates data request in DSSM.TXD, set on write via Debug AP to DSSM.TXD. A read of the DSSM.TXD register by SW will clear the TX field. The tool can check that TXD is empty by reading this field. 0h = TXD is empty 1h = TXD is full

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11 RXD Register (Offset = 1108h) [Reset = 00000000h]

RXD is shown in Figure 35-12 and described in Table 35-25.

Return to the Summary Table.

Receive data register. This register contains the data written by the CPU.
This data is read by external debug tool.

Figure 35-12. RXD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_DATA																															
R/W-0h																															

Table 35-36. RXD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_DATA	R/W	0h	Contains data written by SM/OW.

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12 RXCTL Register (Offset = 110Ch) [Reset = 00000000h]

RXCTL is shown in Figure 35-13 and described in Table 35-26.

Return to the Summary Table.

Receive control register

Figure 35-13. RXCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RECEIVE_FLAGS							RECEIVE
R/W-0h							R-0h

Table 35-38. RXCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	0h	
7-1	RECEIVE_FLAGS	R/W	0h	Generic RX flags that can be set by SW and read by external debug tool. Functionality is defined by SW.
0	RECEIVE	R	0h	Indicates SW write to the DSSM.RXD register. A read of the DSSM.RXD register by SWD Access Port will clear the RX field. 0h = RXD empty 1h = RXD full

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13 SPECIAL_AUTH Register (Offset = 1200h) [Reset = 00000013h]

SPECIAL_AUTH is shown in Figure 35-14 and described in Table 35-27.

Return to the Summary Table.

This register is used to control ET-AP, DFT-TAP, SWD, CFG-AP and SEC-AP.

Figure 35-14. SPECIAL_AUTH Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	PWRAPEN	AHBAPEN	CFGAPEN	ETAPEN	DFTAPEN	SWDPORTEN	SECAPEN
R-0h	R-0h	R-0h	R-1h	R-0h	R-0h	R-1h	R-1h

Table 35-40. SPECIAL_AUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	
6	PWRAPEN	R	0h	An active high input. When asserted (and SWD access is also permitted), the debug tools can then access the PWR-AP to power and reset state of the CPU. When deasserted, a DAPBUS firewall will isolate the AP and prevent access. 0h = Disable PWR-AP 1h = Enable PWR-AP
5	AHBAPEN	R	0h	Disabling / enabling debug access to the M0+ Core via the AHB-AP DAP bus isolation. 0h = Disable AHB-AP 1h = Enable AHB-AP
4	CFGAPEN	R	1h	An active high input. When asserted (and SWD access is also permitted), the debug tools can use the Config-AP to read device configuration information. When deasserted, a DAPBUS firewall will isolate the AP and prevent access to the Config-AP. 0h = Disable CFG-AP 1h = Enable CFG-AP
3	ETAPEN	R	0h	An active high input. When asserted (and SWD access is also permitted), the debug tools can then access an ET-AP external to the DebugSS lite. When deasserted, a DAPBUS firewall will isolate the AP and prevent access. 0h = Disable ET+ -AP 1h = Enable ET+ -AP
2	DFTAPEN	R	0h	An active high input. When asserted (and SWD access is also permitted), the debug tools can then access the DFT-AP external to the DebugSS lite. When deasserted, a DAPBUS firewall will isolate the AP and prevent access. 0h = Disable DFT-TAP 1h = Enable DFT-TAP
1	SWDPORTEN	R	1h	When asserted, the SW-DP functions normally. When deasserted, the SW-DP effectively disables all external debug access. 0h = Disable SWD port 1h = Enable SWD port

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Table 35-40. SPECIAL_AUTH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SECAPEN	R	1h	An active high input. When asserted (and SWD access is also permitted), the debug tools can use the Security-AP to communicate with security control logic. When deasserted, a DAPBUS firewall will isolate the AP and prevent access to the Security-AP. 0h = Disable SEC-AP 1h = Enable SEC-AP

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14 APP_AUTH Register (Offset = 1210h) [Reset = 00000000h]

APP_AUTH is shown in Figure 35-15 and described in Table 35-28.

Return to the Summary Table.

This register is used to control DBGEN, NIDEN, SPIDEN, and SPNIDEN of Application CPU0. DBGEN, NIDEN are further processed by DSW based on Active and Debug IPF ID.

Figure 35-15. APP_AUTH Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				SPNIDEN	SPIDEN	NIDEN	DBGEN
R-0h				R-0h	R-0h	R-0h	R-0h

Table 35-42. APP_AUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	
3	SPNIDEN	R	0h	Secure non-invasive debug enable. 0h = Invasive debug disabled 1h = Invasive debug enabled
2	SPIDEN	R	0h	Secure invasive debug enable. 0h = Invasive debug disabled 1h = Invasive debug enabled
1	NIDEN	R	0h	Controls non-invasive debug enable. 0h = Non-invasive debug disabled 1h = Non-invasive debug enabled
0	DBGEN	R	0h	Controls invasive debug enable. 0h = Invasive debug disabled 1h = Invasive debug enabled

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36 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

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