User's Guide

Hardware Design Considerations for Custom Board Design Using AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family

TEXAS INSTRUMENTS

ABSTRACT

The *Hardware Design Considerations for Custom Board Design* user's guide provides an overview of the design considerations that are recommended to be followed by the custom board designers while designing custom boards using AM625, AM623, AM620-Q1, AM625-Q1 and AM625SIP processor family. The user's guide can be used as guidelines at different phases of custom board design (by custom board designers).

Additionally, links (TI.com product page) are provided to processor product pages, processor related collaterals, FAQs related to processor and processor peripherals published on E2E, and commonly referenced documents during custom board design. The custom board designers can refer to the links during custom board design to minimize design errors, optimize the design efforts, reduce board build iterations and optimize the project timeline.

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1 Introduction

The *Hardware Design Considerations for Custom Board Design Using AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family* can be used as a starting point by custom board designers designing custom board using any of the above listed processors. The user's guide provides an overview of the design flow at different phases of custom board design and highlights important design requirements that are recommended to be addressed. Note that the user's guide does not include all the information required to complete the custom board design. In many cases, the document refers to the device-specific collaterals and various other documents for specific information.

The user's guide has been organized as a sequence of sections. The user's guide starts with decisions that are required to be made during the planning phase of the custom board design, selection of processor and attached devices, electrical and thermal requirements. Recommendations discussed in each of the section are recommended to be addressed before moving to the next section.

Note

The user's guide is applicable to ALW (for AM625, AM623 processor GPNs), AMC (for AM620-Q1, AM625-Q1 processor GPNs) and AMK (for AM625SIP processor GPN) packages.

The user's guide can be used for ALW Q1 processor package. The user's guide does not cover all aspects or phases of custom board design.

Note

The processor family has capabilities to address safety requirements.

The focus of the user's guide is non-safety applications.

1.1 Before Getting Started With the Custom Board Design

The processor family includes a number of peripherals supporting multiple functions (memory, communication) and processing capabilities (all the peripherals and processing capabilities may not used in all the custom board designs). The functional and performance requirements for different custom board designs using the same processor can vary depending on the end application. Custom board designers are expected to understand the requirements before selecting the processor and determining the board level implementation requirements. Additional circuitry can be added to the custom board design to enhance functionality and operate correctly in the end application operating environment. For selecting the processor OPN and to finalize the below key requirements, see the device-specific data sheet, silicon errata, TRM, hardware design considerations for custom board design, schematic design guidelines and schematic review checklist, and SK collaterals (latest, recommendation is to frequently check for updates to collaterals on TI.com):

- Expected operating conditions for the processor, target boot mode, storage type and interfaces
- Processing (performance) requirements for each of the core in the selected processor
- External or integrated LPDDR4 memory
- External DDR memory type (DDR4 or LPDDR4), width, speed, size
- Processor peripherals used (interfaced to the attached devices)

During the custom board design, as a starting point for information on key devices (components) used on the EVMs and SKs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

1.2 Processor-Specific SDK

In case the project is to design a new board or platform, the recommendation is to use the latest Version/ Revision of the software development tools.

Refer below link to download the required SDK version:

PROCESSOR-SDK-AM62x

1. ***MCU-PLUS-SDK-AM62x:*** MCU+ SDK for AM62x – RTOS, No-RTOS
2. ***PROCESSOR-SDK-LINUX-AM62x:*** : Processor SDK Linux for AM62x

Refer to *AM62x Software Build Sheet* (Build Sheet of supported features for AM62x processor family).

In case an older Version/Revision is being used, the recommendation is to verify the compatibility using the release notes or reach out to TI (through E2E).

1.3 Peripheral Circuit Implementation - Compatibility Between Processor Families

During custom board design, when implementing the required functionality (circuit) for peripheral interfaces, memory interface and IO interfaces, the recommendation is to review and follow the processor-specific recommendations including ROC, power sequencing, IO level compatibility as per the processor-specific data sheet and other available collaterals on the product page. The interface connection requirements and circuit implementations may not be similar (or compatible) with the circuit implementations when compared to legacy Processors or MCUs (TI AM335x, AM437x or other TI processors or processors supported by other suppliers). Example peripheral interfaces include SD card interface including support for high-speed UHS-I, USB interface and IO interface implementation including reset (warm or cold) inputs or external IO interfaces (for slew rate, IO level compatibility, fail-safe operation).

1.4 Selection of Required Processor OPN (Orderable Part Number)

Selection of the required processor OPN is an important phase during custom board design. To get an overview of the processor family architecture and for selecting the required processor OPN (that can be used in the custom board) based on the required functionality and features, package (ALW, ALW in Q1 package (AM625, AM623), AMC (AM620-Q1, AM625-Q1), AMK (AM625SIP)) and speed grade, see the *Functional Block Diagram*, *Device Comparison*, *Device Naming Convention*, *Device Speed Grades* and *Packaging Information* sections of the device-specific data sheet.

See the *Device Comparison* chapter, *Device and Documentation Support* section of the device-specific data sheet to choose the required processor OPN.

Refer below FAQ to read the device ID:

[FAQ] AM625/AM623 Custom board hardware design – Reading DEVICE_ID and Unique SOC (CPU) ID

The recommendation is to update the processor OPN in the schematics with the chosen OPN.

The recommendation is to select AM625SIP processor when integrated memory (LPDDR4) is a requirement.

For the list of available packages for AM62x processor family, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A / AM62D-Q1 / AM62P / AM62L Custom board hardware design - Available Device Packages

1.4.1 Processor Support for Secure Boot and Functional Safety

The AM62x device supports secure boot for IP protection with the built-in Hardware Security Module (HSM) and employs advanced power management support for portable and power-sensitive applications. Functional Safety support is available when selecting an orderable part number that includes a Functional Safety code of F.

The recommendation is to refer to *Device Naming Convention* section of the device-specific data sheet for selection of devices that supports secure boot and/or functional safety.

The below summarizes processor type used on custom boards:

HS-FS

High Security - Field Securable: This is a SoC/board state before a customer has blown the keys in the device. i.e. the state at which HS device leaves TI factory. In this state, the device protects the ROM code, TI keys and certain security peripherals. In this state, device do not force authentication for booting, however DMSC is locked.

HS-SE

High Security - Security Enforced: This is a SoC/board state after a customer has successfully blown the keys and set “customer Keys enable”. In HS-SE device all security features enabled. All secrets within the device are fully protected and all of the security goals are fully enforced. The device also enforces secure booting.

Refer below FAQ and the SDK link below for information on secure boot support:

AM625: How user confirm HS-FS and HS-SE

Security

For information and collaterals related to functional safety, the recommendation is to reach out to the local TI sales or start an E2E for customers to support.

Refer below FAQs related for functional safety:

AM623: Please help to provide Safety Features documents for AM623

[FAQ] AM623: Functional safety certification document for AM62x, AM644x

PROCESSOR-SDK-AM62X: Request Functional Safety Documents

Follow below link for information related to the processors supporting functional safety:

Functional safety

1.4.2 Note on AM625SIP Processor Data Sheet

AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM data sheet references to *AM62x Sitara Processor* data sheet. The recommendation is to refer both (AM62x and AM625SIP) data sheets in combination when using AM625SIP processor.

1.4.3 AM625 and AM625SIP Custom Boards, Design Compatibility

The AM625SIP processor is available in AMK package. The package and the BGA pinout is similar to AM6254 processor ALW package. The AM625SIP AMK package follows the same footprint as AM6254 ALW package. Many of the AM625SIP AMK package balls have similar signal assignments (same as AM6254 ALW package).

The AM625SIP ball assignment exceptions are listed in the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

Using AM625SIP as a drop-in replacement on an existing AM625 board is NOT recommended or allowed. Design changes are required to be made for using AM625SIP.

1.5 Technical Documentation

A number of documents relevant to the selected processor (family) are available on the processor-specific product page on TI.com. The recommendation for custom board designers is to read the relevant collateral (listed in the below FAQs) before starting the custom board design.

The following FAQs summarizes the collaterals that can be referred to when starting the custom board design:

[FAQ] AM625 Custom board hardware design – Collaterals to Get started

[FAQ] AM623 Custom board hardware design – Collaterals to Get started

[FAQ] AM620-Q1 / AM625-Q1 Custom board hardware design – Collaterals to Get started

[FAQ] AM625SIP Custom board hardware design – Collaterals to Get started

1.5.1 Updated SK Schematic With Design, Review and Cad Notes Added

During custom board design, as part of the custom board design flow process, the custom board designers can reuse the SK design and make the required edits. Alternatively, custom board designers can reuse the common circuit implementations, including processor, memory and communication interfaces. Since the SK design is expected to have additional functions, custom board designers tend to optimize the SK schematic design as per the custom board requirements. While optimizing the SK schematics, errors can be introduced into the custom board design that can affect functionality, performance or reliability of the custom board. When optimizing, custom board designers can have queries regarding the SK implementation. On many of the customer board reviewed, common design and optimization errors across multiple custom board designs were observed. Based on the customer queries, customer and internal inputs, and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) have been added near each section of the SK schematic for custom board designers to review and follow to (implement to minimize errors).

Additional files as part of the design downloads have been included to support optimizing the evaluation time for the selected processor during the custom board design evaluation phase. The SK design includes the processor that support maximum functionalities.

SK-AM62B: https://www.ti.com/lit/zip/sprr481

SK-AM62B-P1: https://www.ti.com/lit/zip/spar001

SK-AM62-LP: https://www.ti.com/lit/zip/sprr471

SK-AM62-SIP: https://www.ti.com/lit/zip/sprr482

For information related to availability of ASCII (.alg) file for Altium tool, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM62Ax / AM62Px / AM62D-Q1 - .alg (ASCII) file for use with Altium tool

The available downloadable design documents are listed in the below product overview documents:

SK-AM62B Design Package Folder and Files List

SK-AM62B-P1 Design Package Content Overview

SK-AM62-LP Design Package Content Overview

SK-AM62-SIP Design Package Folder and Files List

The following FAQs include the PDF schematic (with D-Notes, R-Notes, CAD notes added) and additional information related to starter kits:

[FAQ] AM625 / AM623 Custom board hardware design - Design and Review notes for Reuse of SK-AM62B Schematics

[FAQ] AM625 / AM623 Custom board hardware design - Design and Review notes for Reuse of SK-AM62B-P1 Schematics

[FAQ] AM620-Q1 / AM625-Q1 Custom board hardware design - Design and Review notes for Reuse of SK-AM62-LP Schematics

[FAQ] AM625SIP - Custom board hardware design - Design and Review notes for Reuse of SK-AM62-SIP Schematics

1.5.2 Collaterals on TI.com, Processor Product Page

The most recently updated collaterals including the data sheet, TRM, silicon errata, hardware design considerations user's guide and schematic design guidelines and schematic review checklist are available on the product page.

Additional collaterals that are in works (being edited or reviewed) are being added (updated) to the product page and the current collaterals are also being updated on a continuous basis. The recommendation is to review the collaterals on TI.com for updated revision or new collateral additions on a regular basis.

1.5.3 Schematic Design Guidelines and Schematic Review Checklist - Processor Family Specific User's Guide

The user's guide is for AM62x processor family covering AM625, AM623, AM620-Q1, AM625-Q1 and AM625SIP processors (GPNs). Each of the processor GPN can have multiple OPNs. The user's guide includes schematic design guidelines and schematic review checklist that can be used during custom board design. Processor family specific user's guide provides processor focused guidelines and checklist and make it easy for the custom board designers to use when designing the board for a specific processor family. The user's guide is simpler and is easy to use for the chosen processor and processor family (AM62x in this case).

AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist

1.5.4 Updates to Hardware Design Considerations User's Guide

There can be changes to the *Hardware Design Considerations* user's guide with respect to the current revision published on TI.com (based on customer feedback, learnings, errors or improvements) that are updated during the next document revision.

The below FAQ lists the changes customer board designers are required to be aware and follow during custom board design before the release of the revised user's guide on TI.com:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design - Updates to Hardware Design Considerations and Schematic Design Guidelines collaterals

1.5.5 Processor and Peripherals Related FAQs to Support Custom Board Designs

Based on interactions with multiple custom board designers, queries from a number of custom board designers and learnings from queries received from custom board designers, a number of FAQs have been created (related to (detailed explanation and example illustrations added) processor functioning, processor connections, processor peripherals and interface, processor evaluation SK, common errors observed during customer board design reviews, data sheet and pin attributes and commonly asked E2E queries) to support custom board designers during the custom board design. Refer the following list of FAQs that can be used during custom board design along with other available design collaterals including *Hardware Design Considerations for Custom Board Design* and *Schematic Design Guidelines and Schematic Review Checklist*:

There is a FAQ master list that provides list of all available FAQs for the Sitara processor families:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

To make it easy for custom board designers working on a specific processor family, processor family wise FAQs have been listed:

[FAQ] AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

See the following FAQ that provides list of all the available FAQs including software related FAQs for sitara family of processors:

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

Note

The FAQs are updated frequently. The recommendation is to review the FAQs of interest on a regular basis for updated information.

1.6 Custom Board Design Documentation

The recommendation is to update custom board design documents periodically to capture the updates to custom board requirements and changes to design (observed while testing or review) during different phases of custom board design. The updated information can be the baseline for the documentation package (design document) required for review (external or internal) support.

1.7 Processor and Processor Peripherals Design Related Queries During Custom Board Design

During the custom board design, for queries related to processor and processor peripherals, the recommendation is to start an E2E query for the device experts to support. The recommendation is to include queries related to a specific section of the design or peripheral or topic in an E2E query to minimize assignment and reply delay.

2 Custom Board Design Block Diagram

Drawing a detailed block diagram, covering all the major (required) functional blocks and interfaces (to external attached devices (peripherals)) is recommended for designing a fully functional custom board.

2.1 Developing the Custom Board Design Block Diagram

The recommendation is to identify and review all the relevant end equipment use case requirements (features), functions and include all critical components (functional blocks), associated devices required for processor functioning (Example: PMIC) and include details of the attached devices interfaced to the processor as part of the block diagram. The recommendation is to draw separate blocks for each function or interface, connect blocks with arrows indicating the directions, label blocks and clearly indicate the interfaces and processor IOs used for connecting the processor and attached devices. The recommendation is to consider grouping of the blocks based on the implemented functions whenever possible. The recommendation is to review, refine and baseline the block diagram before starting the design.

The below resources can be used (as supporting documents) when preparing the detailed block diagram:

- *Starter Kit SK-AM62B-P1* (AM625 / AM623 Starter Kit EVM with PMIC), *Starter Kit SK-AM62-LP* (AM620-Q1 / AM625-Q1 starter kit for low-power Sitara processors), *Starter Kit SK-AM62-SIP* (AM62x system-in-package (AM625SIP) starter kit for Sitara processors) and any other available SKs.
- The links listed below to the processor-specific product page on TI.com includes Functional block diagrams, Data sheet, TRM, User guides, Silicon errata, Application notes, Hardware design considerations for custom board design, Schematic design guidelines and schematic review checklist, and other relevant documents. The design and development section include links to available SK (Starter Kit design files), design tools, simulation models and software. As part of information related to support and training, links to commonly viewed or searched E2E threads and E2E FAQs are available.

The processor product page links on TI.com are listed below:

AM62x [ALW]

- AM625
- AM623

AM62x [AMC]

- AM620-Q1
- AM625-Q1

AM62x [AMK]

- AM625SIP

2.2 Configuring the Boot Mode

The recommendation is to indicate the configured boot mode and the boot mode provisions provided in the block diagram including primary boot and backup boot.

For supported boot mode configurations, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62Ax / AM62Px / AM62D-Q1 / AM62L - Supported bootmode configurations

The processor family supports multiple peripheral interfaces that support boot. For the available boot mode configurations and supported peripherals, see the device-specific TRM. The processor family supports primary boot mode and an optional backup boot mode configuration. If the primary boot (source) mode fails, the ROM switches on to the backup boot mode.

Boot mode configuration to be used (by the ROM code) during boot are set by the boot mode configuration (pullup or pulldown) resistors connected to the processor boot mode inputs directly (or through external buffers). The BOOTMODE [15:0] pin configurations (level) are latched into the Device Status register CTRLMMR_MAIN_DEVSTAT[15:0] as the processor comes out of cold reset, sampled after MCU_PORz input deassertion (rising edge of PORz_OUT output (buffered output of MCU_PORz input)). The boot mode configuration inputs are recommended to be stable before releasing (deassertion) the MCU_PORz input.

Processor boot mode can be configured using discrete (parallel pull) resistors for the below boot configuration (functionality):

PLL Config (Configuration): BOOTMODE [02:00] – PLL config pins are used to indicate the system clock (PLL reference clock selection) frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration

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Note

For supported crystal frequency see the processor-specific data sheet. Configure the boot mode to match the supported crystal or clock frequency. Wrong clock frequency configuration affects the processor performance including resetting of the board.

Primary Boot Mode: BOOTMODE [06:03] – The boot mode pins are used to configure the required primary boot mode, i.e, the peripheral/memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – The boot mode configuration pins support optional configurations for primary boot and are used in conjunction with the primary boot mode selection pins

Backup Boot Mode: BOOTMODE [12:10] – The boot mode pins are used to configure the required backup boot mode, i.e., the peripheral/memory to boot from, in case primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – The boot mode pin provides additional configuration options (optional - depends on the selected backup boot mode pins)

Reserved: BOOTMODE [15:14] – Reserved pins (The recommendation is to not leave the reserved pins unconnected)

Note

Leaving BOOTMODE [15:00] pins unconnected is not recommended or allowed option.

Key considerations when configuring boot mode:

- The recommendation is to always include provision to configure boot modes used during the custom board development phase, such as USB boot (USB0, DFU), UART boot (UART0) or no-boot/Dev boot mode for debug (using JTAG)
- Boot mode pins support alternate functions that can be configured after the boot mode configuration inputs are latched. The recommendation is to take into consideration the alternate function implemented when choosing pullup or pulldown resistors during custom board design. In case the boot mode inputs are being driven by external inputs to support test automation or remote configuration, the boot mode inputs are required to return to the required boot configuration value (level) whenever the processor is reset (indicated by the PORz_OUT output pin) to allow the processor to boot correctly.
- Some of the boot mode pins functionalities are reserved. Boot mode pins marked as Reserved or not used are not recommended or allowed to be unconnected (float). The recommendation is to pull the input high or low using an external resistor. For information regarding connection of reserved boot mode pins, see the *BOOTMODE Pin Mapping* section of the *Initialization* chapter of the device-specific TRM.

For information related to supported boot modes, see the *Initialization* chapter of the device-specific TRM and device-specific silicon errata.

Note

Custom board designers are responsible for providing provision to set the required boot mode configuration (using pullups or pulldowns, or optionally using jumpers/switches (with provision for external ESD protection when set in uncontrolled ESD environment)). The recommendation is to provide provision for pullup and pulldown for the boot mode input pins that have configuration capability for increase design flexibility. Shorting of multiple boot mode input pins together, leaving any of the boot mode input pins unconnected or connecting the boot mode inputs directly to supply or ground is not recommended or allowed.

Note

The recommendation is to connect the processor boot mode input pins (configured for alternate function) to the alternate function through a 0Ω series resistor. Series resistor can be used to isolate the alternate function during testing.

For implementing the boot mode, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation with isolation buffers used

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation without isolation buffers

2.3 Configuring the Processor Pins Functionality (PinMux Configuration)

The processor family supports a number of peripherals, interfaces (memory, synchronous, asynchronous) and GPIOs. To optimize processor size, pin count and package while maximizing functionality, many of the processor pads (pins) provide provision to multiplex (up to eight) signal functions. All peripheral instances may not be configurable or used (on a specific custom board).

TI provides the SysConfig-PinMux Tool that can be used by custom board designers to configure the required functionality (peripherals, interfaces and IOs).

Note

The recommendation is to save the PinMux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

After the selection of the processor OPN and updating the block diagram to include the processor part number, the next phase of the custom board design is the power supply architecture design.

3.1 Power Supply Architecture

The power supply architectures that can be considered are listed below:

3.1.1 Integrated Power Architecture

The integrated power architecture can be based on Multi-channel ICs (PMICs) such as TPS65219 or similar.

For application notes and information on the output voltage configuration for the available OPNs and recommended connections, see the following links:

Powering the AM62x With the TPS65219 PMIC

Powering the AM625SIP With the TPS65219 PMIC

See the TPS65219 OPN specific technical reference manual (Example: *TPS6521901 Technical Reference Manual*) for information related to the NVM (output voltages and IO) configuration.

During power-down, the recommendation is for MCU_PORz input to reach a valid logic low level before the supplies begin to ramp down. The PMIC based power architecture is designed (expected) to monitor (make sure) if all power rails have been turned off and decay below 300mV before initiating a new power-up sequence anytime any of the processor power rail drops below the minimum value defined in *Recommended Operating Conditions*.

Additionally, see the following application note:

Advantages of Using TPS65219 PMIC to Power AM62 Processor Versus a Discrete Power Design

In case a non-TI PMIC is used, the recommendation for custom board designers is to review and follow the relevant processor collaterals including the device-specific data sheet and *Maximum Current Ratings* application note. The recommendation is to review the *Recommended Operating Conditions*, *Supply Slew Rate Requirements*, MCU_PORz input L->H delay (hold time) (for oscillator start-up and stabilization) requirements, *Power-Up Sequencing* and *Power-Down Sequencing* sections of the device-specific data sheet and confirm the selected PMIC based power architecture supports the above requirements and residual voltage (RV) check.

MCU_PORz input is recommended (required) to be held low (active) during power-up until all the processor supplies ramp and are valid (stable) plus minimum delay of 9.5ms (mentioned as 9500000ns in device-specific data sheet) for internal oscillator to start-up and stabilize (when using external crystal plus internal oscillator, see the device-specific data sheet) or MCU_PORz input is held low (active) until all the processor supplies ramp and are valid and external oscillator clock output is stable (when using external LVCMOS digital clock source (oscillator)) plus minimum delay of 1.2µs (mentioned as 1200ns in data sheet) (see the device-specific data sheet).

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Design Recommendations / Custom board hardware design – common queries for PMIC TPS65219

3.1.2 Discrete Power Architecture

The AM62x power architecture can be based on discrete DC-DC converters and LDOs.

For more information on the discrete power architecture implementation, see the *Discrete Power Solution for AM62x* application note.

When a custom (TI or Non-TI) discrete power architecture is implemented, take note of the supplies sizing, supplies sequencing, supplies slew rate and MCU_PORz input L->H delay (hold time) (for oscillator start-up and stabilization) requirements after all the supplies ramp and verify these requirements as per the device-specific data sheet are followed.

During power-down, the recommendation is for the MCU_PORz input to reach a valid logic low level before the supplies begin to ramp down. The discrete power architecture is expected to be designed to be able to turn off all power rails and monitor the power rails decay to less than 300mV before initiating a new power-up sequence anytime a power rail drops below the minimum value defined in *Recommended Operating Conditions*.

MCU_PORz input is recommended (required) to be held low (active) during power-up until all the processor supplies ramp and are valid (stable) plus minimum delay of 9.5ms (mentioned as 9500000ns in device-specific data sheet) for internal oscillator to start-up and stabilize (when using external crystal plus internal oscillator, see the device-specific data sheet) or MCU_PORz input is held low (active) until all the processor supplies ramp and are valid and external oscillator clock output is stable (when using external LVCMOS digital clock source (oscillator)) plus minimum delay of 1.2µs (mentioned as 1200ns in data sheet) (see the device-specific data sheet).

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Discrete power Architecture

3.2 Processor Supply (Power) Rails (Operating Voltage)

For a complete list of processor power supply rails and recommended operating condition (ROC), see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

For more information about processor ROC, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition

The processor family does not support dynamic voltage scaling (switching) for processor core, peripheral core and peripheral analog supplies after the processor cold reset input (MCU_PORz) has been released. Some of the IO supply for IO groups support dynamic voltage switching. Refer to the *IO supply for IO groups* description in the device-specific data sheet for the IO supply for IO groups that support dynamic voltage switching.

For more information about dynamic voltage scaling (DVS) and dynamic frequency scaling (DFS), see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling for SOC core (VDD_CORE), Peripheral Core and Analog supplies

Note

The recommendation is to verify that the supplies connected to the processor supply rails are within the *Recommended Operating Conditions* of the device-specific data sheet.

3.2.1 Supported Low-Power Modes

For the supported low-power modes, see the device-specific data sheet. For additional explanation on the low-power modes and the functioning see the device-specific TRM. PMIC_LPM_EN0 is a dual-function PMIC control output and provides control of PMIC for low-power mode (active low) or PMIC enable (active high). The PMIC_LPM_EN0 pin requires an external pullup to the VDDSHV_CANUART power source. The pin status is HiZ during reset, which allows the pullup to turn on the PMIC as soon as the always on VDDSHV_CANUART supply ramps up. The pin is driven high once the device is released from reset (rising edge of MCU_PORz input). The pin remains high until the device has been put into partial IO (wakeup from CANUART) mode and told to enter deep-sleep, where it is driven low to turn off the PMIC. The pin is driven high once again when the partial IO logic (CANUART IOs) detects an external wakeup event.

3.2.1.1 Partial IO Support for CAN/GPIO/UART Wakeup

The partial IO circuits will be disabled the first time power is applied to the processor. When the partial IO circuits are disabled, the MCU_PORz input signal will propagate to these circuits. The MCU_PORz input signal is blocked from these circuits after software enables the partial IO functionality (circuits) and configures the processor to monitor wakeup inputs. This is necessary since the MCU_PORz input signal will be asserted by the PMIC when it begins the power down sequence associated with the other processor power rails.

3.2.2 Core Power Supply

Processor core supply VDD_CORE and peripheral core supplies VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 (available only on the AMC package) are recommended to be powered from the same power source and can operate at 0.75V or 0.85V (specified nominal operating voltage as per the *Recommended Operating Conditions* (ROC) table). When core supplies are operating at 0.75V, the recommendation is to ramp 0.75V supply before 0.85V supply.

For supply rails that includes a ferrite filter, a bulk capacitor is recommended on the load side of ferrite (connecting to the processor pins).

VDDR_CORE is specified to operate at 0.85V. When VDD_CORE is operating at 0.85V, the recommendation is to ramp VDD_CORE and VDDR_CORE together (powered from the same source).

VDD_CANUART can operate at 0.75V or 0.85V, there is no voltage dependency with the VDD_CORE during normal operation. The only voltage dependency is during power-up and power-down sequencing.

VDD_CANUART is recommended to be connected to an always-on power source when partial IO (low-power) mode is used. The recommendation is to connect VDD_CANUART to the same power source as VDD_CORE when partial IO (low-power) mode is not used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

Note

For information related to selection of core operating voltage, see the *Operating Performance Points* section of the device-specific data sheet.

3.2.3 Peripherals Power Supply

The processor family supports dedicated, peripheral supply (power) pins for USB (common for USB0 and USB1), CSIRX0, PLLs and OLDI0. The nominal voltage is 1.8V. An additional 3.3V analog supply is recommended for USB.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.4 DDR PHY and SDRAM Power Supply

3.2.4.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

For VDDS_DDR (DDR PHY IO supply) and VDDS_DDR_C (DDR clock IO supply), the recommended supply is 1.1V (when interfaced to LPDDR4 memory - attached device) or 1.2V (when interfaced to DDR4 memory - attached device) based on the memory used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.4.2 AM625SIP

VDDS_MEM_1P1 (LPDDR4 SDRAM IO supply (sources the LPDDR4 SDRAM VDD2 and VDDQ power rails)) is recommended to be powered from the same power source as VDDS_DDR (DDR PHY IO supply).

VDDS_MEM_1P1 and VDDS_DDR power rails are recommended to be connected to 1.1V (LPDDR4).

VDDS_MEM_1P8 (LPDDR4 SDRAM core supply (sources the LPDDR4 SDRAM VDD1 power rail)) is recommended to be connected to 1.8V.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

3.2.5 Dual-Voltage IO Supply for IO Group (Processor) Power Supply

The processor family supports x9 (nine) dual-voltage IO supply for IO group (VDDSHVx [x = 0-6], VDDSHV_MCU and VDDSHV_CANUART). Each group is connected (referenced) to a fixed set of IOs. Each IO supply for IO group can be connected to fixed (VDDSHV4, VDDSHV5, VDDSHV6 supports dynamic supply switching) 3.3V or 1.8V supply independently. The IO supply for IO group defines a common operating voltage for the entire set (fixed set) of IOs.

Most of the processor IOs are not fail-safe. For information on available fail-safe IOs, see the device-specific data sheet. The recommendation is to connect the IO supply of attached devices to the same power source connected to the respective processor dual-voltage IO supply for IO group (VDDSHVx) to make sure the custom board design never applies potential to any of the processor IO that is not powered. Applying input to the IOs that are not fail-safe when IO supply is not available can affect the processor functionality, performance and reliability.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe)

Supported IO supply for IO groups are listed below:

- VDDSHV0 – Dual-voltage IO supply for Main reset and General interface IO group (Fixed)
- VDDSHV1 – Dual-voltage IO supply for OSPI0 IO group (Fixed)
- VDDSHV2 – Dual-voltage IO supply for RGMII1, RGMII2 IO group (Fixed)
- VDDSHV3 – Dual-voltage IO supply for GPMC0 IO group (Fixed)
- VDDSHV4 – Dual-voltage IO supply for MMC0 IO group (Fixed or Dynamic supply switching)

- VDDSHV5 – Dual-voltage IO supply for MMC1 IO group (Fixed or Dynamic supply switching)
- VDDSHV6 – Dual-voltage IO supply for MMC2 IO group (Fixed or Dynamic supply switching)
- VDDSHV_MCU – Dual-voltage IO supply for WKUP_MCU IO group (Fixed)
- VDDSHV_CANUART – Dual-voltage IO supply for CANUART IO group (Fixed)

Note

Dynamically switched supply 1.8V or 3.3V can be applied to IO supply for IO groups shown above as dynamic. A fixed 1.8V or 3.3V can be applied to IO supply for IO groups shown above as fixed. There is no IO supply voltage level dependency between 2 IO supply for IO groups.

Note

VDDSHV_CANUART is recommended to be connected to an always-on power source when partial IO (low-power) mode is implemented. The recommendation is to connect VDDSHV_CANUART to any valid IO power source (1.8V or 3.3V) when partial IO (low-power) mode is not used.

3.2.6 Dynamic Voltage Switching Dual-Voltage Power Supply

VDDSHV4, VDDSHV5 and VDDSHV6 IO supply for IO groups referenced to MMC0, MMC1, MMC2 signal groups have been designed to support power-up, power-down, or dynamic supply voltage change (switching) without dependency on other processor supply rails. The dynamic voltage switching capability allows UHS-I SD card support.

When TPS65219 PMIC based power architecture is used, the PMIC integrates an LDO that supports dynamic voltage switching controlled by processor IO.

When discrete power architecture is used, an external LDO with capability to dynamically switch (controlled by processor IO) between 3.3V and 1.8V is recommended.

3.2.7 VPP (eFuse ROM Programming) Power Supply

The recommendation is to implement a separate LDO to supply the VPP for eFuse programming meeting the current requirements as per the device-specific data sheet. VPP supply can be sourced from a separate on-board LDO supply or an external supply with the timing controlled by a processor IO.

VPP supply pin can be left floating (HiZ) or pulled to ground (ok to connect a resistor with a TP to isolate the ground and connect supply) during, processor power-up, power-down and normal operation.

The following hardware requirements are recommended to be taken care when programming eFuse ROM (OTP):

- The VPP power supply is recommended to be applied only after completion of processor power-up sequence and while programming the eFuse.
- The recommendation is to use a fixed output LDO with higher input voltage (2.5V or 3.3V) and enable input (control). The enable input is recommended to be controlled by the processor GPIO for timing the VPP supply.
- The VPP supply is expected to see high load current transients. Local bulk capacitor is recommended near to the processor VPP pin to support the current transient.
- Select LDO with quick discharge capability or use an external discharge resistor.
- A maximum current of 400mA is specified during eFuse programming.
- When an external power supply is used, the supply is recommended to be applied after the processor power supplies ramp and are stable.
- When an external power supply is used, recommend adding on-board bulk capacitor, decoupling capacitor and discharge resistor near to the processor VPP pin. Add a test point to connect external power supply and provision to connect one of the processor GPIO to control timing of the external supply.
- The recommendation is to disable the VPP supply (left floating (HiZ) or grounded) when not programming the eFuses.
- When an adjustable LDO is used, consider adding an external zener for over-voltage protection at the LDO output.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.2.8 Internal LDOs for IO Supply for IO Groups (Processor)

The processor family supports x9 (nine) internal LDOs (CAP_VDDSn [n = 0-6], CAP_VDDS_MCU and CAP_VDDS_CANUART) and each of the LDO output connects to a separate ball (pin) for connecting an external capacitor. For information on recommended capacitor value, voltage, package and connection, refer to the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

Follow the relevant SK design for selection of the capacitor voltage rating and package. Selecting a capacitor (value, voltage rating) that does not follow the SK or the data sheet recommendations can affect the LDO output stability and processor performance.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to CAP_VDDSx CAP_VDDS

3.3 Power Supply Filtering

The processor family supports a number of analog supply pins that provide power to sensitive analog peripherals like VDDA_MCU, VDDA_PLLx [x=0-2], VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0 and VDDA_1P8_USB. For implementing filter, decoupling and bulk capacitors for the supply rails, see the device-specific starter kit schematic.

For supply rails that includes a ferrite filter, a bulk capacitor is recommended on the load side of ferrite (connecting to the processor pins).

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails

3.4 Power Supply Decoupling and Bulk Capacitors

For information on optimizing and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

Note

The decoupling capacitor numbers and type on the SK or EVM are only intended to serve as a guideline for customers. The true pass or fail criteria is the target impedance published in the PDN application note. In case difference is observed between the SK or EVM and the PDN application note on the capacitor number recommendation and value, the recommendation is to consider the recommendations in the PDN application note.

3.4.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

To decouple the processor (and attached device) supplies from board noise, decoupling and bulk capacitors are recommended. For implementing filtering, decoupling and bulk capacitors for the supply rails, see the *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP* and other SK schematics.

3.4.2 AM625SIP

To decouple the processor (and attached device) supplies from board noise, decoupling and bulk capacitors are recommended.

Additional bulk and decoupling capacitors are required to be connected to some of the reassigned processor pins due to the integrated LPDDR4 SDRAM. For implementing filtering, decoupling and bulk capacitors for the supply rails, see the *Starter Kit SK-AM62-SIP* schematic.

3.4.3 Note on PDN Target Impedance

The PDN target impedance values are provided for specific supply (VDD_CORE). The PDN target impedance values are not provided for other (all) supply rails since the target impedance calculation includes reference to the maximum current on the power rails and is dependent on use case.

For updates on the PDN target impedance supplies and values, see the following FAQ:

[FAQ] AM625 Custom board hardware design – Collateral to Get started

Look for PDN target impedance values (VDD_CORE).

For VDDS_DDR supply rail, using target impedance as the signoff criteria is not recommended. See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* which outlines all details of power aware SI/PI simulations that needs to be performed. The eye mask checks from the power aware simulations are the signoff criteria for VDDS_DDR.

3.5 Power Supply Sequencing

A detailed diagram of the recommended *Power Supply Sequencing* (power-up and power-down) are provided in the device-specific data sheet. All associated processor power supplies are recommended to be designed to allow for controlled supply ramp (supply slew rate) and supply sequencing (using a PMIC-based power supply or using on-board logic when discrete power architecture is implemented).

For more information, see the *Power Supply Requirements*, *Power Supply Slew Rate Requirement* and *Power Supply Sequencing* sections of the device-specific data sheet.

The sequence diagrams are updated based on customer inputs and internal analysis. The recommendation is to review the power sequence diagrams when updated revision for device-specific data sheet is available.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Processor power-sequencing requirements for power-up and power-down

3.6 Power Supply Diagnostics (Using Processor Supported External Input Voltage Monitors)

The external power supply input monitors supported by the processor can be used for early detection of power supply failure or power supply diagnostics.

The processor family supports below voltage monitors:

- For the voltage monitor pin VMON_VSYS the recommendation is to always provision for external resistors (voltage divider) for early detection (indication) of supply failure irrespective of the software implementation. The recommendation is to connect 5V or above for the detection to be effective. For connecting the on-board voltage (main supply voltage such as 5V or 12V or 24V) through an external resistor voltage divider, see the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet. The recommendation is to implement a noise filter (capacitor) at (across) the resistor output connected to the VMON_VSYS input since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients.
- The recommendation is to connect a 1.8V supply to be monitored directly to the VMON_1P8_SOC (without any filter capacitor) pin. For the allowed supply voltage range, see the *Recommended Operating Conditions* section of the device-specific data sheet. When the voltage monitor is not used, follow the *Pin Connectivity Requirements* to connect the VMON_1P8_SOC input.
- The recommendation is to connect a 3.3V supply to be monitored directly to the VMON_3P3_SOC (without any filter capacitor) pin. For the allowed supply voltage range, see the *Recommended Operating Conditions* section of the device-specific data sheet. When the voltage monitor is not used or 3.3V IO supply is not available, follow the *Pin Connectivity Requirements* to connect the VMON_3P3_SOC input.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Custom board hardware design – POK VMON Voltage Monitor

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design – Power OK (POK) Module Voltages Monitored and Connection recommendations

3.7 Power Supply Diagnostics (Monitoring Using External Monitoring Circuit (Devices))

For enhancing custom board performance and based on the application requirements, the recommendation is to provide provision for external monitoring circuit (devices) for all the on-board processor and peripheral supply rails voltage and current draw from supply rails.

For more information, see the *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP* and *Starter Kit SK-AM62-SIP* schematics.

Once the power supply architecture and the required devices for generating the supply rails (based on power architecture) have been finalized, the recommendation is to update the block diagram to include the power architecture (include rail voltage value in the supply rail name) and connections. The recommendation is to generate a Power Supply Sequencing (power-up and power-down) diagram and verify the sequence with the device-specific data sheet.

3.8 Custom Board Current Requirements Estimation and Supply Sizing

The current (maximum and minimum) requirements for each of the supply rail are not provided in the device-specific data sheet. Current requirements are highly application dependent and are recommended to be estimated using TI provided tools and documents for a specific use case.

The recommendation is to take into account the maximum current rating (provided in the *Maximum Current Ratings* application note) for power supply sizing.

Power Estimation Tool (PET) and the *Maximum Current Ratings* application note serve two different purposes. The PET is used to estimate active power consumption for a specific use case/application. The *Maximum Current Ratings* application note can be used for supply sizing when designing a custom power solution.

4 Processor Clock (Input and Output)

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

The next phase of the custom board design is implementation of clock architecture for processor and attached devices. The processor clock can be generated using internal oscillator with an external crystal connected or an external oscillator that generates an LVCMOS compatible clock output. Follow the connection recommendations in the device-specific data sheet when using an external oscillator as the clock source. The below section describes the available processor clock sources and requirements.

4.1 Processor Clocking (External Crystal or External Oscillator)

The processor clock sources and recommended connections are shown in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25MHz external crystal connected directly to XI and XO pins that connects to the internal high frequency oscillator through MCU_OSC0_XI / MCU_OSC0_XO is the recommended main clock input source for the processor internal operation. External oscillator based LVCMOS digital clock source connected to MCU_OSC0_XI can be considered as an alternate clocking option. When external oscillator is used, note the connection requirements for XO in the device-specific data sheet.

The recommendation is to follow the device-specific data sheet for the selection of the load capacitance when crystal is used to generate the processor clock.

The device-specific data sheet provides a recommended delay for clock to start-up and be stable before the cold reset input is released.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Queries regarding crystal (MCU_OSC0) Start-up Time

[FAQ] AM6422: How to Switch Back to External Clock After Clock Loss Detection

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1 and AM625SIP processor family.

Spread Spectrum Clocking (SSC) (Clock source (input), internal clocks, PLLs) is not currently supported on AM62x processor family.

For information related to SSC support, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Enabling spread spectrum core clock on PRUSS

The recommendation is to use a 32.768kHz crystal as clock source for low frequency oscillator (WKUP_LFOSC0). Low frequency oscillator (WKUP_LFOSC0) has limited use case and can be optional.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : LFOSC usage in the processor

4.1.1 WKUP_LFOSC0 Connection When Unused

For information on the recommended connections for unused WKUP_LFOSC0, see the *WKUP_LFOSC0 Not Used* section in the *Specifications* chapter of the device-specific data sheet.

4.1.2 MCU_OSC0 and WKUP_LFOSC0, Crystal Selection

When selecting crystal for MCU_OSC0 or WKUP_LFOSC0, the recommendation is to consider the temperature and aging characteristics based on the worst case operating environment and expected life expectancy of the custom board or the end equipment. Verify the crystal load and the crystal load capacitor value used (including addition of the PCB capacitance (for MCU_OSC0)) matches the device-specific data sheet recommendations. The recommendation is to select crystal load which allows selection of a standard capacitor value. Mismatch in value can introduce clock frequency PPM errors.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding Crystal selection and clock specifications

For more information, see the *MCU_OSC0 Crystal Circuit Requirements* and *WKUP_LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

The recommendation is to connect the MCU_OSC0 crystal directly to the processor as per device-specific data sheet.

The recommendation is to verify the crystal selection with the crystal manufacturer (as required).

4.1.3 LVCMOS Compatible Digital Clock Input Source

The MCU_OSC0_XI and WKUP_LFOSC0_XI clock inputs can be sourced from an external 1.8V LVCMOS square-wave digital clock source. For more information, see the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators*, *MCU_OSC0 LVCMOS Digital Clock Source* section in the *Specifications* chapter of the device-specific data sheet.

For more information, See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

Note

Follow the device-specific data sheet recommendations for connecting MCU_OSC0_XO and WKUP_LFOSC0_XO pins when LVCMOS digital clock is connect to the XI input.

Note

For more information, refer to the Notes provided in the *MCU_OSC0 LVCMOS Digital Clock Source* section of device-specific data sheet.

Note

The device-specific data sheet includes specification for selecting the 25MHz crystal. The current data sheet does not define the *MCU_OSC0 LVCMOS Digital Clock Source Requirements*. These requirements can be added to the next revision of the data sheet. For now, refer to the *MCU_OSC0 LVCMOS Digital Clock Source* section of the AM62Dx or AM62Px data sheet. The requirements for AM62x is the same.

4.2 Processor Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for attached devices (External peripherals - Example: EPHY).

WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available after reset as default configuration.

When CLKOUT0 and WKUP_CLKOUT0 are used to source more than x1 attached devices, buffering the CLKOUT0 and WKUP_CLKOUT0 is recommended.

Jitter profile is not defined on any of the clock outputs because there are many custom board specific variables that can impact jitter. Custom board designer is expected to measure clock output jitter of the specific custom board implementation across all operating conditions expected for the final product.

For more information, see the device-specific data sheet and TRM.

4.2.1 Observation Clock Outputs

The processor provides provision to output a MAIN domain observation clock and/or MCU domain observation clock based on the processor family. OBSCLK0 (available on two pins), MCU_OBSCLK0 are observation clock outputs for test and debug purposes only. Observation clocks can be used to select one of the several different clocks as output. The observation clock is not expected to be used as a clock source for any external device. As stated in the device-specific data sheet, OBSCLK0 and MCU_OBSCLK0 signals are provided for test and debug purposes only.

4.3 Clock Tree Tool

Clock Tree Tool (CTT) can be used to visualize the processor clock tree. Being an interactive visual tool, the CTT gives the user a global view of the device clock tree architecture and can be used to determine the register settings to obtain a specific configuration.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – Clock Tree Tool

5 JTAG (Joint Test Action Group)

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

The processor family supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – JTAG

Although JTAG is considered optional for normal board functioning, the recommendation is to include JTAG connections on the custom board design. The recommendation is to add provision for recommended pulls as per pin connectivity requirements and external ESD protection to populate when JTAG interface is used.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires five standard JTAG signals.

- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in the mode.
- Trace port: the trace port allows real-time dumping of certain internal data. The trace port uses the EMUx pins to output the trace data.

For supported JTAG clocking rates, see the device-specific TRM.

Processor JTAG interface signals can be used to perform for boundary scan tests. The BSDL file for boundary scan testing can be downloaded from the below section on the processor-specific product page:

5.1.1.1 BSDL File

- AM625 BSDL (ALW package)
- AM623 BSDL (ALW package)
- AM620-Q1 BSDL (AMC package)
- AM625-Q1 BSDL (AMC package)
- AM625SIP BSDL (AMK package)

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation signals are referenced to the same IO supply for IO group. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 signals are referenced to VDDSHV_MCU (dual-voltage IO) supply rail (IO supply for IO group MCU). VDDSHV_MCU can be connected to 1.8V or 3.3V.

The recommendation is to use the TI recommended, defined and supported 20-pin connector rather then the 10-pin ARM connector. The 10-pin JTAG connector does not include the TRSTn signal or the EMU0, EMU1 signals.

For implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 Connection Recommendations for JTAG Interface Signals

For connection recommendations of JTAG interface signals, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

The recommendation is to always provide provision for TPs for the processor JTAG signals to be able to connect to external JTAG (When JTAG interface is not part of the custom board design) interface signals or debugger. The recommendation is to add the recommended pulls near to the processor JTAG signals as per the *Pin Connectivity Requirements* section of the processor-specific data sheet. Adding provision for external ESD protection and mounting the ESD components when the JTAG interface is used is recommended.

5.1.4 Debug Boot Modes and Boundary Scan Compliance

Refer *On-Chip Debug* chapter of device-specific TRM for supported debug functionalities.

Refer below sections of the of the *On-Chip Debug* chapter:

- JTAG Interface, JTAG Interface Signals
- Trace Port Interface, Trace Port Signals
- Debug Boot Modes and Boundary Scan Compliance

Emulation control inputs EMU0 and EMU1 are used to configure the debug boot mode behavior. Emulation control inputs EMU0 and EMU1 can be used to enable the boundary scan test capability.

Debug Boot Mode

Emulation control inputs EMU0 and EMU1 are sampled when MCU_PORz input is deasserted and the decoded value determines the debug boot mode behavior as detailed in Table *Debug Boot Modes* of the *On-Chip Debug* chapter of device-specific TRM.

Boundary Scan Compliance

Emulation control inputs EMU0 and EMU1 are sampled when TRSTn is deasserted and the decoded value determines the debug boot mode behavior as detailed in Table *Boundary Scan Compliance* of the *On-Chip Debug* chapter of device-specific TRM.

Debug or boundary scan functionalities does not have any dependency on boot mode configuration.

6 Configuration (Processor) and Initialization (Processor and Device)

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

The recommendation is to deassert (release) the processor cold reset input (for MCU, MAIN domain (MCU_PORz)) only after all the recommended processor supplies ramp plus the recommended delay (reset hold time) for the clock (crystal plus internal oscillator or external oscillator) to start-up and stabilize (see device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor family supports x3 (three) external reset inputs (pins) including MCU and MAIN domain cold reset input (MCU_PORz), MCU and MAIN domain warm reset request input (MCU_RESETz) and MAIN domain warm reset request input (RESET_REQz). Note the silicon errata related to MCU_RESETz input and MCU_RESETSTATz output.

For connecting the warm reset inputs, follow the *Pin Connectivity Requirements* section of the device-specific data sheet.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: MCU_PORz input slew rate

The supported processor reset signals (Reset inputs, Reset status outputs) are described in the device-specific data sheet and device-specific TRM.

The processor family provides x3 (three) reset status outputs (pins) including MAIN domain POR (cold reset) status (PORz_OUT) output, MCU domain warm reset status (MCU_RESETSTATz) output and MAIN domain warm reset status (RESETSTATz) output. A pulldown is recommended near to the processor reset status output pin to hold the attached device in reset state during supply ramp. Note the silicon errata related to MCU_RESETz input and MCU_RESETSTATz output.

Use of processor reset status outputs are board architecture and end application dependent. Reset status outputs when not used can be left unconnected. The recommendation is to provide provision for a test point for testing or future enhancements. An optional pulldown is recommended.

MCU_PORz input is 3.3V tolerant, fail-safe input type IO. Although 3.3V input can be applied, the input threshold follow the 1.8V IO level and is referenced to VDDS_OSC0.

Follow the recommended MCU_PORz input timing recommendations in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset options are available through processor internal registers and emulation.

Note

MCU_RESETz input and MCU_RESETSTATz output have specific use case recommendation. See the advisory *i2407- RESET. MCU_RESETSTATz is unreliable when MCU_RESETz is asserted low* of the silicon errata.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Design Recommendations / Custom board hardware design - Processor Reset inputs, Reset Status Outputs and Connection Recommendations

6.2 Latching of Processor Boot Mode Configuration Inputs

For information on the available processor boot options, see above Section 2.2.

Processor boot mode configuration inputs are latched at the rising edge of PORz_OUT output. After the status (level) on the boot mode inputs (pins) are latched, the boot mode input pins are available to be configured for alternate functions (multiplexed). The PORz_OUT output indicates latching of boot mode configuration. PORz_OUT output optionally can also be used for latching the pin strap configuration for attached devices.

6.3 Resetting of the Attached Device

Using an ANDing logic (implemented using a 2-input or 3-input AND gate) to reset the attached devices as applicable (on-board media and data storage devices, and other peripherals) is recommended since the ANDing logic can cover (covers) all processor external reset input conditions. Any of the processor general purpose input/output (GPIO) pin (select an AM62x processor pin with a GPIO multiplexing option that is turned off by default) is connected to one of the AND gate input with provision for 0Ω to isolate the GPIO output to the ANDing logic for testing or debug. MAIN and MCU domain POR (cold reset) status output (PORz_OUT) or MAIN domain warm reset status output (RESETSTATz) can be connected as the other input to the AND gate. Make sure the processor IO supply and the pullup supply connected to the AND logic input is sourced from the same power source. Processor IO buffers are off during reset. The recommendation is to add a pullup near to the ANDing logic AND gate input (input that is connected to the processor GPIO, RESETSTATz output has a pulldown near the processor pin and driven high by the processor reset logic) to prevent the AND gate input from floating and to enable the reset logic controlled by the processor IO during power-up (Example: eMMC flash or OSPI flash comes out of reset as soon as the RESETSTATz output goes high).

Make sure the attached device reset input pull follows the device recommendations.

An ANDing logic (processor reset status and processor IO as inputs) is recommended to reset the attached devices since the ANDing logic provides the flexibility to be able to reset the attached device in all processor reset condition including local reset.

In case the processor MAIN domain warm reset status output (RESETSTATz) is directly used (without ANDing logic) to reset the attached device, the recommendation is to match the IO voltage level of RESETSTATz with the attached device. A level translator is recommended to match the IO levels. A resistor divider can be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the processor to source too much steady-state current during normal operation. The implementation reduces the attached device reset options flexibility.

For SD card interface, to support UHS-I SD card, the recommendation is to provide provision for a software enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as supply input to the power switch.

Use of power switch allows power cycling of the SD card configured for UHS-I speed (since resetting the power switch is the only way to reset the SD card) to the default speed.

For more information on implementing attached device reset and power switch enable reset logic for SD card power supply, see the *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP*, *Starter Kit SK-AM62-SIP*, and other SK schematic.

6.4 Watchdog Timer

Use of watchdog timer is application dependent. An external watchdog or internal watchdog can be considered. The watchdog output can be combined with other reset sources before connecting to the processor reset input. In case a push button is connected to the processor cold reset input or warm reset inputs, the recommendation is to consider using a reset supervisor that is able to debounce the switch and hold the reset signal low long enough to meet the MCU_PORz or MCU_RESETz or RESET_REQz Pulse Width, active (low) time (1200ns min) requirement.

7 Processor - Peripherals Connection

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

The processor peripherals connection section covers the supported processor peripherals and is intended to be used along with the information provided in the device-specific data sheet, TRM, and relevant application notes. The documents type available that can be used include:

- Data Sheet: Pin diagrams, Pin function description, Pin attributes, Processor operating modes (MUX modes), configuration during and after reset, Electrical characteristics, AC Timings
- TRM: Functional description of processor and supported functionalities for the core and peripherals, Programming Guide, Information regarding registers and supported configuration
- Application Notes: Description of specific feature or peripheral, and description of commonly observed issues

Note

Additionally, FAQs and relevant E2E threads (newly created or previously answered) can be leveraged or used.

7.1 Supported Processor Cores and MCU Cores

The recommendation is to refer to *Features* section of the device-specific data sheet for the supported Processor Cores. The *Device Comparison* section of the device-specific data sheet can be referenced for the selection of the Arm Cortex-A53 Microprocessor Subsystem cores.

The *Operating Performance Points OPP* section of the device-specific data sheet can be reference for definition of the required device grade and device operating performance points.

Refer below FAQ for additional details:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on processor core, PLL, VDD_CORE, VDDR_CORE, VPP and other core supplies

7.2 Selecting Peripherals Across Domains

The processor architecture includes multiple domain, each domain includes specific processing cores and peripherals:

- MAIN Domain
- Microcontroller (MCU) Domain
- Wakeup (WKUP) Domain

For most use cases, peripherals from any of the domain can be accessed by any core. All peripherals, regardless of the domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access most of the peripherals in the MCU domain. Similarly, MCU can access most of the peripherals in the MAIN domain.

7.3 Memory Controller (DDRSS)

7.3.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

The processor family supports x1 instance of DDRSS. The DDRSS interface supports DDR4 or LPDDR4. Choice of DDR4 or LPDDR4 memory is application or customer dependent as there are differences in latency and burst lengths in each of the memory type.

For additional information, refer below application note:

Sitara AM62x Benchmarks

Refer *DDR Electrical Characteristics* section of the device-specific data sheet for information related to JEDEC compliance. Refer note below from the device-specific data sheet:

Note

The DDRSS interface is compatible with DDR4 devices that are JESD79-4B standard-compliant, and LPDDR4 devices that are JESD209-4B standard-compliant.

For data bus width, inline ECC support, speed and max addressable range selection, see the *Memory Subsystem, DDR Subsystem* section in the *Features* chapter of device-specific data sheet.

The allowed memory configurations for DDR4 interface are 1x 16-bit or 2x 8-bit.

1x 8-bit memory configuration is not allowed or valid configuration.

When using LPDDR4 memory, based on the application requirements, same memory device can be used with the AM64x, AM625 / AM623 / AM620-Q1 / AM625-Q1, AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1, AM62D-Q1, AM62P / AM62P-Q1 and AM62Lx processors due to the availability of 16-bit configuration support.

For connecting the DDRSS signals when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information on DDR4 or LPDDR4 memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDRSS : DDR4 / LPDDR4 MEMORY Interface

For more information, see the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

7.3.1.1 Processor DDR Subsystem and Device Register Configuration

The DDRSS controller and DDRSS PHY have a number of parameters to configure. To support the configuration, an online tool *(SysConfig tool)* is provided that generates an output file that is consumed by the driver. Choose the *DDR Subsystem Register Configuration* from the *Software tool* pulldown menu and choose the processor. The SysConfig tool takes board information, timing parameters from DDR device-specific data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then initiates the full training sequence.

The SDK includes configuration file for the memory (DDR4 or LPDDR4) device mounted on the SK. In case a new configuration is required for a different memory (DDR4 or LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see the following FAQ:

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design – Processor DDR Subsystem and Device Register configuration

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

7.3.1.2 Calibration Resistor Connection for DDRSS

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations (including value and tolerance) as per the device-specific data sheet.

7.3.1.3 DDRSS Signals Pin (Package) Delay Information

The pin delay for DDRSS signals have been included in the in the *Additional Information: Package Delays* section of *AM62x, AM62Lx DDR Board Design and Layout Guidelines* (SPRAD06C – MARCH 2022 – REVISED MARCH 2025) application note on TI.com.

The package delays provided in this appendix are measured from processor die pad to processor package pin.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM624SIP: AM6254 LPDDR4 LENGHT/DELAY MATCHING

7.3.1.4 Attached Memory Device ZQ and Reset_N (Memory Device Reset) Connection

Follow the SK schematic for connecting the recommended resistors (ZQ (Impedance calibration) and Reset_N (attached memory reset input)) to the memory device including recommended value and tolerance.

7.3.2 AM625SIP

LPDDR4 SDRAM (512MBytes) is internal (integrated) to AM625SIP. For speed and inline ECC support, see the *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter and *Integrated LPDDR4 SDRAM Information* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

7.3.2.1 AMK Package Reassigned DDRSS Pins

The AM6254 DDRSS signals on the ALW package that connects to an external memory (DDR4 or LPDDR4) connects directly to an integrated LPDDR4 SDRAM in the AM625SIP processor family, and the pins associated with these signals were reassigned to different power or signal functions.

See the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

7.3.2.2 DDRSS and Memory Device Calibration Resistor Connection

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations (including value and tolerance) as per the device-specific data sheet. Follow the SK schematics for connecting the recommended resistors (ZQ and Reset) input to the memory devices including values.

7.3.2.3 LPDDR4 (Internal) Memory Calibration Resistor Connection

Follow the DDR_ZQ (LPDDR4 SDRAM Calibration Reference Resistor) connection recommendations (including value and tolerance) as the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

7.4 Media and Data Storage Interfaces (MMC0, MMC1, MMC2, OSPI0/QSPI0 and GPMC0)

The processor family supports x3 (three) Multi-Media Card/Secure Digital (MMC/SD/SDIO) (8b (4b) + 4b + 4b) instances.

MMC0 supports 8-bit eMMC (embedded Multi-Media Card) interface. For supported speeds, see the *MMC0 - eMMC/SD/SDIO Interface* section of device-specific data sheet, refer SK for implementation. Alternatively, the MMC0 signals can be used as IOs or other supported muxed functions, or for on-board SDIO interface. Interfacing SD card to MMC0 port is not recommended. MMC0 is the recommended interface for eMMC interface. The required pulls for the eMMC interface as per the JEDEC standard is required to be implemented external to the processor. An external pulldown for the clock input near to the memory clock input is recommended.

The required pulls for the eMMC interface as per the JEDEC standard is required to be implemented external to the processor. An external pulldown for the clock input near to the memory clock input pin is recommended.

For more information on eMMC memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

For information on the supported speeds, see the following FAQ:

[FAQ] AM623: Can eMMC0 support DDR50 mode

For information on supported interface on the MMC0 port, see the following FAQ:

[FAQ] AM62A3: Any way to get 2 eMMC interfaces?

For information related to eMMC pulls, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: eMMC0_DAT0 not enabled pull up by ROM

For information related to eMMC capability to pause the clock when there are no transfers, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Is the eMMC clocks maintained when read and write operations are finished ?

Refer to the silicon errata for eMMC related erratas.

MMC1/MMC2 supports 4-bit SD card interface including support for UHS-I SD card. MMC1 is recommended for implementing SD card interface since MMC1 supports SD card boot mode, MMC1 CLK, CMD, and DAT[3:0] signal functions have been implemented with SDIO buffers and are powered by (referenced to) VDDSHV5. VDDSHV5 can be operated at 1.8V or 3.3V (dynamically switched). MMC1 SDCD and SDWP signal functions are implemented with LVCMOS buffers and are powered by (referenced to) VDDSHV0, which can be operated at fixed 3.3V or 1.8V. The logic state of the MMC1_SDCD and MMC1_SDWP inputs to the host is not recommended to be changed when IO operating voltage for SD card changes to support UHS-I SD card. The required pulls for the SD card interface as per the SD card specifications is required to be implemented external to the processor. An external pulldown for the clock input near to the memory clock input pin is recommended.

MMC1/MMC2 supports 4-bit embedded SDIO interface. MMC2 is recommended for implementing embedded SDIO interface. MMC2 CLK, CMD, and DAT[3:0] signal functions have been implemented with SDIO buffers and are powered by (referenced to) VDDSHV6. VDDSHV6 can be operated at 1.8V or 3.3V (dynamically switched). MMC2 SDCD and SDWP signal functions are implemented with LVCMOS buffers and are powered by (referenced to) VDDSHV6 (VDDSHV0), which can be operated at fixed 3.3V or 1.8V. Refer *Signal Description* section of the device-specific data sheet for supported pin assignments. The MMC2 pin assignments are different compared to MMC1 because MMC2 is expected to be used with on-board fixed operating voltage SDIO devices similar to Wi-Fi or Bluetooth transceivers. For supported speeds, see the *MMC1/MMC2 -SD/SDIO Interface* section of device-specific data sheet, refer SK for implementation. Pullups (as required, verify the attached device recommendations including supported pulls) for the SDIO interface is required to be implemented external to the processor. An external pulldown (as required, verify the attached device recommendations including supported pulls) for the clock input near to the memory clock input pin is recommended.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design –SD card Interface

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1: Why is MMC1 powered by two different voltage supplies, VDDSHV0 and VDDSHV5?

[FAQ] AM62A7-Q1: how to connect the pin net VDDSHV4, VDDSHV5, and VDDSHV6 if SD card is not used

The FAQs are generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

For MMC1/MMC2, UHS-I SDR50, UHS-I SDR104 receive modes require data training to center the data capture to the center of the data valid window. The timing requirements are not fixed to specific values. The required DLL software configuration settings for MMC1/2 timing modes is provided in the below table:

MMC1/MMC2 DLL Delay Mapping for all Timing Modes of device-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: UHS-I SDR104 Receive mode timing

The processor family supports x1 Octal Serial Peripheral Interface (OSPI0) instance that can be configured for OSPI0 or QSPI0 interface. The recommendation is to follow the SK schematic implementation to interface the OSPI0 interface to a memory device (OSPI or QSPI), addition of series resistor for OSPI0_CLK (for control of possible reflection), pulldown for OSPI0_CLK, pullup for data and CS signals, and implementation of attached memory device reset logic. OSPI0 supports connecting to a x1 (single) attached device.

Refer to the device-specific TRM to connect the supported CS (chip select) to the attached memory device when boot functionality is required to be supported.

OSPI0 supports two data capture modes, PHY mode and Tap mode. To better understand the supported modes, refer to the OSPI, *OSPI0* sub-section in the *Timing and Switching Characteristics* section in the *Specifications* chapter of the device-specific data sheet.

For more information on OSPI or QSPI memory interface, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

[FAQ] OSPI FAQ for Sitara/Jacinto devices

The processor family supports x1 General-Purpose Memory Controller (GPMC) interface instance that can be interfaced to NAND flash using 8-bit or 16-bit NAND flash interface signals or NOR flash using supported parallel memory interface (Synchronous or Asynchronous) options listed in the device-specific data sheet and *Device Comparison* table.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (Memory interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

For more information, see the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Ethernet Interface

The processor family supports x1 instance of CPSW3G Ethernet switch (with 2 external ports) and supports x2 (two) independent Ethernet interface with independent MAC ID (using CPSW3G0 peripheral). CPSW3G0 allows using mixed RGMII/RMII interface topology for the x2 external interface ports. Each of the MAC interface supports RGMII or RMII interface.

Before using the Ethernet ports and configuring the MDIO interface (for boot and normal operation), refer to advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* in the *AM62x Processor Silicon Revision 1.0*.

For more information on the Ethernet interface, see the following FAQs:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 and AM2434, AM2432, AM2431 (ALV, ALX) Custom board hardware design - Ethernet

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RGMII interface and RGMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RMII interface and RMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Ethernet PHY RGMII synchronous clock

7.5.1 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G0)

The CPSW3G0 can be configured either as a 3-port switch (interfaces to 2 external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having individual MAC address.

CPSW3G0 supports RGMII (10/100/1000) or RMII (10/100) interface for each of the external Ethernet interface port.

For implementation of RMII interface, see the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G0 when configured for RMII interface supports processor connections to Ethernet PHY (EPHY) configured as controller (master) or device (slave).

CPSW3G0 when configured for RMII interface, interfaces to EPHY configured for an external 50MHz (connected to a buffered external oscillator or processor clock output CLKOUT0) clock input (one of the buffered clock output connects to processor MAC) or EPHY configured for 25MHz crystal or clock input with 50MHz clock output from EPHY connected to the processor MAC clock input.

One of the CPSW3G0 port is an internal CPPI (Communications Port Programming Interface) host port. CPPI is a streaming interface to provide data from DMA to CPSW3G0 peripheral and vice-versa.

RGMII_ID is enabled by default for Transmit data (TDn). RGMII_ID is not timed, tested, or characterized. Processor MAC does not implement internal delay for the Receive data (RDn) path.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (Ethernet interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

For more information on the CPSW3G0 Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.6 Programmable Real-Time Unit Subsystem (PRUSS)

The processor family provides x2 PRU subsystems. The PRUSS supports Universal Asynchronous Receiver/ Transmitter (UART0), Enhanced Capture (ECAP0), Industrial Ethernet Peripheral (IEP0) modules.

For more information, see the following FAQ:

[FAQ] What is a PRU core? Why are PRU GPIO signals different from regular GPIOs?

For more information, see the *Programmable Real-Time Unit Subsystem (PRUSS)* section in the *Processors and Accelerators* chapter of the device-specific TRM.

7.7 Universal Serial Bus (USB) Subsystem

The processor family supports x2 (two) instances of USB 2.0 interface ports. The USB interfaces (USB0, USB1 ports) can be configured as host or device or Dual-Role Device (DRD). USBn_ID (identification) functionality can be implemented (supported) using any of the processor GPIO.

Follow the *USB (USB VBUS Detect Voltage Divider / Clamp Circuit) VBUS Design Guidelines* section of the device-specific data sheet to scale the external USB VBUS voltage (supply near the USB interface connector) and connecting to USBn_VBUS [n = 0, 1] pins.

Connecting the scaled VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) input is recommended when the USB interface is configured for device mode. Connection of scaled VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) is optional when the USB interface is configured for host mode.

Connecting 3.3V or a permanent on-board supply equivalent to the scaled VBUS input, is not recommended or allowed. The USB VBUS input needs to be switched. The fail-safe input condition is valid only when the supply is connected through the recommended VBUS voltage divider and zener diode.

A USB power switch with OC (over current) output indication is recommended when the USB interface is configured as host for VBUS output voltage control. The USBn_DRVVBUS [n = 0, 1] (internal pulldown enabled during and after reset) controls the power switch. The recommendation is to connect the OC output to a processor IO (input) to detect VBUS over load.

For information related to USB connections and On-The-Go feature support, see the device-specific TRM.

When both USB0 and USB1 interfaces are not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the supply pins.

When USB0 or USB1 interface is not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the interface signals and supply pins.

The recommendation is to always provision for USB0 DFU boot for early board builds for board bring-up and debug.

For more information on USB2.0 interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – USB2.0 interface

For more information, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.8 General Connectivity Peripherals

The processor family supports multiple, general connectivity peripherals and instances. The processor family supports the following peripherals:

The following peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. Make sure the usage of the correct IOSET in the custom board design. Timing closure is based on the IOSETs.

Multichannel Serial Peripheral Interface (MCSPI):

The processor family supports x5 (five) (x3 MAIN domain, x2 MCU domain) instances of MCSPI. The MCSPI module is a multichannel transmit/receive, synchronous serial bus and can operate in controller mode or peripheral mode. In controller mode, the processor SPI interface sources the clock to the attached device. In peripheral mode, the attached device is required to source the SPI clock to processor.

A series resistor (22Ω) is recommended (as a starting point) for the MCSPI clock output signals. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown (10kΩ) is recommended close to the attached device clock input pin.

A pullup (10kΩ) is recommended for the chip select (CS) pin close to the attached device.

The MCSPI peripherals do not support boot. The OSPI0 interface supports SPI boot.

For the MCSPI interface SPIx_D0 and SPIx_D1 are the data lines. The data lines support programming the signals either to transmit data (transmission, output) or receive data (reception, input).

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (MCSPI interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

The recommendation is to connect the SPI interface to x1 (single) memory device. When connecting to multiple memory devices, the recommendation is to follow high-speed design practices and perform simulations to make sure the layout is not going to generate non-monotonic clock transitions when the single clock source is connected to multiple SPI attached devices.

See the following FAQs:

[FAQ] SK-AM64B: MCSPI Integration Guide

[FAQ] AM6412: AM64x SPI D0 and D1 - MISO/MOSI

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

Inter-Integrated Circuit (I2C):

Refer below Section 7.8.1.

Universal Asynchronous Receiver/Transmitter (UART):

The processor family supports x9 (nine) (x7 MAIN domain, x1 MCU domain, x1 WKUP domain) instances of UART interface. Supported UART functions include data transfer (TXD, RXD), Modem control functions (CTS, RTS) and extended modem control signals (DCD, RI, DTR, DSR - supported by MAIN domain UART1).

Refer to the *Signal Descriptions* section of the device-specific data sheet for the supported functionalities for each of the UART instances.

Refer to the *Timing and Switching Characteristics* section of the device-specific data sheet for supported data rate (programmable baud rate).

When external UART interface signals are directly connected to the processor UART interface signals, verify IO level compatibility and fail-safe operation. The recommendation is to provide provision for external ESD protection.

The recommendation is to provision for UART boot (UART0) for early board builds for board bring-up and debug.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (UART interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

General Purpose Input/Output (GPIO):

The processor family supports GPIO0, GPIO1 and MCU_GPIO1 instances of GPIO modules. Processor GPIOs include LVCMOS and SDIO buffer types and are push-pull type outputs. Some specific IOs support open-drain output type IO buffer interface. LVCMOS IOs when configured as I (input) have input slew requirements and O (output) has capacitor loading recommendations. The recommendation is to perform simulation with the connected load capacitor to make sure the output is within the ROC as per device-specific data sheet electrical characteristics.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs that has a trace connected to the processor pads and can float (to prevent the attached device inputs from floating until driven by the host).

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to GPIO

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – Queries related to LVCMOS input Hysteresis

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Information on PADCONFIG bits and PADCONFIG registers default values summary

Note

PADCONFIG register bit configuration - ST_EN: The recommendation is to keep the ST_EN bit enabled in case the PADCONFIG register is modified by the software. The minimum *Input Slew Rate* parameter defined in each *Electrical Characteristics* table of device-specific data sheet is associated with long-term reliability. The parameters are not a function of the ST_EN bit. The schmitt trigger function implemented in the input buffer only changes the output results of the input buffer, by filtering noise pulses that do not exceed the hysteresis. The schmitt trigger function does not change how the input buffer operates when a system applies a slew rate to its input that is slower than defined in the device-specific data sheet.

Audio Peripheral - Multichannel Audio Serial Port (MCASP):

The processor family supports x3 (three) (x3 MAIN Domain) instances of Audio peripheral - Multichannel Audio Serial Port (MCASP). MCASP supports up to 4/6/16 Serial Data Pins (serializer) across x3 MCASP with

Independent TX and RX Clocks. MCASP supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats. A series resistor 22Ω is recommended (as a starting point) for the MCASP clock output. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown is recommended close to the attached device clock input pin.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (MCASP interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L Design Recommendations / Custom board hardware design - Queries related to MCASP

Industrial and Control Interfaces:

The processor family supports multiple instances (refer *Device Comparison* table of the device-specific data sheet) of Industrial and Control Interfaces.

1. Modular Controller Area Network (MCAN) with Full CAN-FD support
2. Enhanced Pulse Width Modulator (EPWM)
3. Enhanced Quadrature Encoder Pulse (EQEP)
4. Enhanced Capture (ECAP)

Modular Controller Area Network (MCAN) with Full CAN-FD support:

The processor family supports x3 (three) (x1 MAIN domain, x2 MCU domain) instances of Modular Controller Area Network (MCAN) with Full CAN-FD support.

The MCAN module supports both classic CAN and CAN-FD (CAN with Flexible Data-Rate) specifications.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (MCAN interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

The required interfaces can be configured using the *SysConfig-PinMux* tool.

For more information on the supported peripherals, see the *Peripherals* chapter of the device-specific TRM.

7.8.1 Inter-Integrated Circuit (I2C) Interface

The processor family supports x6 (six) (x2 (two) I2C compliant, fail-safe open-drain output type IO buffer and x4 (four) LVCMOS buffer type IO based emulated open drain output type IO) I2C interfaces. The supported I2C interfaces include x4 MAIN domain, x1 MCU domain (I2C compliant open-drain output type IO buffer) and x1 WKUP domain (I2C compliant open-drain output type IO buffer) I2C interfaces.

Note

For I2C interfaces with open-drain output type IO buffer (MCU_I2C0 and WKUP_I2C0), a pullup is recommended irrespective of IO configuration. An external pullup is recommended even when the I2C interface (peripheral) is not used. See the *Pin Connectivity Requirements* section of device-specific data sheet.

When open-drain output type IO buffer I2C interfaces are pulled to 3.3V supply, the inputs have slew rate requirements specified. An RC (delay) is recommended to limit the slew rate with the C placed near to the processor pin. For RC implementation, see the AM64x EVM schematic and see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

An external pullup is recommended for LVCMOS IOs when configured as emulated open-drain output type IO buffer I2C interface (I2C0, I2C1, I2C2, I2C3). For the available emulated open-drain output type IO buffer I2C instances, see the device-specific data sheet.

Pullup values in the SK can be used as starting point. The pullup value depends on the I2C interface implementation and loading of the I2C bus. The recommendation is to measure the I2C waveforms and reduce (adjust) the pullup value as required.

Note

Verify the *Exceptions* sub-section in the *Timing and Switching Characteristics, I2C* section of the device-specific data sheet during the custom board design. Take note of the exceptions for the emulated I2C interface. The recommendation is to add series resistor for the I2C interface signals near to the processor to control the fall time.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – I2C interface

[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 and AM62D-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

For more information, see the *Inter-Integrated Circuit (I2C) Interface* section in the *Peripherals* chapter of the device-specific TRM.

7.9 Display Subsystem (DSS)

Display outputs from the processor can be connected to an external display using Open LVDS Display Interface transmitter (OLDITX) and Display Parallel Interface (DPI - directly driven through the processor IOs).

7.9.1 AM625 / AM623 / AM625-Q1 / AM625SIP

OLDI0 (Open LVDS Display Interface):

The processor family supports x4 (four) data lanes and x1 (single) clock lane, x2 (dual) link LVDS OLDI display interface. OLDI0 interface can be configured for x2 OLDI-SL single-link or x1 OLDI-DL dual-link display mode.

When OLDI0 display interface is configured for dual-link display mode, there are "Odd/Even" requirements (for pixels). A0, A1, A2, A3 correspond to Odd pixels and A4, A5, A6, A7 correspond to the Even pixels.

When OLDI0 interface is configured for x2 single-link display mode, the OLDI0 interface supports (can be configured) only mirrored (duplicate, due to internal hardware support/configuration) mode.

Refer below FAQ for supported resolution when the OLDI0 interface is configured for OLDI-DL and OLDI-SL.

For connecting the OLDI0 signals when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information on OLDI0, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62P / AM62P-Q1 Custom board hardware design – OLDI (Open LVDS Display Interface) capabilities

DPI (Display Parallel Interface):

The processor family supports 24-bit per pixel, RGB/YUV422 modes, LVCMOS output, DPI (parallel) display interface.

DPI does not currently support SSC. Start an E2E thread or review available collaterals on the processor-specific product page to check on the status of SSC support for DPI.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (DPI interface signals) that can float (to prevent the attached device inputs from floating until driven by the host).

For more information on DPI, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB- display interface

For more information, see the *Display Subsystem (DSS) and Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

7.9.2 AM620-Q1

Display interfaces (OLDI and DPI) are not supported.

7.10 CSI-Rx (Camera Serial interface)

The processor family supports x1 Camera Serial interface (CSI-RX, CSI-2, CSIRX0), x4 Lane with D-PHY (DPHY, DPHY_RX) and are MIPI CSI-2 v1.3 Compliant + MIPI D-PHY 1.2 compliant (CSIRX0). Supports up to x4 (1, 2, 3, or 4) Data Lane connection to D-PHY (DPHY_RX). For maximum supported data rate, see the *Multimedia, Camera Serial interface (CSI-Rx) - 4 Lane with DPHY* section in the *Features* chapter of device-specific data sheet.

The DPHY_RX (CSI-RX) supports a x1 (single) clock lane and all the data lanes are clocked at the same frequency. The frame rate is determined by start-of-frame, end-of-frame signaling and allows handling the input sources with different frame rates per channel.

For connecting the CSIRX0 signals when not used (complete or partial), see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information on CSIRX0, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625SIP / AM625-Q1 / AM62Ax / AM62Px Custom board hardware design – CSI-2 capabilities

The FAQ includes information related to the allowed data lane and clock lane swapping.

For more information, see the *Camera Subsystem* section in the *Peripherals* chapter of the device-specific TRM.

7.11 Real-Time Clock (RTC) Module

The processor family supports x1 instance of Real-Time (RTC) module to allow easy tracking of time and date and the generation of real time alarms.

For more information, see the *Real-Time Clock* section in *Peripherals* chapter in the device-specific TRM.

The processor family does not support a separate supply for the RTC module to retain the time (timer) value during warm or cold reset. The time (timer) value can be reset during processor generated software reset or external cold or warm reset.

WKUP_LFOSC0 can be used to support the RTC module functionality based on clock accuracy requirement.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 Design Recommendations / Custom board hardware design - Queries related to Real-Time clock (RTC)

7.12 Connection of Processor Power Supply Pins, IOs and Peripherals When not Used

All the processor supply (power) pins are recommended to be supplied (connected) with the supply voltages as per *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified in the *Pin Connectivity Requirements* section of the device-specific data sheet.

The recommendation is to read the notes at the beginning and end of the *Pin Connectivity Requirements*.

The processor family includes pins (package balls) that have specific connectivity requirements and pins that are recommended to be left unconnected.

For more information on connection of unused processor peripherals and IOs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC peripherals and IOs connection when not used

7.12.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

For information on connecting specific unused processor peripherals (USB0, USB1, DDRSS0, CSIRX0 and OLDI0) and IOs, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

7.12.2 AM625SIP

For the AM625SIP processor, the DDRSS0 is internally connected to LPDDR4 SDRAM device. The DDRSS pads have alternate external connections assigned. For connecting the reassigned (DDRSS0) pads, see the *Reassigned DDRSS0 Pins on the AMK Package* table in the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*).

For information on connecting the unused processor peripherals (USB0, USB1, CSIRX0 and OLDI0) and IOs, see the *Pin Connectivity Requirements* section of the *Terminal Configuration and Functions* chapter of the device-specific data sheet (*AM62x Sitara Processor*).

7.12.3 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type fail-safe IO buffer. The recommendation is to connect external pullup when a PCB trace is connected and an external input is not being actively driven. Open-drain output type IO buffer has slew rate requirements specified when pulled up to 3.3V. An RC (delay) is recommended to limit the slew rate with the C placed near to the processor pin.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection

7.12.4 RSVD Reserved Pins (Signals)

Pins named RSVD are Reserved. The recommendation is to leave the RSVD pins unconnected (no test points (TPs)) as recommended in the device-specific data sheet.

The recommendation is to leave the RSVD pins unconnected (the recommendation is to not connect any PCB trace or test point).

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Connection recommendations for RSVD pins

7.13 SK Specific Circuit Implementation (Reuse)

In case some of the SK implementation listed below are reused:

- DPI to HDMI
- AUDIO CODEC
- FT4232 UART TO USB BRIDGE
- XDS110 DEBUGGER
- CPSW3G RGMII or RMII – EPHY
- M.2 INTERFACE – SDIO
- CURRENT MONITORING DEVICES
- USB TYPE-C PD CONTROLLER AND POWER SUPPLY

The recommendation is to follow the below FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Custom board hardware design – Guidelines for reuse of SK specific implementations listed below on custom board design

8 Interfacing of Processor IOs (LVCMOS or SDIO or Open-Drain, Fail-Safe Type IO Buffers) and Performing Simulations

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

An important consideration during the custom board design before start of the schematic capture is to analyze compatibility (Electrical characteristics, IO level, fail-safe operation) between the processor and attached devices.

- The device-specific (processor) data sheet includes information with regards to timing and electrical characteristics.
- For high-speed interfaces, the recommendation is to run simulations using IBIS model.

For more information, refer to the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

For information related to drive strength configuration support, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Drive Strength Configuration for SDIO and LVCMOS I/Os

The IBIS and IBIS-AMI models can be downloaded from the below sections on the processor-specific product page:

8.1 IBIS Model

- AM625 IBIS Model (ALW package)
- AM623 IBIS Model (ALW package)
- AM620-Q1 IBIS Model (AMC package)
- AM625-Q1 IBIS Model (AMC package)
- AM625SIP IBIS Model (AMK package)

Note

Separate IBIS models are provided for each package.

Refer TI.com for availability of IBIS model for ALW Q1 processor package.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to IBIS model

8.2 IBIS-AMI Model

- AM625 IBIS-AMI Model (ALW package)
- AM623 IBIS-AMI Model (ALW package)
- AM620-Q1 IBIS-AMI Model (AMC package)
- AM625-Q1 IBIS-AMI Model (AMC package)
- AM625SIP IBIS-AMI Model (AMK package)

Note

The recommendation is to double click on the .exe file to install the IBIS-AMI models. Installing IBIS-AMI model is the only supported option to use IBIS-AMI model.

Refer TI.com for availability of IBIS-AMI model for ALW Q1 processor package.

9 Processor Current Draw and Thermal Analysis

The custom board current requirements depends on selected processor, peripherals used, end equipment features implemented, application environment, operating temperature requirements, and temperature/operating voltage variations.

For more information, see the following FAQ:

[FAQ] AM623: Package ALW contact pressure specification for thermopad

9.1 Power Estimation

For estimating the processor current (power) based on the use case, use below:

- AM625 Power Estimation Tool
- AM623 Power Estimation Tool
- AM620-Q1 Power Estimation Tool
- AM625-Q1 Power Estimation Tool
- AM625SIP Power Estimation Tool

9.2 Maximum Current Rating for Different Supply Rails

For information on the maximum current rating at the processor power terminals for power supply groups, see the *AM62x Maximum Current Ratings* application note. The application note covers both ALW and AMC packages. The recommendation is to follow the *Maximum Current Ratings* application note for power supply sizing.

Note

The Power Estimation Tool (PET) and the *Maximum Current Rating* application note serve two different purposes. The PET is used to estimate active power consumption for a specific use case/ application. The *Maximum Current Rating* application note can be used for supply sizing when designing a custom power architecture.

9.3 Supported Power Modes

For information on the supported power modes (including Partial IO, DeepSleep), see the *Power Modes* sub-section, *Power* section in the *Device Configuration* chapter of the device-specific TRM.

For more information, see the following application notes:

Enabling Low Power Embedded Systems With AM62x Processors

AM62x Power Consumption

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application note provides guidance for implementation of a thermal option for custom board designs using Sitara family of processors. The application note provides background information on common terms and methods. Any follow-up design support that may be required is provided only for board designs that follow thermal design guidelines contained in the application note.

The Thermal model can be downloaded from the below section on the processor-specific product page:

9.4.1 Thermal Model

- AM625 Thermal Model (ALW package)
- AM623 Thermal Model (ALW package)
- AM620-Q1 Thermal Model (AMC package)
- AM625-Q1 Thermal Model (AMC package)
- AM625SIP Thermal Model (AMK package)

Note

Refer TI.com for availability of thermal model for ALW Q1 processor package.

9.4.2 Voltage Thermal Management Module (VTM)

Independent temperature sensors are located at designated hotspots on the processor. The device-specific data sheet provides the VTM accuracy and the device-specific TRM provides information on the location of the temperature sensors.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x (ALV, ALX) Custom board hardware design – Voltage and Thermal Manager (VTM)

10 Schematic:- Capture, Entry and Review

The schematic, capture and entry can now be started for the custom board design.

The below FAQ summarizes key collaterals that can be referenced during custom board schematic design and custom board schematic review:

[FAQ] AM64x, AM243x (ALV, ALX), AM62x, AM62Ax, AM62Px, AM62D-Q1, AM62L Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

For guidelines on component selection, schematic capture and review, see the following sections:

10.1 Custom Board Design Passive Components and Values Selection

When selecting passive components, the recommendation is to follow the device-specific data sheet (as applicable) for the values including the tolerance and voltage rating. The recommendation is to follow the derating guidelines (generic or company specific for passives (Example: resistor wattage and capacitor voltage rating)).

Note

Component values, package size and voltage rating in the SK have been provided as a good starting point for the custom board designer.

During custom board design, the recommendation is for the custom board designers to validate if the TI recommended values, tolerance, package size and voltage rating are appropriate for the specific custom board design (end equipment) implementation and make required updates.

10.2 Custom Board Design Electronic Computer Aided Design (ECAD) Tools Considerations

Orcad is the Electronic Computer Aided Design (ECAD) tool used for SK schematics.

Allegro is the ECAD tool used for SK layout.

For information on the ECAD tools used for SK design, see the following FAQ:

[FAQ] AM625 / AM623 / AM62L / AM625-Q1 / AM62A7 / AM62A3 / AM62A1 / AM62P-Q1 / AM62D-Q1 Custom board hardware design – processor evaluation modules or starter kits information including Board Design CAD tools version

A .alg file is provided for translating the Allegro design file to Altium. In case an altium converted design files are required, the recommendation is to check the relevant SK or processor product page for availability or add an E2E query.

10.3 Custom Board Design Schematic Capture

The next phase of the custom board design after completing the schematics design is the schematics capture. During the schematic capture phase, the custom board schematics can be newly drawn or the SK schematic design can be used (reused as a starting point) to make the updates.

For more information, see the *Starter Kit SK-AM62B-P1* schematic for ALW package, *Starter Kit SK-AM62-LP* schematic for AMC package and *Starter Kit SK-AM62-SIP* schematic for AMK package.

Note

During the custom board design cycle, the recommendation is to follow *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist* user's guide along with *Hardware Design Considerations for Custom Board Design* user's guide.

Additionally, the below FAQ can be used that includes schematic review checklist for AM62x processor families:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

The below FAQ summarizes the considerations when SK schematics design files are reused for custom board designs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design - Reusing TI SK (EVM) design files

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Note

When the SK design (schematic) is reused, take care of implementation completeness of the required functionalities (implemented on multiple pages) and change in net names due to design changes or optimization are reviewed and updated. Review and follow the notes (Design, Review and CAD) added on the schematic pages close to the circuit before implementation.

When the SK design (schematic) is reused, the DNI settings for all the components can reset. Make sure the DNIs are reconfigured (populating DNIs can affect the functionality). Review the DNI notes added on the schematic pages close to the circuit implementation.

10.4 Custom Board Design Schematic Review

After the completion of the schematic capture, the recommendation is to perform a self review using the *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist*.

The below FAQ lists the collaterals and steps that can be followed for performing self-review of the custom board schematic design:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Design Recommendations / Custom board hardware design - Custom board schematics self-review

Additionally, the below FAQ can be used that includes schematic review checklist for AM62x processor families:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

Refer below FAQ for information related to some of the common errors observed during schematic updates:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

For information on connecting used/unused processor pins, and peripherals, see the following FAQ:

[FAQ] AM62x, AM62Ax, AM62D-Q1, AM62L, AM62Px, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals and add pullup or pulldown? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...)

The recommendation is to plan a formal schematic review internally to review the custom board schematics with reference to the *Schematic Design Guidelines and Schematic Review Checklist*. The recommendation is to review custom board design implementation for possible design errors, change in component values, connection errors, missing net connections, and other design recommendations (not being followed).

In case a schematics review request is required to be submitted to TI, the recommendation is to follow the below FAQ:

[FAQ] Sitara MPU Hardware Applications Support - Schematics review request

The FAQ is generic and can also be used for AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP processor family.

As part of the review, recommendation is to verify if the custom board schematic design follows the recommendations as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers and Simulation

After the schematic capture and reviews (self, team and external (review by attached device silicon suppliers)) have been planned, completed and required updates are made, the recommendation is to perform component placement analysis (floor plan) for the custom board design to determine the optimal component placement approach and the interconnect distances between processor and various ICs (attached devices), determine board dimensions and outline.

The next phase of the custom board design is board layout (placing the components, finalizing the form-factor and board layout).

See the following sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

Below application notes describe the recommended PCB escape routing for the processors can be referenced during custom board layout.

- *AM62 Escape Routing for PCB Design*
- *AM62x (AMC) Escape Routing for PCB Design*
- *AM62x SiP Escape Routing for PCB Design*

See the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Layout guidelines maximum trace length, length matching tolerance, impedance, trace spacing requirements for EMMC, RMII, OLDI interfaces

11.2 DDR Design and Layout Guidelines

11.2.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*. Use of guidelines simplifies DDR4 or LPDDR4 board layout. Layout guidelines and requirements have been captured as a set of layout (placement and routing) recommendations that allow custom board designers to implement a custom board design that support the required functionality for the memory connection topologies supported by the processor. Any follow-up design support that may be required are provided only for board designs that follow the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for the recommended trace impedance for routing the DDRSS (DDR4 or LPDDR4) signals.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for supported, DDR4 data rate, device bit width, device count, Channel Width, Channels, Die, Ranks.

For the propagation delay, the delay to be considered for DDR4 or LPDDR4 is the delay related to the traces on the board. On a need basis, the package delay that has been included in the *Additional Information: Package Delays* section of *AM62x, AM62Lx DDR Board Design and Layout Guidelines* can be added.

AM62x, AM62Lx DDR Board Design and Layout Guidelines includes guidelines for bit swapping.

The recommendation is to perform signal integrity (SI) simulations during custom board schematic design and the board layout phase.

Note

DDR2 and DDR3 interfaces are not supported.

11.2.2 AM625SIP

Follow the recommendations in the device-specific data sheet (*AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*) to connect the recommended power supplies and ground and DDR_ZQ (LPDDR4 SDRAM Calibration Reference Resistor).

Follow the recommendations in the device-specific data sheet (*AM62x Sitara Processor*) to connect the recommended DDR0_CAL0 (IO Pad Calibration Resistor).

Follow the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* and SK schematic to connect the LPDDR4 reset resistor (DDR0_RESET0_n).

Note

External memory (DDR) interface is not supported.

11.3 High-Speed Differential Signal Routing Guidelines

The *High-Speed Interface Layout Guidelines* application note provides guidelines for routing the high-speed differential signals. Guidelines include PCB layer stack-up, PCB material selection guidance as well as routing skew, length, and spacing guidelines. Any follow-up design support that may be required is provided for custom board designs that follow *High-Speed Interface Layout Guidelines*.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

Note

Consider using the *Starter Kit SK-AM62B-P1* and *Starter Kit SK-AM62-LP* SK layouts for reference (as required for ALW and AMC packages) during custom board design.

11.4 Processor-Specific SK Board Layout

The processor-specific SK board layout can be used as reference when doing a custom board layout or the SK board layout can be reused and required modifications can be made. The required simulations has been performed for all the high-speed interfaces on the SK board. For the peripheral the recommendations is to follow general board layout guidelines.

Below FAQ provides links to some of the available TI high-speed guidelines that can be referenced during the layout stage:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines

11.5 Custom Board Layer Count and Layer Stack-up

11.5.1 AM625 / AM623 / AM620-Q1 / AM625-Q1

One of the important requirement to be considered in determining layer count is the number of layers required to implement the high-speed DDR4 or LPDDR4 memory interface. Following the recommended layout guidelines typically requires the number of layers used in the Starter Kit (TI recommended) or the layers recommended in the *AM62 Escape Routing for PCB Design* / *AM62x (AMC) Escape Routing for PCB Design* application note. Optimization of layer count can be considered based on the custom board design functionalities.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for further guidance and recommendations for implementing the DDR4 or LPDDR4 memory interface.

AM62 Escape Routing for PCB Design application note can be used as a guideline during custom board layout. Use of TI Via Channel Array (VCA) technology (for ALW package) supports further layer optimization.

11.5.2 AM625SIP

Integration of LPDDR4 optimizes simulation, design and layout efforts. Integrated LPDDR4 provides flexibility in optimizing the layer count.

AM62x SiP Escape Routing for PCB Design application note can be used as a guideline during custom board layout that discusses a 4-layer escape for custom board design. Use of TI Via Channel Array (VCA) technology (for AMK package) supports further layer optimization.

11.5.3 Simulation Recommendations

Simulation is recommended for any layout changes or optimizations done with respect to the SK layout.

11.6 DDR-MARGIN-FW

The DDR margin firmware and supporting scripts allow visualization and measurement of system margin in the DDR interface on board. These tools enable probe-less measurement of critical data signals to understand if the custom board design follows the recommended design guidelines of the interface.

DDR-MARGIN-FW - Firmware and scripts to measure system DDR margin

For more information, see the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Question about AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP DDR MARGIN TEST Tool

11.7 Reference for Steps to be Followed for Running Board Simulation

To get an overview of the board extraction, simulation, and analysis methodologies for LPDDR4 memory interface, see the *LPDDR4 Board Design Simulations* chapter of the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62L / AM62P / AM62P-Q1 / AM64x / AM243x Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM243x (ALV), AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px

11.8 Software Development Training (Academy) for Processors

Academy (online easy-to-use training modules for TI AM62x and AM64x) is a great resource for developers to learn about the Sitara processor platform.

AM62x Academy

Look for AM62x Academy Designed to simplify and accelerate custom AM62x development.

12 Custom Board Assembly and Testing

The next phase of custom board design is board, assembly and bring-up, functional testing, software integration testing and performance testing.

The recommendation is to, verify that components marked as DNP or DNI in the design are not populated before applying power supply to the custom board.

The recommendation is to not connect any external inputs to the processor IOs before the processor IO supplies ramp (most processor IOs are not fail-safe, refer device-specific data sheet for available fail-safe IOs).

The recommendation is to verify the IO level compatibility when external inputs are directly connected to processor inputs. The recommendation is to provide provision to add an external ESD protection (as required) on-board or on the interface board.

The recommendation is to verify that none of the processor IO pullups have the supply rail referenced to the power source that is available before the processor IO supplies ramp.

12.1 Custom Board Bring-up Tips and Debug Guidelines

See the following FAQs during board bring-up:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Circuit Optimization of Custom board hardware design

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px)

13 Processor (Device) Handling and Assembly

Moisture Sensitivity Level (MSL) rating/Peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, lead finish/ball material and the recommended MSL rating/Peak reflow to be followed.

For more information, see the following links:

AM625 Ordering and quality

AM623 Ordering and quality

AM620-Q1 Ordering and quality

AM625-Q1 Ordering and quality

AM625SIP Ordering and quality

13.1 Processor (Device) Soldering Recommendations

Note the MSL rating/Peak reflow recommendation on TI.com for the selected processor.

13.1.1 Additional References

For information on Moisture sensitivity level, see the following:

MSL Ratings and Reflow Profiles

Moisture sensitivity level search.

14 References

14.1 AM625SIP

- Texas Instruments: *AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM*
- Texas Instruments: *Starter Kit SK-AM62-SIP*
- Texas Instruments: *AM62x SiP Escape Routing for PCB Design*
- Texas Instruments: *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*
- Texas Instruments: *Powering the AM625SIP With the TPS65219 PMIC*
- Texas Instruments: *SK-AM62-SIP Design Package Folder and Files List*

14.2 AM625 / AM623

- Texas Instruments: *Starter Kit SK-AM62B-P1*
- Texas Instruments: *AM62 Escape Routing for PCB Design*
- Texas Instruments: *SK-AM62B-P1 Design Package Content Overview (Rev. A)*
- Texas Instruments: *SK-AM62B Design Package Folder and Files List*

14.3 AM620-Q1 / AM625-Q1

- Texas Instruments: *Starter Kit SK-AM62-LP*
- Texas Instruments: *AM62x (AMC) Escape Routing for PCB Design*
- Texas Instruments: *SK-AM62-LP Design Package Content Overview*

14.4 AM625 / AM623 / AM620-Q1 / AM625-Q1

- Texas Instruments: *AM62x, AM62Lx DDR Board Design and Layout Guidelines*

14.5 Common for all AM62x family of processors

- Texas Instruments: *AM62x Sitara Processor Data Sheet*
- Texas Instruments: *AM62x Silicon Errata*
- Texas Instruments: *AM62x Sitara Processor Technical Reference Manual*
- Texas Instruments: *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP Processor Family Schematic Design Guidelines and Schematic Review Checklist*

- Texas Instruments: *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP, AM62A3, AM62A7, AM62A7-Q1, AM62A1-Q1, AM62D-Q1, AM62P-Q1 Schematic, Design Guidelines and Review Checklist*
- Texas Instruments, *Sitara AM62x Benchmarks*
- Texas Instruments: *AM62x Power Consumption*
- Texas Instruments: *AM62x Maximum Current Ratings*
- Texas Instruments: *AM62x Power Estimation Tool*
- Texas Instruments: *Powering the AM62x With the TPS65219 PMIC*
- Texas Instruments: *Discrete Power Solution for AM62x*
- Texas Instruments: *Enabling Low Power Embedded Systems With AM62x Processors*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*
- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto 7 DDRSS Register Configuration Tool*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Using IBIS Models for Timing Analysis*
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*

15 Terminology

BSDL	Boundary-Scan Description Language
CAN-FD	Controller Area Network Flexible Data-Rate
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
CSIRX	Camera Streaming Interface Receiver
DPI	Display Parallel Interface
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECAD	Electronic Computer Aided Design
ECAP	enhanced Capture
ECC	Error-Correcting Code
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EPWM	enhanced Pulse-Width Modulator
EQEP	enhanced Quadrature Encoder Pulse
GEMAC	Gigabit Ethernet Media Access Controller
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High-Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification

IEP	Industrial Ethernet Peripheral
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
MCAN	Modular Controller Area Network
MCASP	Multichannel Audio Serial Ports
MCU	Micro Controller Unit
MMC	Multi-Media Card
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
OLDI	Open LVDS Display Interface
OSPI	Octal Serial Peripheral Interface
OTP	One-Time Programmable
PCB	Printed Circuit Board
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
PRUSS	Programmable Real-Time Unit Subsystem
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select Input
TRM	Technical Reference Manual
TRSTn	Test Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCA	Via Channel Array
WKUP	Wakeup
XDS	eXtended Development System

16 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2025) to Revision E (October 2025) **Page**

- (Introduction): Added ALW Q1 information.......... 3