TDA4VPE-Q1, TDA4APE-Q1 Jacinto™ Automotive Processors

1 Features

Processor cores:

- Up to Three C7x floating point, vector DSP, up to 1.0GHz, 240GFLOPS, 768GOPS
- Up to Two Deep-learning matrix multiply accelerator (MMAv2), up to 16TOPS (8b) at 1.0GHz
- Up to Two Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators
- Depth and Motion Processing Accelerators (DMPAC)
- Four Arm® Cortex®-A72 microprocessor subsystem at up to 2.0GHz
  - 2MB shared L2 cache per quad-core Cortex®-A72 cluster
  - 32KB L1 DCache and 48KB L1 ICache per Cortex®-A72 core
- Eight Arm® Cortex®-R5F MCUs at up to 1.0GHz
  - 32K I-Cache, 32K D-Cache, 64K L2 TCM
  - Two Arm® Cortex®-R5F MCUs in isolated MCU subsystem
  - Six Arm® Cortex®-R5F MCUs in general compute partition
- GPU IMG BXS-4-64, 256kB Cache, up to 800MHz, 50GFLOPS, 4GTexels/s (**TDA4VPE**)
- Custom-designed interconnect fabric supporting near max processing entitlement

Memory subsystem:

- Up to 8MB of on-chip L3 RAM with ECC and coherency
  - ECC error protection
  - Shared coherent cache
  - Supports internal DMA engine
- Up to Two External Memory Interface (EMIF) modules with ECC
  - Supports LPDDR4 memory types
  - Supports speeds up to 4266MT/s
  - Up to 2x32-b bus with inline ECC up to 34GB/s
- General-Purpose Memory Controller (GPMC)
- 3x512KB on-chip SRAM in MAIN domain, protected by ECC

Functional Safety:

- Functional Safety-Compliant targeted (on select part numbers)
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262/IEC 61508 functional safety system design up to ASIL D/SIL 3
  - Systematic capability up to ASIL-D/SIL-3
  - Hardware integrity up to ASIL-D/SIL-3for MCU Domain
  - Hardware integrity up to ASIL-B/SIL-2 for Main Domain
  - Hardware integrity up to ASIL-D/SIL-3 for Extended MCU (EMCU) portion of the Main Domain
- Safety-related certification
  - ISO 26262/IEC 61508 certification up to ASIL D/SIL 3 by TÜV SÜD
- AEC-Q100 qualified on part number variants ending in Q1

Device security (on select part numbers):

- Secure boot with secure run-time support
- Customer programmable root key, up to RSA-4K or ECC-512
- Embedded hardware security module
- Crypto hardware accelerators – PKA with ECC, AES, SHA, RNG, DES and 3DES

High speed serial interfaces:

- Integrated Ethernet switch supporting 4 external ports
  - Two ports support 5Gb, 10Gb USXGMII/XFI
  - All ports support 1Gb, 2.5Gb SGMII
  - All ports can support QSGMII. A maximum of 1 QSGMII can be enabled and uses all 4 internal lanes
- Up to 2x2L/1x4L PCI-Express® (PCIe) Gen3 controllers
  - Gen1 (2.5GT/s), Gen2 (5.0GT/s), and Gen3 (8.0GT/s) operation with auto-negotiation
- One USB 3.0 dual-role device (DRD) subsystem
  - Enhanced SuperSpeed Gen1 Port
  - Supports Type-C switching
  - Independently configurable as USB host, USB peripheral, or USB DRD
- Three CSI2.0 4L Camera Serial interface RX (CSI-RX) plus two CSI2.0 4L TX (CSI-TX) with DPHY
  - MIPI CSI 1.3 Compliant + MIPI-DPHY 1.2
  - CSI-RX supports for 1,2,3, or 4 data lane mode up to 2.5Gbps per lane
  - CSI-TX supports for 1,2, or 4 data lane mode up to 2.5Gbps per lane

Ethernet:

- Two RGMII/RMII interfaces

Automotive interfaces:

- Twenty Modular Controller Area Network (MCAN) modules with full CAN-FD support

Display subsystem:

- Two DSI 4L TX (up to 2.5k)
- One eDP/DP interface with Multi-Display Support (MST)
- One DPI

Audio interfaces:

- Five Multichannel Audio Serial Port (MCASP) modules

Video acceleration:

- H.264/H.265 Encode/Decode, up to 960MP/s

Flash memory interfaces:

- Embedded MultiMediaCard Interface (eMMC™ 5.1)
- One Secure Digital® 3.0 / Secure Digital Input Output 3.0 interfaces (SD3.0/SDIO3.0
- Universal Flash Storage (UFS 2.1) interface with two lanes
- Two independent flash interfaces configured as
  - One OSPI or HyperBus™ or QSPI flash interfaces, and
  - One QSPI flash interface

System-on-Chip (SoC) architecture:

- 16-nm FinFET technology
- 27mm × 27mm, 0.8-mm pitch, 1063-pin FCBGA (AND), enables IPC class 3 PCB routing

TPS6594-Q1 Companion Power Management ICs (PMIC):

- Functional Safety-Compliant support up to ASIL D/SIL 3
- Flexible mapping to support different use cases

2 Applications

- Automotive:
- Advanced surround view and park assistance systems
- Autonomous sensor fusion / perception systems including camera, radar and LiDAR sensors
- Mono and multi-sensor Front camera systems
- Next generation eMirror systems
- Off-highway vehicle control
- ADAS Domain Controller

3 Description

The TDA4VPE-Q1 TDA4APE-Q1 processor family is based on the evolutionary Jacinto™ 7 architecture, targeted at ADAS and Autonomous Vehicle (AV) applications and built on extensive market knowledge accumulated over a decade of TI's leadership in the ADAS processor market. The unique combination high-performance compute, deep-learning engine, dedicated accelerators for signal and image processing in an functional safety compliant targeted architecture make the TDA4VPE-Q1 TDA4APE-Q1 devices a great fit for several imaging, vision, radar, sensor fusion and AI applications such as: Robotics, Mobile machineries, Off-highway vehicle controller, Machine Vision, AI BOX, Gateways, Retail automation, Medical Imaging, and so on. The TDA4VPE-Q1 TDA4APE-Q1 provides high performance compute for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced automotive platforms supporting multiple sensor modalities in centralized ECUs or stand-alone sensors. Key cores include next generation DSP with scalar and vector cores, dedicated deep learning and traditional algorithm accelerators, latest Arm and GPU processors for general compute, an integrated next generation imaging subsystem (ISP), video codec, Ethernet hub and isolated MCU island. All protected by automotive grade safety and security hardware accelerators.

Key Performance Cores Overview

The "C7x" next generation DSP combines TI's industry leading DSP and EVE cores into a single higher performance core and adds floating point vector calculation capabilities, enabling backward compatibility for legacy code while simplifying software programming. A single instance of the new "MMAv2" deep learning accelerator enables performance up to 8 TOPS within the lowest power envelope in the industry when operating at the typical automotive worst case junction temperature of 125°C. The dedicated ADAS/AV hardware accelerators provide vision pre-processing plus distance and motion processing with no impact on system performance.

General Compute Cores and Integration Overview

Separate four core cluster configuration of Arm® Cortex®-A72 facilitates multi-OS applications with minimal need for a software hypervisor. Four Arm® Cortex®-R5F subsystems enable low-level, timing critical processing tasks to leave the Arm® Cortex®-A72's unencumbered for applications. The integrated IMG BXS-4-64 GPU offers up to 50GFLOPS to enable dynamic 3D rendering for enhanced viewing applications. Building on the existing world-class ISP, TI's 7th generation ISP includes flexibility to process a broader sensor suite, support for higher bit depth, and features targeting analytics applications. Integrated diagnostics and safety features support operations up to ASIL-D/SIL-3 levels while the integrated security features protect data against modern day attacks. To enable systems requiring heavy data bandwidth, a PCIe hub and Gigabit Ethernet switch are included along with CSI-2 ports to support throughput for many sensor inputs. To further the integration, the TDA4VPE-Q1 TDA4APE-Q1 family also includes an MCU island eliminating the need for an external system microcontroller.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TDA4VPE-Q1	AND (FCBGA, 1063)	27mm x 27mm
TDA4APE-Q1	AND (FCBGA, 1063)	27mm x 27mm
XJ742S2	AND (FCBGA, 1063)	27mm x 27mm

(1) For more information, see Section 10, *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

3.1 Functional Block Diagram

Figure 3-1 is functional block diagram for the device.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the TDA4VH Software Build Sheet (PROCESSOR-SDK-J742S2).

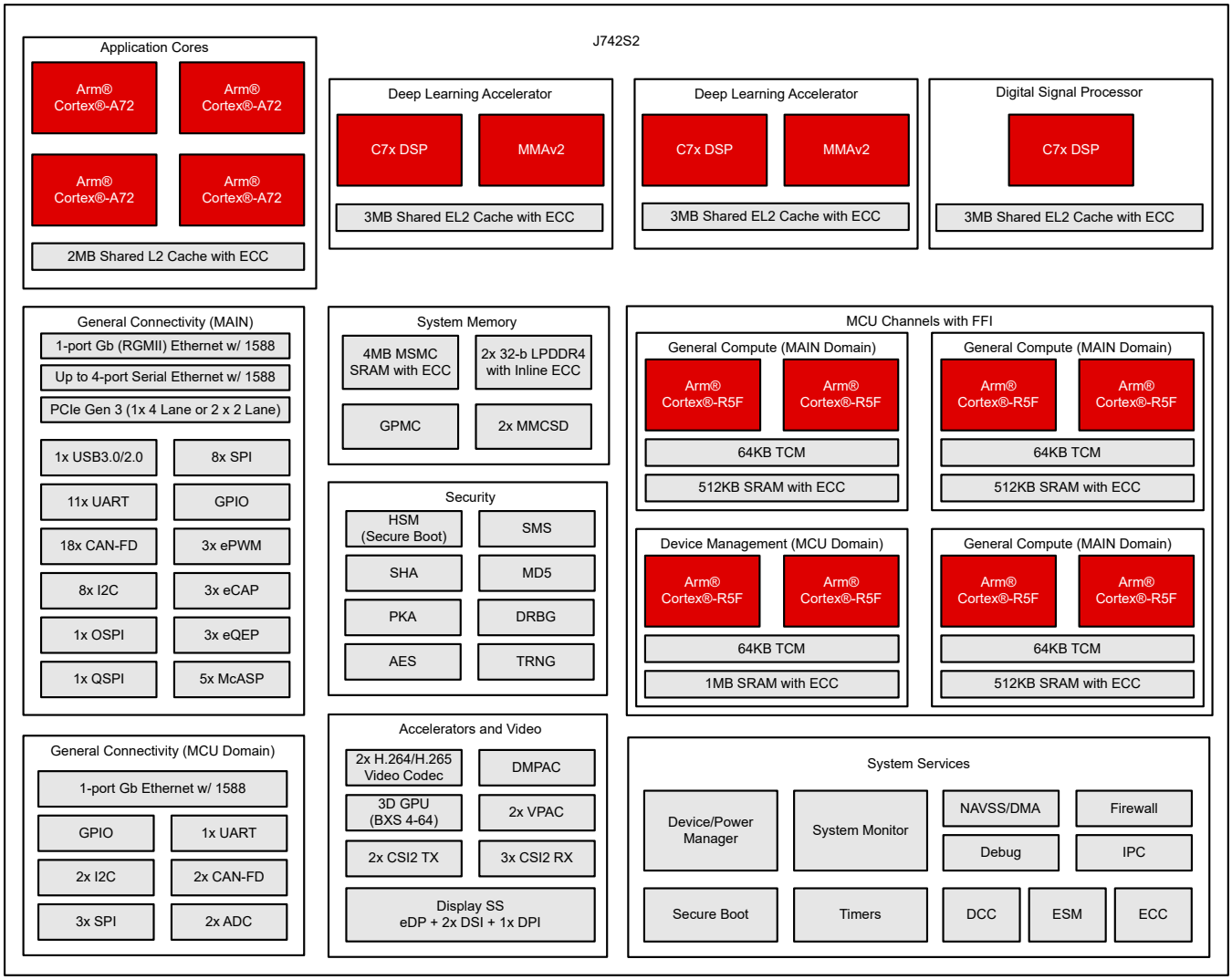

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 shows the features of the SoC.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the TDA4VH Software Build Sheet (PROCESSOR-SDK-J742S2).

Table 4-1. Device Comparison

FEATURES[9]	REFERENCE NAME	TDA4VPE6	TDA4APE6	TDA4VPE4	TDA4APE4
FEATURES					
PROCESSORS AND ACCELERATORS					
Speed Grades		T	T	T	T
Arm Cortex-A72 Microprocessor Subsystem	Arm A72	Quad Core[12]			
Arm Cortex-R5F	Arm R5F	Octal Core			
	Lockstep	Optional[1]			
Security Management	SMS	Yes			
Security Accelerators	SA	Yes			
C7x Floating Point, Vector DSP	C7x DSP	Tri Core			
Deep Learning Accelerator	MMA	Dual Core			
Graphics Accelerator IMG BXS-4-64	GPU	Yes	No	Yes	No
Depth and Motion Processing Accelerators	DMPAC	Yes			
Vision Processing Accelerators	VPAC	2		1	
Video Encoder / Decoder	VENC/ VDEC	Enc/Dec 960MP/s		Enc/Dec 480MP/s	
SAFETY AND SECURITY					
Safety Targeted	Safety	Optional[1]		Optional[1]	
Device Security	Security	Optional[2]		Optional[2]	
AEC-Q100 Qualified	Q1	Optional[3]		Optional[3]	
PROGRAM AND DATA STORAGE					
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	3x512KB SRAM		3x512KB SRAM	
On-Chip Shared Memory (RAM) in MCU Domain	MCU_MSRAM	1MB SRAM		1MB SRAM	
Multicore Shared Memory Controller	MSMC	8MB (On-Chip SRAM with ECC)		4MB (On-Chip SRAM with ECC)	
LPDDR4 DDR Subsystem	DDRSS0[5]	32-b w/ inline ECC		32-b w/ inline ECC	
	DDRSS1[5]	32-b w/ inline ECC		32-b w/ inline ECC	
	DDRSS2[4] [5]	No			
	DDRSS3[4] [5]	No			
	SECDED	7-Bit			
General-Purpose Memory Controller	GPMC	Yes			
PERIPHERALS					
Display Subsystem	DSS	Yes		Yes	
	DSI 4L TX	2		2	
	eDP 4L	1		1	
	DPI	1		1	
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	20		20	
General-Purpose I/O	GPIO	155		155	
Inter-Integrated Circuit Interface	I2C	10		10	

Table 4-1. Device Comparison (continued)

FEATURES[9]	REFERENCE NAME	TDA4VPE6	TDA4APE6	TDA4VPE4	TDA4APE4
Improved Inter-Integrated Circuit Interface	I3C	1		1	
Analog-to-Digital Converter	ADC	2		2	
Capture Subsystem with Camera Serial Interface (CSI2)	CSI2.0 4L RX	3		3	
	CSI2.0 4L TX	2		2	
Multichannel Serial Peripheral Interface	MCSPI	11		11	
Multichannel Audio Serial Port	MCASP0	16 Serializers		16 Serializers	
	MCASP1	5 Serializers		5 Serializers	
	MCASP2	5 Serializers		5 Serializers	
	MCASP3	3 Serializers		3 Serializers	
	MCASP4	5 Serializers		5 Serializers	
MultiMedia Card/ Secure Digital Interface	MMCSD0	eMMC (8-bits)		eMMC (8-bits)	
	MMCSD1	SD/SDIO (4-bits)		SD/SDIO (4-bits)	
Universal Flash Storage	UFS 2L	Yes		Yes	
Flash Subsystem (FSS)	OSPI0	8-bits[8]		8-bits[8]	
	OSPI1[10]	4-bits		4-bits	
	HyperBus	Yes[8]		Yes[8]	
4x PCI Express Port with Integrated PHY	PCIE	*1x4L or 2x2L* [6] [11]		*1x4L or 2x2L* [6] [11]	
Ethernet Interfaces	MCU CPSW2G	RMII or RGMII		RMII or RGMII	
	MAIN CPSW2G	RMII or RGMII		RMII or RGMII	
	CPSW9G	4 port SERDES[6] [7]		4 port SERDES[6] [7]	
General-Purpose Timers	TIMER	30		30	
Enhanced High Resolution Pulse-Width Modulator Module	eHRPWM	6		6	
Enhanced Capture Module	eCAP	3		3	
Enhanced Quadrature Encoder Pulse Module	eQEP	3		3	
Universal Asynchronous Receiver and Transmitter	UART	12		12	
Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY	USB0	Yes[6]		Yes[6]	

(1) Safety features including R5F Lockstep and SIL/ASIL ratings are only applicable to select part number variants as indicated by the Device Type (Y) identifier in the Nomenclature Description table.
(2) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the Nomenclature Description table.
(3) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Nomenclature Description table.
(4) DDRSS2 and DDRSS3 are not available on the 27mm package variant of this SoC. DDR2/DDR3 should be not be used if software compatibility is desired with systems that use the 27mm package
(5) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces.
(6) DP, SGMII, USB3.0, and PCIE share total of 8 or 12 SerDes lanes:
- TDA4xPE6 does not support SERDES2 lanes
- TDA4xPE4 does not support SERDES0 and SERDES2 lanes
- TDA4xPE4 has additional muxing limitations for PCIe and SGMII on available SERDES lanes. SERDES and Mux limitations are shown in Pin Attributes Table "VPE4 APE4" column.

(7) **TDA4xPE** CPSW supports up to 4 ports.
- TDA4xPE6 allows additional pin muxing flexibility compared to TDA4xPE4
- TDA4xPE6 allows the system designer to choose based on any available PORTS, but must limit the total number of ports used to four or fewer

- TDA4xPE4 reduces the pin muxing availability as shown in Pin Attributes Table "VPE4 APE4" column

The following instances, signals, and modes of operation are available across the 8 ports:

- PORT1 **Signals**: SGMII1, **Modes**: One of *5Gb, 10Gb USXGMII/XFI*, 2.5Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII
- PORT2 **Signals**: SGMII2, **Modes**: One of *5Gb, 10Gb USXGMII/XFI*, 2.5Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII
- PORTn (n=3 thru 8) **Signals**: SGMIIn, **Modes**: One of 2.5Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII

If QSGMII is used on any SGMII Port 1 thru 4, then SGMII1/2/3/4 cannot be used for Ethernet functionality since all 4 internal CPSW ports map to the selected QSGMII SERDES port.
If QSGMII is used on any SGMII Port 5 thru 8, then SGMII5/6/7/8 cannot be used for Ethernet functionality since all 4 internal CPSW ports map to the selected QSGMII SERDES port.

(8) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.
(9) XJ742S2 is the base part number for the superset device. Software should constrain the features used to match the intended production device.
(10) OSPI1 module only pins out 4 pins and is referred to as QSPI in some contexts.
(11) **TDA4xPE** PCIe supports 1x4L or 2x2L options.

- TDA4xPE6 allows additional pin muxing flexibility compared to the TDA4xPE4 device
- TDA4xPE6 allows the system designer to choose any available PCIe instances or available PORTS but must limit to a maximum of 1x4L or 2x2L
- TDA4xPE4 reduces the pin muxing availability as shown in Pin Attributes Table "VPE4 APE4" column

(12) The A72SS Quad Core variant provides a single quad core cluster, namely A72SS0_CORE[3:0].

5 Terminal Configuration and Functions

5.1 Pin Diagrams

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 5-1 shows the ball locations for the 1063-ball flip chip ball grid array (FCBGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjuction with Table 5-1 through Table 5-118 (*Pin Attributes* table and all *Signal Descriptions* tables, including the *Pin Connectivity Requirements* table).

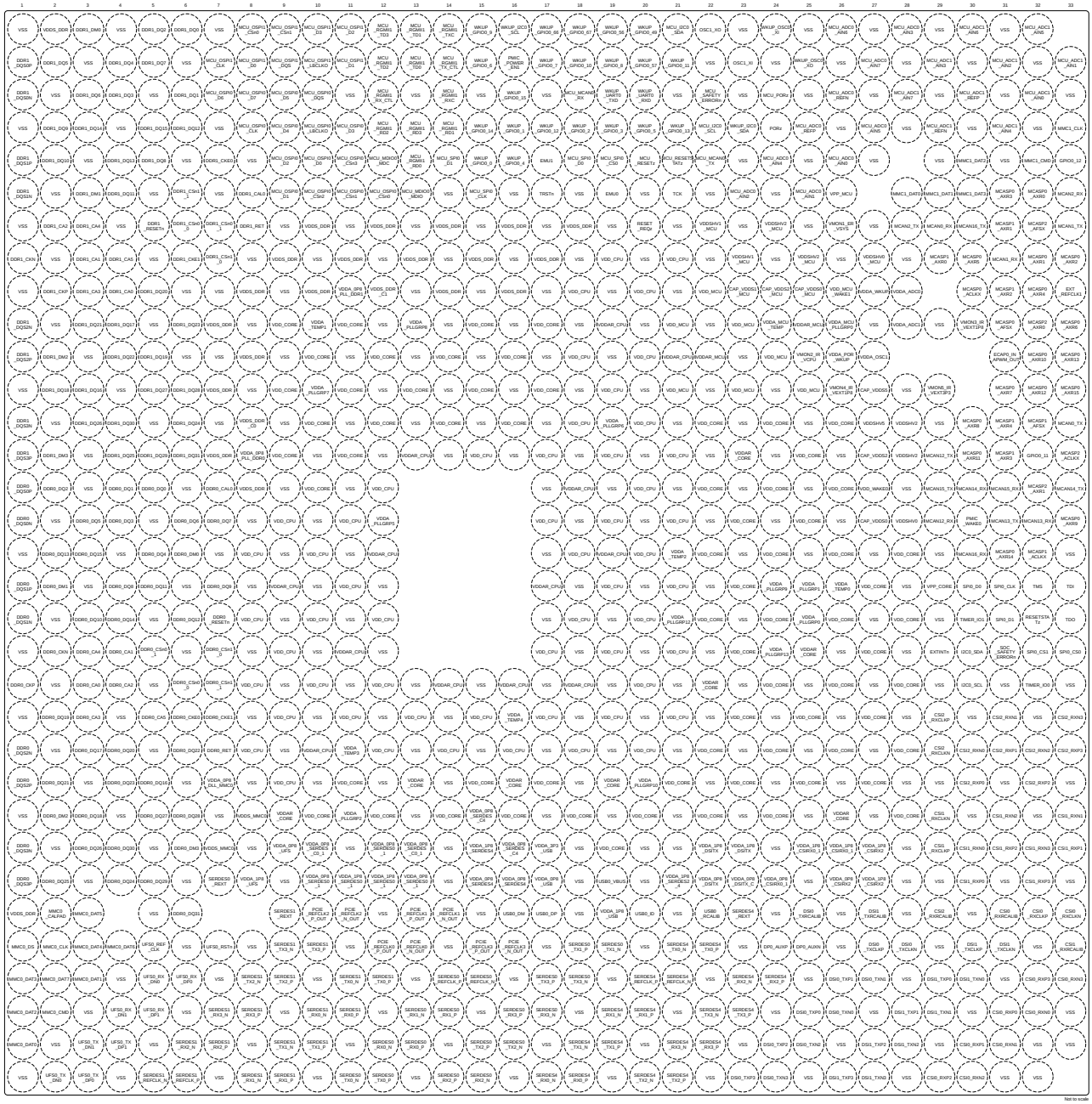


Figure 5-1. AND FCBGA-N1063 Pin Diagram (Top View)

5.2 Pin Attributes

The following list describes the contents of each column in the Table 5-1, *Pin Attributes (AND Package)* table:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

Note

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

The Table 5-1, *Pin Attributes (AND Package)* table only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

Note

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programable via MUXMODE.
   d. An empty box means Not Applicable.

Note

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **VPE4 APE4:** Identifies the suppported MUXMODE for **TDA4VPE4**, **TDA4APE4** devices. "No" means this MUXMODE is not supported. An empty box means supported.
6. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function

- OZ = Output with three-state output function
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor.

7. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box means Not Applicable.
8. **BALL STATE DURING RESET (RX/TX/PULL):** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - Low: The output buffer is **enabled** and drives V_{OL}.
     - High: The output buffer is **enabled** and drives V_{OH}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off**.
     - Up: Internal **pull-up** resistor is turned on.
     - Down: Internal **pull-down** resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
9. **BALL STATE AFTER RESET (RX/TX/PULL):** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off**.
     - Up: Internal **pull-up** resistor is turned on.
     - Down: Internal **pull-down** resistor is turned on.
     - NA: Not Applicable.
   - An empty box, NA, or "-" means Not Applicable.
10. **MUX MODE AFTER RESET:** The value found in this column defines the **default** pin multiplexed signal function after MCU_PORz is deasserted.

    An empty box, NA, or "-" means Not Applicable.
11. **I/O VOLTAGE VALUE**: This column describes I/O operating voltage options of the respective power supply, when applicable.

    An empty box means Not Applicable.

For more information, see valid operating voltage range(s) defined for each power supply in Section 6.4, *Recommended Operating Conditions*.

12. **POWER:** The power supply of the associated I/O, when applicable.

    An empty box means Not Applicable.

13. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box means Not Applicable.

    For more information, see the hysteresis values in Section 6.6, *Electrical Characteristics*.

14. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in Section 6.6, *Electrical Characteristics*.

15. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box means No internal pull.

    Note

    Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

    When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

16. **PADCONFIG Register:** Name of the IO pad configuration register associated with Ball.
17. **PADCONFIG Address:** Physical address of the IO pad configuration register associated with Ball.

Table 5-1. Pin Attributes (AND Package)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
T27	CAP_VDDS0	CAP_VDDS0			CAP									
J25	CAP_VDDS0_MCU	CAP_VDDS0_MCU			CAP									
J23	CAP_VDDS1_MCU	CAP_VDDS1_MCU			CAP									
P27	CAP_VDDS2	CAP_VDDS2			CAP									
J24	CAP_VDDS2_MCU	CAP_VDDS2_MCU			CAP									
M27	CAP_VDDS5	CAP_VDDS5			CAP									
AH33	CSI0_RXCLKN	CSI0_RXCLKN			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AH32	CSI0_RXCLKP	CSI0_RXCLKP			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AH31	CSI0_RXRCALIB	CSI0_RXRCALIB			A					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AE29	CSI1_RXCLKN	CSI1_RXCLKN			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AF29	CSI1_RXCLKP	CSI1_RXCLKP			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AJ33	CSI1_RXRCALIB	CSI1_RXRCALIB			A					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AC29	CSI2_RXCLKN	CSI2_RXCLKN			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AB29	CSI2_RXCLKP	CSI2_RXCLKP			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AH29	CSI2_RXRCALIB	CSI2_RXRCALIB			A					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AL32	CSI0_RXN0	CSI0_RXN0			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AM31	CSI0_RXN1	CSI0_RXN1			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AN30	CSI0_RXN2	CSI0_RXN2			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AK33	CSI0_RXN3	CSI0_RXN3			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AL31	CSI0_RXP0	CSI0_RXP0			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AM30	CSI0_RXP1	CSI0_RXP1			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AN29	CSI0_RXP2	CSI0_RXP2			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AK32	CSI0_RXP3	CSI0_RXP3			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AF30	CSI1_RXN0	CSI1_RXN0			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AE33	CSI1_RXN1	CSI1_RXN1			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AE31	CSI1_RXN2	CSI1_RXN2			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AF32	CSI1_RXN3	CSI1_RXN3			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AG30	CSI1_RXP0	CSI1_RXP0			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AF33	CSI1_RXP1	CSI1_RXP1			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AF31	CSI1_RXP2	CSI1_RXP2			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AG32	CSI1_RXP3	CSI1_RXP3			I					1.8 V	VDDA_0P8_CSIRX0_1 / VDDA_1P8_CSIRX0_1		D-PHY	
AC30	CSI2_RXN0	CSI2_RXN0			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AB31	CSI2_RXN1	CSI2_RXN1			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AC32	CSI2_RXN2	CSI2_RXN2			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AB33	CSI2_RXN3	CSI2_RXN3			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AD30	CSI2_RXP0	CSI2_RXP0			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AC31	CSI2_RXP1	CSI2_RXP1			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AD32	CSI2_RXP2	CSI2_RXP2			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
AC33	CSI2_RXP3	CSI2_RXP3			I					1.8 V	VDDA_0P8_CSIRX2 / VDDA_1P8_CSIRX2		D-PHY	
Y2	DDR0_CKN	DDR0_CKN			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AA1	DDR0_CKP	DDR0_CKP			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
W7	DDR0_RESETn	DDR0_RESETn			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AC7	DDR0_RET	DDR0_RET			I					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
H1	DDR1_CKN	DDR1_CKN			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
J2	DDR1_CKP	DDR1_CKP			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G5	DDR1_RESETn	DDR1_RESETn			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G8	DDR1_RET	DDR1_RET			I					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
AA3	DDR0_CA0	DDR0_CA0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
Y4	DDR0_CA1	DDR0_CA1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AA4	DDR0_CA2	DDR0_CA2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AB3	DDR0_CA3	DDR0_CA3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
Y3	DDR0_CA4	DDR0_CA4			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AB5	DDR0_CA5	DDR0_CA5			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
R7	DDR0_CAL0	DDR0_CAL0			A					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AB6	DDR0_CKE0	DDR0_CKE0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AB7	DDR0_CKE1	DDR0_CKE1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AA6	DDR0_CSn0_0	DDR0_CSn0_0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
Y5	DDR0_CSn0_1	DDR0_CSn0_1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
Y7	DDR0_CSn1_0	DDR0_CSn1_0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AA7	DDR0_CSn1_1	DDR0_CSn1_1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
U6	DDR0_DM0	DDR0_DM0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
V2	DDR0_DM1	DDR0_DM1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AE2	DDR0_DM2	DDR0_DM2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AF6	DDR0_DM3	DDR0_DM3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
R5	DDR0_DQ0	DDR0_DQ0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
R4	DDR0_DQ1	DDR0_DQ1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
R2	DDR0_DQ2	DDR0_DQ2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
T4	DDR0_DQ3	DDR0_DQ3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
U5	DDR0_DQ4	DDR0_DQ4			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
T3	DDR0_DQ5	DDR0_DQ5			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
T6	DDR0_DQ6	DDR0_DQ6			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
T7	DDR0_DQ7	DDR0_DQ7			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
V4	DDR0_DQ8	DDR0_DQ8			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
V7	DDR0_DQ9	DDR0_DQ9			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
W3	DDR0_DQ10	DDR0_DQ10			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
V5	DDR0_DQ11	DDR0_DQ11			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
W6	DDR0_DQ12	DDR0_DQ12			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
U2	DDR0_DQ13	DDR0_DQ13			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
W4	DDR0_DQ14	DDR0_DQ14			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
U3	DDR0_DQ15	DDR0_DQ15			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AD5	DDR0_DQ16	DDR0_DQ16			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AC3	DDR0_DQ17	DDR0_DQ17			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AE3	DDR0_DQ18	DDR0_DQ18			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AB2	DDR0_DQ19	DDR0_DQ19			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AC4	DDR0_DQ20	DDR0_DQ20			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AD2	DDR0_DQ21	DDR0_DQ21			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AC6	DDR0_DQ22	DDR0_DQ22			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AD4	DDR0_DQ23	DDR0_DQ23			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AG4	DDR0_DQ24	DDR0_DQ24			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AG2	DDR0_DQ25	DDR0_DQ25			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AF3	DDR0_DQ26	DDR0_DQ26			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AE5	DDR0_DQ27	DDR0_DQ27			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AE6	DDR0_DQ28	DDR0_DQ28			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AG5	DDR0_DQ29	DDR0_DQ29			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AF4	DDR0_DQ30	DDR0_DQ30			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AH6	DDR0_DQ31	DDR0_DQ31			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
T1	DDR0_DQS0N	DDR0_DQS0N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
R1	DDR0_DQS0P	DDR0_DQS0P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
W1	DDR0_DQS1N	DDR0_DQS1N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
V1	DDR0_DQS1P	DDR0_DQS1P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AC1	DDR0_DQS2N	DDR0_DQS2N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AD1	DDR0_DQS2P	DDR0_DQS2P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AF1	DDR0_DQS3N	DDR0_DQS3N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
AG1	DDR0_DQS3P	DDR0_DQS3P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C0		DDR	
J4	DDR1_CA0	DDR1_CA0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
H3	DDR1_CA1	DDR1_CA1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G2	DDR1_CA2	DDR1_CA2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
J3	DDR1_CA3	DDR1_CA3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G3	DDR1_CA4	DDR1_CA4			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
H4	DDR1_CA5	DDR1_CA5			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
F8	DDR1_CAL0	DDR1_CAL0			A					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
E7	DDR1_CKE0	DDR1_CKE0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
H6	DDR1_CKE1	DDR1_CKE1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G6	DDR1_CSn0_0	DDR1_CSn0_0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
G7	DDR1_CSn0_1	DDR1_CSn0_1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
H7	DDR1_CSn1_0	DDR1_CSn1_0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
F6	DDR1_CSn1_1	DDR1_CSn1_1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
A3	DDR1_DM0	DDR1_DM0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
F3	DDR1_DM1	DDR1_DM1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
L2	DDR1_DM2	DDR1_DM2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
P2	DDR1_DM3	DDR1_DM3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
A6	DDR1_DQ0	DDR1_DQ0			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
C6	DDR1_DQ1	DDR1_DQ1			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
A5	DDR1_DQ2	DDR1_DQ2			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
C4	DDR1_DQ3	DDR1_DQ3			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
B4	DDR1_DQ4	DDR1_DQ4			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
B2	DDR1_DQ5	DDR1_DQ5			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
C3	DDR1_DQ6	DDR1_DQ6			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
B5	DDR1_DQ7	DDR1_DQ7			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
E5	DDR1_DQ8	DDR1_DQ8			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
D2	DDR1_DQ9	DDR1_DQ9			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
E2	DDR1_DQ10	DDR1_DQ10			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
F4	DDR1_DQ11	DDR1_DQ11			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
D6	DDR1_DQ12	DDR1_DQ12			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
E4	DDR1_DQ13	DDR1_DQ13			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
D3	DDR1_DQ14	DDR1_DQ14			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
D5	DDR1_DQ15	DDR1_DQ15			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
M3	DDR1_DQ16	DDR1_DQ16			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
K4	DDR1_DQ17	DDR1_DQ17			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
M2	DDR1_DQ18	DDR1_DQ18			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
L5	DDR1_DQ19	DDR1_DQ19			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
J5	DDR1_DQ20	DDR1_DQ20			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
K3	DDR1_DQ21	DDR1_DQ21			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
L4	DDR1_DQ22	DDR1_DQ22			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
K6	DDR1_DQ23	DDR1_DQ23			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
N6	DDR1_DQ24	DDR1_DQ24			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
P4	DDR1_DQ25	DDR1_DQ25			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
N3	DDR1_DQ26	DDR1_DQ26			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
M5	DDR1_DQ27	DDR1_DQ27			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
M6	DDR1_DQ28	DDR1_DQ28			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
P5	DDR1_DQ29	DDR1_DQ29			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
N4	DDR1_DQ30	DDR1_DQ30			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
P6	DDR1_DQ31	DDR1_DQ31			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
C1	DDR1_DQS0N	DDR1_DQS0N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
B1	DDR1_DQS0P	DDR1_DQS0P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
F1	DDR1_DQS1N	DDR1_DQS1N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
E1	DDR1_DQS1P	DDR1_DQS1P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
K1	DDR1_DQS2N	DDR1_DQS2N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
L1	DDR1_DQS2P	DDR1_DQS2P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
N1	DDR1_DQS3N	DDR1_DQS3N			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
P1	DDR1_DQS3P	DDR1_DQS3P			IO					1.1 V	VDDS_DDR / VDDS_DDR_C1		DDR	
AJ25	DP0_AUXN	DP0_AUXN			IO					1.8 V	VDDA_1P8_SERDES2_4		AUX-PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AJ24	DP0_AUXP	DP0_AUXP			IO					1.8 V	VDDA_1P8_SERDES2_4		AUX-PHY	
AJ28	DSI0_TXCLKN	DSI0_TXCLKN			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI0_TXCLKN			O									
AJ27	DSI0_TXCLKP	CSI0_TXCLKP			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI0_TXCLKP			O									
AH25	DSI0_TXRCALIB	DSI0_TXRCALIB			A					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
AJ31	DSI1_TXCLKN	CSI1_TXCLKN			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXCLKN			O									
AJ30	DSI1_TXCLKP	DSI1_TXCLKP			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI1_TXCLKP			O									
AH27	DSI1_TXRCALIB	DSI1_TXRCALIB			A					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
AL26	DSI0_TXN0	CSI0_TXN0			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI0_TXN0			IO									
AK27	DSI0_TXN1	CSI0_TXN1			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI0_TXN1			O									
AM25	DSI0_TXN2	DSI0_TXN2			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI0_TXN2			O									
AN24	DSI0_TXN3	DSI0_TXN3			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI0_TXN3			O									
AL25	DSI0_TXP0	CSI0_TXP0			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI0_TXP0			IO									
AK26	DSI0_TXP1	DSI0_TXP1			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI0_TXP1			O									
AM24	DSI0_TXP2	DSI0_TXP2			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI0_TXP2			O									
AN23	DSI0_TXP3	CSI0_TXP3			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI0_TXP3			O									
AK30	DSI1_TXN0	CSI1_TXN0			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXN0			IO									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AL29	DSI1_TXN1	DSI1_TXN1			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI1_TXN1			O									
AM28	DSI1_TXN2	CSI1_TXN2			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXN2			O									
AN27	DSI1_TXN3	CSI1_TXN3			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXN3			O									
AK29	DSI1_TXP0	CSI1_TXP0			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXP0			IO									
AL28	DSI1_TXP1	CSI1_TXP1			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXP1			O									
AM27	DSI1_TXP2	CSI1_TXP2			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		DSI1_TXP2			O									
AN26	DSI1_TXP3	DSI1_TXP3			O					1.8 V	VDDA_0P8_DSITX / VDDA_0P8_DSITX_C / VDDA_1P8_DSITX		D-PHY	
		CSI1_TXP3			O									
L31	ECAP0_IN_APWM_OUT PADCONFIG PADCONFIG_49 0x0011C0C4	ECAP0_IN_APWM_OUT	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_AXR2	1		IO	0								
		CPTS0_RFT_CLK	2		I	0								
		MCAN12_TX	4		O									
		VOUT0_DATA23	5		O									
		GPMC0_AD5	6		IO	0								
		GPIO0_49	7		IO	pad								
		SPI6_D0	8		IO	0								
		SYNC0_OUT	9		O									
		TRC_DATA1	10		O									
		UART2_CTSn	11		I	1								
		CPTS0_HW1TSPUSH	12		I	0								
		I2C1_SCL	13		IOD	1								
		UART3_RXD	14		I	1								
F19	EMU0 PADCONFIG WKUP_PADCONFIG_75 0x4301C12C	EMU0	0		IO		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
E17	EMU1 PADCONFIG WKUP_PADCONFIG_76 0x4301C130	EMU1	0		IO		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
Y29	EXTINTn PADCONFIG PADCONFIG_0 0x0011C000	EXTINTn	0		I	1	Off / Off / NA	Off / SS / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO0_0	7		IO	pad								
J33	EXT_REFCLK1 PADCONFIG PADCONFIG_50 0x0011C0C8	EXT_REFCLK1	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_ACLKX	1		IO	0								
		VOUT0_DATA16	2		O									
		MCAN1_RX	4		I	1								
		GPMC0_AD6	6		IO	0								
		GPIO0_50	7		IO	pad								
		SYNC1_OUT	9		O									
		TRC_CLK	10		O									
		UART2_RTSn	11		O									
		CPTS0_HW2TSPUSH	12		I	0								
		I2C1_SDA	13		IOD	1								
		UART3_TXD	14		O									
P32	GPIO0_11 PADCONFIG PADCONFIG_11 0x0011C02C	MCAN17_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA18	2		O									
		GPMC0_A14	6		OZ									
		GPIO0_11	7		IO	pad								
		SPI7_CS3	8		IO	1								
		TRC_DATA25	10		O									
		GPMC0_CSn2	12		O									
		UART7_RXD	13		I	1								
		USB0_DRVVBUS	14		O									
E33	GPIO0_12 PADCONFIG PADCONFIG_12 0x0011C030	MCAN12_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA17	2		O									
		VOUT0_DATA22	5		O									
		GPMC0_AD4	6		IO	0								
		GPIO0_12	7		IO	pad								
		SPI6_CLK	8		IO	0								
		EQEP1_I	9		IO	0								
		TRC_DATA2	10		O									
		UART9_CTSn	11		I	1								
		UART6_RXD	12		I	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AA30	I2C0_SCL PADCONFIG PADCONFIG_56 0x0011C0E0	I2C0_SCL	0		IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO0_56	7		IO	pad								
Y30	I2C0_SDA PADCONFIG PADCONFIG_57 0x0011C0E4	I2C0_SDA	0		IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OPEN DRAIN	
		GPIO0_57	7		IO	pad								
G29	MCAN0_RX PADCONFIG PADCONFIG_26 0x0011C068	MCAN0_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_AXR1	1		IO	0								
		VOUT0_DATA3	2		O									
		GPMC0_AD15	6		IO	0								
		GPIO0_26	7		IO	pad								
		SPI5_CS0	8		IO	1								
		EHRPWM0_A	9		IO	0								
		TRC_DATA16	10		O									
		UART2_TXD	11		O									
		UART6_RTSn	12		O									
		SPI7_D0	13		IO	0								
N33	MCAN0_TX PADCONFIG PADCONFIG_25 0x0011C064	MCAN0_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AXR2	1		IO	0								
		VOUT0_DATA4	2		O									
		GPMC0_AD14	6		IO	0								
		GPIO0_25	7		IO	pad								
		SPI5_CS1	8		IO	1								
		EHRPWM0_B	9		IO	0								
		TRC_DATA11	10		O									
		UART2_RXD	11		I	1								
		UART6_CTSn	12		I	1								
		I2C3_SCL	13		IOD	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
H31	MCAN1_RX PADCONFIG PADCONFIG_28 0x0011C070	MCAN1_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_AXR3	1		IO	0								
		VOUT0_DATA1	2		O									
		VOUT0_DATA19	5		O									
		GPMC0_BE0n_CLE	6		O									
		GPIO0_28	7		IO	pad								
		SPI5_D0	8		IO	0								
		EHRPWM0_SYNCI	9		I	0								
		TRC_DATA5	10		O									
		UART3_RTSn	11		O									
G33	MCAN1_TX PADCONFIG PADCONFIG_27 0x0011C06C	MCAN1_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_AFSX	1		IO	0								
		VOUT0_EXTPCLKIN	2		I	0								
		DSS_FSYNC0	4		O									
		GPMC0_AD7	6		IO	0								
		GPIO0_27	7		IO	pad								
		EHRPWM_TZn_IN5	9		I	0								
		TRC_CTL	10		O									
		UART6_TXD	11		O									
F33	MCAN2_RX PADCONFIG PADCONFIG_30 0x0011C078	MCAN2_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK1	1		IO	0								
		VOUT0_PCLK	2		O									
		GPMC0_CSn1	6		O									
		GPIO0_30	7		IO	pad								
		SPI6_CS1	8		IO	1								
		EHRPWM4_B	9		IO	0								
		TRC_DATA17	10		O									
		UART3_TXD	11		O									
		GPMC0_DIR	12		O									
		I2C5_SDA	13		IOD	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
G28	MCAN2_TX PADCONFIG PADCONFIG_29 0x0011C074	MCAN2_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AXR3	1		IO	0								
		VOUT0_DATA0	2		O									
		VOUT0_DATA18	5		O									
		GPMC0_WAIT0	6		I	0								
		GPIO0_29	7		IO	pad								
		SPI6_D1	8		IO	0								
		EHRPWM1_B	9		IO	0								
		TRC_DATA3	10		O									
		UART3_RXD	11		I	1								
		GPMC0_DIR	12		O									
		I2C5_SCL	13		IOD	1								
T29	MCAN12_RX PADCONFIG PADCONFIG_2 0x0011C008	MCAN12_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		UART0_DCDn	1		I	1								
		DSS_FSYNC1	3		O									
		GPMC0_A23	6		OZ									
		GPIO0_2	7		IO	pad								
		TRC_CTL	10		O									
		UART5_RXD	11		I	1								
		GPMC0_CSn3	12		O									
P29	MCAN12_TX PADCONFIG PADCONFIG_1 0x0011C004	MCAN12_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		DSS_FSYNC0	3		O									
		GPMC0_A24	6		OZ									
		GPIO0_1	7		IO	pad								
		TRC_CLK	10		O									
		UART5_TXD	11		O									
		GPMC0_CLK	12		IO	0								
T32	MCAN13_RX PADCONFIG PADCONFIG_4 0x0011C010	MCAN13_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		UART0_DTRn	1		O									
		DSS_FSYNC3	3		O									
		GPMC0_A21	6		OZ									
		GPIO0_4	7		IO	pad								
		I2C4_SDA	8		IOD	1								
		TRC_DATA1	10		O									
		UART6_TXD	11		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
T31	MCAN13_TX PADCONFIG PADCONFIG_3 0x0011C00C	MCAN13_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		UART0_DSRn	1		I	1								
		DSS_FSYNC2	3		O									
		GPMC0_A22	6		OZ									
		GPIO0_3	7		IO	pad								
		TRC_DATA0	10		O									
		UART4_TXD	11		O									
		GPMC0_WAIT2	12		I	0								
R30	MCAN14_RX PADCONFIG PADCONFIG_6 0x0011C018	MCAN14_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA23	2		O									
		GPMC0_A19	6		OZ									
		GPIO0_6	7		IO	pad								
		I2C5_SDA	8		IOD	1								
		TRC_DATA3	10		O									
		UART9_TXD	11		O									
R33	MCAN14_TX PADCONFIG PADCONFIG_5 0x0011C014	MCAN14_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		UART0_RIn	1		I	1								
		GPMC0_A20	6		OZ									
		GPIO0_5	7		IO	pad								
		I2C4_SCL	8		IOD	1								
		TRC_DATA2	10		O									
		UART6_RXD	11		I	1								
		DP0_HPD	13		I	0								
R31	MCAN15_RX PADCONFIG PADCONFIG_8 0x0011C020	MCAN15_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA21	2		O									
		GPMC0_A17	6		OZ									
		GPIO0_8	7		IO	pad								
		SPI0_CS2	8		IO	1								
		TRC_DATA22	10		O									
		I2C1_SCL	12		IOD	1								
R29	MCAN15_TX PADCONFIG PADCONFIG_7 0x0011C01C	MCAN15_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA22	2		O									
		GPMC0_A18	6		OZ									
		GPIO0_7	7		IO	pad								
		I2C5_SCL	8		IOD	1								
		TRC_DATA21	10		O									
		UART9_RXD	11		I	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
U30	MCAN16_RX PADCONFIG PADCONFIG_10 0x0011C028	MCAN16_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA19	2		O									
		GPMC0_A15	6		OZ									
		GPIO0_10	7		IO	pad								
		SPI0_CS3	8		IO	1								
		TRC_DATA24	10		O									
		GPMC0_WAIT1	12		I	0								
G30	MCAN16_TX PADCONFIG PADCONFIG_9 0x0011C024	MCAN16_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		VOUT0_DATA20	2		O									
		GPMC0_A16	6		OZ									
		GPIO0_9	7		IO	pad								
		SPI1_CS3	8		IO	1								
		TRC_DATA23	10		O									
		I2C1_SDA	12		IOD	1								
J30	MCASP0_ACLKX PADCONFIG PADCONFIG_14 0x0011C038	MCAN5_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_ACLKX	1		IO	0								
		VOUT0_DATA15	2		O									
		GPMC0_AD0	6		IO	0								
		GPIO0_14	7		IO	pad								
		EHRPWM_TZn_IN2	9		I	0								
		UART8_RXD	11		I	1								
K31	MCASP0_AFSX PADCONFIG PADCONFIG_15 0x0011C03C	MCAN5_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AFSX	1		IO	0								
		VOUT0_DATA14	2		O									
		GPMC0_AD1	6		IO	0								
		GPIO0_15	7		IO	pad								
		EHRPWM2_B	9		IO	0								
		UART8_TXD	11		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
U32	MCASP1_ACLKX PADCONFIG PADCONFIG_46 0x0011C0B8	MCAN10_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_ACLKX	1		IO	0								
		DP0_HPD	3		I	0								
		PCIE0_CLKREQn	4		IO	0								
		GPMC0_A11	5		OZ									
		RGMII1_RD0	6		I	0								
		GPIO0_46	7		IO	pad								
		EQEP0_S	9		IO	0								
		UART4_RTSn	11		O									
		SPI3_CS3	12		IO	1								
		UART9_RTSn	13		O									
N32	MCASP1_AFSX PADCONFIG PADCONFIG_47 0x0011C0BC	MCAN11_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AFSX	1		IO	0								
		GPMC0_A12	5		OZ									
		MDIO0_MDIO	6		IO	0								
		GPIO0_47	7		IO	pad								
		SPI3_CS0	8		IO	1								
		EQEP0_I	9		IO	0								
		UART0_RXD	11		I	1								
P33	MCASP2_ACLKX PADCONFIG PADCONFIG_21 0x0011C054	MCAN8_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_ACLKX	1		IO	0								
		VOUT0_DATA8	2		O									
		VOUT0_DATA20	5		O									
		GPMC0_AD10	6		IO	0								
		GPIO0_21	7		IO	pad								
		SPI5_CS2	8		IO	1								
		EQEP2_S	9		IO	0								
		TRC_DATA4	10		O									
		UART1_RXD	11		I	1								
		SPI7_CS1	13		IO	1								
		SYNC3_OUT	14		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
G32	MCASP2_AFSX PADCONFIG PADCONFIG_22 0x0011C058	MCAN9_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AFSX	1		IO	0								
		VOUT0_DATA7	2		O									
		MDIO1_MDC	4		O									
		GPMC0_AD11	6		IO	0								
		GPIO0_22	7		IO	pad								
		SPI5_CS3	8		IO	1								
		EHRPWM_SOCA	9		O									
		TRC_DATA9	10		O									
		UART1_TXD	11		O									
		SPI7_CS2	13		IO	1								
F32	MCASP0_AXR0 PADCONFIG PADCONFIG_16 0x0011C040	MCAN6_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR0	1		IO	0								
		VOUT0_DATA13	2		O									
		GPMC0_AD2	6		IO	0								
		GPIO0_16	7		IO	pad								
		SPI2_CS2	8		IO	1								
		EHRPWM2_A	9		IO	0								
		TRC_DATA14	10		O									
		UART4_RXD	11		I	1								
		SPI7_CLK	13		IO	0								
		UART8_CTSn	14		I	1								
H32	MCASP0_AXR1 PADCONFIG PADCONFIG_17 0x0011C044	MCAN6_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR1	1		IO	0								
		VOUT0_DATA12	2		O									
		OBSCLK1	4		O									
		GPMC0_AD3	6		IO	0								
		GPIO0_17	7		IO	pad								
		SPI2_CS3	8		IO	1								
		EHRPWM0_SYNCO	9		O									
		TRC_DATA12	10		O									
		UART4_TXD	11		O									
		SPI7_CS0	13		IO	1								
		UART8_RTSn	14		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
H33	MCASP0_AXR2 PADCONFIG PADCONFIG_18 0x0011C048	MCAN7_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR2	1		IO	0								
		VOUT0_DATA11	2		O									
		GPMC0_ADVn_ALE	6		O									
		GPIO0_18	7		IO	pad								
		EQEP2_A	9		I	0								
		TRC_DATA10	10		O									
		UART4_CTSn	11		I	1								
		GPMC0_WPn	12		O									
		UART9_CTSn	13		I	1								
F31	MCASP0_AXR3 PADCONFIG PADCONFIG_31 0x0011C07C	MCAN3_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR3	1		IO	0								
		VOUT0_DATA2	2		O									
		GPMC0_BE1n	6		O									
		GPIO0_31	7		IO	pad								
		SPI5_CLK	8		IO	0								
		EHRPWM_TZn_IN0	9		I	0								
		TRC_DATA7	10		O									
		UART3_CTSn	11		I	1								
		SPI3_CS1	12		IO	1								
		SPI7_D1	13		IO	0								
J32	MCASP0_AXR4 PADCONFIG PADCONFIG_32 0x0011C080	MCAN3_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR4	1		IO	0								
		VOUT0_HSYNC	2		O									
		VOUT0_VP0_HSYNC	4		O									
		VOUT0_VP2_HSYNC	5		O									
		GPMC0_OEn_REn	6		O									
		GPIO0_32	7		IO	pad								
		SPI6_CS2	8		IO	1								
		EHRPWM5_B	9		IO	0								
		TRC_DATA18	10		O									
		I2C4_SDA	13		IOD	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
H30	MCASP0_AXR5 PADCONFIG PADCONFIG_33 0x0011C084	MCAN4_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR5	1		IO	0								
		VOUT0_DE	2		O									
		MCASP1_ACLKR	3		IO	0								
		VOUT0_VP0_DE	4		O									
		VOUT0_VP2_DE	5		O									
		GPMC0_CSn0	6		O									
		GPIO0_33	7		IO	pad								
		SPI6_CS3	8		IO	1								
		EHRPWM5_A	9		IO	0								
		TRC_DATA19	10		O									
		I2C4_SCL	13		IOD	1								
K33	MCASP0_AXR6 PADCONFIG PADCONFIG_34 0x0011C088	MCAN4_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR6	1		IO	0								
		VOUT0_VSYNC	2		O									
		MCASP1_AFSR	3		IO	0								
		VOUT0_VP0_VSYNC	4		O									
		VOUT0_VP2_VSYNC	5		O									
		GPMC0_CLKOUT	6		O									
		GPIO0_34	7		IO	pad								
		SPI3_CS2	8		IO	1								
		EHRPWM_TZn_IN4	9		I	0								
		TRC_DATA20	10		O									
		SPI5_D1	11		IO	0								
		GPMC0_FCLK_MUX	12		O									
M31	MCASP0_AXR7 PADCONFIG PADCONFIG_35 0x0011C08C	MCAN5_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR7	1		IO	0								
		MCASP4_ACLKR	3		IO	0								
		GPMC0_A0	5		OZ									
		RGMII1_TD0	6		O									
		GPIO0_35	7		IO	pad								
		GPMC0_A14	8		OZ									
		EHRPWM3_A	9		IO	0								
		UART4_RXD	11		I	1								
		GPMC0_CSn2	12		O									
		USB0_DRVVBUS	14		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
N30	MCASP0_AXR8 PADCONFIG PADCONFIG_36 0x0011C090	MCAN5_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR8	1		IO	0								
		MCASP4_AFSR	3		IO	0								
		GPMC0_A1	5		OZ									
		RGMII1_TD1	6		O									
		GPIO0_36	7		IO	pad								
		RMII1_RXD0	8		I	0								
		EHRPWM_TZn_IN3	9		I	0								
		UART4_TXD	11		O									
T33	MCASP0_AXR9 PADCONFIG PADCONFIG_37 0x0011C094	MCAN6_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR9	1		IO	0								
		MCASP4_AXR4	2		IO	0								
		GPMC0_A2	5		OZ									
		RGMII1_TD2	6		O									
		GPIO0_37	7		IO	pad								
		RMII1_RXD1	8		I	0								
		EHRPWM3_SYNCO	9		O									
		UART4_CTSn	11		I	1								
L32	MCASP0_AXR10 PADCONFIG PADCONFIG_38 0x0011C098	MCAN6_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR10	1		IO	0								
		GPMC0_A3	5		OZ									
		RGMII1_TD3	6		O									
		GPIO0_38	7		IO	pad								
		RMII1_CRS_DV	8		I	0								
		EHRPWM3_SYNCI	9		I	0								
		UART4_RTSn	11		O									
P30	MCASP0_AXR11 PADCONFIG PADCONFIG_39 0x0011C09C	MCAN7_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR11	1		IO	0								
		DSS_FSYNC2	4		O									
		GPMC0_A4	5		OZ									
		RGMII1_TX_CTL	6		O									
		GPIO0_39	7		IO	pad								
		RMII1_RX_ER	8		I	0								
		EHRPWM3_B	9		IO	0								
		SPI2_CS1	10		IO	1								
		UART5_RXD	11		I	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
M32	MCASP0_AXR12 PADCONFIG PADCONFIG_40 0x0011C0A0	MCAN7_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR12	1		IO	0								
		MCASP2_ACLKR	3		IO	0								
		DSS_FSYNC3	4		O									
		GPMC0_A5	5		OZ									
		RGMII1_RD1	6		I	0								
		GPIO0_40	7		IO	pad								
		RMII1_TXD0	8		O									
		EHRPWM_SOCB	9		O									
		SPI2_CLK	10		IO	0								
		UART5_TXD	11		O									
L33	MCASP0_AXR13 PADCONFIG PADCONFIG_41 0x0011C0A4	MCAN8_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR13	1		IO	0								
		MCASP2_AFSR	3		IO	0								
		GPMC0_A6	5		OZ									
		RGMII1_RD2	6		I	0								
		GPIO0_41	7		IO	pad								
		RMII_REF_CLK	8		I	0								
		EHRPWM4_A	9		IO	0								
		SPI2_CS0	10		IO	1								
		UART5_CTSn	11		I	1								
		UART7_RXD	13		I	1								
U31	MCASP0_AXR14 PADCONFIG PADCONFIG_42 0x0011C0A8	MCAN8_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR14	1		IO	0								
		MCASP2_AXR4	2		IO	0								
		MCASP0_ACLKR	3		IO	0								
		GPMC0_A7	5		OZ									
		RGMII1_RD3	6		I	0								
		GPIO0_42	7		IO	pad								
		CLKOUT	8		IO	0								
		EQEP0_A	9		I	0								
		SPI2_D0	10		IO	0								
		UART5_RTSn	11		O									
		UART7_TXD	13		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
M33	MCASP0_AXR15 PADCONFIG PADCONFIG_43 0x0011C0AC	MCAN9_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP0_AXR15	1		IO	0								
		MCASP0_AFSR	3		IO	0								
		GPMC0_A8	5		OZ									
		RGMII1_RX_CTL	6		I	0								
		GPIO0_43	7		IO	pad								
		RMII1_TX_EN	8		O									
		EQEP0_B	9		I	0								
		SPI2_D1	10		IO	0								
		UART8_RXD	11		I	1								
		I2C1_SCL	13		IOD	1								
H29	MCASP1_AXR0 PADCONFIG PADCONFIG_48 0x0011C0C0	MCAN11_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AXR0	1		IO	0								
		GPMC0_A13	5		OZ									
		MDIO0_MDC	6		O									
		GPIO0_48	7		IO	pad								
		SPI3_CLK	8		IO	0								
		EQEP1_S	9		IO	0								
		UART0_TXD	11		O									
		GPMC0_WAIT3	12		I	0								
		SYNC2_OUT	14		O									
G31	MCASP1_AXR1 PADCONFIG PADCONFIG_19 0x0011C04C	MCAN7_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AXR1	1		IO	0								
		VOUT0_DATA10	2		O									
		GPMC0_AD8	6		IO	0								
		GPIO0_19	7		IO	pad								
		SPI3_D0	8		IO	0								
		EHRPWM_TZn_IN1	9		I	0								
		TRC_DATA8	10		O									
		UART0_CTSn	11		I	1								
		UART9_RXD	12		I	1								
		I2C2_SCL	13		IOD	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
J31	MCASP1_AXR2 PADCONFIG PADCONFIG_20 0x0011C050	MCAN8_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AXR2	1		IO	0								
		VOUT0_DATA9	2		O									
		VOUT0_DATA21	5		O									
		GPMC0_AD9	6		IO	0								
		GPIO0_20	7		IO	pad								
		SPI3_D1	8		IO	0								
		EQEP2_B	9		I	0								
		TRC_DATA6	10		O									
		UART0_RTSn	11		O									
		UART9_TXD	12		O									
		I2C2_SDA	13		IOD	1								
P31	MCASP1_AXR3 PADCONFIG PADCONFIG_44 0x0011C0B0	MCAN9_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AXR3	1		IO	0								
		PCIE2_CLKREQn	4	No	IO	0								
		GPMC0_A9	5		OZ									
		RGMII1_RXC	6		I	0								
		GPIO0_44	7		IO	pad								
		RMII1_TXD1	8		O									
		EQEP1_A	9		I	0								
		UART8_TXD	11		O									
		I2C1_SDA	13		IOD	1								
N31	MCASP1_AXR4 PADCONFIG PADCONFIG_45 0x0011C0B4	MCAN10_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP1_AXR4	1		IO	0								
		PCIE3_CLKREQn	4	No	IO	0								
		GPMC0_A10	5		OZ									
		RGMII1_TXC	6		O									
		GPIO0_45	7		IO	pad								
		EQEP1_B	9		I	0								
		UART4_RXD	11		I	1								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
K32	MCASP2_AXR0 PADCONFIG PADCONFIG_23 0x0011C05C	MCAN9_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AXR0	1		IO	0								
		VOUT0_DATA6	2		O									
		MDIO1_MDIO	4		IO	0								
		GPMC0_AD12	6		IO	0								
		GPIO0_23	7		IO	pad								
		EQEP2_I	9		IO	0								
		TRC_DATA15	10		O									
		UART1_CTSn	11		I	1								
		UART6_RXD	12		I	1								
R32	MCASP2_AXR1 PADCONFIG PADCONFIG_24 0x0011C060	MCAN17_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AXR1	1		IO	0								
		VOUT0_DATA5	2		O									
		GPMC0_AD13	6		IO	0								
		GPIO0_24	7		IO	pad								
		EHRPWM1_A	9		IO	0								
		TRC_DATA13	10		O									
		UART1_RTSn	11		O									
		UART6_TXD	12		O									
		I2C3_SDA	13		IOD	1								
C26	MCU_ADC0_REFN	MCU_ADC0_REFN			A					1.8 V	VDDA_ADC0		ADC12B	
D25	MCU_ADC0_REFP	MCU_ADC0_REFP			A					1.8 V	VDDA_ADC0		ADC12B	
D29	MCU_ADC1_REFN	MCU_ADC1_REFN			A					1.8 V	VDDA_ADC1		ADC12B	
C30	MCU_ADC1_REFP	MCU_ADC1_REFP			A					1.8 V	VDDA_ADC1		ADC12B	
E26	MCU_ADC0_AIN0 PADCONFIG WKUP_PADCONFIG_77 0x4301C134	MCU_ADC0_AIN0	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
		WKUP_GPIO0_71	7 (1)		I	pad								
F25	MCU_ADC0_AIN1 PADCONFIG WKUP_PADCONFIG_78 0x4301C138	MCU_ADC0_AIN1	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
		WKUP_GPIO0_72	7 (1)		I	pad								
F23	MCU_ADC0_AIN2 PADCONFIG WKUP_PADCONFIG_79 0x4301C13C	MCU_ADC0_AIN2	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
		WKUP_GPIO0_73	7 (1)		I	pad								
A28	MCU_ADC0_AIN3 PADCONFIG WKUP_PADCONFIG_80 0x4301C140	MCU_ADC0_AIN3	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
		WKUP_GPIO0_74	7 (1)		I	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
E24	MCU_ADC0_AIN4	MCU_ADC0_AIN4	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
	PADCONFIG WKUP_PADCONFIG_81 0x4301C144	WKUP_GPIO0_75	7 (1)		I	pad								
D27	MCU_ADC0_AIN5	MCU_ADC0_AIN5	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
	PADCONFIG WKUP_PADCONFIG_82 0x4301C148	WKUP_GPIO0_76	7 (1)		I	pad								
A26	MCU_ADC0_AIN6	MCU_ADC0_AIN6	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
	PADCONFIG WKUP_PADCONFIG_83 0x4301C14C	WKUP_GPIO0_77	7 (1)		I	pad								
B27	MCU_ADC0_AIN7	MCU_ADC0_AIN7	0		A				0	1.8 V	VDDA_ADC0		ADC12B	
	PADCONFIG WKUP_PADCONFIG_84 0x4301C150	WKUP_GPIO0_78	7 (1)		I	pad								
C32	MCU_ADC1_AIN0	MCU_ADC1_AIN0	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_85 0x4301C154	WKUP_GPIO0_79	7 (1)		I	pad								
B33	MCU_ADC1_AIN1	MCU_ADC1_AIN1	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_86 0x4301C158	WKUP_GPIO0_80	7 (1)		I	pad								
B31	MCU_ADC1_AIN2	MCU_ADC1_AIN2	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_87 0x4301C15C	WKUP_GPIO0_81	7 (1)		I	pad								
B29	MCU_ADC1_AIN3	MCU_ADC1_AIN3	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_88 0x4301C160	WKUP_GPIO0_82	7 (1)		I	pad								
D31	MCU_ADC1_AIN4	MCU_ADC1_AIN4	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_89 0x4301C164	WKUP_GPIO0_83	7 (1)		I	pad								
A32	MCU_ADC1_AIN5	MCU_ADC1_AIN5	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_90 0x4301C168	WKUP_GPIO0_84	7 (1)		I	pad								
A30	MCU_ADC1_AIN6	MCU_ADC1_AIN6	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_91 0x4301C16C	WKUP_GPIO0_85	7 (1)		I	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
C28	MCU_ADC1_AIN7	MCU_ADC1_AIN7	0		A				0	1.8 V	VDDA_ADC1		ADC12B	
	PADCONFIG WKUP_PADCONFIG_92 0x4301C170	WKUP_GPIO0_86	7 (1)		I	pad								
D22	MCU_I2C0_SCL	MCU_I2C0_SCL	0		IOD	1	Off / Off / NA	On / SS / NA	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OPEN DRAIN	
	PADCONFIG WKUP_PADCONFIG_66 0x4301C108	WKUP_GPIO0_65	7		IO	pad								
A21	MCU_I2C0_SDA	MCU_I2C0_SDA	0		IOD	1	Off / Off / NA	On / SS / NA	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OPEN DRAIN	
	PADCONFIG WKUP_PADCONFIG_67 0x4301C10C	WKUP_GPIO0_87	7		IO	pad								
C18	MCU_MCAN0_RX	MCU_MCAN0_RX	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_47 0x4301C0BC	WKUP_GPIO0_61	7		IO	pad								
E22	MCU_MCAN0_TX	MCU_MCAN0_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_46 0x4301C0B8	WKUP_GPIO0_60	7		IO	pad								
E12	MCU_MDIO0_MDC	MCU_MDIO0_MDC	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_39 0x4301C09C	WKUP_GPIO0_53	7		IO	pad								
F13	MCU_MDIO0_MDIO	MCU_MDIO0_MDIO	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_38 0x4301C098	WKUP_GPIO0_52	7		IO	pad								
D8	MCU_OSPI0_CLK	MCU_OSPI0_CLK	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_0 0x4301C000	MCU_HYPERBUS0_CK	1		O									
		WKUP_GPIO0_16	7		IO	pad								
C10	MCU_OSPI0_DQS	MCU_OSPI0_DQS	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_2 0x4301C008	MCU_HYPERBUS0_RWDS	1		IO	0								
		WKUP_GPIO0_18	7		IO	pad								
D10	MCU_OSPI0_LBCLKO	MCU_OSPI0_LBCLKO	0		IO	0	Off / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_1 0x4301C004	MCU_HYPERBUS0_CKn	1		O									
		WKUP_GPIO0_17	7		IO	pad								
B7	MCU_OSPI1_CLK	MCU_OSPI1_CLK	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_16 0x4301C040	WKUP_GPIO0_31	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
B9	MCU_OSPI1_DQS PADCONFIG WKUP_PADCONFIG_18 0x4301C048	MCU_OSPI1_DQS	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_OSPI0_CSn3	1		O									
		MCU_HYPERBUS0_INTn	2		I	1								
		MCU_OSPI0_ECC_FAIL	6		I	1								
		WKUP_GPIO0_33	7		IO	pad								
B10	MCU_OSPI1_LBCLKO PADCONFIG WKUP_PADCONFIG_17 0x4301C044	MCU_OSPI1_LBCLKO	0		IO	0	Off / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_OSPI0_CSn2	1		O									
		MCU_HYPERBUS0_RESETOn	2		I	1								
		MCU_OSPI0_RESET_OUT0	6		O									
		WKUP_GPIO0_32	7		IO	pad								
F12	MCU_OSPI0_CSn0 PADCONFIG WKUP_PADCONFIG_11 0x4301C02C	MCU_OSPI0_CSn0	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_CSn0	1		O									
		WKUP_GPIO0_27	7		IO	pad								
F11	MCU_OSPI0_CSn1 PADCONFIG WKUP_PADCONFIG_12 0x4301C030	MCU_OSPI0_CSn1	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_RESETn	1		O									
		WKUP_GPIO0_28	7		IO	pad								
F10	MCU_OSPI0_CSn2 PADCONFIG WKUP_PADCONFIG_14 0x4301C038	MCU_OSPI0_CSn2	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_OSPI0_CSn2	1		O									
		MCU_HYPERBUS0_RESETOn	2		I	1								
		MCU_HYPERBUS0_WPn	3		O									
		MCU_HYPERBUS0_CSn1	4		O									
		MCU_OSPI0_RESET_OUT0	6		O									
		WKUP_GPIO0_29	7		IO	pad								
E11	MCU_OSPI0_CSn3 PADCONFIG WKUP_PADCONFIG_15 0x4301C03C	MCU_OSPI0_CSn3	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_OSPI0_CSn3	1		O									
		MCU_HYPERBUS0_INTn	2		I	1								
		MCU_HYPERBUS0_WPn	3		O									
		MCU_OSPI0_RESET_OUT1	5		O									
		MCU_OSPI0_ECC_FAIL	6		I	1								
		WKUP_GPIO0_30	7		IO	pad								
E10	MCU_OSPI0_D0 PADCONFIG WKUP_PADCONFIG_3 0x4301C00C	MCU_OSPI0_D0	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ0	1		IO	0								
		WKUP_GPIO0_19	7		IO	pad								
		BOOTMODE00	Bootstrap		I									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
F9	MCU_OSPI0_D1 PADCONFIG WKUP_PADCONFIG_4 0x4301C010	MCU_OSPI0_D1	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ1	1		IO	0								
		WKUP_GPIO0_20	7		IO	pad								
		BOOTMODE01	Bootstrap		I									
E9	MCU_OSPI0_D2 PADCONFIG WKUP_PADCONFIG_5 0x4301C014	MCU_OSPI0_D2	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ2	1		IO	0								
		WKUP_GPIO0_21	7		IO	pad								
D11	MCU_OSPI0_D3 PADCONFIG WKUP_PADCONFIG_6 0x4301C018	MCU_OSPI0_D3	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ3	1		IO	0								
		WKUP_GPIO0_22	7		IO	pad								
D9	MCU_OSPI0_D4 PADCONFIG WKUP_PADCONFIG_7 0x4301C01C	MCU_OSPI0_D4	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ4	1		IO	0								
		WKUP_GPIO0_23	7		IO	pad								
		BOOTMODE02	Bootstrap		I									
C9	MCU_OSPI0_D5 PADCONFIG WKUP_PADCONFIG_8 0x4301C020	MCU_OSPI0_D5	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ5	1		IO	0								
		WKUP_GPIO0_24	7		IO	pad								
		BOOTMODE03	Bootstrap		I									
C7	MCU_OSPI0_D6 PADCONFIG WKUP_PADCONFIG_9 0x4301C024	MCU_OSPI0_D6	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ6	1		IO	0								
		WKUP_GPIO0_25	7		IO	pad								
C8	MCU_OSPI0_D7 PADCONFIG WKUP_PADCONFIG_10 0x4301C028	MCU_OSPI0_D7	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_DQ7	1		IO	0								
		WKUP_GPIO0_26	7		IO	pad								
A8	MCU_OSPI1_CSn0 PADCONFIG WKUP_PADCONFIG_23 0x4301C05C	MCU_OSPI1_CSn0	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_38	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
A9	MCU_OSPI1_CSn1 PADCONFIG WKUP_PADCONFIG_24 0x4301C060	MCU_OSPI1_CSn1	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_HYPERBUS0_WPn	1		O									
		MCU_TIMER_IO0	2		IO	0								
		MCU_HYPERBUS0_CSn1	3		O									
		MCU_UART0_RTSn	4		O									
		MCU_SPI0_CS2	5		IO	1								
		MCU_OSPI0_RESET_OUT1	6		O									
		WKUP_GPIO0_39	7		IO	pad								
B8	MCU_OSPI1_D0 PADCONFIG WKUP_PADCONFIG_19 0x4301C04C	MCU_OSPI1_D0	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_34	7		IO	pad								
B11	MCU_OSPI1_D1 PADCONFIG WKUP_PADCONFIG_20 0x4301C050	MCU_OSPI1_D1	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_UART0_RXD	4		I	1								
		MCU_SPI1_CS1	5		IO	1								
		WKUP_GPIO0_35	7		IO	pad								
A11	MCU_OSPI1_D2 PADCONFIG WKUP_PADCONFIG_21 0x4301C054	MCU_OSPI1_D2	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_UART0_TXD	4		O									
		MCU_SPI1_CS2	5		IO	1								
		WKUP_GPIO0_36	7		IO	pad								
A10	MCU_OSPI1_D3 PADCONFIG WKUP_PADCONFIG_22 0x4301C058	MCU_OSPI1_D3	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD
		MCU_UART0_CTSn	4		I	1								
		MCU_SPI0_CS1	5		IO	1								
		WKUP_GPIO0_37	7		IO	pad								
C24	MCU_PORz	MCU_PORz			I					1.8 V	VDDA_WKUP	Yes	FS_RESET	
E21	MCU_RESETSTATz PADCONFIG WKUP_PADCONFIG_71 0x4301C11C	MCU_RESETSTATz	0		O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_68	7		IO	pad								
E20	MCU_RESETz PADCONFIG WKUP_PADCONFIG_70 0x4301C118	MCU_RESETz	0		I		On / NA / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
C14	MCU_RGMII1_RXC PADCONFIG WKUP_PADCONFIG_33 0x4301C084	MCU_RGMII1_RXC	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_REF_CLK	1		I	0								
		WKUP_GPIO0_47	7		IO	pad								
C12	MCU_RGMII1_RX_CTL PADCONFIG WKUP_PADCONFIG_27 0x4301C06C	MCU_RGMII1_RX_CTL	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_RX_ER	1		I	0								
		WKUP_GPIO0_41	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
A14	MCU_RGMII1_TXC PADCONFIG WKUP_PADCONFIG_32 0x4301C080	MCU_RGMII1_TXC	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_TX_EN	1		O									
		WKUP_GPIO0_46	7		IO	pad								
B14	MCU_RGMII1_TX_CTL PADCONFIG WKUP_PADCONFIG_26 0x4301C068	MCU_RGMII1_TX_CTL	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_CRS_DV	1		I	0								
		WKUP_GPIO0_40	7		IO	pad								
E13	MCU_RGMII1_RD0 PADCONFIG WKUP_PADCONFIG_37 0x4301C094	MCU_RGMII1_RD0	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_RXD0	1		I	0								
		WKUP_GPIO0_51	7		IO	pad								
D14	MCU_RGMII1_RD1 PADCONFIG WKUP_PADCONFIG_36 0x4301C090	MCU_RGMII1_RD1	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_RXD1	1		I	0								
		WKUP_GPIO0_50	7		IO	pad								
D12	MCU_RGMII1_RD2 PADCONFIG WKUP_PADCONFIG_35 0x4301C08C	MCU_RGMII1_RD2	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO5	1		IO	0								
		WKUP_GPIO0_62	7		IO	pad								
D13	MCU_RGMII1_RD3 PADCONFIG WKUP_PADCONFIG_34 0x4301C088	MCU_RGMII1_RD3	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO4	1		IO	0								
		WKUP_GPIO0_48	7		IO	pad								
B13	MCU_RGMII1_TD0 PADCONFIG WKUP_PADCONFIG_31 0x4301C07C	MCU_RGMII1_TD0	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_TXD0	1		O									
		WKUP_GPIO0_45	7		IO	pad								
A13	MCU_RGMII1_TD1 PADCONFIG WKUP_PADCONFIG_30 0x4301C078	MCU_RGMII1_TD1	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_RMII1_TXD1	1		O									
		WKUP_GPIO0_44	7		IO	pad								
B12	MCU_RGMII1_TD2 PADCONFIG WKUP_PADCONFIG_29 0x4301C074	MCU_RGMII1_TD2	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO3	1		IO	0								
		MCU_ADC_EXT_TRIGGER1	3		I	0								
		WKUP_GPIO0_43	7		IO	pad								
A12	MCU_RGMII1_TD3 PADCONFIG WKUP_PADCONFIG_28 0x4301C070	MCU_RGMII1_TD3	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO2	1		IO	0								
		MCU_ADC_EXT_TRIGGER0	3		I	0								
		WKUP_GPIO0_42	7		IO	pad								
C22	MCU_SAFETY_ERRORn PADCONFIG WKUP_PADCONFIG_69 0x4301C114	MCU_SAFETY_ERRORn	0		IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDA_WKUP	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
F15	MCU_SPI0_CLK PADCONFIG WKUP_PADCONFIG_40 0x4301C0A0	MCU_SPI0_CLK	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_54	7		IO	pad								
		MCU_BOOTMODE00	Bootstrap		I									
E19	MCU_SPI0_CS0 PADCONFIG WKUP_PADCONFIG_43 0x4301C0AC	MCU_SPI0_CS0	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO1	4		IO	0								
		WKUP_GPIO0_70	7		IO	pad								
E18	MCU_SPI0_D0 PADCONFIG WKUP_PADCONFIG_41 0x4301C0A4	MCU_SPI0_D0	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_55	7		IO	pad								
		MCU_BOOTMODE01	Bootstrap		I									
E14	MCU_SPI0_D1 PADCONFIG WKUP_PADCONFIG_42 0x4301C0A8	MCU_SPI0_D1	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	4		IO	0								
		WKUP_GPIO0_69	7		IO	pad								
		MCU_BOOTMODE02	Bootstrap		I									
AH2	MMC0_CALPAD	MMC0_CALPAD			A					1.8 V	VDDS_MMC0		eMMCPHY	
AJ2	MMC0_CLK	MMC0_CLK			O		On / Low / Off	On / SS / Off		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AL2	MMC0_CMD	MMC0_CMD			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AJ1	MMC0_DS	MMC0_DS			IO	1	On / Off / Down	On / Off / Down		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
D33	MMC1_CLK PADCONFIG PADCONFIG_65 0x0011C104	MMC1_CLK	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART8_RXD	1		I	1								
		TIMER_IO6	3		IO	0								
		EHRPWM2_B	4		IO	0								
		UART4_CTSn	5		I	1								
		EHRPWM5_A	6		IO	0								
		GPIO0_64	7		IO	pad								
		SPI1_CLK	8		IO	0								
		UART0_RTSn	9		O									
		I2C6_SDA	10		IOD	1								
		MCAN15_TX	11		O									
		PCIE2_CLKREQn	12	No	IO	0								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
E32	MMC1_CMD PADCONFIG PADCONFIG_66 0x0011C108	MMC1_CMD	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART8_TXD	1		O									
		TIMER_IO7	3		IO	0								
		EHRPWM2_A	4		IO	0								
		UART4_RTSn	5		O									
		GPIO0_65	7		IO	pad								
		SPI1_D1	8		IO	0								
		I2C6_SCL	10		IOD	1								
		MCAN15_RX	11		I	1								
		PCIE3_CLKREQn	12	No	IO	0								
AM1	MMC0_DAT0	MMC0_DAT0			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AK3	MMC0_DAT1	MMC0_DAT1			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AL1	MMC0_DAT2	MMC0_DAT2			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AK1	MMC0_DAT3	MMC0_DAT3			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AJ3	MMC0_DAT4	MMC0_DAT4			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AH3	MMC0_DAT5	MMC0_DAT5			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AJ4	MMC0_DAT6	MMC0_DAT6			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
AK2	MMC0_DAT7	MMC0_DAT7			IO	1	On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD
F28	MMC1_DAT0 PADCONFIG PADCONFIG_63 0x0011C0FC	MMC1_DAT0	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART7_RTSn	1		O									
		ECAP1_IN_APWM_OUT	2		IO	0								
		TIMER_IO5	3		IO	0								
		EHRPWM1_A	4		IO	0								
		UART4_TXD	5		O									
		GPIO0_63	7		IO	pad								
		SPI1_D0	8		IO	0								
		UART5_RTSn	9		O									
		I2C4_SCL	10		IOD	1								
		UART2_TXD	11		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
F29	MMC1_DAT1 PADCONFIG PADCONFIG_62 0x0011C0F8	MMC1_DAT1	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART7_CTSn	1		I	1								
		ECAP0_IN_APWM_OUT	2		IO	0								
		TIMER_IO4	3		IO	0								
		EHRPWM1_B	4		IO	0								
		UART4_RXD	5		I	1								
		EHRPWM4_A	6		IO	0								
		GPIO0_62	7		IO	pad								
		SPI1_CS2	8		IO	1								
		UART5_CTSn	9		I	1								
		I2C4_SDA	10		IOD	1								
		UART2_RXD	11		I	1								
E30	MMC1_DAT2 PADCONFIG PADCONFIG_61 0x0011C0F4	MMC1_DAT2	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART7_TXD	1		O									
		TIMER_IO3	3		IO	0								
		EHRPWM0_A	4		IO	0								
		GPIO0_61	7		IO	pad								
		SPI1_CS1	8		IO	1								
		CPTS0_TS_SYNC	9		O									
		I2C3_SDA	10		IOD	1								
		UART5_TXD	11		O									
F30	MMC1_DAT3 PADCONFIG PADCONFIG_60 0x0011C0F0	MMC1_DAT3	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART7_RXD	1		I	1								
		PCIE1_CLKREQn	2		IO	0								
		TIMER_IO2	3		IO	0								
		EHRPWM0_B	4		IO	0								
		EHRPWM3_A	6		IO	0								
		GPIO0_60	7		IO	pad								
		SPI1_CS0	8		IO	1								
		UART0_CTSn	9		I	1								
		I2C3_SCL	10		IOD	1								
		UART5_RXD	11		I	1								
B23	OSC1_XI	OSC1_XI			I					1.8 V	VDDA_OSC1	Yes	HFXOSC	
A22	OSC1_XO	OSC1_XO			O					1.8 V	VDDA_OSC1	Yes	HFXOSC	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AJ13	PCIE_REFCLK0_N_OUT	PCIE_REFCLK0_N_OUT			O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AJ12	PCIE_REFCLK0_P_OUT	PCIE_REFCLK0_P_OUT			O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AH14	PCIE_REFCLK1_N_OUT	PCIE_REFCLK1_N_OUT			O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AH13	PCIE_REFCLK1_P_OUT	PCIE_REFCLK1_P_OUT			O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AH11	PCIE_REFCLK2_N_OUT	PCIE_REFCLK2_N_OUT		No	O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AH10	PCIE_REFCLK2_P_OUT	PCIE_REFCLK2_P_OUT		No	O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AJ16	PCIE_REFCLK3_N_OUT	PCIE_REFCLK3_N_OUT		No	O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AJ15	PCIE_REFCLK3_P_OUT	PCIE_REFCLK3_P_OUT		No	O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
B16	PMIC_POWER_EN1	PMIC_POWER_EN1	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_68 0x4301C110	MCU_I3C0_SDAPULLEN	5		OD									
		WKUP_GPIO0_88	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
T30	PMIC_WAKE0 PADCONFIG PADCONFIG_13 0x0011C034	PMIC_WAKE0	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP4_AXR0	1		IO	0								
		DSS_FSYNC1	4		O									
		MCAN17_RX	5		I	1								
		GPMC0_WEn	6		O									
		GPIO0_13	7		IO	pad								
		SPI6_CS0	8		IO	1								
		TRC_DATA0	10		O									
		UART9_RTSn	11		O									
		UART7_TXD	13		O									
		AUDIO_EXT_REFCLK0	14		IO	0								
D24	PORz PADCONFIG WKUP_PADCONFIG_94 0x4301C178	PORz	0		I				0	1.8 V	VDDA_WKUP	Yes	FS_RESET	
W32	RESETSTATz PADCONFIG PADCONFIG_67 0x0011C10C	RESETSTATz	0		O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
G20	RESET_REQz PADCONFIG WKUP_PADCONFIG_93 0x4301C174	RESET_REQz	0		I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
AK15	SERDES0_REFCLK_N	SERDES0_REFCLK_N		No	IO					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AK14	SERDES0_REFCLK_P	SERDES0_REFCLK_P		No	IO					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AG7	SERDES0_REXT	SERDES0_REXT		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AN5	SERDES1_REFCLK_N	SERDES1_REFCLK_N			IO					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AN6	SERDES1_REFCLK_P	SERDES1_REFCLK_P			IO					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AH9	SERDES1_REXT	SERDES1_REXT			I					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AK21	SERDES4_REFCLK_N	SERDES4_REFCLK_N			IO					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AK20	SERDES4_REFCLK_P	SERDES4_REFCLK_P			IO					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AH23	SERDES4_REXT	SERDES4_REXT			IO					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AM12	SERDES0_RX0_N	PCIE1_RXN0		No	I					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AM13	SERDES0_RX0_P	PCIE1_RXP0		No	I					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AL13	SERDES0_RX1_N	PCIE1_RXN1		No	I					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
AL14	SERDES0_RX1_P	PCIE1_RXP1		No	I					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AN15	SERDES0_RX2_N	USB0_SSRX1N		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE1_RXN2		No	I									
		PCIE3_RXN0		No	I									
AN14	SERDES0_RX2_P	USB0_SSRX1P		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE1_RXP2		No	I									
		PCIE3_RXP0		No	I									
AL17	SERDES0_RX3_N	USB0_SSRX2N		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE3_RXN1		No	I									
		PCIE1_RXN3		No	I									
AL16	SERDES0_RX3_P	USB0_SSRX2P		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE3_RXP1		No	I									
		PCIE1_RXP3		No	I									
AN11	SERDES0_TX0_N	PCIE1_TXN0		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AN12	SERDES0_TX0_P	PCIE1_TXP0		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AJ19	SERDES0_TX1_N	PCIE1_TXN1		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AJ18	SERDES0_TX1_P	PCIE1_TXP1		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
AM16	SERDES0_TX2_N	PCIE1_TXN2		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		USB0_SSTX1N		No	O									
		PCIE3_TXN0		No	O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AM15	SERDES0_TX2_P	USB0_SSTX1P		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE3_TXP0		No	O									
		PCIE1_TXP2		No	O									
AK18	SERDES0_TX3_N	PCIE3_TXN1		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		USB0_SSTX2N		No	O									
		PCIE1_TXN3		No	O									
AK17	SERDES0_TX3_P	USB0_SSTX2P		No	O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE1_TXP3		No	O									
		PCIE3_TXP1		No	O									
AL10	SERDES1_RX0_N	SGMII3_RXN0			I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXN0			I									
AL11	SERDES1_RX0_P	SGMII3_RXP0			I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXP0			I									
AN8	SERDES1_RX1_N	SGMII4_RXN0			I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXN1			I									
AN9	SERDES1_RX1_P	SGMII4_RXP0			I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXP1			I									
AM6	SERDES1_RX2_N	PCIE2_RXN0		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXN2			I									
		SGMII1_RXN0			I									
AM7	SERDES1_RX2_P	PCIE2_RXP0		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_RXP2			I									
		SGMII1_RXP0			I									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AL7	SERDES1_RX3_N	PCIE2_RXN1		No	I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		SGMII2_RXN0			I									
		PCIE0_RXN3			I									
AL8	SERDES1_RX3_P	SGMII2_RXP0			I					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE2_RXP1		No	I									
		PCIE0_RXP3			I									
AK11	SERDES1_TX0_N	PCIE0_TXN0			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		SGMII3_TXN0			O									
AK12	SERDES1_TX0_P	PCIE0_TXP0			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		SGMII3_TXP0			O									
AM9	SERDES1_TX1_N	PCIE0_TXN1			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		SGMII4_TXN0			O									
AM10	SERDES1_TX1_P	SGMII4_TXP0			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE0_TXP1			O									
AK8	SERDES1_TX2_N	PCIE0_TXN2			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE2_TXN0		No	O									
		SGMII1_TXN0			O									
AK9	SERDES1_TX2_P	PCIE0_TXP2			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE2_TXP0		No	O									
		SGMII1_TXP0			O									
AJ9	SERDES1_TX3_N	SGMII2_TXN0			O					1.8 V	VDDA_0P8_SERDES0_1 / VDDA_0P8_SERDES_C0_1 / VDDA_1P8_SERDES0_1		4L_PHY	
		PCIE2_TXN1		No	O									
		PCIE0_TXN3			O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AJ10	SERDES1_TX3_P	SGMII2_TXP0			O					1.8 V	VDDA_0P8_SERDES 0_1 / VDDA_0P8_SERDES _C0_1 / VDDA_1P8_SERDES 0_1		4L_PHY	
		PCIE0_TXP3			O									
		PCIE2_TXP1		No	O									
AN17	SERDES4_RX0_N	SGMII5_RXN0		No	I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AN18	SERDES4_RX0_P	SGMII5_RXP0		No	I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AL19	SERDES4_RX1_N	SGMII6_RXN0		No	I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AL20	SERDES4_RX1_P	SGMII6_RXP0		No	I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
AK23	SERDES4_RX2_N	USB0_SSRX1N			I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
		SGMII7_RXN0		No	I									
AK24	SERDES4_RX2_P	USB0_SSRX1P			I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
		SGMII7_RXP0		No	I									
AM21	SERDES4_RX3_N	USB0_SSRX2N			I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
		SGMII8_RXN0		No	I									
AM22	SERDES4_RX3_P	SGMII8_RXP0		No	I					1.8 V	VDDA_0P8_SERDES 4 / VDDA_0P8_SERDES _C4 / VDDA_1P8_SERDES 4		4L_PHY	
		USB0_SSRX2P			I									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AJ21	SERDES4_TX0_N	SGMII5_TXN0		No	O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		DP0_TXN0			O									
AJ22	SERDES4_TX0_P	SGMII5_TXP0		No	O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		DP0_TXP0			O									
AM18	SERDES4_TX1_N	SGMII6_TXN0		No	O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		DP0_TXN1			O									
AM19	SERDES4_TX1_P	DP0_TXP1			O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		SGMII6_TXP0		No	O									
AN20	SERDES4_TX2_N	DP0_TXN2			O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		SGMII7_TXN0		No	O									
		USB0_SSTX1N			O									
AN21	SERDES4_TX2_P	SGMII7_TXP0		No	O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		USB0_SSTX1P			O									
		DP0_TXP2			O									
AL22	SERDES4_TX3_N	SGMII8_TXN0		No	O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		USB0_SSTX2N			O									
		DP0_TXN3			O									
AL23	SERDES4_TX3_P	USB0_SSTX2P			O					1.8 V	VDDA_0P8_SERDES4 / VDDA_0P8_SERDES_C4 / VDDA_1P8_SERDES4		4L_PHY	
		DP0_TXP3			O									
		SGMII8_TXP0		No	O									
Y31	SOC_SAFETY_ERRORn PADCONFIG PADCONFIG_68 0x0011C110	SOC_SAFETY_ERRORn	0		IO		Off / Off / Down	On / SS / Down	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
V31	SPI0_CLK PADCONFIG PADCONFIG_53 0x0011C0D4	SPI0_CLK	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_CTSn	1		I	1								
		I2C2_SCL	2		IOD	1								
		MCASP3_AXR0	3		IO	0								
		EHRPWM2_A	5		IO	0								
		GPIO0_53	7		IO	pad								
		UART8_TXD	11		O									
Y33	SPI0_CS0 PADCONFIG PADCONFIG_51 0x0011C0CC	SPI0_CS0	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		MCASP3_ACLKX	3		IO	0								
		MCASP3_ACLKR	4		IO	0								
		EHRPWM0_A	5		IO	0								
		GPIO0_51	7		IO	pad								
		MCAN14_TX	9		O									
		DP0_HPD	12		I	0								
Y32	SPI0_CS1 PADCONFIG PADCONFIG_52 0x0011C0D0	SPI0_CS1	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_TS_COMP	1		O									
		UART0_RTSn	2		O									
		MCASP3_AFSX	3		IO	0								
		MCASP3_AFSR	4		IO	0								
		EHRPWM1_A	5		IO	0								
		GPIO0_52	7		IO	pad								
		MCAN14_RX	9		I	1								
		UART8_RXD	11		I	1								
V30	SPI0_D0 PADCONFIG PADCONFIG_54 0x0011C0D8	SPI0_D0	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RTSn	1		O									
		I2C2_SDA	2		IOD	1								
		MCASP3_AXR1	3		IO	0								
		EHRPWM3_A	5		IO	0								
		GPIO0_54	7		IO	pad								
		UART2_RXD	11		I	1								
W31	SPI0_D1 PADCONFIG PADCONFIG_55 0x0011C0DC	SPI0_D1	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		MCASP3_AXR2	3		IO	0								
		EHRPWM4_A	5		IO	0								
		GPIO0_55	7		IO	pad								
		UART2_TXD	11		O									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
F21	TCK PADCONFIG WKUP_PADCONFIG_73 0x4301C124	TCK	0		I		On / NA / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
V33	TDI PADCONFIG PADCONFIG_69 0x0011C114	TDI	0		I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
W33	TDO PADCONFIG PADCONFIG_70 0x0011C118	TDO	0		OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
AA32	TIMER_IO0 PADCONFIG PADCONFIG_58 0x0011C0E8	TIMER_IO0	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP1_IN_APWM_OUT	1		IO	0								
		SYSCLKOUT0	2		O									
		UART3_RXD	5		I	1								
		PCIE1_CLKREQn	6		IO	0								
		GPIO0_58	7		IO	pad								
		MMC1_SDCD	8		I	1								
		MCAN13_TX	9		O									
		I2C6_SDA	13		IOD	1								
W30	TIMER_IO1 PADCONFIG PADCONFIG_59 0x0011C0EC	TIMER_IO1	0		IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP2_IN_APWM_OUT	1		IO	0								
		UART3_TXD	5		O									
		USB0_DRVVBUS	6		O									
		GPIO0_59	7		IO	pad								
		MMC1_SDWP	8		I	1								
		MCAN13_RX	9		I	1								
		I2C6_SCL	13		IOD	1								
V32	TMS PADCONFIG PADCONFIG_71 0x0011C11C	TMS	0		I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
F17	TRSTn PADCONFIG WKUP_PADCONFIG_74 0x4301C128	TRSTn	0		I		On / NA / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
AJ5	UFS0_REF_CLK	UFS0_REF_CLK			O					1.2 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AJ7	UFS0_RSTn	UFS0_RSTn			O					1.2 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AK5	UFS0_RX_DN0	UFS0_RX_DN0			I					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AL4	UFS0_RX_DN1	UFS0_RX_DN1			I					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AK6	UFS0_RX_DP0	UFS0_RX_DP0			I					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AL5	UFS0_RX_DP1	UFS0_RX_DP1			I					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AN2	UFS0_TX_DN0	UFS0_TX_DN0			O					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AM3	UFS0_TX_DN1	UFS0_TX_DN1			O					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AN3	UFS0_TX_DP0	UFS0_TX_DP0			O					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AM4	UFS0_TX_DP1	UFS0_TX_DP1			O					1.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY	
AH16	USB0_DM	USB0_DM			IO					3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY	
AH17	USB0_DP	USB0_DP			IO					3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY	
AH20	USB0_ID	USB0_ID			A					3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY	
AH22	USB0_RCALIB	USB0_RCALIB			A					3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY	
AG19	USB0_VBUS	USB0_VBUS			A					5.0 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		DDR	
AA22, AD13, AD16, AD19, AE26, AE9, P23, Y25	VDDAR_CORE	VDDAR_CORE			PWR									
AA14, AA16, AA18, AC10, K19, L21, P13, R18, U12, U19, V17, V9, Y11	VDDAR_CPU	VDDAR_CPU			PWR									
K25, L22	VDDAR_MCU	VDDAR_MCU			PWR									
AG22	VDDA_0P8_DSITX	VDDA_0P8_DSITX			PWR									
AG23	VDDA_0P8_DSITX_C	VDDA_0P8_DSITX_C			PWR									
AF9	VDDA_0P8_UFS	VDDA_0P8_UFS			PWR									
AG17	VDDA_0P8_USB	VDDA_0P8_USB			PWR									
AG26	VDDA_0P8_CSIRX2	VDDA_0P8_CSIRX2			PWR									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AG24	VDDA_0P8_CSIRX0_1	VDDA_0P8_CSIRX0_1			PWR									
AD7	VDDA_0P8_DLL_MMC0	VDDA_0P8_DLL_MMC0			PWR									
P8	VDDA_0P8_PLL_DDR0	VDDA_0P8_PLL_DDR0			PWR									
J11	VDDA_0P8_PLL_DDR1	VDDA_0P8_PLL_DDR1			PWR									
AG15, AG16	VDDA_0P8_SERDES4	VDDA_0P8_SERDES4			PWR									
AF12, AG10, AG13	VDDA_0P8_SERDES0_1	VDDA_0P8_SERDES0_1			PWR									
AE15, AF16	VDDA_0P8_SERDES_C4	VDDA_0P8_SERDES_C4			PWR									
AF10, AF13	VDDA_0P8_SERDES_C0_1	VDDA_0P8_SERDES_C0_1			PWR									
AF22, AF23	VDDA_1P8_DSITX	VDDA_1P8_DSITX			PWR									
AG8	VDDA_1P8_UFS	VDDA_1P8_UFS			PWR									
AH19	VDDA_1P8_USB	VDDA_1P8_USB			PWR									
AF27, AG27	VDDA_1P8_CSIRX2	VDDA_1P8_CSIRX2			PWR									
AF25, AF26	VDDA_1P8_CSIRX0_1	VDDA_1P8_CSIRX0_1			PWR									
AF15	VDDA_1P8_SERDES4	VDDA_1P8_SERDES4			PWR									
AG11, AG12	VDDA_1P8_SERDES0_1	VDDA_1P8_SERDES0_1			PWR									
AG21	VDDA_1P8_SERDES2_4	VDDA_1P8_SERDES2_4			PWR									
AF17	VDDA_3P3_USB	VDDA_3P3_USB			PWR									
J28	VDDA_ADC0	VDDA_ADC0			PWR									
K28	VDDA_ADC1	VDDA_ADC1			PWR									
K26	VDDA_MCU_PLLGRP0	VDDA_MCU_PLLGRP0			PWR									
K24	VDDA_MCU_TEMP	VDDA_MCU_TEMP			PWR									
L27	VDDA_OSC1	VDDA_OSC1			PWR									
W25	VDDA_PLLGRP0	VDDA_PLLGRP0			PWR									
V25	VDDA_PLLGRP1	VDDA_PLLGRP1			PWR									
AE11	VDDA_PLLGRP2	VDDA_PLLGRP2			PWR									
T12	VDDA_PLLGRP5	VDDA_PLLGRP5			PWR									
N19	VDDA_PLLGRP6	VDDA_PLLGRP6			PWR									
M10	VDDA_PLLGRP7	VDDA_PLLGRP7			PWR									
K13	VDDA_PLLGRP8	VDDA_PLLGRP8			PWR									
V24	VDDA_PLLGRP9	VDDA_PLLGRP9			PWR									
AD20	VDDA_PLLGRP10	VDDA_PLLGRP10			PWR									
W21	VDDA_PLLGRP12	VDDA_PLLGRP12			PWR									
Y24	VDDA_PLLGRP13	VDDA_PLLGRP13			PWR									
L26	VDDA_POR_WKUP	VDDA_POR_WKUP			PWR									
V26	VDDA_TEMP0	VDDA_TEMP0			PWR									
K10	VDDA_TEMP1	VDDA_TEMP1			PWR									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
U21	VDDA_TEMP2	VDDA_TEMP2			PWR									
AC11	VDDA_TEMP3	VDDA_TEMP3			PWR									
AB16	VDDA_TEMP4	VDDA_TEMP4			PWR									
J27	VDDA_WKUP	VDDA_WKUP			PWR									
T28	VDDSHV0	VDDSHV0			PWR									
H27	VDDSHV0_MCU	VDDSHV0_MCU			PWR									
G22, H23	VDDSHV1_MCU	VDDSHV1_MCU			PWR									
N28, P28	VDDSHV2	VDDSHV2			PWR									
G24, H25	VDDSHV2_MCU	VDDSHV2_MCU			PWR									
N27	VDDSHV5	VDDSHV5			PWR									
A2, AH1, G10, G12, G14, G16, G18, H11, H13, H15, H17, H9, J10, J14, J16, J8, K7, L8, M7, P7, R8	VDDS_DDR	VDDS_DDR			PWR									
N8	VDDS_DDR_C0	VDDS_DDR_C0			PWR									
J12	VDDS_DDR_C1	VDDS_DDR_C1			PWR									
AE8, AF7	VDDS_MMC0	VDDS_MMC0			PWR									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AA24, AA26, AA28, AB23, AB25, AB27, AC22, AC24, AC26, AC28, AD11, AD15, AD17, AD21, AD23, AD25, AD27, AE10, AE12, AE14, AE16, AE18, AE20, AE22, AE24, AE28, AF19, K11, K15, K17, K9, L10, L12, L14, L16, M11, M13, M15, M17, M9, N10, N12, N14, N16, N22, N24, N26, P11, P25, P9, R10, R22, R24, R26, T23, T25, U22, U24, U26, U28, V23, V27, W22, W24, W26, W28, Y23, Y27	VDD_CORE	VDD_CORE			PWR									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AA10, AA12, AA20, AA8, AB11, AB13, AB15, AB17, AB19, AB21, AB9, AC12, AC14, AC16, AC18, AC20, AC8, AD9, H19, H21, J18, J20, L18, L20, M19, N18, N20, P15, P17, P19, P21, R12, R20, T11, T17, T19, T21, T9, U10, U18, U20, U8, V11, V19, V21, W10, W12, W18, W20, W8, Y17, Y19, Y21, Y9	VDD_CPU	VDD_CPU			PWR									
J22, K21, K23, L24, M21, M23, M25	VDD_MCU	VDD_MCU			PWR									
J26	VDD_MCU_WAKE1	VDD_MCU_WAKE1			PWR									
R27	VDD_WAKE0	VDD_WAKE0			PWR									
G26	VMON1_ER_VSYS	VMON1_ER_VSYS			A									
L25	VMON2_IR_VCPU	VMON2_IR_VCPU			A									
K30	VMON3_IR_VEXT1P8	VMON3_IR_VEXT1P8			A									
M26	VMON4_IR_VEXT1P8	VMON4_IR_VEXT1P8			A									
M29	VMON5_IR_VEXT3P3	VMON5_IR_VEXT3P3			A									
V29	VPP_CORE	VPP_CORE			PWR									
F26	VPP_MCU	VPP_MCU			PWR									
E15	WKUP_GPIO0_0 PADCONFIG WKUP_PADCONFIG_48 0x4301C0C0	MCU_SPI1_CLK	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_CLK	1		IO	0								
		WKUP_GPIO0_0	7		IO	pad								
		MCU_BOOTMODE03	Bootstrap		I									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
D16	WKUP_GPIO0_1 PADCONFIG WKUP_PADCONFIG_49 0x4301C0C4	MCU_SPI1_D0	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_D0	1		IO	0								
		WKUP_GPIO0_1	7		IO	pad								
		MCU_BOOTMODE04	Bootstrap		I									
D18	WKUP_GPIO0_2 PADCONFIG WKUP_PADCONFIG_50 0x4301C0C8	MCU_SPI1_D1	0		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_D1	1		IO	0								
		WKUP_GPIO0_2	7		IO	pad								
		MCU_BOOTMODE05	Bootstrap		I									
D19	WKUP_GPIO0_3 PADCONFIG WKUP_PADCONFIG_51 0x4301C0CC	MCU_SPI1_CS0	0		IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_CS0	1		IO	1								
		WKUP_GPIO0_3	7		IO	pad								
E16	WKUP_GPIO0_4 PADCONFIG WKUP_PADCONFIG_52 0x4301C0D0	MCU_MCAN1_TX	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_MCAN1_TX	1		O									
		MCU_SPI0_CS3	2		IO	1								
		MCU_ADC_EXT_TRIGGER0	3		I	pad								
		WKUP_GPIO0_4	7		IO	pad								
D20	WKUP_GPIO0_5 PADCONFIG WKUP_PADCONFIG_53 0x4301C0D4	MCU_MCAN1_RX	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_MCAN1_RX	1		I	1								
		MCU_SPI1_CS3	2		IO	1								
		MCU_ADC_EXT_TRIGGER1	3		I	pad								
		WKUP_GPIO0_5	7		IO	pad								
B15	WKUP_GPIO0_6 PADCONFIG WKUP_PADCONFIG_54 0x4301C0D8	WKUP_UART0_CTSn	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_UART0_CTSn	1		I	1								
		MCU_CPTS0_HW1TSPUSH	2		I	0								
		MCU_I2C1_SCL	3		IOD	1								
		WKUP_GPIO0_6	7		IO	pad								
B17	WKUP_GPIO0_7 PADCONFIG WKUP_PADCONFIG_55 0x4301C0DC	WKUP_UART0_RTSn	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_UART0_RTSn	1		O									
		MCU_CPTS0_HW2TSPUSH	2		I	0								
		MCU_I2C1_SDA	3		IOD	1								
		WKUP_GPIO0_7	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
B19	WKUP_GPIO0_8 PADCONFIG WKUP_PADCONFIG_56 0x4301C0E0	MCU_I2C1_SCL	0		IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_I2C1_SCL	1		IOD	1								
		MCU_CPTS0_TS_SYNC	2		O									
		MCU_I3C0_SCL	3		IO	1								
		MCU_TIMER_IO6	4		IO	0								
		WKUP_GPIO0_8	7		IO	pad								
A15	WKUP_GPIO0_9 PADCONFIG WKUP_PADCONFIG_57 0x4301C0E4	MCU_I2C1_SDA	0		IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_I2C1_SDA	1		IOD	1								
		MCU_CPTS0_TS_COMP	2		O									
		MCU_I3C0_SDA	3		IO	1								
		MCU_TIMER_IO7	4		IO	0								
		WKUP_GPIO0_9	7		IO	pad								
B18	WKUP_GPIO0_10 PADCONFIG WKUP_PADCONFIG_58 0x4301C0E8	MCU_EXT_REFCLK0	0		I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_EXT_REFCLK0	1		I	0								
		MCU_UART0_TXD	2		O									
		MCU_ADC_EXT_TRIGGER0	3		I	0								
		MCU_CPTS0_RFT_CLK	4		I	0								
		MCU_SYSCLKOUT0	5		O									
		WKUP_GPIO0_10	7		IO	pad								
B21	WKUP_GPIO0_11 PADCONFIG WKUP_PADCONFIG_59 0x4301C0EC	MCU_OBSCLK0	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1		O									
		MCU_UART0_RXD	2		I	1								
		MCU_ADC_EXT_TRIGGER1	3		I	0								
		MCU_TIMER_IO1	4		IO	0								
		MCU_I3C0_SDAPULLEN	5		OD									
		MCU_CLKOUT0	6		OZ									
		WKUP_GPIO0_11	7		IO	pad								
D17	WKUP_GPIO0_12 PADCONFIG WKUP_PADCONFIG_60 0x4301C0F0	MCU_UART0_TXD	0		O		On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI0_CS1	1		IO	1								
		WKUP_GPIO0_12	7		IO	pad								
		MCU_BOOTMODE08	Bootstrap		I									
D21	WKUP_GPIO0_13 PADCONFIG WKUP_PADCONFIG_61 0x4301C0F4	MCU_UART0_RXD	0		I	1	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_CS1	1		IO	1								
		WKUP_GPIO0_13	7		IO	pad								
		MCU_BOOTMODE09	Bootstrap		I									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
D15	WKUP_GPIO0_14 PADCONFIG WKUP_PADCONFIG_62 0x4301C0F8	MCU_UART0_CTSn	0		I	1	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI0_CS2	1		IO	1								
		MCU_TIMER_IO8	4		IO	0								
		WKUP_GPIO0_14	7		IO	pad								
		MCU_BOOTMODE06	Bootstrap		I									
C16	WKUP_GPIO0_15 PADCONFIG WKUP_PADCONFIG_63 0x4301C0FC	MCU_UART0_RTSn	0		O		On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_SPI1_CS2	1		IO	1								
		MCU_TIMER_IO9	4		IO	0								
		WKUP_GPIO0_15	7		IO	pad								
		MCU_BOOTMODE07	Bootstrap		I									
A20	WKUP_GPIO0_49 PADCONFIG WKUP_PADCONFIG_100 0x4301C190	PMIC_WAKE1	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		MCU_EXT_REFCLK0	1		I	0								
		MCU_CPTS0_RFT_CLK	2		I	0								
		WKUP_GPIO0_49	7		IO	pad								
A19	WKUP_GPIO0_56 PADCONFIG WKUP_PADCONFIG_72 0x4301C120	MCU_TIMER_IO6	4		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_56	7		IO	pad								
		BOOTMODE04	Bootstrap		I									
B20	WKUP_GPIO0_57 PADCONFIG WKUP_PADCONFIG_95 0x4301C17C	MCU_TIMER_IO7	4		IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_57	7		IO	pad								
		BOOTMODE05	Bootstrap		I									
A17	WKUP_GPIO0_66 PADCONFIG WKUP_PADCONFIG_96 0x4301C180	WKUP_GPIO0_66	7		IO	pad	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		BOOTMODE06	Bootstrap		I									
A18	WKUP_GPIO0_67 PADCONFIG WKUP_PADCONFIG_97 0x4301C184	WKUP_LF_CLKIN	1		I	pad	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
		WKUP_GPIO0_67	7		IO	pad								
		BOOTMODE07	Bootstrap		I									
A16	WKUP_I2C0_SCL PADCONFIG WKUP_PADCONFIG_64 0x4301C100	WKUP_I2C0_SCL	0		IOD	1	Off / Off / NA	On / SS / NA	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OPEN DRAIN	
		WKUP_GPIO0_63	7		IO	pad								
D23	WKUP_I2C0_SDA PADCONFIG WKUP_PADCONFIG_65 0x4301C104	WKUP_I2C0_SDA	0		IOD	1	Off / Off / NA	On / SS / NA	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OPEN DRAIN	
		WKUP_GPIO0_64	7		IO	pad								
A24	WKUP_OSC0_XI	WKUP_OSC0_XI			I					1.8 V	VDDA_WKUP	Yes	HFXOSC	

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
B25	WKUP_OSC0_XO	WKUP_OSC0_XO			O					1.8 V	VDDA_WKUP	Yes	HFXOSC	
C20	WKUP_UART0_RXD	WKUP_UART0_RXD	0		I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_44 0x4301C0B0	WKUP_GPIO0_58	7		IO	pad								
C19	WKUP_UART0_TXD	WKUP_UART0_TXD	0		O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG WKUP_PADCONFIG_45 0x4301C0B4	WKUP_GPIO0_59	7		IO	pad								

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
A1, A23, A25, A27, A29, A31, A4, A7, AA11, AA13, AA15, AA17, AA19, AA2, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA5, AA9, AB1, AB10, AB12, AB14, AB18, AB20, AB22, AB24, AB26, AB28, AB30, AB32, AB4, AB8, AC13, AC15, AC17, AC19, AC2, AC21, AC23, AC25, AC27, AC5, AC9, AD10, AD12, AD14, AD18, AD22, AD24, AD26, AD28, AD29, AD3, AD31, AD33, AD6, AD8, AE1, AE13, AE17, AE19, AE21, AE23, AE25, AE27, AE30, AE32, AE4, AE7, AF11, AF14, AF18, AF2, AF20, AF21, AF24, AF28, AF5, AF8, AG14, AG18, AG20, AG25, AG28, AG29, AG3, AG31, AG33, AG6, AG9, AH12, AH15, AH18, AH21, AH24, AH26, AH28, AH30, AH5, AJ11, AJ14, AJ17, AJ20, AJ23, AJ26, AJ29, AJ32, AJ6, AJ8, AK10, AK13, AK16, AK19,	VSS	VSS			GND									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AK22, AK25, AK28, AK31, AK4, AK7, AL12, AL15, AL18, AL21, AL24, AL27, AL3, AL30, AL33, AL6, AL9, AM11, AM14, AM17, AM2, AM20, AM23, AM26, AM29, AM32, AM33, AM5, AM8, AN1, AN10, AN13, AN16														

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
AN19, AN22, AN25, AN28, AN31, AN32, AN4, AN7, B22, B24, B26, B28, B3, B30, B32, B6, C11, C13, C15, C17, C2, C21, C23, C25, C27, C29, C31, C33, C5, D1, D26, D28, D30, D32, D4, D7, E23, E25, E27, E29, E3, E31, E6, E8, F14, F16, F18, F2, F20, F22, F24, F5, F7, G1, G11, G13, G15, G17, G19, G21, G23, G25, G27, G4, G9, H10, H12, H14, H16, H18, H2, H20, H22, H24, H26, H28, H5, H8, J1, J13, J15, J17, J19, J21, J6, J7, J9, K12, K14, K16, K18, K2, K20, K22, K27, K29, K5, K8, L11, L13, L15, L17, L19, L23, L3, L6, L7, L9, M1, M12, M14, M16, M18, M20, M22, M24, M28, M4, M8, N11, N13, N15, N17, N2, N21, N23, N25, N29, N5, N7, N9,	VSS (continued)	VSS			GND									

Table 5-1. Pin Attributes (AND Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [16] PADCONFIG Address [17]	SIGNAL NAME [3]	MUX MODE [4]	VPE4 APE4 [5]	TYPE [6]	DSIS [7]	BALL STATE DURING RESET (RX/TX/PULL) [8]	BALL STATE AFTER RESET (RX/TX/PULL) [9]	MUX MODE AFTER RESET [10]	I/O OPERATING VOLTAGE [11]	POWER [12]	HYS [13]	BUFFER TYPE [14]	PULL UP/DOWN TYPE [15]
P10, P12, P14, P16, P18, P20, P22, P24, P26, P3, R11, R17, R19, R21, R23, R25, R28, R3, R6														
R9, T10, T18, T2, T20, T22, T24, T26, T5, T8, U1, U11, U17, U23, U25, U27, U29, U33, U4, U7, U9, V10, V12, V18, V20, V22, V28, V3, V6, V8, W11, W17, W19, W2, W23, W27, W29, W5, W9, Y1, Y10, Y12, Y18, Y20, Y22, Y26, Y28, Y6, Y8	VSS (continued)	VSS			GND									

(1) The MUXMODE field is not used to select the multiplexed signal function for this pin. For more information, see *ADC Integration Details* section in *Device Configuration* chapter of the device TRM.

5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Ball number(s) associated with signal

5.3.1 ADC

5.3.1.1 MCU Domain

Table 5-2. MCU_ADC Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_ADC_EXT_TRIGGER0	I	ADC Trigger Input	A12, B18, E16
MCU_ADC_EXT_TRIGGER1	I	ADC Trigger Input	B12, B21, D20

Table 5-3. MCU_ADC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_ADC0_REFN	A	ADC Reference (Negative)	C26
MCU_ADC0_REFP	A	ADC Reference (Positive)	D25
MCU_ADC0_AIN0	A	ADC Input 0	E26
MCU_ADC0_AIN1	A	ADC Input 1	F25
MCU_ADC0_AIN2	A	ADC Input 2	F23
MCU_ADC0_AIN3	A	ADC Input 3	A28
MCU_ADC0_AIN4	A	ADC Input 4	E24
MCU_ADC0_AIN5	A	ADC Input 5	D27
MCU_ADC0_AIN6	A	ADC Input 6	A26

Table 5-3. MCU_ADC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_ADC0_AIN7	A	ADC Input 7	B27

Table 5-4. MCU_ADC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_ADC1_REFN	A	ADC Reference (Negative)	D29
MCU_ADC1_REFP	A	ADC Reference (Positive)	C30
MCU_ADC1_AIN0	A	ADC Input 0	C32
MCU_ADC1_AIN1	A	ADC Input 1	B33
MCU_ADC1_AIN2	A	ADC Input 2	B31
MCU_ADC1_AIN3	A	ADC Input 3	B29
MCU_ADC1_AIN4	A	ADC Input 4	D31
MCU_ADC1_AIN5	A	ADC Input 5	A32
MCU_ADC1_AIN6	A	ADC Input 6	A30
MCU_ADC1_AIN7	A	ADC Input 7	C28

5.3.2 CPSW2G

5.3.2.1 MAIN Domain

Table 5-5. CPSW2G0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CLKOUT	IO	RMII Clock Output	U31
RGMII1_RXC	I	RGMII Receive Clock	P31
RGMII1_RX_CTL	I	RGMII Receive Control	M33
RGMII1_TXC	O	RGMII Transmit Clock	N31
RGMII1_TX_CTL	O	RGMII Transmit Control	P30
RGMII1_RD0	I	RGMII Receive Data 0	U32
RGMII1_RD1	I	RGMII Receive Data 1	M32
RGMII1_RD2	I	RGMII Receive Data 2	L33
RGMII1_RD3	I	RGMII Receive Data 3	U31
RGMII1_TD0	O	RGMII Transmit Data 0	M31
RGMII1_TD1	O	RGMII Transmit Data 1	N30
RGMII1_TD2	O	RGMII Transmit Data 2	T33
RGMII1_TD3	O	RGMII Transmit Data 3	L32
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	L32
RMII1_RX_ER	I	RMII Receive Data Error	P30
RMII1_TX_EN	O	RMII Transmit Enable	M33
RMII1_RXD0	I	RMII Receive Data 0	N30
RMII1_RXD1	I	RMII Receive Data 1	T33
RMII1_TXD0	O	RMII Transmit Data 0	M32
RMII1_TXD1	O	RMII Transmit Data 1	P31
RMII_REF_CLK	I	RMII Reference Clock	L33

5.3.2.2 MCU Domain

Table 5-6. MCU_CPSW2G0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_RGMII1_RXC	I	RGMII Receive Clock	C14
MCU_RGMII1_RX_CTL	I	RGMII Receive Control	C12
MCU_RGMII1_TXC	O	RGMII Transmit Clock	A14
MCU_RGMII1_TX_CTL	O	RGMII Transmit Control	B14
MCU_RGMII1_RD0	I	RGMII Receive Data 0	E13
MCU_RGMII1_RD1	I	RGMII Receive Data 1	D14
MCU_RGMII1_RD2	I	RGMII Receive Data 2	D12
MCU_RGMII1_RD3	I	RGMII Receive Data 3	D13
MCU_RGMII1_TD0	O	RGMII Transmit Data 0	B13
MCU_RGMII1_TD1	O	RGMII Transmit Data 1	A13
MCU_RGMII1_TD2	O	RGMII Transmit Data 2	B12
MCU_RGMII1_TD3	O	RGMII Transmit Data 3	A12
MCU_RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	B14
MCU_RMII1_REF_CLK	I	RMII Reference Clock	C14
MCU_RMII1_RX_ER	I	RMII Receive Data Error	C12
MCU_RMII1_TX_EN	O	RMII Transmit Enable	A14
MCU_RMII1_RXD0	I	RMII Receive Data 0	E13
MCU_RMII1_RXD1	I	RMII Receive Data 1	D14
MCU_RMII1_TXD0	O	RMII Transmit Data 0	B13
MCU_RMII1_TXD1	O	RMII Transmit Data 1	A13

5.3.3 CPTS

5.3.3.1 MAIN Domain

Table 5-7. CPTS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CPTS0_RFT_CLK	I	CPTS Reference Clock	L31
CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare	Y32
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit	E30
CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push 1	L31
CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push 2	J33

5.3.3.2 MCU Domain

Table 5-8. MCU_CPTS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_CPTS0_RFT_CLK	I	CPTS Reference Clock	A20, B18
MCU_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare	A15
MCU_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit	B19
MCU_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push 1	B15
MCU_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push 2	B17

5.3.4 CSI

5.3.4.1 MAIN Domain

Table 5-9. CSI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI0_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AH33
CSI0_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AH32
CSI0_RXRCALIB (1)	A	CSI Pin connected to external resistor for on-chip resistor calibration	AH31
CSI0_RXN0	I	CSI Differential Receive Input (negative)	AL32
CSI0_RXN1	I	CSI Differential Receive Input (negative)	AM31
CSI0_RXN2	I	CSI Differential Receive Input (negative)	AN30
CSI0_RXN3	I	CSI Differential Receive Input (negative)	AK33
CSI0_RXP0	I	CSI Differential Receive Input (positive)	AL31
CSI0_RXP1	I	CSI Differential Receive Input (positive)	AM30
CSI0_RXP2	I	CSI Differential Receive Input (positive)	AN29
CSI0_RXP3	I	CSI Differential Receive Input (positive)	AK32

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

Table 5-10. CSI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI1_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AE29
CSI1_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AF29
CSI1_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AJ33
CSI1_RXN0	I	CSI Differential Receive Input (negative)	AF30
CSI1_RXN1	I	CSI Differential Receive Input (negative)	AE33
CSI1_RXN2	I	CSI Differential Receive Input (negative)	AE31
CSI1_RXN3	I	CSI Differential Receive Input (negative)	AF32
CSI1_RXP0	I	CSI Differential Receive Input (positive)	AG30
CSI1_RXP1	I	CSI Differential Receive Input (positive)	AF33
CSI1_RXP2	I	CSI Differential Receive Input (positive)	AF31
CSI1_RXP3	I	CSI Differential Receive Input (positive)	AG32

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

Table 5-11. CSI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI2_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AC29
CSI2_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AB29
CSI2_RXRCALIB (1)	A	CSI Pin connected to external resistor for on-chip resistor calibration	AH29
CSI2_RXN0	I	CSI Differential Receive Input (negative)	AC30
CSI2_RXN1	I	CSI Differential Receive Input (negative)	AB31
CSI2_RXN2	I	CSI Differential Receive Input (negative)	AC32
CSI2_RXN3	I	CSI Differential Receive Input (negative)	AB33
CSI2_RXP0	I	CSI Differential Receive Input (positive)	AD30
CSI2_RXP1	I	CSI Differential Receive Input (positive)	AC31

Table 5-11. CSI2 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI2_RXP2	I	CSI Differential Receive Input (positive)	AD32
CSI2_RXP3	I	CSI Differential Receive Input (positive)	AC33

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

5.3.5 DDRSS

5.3.5.1 MAIN Domain

Table 5-12. DDRSS0 Signal Descriptions

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DDR0_CKN	IO	DDRSS Differential Clock (negative)	Y2
DDR0_CKP	IO	DDRSS Differential Clock (positive)	AA1
DDR0_RESETn	IO	DDRSS Reset	W7
DDR0_RET	I	DDR Retention Enable	AC7
DDR0_CA0	IO	DDRSS Command Address	AA3
DDR0_CA1	IO	DDRSS Command Address	Y4
DDR0_CA2	IO	DDRSS Command Address	AA4
DDR0_CA3	IO	DDRSS Command Address	AB3
DDR0_CA4	IO	DDRSS Command Address	Y3
DDR0_CA5	IO	DDRSS Command Address	AB5
DDR0_CAL0 (1)	A	IO Pad Calibration Resistor	R7
DDR0_CKE0	IO	DDRSS Clock Enable	AB6
DDR0_CKE1	IO	DDRSS Clock Enable	AB7
DDR0_CSn0_0	IO	DDRSS Chip Select	AA6
DDR0_CSn0_1	IO	DDRSS Chip Select	Y5
DDR0_CSn1_0	IO	DDRSS Chip Select	Y7
DDR0_CSn1_1	IO	DDRSS Chip Select	AA7
DDR0_DM0	IO	DDRSS Data Mask	U6
DDR0_DM1	IO	DDRSS Data Mask	V2
DDR0_DM2	IO	DDRSS Data Mask	AE2
DDR0_DM3	IO	DDRSS Data Mask	AF6
DDR0_DQ0	IO	DDRSS Data	R5
DDR0_DQ1	IO	DDRSS Data	R4
DDR0_DQ2	IO	DDRSS Data	R2
DDR0_DQ3	IO	DDRSS Data	T4
DDR0_DQ4	IO	DDRSS Data	U5
DDR0_DQ5	IO	DDRSS Data	T3
DDR0_DQ6	IO	DDRSS Data	T6
DDR0_DQ7	IO	DDRSS Data	T7
DDR0_DQ8	IO	DDRSS Data	V4
DDR0_DQ9	IO	DDRSS Data	V7
DDR0_DQ10	IO	DDRSS Data	W3
DDR0_DQ11	IO	DDRSS Data	V5
DDR0_DQ12	IO	DDRSS Data	W6
DDR0_DQ13	IO	DDRSS Data	U2
DDR0_DQ14	IO	DDRSS Data	W4

Table 5-12. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DDR0_DQ15	IO	DDRSS Data	U3
DDR0_DQ16	IO	DDRSS Data	AD5
DDR0_DQ17	IO	DDRSS Data	AC3
DDR0_DQ18	IO	DDRSS Data	AE3
DDR0_DQ19	IO	DDRSS Data	AB2
DDR0_DQ20	IO	DDRSS Data	AC4
DDR0_DQ21	IO	DDRSS Data	AD2
DDR0_DQ22	IO	DDRSS Data	AC6
DDR0_DQ23	IO	DDRSS Data	AD4
DDR0_DQ24	IO	DDRSS Data	AG4
DDR0_DQ25	IO	DDRSS Data	AG2
DDR0_DQ26	IO	DDRSS Data	AF3
DDR0_DQ27	IO	DDRSS Data	AE5
DDR0_DQ28	IO	DDRSS Data	AE6
DDR0_DQ29	IO	DDRSS Data	AG5
DDR0_DQ30	IO	DDRSS Data	AF4
DDR0_DQ31	IO	DDRSS Data	AH6
DDR0_DQS0N	IO	DDRSS Complimentary Data Strobe	T1
DDR0_DQS0P	IO	DDRSS Data Strobe	R1
DDR0_DQS1N	IO	DDRSS Complimentary Data Strobe	W1
DDR0_DQS1P	IO	DDRSS Data Strobe	V1
DDR0_DQS2N	IO	DDRSS Complimentary Data Strobe	AC1
DDR0_DQS2P	IO	DDRSS Data Strobe	AD1
DDR0_DQS3N	IO	DDRSS Complimentary Data Strobe	AF1
DDR0_DQS3P	IO	DDRSS Data Strobe	AG1

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(2) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces.

Table 5-13. DDRSS1 Signal Descriptions

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DDR1_CKN	IO	DDRSS Differential Clock (negative)	H1
DDR1_CKP	IO	DDRSS Differential Clock (positive)	J2
DDR1_RESETn	IO	DDRSS Reset	G5
DDR1_RET	I	DDR Retention Enable	G8
DDR1_CA0	IO	DDRSS Command Address	J4
DDR1_CA1	IO	DDRSS Command Address	H3
DDR1_CA2	IO	DDRSS Command Address	G2
DDR1_CA3	IO	DDRSS Command Address	J3
DDR1_CA4	IO	DDRSS Command Address	G3
DDR1_CA5	IO	DDRSS Command Address	H4
DDR1_CAL0 (1)	A	IO Pad Calibration Resistor	F8
DDR1_CKE0	IO	DDRSS Clock Enable	E7
DDR1_CKE1	IO	DDRSS Clock Enable	H6

Table 5-13. DDRSS1 Signal Descriptions (continued)

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DDR1_CSn0_0	IO	DDRSS Chip Select	G6
DDR1_CSn0_1	IO	DDRSS Chip Select	G7
DDR1_CSn1_0	IO	DDRSS Chip Select	H7
DDR1_CSn1_1	IO	DDRSS Chip Select	F6
DDR1_DM0	IO	DDRSS Data Mask	A3
DDR1_DM1	IO	DDRSS Data Mask	F3
DDR1_DM2	IO	DDRSS Data Mask	L2
DDR1_DM3	IO	DDRSS Data Mask	P2
DDR1_DQ0	IO	DDRSS Data	A6
DDR1_DQ1	IO	DDRSS Data	C6
DDR1_DQ2	IO	DDRSS Data	A5
DDR1_DQ3	IO	DDRSS Data	C4
DDR1_DQ4	IO	DDRSS Data	B4
DDR1_DQ5	IO	DDRSS Data	B2
DDR1_DQ6	IO	DDRSS Data	C3
DDR1_DQ7	IO	DDRSS Data	B5
DDR1_DQ8	IO	DDRSS Data	E5
DDR1_DQ9	IO	DDRSS Data	D2
DDR1_DQ10	IO	DDRSS Data	E2
DDR1_DQ11	IO	DDRSS Data	F4
DDR1_DQ12	IO	DDRSS Data	D6
DDR1_DQ13	IO	DDRSS Data	E4
DDR1_DQ14	IO	DDRSS Data	D3
DDR1_DQ15	IO	DDRSS Data	D5
DDR1_DQ16	IO	DDRSS Data	M3
DDR1_DQ17	IO	DDRSS Data	K4
DDR1_DQ18	IO	DDRSS Data	M2
DDR1_DQ19	IO	DDRSS Data	L5
DDR1_DQ20	IO	DDRSS Data	J5
DDR1_DQ21	IO	DDRSS Data	K3
DDR1_DQ22	IO	DDRSS Data	L4
DDR1_DQ23	IO	DDRSS Data	K6
DDR1_DQ24	IO	DDRSS Data	N6
DDR1_DQ25	IO	DDRSS Data	P4
DDR1_DQ26	IO	DDRSS Data	N3
DDR1_DQ27	IO	DDRSS Data	M5
DDR1_DQ28	IO	DDRSS Data	M6
DDR1_DQ29	IO	DDRSS Data	P5
DDR1_DQ30	IO	DDRSS Data	N4
DDR1_DQ31	IO	DDRSS Data	P6
DDR1_DQS0N	IO	DDRSS Complimentary Data Strobe	C1
DDR1_DQS0P	IO	DDRSS Data Strobe	B1
DDR1_DQS1N	IO	DDRSS Complimentary Data Strobe	F1
DDR1_DQS1P	IO	DDRSS Data Strobe	E1

Table 5-13. DDRSS1 Signal Descriptions (continued)

SIGNAL NAME [1] ((2))	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DDR1_DQS2N	IO	DDRSS Complimentary Data Strobe	K1
DDR1_DQS2P	IO	DDRSS Data Strobe	L1
DDR1_DQS3N	IO	DDRSS Complimentary Data Strobe	N1
DDR1_DQS3P	IO	DDRSS Data Strobe	P1

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(2) DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces.

5.3.6 Display Port

5.3.6.1 MAIN Domain

Table 5-14. DP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DP0_AUXN	IO	Display Port Differential Auxiliary Data (negative)	AJ25
DP0_AUXP	IO	Display Port Differential Auxiliary Data (positive)	AJ24
DP0_HPD	I	Display Port Hot Plug Detection	R33, U32, Y33
DP0_TXN0	O	Display Port Differential Transmit (negative)	AJ21
DP0_TXN1	O	Display Port Differential Transmit (negative)	AM18
DP0_TXN2	O	Display Port Differential Transmit (negative)	AN20
DP0_TXN3	O	Display Port Differential Transmit (negative)	AL22
DP0_TXP0	O	Display Port Differential Transmit (positive)	AJ22
DP0_TXP1	O	Display Port Differential Transmit (positive)	AM19
DP0_TXP2	O	Display Port Differential Transmit (positive)	AN21
DP0_TXP3	O	Display Port Differential Transmit (positive)	AL23

5.3.7 DMTIMER

5.3.7.1 MAIN Domain

Table 5-15. DMTIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	AA32
TIMER_IO1	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	W30
TIMER_IO2	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	F30
TIMER_IO3	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	E30
TIMER_IO4	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	F29
TIMER_IO5	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	F28
TIMER_IO6	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	D33
TIMER_IO7	IO	Timer Inputs and Outputs (Can be used with any MAIN domain timer instance)	E32

5.3.7.2 MCU Domain

Table 5-16. MCU_DMTIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	A9, E14
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	B21, E19
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	A12
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	B12
MCU_TIMER_IO4	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	D13
MCU_TIMER_IO5	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	D12
MCU_TIMER_IO6	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	A19, B19
MCU_TIMER_IO7	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	A15, B20
MCU_TIMER_IO8	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	D15
MCU_TIMER_IO9	IO	Timer Inputs and Outputs (Can be used with any MCU domain timer instance.)	C16

5.3.8 DSI

5.3.8.1 MAIN Domain

Table 5-17. DSI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI0_TXCLKN	O	CSI Differential Transmit Clock Output (negative)	AJ28
CSI0_TXCLKP	O	CSI Differential Transmit Clock Output (positive)	AJ27
CSI0_TXN0	O	CSI Differential Transmit Output (negative)	AL26
CSI0_TXN1	O	CSI Differential Transmit Output (negative)	AK27
CSI0_TXN2	O	CSI Differential Transmit Output (negative)	AM25
CSI0_TXN3	O	CSI Differential Transmit Output (negative)	AN24
CSI0_TXP0	O	CSI Differential Transmit Output (positive)	AL25
CSI0_TXP1	O	CSI Differential Transmit Output (positive)	AK26
CSI0_TXP2	O	CSI Differential Transmit Output (positive)	AM24
CSI0_TXP3	O	CSI Differential Transmit Output (positive)	AN23
DSI0_TXCLKN	O	DSI Transmit clock (negative)	AJ28
DSI0_TXCLKP	O	DSI Transmit clock (positive)	AJ27
DSI0_TXRCALIB (1)	A	DSI Transmit Calibration Resistor	AH25
DSI0_TXN0	IO	DSI Transmit (negative)	AL26
DSI0_TXN1	O	DSI Transmit (negative)	AK27
DSI0_TXN2	O	DSI Transmit (negative)	AM25
DSI0_TXN3	O	DSI Transmit (negative)	AN24
DSI0_TXP0	IO	DSI Transmit (positive)	AL25
DSI0_TXP1	O	DSI Transmit (positive)	AK26
DSI0_TXP2	O	DSI Transmit (positive)	AM24

Table 5-17. DSI0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DSI0_TXP3	O	DSI Transmit (positive)	AN23

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

Table 5-18. DSI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CSI1_TXCLKN	O	CSI Differential Transmit Clock Output (negative)	AJ31
CSI1_TXCLKP	O	CSI Differential Transmit Clock Output (positive)	AJ30
CSI1_TXN0	O	CSI Differential Transmit Output (negative)	AK30
CSI1_TXN1	O	CSI Differential Transmit Output (negative)	AL29
CSI1_TXN2	O	CSI Differential Transmit Output (negative)	AM28
CSI1_TXN3	O	CSI Differential Transmit Output (negative)	AN27
CSI1_TXP0	O	CSI Differential Transmit Output (positive)	AK29
CSI1_TXP1	O	CSI Differential Transmit Output (positive)	AL28
CSI1_TXP2	O	CSI Differential Transmit Output (positive)	AM27
CSI1_TXP3	O	CSI Differential Transmit Output (positive)	AN26
DSI1_TXCLKN	O	DSI Transmit clock (negative)	AJ31
DSI1_TXCLKP	O	DSI Transmit clock (positive)	AJ30
DSI1_TXRCALIB (1)	A	DSI Transmit Calibration Resistor	AH27
DSI1_TXN0	IO	DSI Transmit (negative)	AK30
DSI1_TXN1	O	DSI Transmit (negative)	AL29
DSI1_TXN2	O	DSI Transmit (negative)	AM28
DSI1_TXN3	O	DSI Transmit (negative)	AN27
DSI1_TXP0	IO	DSI Transmit (positive)	AK29
DSI1_TXP1	O	DSI Transmit (positive)	AL28
DSI1_TXP2	O	DSI Transmit (positive)	AM27
DSI1_TXP3	O	DSI Transmit (positive)	AN26

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

5.3.9 DSS

5.3.9.1 MAIN Domain

Table 5-19. DSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
DSS_FSYNC0	O	Video Output Frame Sync	G33, P29
DSS_FSYNC1	O	Video Output Frame Sync	T29, T30
DSS_FSYNC2	O	Video Output Frame Sync	P30, T31
DSS_FSYNC3	O	Video Output Frame Sync	M32, T32
VOUT0_DE	O	Video Output Data Enable	H30
VOUT0_EXTPCLKIN	I	Video Output External Pixel Clock Input	G33
VOUT0_HSYNC	O	Video Output Horizontal Sync	J32
VOUT0_PCLK	O	Video Output Pixel Clock Output	F33
VOUT0_VSYNC	O	Video Output Vertical Sync	K33
VOUT0_DATA0	O	Video Output Data 0	G28
VOUT0_DATA1	O	Video Output Data 1	H31

Table 5-19. DSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VOUT0_DATA2	O	Video Output Data 2	F31
VOUT0_DATA3	O	Video Output Data 3	G29
VOUT0_DATA4	O	Video Output Data 4	N33
VOUT0_DATA5	O	Video Output Data 5	R32
VOUT0_DATA6	O	Video Output Data 6	K32
VOUT0_DATA7	O	Video Output Data 7	G32
VOUT0_DATA8	O	Video Output Data 8	P33
VOUT0_DATA9	O	Video Output Data 9	J31
VOUT0_DATA10	O	Video Output Data 10	G31
VOUT0_DATA11	O	Video Output Data 11	H33
VOUT0_DATA12	O	Video Output Data 12	H32
VOUT0_DATA13	O	Video Output Data 13	F32
VOUT0_DATA14	O	Video Output Data 14	K31
VOUT0_DATA15	O	Video Output Data 15	J30
VOUT0_DATA16	O	Video Output Data 16	J33
VOUT0_DATA17	O	Video Output Data 17	E33
VOUT0_DATA18	O	Video Output Data 18	G28, P32
VOUT0_DATA19	O	Video Output Data 19	H31, U30
VOUT0_DATA20	O	Video Output Data 20	G30, P33
VOUT0_DATA21	O	Video Output Data 21	J31, R31
VOUT0_DATA22	O	Video Output Data 22	E33, R29
VOUT0_DATA23	O	Video Output Data 23	L31, R30
VOUT0_VP0_DE	O	Alternative Output Data Enable	H30
VOUT0_VP0_HSYNC	O	Alternative Output Horizontal Sync	J32
VOUT0_VP0_VSYNC	O	Alternative Output Vertical Sync	K33
VOUT0_VP2_DE	O	Alternative Output Data Enable	H30
VOUT0_VP2_HSYNC	O	Alternative Output Horizontal Sync	J32
VOUT0_VP2_VSYNC	O	Alternative Output Vertical Sync	K33

5.3.10 ECAP

5.3.10.1 MAIN Domain

Table 5-20. ECAP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	F29, L31

Table 5-21. ECAP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	AA32, F28

Table 5-22. ECAP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	W30

5.3.11 EPWM

5.3.11.1 MAIN Domain

Table 5-23. EPWM Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	G32
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	M32
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	F31
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	G31
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	J30
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	N30
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	K33
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	G33

Table 5-24. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM0_A	IO	EHRPWM Output A	E30, G29, Y33
EHRPWM0_B	IO	EHRPWM Output B	F30, N33
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	H31
EHRPWM0_SYNCO	O	Sync Output to EHRPWM module to an external pin	H32

Table 5-25. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM1_A	IO	EHRPWM Output A	F28, R32, Y32
EHRPWM1_B	IO	EHRPWM Output B	F29, G28

Table 5-26. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM2_A	IO	EHRPWM Output A	E32, F32, V31
EHRPWM2_B	IO	EHRPWM Output B	D33, K31

Table 5-27. EPWM3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM3_A	IO	EHRPWM Output A	F30, M31, V30
EHRPWM3_B	IO	EHRPWM Output B	P30
EHRPWM3_SYNCI	I	Sync Input to EHRPWM module from an external pin	L32
EHRPWM3_SYNCO	O	Sync Output to EHRPWM module to an external pin	T33

Table 5-28. EPWM4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM4_A	IO	EHRPWM Output A	F29, L33, W31
EHRPWM4_B	IO	EHRPWM Output B	F33

Table 5-29. EPWM5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EHRPWM5_A	IO	EHRPWM Output A	D33, H30
EHRPWM5_B	IO	EHRPWM Output B	J32

5.3.12 EQEP

5.3.12.1 MAIN Domain

Table 5-30. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EQEP0_A	I	EQEP Quadrature Input A	U31
EQEP0_B	I	EQEP Quadrature Input B	M33
EQEP0_I	IO	EQEP Index	N32
EQEP0_S	IO	EQEP Strobe	U32

Table 5-31. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EQEP1_A	I	EQEP Quadrature Input A	P31
EQEP1_B	I	EQEP Quadrature Input B	N31
EQEP1_I	IO	EQEP Index	E33
EQEP1_S	IO	EQEP Strobe	H29

Table 5-32. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EQEP2_A	I	EQEP Quadrature Input A	H33
EQEP2_B	I	EQEP Quadrature Input B	J31
EQEP2_I	IO	EQEP Index	K32
EQEP2_S	IO	EQEP Strobe	P33

5.3.13 GPIO

5.3.13.1 MAIN Domain

Table 5-33. GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPIO0_0	IO	General Purpose Input/Output	Y29
GPIO0_1	IO	General Purpose Input/Output	P29
GPIO0_2	IO	General Purpose Input/Output	T29
GPIO0_3	IO	General Purpose Input/Output	T31
GPIO0_4	IO	General Purpose Input/Output	T32
GPIO0_5	IO	General Purpose Input/Output	R33

Table 5-33. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPIO0_6	IO	General Purpose Input/Output	R30
GPIO0_7	IO	General Purpose Input/Output	R29
GPIO0_8	IO	General Purpose Input/Output	R31
GPIO0_9	IO	General Purpose Input/Output	G30
GPIO0_10	IO	General Purpose Input/Output	U30
GPIO0_11	IO	General Purpose Input/Output	P32
GPIO0_12	IO	General Purpose Input/Output	E33
GPIO0_13	IO	General Purpose Input/Output	T30
GPIO0_14	IO	General Purpose Input/Output	J30
GPIO0_15	IO	General Purpose Input/Output	K31
GPIO0_16	IO	General Purpose Input/Output	F32
GPIO0_17	IO	General Purpose Input/Output	H32
GPIO0_18	IO	General Purpose Input/Output	H33
GPIO0_19	IO	General Purpose Input/Output	G31
GPIO0_20	IO	General Purpose Input/Output	J31
GPIO0_21	IO	General Purpose Input/Output	P33
GPIO0_22	IO	General Purpose Input/Output	G32
GPIO0_23	IO	General Purpose Input/Output	K32
GPIO0_24	IO	General Purpose Input/Output	R32
GPIO0_25	IO	General Purpose Input/Output	N33
GPIO0_26	IO	General Purpose Input/Output	G29
GPIO0_27	IO	General Purpose Input/Output	G33
GPIO0_28	IO	General Purpose Input/Output	H31
GPIO0_29	IO	General Purpose Input/Output	G28
GPIO0_30	IO	General Purpose Input/Output	F33
GPIO0_31	IO	General Purpose Input/Output	F31
GPIO0_32	IO	General Purpose Input/Output	J32
GPIO0_33	IO	General Purpose Input/Output	H30
GPIO0_34	IO	General Purpose Input/Output	K33
GPIO0_35	IO	General Purpose Input/Output	M31
GPIO0_36	IO	General Purpose Input/Output	N30
GPIO0_37	IO	General Purpose Input/Output	T33
GPIO0_38	IO	General Purpose Input/Output	L32
GPIO0_39	IO	General Purpose Input/Output	P30
GPIO0_40	IO	General Purpose Input/Output	M32
GPIO0_41	IO	General Purpose Input/Output	L33
GPIO0_42	IO	General Purpose Input/Output	U31
GPIO0_43	IO	General Purpose Input/Output	M33
GPIO0_44	IO	General Purpose Input/Output	P31
GPIO0_45	IO	General Purpose Input/Output	N31
GPIO0_46	IO	General Purpose Input/Output	U32
GPIO0_47	IO	General Purpose Input/Output	N32
GPIO0_48	IO	General Purpose Input/Output	H29
GPIO0_49	IO	General Purpose Input/Output	L31

Table 5-33. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPIO0_50	IO	General Purpose Input/Output	J33
GPIO0_51	IO	General Purpose Input/Output	Y33
GPIO0_52	IO	General Purpose Input/Output	Y32
GPIO0_53	IO	General Purpose Input/Output	V31
GPIO0_54	IO	General Purpose Input/Output	V30
GPIO0_55	IO	General Purpose Input/Output	W31
GPIO0_56	IO	General Purpose Input/Output	AA30
GPIO0_57	IO	General Purpose Input/Output	Y30
GPIO0_58	IO	General Purpose Input/Output	AA32
GPIO0_59	IO	General Purpose Input/Output	W30
GPIO0_60	IO	General Purpose Input/Output	F30
GPIO0_61	IO	General Purpose Input/Output	E30
GPIO0_62	IO	General Purpose Input/Output	F29
GPIO0_63	IO	General Purpose Input/Output	F28
GPIO0_64	IO	General Purpose Input/Output	D33
GPIO0_65	IO	General Purpose Input/Output	E32

5.3.13.2 WKUP Domain

Table 5-34. WKUP_GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_GPIO0_0	IO	General Purpose Input/Output	E15
WKUP_GPIO0_1	IO	General Purpose Input/Output	D16
WKUP_GPIO0_2	IO	General Purpose Input/Output	D18
WKUP_GPIO0_3	IO	General Purpose Input/Output	D19
WKUP_GPIO0_4	IO	General Purpose Input/Output	E16
WKUP_GPIO0_5	IO	General Purpose Input/Output	D20
WKUP_GPIO0_6	IO	General Purpose Input/Output	B15
WKUP_GPIO0_7	IO	General Purpose Input/Output	B17
WKUP_GPIO0_8	IO	General Purpose Input/Output	B19
WKUP_GPIO0_9	IO	General Purpose Input/Output	A15
WKUP_GPIO0_10	IO	General Purpose Input/Output	B18
WKUP_GPIO0_11	IO	General Purpose Input/Output	B21
WKUP_GPIO0_12	IO	General Purpose Input/Output	D17
WKUP_GPIO0_13	IO	General Purpose Input/Output	D21
WKUP_GPIO0_14	IO	General Purpose Input/Output	D15
WKUP_GPIO0_15	IO	General Purpose Input/Output	C16
WKUP_GPIO0_16	IO	General Purpose Input/Output	D8
WKUP_GPIO0_17	IO	General Purpose Input/Output	D10
WKUP_GPIO0_18	IO	General Purpose Input/Output	C10
WKUP_GPIO0_19	IO	General Purpose Input/Output	E10
WKUP_GPIO0_20	IO	General Purpose Input/Output	F9
WKUP_GPIO0_21	IO	General Purpose Input/Output	E9
WKUP_GPIO0_22	IO	General Purpose Input/Output	D11
WKUP_GPIO0_23	IO	General Purpose Input/Output	D9

Table 5-34. WKUP_GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_GPIO0_24	IO	General Purpose Input/Output	C9
WKUP_GPIO0_25	IO	General Purpose Input/Output	C7
WKUP_GPIO0_26	IO	General Purpose Input/Output	C8
WKUP_GPIO0_27	IO	General Purpose Input/Output	F12
WKUP_GPIO0_28	IO	General Purpose Input/Output	F11
WKUP_GPIO0_29	IO	General Purpose Input/Output	F10
WKUP_GPIO0_30	IO	General Purpose Input/Output	E11
WKUP_GPIO0_31	IO	General Purpose Input/Output	B7
WKUP_GPIO0_32	IO	General Purpose Input/Output	B10
WKUP_GPIO0_33	IO	General Purpose Input/Output	B9
WKUP_GPIO0_34	IO	General Purpose Input/Output	B8
WKUP_GPIO0_35	IO	General Purpose Input/Output	B11
WKUP_GPIO0_36	IO	General Purpose Input/Output	A11
WKUP_GPIO0_37	IO	General Purpose Input/Output	A10
WKUP_GPIO0_38	IO	General Purpose Input/Output	A8
WKUP_GPIO0_39	IO	General Purpose Input/Output	A9
WKUP_GPIO0_40	IO	General Purpose Input/Output	B14
WKUP_GPIO0_41	IO	General Purpose Input/Output	C12
WKUP_GPIO0_42	IO	General Purpose Input/Output	A12
WKUP_GPIO0_43	IO	General Purpose Input/Output	B12
WKUP_GPIO0_44	IO	General Purpose Input/Output	A13
WKUP_GPIO0_45	IO	General Purpose Input/Output	B13
WKUP_GPIO0_46	IO	General Purpose Input/Output	A14
WKUP_GPIO0_47	IO	General Purpose Input/Output	C14
WKUP_GPIO0_48	IO	General Purpose Input/Output	D13
WKUP_GPIO0_49	IO	General Purpose Input/Output	A20
WKUP_GPIO0_50	IO	General Purpose Input/Output	D14
WKUP_GPIO0_51	IO	General Purpose Input/Output	E13
WKUP_GPIO0_52	IO	General Purpose Input/Output	F13
WKUP_GPIO0_53	IO	General Purpose Input/Output	E12
WKUP_GPIO0_54	IO	General Purpose Input/Output	F15
WKUP_GPIO0_55	IO	General Purpose Input/Output	E18
WKUP_GPIO0_56	IO	General Purpose Input/Output	A19
WKUP_GPIO0_57	IO	General Purpose Input/Output	B20
WKUP_GPIO0_58	IO	General Purpose Input/Output	C20
WKUP_GPIO0_59	IO	General Purpose Input/Output	C19
WKUP_GPIO0_60	IO	General Purpose Input/Output	E22
WKUP_GPIO0_61	IO	General Purpose Input/Output	C18
WKUP_GPIO0_62	IO	General Purpose Input/Output	D12
WKUP_GPIO0_63	IO	General Purpose Input/Output	A16
WKUP_GPIO0_64	IO	General Purpose Input/Output	D23
WKUP_GPIO0_65	IO	General Purpose Input/Output	D22
WKUP_GPIO0_66	IO	General Purpose Input/Output	A17
WKUP_GPIO0_67	IO	General Purpose Input/Output	A18

Table 5-34. WKUP_GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_GPIO0_68	IO	General Purpose Input/Output	E21
WKUP_GPIO0_69	IO	General Purpose Input/Output	E14
WKUP_GPIO0_70	IO	General Purpose Input/Output	E19
WKUP_GPIO0_71	I	General Purpose Input/Output	E26
WKUP_GPIO0_72	I	General Purpose Input/Output	F25
WKUP_GPIO0_73	I	General Purpose Input/Output	F23
WKUP_GPIO0_74	I	General Purpose Input/Output	A28
WKUP_GPIO0_75	I	General Purpose Input/Output	E24
WKUP_GPIO0_76	I	General Purpose Input/Output	D27
WKUP_GPIO0_77	I	General Purpose Input/Output	A26
WKUP_GPIO0_78	I	General Purpose Input/Output	B27
WKUP_GPIO0_79	I	General Purpose Input/Output	C32
WKUP_GPIO0_80	I	General Purpose Input/Output	B33
WKUP_GPIO0_81	I	General Purpose Input/Output	B31
WKUP_GPIO0_82	I	General Purpose Input/Output	B29
WKUP_GPIO0_83	I	General Purpose Input/Output	D31
WKUP_GPIO0_84	I	General Purpose Input/Output	A32
WKUP_GPIO0_85	I	General Purpose Input/Output	A30
WKUP_GPIO0_86	I	General Purpose Input/Output	C28
WKUP_GPIO0_87	IO	General Purpose Input/Output	A21
WKUP_GPIO0_88	IO	General Purpose Input/Output	B16

5.3.14 GPMC

5.3.14.1 MAIN Domain

Table 5-35. GPMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	H33
GPMC0_CLK	IO	GPMC clock	P29
GPMC0_CLKOUT	O	GPMC clock generated for external synchronization	K33
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	F33, G28
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	J32
GPMC0_WEn	O	GPMC Write Enable (active low)	T30
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	H33
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	M31
GPMC0_A1	OZ	GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	N30
GPMC0_A2	OZ	GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	T33
GPMC0_A3	OZ	GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	L32
GPMC0_A4	OZ	GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	P30

Table 5-35. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPMC0_A5	OZ	GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	M32
GPMC0_A6	OZ	GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	L33
GPMC0_A7	OZ	GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	U31
GPMC0_A8	OZ	GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	M33
GPMC0_A9	OZ	GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	P31
GPMC0_A10	OZ	GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	N31
GPMC0_A11	OZ	GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	U32
GPMC0_A12	OZ	GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	N32
GPMC0_A13	OZ	GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	H29
GPMC0_A14	OZ	GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	M31, P32
GPMC0_A15	OZ	GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	U30
GPMC0_A16	OZ	GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	G30
GPMC0_A17	OZ	GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R31
GPMC0_A18	OZ	GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R29
GPMC0_A19	OZ	GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R30
GPMC0_A20	OZ	GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R33
GPMC0_A21	OZ	GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T32
GPMC0_A22	OZ	GPMC Address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T31
GPMC0_A23	OZ	GPMC Address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T29
GPMC0_A24	OZ	GPMC Address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P29
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	J30
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	K31
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	F32
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	H32

Table 5-35. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	E33
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	L31
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	J33
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	G33
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	G31
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	J31
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	P33
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	G32
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	K32
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	R32
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	N33
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	G29
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	H31
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	F31
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	H30
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	F33
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	M31, P32
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	T29
GPMC0_WAIT0	I	GPMC External Indication of Wait	G28
GPMC0_WAIT1	I	GPMC External Indication of Wait	U30
GPMC0_WAIT2	I	GPMC External Indication of Wait	T31
GPMC0_WAIT3	I	GPMC External Indication of Wait	H29

5.3.15 HYPERBUS

5.3.15.1 MCU Domain

Table 5-36. MCU_HYPERBUS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_HYPERBUS0_CK	O	Hyperbus Differential Clock (positive)	D8
MCU_HYPERBUS0_CKn	O	Hyperbus Differential Clock (negative)	D10
MCU_HYPERBUS0_INTn	I	Hyperbus Interrupt (active low)	B9, E11
MCU_HYPERBUS0_RESETn	O	Hyperbus Reset (active low) Output	F11
MCU_HYPERBUS0_RESETOn	I	Hyperbus Reset Status Indicator (active low) from Hyperbus Memory	B10, F10
MCU_HYPERBUS0_RWDS	IO	Hyperbus Read-Write Data Strobe	C10
MCU_HYPERBUS0_WPn	O	Hyperbus Write Protect (Not in use)	A9, E11, F10
MCU_HYPERBUS0_CSn0	O	Hyperbus Chip Select 0	F12
MCU_HYPERBUS0_CSn1	O	Hyperbus Chip Select 1	A9, F10
MCU_HYPERBUS0_DQ0	IO	Hyperbus Data 0	E10
MCU_HYPERBUS0_DQ1	IO	Hyperbus Data 1	F9
MCU_HYPERBUS0_DQ2	IO	Hyperbus Data 2	E9
MCU_HYPERBUS0_DQ3	IO	Hyperbus Data 3	D11
MCU_HYPERBUS0_DQ4	IO	Hyperbus Data 4	D9
MCU_HYPERBUS0_DQ5	IO	Hyperbus Data 5	C9
MCU_HYPERBUS0_DQ6	IO	Hyperbus Data 6	C7
MCU_HYPERBUS0_DQ7	IO	Hyperbus Data 7	C8

5.3.16 I2C

5.3.16.1 MAIN Domain

Table 5-37. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C0_SCL	IOD	I2C Clock	AA30
I2C0_SDA	IOD	I2C Data	Y30

Table 5-38. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C1_SCL	IOD	I2C Clock	L31, M33, R31
I2C1_SDA	IOD	I2C Data	G30, J33, P31

Table 5-39. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C2_SCL	IOD	I2C Clock	G31, V31
I2C2_SDA	IOD	I2C Data	J31, V30

Table 5-40. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C3_SCL	IOD	I2C Clock	F30, N33

Table 5-40. I2C3 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C3_SDA	IOD	I2C Data	E30, R32

Table 5-41. I2C4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C4_SCL	IOD	I2C Clock	F28, H30, R33
I2C4_SDA	IOD	I2C Data	F29, J32, T32

Table 5-42. I2C5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C5_SCL	IOD	I2C Clock	G28, R29
I2C5_SDA	IOD	I2C Data	F33, R30

Table 5-43. I2C6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
I2C6_SCL	IOD	I2C Clock	E32, W30
I2C6_SDA	IOD	I2C Data	AA32, D33

5.3.16.2 MCU Domain

Table 5-44. MCU_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_I2C0_SCL	IOD	I2C Clock	D22
MCU_I2C0_SDA	IOD	I2C Data	A21

Table 5-45. MCU_I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_I2C1_SCL	IOD	I2C Clock	B15, B19
MCU_I2C1_SDA	IOD	I2C Data	A15, B17

5.3.16.3 WKUP Domain

Table 5-46. WKUP_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_I2C0_SCL	IOD	I2C Clock	A16
WKUP_I2C0_SDA	IOD	I2C Data	D23

5.3.17 I3C

5.3.17.1 MCU Domain

Table 5-47. MCU_I3C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_I3C0_SCL	IO	I3C Clock	B19
MCU_I3C0_SDA	IO	I3C Data	A15

Table 5-47. MCU_I3C0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_I3C0_SDAPULLEN	OD	I3C Data Pull Enable	B16, B21

5.3.18 MCAN

5.3.18.1 MAIN Domain

Table 5-48. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN0_RX	I	MCAN Receive Data	G29
MCAN0_TX	O	MCAN Transmit Data	N33

Table 5-49. MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN1_RX	I	MCAN Receive Data	H31, J33
MCAN1_TX	O	MCAN Transmit Data	G33

Table 5-50. MCAN2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN2_RX	I	MCAN Receive Data	F33
MCAN2_TX	O	MCAN Transmit Data	G28

Table 5-51. MCAN3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN3_RX	I	MCAN Receive Data	J32
MCAN3_TX	O	MCAN Transmit Data	F31

Table 5-52. MCAN4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN4_RX	I	MCAN Receive Data	K33
MCAN4_TX	O	MCAN Transmit Data	H30

Table 5-53. MCAN5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN5_RX	I	MCAN Receive Data	K31, N30
MCAN5_TX	O	MCAN Transmit Data	J30, M31

Table 5-54. MCAN6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN6_RX	I	MCAN Receive Data	H32, L32
MCAN6_TX	O	MCAN Transmit Data	F32, T33

Table 5-55. MCAN7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN7_RX	I	MCAN Receive Data	G31, M32
MCAN7_TX	O	MCAN Transmit Data	H33, P30

Table 5-56. MCAN8 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN8_RX	I	MCAN Receive Data	P33, U31
MCAN8_TX	O	MCAN Transmit Data	J31, L33

Table 5-57. MCAN9 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN9_RX	I	MCAN Receive Data	K32, P31
MCAN9_TX	O	MCAN Transmit Data	G32, M33

Table 5-58. MCAN10 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN10_RX	I	MCAN Receive Data	U32
MCAN10_TX	O	MCAN Transmit Data	N31

Table 5-59. MCAN11 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN11_RX	I	MCAN Receive Data	H29
MCAN11_TX	O	MCAN Transmit Data	N32

Table 5-60. MCAN12 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN12_RX	I	MCAN Receive Data	E33, T29
MCAN12_TX	O	MCAN Transmit Data	L31, P29

Table 5-61. MCAN13 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN13_RX	I	MCAN Receive Data	T32, W30
MCAN13_TX	O	MCAN Transmit Data	AA32, T31

Table 5-62. MCAN14 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN14_RX	I	MCAN Receive Data	R30, Y32
MCAN14_TX	O	MCAN Transmit Data	R33, Y33

Table 5-63. MCAN15 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN15_RX	I	MCAN Receive Data	E32, R31
MCAN15_TX	O	MCAN Transmit Data	D33, R29

Table 5-64. MCAN16 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN16_RX	I	MCAN Receive Data	U30
MCAN16_TX	O	MCAN Transmit Data	G30

Table 5-65. MCAN17 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCAN17_RX	I	MCAN Receive Data	R32, T30
MCAN17_TX	O	MCAN Transmit Data	P32

5.3.18.2 MCU Domain

Table 5-66. MCU_MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_MCAN0_RX	I	MCAN Receive Data	C18
MCU_MCAN0_TX	O	MCAN Transmit Data	E22

Table 5-67. MCU_MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_MCAN1_RX	I	MCAN Receive Data	D20
MCU_MCAN1_TX	O	MCAN Transmit Data	E16

5.3.19 MCASP

5.3.19.1 MAIN Domain

Table 5-68. MCASP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP0_ACLKR	IO	MCASP Receive Bit Clock	U31
MCASP0_ACLKX	IO	MCASP Transmit Bit Clock	J30
MCASP0_AFSR	IO	MCASP Receive Frame Sync	M33
MCASP0_AFSX	IO	MCASP Transmit Frame Sync	K31
MCASP0_AXR0	IO	MCASP Serial Data (Input/Output)	F32
MCASP0_AXR1	IO	MCASP Serial Data (Input/Output)	H32
MCASP0_AXR2	IO	MCASP Serial Data (Input/Output)	H33
MCASP0_AXR3	IO	MCASP Serial Data (Input/Output)	F31
MCASP0_AXR4	IO	MCASP Serial Data (Input/Output)	J32
MCASP0_AXR5	IO	MCASP Serial Data (Input/Output)	H30
MCASP0_AXR6	IO	MCASP Serial Data (Input/Output)	K33
MCASP0_AXR7	IO	MCASP Serial Data (Input/Output)	M31
MCASP0_AXR8	IO	MCASP Serial Data (Input/Output)	N30

Table 5-68. MCASP0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP0_AXR9	IO	MCASP Serial Data (Input/Output)	T33
MCASP0_AXR10	IO	MCASP Serial Data (Input/Output)	L32
MCASP0_AXR11	IO	MCASP Serial Data (Input/Output)	P30
MCASP0_AXR12	IO	MCASP Serial Data (Input/Output)	M32
MCASP0_AXR13	IO	MCASP Serial Data (Input/Output)	L33
MCASP0_AXR14	IO	MCASP Serial Data (Input/Output)	U31
MCASP0_AXR15	IO	MCASP Serial Data (Input/Output)	M33

Table 5-69. MCASP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP1_ACLKR	IO	MCASP Receive Bit Clock	H30
MCASP1_ACLKX	IO	MCASP Transmit Bit Clock	U32
MCASP1_AFSR	IO	MCASP Receive Frame Sync	K33
MCASP1_AFSX	IO	MCASP Transmit Frame Sync	N32
MCASP1_AXR0	IO	MCASP Serial Data (Input/Output)	H29
MCASP1_AXR1	IO	MCASP Serial Data (Input/Output)	G31
MCASP1_AXR2	IO	MCASP Serial Data (Input/Output)	J31
MCASP1_AXR3	IO	MCASP Serial Data (Input/Output)	P31
MCASP1_AXR4	IO	MCASP Serial Data (Input/Output)	N31

Table 5-70. MCASP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP2_ACLKR	IO	MCASP Receive Bit Clock	M32
MCASP2_ACLKX	IO	MCASP Transmit Bit Clock	P33
MCASP2_AFSR	IO	MCASP Receive Frame Sync	L33
MCASP2_AFSX	IO	MCASP Transmit Frame Sync	G32
MCASP2_AXR0	IO	MCASP Serial Data (Input/Output)	K32
MCASP2_AXR1	IO	MCASP Serial Data (Input/Output)	R32
MCASP2_AXR2	IO	MCASP Serial Data (Input/Output)	N33
MCASP2_AXR3	IO	MCASP Serial Data (Input/Output)	G28
MCASP2_AXR4	IO	MCASP Serial Data (Input/Output)	U31

Table 5-71. MCASP3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP3_ACLKR	IO	MCASP Receive Bit Clock	Y33
MCASP3_ACLKX	IO	MCASP Transmit Bit Clock	Y33
MCASP3_AFSR	IO	MCASP Receive Frame Sync	Y32
MCASP3_AFSX	IO	MCASP Transmit Frame Sync	Y32
MCASP3_AXR0	IO	MCASP Serial Data (Input/Output)	V31
MCASP3_AXR1	IO	MCASP Serial Data (Input/Output)	V30
MCASP3_AXR2	IO	MCASP Serial Data (Input/Output)	W31

Table 5-72. MCASP4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCASP4_ACLKR	IO	MCASP Receive Bit Clock	M31
MCASP4_ACLKX	IO	MCASP Transmit Bit Clock	J33
MCASP4_AFSR	IO	MCASP Receive Frame Sync	N30
MCASP4_AFSX	IO	MCASP Transmit Frame Sync	G33
MCASP4_AXR0	IO	MCASP Serial Data (Input/Output)	T30
MCASP4_AXR1	IO	MCASP Serial Data (Input/Output)	G29
MCASP4_AXR2	IO	MCASP Serial Data (Input/Output)	L31
MCASP4_AXR3	IO	MCASP Serial Data (Input/Output)	H31
MCASP4_AXR4	IO	MCASPI Serial Data (Input/Output)	T33

5.3.20 MCSPI

5.3.20.1 MAIN Domain

Table 5-73. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI0_CLK	IO	SPI Clock	V31
SPI0_CS0	IO	SPI Chip Select 0	Y33
SPI0_CS1	IO	SPI Chip Select 1	Y32
SPI0_CS2	IO	SPI Chip Select 2	R31
SPI0_CS3	IO	SPI Chip Select 3	U30
SPI0_D0	IO	SPI Data 0	V30
SPI0_D1	IO	SPI Data 1	W31

Table 5-74. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI1_CLK	IO	SPI Clock	D33
SPI1_CS0	IO	SPI Chip Select 0	F30
SPI1_CS1	IO	SPI Chip Select 1	E30
SPI1_CS2	IO	SPI Chip Select 2	F29
SPI1_CS3	IO	SPI Chip Select 3	G30
SPI1_D0	IO	SPI Data 0	F28
SPI1_D1	IO	SPI Data 1	E32

Table 5-75. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI2_CLK	IO	SPI Clock	M32
SPI2_CS0	IO	SPI Chip Select 0	L33
SPI2_CS1	IO	SPI Chip Select 1	P30
SPI2_CS2	IO	SPI Chip Select 2	F32
SPI2_CS3	IO	SPI Chip Select 3	H32
SPI2_D0	IO	SPI Data 0	U31
SPI2_D1	IO	SPI Data 1	M33

Table 5-76. MCSPI3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI3_CLK	IO	SPI Clock	H29
SPI3_CS0	IO	SPI Chip Select 0	N32
SPI3_CS1	IO	SPI Chip Select 1	F31
SPI3_CS2	IO	SPI Chip Select 2	K33
SPI3_CS3	IO	SPI Chip Select 3	U32
SPI3_D0	IO	SPI Data 0	G31
SPI3_D1	IO	SPI Data 1	J31

Table 5-77. MCSPI5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI5_CLK	IO	SPI Clock	F31
SPI5_CS0	IO	SPI Chip Select 0	G29
SPI5_CS1	IO	SPI Chip Select 1	N33
SPI5_CS2	IO	SPI Chip Select 2	P33
SPI5_CS3	IO	SPI Chip Select 3	G32
SPI5_D0	IO	SPI Data 0	H31
SPI5_D1	IO	SPI Data 1	K33

Table 5-78. MCSPI6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI6_CLK	IO	SPI Clock	E33
SPI6_CS0	IO	SPI Chip Select 0	T30
SPI6_CS1	IO	SPI Chip Select 1	F33
SPI6_CS2	IO	SPI Chip Select 2	J32
SPI6_CS3	IO	SPI Chip Select 3	H30
SPI6_D0	IO	SPI Data 0	L31
SPI6_D1	IO	SPI Data 1	G28

Table 5-79. MCSPI7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SPI7_CLK	IO	SPI Clock	F32
SPI7_CS0	IO	SPI Chip Select 0	H32
SPI7_CS1	IO	SPI Chip Select 1	P33
SPI7_CS2	IO	SPI Chip Select 2	G32
SPI7_CS3	IO	SPI Chip Select 3	P32
SPI7_D0	IO	SPI Data 0	G29
SPI7_D1	IO	SPI Data 1	F31

5.3.20.2 MCU Domain

Table 5-80. MCU_MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_SPI0_CLK	IO	SPI Clock	F15

Table 5-80. MCU_MCSPI0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_SPI0_CS0	IO	SPI Chip Select 0	E19
MCU_SPI0_CS1	IO	SPI Chip Select 1	A10, D17
MCU_SPI0_CS2	IO	SPI Chip Select 2	A9, D15
MCU_SPI0_CS3	IO	SPI Chip Select 3	E16
MCU_SPI0_D0	IO	SPI Data 0	E18
MCU_SPI0_D1	IO	SPI Data 1	E14

Table 5-81. MCU_MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_SPI1_CLK	IO	SPI Clock	E15
MCU_SPI1_CS0	IO	SPI Chip Select 0	D19
MCU_SPI1_CS1	IO	SPI Chip Select 1	B11, D21
MCU_SPI1_CS2	IO	SPI Chip Select 2	A11, C16
MCU_SPI1_CS3	IO	SPI Chip Select 3	D20
MCU_SPI1_D0	IO	SPI Data 0	D16
MCU_SPI1_D1	IO	SPI Data 1	D18

5.3.21 MDIO

5.3.21.1 MAIN Domain

Table 5-82. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MDIO0_MDC	O	MDIO Clock	H29
MDIO0_MDIO	IO	MDIO Data	N32

Table 5-83. MDIO1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MDIO1_MDC	O	MDIO Clock	G32
MDIO1_MDIO	IO	MDIO Data	K32

5.3.21.2 MCU Domain

Table 5-84. MCU_MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_MDIO0_MDC	O	MDIO Clock	E12
MCU_MDIO0_MDIO	IO	MDIO Data	F13

5.3.22 MMC

5.3.22.1 MAIN Domain

Table 5-85. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MMC0_CALPAD (1)	A	MMC/SD/SDIO Calibration Resistor	AH2
MMC0_CLK	O	MMC/SD/SDIO Clock	AJ2

Table 5-85. MMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MMC0_CMD	IO	MMC/SD/SDIO Command	AL2
MMC0_DS	IO	MMC Data Strobe	AJ1
MMC0_DAT0	IO	MMC/SD/SDIO Data	AM1
MMC0_DAT1	IO	MMC/SD/SDIO Data	AK3
MMC0_DAT2	IO	MMC/SD/SDIO Data	AL1
MMC0_DAT3	IO	MMC/SD/SDIO Data	AK1
MMC0_DAT4	IO	MMC/SD/SDIO Data	AJ3
MMC0_DAT5	IO	MMC/SD/SDIO Data	AH3
MMC0_DAT6	IO	MMC/SD/SDIO Data	AJ4
MMC0_DAT7	IO	MMC/SD/SDIO Data	AK2

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Table 5-86. MMC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MMC1_CLK (2)	IO	MMC/SD/SDIO Clock	D33
MMC1_CMD	IO	MMC/SD/SDIO Command	E32
MMC1_SDCD (1)	I	SD Card Detect	AA32
MMC1_SDWP	I	SD Write Protect	W30
MMC1_DAT0	IO	MMC/SD/SDIO Data	F28
MMC1_DAT1	IO	MMC/SD/SDIO Data	F29
MMC1_DAT2	IO	MMC/SD/SDIO Data	E30
MMC1_DAT3	IO	MMC/SD/SDIO Data	F30

(1) For ROM boot from MMC1 interface to work properly, the MMC1_SDCD pin should be pulled low externally with a resistor to indicate an SD Card/Memory device is present.
(2) For MMC1_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG64 register should be set to 0x1 because of retiming purposes.

5.3.23 OSPI

5.3.23.1 MCU Domain

Table 5-87. MCU_OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_OSPI0_CLK	O	OSPI Clock	D8
MCU_OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	C10
MCU_OSPI0_ECC_FAIL	I	OSPI ECC Status	B9, E11
MCU_OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	D10
MCU_OSPI0_CSn0	O	OSPI Chip Select 0 (active low)	F12
MCU_OSPI0_CSn1	O	OSPI Chip Select 1 (active low)	F11
MCU_OSPI0_CSn2	O	OSPI Chip Select 2 (active low)	B10, F10
MCU_OSPI0_CSn3	O	OSPI Chip Select 3 (active low)	B9, E11
MCU_OSPI0_D0	IO	OSPI Data 0	E10
MCU_OSPI0_D1	IO	OSPI Data 1	F9
MCU_OSPI0_D2	IO	OSPI Data 2	E9
MCU_OSPI0_D3	IO	OSPI Data 3	D11
MCU_OSPI0_D4	IO	OSPI Data 4	D9

Table 5-87. MCU_OSPI0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_OSPI0_D5	IO	OSPI Data 5	C9
MCU_OSPI0_D6	IO	OSPI Data 6	C7
MCU_OSPI0_D7	IO	OSPI Data 7	C8
MCU_OSPI0_RESET_OUT0	O	OSPI Reset	B10, F10
MCU_OSPI0_RESET_OUT1	O	OSPI Reset	A9, E11

Table 5-88. MCU_OSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_OSPI1_CLK	O	OSPI Clock	B7
MCU_OSPI1_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	B9
MCU_OSPI1_LBCLKO	IO	OSPI Loopback Clock Output	B10
MCU_OSPI1_CSn0	O	OSPI Chip Select 0 (active low)	A8
MCU_OSPI1_CSn1	O	OSPI Chip Select 1 (active low)	A9
MCU_OSPI1_D0	IO	OSPI Data 0	B8
MCU_OSPI1_D1	IO	OSPI Data 1	B11
MCU_OSPI1_D2	IO	OSPI Data 2	A11
MCU_OSPI1_D3	IO	OSPI Data 3	A10

5.3.24 PCIE

5.3.24.1 MAIN Domain

Table 5-89. PCIE Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
PCIE0_CLKREQn	IO	PCIE Clock Request Signal	U32
PCIE1_CLKREQn	IO	PCIE Clock Request Signal	AA32, F30
PCIE2_CLKREQn (1)	IO	PCIE Clock Request Signal	D33, P31
PCIE3_CLKREQn (1)	IO	PCIE Clock Request Signal	E32, N31
PCIE0_RXN0	I	SERDES_PCIE Differential Receive Data (negative)	AL10
PCIE0_RXN1	I	SERDES_PCIE Differential Receive Data (negative)	AN8
PCIE0_RXN2	I	SERDES_PCIE Differential Receive Data (negative)	AM6
PCIE0_RXN3	I	SERDES_PCIE Differential Receive Data (negative)	AL7
PCIE0_RXP0	I	SERDES_PCIE Differential Receive Data (positive)	AL11
PCIE0_RXP1	I	SERDES_PCIE Differential Receive Data (positive)	AN9
PCIE0_RXP2	I	SERDES_PCIE Differential Receive Data (positive)	AM7
PCIE0_RXP3	I	SERDES_PCIE Differential Receive Data (positive)	AL8
PCIE0_TXN0	O	SERDES_PCIE Differential Transmit Data (negative)	AK11
PCIE0_TXN1	O	SERDES_PCIE Differential Transmit Data (negative)	AM9
PCIE0_TXN2	O	SERDES_PCIE Differential Transmit Data (negative)	AK8
PCIE0_TXN3	O	SERDES_PCIE Differential Transmit Data (positive)	AJ9
PCIE0_TXP0	O	SERDES_PCIE Differential Transmit Data (positive)	AK12
PCIE0_TXP1	O	SERDES_PCIE Differential Transmit Data (positive)	AM10
PCIE0_TXP2	O	SERDES_PCIE Differential Transmit Data (positive)	AK9
PCIE0_TXP3	O	SERDES_PCIE Differential Transmit Data (positive)	AJ10
PCIE1_RXN0 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AM12

Table 5-89. PCIE Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
PCIE1_RXN1 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AL13
PCIE1_RXN2 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AN15
PCIE1_RXN3 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AL17
PCIE1_RXP0 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AM13
PCIE1_RXP1 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AL14
PCIE1_RXP2 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AN14
PCIE1_RXP3 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AL16
PCIE1_TXN0 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AN11
PCIE1_TXN1 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AJ19
PCIE1_TXN2 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AM16
PCIE1_TXN3 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AK18
PCIE1_TXP0 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AN12
PCIE1_TXP1 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AJ18
PCIE1_TXP2 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AM15
PCIE1_TXP3 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AK17
PCIE2_RXN0 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AM6
PCIE2_RXN1 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AL7
PCIE2_RXP0 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AM7
PCIE2_RXP1 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AL8
PCIE2_TXN0 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AK8
PCIE2_TXN1 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AJ9
PCIE2_TXP0 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AK9
PCIE2_TXP1 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AJ10
PCIE3_RXN0 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AN15
PCIE3_RXN1 (1)	I	SERDES_PCIE Differential Receive Data (negative)	AL17
PCIE3_RXP0 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AN14
PCIE3_RXP1 (1)	I	SERDES_PCIE Differential Receive Data (positive)	AL16
PCIE3_TXN0 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AM16
PCIE3_TXN1 (1)	O	SERDES_PCIE Differential Transmit Data (negative)	AK18
PCIE3_TXP0 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AM15
PCIE3_TXP1 (1)	O	SERDES_PCIE Differential Transmit Data (positive)	AK17
PCIE_REFCLK0_N_OUT	O	SERDES_PCIE Reference Clock Negative	AJ13
PCIE_REFCLK0_P_OUT	O	SERDES_PCIE Reference Clock Positive	AJ12
PCIE_REFCLK1_N_OUT	O	SERDES_PCIE Reference Clock Out Negative	AH14
PCIE_REFCLK1_P_OUT	O	SERDES_PCIE Reference Clock Out Positive	AH13
PCIE_REFCLK2_N_OUT (1)	O	SERDES_PCIE Reference Clock Out Negative	AH11
PCIE_REFCLK2_P_OUT (1)	O	SERDES_PCIE Reference Clock Out Positive	AH10
PCIE_REFCLK3_N_OUT (1)	O	SERDES_PCIE Reference Clock Out Negative	AJ16
PCIE_REFCLK3_P_OUT (1)	O	SERDES_PCIE Reference Clock Out Positive	AJ15

(1) This signal is not supported on **TDA4VPE4**, **TDA4APE4** devices. Please refer to Device Comparison and Pin Attributes table for the complete list of supported IP and signals.

5.3.25 SERDES

5.3.25.1 MAIN Domain

Table 5-90. SERDES0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SERDES0_REFCLK_N (1)	IO	Serdes Reference Clock Input/Output (negative)	AK15
SERDES0_REFCLK_P (1)	IO	Serdes Reference Clock Input/Output (positive)	AK14
SERDES0_REXT (1) (2)	I	External Calibration Resistor	AG7

(1) This signal is not supported on **TDA4VPE4**, **TDA4APE4** devices. Please refer to Device Comparison and Pin Attributes table for the complete list of supported IP and signals.
(2) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Table 5-91. SERDES1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SERDES1_REFCLK_N	IO	Serdes Reference Clock Input/Output (negative)	AN5
SERDES1_REFCLK_P	IO	Serdes Reference Clock Input/Output (positive)	AN6
SERDES1_REXT (1)	I	External Calibration Resistor	AH9

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Table 5-92. SERDES4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SERDES4_REFCLK_N	IO	Serdes Reference Clock Input/Output (negative)	AK21
SERDES4_REFCLK_P	IO	Serdes Reference Clock Input/Output (positive)	AK20
SERDES4_REXT (1)	IO	External Calibration Resistor	AH23

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

5.3.26 SGMII

5.3.26.1 MAIN Domain

Table 5-93. CPSW9X0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SGMII1_RXN0 (1)	I	SGMII Receive (negative)	AM6
SGMII1_RXP0 (1)	I	SGMIi Receive (positive)	AM7
SGMII1_TXN0 (1)	O	SGMII Transmit (negative)	AK8
SGMII1_TXP0 (1)	O	SGMII Transmit (positive)	AK9
SGMII2_RXN0 (1)	I	SGMII Receive (negative)	AL7
SGMII2_RXP0 (1)	I	SGMIi Receive (positive)	AL8
SGMII2_TXN0 (1)	O	SGMII Transmit (negative)	AJ9
SGMII2_TXP0 (1)	O	SGMII Transmit (positive)	AJ10
SGMII3_RXN0	I	SGMII Receive (negative)	AL10
SGMII3_RXP0	I	SGMIi Receive (positive)	AL11
SGMII3_TXN0	O	SGMII Transmit (negative)	AK11
SGMII3_TXP0	O	SGMII Transmit (positive)	AK12
SGMII4_RXN0	I	SGMII Receive (negative)	AN8
SGMII4_RXP0	I	SGMIi Receive (positive)	AN9
SGMII4_TXN0	O	SGMII Transmit (negative)	AM9
SGMII4_TXP0	O	SGMII Transmit (positive)	AM10

Table 5-93. CPSW9X0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SGMII5_RXN0 (1)	I	SGMII Receive (negative)	AN17
SGMII5_RXP0 (1)	I	SGMIi Receive (positive)	AN18
SGMII5_TXN0 (1)	O	SGMII Transmit (negative)	AJ21
SGMII5_TXP0 (1)	O	SGMII Transmit (positive)	AJ22
SGMII6_RXN0 (1)	I	SGMII Receive (negative)	AL19
SGMII6_RXP0 (1)	I	SGMIi Receive (positive)	AL20
SGMII6_TXN0 (1)	O	SGMII Transmit (negative)	AM18
SGMII6_TXP0 (1)	O	SGMII Transmit (positive)	AM19
SGMII7_RXN0 (1)	I	SGMII Receive (negative)	AK23
SGMII7_RXP0 (1)	I	SGMIi Receive (positive)	AK24
SGMII7_TXN0 (1)	O	SGMII Transmit (negative)	AN20
SGMII7_TXP0 (1)	O	SGMII Transmit (positive)	AN21
SGMII8_RXN0 (1)	I	SGMII Receive (negative)	AM21
SGMII8_RXP0 (1)	I	SGMIi Receive (positive)	AM22
SGMII8_TXN0 (1)	O	SGMII Transmit (negative)	AL22
SGMII8_TXP0 (1)	O	SGMII Transmit (positive)	AL23

(1) This signal is not supported on **TDA4VPE4**, **TDA4APE4** devices. Please refer to Device Comparison and Pin Attributes table for the complete list of supported IP and signals.

5.3.27 UART

5.3.27.1 MAIN Domain

Table 5-94. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	F30, G31
UART0_DCDn	I	UART Data Carrier Detect (active low)	T29
UART0_DSRn	I	UART Data Set Ready (active low)	T31
UART0_DTRn	O	UART Data Terminal Ready (active low)	T32
UART0_RIn	I	UART Ring Indicator	R33
UART0_RTSn	O	UART Request to Send (active low)	D33, J31, Y32
UART0_RXD	I	UART Receive Data	N32
UART0_TXD	O	UART Transmit Data	H29

Table 5-95. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	K32, V31
UART1_RTSn	O	UART Request to Send (active low)	R32, V30
UART1_RXD	I	UART Receive Data	P33
UART1_TXD	O	UART Transmit Data	G32

Table 5-96. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	L31
UART2_RTSn	O	UART Request to Send (active low)	J33

Table 5-96. UART2 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART2_RXD	I	UART Receive Data	F29, N33, V30
UART2_TXD	O	UART Transmit Data	F28, G29, W31

Table 5-97. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	F31
UART3_RTSn	O	UART Request to Send (active low)	H31
UART3_RXD	I	UART Receive Data	AA32, G28, L31
UART3_TXD	O	UART Transmit Data	F33, J33, W30

Table 5-98. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	D33, H33, T33
UART4_RTSn	O	UART Request to Send (active low)	E32, L32, U32
UART4_RXD	I	UART Receive Data	F29, F32, M31, N31
UART4_TXD	O	UART Transmit Data	F28, H32, N30, T31

Table 5-99. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	F29, L33
UART5_RTSn	O	UART Request to Send (active low)	F28, U31
UART5_RXD	I	UART Receive Data	F30, P30, T29
UART5_TXD	O	UART Transmit Data	E30, M32, P29

Table 5-100. UART6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	N33
UART6_RTSn	O	UART Request to Send (active low)	G29
UART6_RXD	I	UART Receive Data	E33, K32, R33
UART6_TXD	O	UART Transmit Data	G33, R32, T32

Table 5-101. UART7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART7_CTSn	I	UART Clear to Send (active low)	F29
UART7_RTSn	O	UART Request to Send (active low)	F28
UART7_RXD	I	UART Receive Data	F30, L33, P32
UART7_TXD	O	UART Transmit Data	E30, T30, U31

Table 5-102. UART8 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART8_CTSn	I	UART Clear to Send (active low)	F32

Table 5-102. UART8 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART8_RTSn	O	UART Request to Send (active low)	H32
UART8_RXD	I	UART Receive Data	D33, J30, M33, Y32
UART8_TXD	O	UART Transmit Data	E32, K31, P31, V31

Table 5-103. UART9 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UART9_CTSn	I	UART Clear to Send (active low)	E33, H33
UART9_RTSn	O	UART Request to Send (active low)	T30, U32
UART9_RXD	I	UART Receive Data	G31, R29
UART9_TXD	O	UART Transmit Data	J31, R30

5.3.27.2 MCU Domain

Table 5-104. MCU_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_UART0_CTSn	I	UART Clear to Send (active low)	A10, D15
MCU_UART0_RTSn	O	UART Request to Send (active low)	A9, C16
MCU_UART0_RXD	I	UART Receive Data	B11, B21, D21
MCU_UART0_TXD	O	UART Transmit Data	A11, B18, D17

5.3.27.3 WKUP Domain

Table 5-105. WKUP_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_UART0_CTSn	I	UART Clear to Send (active low)	B15
WKUP_UART0_RTSn	O	UART Request to Send (active low)	B17
WKUP_UART0_RXD	I	UART Receive Data	C20
WKUP_UART0_TXD	O	UART Transmit Data	C19

5.3.28 UFS

5.3.28.1 MAIN Domain

Table 5-106. UFS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
UFS0_REF_CLK	O	UFS Reference Clock	AJ5
UFS0_RSTn	O	UFS Reset	AJ7
UFS0_RX_DN0	I	UFS Receive Data (negative)	AK5
UFS0_RX_DN1	I	UFS Receive Data (negative)	AL4
UFS0_RX_DP0	I	UFS Receive Data (positive)	AK6
UFS0_RX_DP1	I	UFS Receive Data (positive)	AL5
UFS0_TX_DN0	O	UFS Transmit Data (negative)	AN2
UFS0_TX_DN1	O	UFS Transmit Data (negative)	AM3
UFS0_TX_DP0	O	UFS Transmit Data (positive)	AN3
UFS0_TX_DP1	O	UFS Transmit Data (positive)	AM4

5.3.29 USB

5.3.29.1 MAIN Domain

Table 5-107. USB0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	AH16
USB0_DP	IO	USB 2.0 Differential Data (positive)	AH17
USB0_DRVVBUS	O	USB VBUS Control Output (active high)	M31, P32, W30
USB0_ID	A	USB 2.0 Dual-Role Device Role Select	AH20
USB0_RCALIB (2)	A	Pin to connect to calibration resistor	AH22
USB0_VBUS (3)	A	USB Level-shifted VBUS Detector	AG19
USB0_SSRX1N (1)	I	SERDES_USB Differential Receive Data (negative)	AK23, AN15
USB0_SSRX1P (1)	I	SERDES_USB Differential Receive Data (positive)	AK24, AN14
USB0_SSRX2N (1)	I	SERDES_USB Differential Receive Data (negative)	AL17, AM21
USB0_SSRX2P (1)	I	SERDES_USB Differential Receive Data (positive)	AL16, AM22
USB0_SSTX1N (1)	O	SERDES_USB Differential Transmit Data (negative)	AM16, AN20
USB0_SSTX1P (1)	O	SERDES_USB Differential Transmit Data (positive)	AM15, AN21
USB0_SSTX2N (1)	O	SERDES_USB Differential Transmit Data (negative)	AK18, AL22
USB0_SSTX2P (1)	O	SERDES_USB Differential Transmit Data (positive)	AK17, AL23

(1) Only a subset of the pin multiplexing options are supported for this signal on **TDA4VPE4**, **TDA4APE4** devices. Please refer to Device Comparison and Pin Attributes table for the complete list of supported IP and signals.
(2) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused
(3) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see *USB VBUS Design Guidelines*.

5.3.30 Emulation and Debug

5.3.30.1 MAIN Domain

Table 5-108. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
EMU0	IO	Emulation Control 0	F19
EMU1	IO	Emulation Control 1	E17
TCK	I	JTAG Test Clock Input	F21
TDI	I	JTAG Test Data Input	V33
TDO	OZ	JTAG Test Data Output	W33
TMS	I	JTAG Test Mode Select Input	V32
TRSTn	I	JTAG Reset	F17

Table 5-109. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
TRC_CLK	O	Trace Clock	J33, P29
TRC_CTL	O	Trace Control	G33, T29
TRC_DATA0	O	Trace Data 0	T30, T31
TRC_DATA1	O	Trace Data 1	L31, T32
TRC_DATA2	O	Trace Data 2	E33, R33
TRC_DATA3	O	Trace Data 3	G28, R30
TRC_DATA4	O	Trace Data 4	P33
TRC_DATA5	O	Trace Data 5	H31

Table 5-109. Trace Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
TRC_DATA6	O	Trace Data 6	J31
TRC_DATA7	O	Trace Data 7	F31
TRC_DATA8	O	Trace Data 8	G31
TRC_DATA9	O	Trace Data 9	G32
TRC_DATA10	O	Trace Data 10	H33
TRC_DATA11	O	Trace Data 11	N33
TRC_DATA12	O	Trace Data 12	H32
TRC_DATA13	O	Trace Data 13	R32
TRC_DATA14	O	Trace Data 14	F32
TRC_DATA15	O	Trace Data 15	K32
TRC_DATA16	O	Trace Data 16	G29
TRC_DATA17	O	Trace Data 17	F33
TRC_DATA18	O	Trace Data 18	J32
TRC_DATA19	O	Trace Data 19	H30
TRC_DATA20	O	Trace Data 20	K33
TRC_DATA21	O	Trace Data 21	R29
TRC_DATA22	O	Trace Data 22	R31
TRC_DATA23	O	Trace Data 23	G30
TRC_DATA24	O	Trace Data 24	U30
TRC_DATA25	O	Trace Data 25	P32

5.3.31 System and Miscellaneous

5.3.31.1 Boot Mode Configuration

Table 5-110. Sysboot Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
BOOTMODE00	I	Bootmode Pin 0	E10
BOOTMODE01	I	Bootmode Pin 1	F9
BOOTMODE02	I	Bootmode Pin 2	D9
BOOTMODE03	I	Bootmode Pin 3	C9
BOOTMODE04	I	Bootmode Pin 4	A19
BOOTMODE05	I	Bootmode Pin 5	B20
BOOTMODE06	I	Bootmode Pin 6	A17
BOOTMODE07	I	Bootmode Pin 7	A18
MCU_BOOTMODE00	I	MCU Bootmode Pin 0	F15
MCU_BOOTMODE01	I	MCU Bootmode Pin 1	E18
MCU_BOOTMODE02	I	MCU Bootmode Pin 2	E14
MCU_BOOTMODE03	I	MCU Bootmode Pin 3	E15
MCU_BOOTMODE04	I	MCU Bootmode Pin 4	D16
MCU_BOOTMODE05	I	MCU Bootmode Pin 5	D18
MCU_BOOTMODE06	I	MCU Bootmode Pin 6	D15
MCU_BOOTMODE07	I	MCU Bootmode Pin 7	C16
MCU_BOOTMODE08	I	MCU Bootmode Pin 8	D17
MCU_BOOTMODE09	I	MCU Bootmode Pin 9	D21

5.3.31.2 Clock

Table 5-111. Clock0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
WKUP_LF_CLKIN	I	Low Frequency (32.768 KHz) Oscillator Input	A18
WKUP_OSC0_XI	I	High Frequency Oscillator Input	A24
WKUP_OSC0_XO	O	High Frequency Oscillator Output	B25

Table 5-112. Clock1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
OSC1_XI	I	High Frequency Oscillator Input	B23
OSC1_XO	O	High Frequency Oscillator Output	A22

5.3.31.3 EFUSE

Table 5-113. EFUSE Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VPP_CORE	PWR	Programming Voltage for MAIN Domain Efuses	V29
VPP_MCU	PWR	Programming Voltage for MCU Domain Efuses	F26

5.3.31.4 System

Table 5-114. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
AUDIO_EXT_REFCLK0	IO	External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP	T30
AUDIO_EXT_REFCLK1	IO	External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP	F33
EXTINTn	I	External Interrupt	Y29
EXT_REFCLK1	I	External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL)	J33
GPMC0_FCLK_MUX	O	GPMC functional clock output selected through a mux logic	K33
OBSCLK1	O	Observation clock output for test and debug purposes only	H32
PMIC_POWER_EN1	O	Power enable output for MAIN Domain supplies	B16
PMIC_WAKE0	O	PMIC WakeUp (active low)	T30
PMIC_WAKE1	O	PMIC WakeUp (active low)	A20
PORz	I	SoC PORz Reset Signal	D24
RESETSTATz	O	Main Domain Warm Reset status output	W32
RESET_REQz	I	Main Domain external Warm Reset request input	G20
SOC_SAFETY_ERRORn	IO	Error signal output from Main Domain ESM	Y31
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0	L31
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1	J33
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2	H29
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3	P33

Table 5-114. System Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
SYSCLKOUT0	O	SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only	AA32

Table 5-115. MCU System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
MCU_CLKOUT0	OZ	Reference clock output for Ethernet PHYs (50MHz or 25MHz)	B21
MCU_EXT_REFCLK0	I	External system clock input	A20, B18
MCU_OBSCLK0	O	Observation clock output for test and debug purposes only	B21
MCU_PORz	I	MCU Domain Cold Reset	C24
MCU_RESETSTATz	O	MCU Domain Warm Reset status output	E21
MCU_RESETz	I	MCU Domain Warm Reset	E20
MCU_SAFETY_ERRORn	IO	Error signal output from MCU Domain ESM	C22
MCU_SYSCLKOUT0	O	MCU Domain system clock output for test and debug purposes only	B18

5.3.31.5 VMON

Table 5-116. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VMON1_ER_VSYS	A	Voltage Monitor, fixed 0.45V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	G26
VMON2_IR_VCPU	A	Must be externally connected directly to VDD_CPU	L25
VMON3_IR_VEXT1P8	A	General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.	K30
VMON4_IR_VEXT1P8	A	General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.	M26
VMON5_IR_VEXT3P3	A	General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor divider.	M29

5.3.32 Power

Table 5-117. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
CAP_VDDS0 (1)	CAP	External Capacitor Connection	T27
CAP_VDDS0_MCU (1)	CAP	External Capacitor Connection	J25
CAP_VDDS1_MCU (1)	CAP	External Capacitor Connection	J23
CAP_VDDS2 (1)	CAP	External Capacitor Connection	P27
CAP_VDDS2_MCU (1)	CAP	External Capacitor Connection	J24
CAP_VDDS5 (1)	CAP	External Capacitor Connection	M27
VDDAR_CORE	PWR	Core RAM Supply	AA22, AD13, AD16, AD19, AE26, AE9, P23, Y25
VDDAR_CPU	PWR	CPU RAM Supply	AA14, AA16, AA18, AC10, K19, L21, P13, R18, U12, U19, V17, V9, Y11

Table 5-117. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VDDAR_MCU	PWR	MCU RAM Supply	K25, L22
VDDA_0P8_DSITX	PWR	Analog Supply for DSITX	AG22
VDDA_0P8_DSITX_C	PWR	DSITX Clock Supply	AG23
VDDA_0P8_UFS	PWR	UFS 0.8V Supply	AF9
VDDA_0P8_USB	PWR	USB 0.8V Supply	AG17
VDDA_0P8_CSIRX2	PWR	Analog Supply for CSIRX	AG26
VDDA_0P8_CSIRX0_1	PWR	Analog Supply for CSIRX	AG24
VDDA_0P8_DLL_MMC0	PWR	MMC DLL Analog Supply	AD7
VDDA_0P8_PLL_DDR0	PWR	DDR de-skew PLL Analog Supply	P8
VDDA_0P8_PLL_DDR1	PWR	DDR de-skew PLL Analog Supply	J11
VDDA_0P8_SERDES4	PWR	SERDES 0.8V Supply	AG15, AG16
VDDA_0P8_SERDES0_1	PWR	SERDES 0.8V Supply	AF12, AG10, AG13
VDDA_0P8_SERDES_C4	PWR	SERDES 0.8V Clock Supply	AE15, AF16
VDDA_0P8_SERDES_C0_1	PWR	SERDES 0.8V Clock Supply	AF10, AF13
VDDA_1P8_DSITX	PWR	Analog Supply for DSITX	AF22, AF23
VDDA_1P8_UFS	PWR	UFS 1.8V Supply	AG8
VDDA_1P8_USB	PWR	USB 1.8V Supply	AH19
VDDA_1P8_CSIRX2	PWR	Analog Supply for CSIRX	AF27, AG27
VDDA_1P8_CSIRX0_1	PWR	Analog Supply for CSIRX	AF25, AF26
VDDA_1P8_SERDES4	PWR	SERDES 1.8V Supply	AF15
VDDA_1P8_SERDES0_1	PWR	SERDES 1.8V Supply	AG11, AG12
VDDA_1P8_SERDES2_4	PWR	SERDES 1.8V Supply	AG21
VDDA_3P3_USB	PWR	USB 3.3V Supply	AF17
VDDA_ADC0	PWR	ADC0 Analog Supply	J28
VDDA_ADC1	PWR	ADC1 Analog Supply	K28
VDDA_MCU_PLLGRP0	PWR	Analog Supply for MCU PLL Group 0	K26
VDDA_MCU_TEMP	PWR	Analog Supply for MCU temperature sensor	K24
VDDA_OSC1	PWR	HFOSC1 Supply	L27
VDDA_PLLGRP0	PWR	Analog Supply for MAIN PLL Group 0	W25
VDDA_PLLGRP1	PWR	Analog Supply for MAIN PLL Group 1	V25
VDDA_PLLGRP2	PWR	Analog Supply for MAIN PLL Group 2	AE11
VDDA_PLLGRP5	PWR	Analog Supply for MAIN PLL Group 5	T12
VDDA_PLLGRP6	PWR	Analog Supply for MAIN PLL Group 6	N19
VDDA_PLLGRP7	PWR	Analog Supply for MAIN PLL Group 7	M10
VDDA_PLLGRP8	PWR	Analog Supply for MAIN PLL Group 8	K13
VDDA_PLLGRP9	PWR	Analog Supply for MAIN PLL Group 9	V24
VDDA_PLLGRP10	PWR	Analog Supply for MAIN PLL Group 10	AD20
VDDA_PLLGRP12	PWR	Analog Supply for MAIN PLL Group 12	W21
VDDA_PLLGRP13	PWR	Analog Supply for MAIN PLL Group 13	Y24
VDDA_POR_WKUP	PWR	WKUP domain Analog Supply	L26
VDDA_TEMP0	PWR	Analog Supply for temperature sensor 0	V26
VDDA_TEMP1	PWR	Analog Supply for temperature sensor 1	K10
VDDA_TEMP2	PWR	Analog Supply for temperature sensor 2	U21
VDDA_TEMP3	PWR	Analog Supply for temperature sensor 3	AC11

Table 5-117. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VDDA_TEMP4	PWR	Analog Supply for temperature sensor 4	AB16
VDDA_WKUP	PWR	Oscillator Supply for WKUP domain	J27
VDDSHV0	PWR	IO Power Supply	T28
VDDSHV0_MCU	PWR	IO Power Supply	H27
VDDSHV1_MCU	PWR	IO Power Supply	G22, H23
VDDSHV2	PWR	IO Power Supply	N28, P28
VDDSHV2_MCU	PWR	IO Power Supply	G24, H25
VDDSHV5	PWR	IO Power Supply	N27
VDDS_DDR	PWR	DDR PHY IO Supply	A2, AH1, G10, G12, G14, G16, G18, H11, H13, H15, H17, H9, J10, J14, J16, J8, K7, L8, M7, P7, R8
VDDS_DDR_C0	PWR	IO Power Supply for DDR Clock	N8
VDDS_DDR_C1	PWR	IO Power Supply for DDR Clock	J12
VDDS_MMC0	PWR	MMC0 PHY IO Supply	AE8, AF7
VDD_CORE	PWR	MAIN domain core Supply	AA24, AA26, AA28, AB23, AB25, AB27, AC22, AC24, AC26, AC28, AD11, AD15, AD17, AD21, AD23, AD25, AD27, AE10, AE12, AE14, AE16, AE18, AE20, AE22, AE24, AE28, AF19, K11, K15, K17, K9, L10, L12, L14, L16, M11, M13, M15, M17, M9, N10, N12, N14, N16, N22, N24, N26, P11, P25, P9, R10, R22, R24, R26, T23, T25, U22, U24, U26, U28, V23, V27, W22, W24, W26, W28, Y23, Y27
VDD_CPU	PWR	CPU core Supply	AA10, AA12, AA20, AA8, AB11, AB13, AB15, AB17, AB19, AB21, AB9, AC12, AC14, AC16, AC18, AC20, AC8, AD9, H19, H21, J18, J20, L18, L20, M19, N18, N20, P15, P17, P19, P21, R12, R20, T11, T17, T19, T21, T9, U10, U18, U20, U8, V11, V19, V21, W10, W12, W18, W20, W8, Y17, Y19, Y21, Y9
VDD_MCU	PWR	MCU core Supply	J22, K21, K23, L24, M21, M23, M25
VDD_MCU_WAKE1	PWR	Core Supply for MCU daisy chain	J26
VDD_WAKE0	PWR	Core Supply for MAIN domain daisy chain	R27

Table 5-117. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VSS	GND	Ground	A1, A23, A25, A27, A29, A31, A4, A7, AA11, AA13, AA15, AA17, AA19, AA2, AA21, AA23, AA25, AA27, AA29, AA31, AA33, AA5, AA9, AB1, AB10, AB12, AB14, AB18, AB20, AB22, AB24, AB26, AB28, AB30, AB32, AB4, AB8, AC13, AC15, AC17, AC19, AC2, AC21, AC23, AC25, AC27, AC5, AC9, AD10, AD12, AD14, AD18, AD22, AD24, AD26, AD28, AD29, AD3, AD31, AD33, AD6, AD8, AE1, AE13, AE17, AE19, AE21, AE23, AE25, AE27, AE30, AE32, AE4, AE7, AF11, AF14, AF18, AF2, AF20, AF21, AF24, AF28, AF5, AF8, AG14, AG18, AG20, AG25, AG28, AG29, AG3, AG31, AG33, AG6, AG9, AH12, AH15, AH18, AH21, AH24, AH26, AH28, AH30, AH5, AJ11, AJ14, AJ17, AJ20, AJ23, AJ26, AJ29, AJ32, AJ6, AJ8, AK10, AK13, AK16, AK19, AK22, AK25, AK28, AK31, AK4, AK7, AL12, AL15, AL18, AL21, AL24, AL27, AL3, AL30, AL33, AL6, AL9, AM11, AM14, AM17, AM2, AM20, AM23, AM26, AM29, AM32, AM33, AM5, AM8, AN1, AN10, AN13, AN16

Table 5-117. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AND PIN [4]
VSS (continued)	GND	Ground	AN19, AN22, AN25, AN28, AN31, AN32, AN4, AN7, B22, B24, B26, B28, B3, B30, B32, B6, C11, C13, C15, C17, C2, C21, C23, C25, C27, C29, C31, C33, C5, D1, D26, D28, D30, D32, D4, D7, E23, E25, E27, E29, E3, E31, E6, E8, F14, F16, F18, F2, F20, F22, F24, F5, F7, G1, G11, G13, G15, G17, G19, G21, G23, G25, G27, G4, G9, H10, H12, H14, H16, H18, H2, H20, H22, H24, H26, H28, H5, H8, J1, J13, J15, J17, J19, J21, J6, J7, J9, K12, K14, K16, K18, K2, K20, K22, K27, K29, K5, K8, L11, L13, L15, L17, L19, L23, L3, L6, L7, L9, M1, M12, M14, M16, M18, M20, M22, M24, M28, M4, M8, N11, N13, N15, N17, N2, N21, N23, N25, N29, N5, N7, N9, P10, P12, P14, P16, P18, P20, P22, P24, P26, P3, R11, R17, R19, R21, R23, R25, R28, R3, R6
VSS (continued)	GND	Ground	R9, T10, T18, T2, T20, T22, T24, T26, T5, T8, U1, U11, U17, U23, U25, U27, U29, U33, U4, U7, U9, V10, V12, V18, V20, V22, V28, V3, V6, V8, W11, W17, W19, W2, W23, W27, W29, W5, W9, Y1, Y10, Y12, Y18, Y20, Y22, Y26, Y28, Y6, Y8

(1) This pin must always be connected via a 1-µF ±10% capacitor to VSS.

5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

Note

All power balls must be supplied with the voltages specified in the Recommended Operating Conditions section, unless otherwise specified in Signal Descriptions.

Note

For additional clarification, "leave unconnected" or "no connect" (NC) means no signal traces can be connected to these device ball number.

Table 5-118 shows the connectivity requirements for specific signals by ball name and ball number.

Table 5-118. Connectivity Requirements

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENT
B23	OSC1_XI	Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low-level, if unused.
A24	WKUP_OSC0_XI	
F17	TRSTN	
R1	DDR0_DQS0P	
V1	DDR0_DQS1P	
AD1	DDR0_DQS2P	
AG1	DDR0_DQS3P	
B1	DDR1_DQS0P	
E1	DDR1_DQS1P	
L1	DDR1_DQS2P	
P1	DDR1_DQS3P	
AC7	DDR0_RET	
G8	DDR1_RET	
G26	VMON1_ER_VSYS	
L25	VMON2_IR_VCPU	
K30	VMON3_IR_VEXT1P8	
M26	VMON4_IR_VEXT1P8	
M29	VMON5_IR_VEXT3P3	
E26	MCU_ADC0_AIN0	Each of these balls can be connected to VSS through a separate external pull resistor or can be connected directly to VSS to ensure these balls are held to a valid logic low-level, if unused.
F25	MCU_ADC0_AIN1	
F23	MCU_ADC0_AIN2	
A28	MCU_ADC0_AIN3	
E24	MCU_ADC0_AIN4	
D27	MCU_ADC0_AIN5	
A26	MCU_ADC0_AIN6	
B27	MCU_ADC0_AIN7	
C32	MCU_ADC1_AIN0	
B33	MCU_ADC1_AIN1	
B31	MCU_ADC1_AIN2	
B29	MCU_ADC1_AIN3	
D31	MCU_ADC1_AIN4	
A32	MCU_ADC1_AIN5	
A30	MCU_ADC1_AIN6	
C28	MCU_ADC1_AIN7	

Table 5-118. Connectivity Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENT
AG7	SERDES0_REXT	Each of these balls must be connected to VSS through appropriate external pull resistor to ensure these balls are held to a valid logic low level, if unused. Refer to Signal Descriptions footnote for appropriate value of pull-resistor for each signal.
AH9	SERDES1_REXT	
AH23	SERDES4_REXT	
AH31	CSI0_RXRCALIB	
AJ33	CSI1_RXRCALIB	
AH29	CSI2_RXRCALIB	
R7	DDR0_CAL0	
F8	DDR1_CAL0	
AH25	DSI0_TXRCALIB	
AH27	DSI1_TXRCALIB	
AH22	USB0_RCALIB	
E20	MCU_RESETZ	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level, if unused.
C24	MCU_PORZ	
D24	PORZ	
G20	RESET_REQZ	
F21	TCK	
V32	TMS	
A21	MCU_I2C0_SDA	
D22	MCU_I2C0_SCL	
A16	WKUP_I2C0_SCL	
D23	WKUP_I2C0_SDA	
AA30	I2C0_SCL	
Y30	I2C0_SDA	
Y29	EXTINTn	
V33	TDI	
W33	TDO	
F19	EMU0	
E17	EMU1	
T1	DDR0_DQS0N	
W1	DDR0_DQS1N	
AC1	DDR0_DQS2N	
AF1	DDR0_DQS3N	
C1	DDR1_DQS0N	
F1	DDR1_DQS1N	
K1	DDR1_DQS2N	
N1	DDR1_DQS3N	
D25	MCU_ADC0_REFP	If the MCU_ADCn interface is not used, these signals should be connected to the same power supply as the VDDA_ADCn supply input.
C30	MCU_ADC1_REFP	
C26	MCU_ADC0_REFN	If the MCU_ADCn interface is not used, these signals should be connected to VSS.
D29	MCU_ADC1_REFN	
F26	VPP_MCU	Each of these balls must be left unconnected, if unused.
V29	VPP_CORE	
AH2	MMC0_CALPAD	

Table 5-118. Connectivity Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENT
	DDR0_*	DDRSS0 and DDRSS1 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces.
	DDR1_*	

Table 5-119 shows the specific connection requirements for the RESERVED ball numbers on the device.

Note

For additional clarification, "left unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

Table 5-119. Reserved Balls Specific Connection Requirements

BALL NUMBERS	CONNECTION REQUIREMENTS
E28 / F27 / J29 / L28 / L29 / L30 / M30 / AH4 / AH7 / AH8	RESERVED. These balls must be left unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

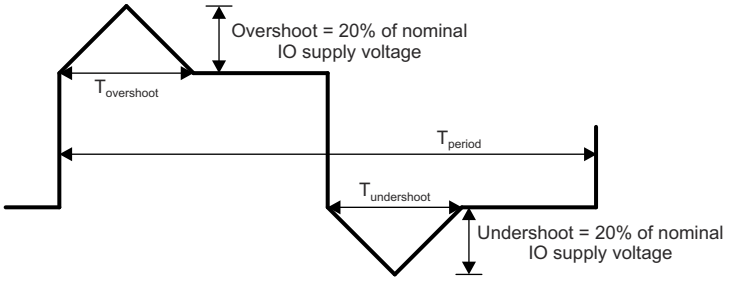
over operating free–air temperature range (unless otherwise noted)(1) (2)

PARAMETER			MIN	MAX	UNIT
VDD_*(3)	Core supplies		–0.3	1.05	V
VDDAR_*(3)	RAM supplies		–0.3	1.05	V
VDDA_0P8_*(3)	Analog supplies for 0.8V domains		–0.3	1.05	V
VDDA_1P8_*(3)	Analog supplies for 1.8 V PHY domains		–0.3	2.2	V
VDDA_3P3_USB	Analog supply for 3.3V USB domain		–0.3	3.8	V
VDDA_*(3)	Analog supply for 1.8V PLL and other domains		–0.3	2.2	V
VDDS_DDR_*(3)	DDR inteface power supplies		–0.3	1.2	V
VDDS_MMC0	MMC0 IO supply		–0.3	2.2	V
VDDSHV*(3)	Dual Voltage LVCMOS IO supplies	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VPP_CORE VPP MCU	Supply voltage range for EFUSE domains		–0.3	1.89	V
USB0_VBUS(9)	Voltage range for USB VBUS comparator input		–0.3	3.6	V
Steady State Max. Voltage at all fail–safe IO pins		I2C0_SCL, I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn	–0.3	3.8	V
		MCU_PORz, PORz	–0.3	3.8	V
Steady State Max. Voltage at all other IO pins(4)		VMON1_ER_VSYS(8), VMON3_IR_VEXT1P8, VMON4_IR_VEXT1P8	–0.3	2.2	V
		VMON2_IR_VCPU	–0.3	1.05	V
		VMON5_IR_VEXT3P3	–0.3	3.8	V
		All other IO pins	–0.3	IO supply voltage + 0.3	V
Transient Overshoot and Undershoot specification at IO pin		20% of IO supply voltage for up to 20% of signal period Figure 6-1 (see *IO Transient Voltage Ranges*)		0.2 × VDD(7)	V
Latch–up Performance, Class II (125°C)(5)		I–Test	–100	100	mA
		Over–Voltage (OV) Test	NA	1.5 × VDD(7)	V
T_{STG} (6)		Storage temperature	–55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to their associated VSS or VSSA_x, unless otherwise noted.
(3) **VDD_* includes:** VDD_CORE, VDD_CPU, VDD_MCU, VDD_MCU_WAKE1, VDD_WAKE0
VDDAR_* includes: VDDAR_CORE, VDDAR_CPU, VDDAR_MCU
VDDA_0P8_* includes: VDDA_0P8_CSIRX0_1, VDDA_0P8_CSIRX2, VDDA_0P8_DLL_MMC0, VDDA_0P8_DSITX, VDDA_0P8_DSITX_C, VDDA_0P8_PLL_DDR0, VDDA_0P8_PLL_DDR1, VDDA_0P8_PLL_DDR2, VDDA_0P8_PLL_DDR3, VDDA_0P8_SERDES_C0_1, VDDA_0P8_SERDES_C2, VDDA_0P8_SERDES_C4, VDDA_0P8_SERDES0_1, VDDA_0P8_SERDES2, VDDA_0P8_SERDES4, VDDA_0P8_UFS, VDDA_0P8_USB
VDDA_1P8_* includes: VDDA_1P8_CSIRX0_1, VDDA_1P8_CSIRX2, VDDA_1P8_DSITX, VDDA_1P8_SERDES0_1, VDDA_1P8_SERDES2, VDDA_1P8_SERDES2_4, VDDA_1P8_SERDES4, VDDA_1P8_UFS, VDDA_1P8_USB
VDDA_* includes: VDDA_ADC0, VDDA_ADC1, VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_OSC1, VDDA_PLLGRP0, VDDA_PLLGRP1, VDDA_PLLGRP10, VDDA_PLLGRP12, VDDA_PLLGRP13, VDDA_PLLGRP2, VDDA_PLLGRP5, VDDA_PLLGRP6, VDDA_PLLGRP7, VDDA_PLLGRP8, VDDA_PLLGRP9, VDDA_POR_WKUP, VDDA_TEMP0, VDDA_TEMP1, VDDA_TEMP2, VDDA_TEMP3, VDDA_TEMP4, VDDA_WKUP
VDDS_DDR_* includes: VDDS_DDR, VDDS_DDR_C0, VDDS_DDR_C1, VDDS_DDR_C2, VDDS_DDR_C3
VDDSHV* includes: VDDSHV0, VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2, VDDSHV2_MCU, VDDSHV5
(4) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp–up and ramp–down sequences.
(5) For current pulse injection:
Pins stressed per JEDEC JESD78E (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.
For overvoltage performance:
Supplies stressed per JEDEC JESD78E (Class II) and passed specified voltage injection.
(6) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
(7) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(8) The VMON_ER_VSYS pin provides a way to monitor the system power supply. For more information, see System Power Supply Monitor Design Guidelines using VMON/POK.
(9) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see the USB VBUS Design Guidelines.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, DDR_FS_RESETn, and NMIn are the only fail–safe IO terminals. All other IO terminals are not fail–safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in Absolute Maximum Ratings.



A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

Figure 6-1. IO Transient Voltage Ranges

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±250	
			Corner pins (A1, AJ29)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Power-On-Hour (POH) Limits

IP(1) (2) (3)	VOLTAGE DOMAIN	VOLTAGE (V) (MAX)	FREQUENCY (MHz) (MAX)	Tj(°C)	POH
All	100%	All	All Supported OPPs	Automotive -40°C to 125°C (4)	20000
All	100%	All	All Supported OPPs	Extended -40°C to 105°C	100000
All	100%	All	All Supported OPPs	Commercial 0°C to 90°C	100000

(1) The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures
(3) POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.
(4) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, 10%@125°C.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDD_CORE	Boot/Active voltage for MAIN domain core supply		0.76(1)	0.8	0.84(1)	V
VDD_MCU	Boot/Active voltage for MCUSS core supply		0.76(1)	0.8	0.89(1)	V
VDD_CPU	Boot voltage for CPU core supply, applied at cold power up event		0.76(1)	0.8	0.84(1)	V
	Active voltage for CPU core supply, after AVS mode enabled in software		AVS(3)–5%(1)	AVS(3)	AVS(3)+5%(1)	V
VDD_CPU AVS Range	AVS valid voltage range for VDD_CPU		0.6		0.9	V
VDDAR_*(5)	RAM supplis		0.81	0.85	0.89	V
VDDA_0P8_*(5)	Analog supplies for 0.8V domains		0.76	0.8	0.84	V
VDDA_1P8_*(5)	Analog supplies for 1.8V PHY domains		1.71	1.8	1.89	V
VDDA_3P3_USB(5)	Analog supply for 3.3V USB domain		3.14	3.3	3.46	V
VDDA_*(5)	Analog supply for 1.8V PLL and other domains		1.71	1.8	1.89	V
VDDA_*	Peak to Peak Noise for all VDDA inputs				25	mV
VDDS_DDR_*(5)	DDR inteface power supply		1.06	1.1	1.15	V
VDDS_MMC0	MMC0 IO supply		1.71	1.8	1.89	V
VPP_*(5)	eFuse ROM programming supply		See (6)	See (6)	See (6)	V
VDDSHV*(5)	Dual Voltage LVCMOS IO supplies	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
USB0_VBUS	Voltage range for USB VBUS comparator input		0	See (4)	3.46	V
USB0_ID	Voltage range for the USB ID input			See (2)		V
VSS	Ground			0		V
T_J	Operating junction temperature range	Automotive	–40		125	°C
		Extended	-40		105	°C
		Commercial	0		90	°C

(1) For all VDD* supply inputs, the voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth. This is required for all supply inputs, but special care should be given to the VDD_CORE, VDD_MCU, and VDD_CPU domains which have higher transient current demand compared to other rails.
(2) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

(3) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM_DEVINFO_VDn. For information about VTM_DEVINFO_VDn Registers address, please refer to Voltage and Thermal Manager section in the device TRM. The power supply should be adjustable over the ranges shown in the VDD_CPU AVS Range entry.

(4) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see USB VBUS Design Guidelines.

(5) **VDD_* includes:** VDD_CORE, VDD_CPU, VDD_MCU, VDD_MCU_WAKE1, VDD_WAKE0
VDDAR_* includes: VDDAR_CORE, VDDAR_CPU, VDDAR_MCU
VDDA_0P8_* includes: VDDA_0P8_CSIRX0_1, VDDA_0P8_CSIRX2, VDDA_0P8_DLL_MMC0, VDDA_0P8_DSITX, VDDA_0P8_DSITX_C, VDDA_0P8_PLL_DDR0, VDDA_0P8_PLL_DDR1, VDDA_0P8_PLL_DDR2, VDDA_0P8_PLL_DDR3, VDDA_0P8_SERDES_C0_1, VDDA_0P8_SERDES_C2, VDDA_0P8_SERDES_C4, VDDA_0P8_SERDES0_1, VDDA_0P8_SERDES2, VDDA_0P8_SERDES4, VDDA_0P8_UFS, VDDA_0P8_USB
VDDA_1P8_* includes: VDDA_1P8_CSIRX0_1, VDDA_1P8_CSIRX2, VDDA_1P8_DSITX, VDDA_1P8_SERDES0_1, VDDA_1P8_SERDES2, VDDA_1P8_SERDES2_4, VDDA_1P8_SERDES4, VDDA_1P8_UFS, VDDA_1P8_USB
VDDA_* includes: VDDA_ADC0, VDDA_ADC1, VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_OSC1, VDDA_PLLGRP0, VDDA_PLLGRP1, VDDA_PLLGRP10, VDDA_PLLGRP12, VDDA_PLLGRP13, VDDA_PLLGRP2, VDDA_PLLGRP5, VDDA_PLLGRP6, VDDA_PLLGRP7, VDDA_PLLGRP8, VDDA_PLLGRP9, VDDA_POR_WKUP, VDDA_TEMP0, VDDA_TEMP1, VDDA_TEMP2, VDDA_TEMP3, VDDA_TEMP4, VDDA_WKUP
VDDS_DDR_* includes: VDDS_DDR, VDDS_DDR_C0, VDDS_DDR_C1, VDDS_DDR_C2, VDDS_DDR_C3
VDDSHV* includes: VDDSHV0, VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2, VDDSHV2_MCU, VDDSHV5
VPP_* includes:VPP_CORE, VPP_MCU

(6) See the Recommended Operating Conditions for OTP eFuse Programming table for VPP supply voltages based on eFuse usage.

6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

Table 6-1 describes the maximum supported frequency per speed grade for the device.

Table 6-1. Speed Grade Maximum Frequency

DEVICE	MAXIMUM FREQUENCY (MHz)										
	A72SS0	C71SS0	R5FSS0/1	MCU_ R5SS0	GPU	CBASS0	VPAC	DMPAC	VENCDEC	DMSC	LPDDR4
TDA4xxxT	2000	1000	1000	1000	800	500	720(1)	520(1)	600 (960 or 480MP/s)(3)	333	4266 MT/s(2)

(1) Max VPAC and DMPAC speeds not available concurrently due to PLL sharing (max combinations are 720/480 and 650/520 for VPAC/DMPAC, respectively.

(2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the Jacinto 7 DDR Board Design and Layout Guidelines for details.

(3) Refer to Device Comparison table to determine specific part numbers that include 1x VENCDEC module (480 MP/s) or 2x VENCDEC module (960 MP/s)

6.6 Electrical Characteristics

Note

The interfaces or signals described in Section 6.6.1 through Section 6.6.8 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

6.6.1 I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
V_{IL}	Input low-level threshold				0.3 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.3 × VDDSHV(1)	V
V_{IH}	Input high-level threshold		0.7 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV(1)			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDDSHV(1)			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
V_{OL}	Output low-level voltage				0.2 × VDDSHV(1)	V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	6			mA
3.3-V MODE						
V_{IL}	Input low-level threshold				0.3 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.25 × VDDSHV(1)	V
V_{IH}	Input high-level threshold		0.7 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV(1)			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDDSHV(1)			mV
I_{IN}	Input Leakage Current	V_I = 3.3 V or 0 V			±10	µA
V_{OL}	Output low-level voltage				0.4	V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	6			mA

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the Pin Attributes, POWER column.

6.6.2 Fail-Safe Reset (FS Reset) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low-level threshold				0.3 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.3 × VDDSHV(1)	V

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high-level threshold		0.7 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV(1)			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

6.6.3 HFOSC/LFOSC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH FREQUENCY OSCILLATOR						
V_{IH}	Input high-level threshold		0.65 × VDDSHV(1)			V
V_{IL}	Input low-level threshold				0.35 × VDDSHV(1)	V
V_{HYS}	Input Hysteresis Voltage			49		mV
LOW FREQUENCY OSCILLATOR						
V_{IH}	Input high-level threshold		0.65 × VDDA_WKUP (1)			V
V_{IL}	Input low-level threshold				0.35 × VDDA_WKUP (1)	V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV

(1) VDDSHV stands for corresponding power supply. For WKUP_OSC0, the corresponding power supply is VDDA_WKUP. For OSC1_XI, the corresponding power supply is VDDS_OSC1.

6.6.4 eMMCPHY Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IL}	Input low-level threshold				0.35 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.20	V
V_{IH}	Input high-level threshold		0.65 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		1.4			V
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
I_{OZ}	Tri-state Output Leakage Current	V_O = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	20	25	kΩ
R_{PD}	Pull-down Resistor		15	20	25	kΩ
V_{OL}	Output low-level voltage				0.30	V
V_{OH}	Output high-level voltage		VDDSHV - 0.30(1)			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	2			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	2			mA

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SR_I	Input Slew Rate		5E +8			V/s

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column..

6.6.5 SDIO Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
1.8-V MODE						
V_{IL}	Input low-level threshold				0.58	V
V_{ILSS}	Input low-level threshold steady state				0.58	V
V_{IH}	Input high-level threshold		1.27			V
V_{IHSS}	Input high-level threshold steady state		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output low-level voltage				0.45	V
V_{OH}	Output high-level voltage		VDDSHV-0.45[1]			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	4			mA
3.3-V Mode						
V_{IL}	Input low-level threshold				0.25 × VDDSHV[1]	V
V_{ILSS}	Input low-level threshold steady state				0.15 × VDDSHV[1]	V
V_{IH}	Input high-level threshold		0.625 × VDDSHV[1]			V
V_{IHSS}	Input high-level threshold steady state		0.625 × VDDSHV[1]			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output low-level voltage				0.125 × VDDSHV[1]	V
V_{OH}	Output high-level voltage		0.75 × VDDSHV[1]			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	10			mA

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes* , POWER column.

6.6.6 CSI2/DSI D-PHY Electrical Characteristics

Note

The CSI2/DSI DPHY interfaces electrical characteristics are compliant with the MIPI D-PHY Specifications v1.2 (August 1, 2014) including ECNs and Errata, as applicable.

6.6.7 ADC12B Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
$V_{MCU\_ADC0/1\_AIN[7:0]}$	Full-scale Input Range		VSS		VDDA_ADC0/1	V
DNL	Differential Non-Linearity		-1	0.5	4	LSB
INL	Integral Non-Linearity			±1	±4	LSB
$LSB_{GAIN-ERROR}$	Gain Error			±2		LSB
$LSB_{OFFSET-ERROR}$	Offset Error			±2		LSB
C_{IN}	Input Sampling Capacitance			5.5		pF
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		70		dB
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		73		dB
SFDR	Spurious Free Dynamic Range	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		76		dB
$SNR_{(PLUS)}$	Signal-to-Noise Plus Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		69		dB
$R_{MCU\_ADC0/1\_AIN[0:7]}$	Input Impedance of MCU_ADC0/1_AIN[7:0]	f = input frequency		$[1/((65.97 \times 10^{-12}) \times f_{SMPL\_CLK})]$		Ω
I_{IN}	Input Leakage	MCU_ADC0/1_AIN[7:0] = VSS			-10	µA
		MCU_ADC0/1_AIN[7:0] = VDDA_ADC0/1			24	µA
Sampling Dynamics						
F_{SMPL_CLK}	SMPL_CLK Frequency			60		MHz
t_C	Conversion Time			13		ADC0/1 SMPL_CLK Cycles
t_{ACQ}	Acquisition time		2		257	ADC0/1 SMPL_CLK Cycles
T_R	Sampling Rate	ADC0/1 SMPL_CLK = 60 MHz		4		MSPS
CCISO	Channel to Channel Isolation			100		dB
General Purpose Input Mode (1)						
V_{IL}	Input low-level threshold				0.35 × VDDA_ADC0/1	V

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ILSS}	Input high-level threshold steady state				0.35 × VDDA_ADC0/1	V
V_{IH}	Input high-level threshold		0.65 × VDDA_ADC0/1			V
V_{IHSS}	Input high-level threshold steady state		0.65 × VDDA_ADC0/1			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			6	µA

(1) MCU_ADC0/1 can be configured to operate in General Purpose Input mode, where all MCU_ADC0/1_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0/1_CTRL register (gpi_mode_en = 1).

6.6.8 LVCMOS Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH}	High Level Output Current	$V_{OH(MIN)}$	3			mA
3.3-V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH}	High Level Output Current	$V_{OH(MIN)}$	6			mA

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

6.6.9 USB2PHY Electrical Characteristics

Note

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

6.6.10 SerDes 2-L-PHY/4-L-PHY Electrical Characteristics

Note

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, September 27, 2017.

This Device imposes an additional limit on SERDES REFCLK when used in Input mode with internal termination enabled, as described by parameter V_{REFCLK_TERM} in Table 6-2, *4-L-PHY SERDES REFCLK Electrical Characteristics*. Internal termination is enabled by default and must be disabled before applying a reference clock signal that exceeds the limits defined by V_{REFCLK_TERM}. External termination should always be enabled on the source side.

Table 6-2. 4-L-PHY SERDES REFCLK Electrical Characteristics

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{REFCLK_TERM}	Single ended voltage threshold at the reference clock pin when internal termination is enabled			450	mV
R_{TERM}	Internal termination	40	50	62.5	Ω

Note

The SerDes USB interfaces are compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0 , July 26, 2013.

Note

The SGMII interfaces electrical characteristics are compliant with 1000BASE-KX per IEEE802.3 Clause 70.

Note

The SGMII 2.5G / XAUI interfaces electrical characteristics are compliant with IEEE802.3 Clause 47.

Note

The QSGMII interface electrical characteristics are compliant with QSGMII Specification revision 1.2.

Note

USXGMII supports IEEE 802.3 TX and RX electrical characteristics of Clause 72-7 and Annex 69B. It does not support 10GBase-KR auto-negotiation (Clause 73) and link training (Clause 72).

IEEE 802.3 Tables 72-7 and 72-8 are not required by USXGMII since these tables are associated with training (Clause 72-6), which is not a requirement of USXGMII.

The pre, main, and post cursors should be set by using BER sweeps.

Note

The XFI interface electrical characteristics are compliant with the INF-8077_XFP_XFI_10Gbps_1X specification revision 4.5, August 31, 2005.

Note

The UFS interface electrical characteristics are compliant with MIPI M-PHY Specification v3.1, February 17, 2014.

Note

The DP interface electrical characteristics are compliant with the VESA DisplayPort (DP) Standard v 1.4 February 23, 2016.

Note

The eDP interface electrical characteristics are compliant with the VESA Embedded DisplayPort (eDP) Standard v1.4b October 23, 2015.

6.6.13 DDR0 Electrical Characteristics

Note

The DDR interface is compatible with JESD209-4B standard compliant LPDDR4 SDRAM devices.

6.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

6.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation	See Recommended Operating Conditions			V
VDD_MCU	Supply voltage range for the core domain during OTP operation	See Recommended Operating Conditions			V
VDD_CPU	Supply voltage range for the core domain during OTP operation; (BOOT voltage)	See Recommended Operating Conditions			V
VPP_CORE	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM	NC(2)			V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM	0			V
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.71	1.8	1.89	V

6.7.1 Recommended Operating Conditions for OTP eFuse Programming (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VPP_MCU	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(2)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.71	1.8	1.89	V
$SR_{(VPP)}$	VPP Power-up Slew Rate			6E + 4	V/s

(1) Supply voltage range includes DC errors and peak-to-peak noise.
(2) NC indicates No Connect.

6.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP_CORE and VPP_MCU power supplies must be disabled when not programming OTP registers.
- The VPP_CORE and VPP_MCU power supplies must be ramped up after the proper device power-up sequence (for more details, see *Power Supply Sequencing*).

6.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP_CORE and VPP_MCU terminals during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP_CORE and VPP_MCU terminals according to the specification in Section 6.7.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP_CORE and VPP_MCU terminals.

6.7.4 Impact to Your Hardware Warranty

You accept that eFusing the TI Devices with security keys permanently alters them. You acknowledge that the eFuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI device inoperable and TI will be unable to confirm whether the TI devices conformed to their specifications prior to the attempted eFuse. Consequently, TI will have no liability (*warranty or otherwise*) for any TI devices that have been incorrectly eFused by customers.

6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

6.8.1 Thermal Resistance Characteristics for AND Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	AND PACKAGE	
			°C/W(1) (3)	AIR FLOW (m/s)(2)
T1	$R\Theta_{JC}$	Junction-to-case	0.16	N/A
T2	$R\Theta_{JB}$	Junction-to-board	1.47	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	9.22	0
T4		Junction-to-moving air	5.07	1
T5			4.31	2
T7	Ψ_{JT}	Junction-to-package top	0.10	0
T8			0.10	1
T9			0.10	2
T11	Ψ_{JB}	Junction-to-board	1.30	0
T12			1.23	1
T13			1.18	2

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.
(3) °C/W = degrees Celsius per watt.

6.9 Temperature Sensor Characteristics

This section summarizes the Voltage and Temperature Module (VTM) on die temperature sensor characteristics.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in the Recommended Operating Conditions.

Table 6-3. VTM Die Temperature sensor Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	VTM temperature sensor accuracy	–40 to 110 ℃	–5		5	℃
		110 to 125 ℃	–2		2	℃

6.10 Timing and Switching Characteristics

Note

The timings presented in this section are valid when the DRV_STR (Drive Strength) control in the associated PADCONFIG registers are set to the default “0h – Nominal (recommended)” value.

6.10.1 Timing Parameters and Information

The timing parameter symbols used in Timing and Switching Characteristics are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 6-4:

Table 6-4. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.10.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The device can be operated using either an isolated or combined MCU & Main power distribution network (PDN). Two different primary power sequences are recommended based upon isolated and combined MCU & Main PDNs. In addition, the device can be operated in either MCU Only or DDR Retention or GPIO Retentioon low power modes. Two different desired device power supply sequences for entry and exit of low power modes are shown.

The power supply names used in this section are specific to this device and align to names given in the Signal Descriptions section. Common power supply names may be used across different devices within the Jacinto 7™ processor family. These common supply names will have very similar if not identical functions across devices.

All power sequencing timing diagrams shown will use the following terminology:

- Primary = Essential power sequences of all voltage domains between off and full active states.
- $V_{OPR\ MIN}$ = Minimum operational voltage level that ensures functionality as specified in Recommended Operating Conditions
- Ramp-up = start of a voltage supply transition time from off condition to Vopr min.
- Ramp-down = start of a voltage supply transition time from Vopr to off condition
- Supply_“n” = multiple instances of similar power supplies (i.e. VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 … VDDSHV6)
- Supply_“xxx” = multiple instances of similar power supplies used for different signal types (i.e. VDDA_1P8_xxx = VDDA_1P8_DSITX, VDDA_1P8_USB, VDDA_0P8_DSITX, VDDA_0P8_USB, etc.)
- Time stamps = “T#” markers with descriptions and approximate elapsed times for general reference. Specific timing transitions are dependent upon PDN design (see PDN User Guide for details).

6.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/us, as shown in Figure 6-2. For instance, a 1.8V supply should have a ramp time > 18 µs to ensure the slew rate < 100mV/us.

Figure 6-2 describes the Power Supply Slew Rate Requirement in the device.

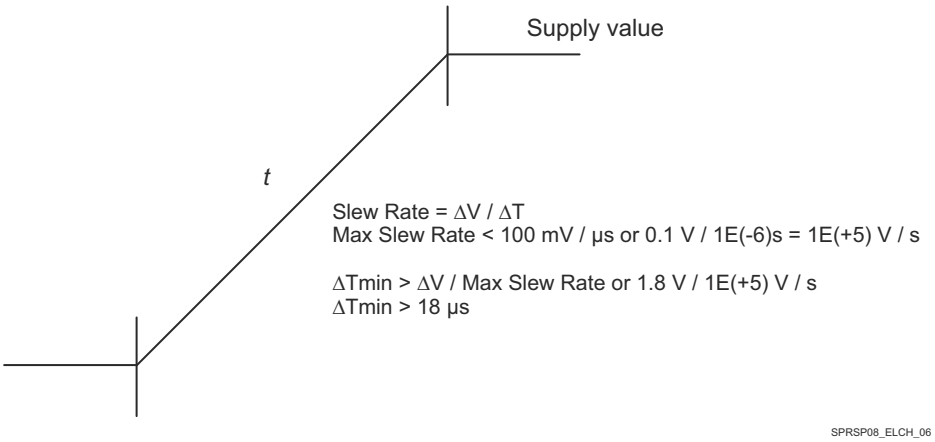
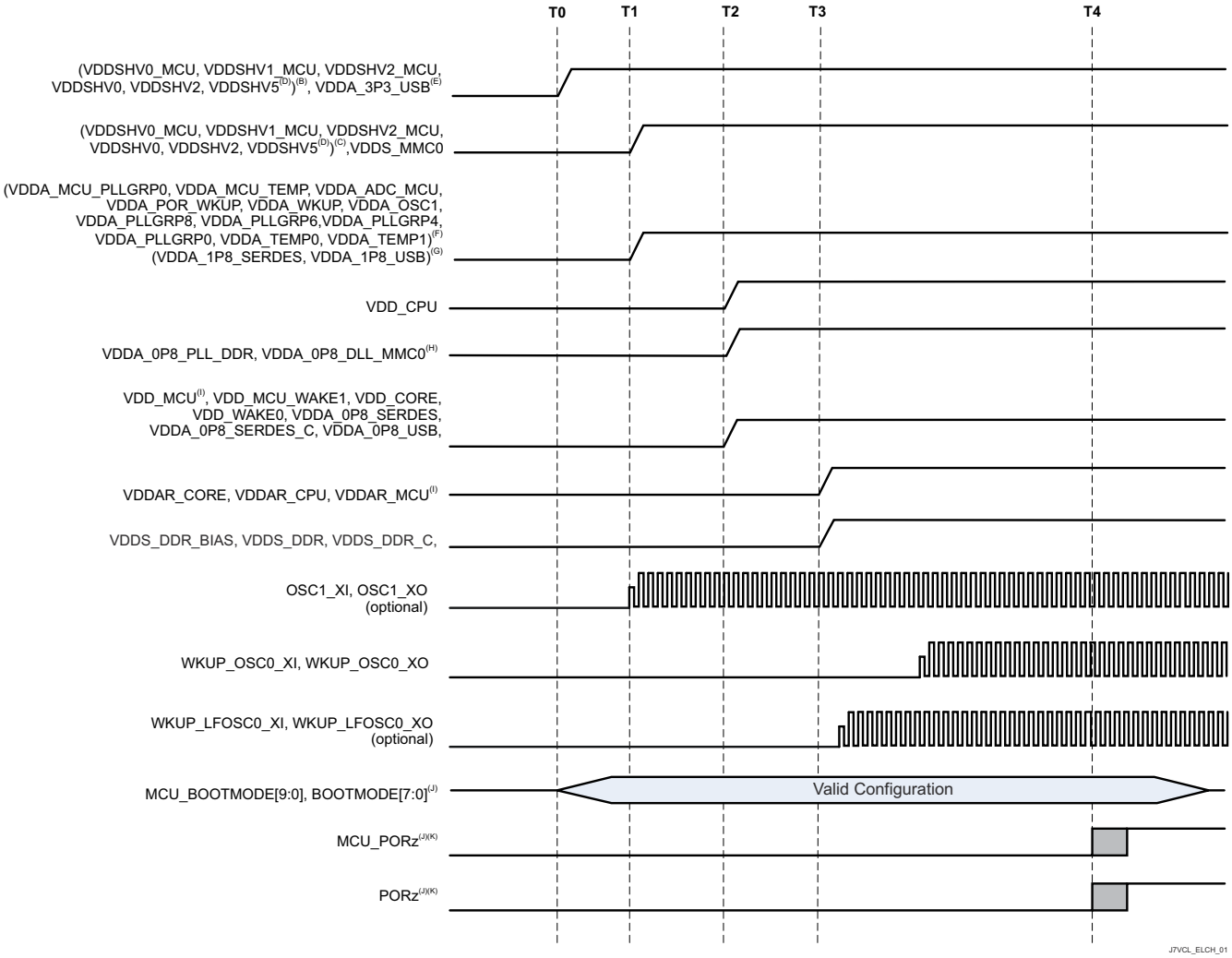


Figure 6-2. Power Supply Slew and Slew Rate

6.10.2.2 Combined MCU and Main Domains Power- Up Sequencing

Section 6.10.2.2 describes the primary power-up sequencing when similar MCU and Main voltage domains are combined into common power rails. Combining MCU and Main voltage domains simplifies PDN design by reducing total number of power rails and sources while making MCU and Main processor sub-systems operational dependent on common power rails.



A. Time stamp markers:
- T0 – 3.3V voltages start ramp-up to $V_{OPR\ MIN}$. (0 ms)
- T1 – 1.8-V voltages start ramp-up to $V_{OPR\ MIN}$. (2 ms)
- T2 – Low voltage core supplies start ramp-up to $V_{OPR\ MIN}$. (3 ms)
- T3 – Low voltage RAM array voltages start ramp-up to $V_{OPR\ MIN}$. (4 ms)
- T4 – OSC1 is stable and PORz/MCU_PORz are de-asserted to release processor from reset. (13 ms)

B. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.

C. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-up aligned to T3 due to PDN designs grouping supplies with VDD_MMC0.

D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3 V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.

E. VDDA_3P3_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.

F. VDDA_1P8_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA_1p8_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.

G. VDDA_1P8_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.

H. VDDA_0P8_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.

I. VDD_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR_MCU domain or with VDD_CORE; for the “Combined MCU and Main Domains Power-Up Sequencing,” VDD_MCU can be grouped with VDD_CORE, and VDDAR_MCU can be grouped with VDDAR_CPU and VDDAR_CORE. If VDD_MCU is grouped with VDD_CORE, VDD_MCU must be ramped-up from a common voltage resource with 0.8-V VDD_CORE at T2. If VDD_MCU is not grouped with VDD_CORE, VDD_MCU must be ramped-up before T2. In either case, the VDDAR supplies must be ramped at T3.

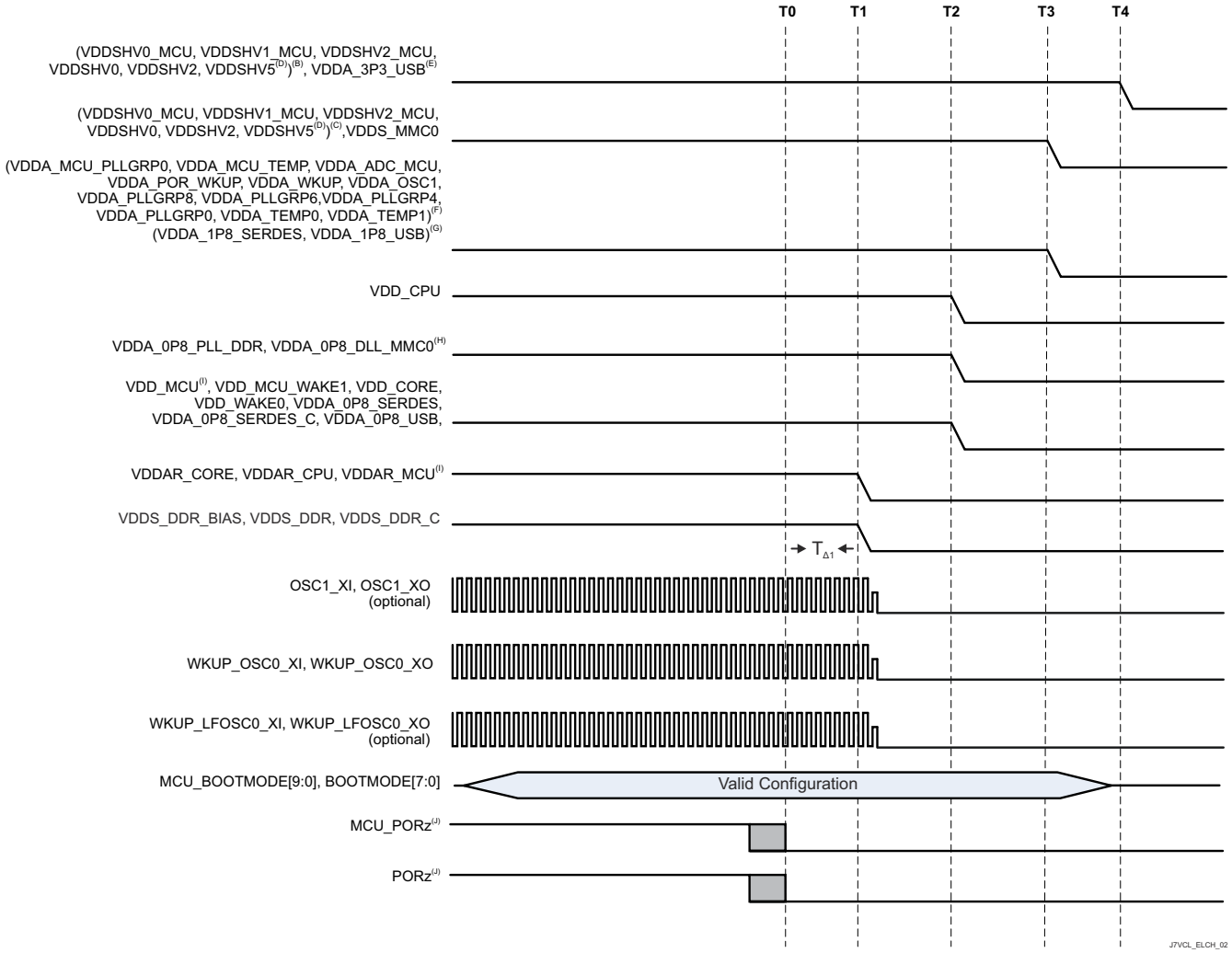
J. Minimum set-up and hold times shown with respect to MCU_PORz and PORz asserting high to latch MCU_BOOTMODEn (referenced to MCU_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.

K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer’s clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

Figure 6-3. Combined MCU and Main Domains, Primary Power-Up Sequence

6.10.2.3 Combined MCU and Main Domains Power- Down Sequencing - Option 1

Figure 6-4 describes the device power-down sequencing for option 1.



A. Time stamp markers:
   - T0 – MCU_PORz & PORz assert low to put all processor resources in safe state. (0ms)
   - T1 – Main DDR, SRAM Core, and SRAM CPU power supplies start ramp-down. (0.5ms)
   - T2 – Low voltage core supplies start supply ramp-down. (2.5ms)
   - T3 - 1.8-V voltages start supply ramp-down. (3.0ms)
   - T4 – 3.3-V voltages start supply ramp-down. (3.5ms)

B. Any MCU or Main dual voltage IO domains (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3-V digital interfaces.

C. Any MCU or Main dual voltage IO domains (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8-V digital interfaces.

D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3V/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8-V power rail.

E. VDDA_3P3_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.

F. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA_1p8_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required .

G. VDDA_1P8_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.

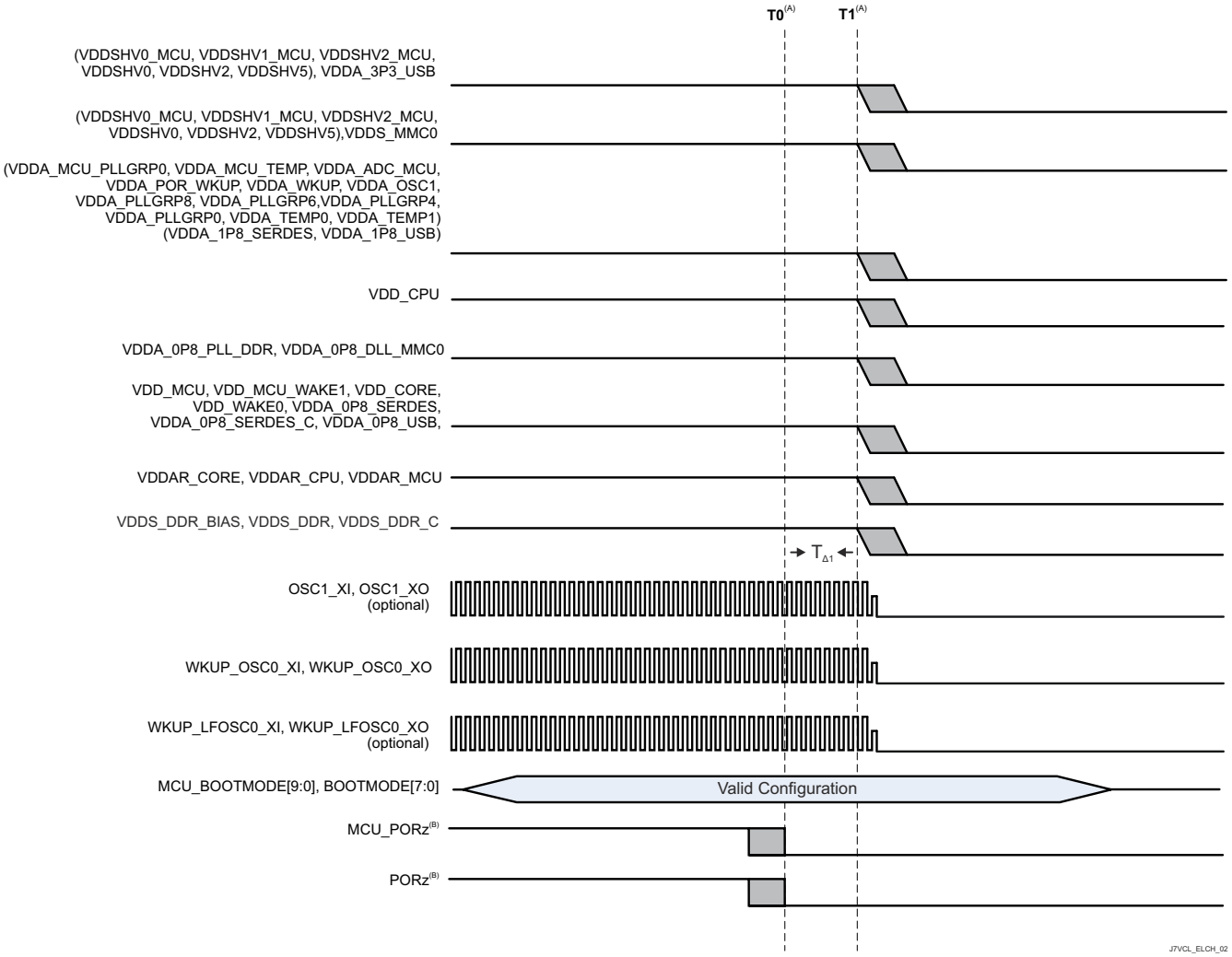
H. VDDA_0P8_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.

I. MCU_PORz and PORz must be asserted low for TΔ1 = 200µs MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

Figure 6-4. Combined MCU and Main Domains, Primary Power-Down Sequence - Option 1

Combined MCU and Main Domains Power- Down Sequencing - Option 2

Figure 6-5 describes the device power-down sequencing for option 2.



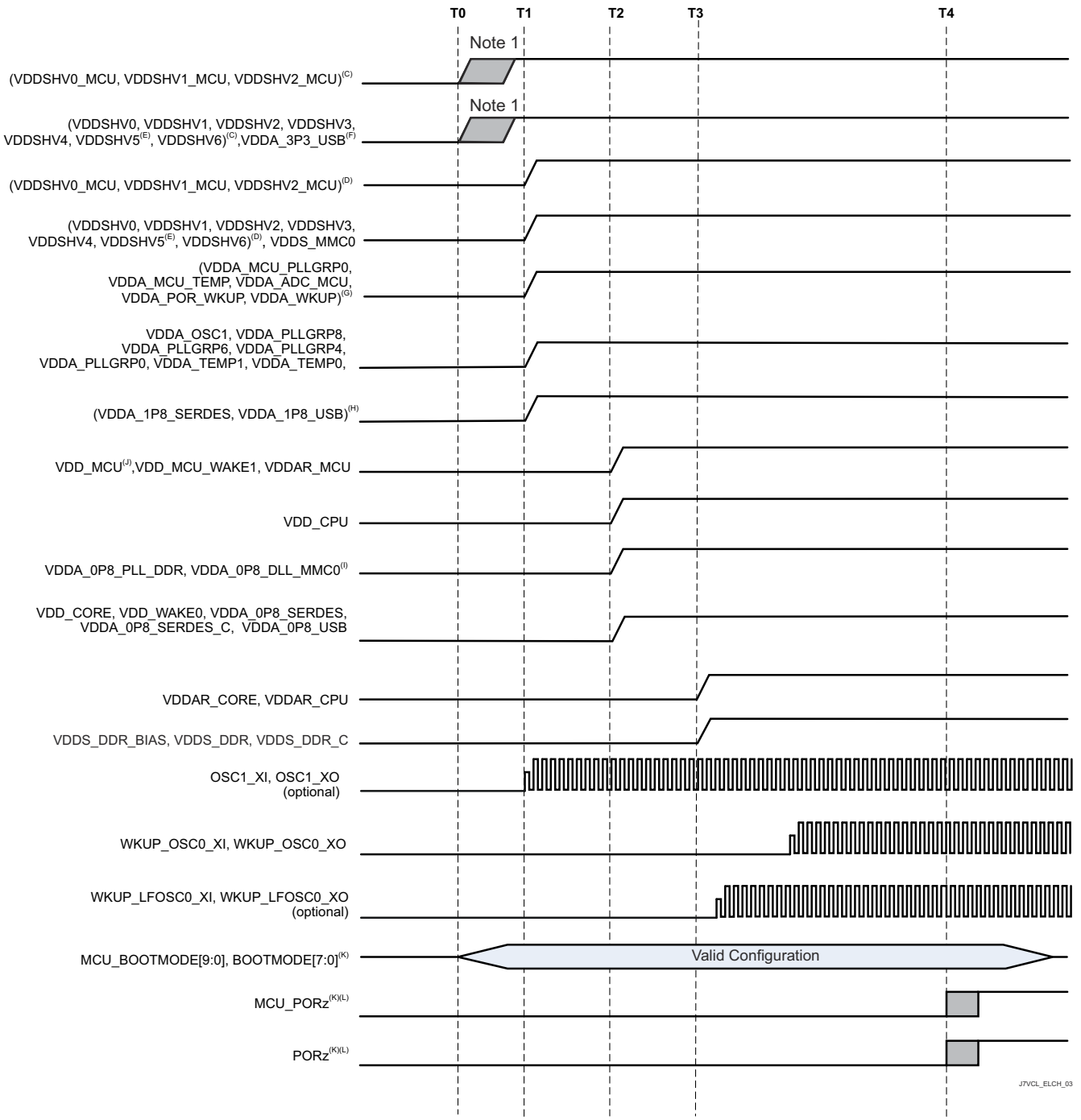
A. Time stamp markers:
   - T0 – MCU_PORz & PORz assert low to put all processor resources in safe state. (0ms)
   - T1 – All power supplies start ramp-down. (0.2ms)

B. MCU_PORz and PORz must be asserted low for TΔ1 = 200µs MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

Figure 6-5. Combined MCU and Main Domains, Primary Power-Down Sequence - Option 2

6.10.2.4 Isolated MCU and Main Domains Power- Up Sequencing

Isolated MCU and Main voltage domains enable an SoC's MCU and Main processor sub-systems to operate independently. There are 2 reasons an SoC's PDN design may need to support independent MCU and Main processor functionality. First is to provide flexibility to enable SoC low power modes that can significant reduce SoC power dissipation when processor operations are not needed. Second is to enable robustness to gain freedom from interference (FFI) of a single fault impacting both MCU and Main processor sub-systems which is especially beneficial if using the SoC's MCU as the system safety monitoring processor. The number of additional PDN power rails needed is dependent upon number of different MCU IO signaling voltage levels. If only 1.8V IO signaling is used, then only 2 additional power rails could be required. If both 1.8 and 3.3V IO signaling is desired, then 4 additional power rails could be needed.



A. T1Time stamp markers:
- T0 – All 3.3-V voltages start supply ramp-up to $V_{OPR\ MIN}$. (0 ms)
- T1 – All 1.8-V voltages start supply ramp-up to $V_{OPR\ MIN}$. (2 ms)
- T2 – All core voltages start supply ramp-up to $V_{OPR\ MIN}$. (3 ms)
- T3 – All RAM array voltages start supply ramp-up to $V_{OPR\ MIN}$. (4 ms)
- T4 – OSC1 is stable and PORz/MCU_PORz are de-asserted to release processor from reset. (13 ms)

B. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.

C. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have delayed start times that aligns to T3 due to PDN designs grouping supplies with VDD_MMC0.

D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant UHS-I SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then supply can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then supply can be grouped with digital IO 1.8-V power rail.

E. VDDA_3P3_USB is 3.3-V analog supply used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then supply can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.

F. VDDA_1P8_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA_1p8_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.

G. VDDA_1P8_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.

H. VDDA_0P8_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.

I. VDD_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR_MCU domain or with VDD_CORE; for the “Isolated MCU and Main Domains Power-Up Sequencing,” VDD_MCU can be grouped with VDDAR_MCU; VDD_MCU must be ramped-up before T2. If VDDAR_MCU is not grouped with VDD_MCU, it must be ramped at T3.

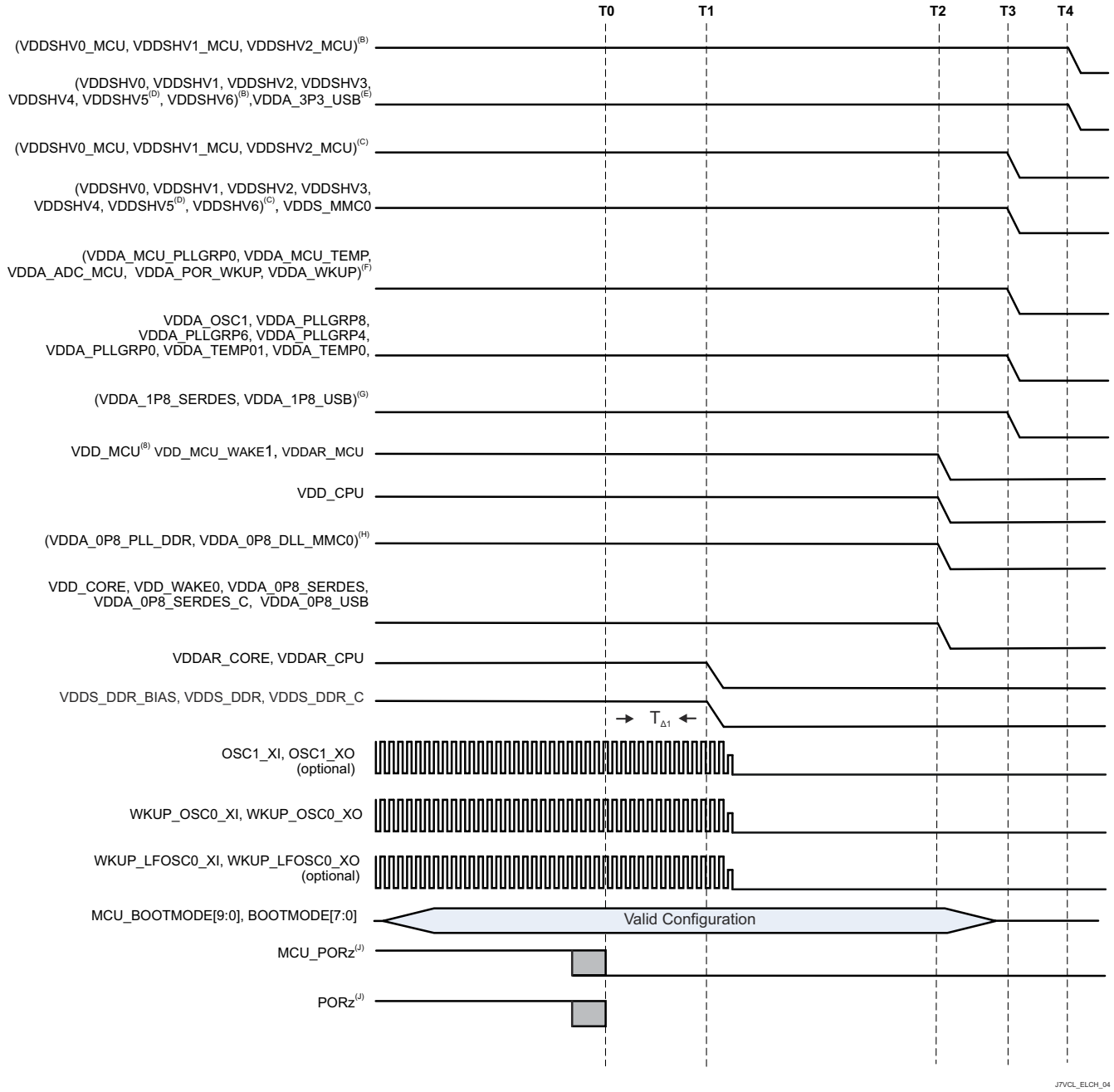
J. Minimum set-up and hold times shown with respect to MCU_PORz and PORz asserting high to latch MCU_BOOTMODEn (referenced to MCU_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.

K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer’s clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

Figure 6-6. Isolated MCU and Main Domains, Primary Power-Up Sequence

6.10.2.5 Isolated MCU and Main Domains Power- Down Sequencing - Option 1

Figure 6-7 describes the device power-down sequencing for option 1.



A. Time stamp markers:
   - T0 – MCU_PORz and PORz assert low to put all processor resources in safe state. (0ms)
   - T1 – Main DDR, SRAM Core, and SRAM CPU power domains start ramp-down. (0.5ms)
   - T2 – All core voltages start supply ramp-down. (2.5ms)
   - T3 – All 1.8-V voltages start supply ramp-down. (3.0ms)
   - T4 – All 3.3-V voltages start supply ramp-down. (3.5ms)

B. Any MCU or Main dual voltage IO domains (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3-V digital interfaces.

C. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-down aligned to T1 due to PDN designs grouping supplies with VDD_MMC0.

D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3V/1.8V) power rail is required for compliant, high-speed SD card operations. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3V/1.8V) power source and rail are required. The start of ramp-down from 3.3V/1.8V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8-V power rail.

E. VDDA_3P3_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-down from 3.3V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.

F. VDDA_1P8_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA_1p8_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.

G. VDDA_1P8_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.

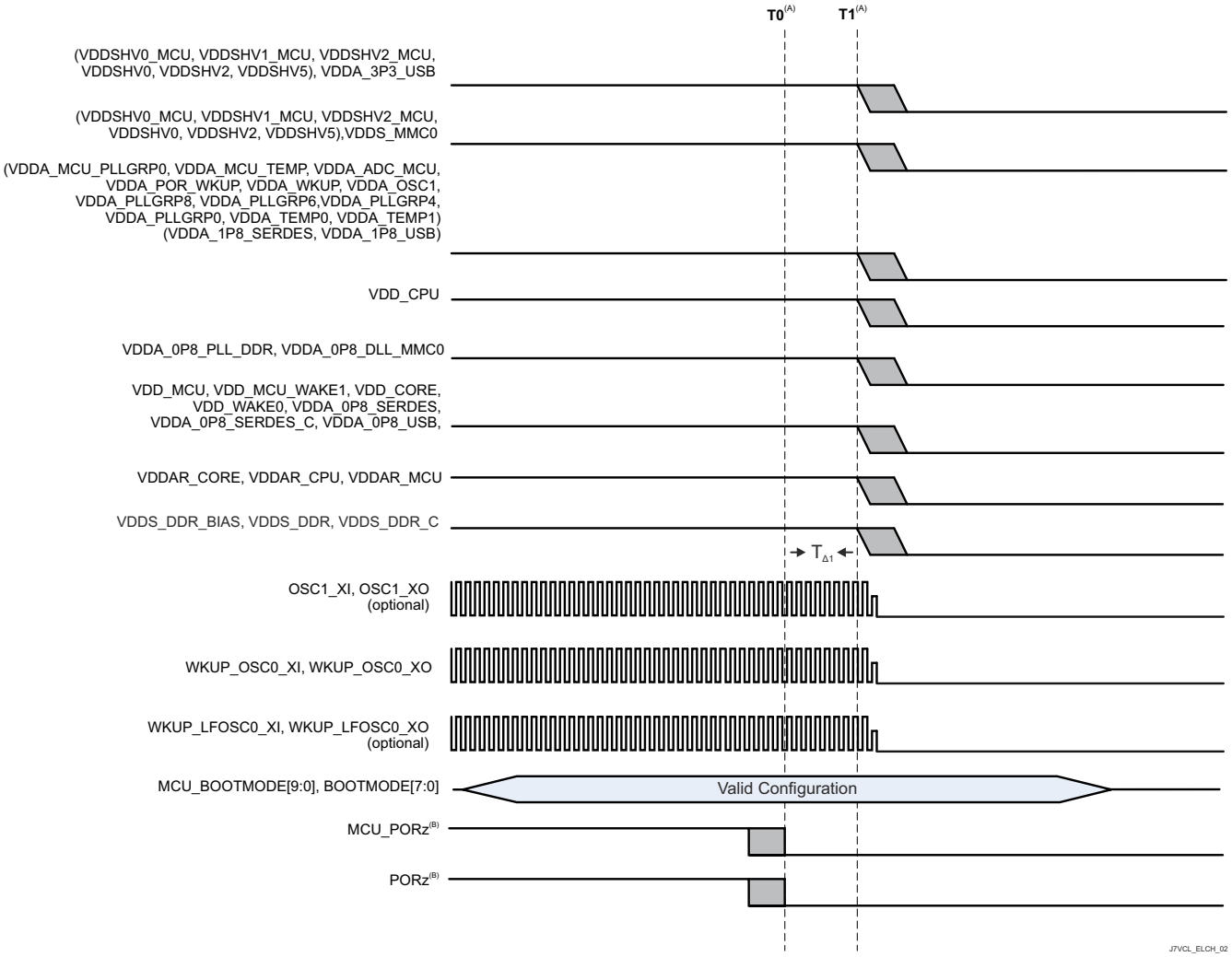
H. VDDA_0P8_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.

I. MCU_PORz and PORz must be asserted low for TΔ1 = 200µs MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

Figure 6-7. Isolated MCU and Main Domains, Primary Power- Down Sequencing - Option 1

Isolated MCU and Main Domains Power- Down Sequencing - Option 2

Figure 6-8 describes the device power-down sequencing for option 2.



A. Time stamp markers:
   - T0 – MCU_PORz and PORz assert low to put all processor resources in safe state. (0ms)
   - T1 – All power supplies start ramp-down. (0.2ms)

B. MCU_PORz and PORz must be asserted low for TΔ1 = 200µs MIN to ensure SoC resources enter into safe state before any voltage begins to ramp down.

Figure 6-8. Isolated MCU and Main Domains, Primary Power- Down Sequencing - Option 2

6.10.2.6 Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing

Entry into MCU Only state is accomplished by executing a power down sequence except for the 4 MCU domains that remain energized. Exit from MCU Only state is accomplished by executing a power up sequence with the 4 MCU domains remaining energized throughout the seque.

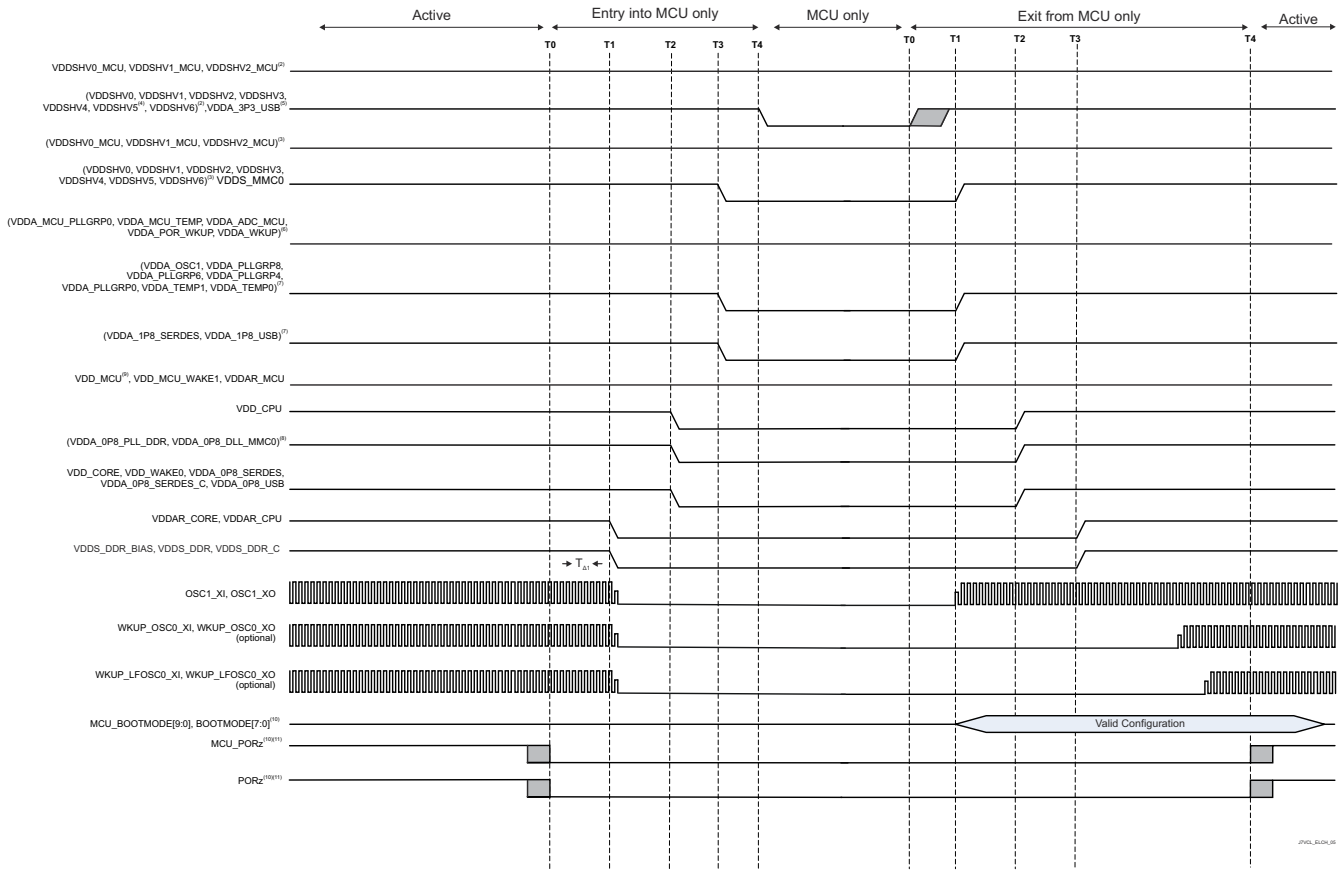


Figure 6-9. Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing

6.10.2.7 Independent MCU and Main Domains, Entry and Exit of DDR Retention State

Entry into DDR Retention state is accomplished by executing a power down sequence except for the 4 DDR domains that remain energized. Exit from DDR Retention state is accomplished by executing a power up sequence with the 3 DDR domains remaining energized throughout the sequence.

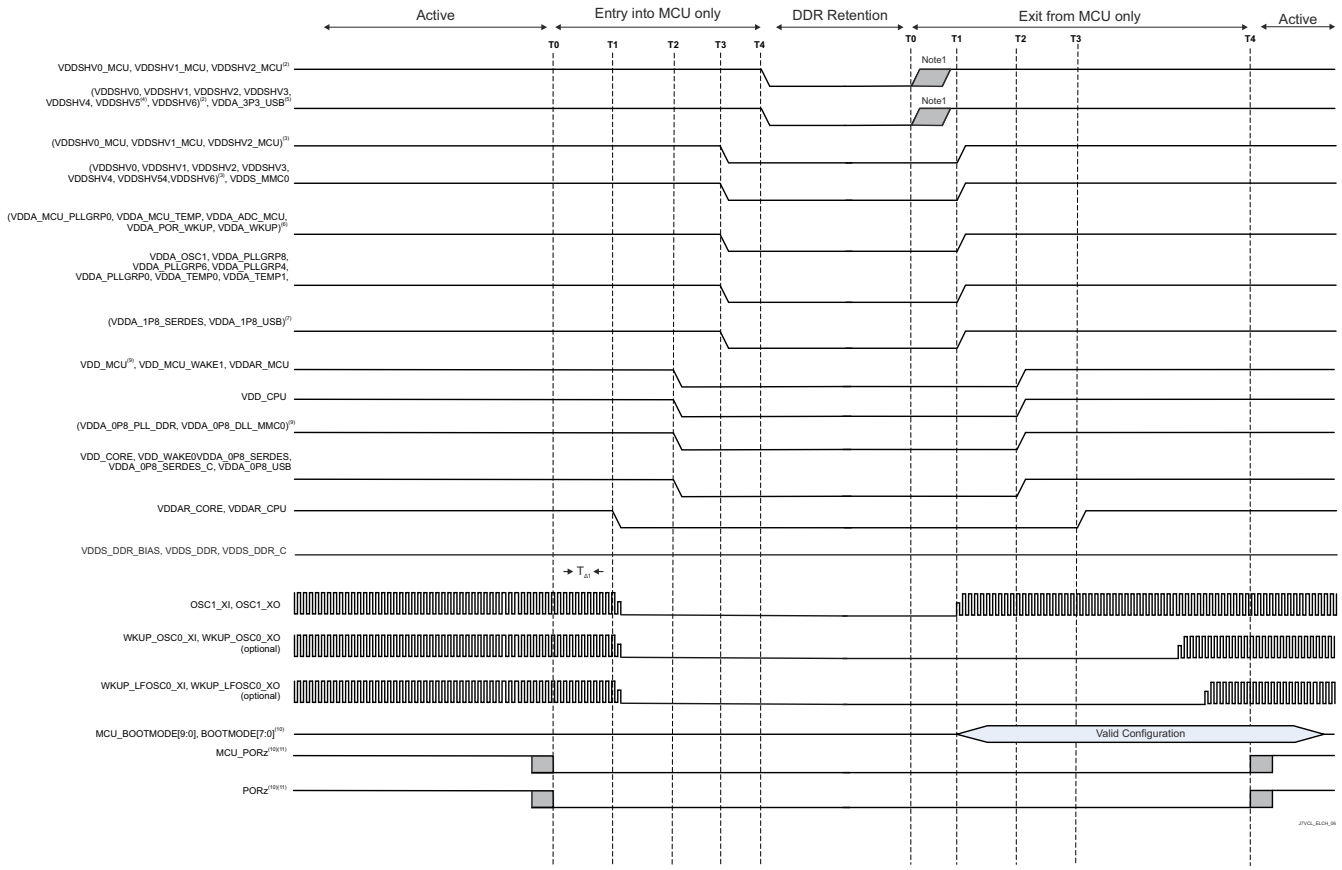


Figure 6-10. Independent MCU and Main Domains, Entry and Exit of DDR Retention State

6.10.2.8 Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing

Entry into GPIO Retention state is accomplished by executing a power down sequence except for the 2 or 4 wake domains that remain energized. Exit from GPIO Retention state is accomplished by executing a power up sequence with the 2 or 4 wake DDR domains remaining energized throughout the sequence.

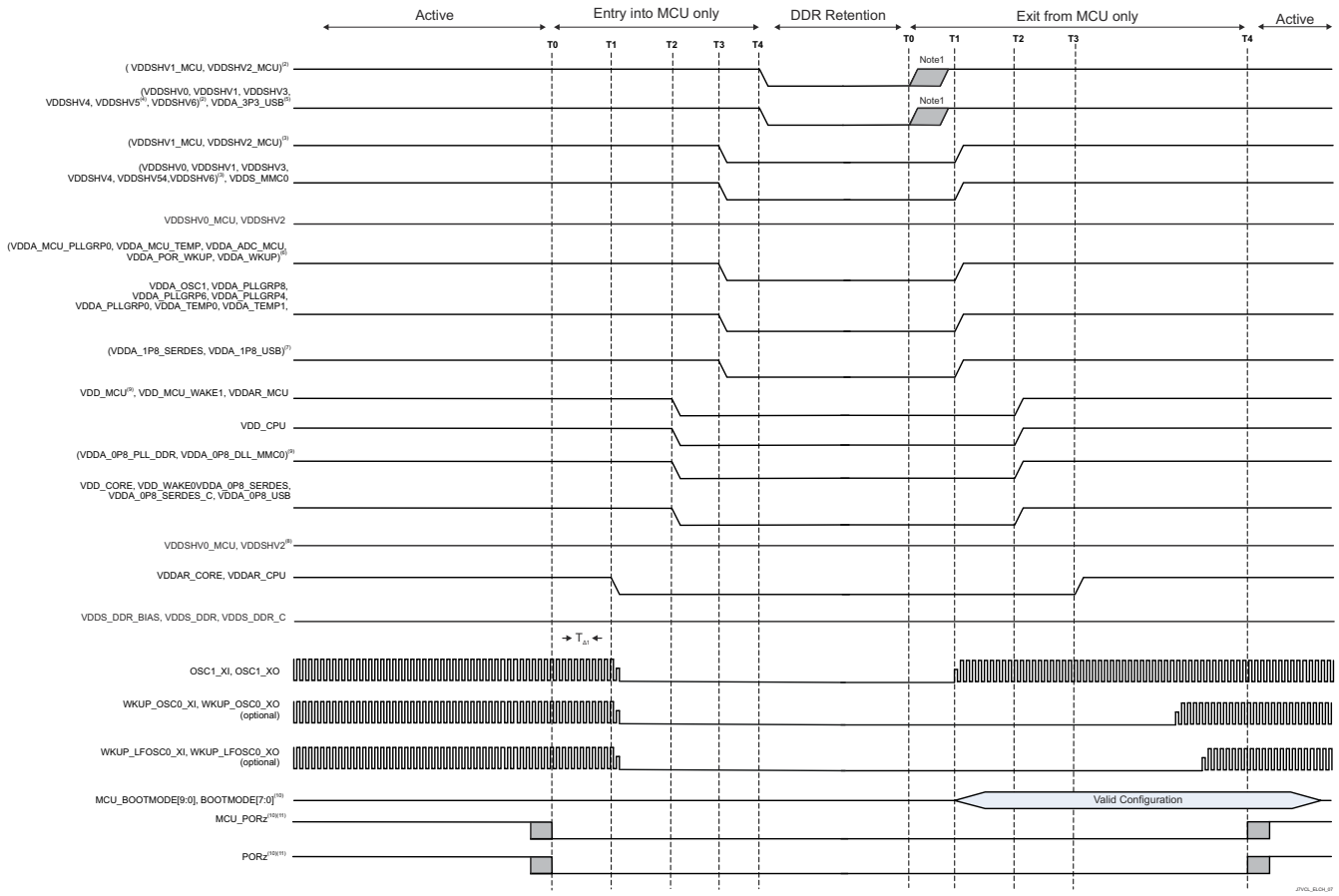


Figure 6-11. Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing

6.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within Signal Descriptions.

6.10.3.1 Reset Timing

The tables and figures provided in this section define the timing conditions, timing requirements, and switching characteristics for reset related signals.

Table 6-5. Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.0018		V/ns
		VDD(1) = 3.3V	0.0033		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance			30	pF

(1) VDD stands for the corresponding power supply. For more information on the power supply name and the corresponding ball/balls, see the POWER column of the Pin Attributes table.

Table 6-6. MCU_PORz Timing Requirements

see Figure 6-12

NO.			MIN	TYP	MAX	UNIT
RST1	$t_{h(MCUD\_SUPPLIES\_VALID - MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies valid (using external crystal)	N + 1200(2)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies(1) valid and external clock stable (using external LVCMOS oscillator)	1200			ns
RST3	$t_{w(MCU\_PORzL)}$	Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200			ns

(1) For the definition of the MCU DOMAIN supplies, see the Combined MCU and Main Domains Power-Up Sequencing.
(2) N = oscillator start-up time

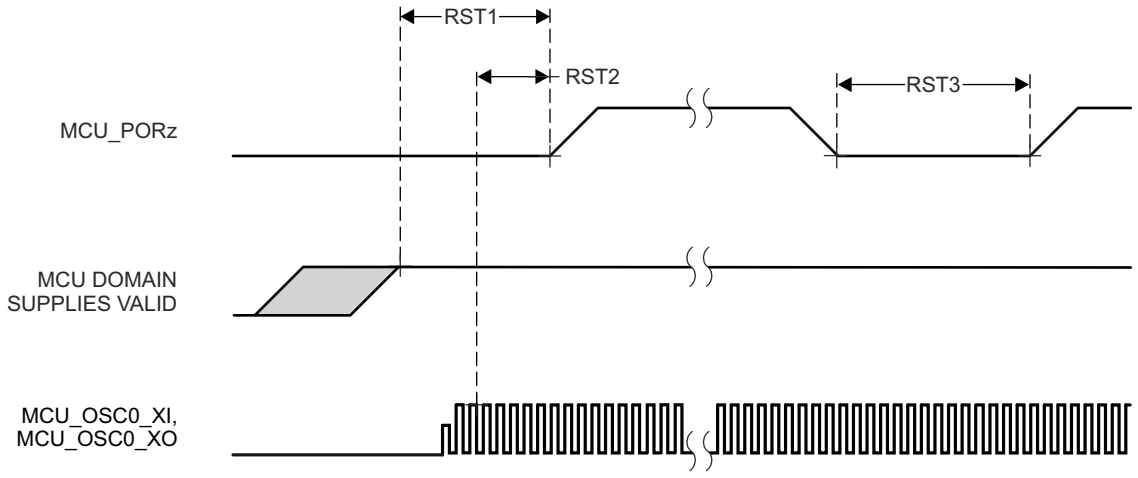


Figure 6-12. MCU_PORz Timing Requirements

Table 6-7. PORz Timing Requirements

see Figure 6-13

NO.			MIN	MAX	UNIT
RST4	$t_{h(MAIND\_SUPPLIES\_VALID - PORz)}$	Hold time, PORz active (low) at Power-up after all MAIN DOMAIN supplies(1) valid	1200		ns
RST5	$t_{w(PORzL)}$	Pulse Width minimum, PORz low after Power-up	1200		ns

(1) For the definition of the MAIN DOMAIN supplies, see the Combined MCU and Main Domains Power-Up Sequencing.

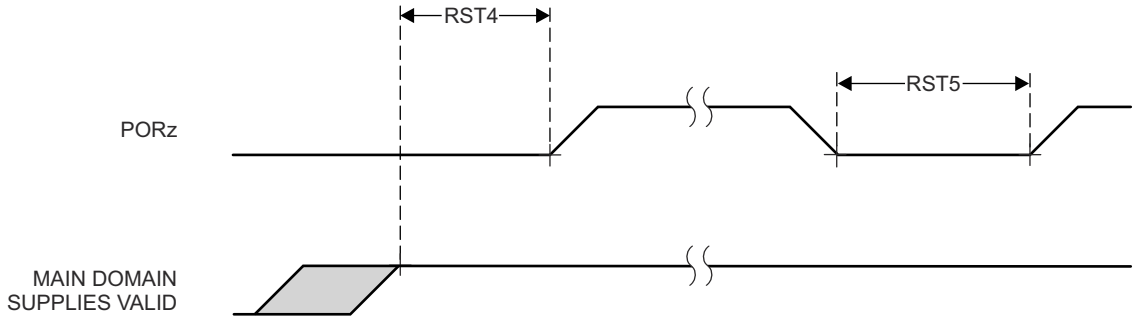


Figure 6-13. PORz Timing Requirements

Table 6-8. MCU_PORz initiates; MCU_PORz_OUT, PORz_OUT, MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 6-14

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST6	$t_{d(MCU\_PORzL-MCU\_PORz\_OUTL)}$	Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)		0		ns
RST7	$t_{d(MCU\_PORzH-MCU\_PORz\_OUTH)}$	Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)		0		ns
RST8	$t_{d(MCU\_PORzL-PORz\_OUTL)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)		0		ns
RST9	$t_{d(MCU\_PORzH-PORz\_OUTH)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)		1500		ns
RST10	$t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)		0		ns
RST11	$t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	POST bypass	12000*S(1)		ns
RST12	$t_{d(MCU\_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)		0		ns
RST13	$t_{d(MCU\_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)		14500*S(1)		ns
RST14	$t_{w(MCU\_PORz\_OUTL)}$	Pulse width minimum, MCU_PORz_OUT active (low)		1200		ns
RST15	$t_{w(PORz\_OUTL)}$	Pulse Width Minimum PORz_OUT low		2550		ns
RST16	$t_{w(MCU\_RESETSTATzL)}$	Pulse Width Minimum MCU_RESETSTATz low		3900*S(1)		ns
RST17	$t_{w(RESETSTATzL)}$	Pulse Width Minimum RESETSTATz low		2650*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period.

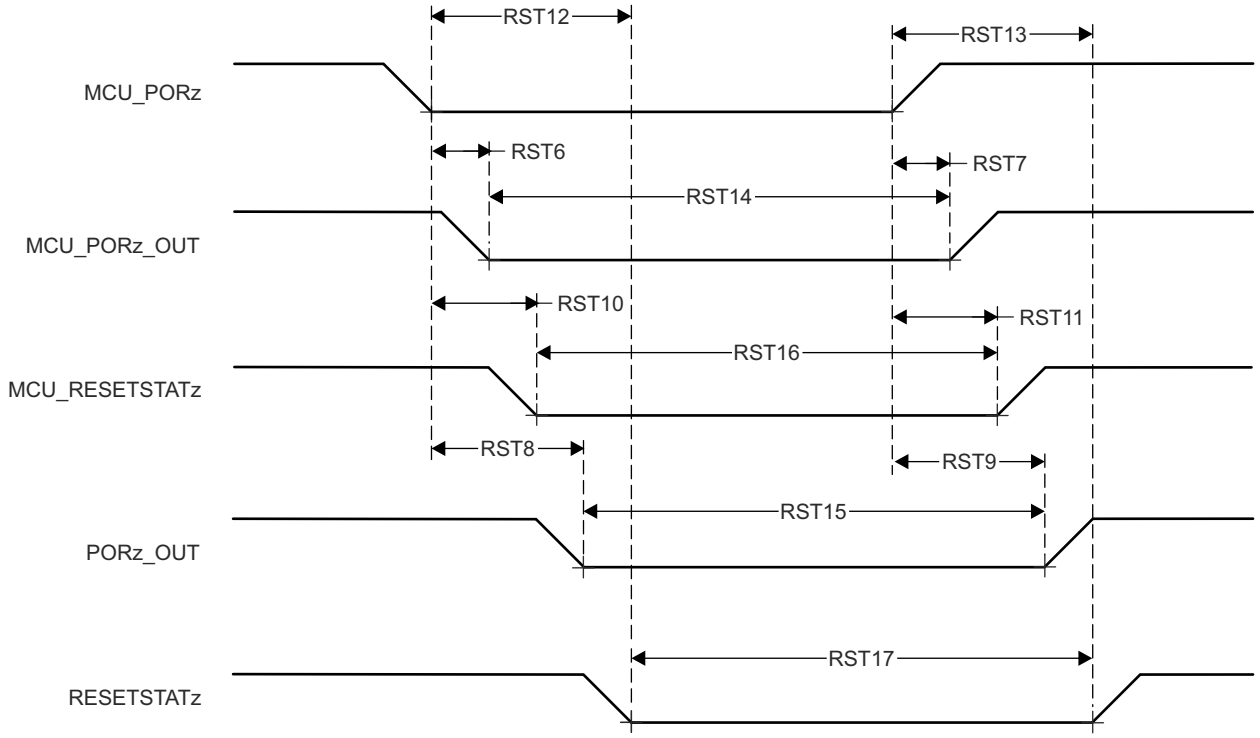


Figure 6-14. MCU_PORz initiates; MCU_PORz_OUT, PORz_OUT, MCU_RESETSTATz, and RESETSTATz Switching Characteristics

Table 6-9. PORz Initiates; PORz_OUT and RESETSTATz Switching Characteristics

see Figure 6-15

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST18	$t_{d(PORzL-PORz\_OUTL)}$	Delay time, PORz active (low) toPORz_OUT active (low)	software control of POR_RST_ISO_DONE_Z	T(1)		
			CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0	0		ns
RST19	$t_{d(PORzH-PORz\_OUTH)}$	Delay time, PORz active (high) toPORz_OUT active (high)		1300		ns
RST20	$t_{d(PORzL-RESETSTATzL)}$	Delay time, PORz active (low) to RESETSTATz active (low)		T(1)		
			CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0	0		ns
RST21	$t_{d(PORzH-RESETSTATzH)}$	Delay time, PORz active (high) to RESETSTATz active (high)		14500*S (2)		ns

(1) T = Reset Isolation Time (Software Dependent).
(2) S = MCU_OSC0_XI/XO clock period.

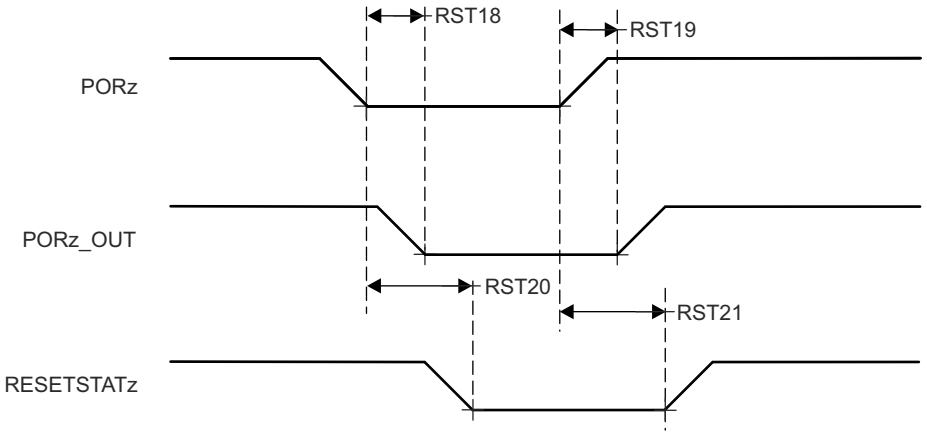


Figure 6-15. PORz initiates; PORz_OUT and RESETSTATz Switching Characteristics

Table 6-10. MCU_RESETz Timing Requirements

see Figure 6-16

NO.			MIN	MAX	UNIT
RST22	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width minimum, MCU_RESETz active (low)	1200		ns

(1) Timing for MCU_RESETz is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 6-11. MCU_RESETz initiates; MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 6-16

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	800		ns
RST24	$t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	3900*S(1)		ns
RST25	$t_{d(MCU\_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	800		ns
RST26	$t_{d(MCU\_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	3900*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period.

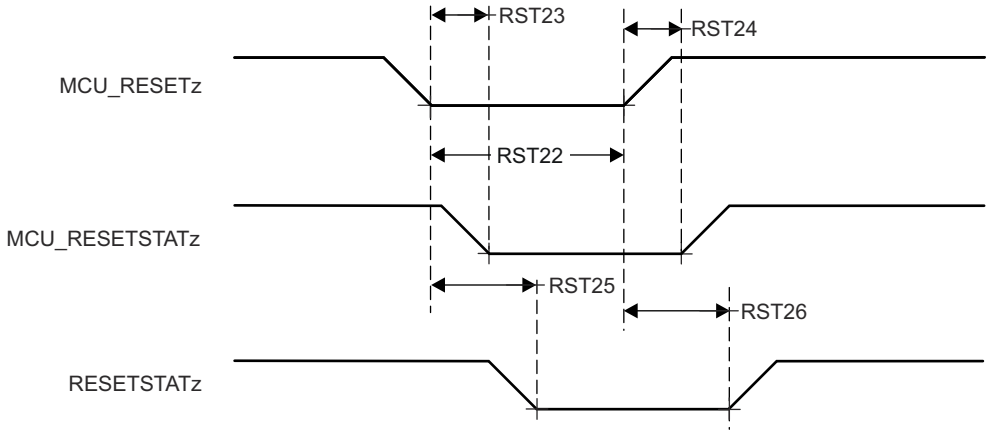


Figure 6-16. MCU_RESETz initiates; MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

Table 6-12. RESET_REQz Timing Requirements

see Figure 6-17

NO.			MIN	MAX	UNIT
RST27	$t_{w(RESET\_REQzL)}$ (1)	Pulse Width minimum, RESET_REQz active (low)	1200		ns

(1) Timing for RESET_REQz is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 6-13. RESET_REQz initiates; RESETSTATz Switching Characteristics

see Figure 6-17

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST28	$t_{d(RESET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	software control of SOC_WARMRST_ISO_DONE_Z	T(1)		
			CTRLMMR_WKUP_MAIN_WARM_RST_CTRL[0].SOC_WARMRST_ISO_DONE_Z = 0	740		ns
RST29	$t_{d(RESET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)		2650*S (2)		ns

(1) T = Reset Isolation Time (Software Dependent).
(2) S = MCU_OSC0_XI/XO clock period.

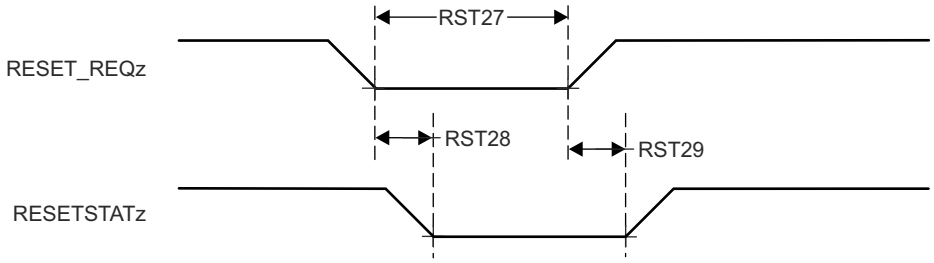


Figure 6-17. RESET_REQz initiates; RESETSTATz Timing Requirements and Switching Characteristics

Table 6-14. EMUx Timing Requirements

see Figure 6-18

NO.			MIN	MAX	UNIT
RST30	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST31	$t_{h(MCU\_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period.

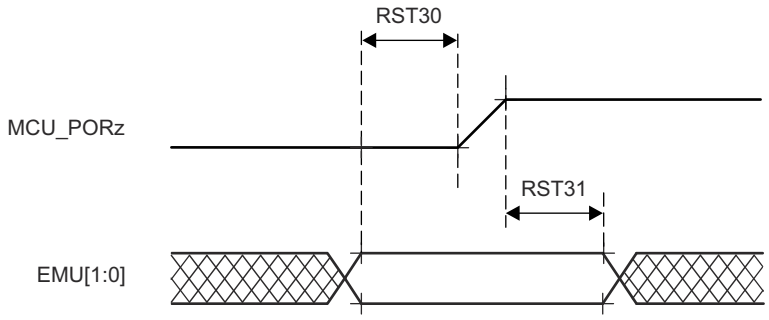


Figure 6-18. EMUx Timing Requirements

Table 6-15. MCU_BOOTMODE Timing Requirements

see Figure 6-19

NO.			MIN	MAX	UNIT
RST32	$t_{su(MCU\_BOOTMODE-MCU\_PORz\_OUT)}$	Setup time, MCU_BOOTMODE[09:00] before MCU_PORz_OUT high	3*S(1)		ns
RST33	$t_{h(MCU\_PORz\_OUT - MCU\_BOOTMODE)}$	Hold time, MCU_BOOTMODE[09:00] after MCU_PORz_OUT high	0		ns

(1) S = MCU_OSC0_XI/XO clock period.

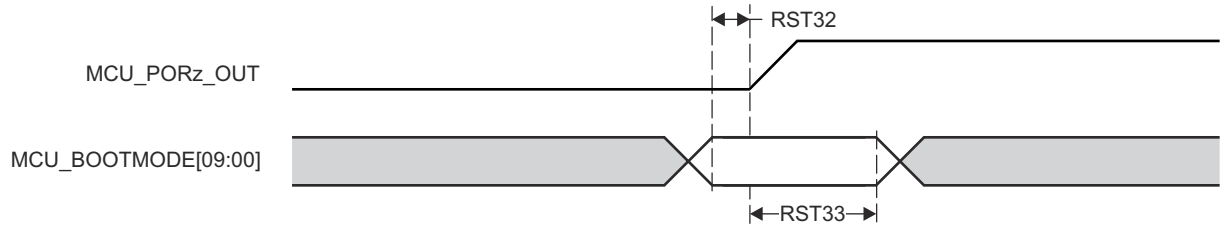


Figure 6-19. MCU_BOOTMODE Timing Requirements

Table 6-16. BOOTMODE Timing Requirements

see Figure 6-20

NO.			MIN	MAX	UNIT
RST34	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[7:0] before PORz_OUT high	3*S(1)		ns
RST35	$t_{h(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[7:0] after PORz_OUT high	0		ns

(1) S = MCU_OSC0_XI/XO clock period.

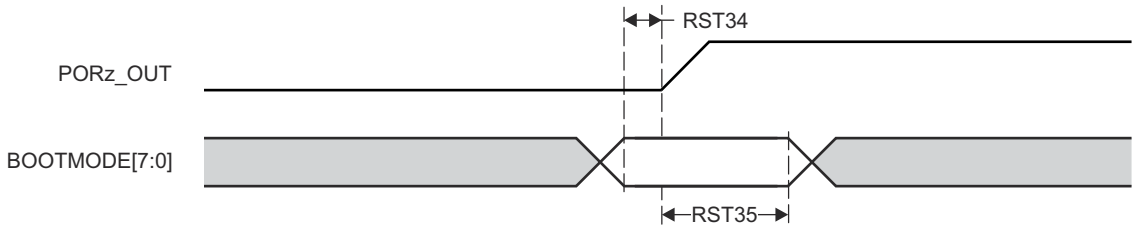


Figure 6-20. BOOTMODE Timing Requirements

6.10.3.2 Safety Signal Timing

Tables and figures provided in this section define timing conditions, switching characteristics for MCU_SAFETY_ERRORn and SOC_SAFETY_ERRORn.

Table 6-17. Error Signal Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	30	pF

Table 6-18. MCU_SAFETY_ERRORn Switching Characteristics

see Figure 6-21

NO.	PARAMETER		MIN	MAX	UNIT
SFTY1	$t_{w(MCU\_SAFETY\_ERRORn)}$	Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)	P*R(1) (2)		ns
SFTY2	$t_{d\ (ERROR\_CONDITION-MCU\_SAFETY\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active	50*P(1)		ns

(1) P = ESM functional clock (MCU_SYSCLK0 /6).
(2) R = Error Pin Counter Pre-Load Register count value.

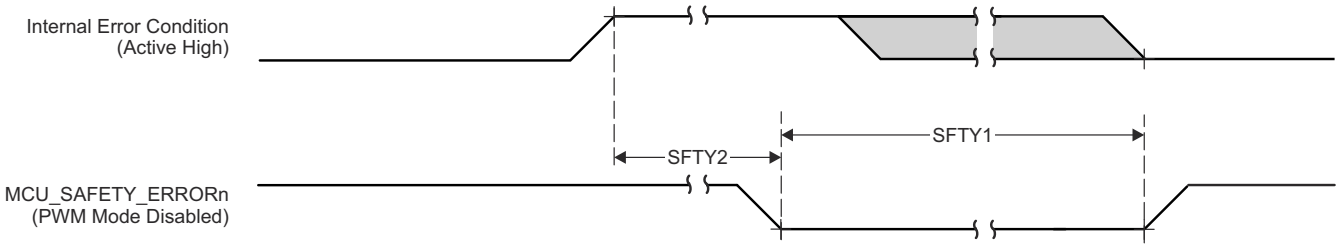


Figure 6-21. MCU_SAFETY_ERRORn Switching Characteristics

Table 6-19. SOC_SAFETY_ERRORn Switching Characteristics

see Figure 6-22

NO.	PARAMETER		MIN	MAX	UNIT
SFTY3	$t_{w(SOC\_SAFETY\_ERRORn)}$	Pulse width minimum,SOC_SAFETY_ERRORn active (PWM mode disabled)	P*R(1) (2)		ns
SFTY4	$t_{d\ (ERROR\_CONDITION-SOC\_SAFETY\_ERRORnL)}$	Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active	50*P(1)		ns

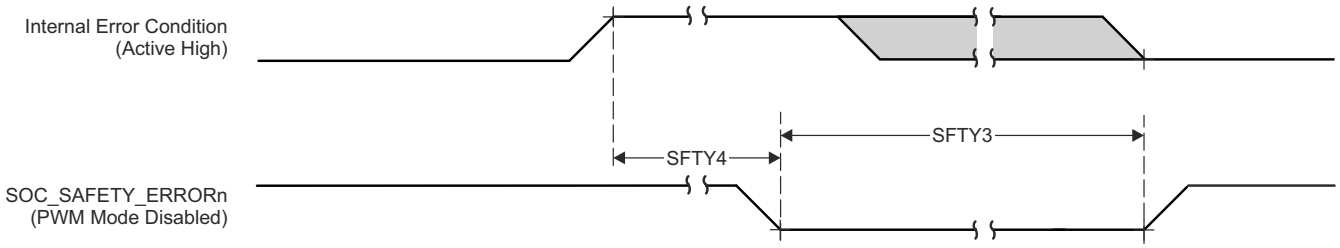


Figure 6-22. SOC_SAFETY_ERRORn Switching Characteristics

6.10.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

Table 6-20. Clock Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	30	pF

Table 6-21. Clock Timng Requiements

see Figure 6-23

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration minimum, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration minimum, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns

(1) E = EXT_REFCLK1 cycle time.

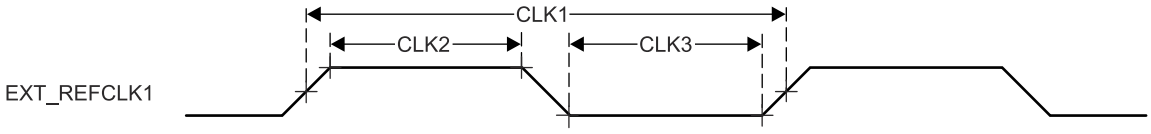


Figure 6-23. Clock Timing Requirements

Table 6-22. Clock Switching Characteristics

see Figure 6-24

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration minimum, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration minimum, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK7	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK8	$t_{w(OBSCLK0H)}$	Pulse Duration minimum, OBSCLK0 high	B*0.4(2)	B*0.6(2)	ns
CLK9	$t_{w(OBSCLK0L)}$	Pulse Duration minimum,OBSCLK0 low	B*0.4(2)	B*0.6(2)	ns
CLK10	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK11	$t_{w(CLKOUT0H)}$	Pulse Duration minimum, CLKOUT0 high	C*0.4(3)	C*0.6(3)	ns
CLK12	$t_{w(CLKOUT0L)}$	Pulse Duration minimum,CLKOUT0 low	C*0.4(3)	C*0.6(3)	ns

(1) A = SYSCLKOUT0 cycle time.
(2) B = OBSCLK0 cycle time.
(3) C = CLKOUT0 cycle time.

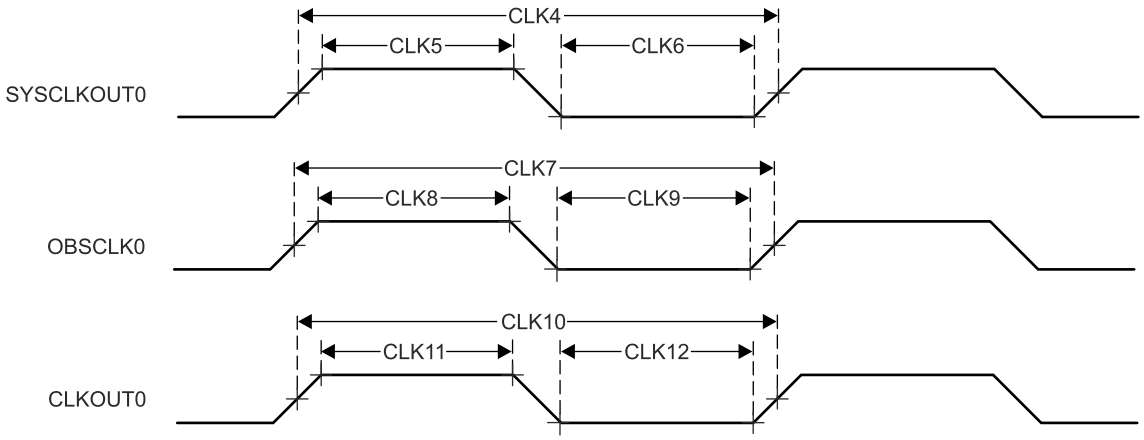


Figure 6-24. Clock Switching Characteristics

6.10.4 Clock Specifications

6.10.4.1 Input and Output Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators inputs
  - OSC1_XO/OSC1_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within MCU domain and MAIN domain. This high-frequency oscillator is used to provide audio clock frequencies to MCASPs.
  - WKUP_OSC0_XO/WKUP_OSC0_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within WKUP and MAIN domain.
- Low frequency digital input
  - WKUP_LF_CLKIN - Low Frequency 32k digital clock input, optionally sourced from an external PMIC or other clock source. This SoC does not support a LFOSC crystal input.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 - optional external System clock input (MCU domain).
  - EXT_REFCLK1 — optional external System clock input (MAIN domain).
- Peripheral clocks - refer to the Signal Descriptions for peripheral specific clocks

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

6.10.4.1.1 WKUP_OSC0 Internal Oscillator Clock Source

Figure 6-25 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the WKUP_OSC0_XI and WKUP_OSC0_XO pins.

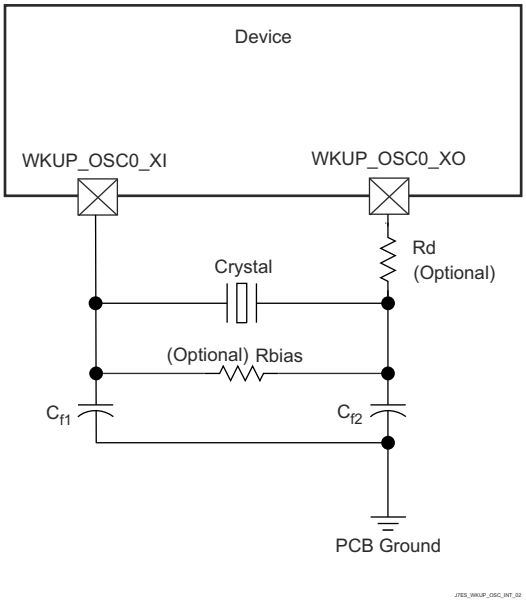


Figure 6-25. WKUP_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-23 summarizes the required electrical constraints.

Table 6-23. WKUP_OSC0 Crystal Electrical Characteristics

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				19.2, 20, 24, 25, 26, 27		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	19.2 MHz, 20MHz	ESR_{xtal} ≤ 30 Ω			7	pF
			30 Ω < ESR_{xtal} ≤ 80 Ω			5	pF
			80 Ω < ESR_{xtal} ≤ 100 Ω			3	pF
		24MHz	ESR_{xtal} ≤ 30 Ω			7	pF
			30 Ω < ESR_{xtal} ≤ 60 Ω			5	pF
			60 Ω < ESR_{xtal} ≤ 80 Ω			3	pF
			Not Supported: 80 Ω ≤ ESR_{xtal}			–	
		25MHz	ESR_{xtal} ≤ 30 Ω			7	pF
			30 Ω < ESR_{xtal} ≤ 50 Ω			5	pF
			50 Ω < ESR_{xtal} ≤ 80 Ω			3	pF
			Not Supported: 80 Ω ≤ ESR_{xtal}			–	
		26 MHz, 27 MHz	ESR_{xtal} ≤ 30 Ω			7	pF
			30 Ω < ESR_{xtal} ≤ 50 Ω			5	pF
			Not Supported: 50 Ω ≤ ESR_{xtal}			–	
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-24 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-24. WKUP_OSC0 Switching Characteristics – Crystal Mode

PARAMETER		PACKAGE	MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance	AND			2.047	pF
C_{XO}	XO Capacitance	AND			1.972	pF
C_{XIXO}	XI to XO Mutual Capacitance	AND			0.01	pF
t_s	Start-up Time			9.5(1)		ms

(1) **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.**

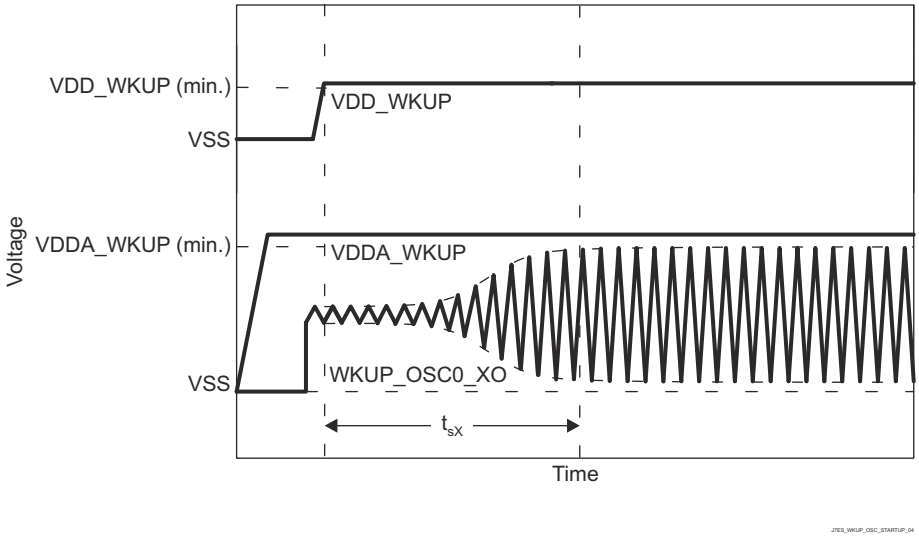


Figure 6-26. WKUP_OSC0 Start-up Time

6.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP_OSC0_XI and WKUP_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The WKUP_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in Table 6-24.

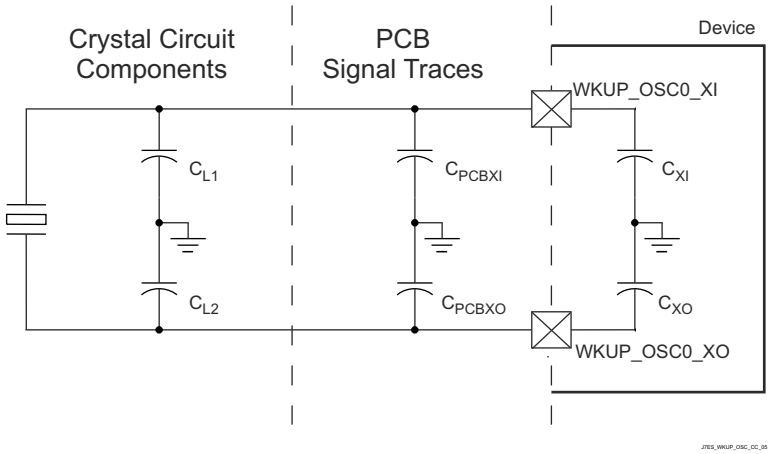


Figure 6-27. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in Figure 6-25, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 × 10 pF) - 2.9 pF - 0.5 pF)] = 16.6 pF and C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 × 10 pF) - 3.7 pF - 0.5 pF)] = 15.8 pF

6.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for WKUP_OSC0 operating conditions defined in Table 6-23. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in Table 6-24.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

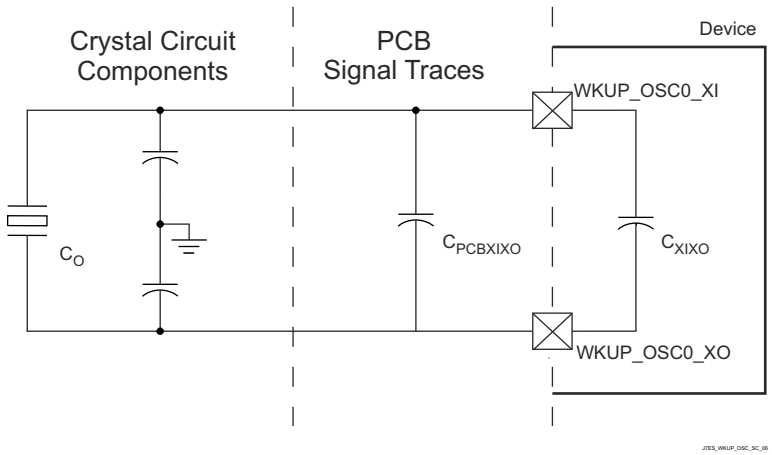


Figure 6-28. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

6.10.4.1.2 WKUP_OSC0 LVCMOS Digital Clock Source

Figure 6-29 shows the recommended oscillator connections when WKUP_OSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

Note

A DC steady-state condition is not allowed on WKUP_OSC0_XI when the oscillator is powered up. This is not allowed because WKUP_OSC0_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down WKUP_OSC0 any time WKUP_OSC0_XI is not toggling between logic states.

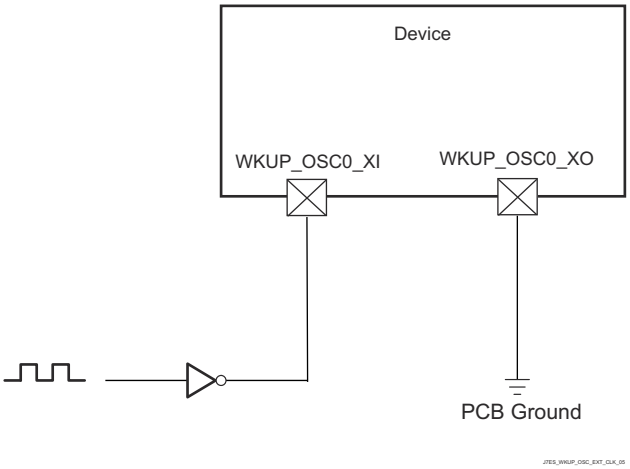


Figure 6-29. 1.8-V LVCMOS-Compatible Clock Input

6.10.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source

Figure 6-30 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the OSC1_XI and OSC1_XO pins.

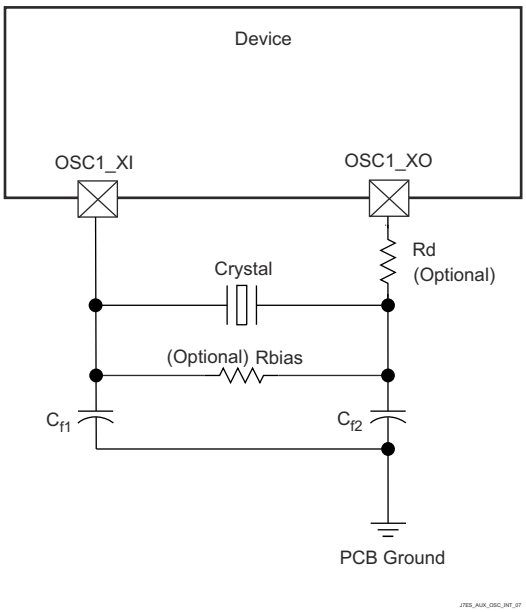


Figure 6-30. OSC1 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-25 summarizes the required electrical constraints.

Table 6-25. OSC1 Crystal Electrical Characteristics

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency			19.2		27	MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	19.2MHz < F_{xtal} ≤ 20MHz	ESR_{xtal} ≤ 30Ω			7	pF
			30Ω < ESR_{xtal} ≤ 80Ω			5	pF
			80Ω < ESR_{xtal} ≤ 100Ω			3	pF
		20MHz < F_{xtal} ≤ 24.576MHz	ESR_{xtal} ≤ 30Ω			7	pF
			30Ω ≤ ESR_{xtal} ≤ 60Ω			5	pF
			60Ω < ESR_{xtal} ≤ 80Ω			3	pF
			Not Supported: 80Ω ≤ ESR_{xtal}			–	
		24.576MHz < F_{xtal} ≤ 25MHz	ESR_{xtal} ≤ 30Ω			7	pF
			30Ω < ESR_{xtal} ≤ 50Ω			5	pF
			50Ω < ESR_{xtal} ≤ 80Ω			3	pF
			Not Supported: 80Ω ≤ ESR_{xtal}			–	
		25MHz < F_{xtal} ≤ 27MHz	ESR_{xtal} ≤ 30Ω			7	pF
			30Ω < ESR_{xtal} ≤ 50Ω			5	pF
			Not Supported: 50Ω ≤ ESR_{xtal}			–	
ESR_{xtal}	Crystal Effective Series Resistance					100	Ω

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-26 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 6-26. OSC1 Switching Characteristics – Crystal Mode

PARAMETER		PACKAGE	MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance	AND			2.548	pF
C_{XO}	XO Capacitance	AND			2.878	pF
C_{XIXO}	XI to XO Mutual Capacitance	AND			0.01	pF
t_s	Start-up Time			9.5(1)		ms

(1) **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.**

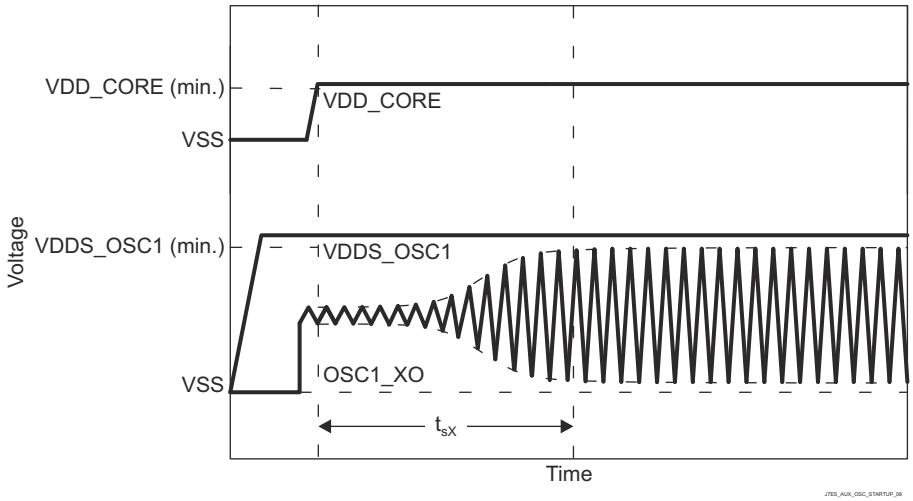


Figure 6-31. OSC1 Start-up Time

6.10.4.1.3.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1_XI and OSC1_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The OSC1 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in Table 6-26.

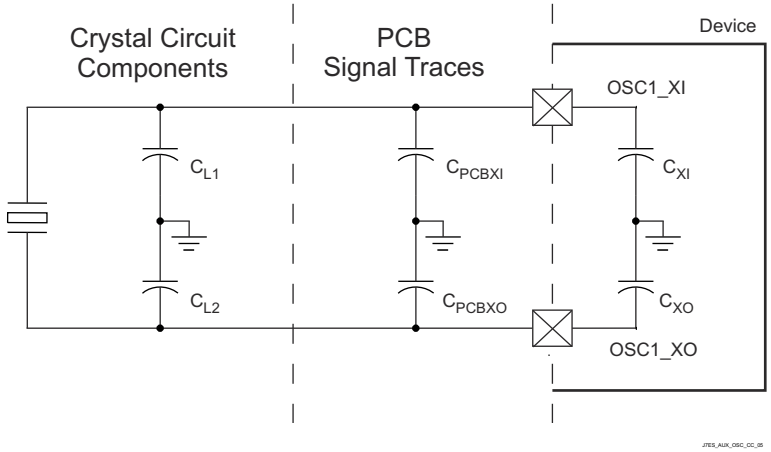


Figure 6-32. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in Figure 6-30, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 × 10 pF) - 2.9 pF - 0.5 pF)] = 16.6 pF and C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 × 10 pF) - 3.7 pF - 0.5 pF)] = 15.8 pF

6.10.4.1.3.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for OSC1 operating conditions defined in Table 6-25. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in Table 6-26.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

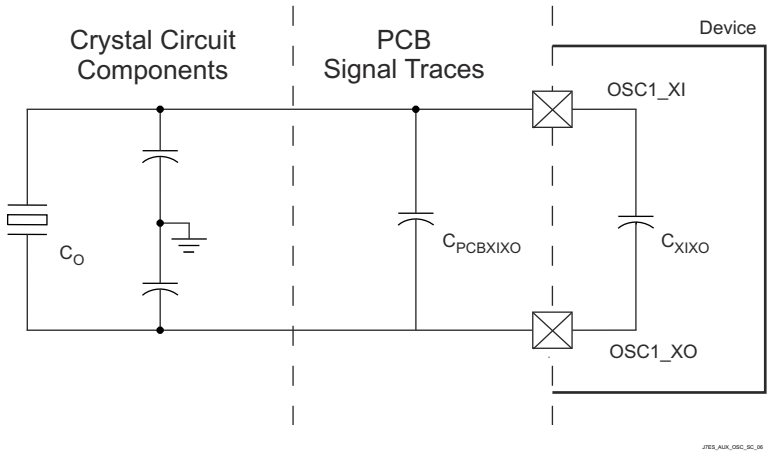


Figure 6-33. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

6.10.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

Figure 6-34 shows the recommended oscillator connections when OSC1 is connected to a 1.8-V LVCMOS square-wave digital clock source.

Note

A DC steady-state condition is not allowed on OSC1_XI when the oscillator is powered up. This is not allowed because OSC1_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down OSC1 any time OSC1_XI is not toggling between logic states.

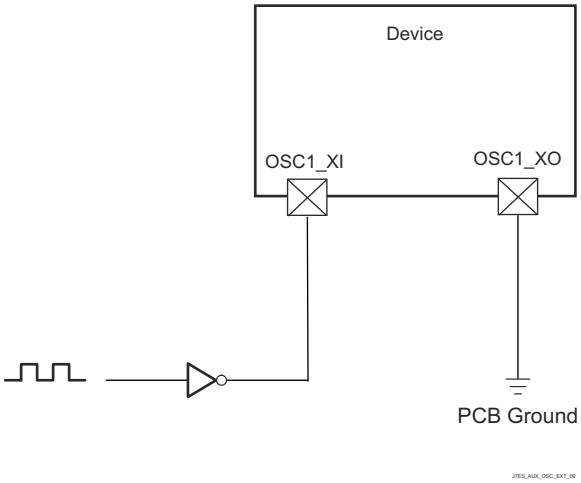


Figure 6-34. 1.8-V LVCMOS-Compatible Clock Input

6.10.4.1.5 Auxiliary OSC1 Not Used

Figure 6-35 shows the recommended oscillator connections when OSC1 is not used. OSC1_XI must be connected to VSS through an external pull resistor (R_{pd}) to ensure this input is held to a valid low level when unused since the internal pull-down resistor is disabled by default.

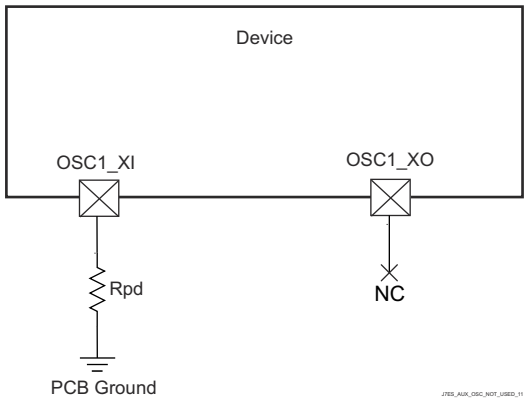


Figure 6-35. OSC1 Not Used

6.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_CLKOUT0**
  - Reference clock output for Ethernet PHYs (50 MHz or 25 MHz)
- **MCU_SYSCLKOUT0**
  - MCU_SYSCLK0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (MCU_SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.
- **MCU_OBSCLK0**
  - On the clock output MCU_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug. This signal should not be used as a clock source for external devices on a board.
- **SYSCLKOUT0**
  - SYSCLK0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.
- **CLKOUT**

  - Reference clock output for Ethernet PHYs (50 MHz)
- **OBSCLK[1:0]**
  - On the clock output OBSCLK0/1, oscillators and PLLs clocks can be observed for tests and debug.

6.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuitries (PLLs) by internal regulators that derive power from the off-chip power-supply.

There are total of three PLLs in the device in WKUP and MCU domains:

- MCU_PLL0 (MCU R5FSS PLL) with WKUP_PLLCTRL0
- MCU_PLL1 (MCU PERIPHERAL PLL)
- MCU_PLL2 (MCU CPSW PLL)

There are total of twenty PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL3 (CPSW9G PLL)
- PLL4 (AUDIO0 PLL)
- PLL5 (VIDEO PLL)
- PLL6 (GPU PLL)
- PLL7 (C7x PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL13 (C66 PLL)
- PLL14 (R5F PLL)
- PLL15 (AUDIO1 PLL)
- PLL16 (DSS PLL0)
- PLL17 (DSS PLL1)
- PLL18 (DSS PLL2)
- PLL19 (DSS PLL3)
- PLL23 (DSS PLL7)
- PLL24 (MLB PLL)
- PLL25 (VISION PLL)

Note

For more information, see:

- *Device Configuration* / *Clocking* / *PLLs* section in the device TRM.
- *Peripherals* / *Display Subsystem* Overview section in the device TRM.

Note

The input reference clock (OSC1_XI/OSC1_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

6.10.4.4 Module and Peripheral Clocks Frequencies

Section 6.10.5, *Peripherals* section documents the maximum frequency associated with the peripheral clocks of the device.

For more details on the clocking structure of each module, reference *Device Configurations* chapter in the device TRM.

6.10.5 Peripherals

6.10.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

Note

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

Table 6-27 represents ATL timing conditions.

Table 6-27. ATL Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	External reference CLK	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	Internal reference CLK	1	10	pF

Section 6.10.5.1.1, Section 6.10.5.1.2, Section 6.10.5.1.3, and Section 6.10.5.1.4 present timing requirements and switching characteristics for ATL.

6.10.5.1.1 ATL_PCLK Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, ATL_PCLK	External reference CLK	5		ns
D2	$t_{w(pclkL)}$	Pulse Duration, ATL_PCLK low	External reference CLK	0.45 × M (1) + 2.5		ns
D3	$t_{w(pclkH)}$	Pulse Duration, ATL_PCLK high	External reference CLK	0.45 × M (1) + 2.5		ns

(1) M = ATL_CLK[x] period

6.10.5.1.2 ATL_AWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D4	$t_{c(aws)}$	Cycle Time, ATL_AWS[x](3)	External reference CLK	2 × M(1)		ns
D5	$t_{w(awsL)}$	Pulse Duration, ATL_AWS[x](3) low	External reference CLK	0.45 × A(2) + 2.5		ns
D6	$t_{w(awsH)}$	Pulse Duration, ATL_AWS[x](3) high	External reference CLK	0.45 × A(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) A = ATL_AWS[x] period
(3) x = 0 to 3

6.10.5.1.3 ATL_BWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D7	$t_{c(bws)}$	Cycle Time, ATL_BWS[x](3)	External reference clock	2 × M(1)		ns
D8	$t_{w(bwsL)}$	Pulse Duration, ATL_BWS[x] low(3)	External reference clock	0.45 × B(2) + 2.5		ns

NO.			MODE	MIN	MAX	UNIT
D9	$t_{w(bwsH)}$	Pulse Duration, ATL_BWS[x] high(3)	External reference clock	0.45 × B(2) + 2.5		ns

(1) M = ATL_CLK[x] period
(2) B = ATL_BWS[x] period
(3) x = 0 to 3

6.10.5.1.4 ATCLK[x] Switching Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D10	$t_{c(atclk)}$	Cycle time, ATCLK[x](3)	Internal reference CLK	20		ns
D11	$t_{w(atclkL)}$	Pulse Duration, ATCLK[x] low(3)	Internal reference CLK	0.45 × P(2) - M(1) - 0.3		ns
D12	$t_{w(atclkH)}$	Pulse Duration, ATCLK[x] high(3)	Internal reference CLK	0.45 × P(2) - M(1) - 0.3		ns

(1) M = ATL_CLK[x] period
(2) P = ATCLK[x] period
(3) x = 0 to 3

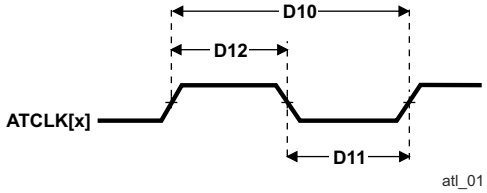


Figure 6-36. ATCLK[x] Timing

6.10.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within Signal Descriptions and *Detailed Description*.

6.10.5.2.1 CPSW2G MDIO Interface Timings

Table 6-28 represents CPSW2G timing conditions.

Table 6-28. CPSW2G MDIO Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input signal slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

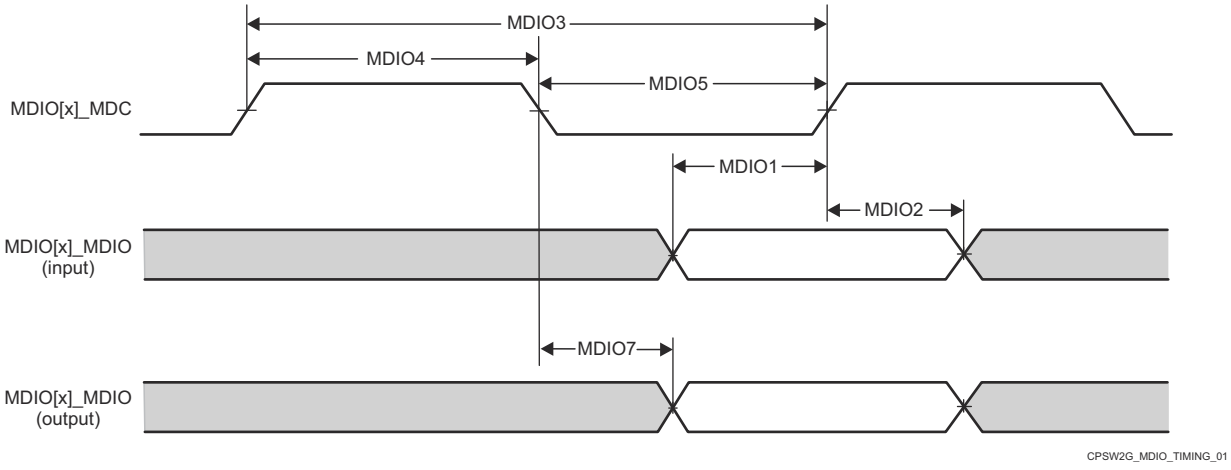
Table 6-29, Table 6-30, and Figure 6-37 present timing requirements for MDIO.

Table 6-29. CPSW2G MDIO Timing Requirements

NO.			MIN	MAX	UNIT
MDIO1	$t_{su(mdioV-mdcH)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(mdcH-mdioV)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

Table 6-30. CPSW2G MDIO Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(mdc)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(mdcH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(mdcL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(mdcL-mdioV)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	–150	150	ns



Note

x = 0 in MCU domain

Figure 6-37. CPSW2G MDIO Timing Requirements and Switching Characteristics

6.10.5.2.2 CPSW2G RMII Timings

Table 6-31, Section 6.10.5.2.2.1, Section 6.10.5.2.2.2, and Section 6.10.5.2.2.3 present timing conditions, requirements, and switching characteristics for CPSW2G RMII.

Table 6-31. CPSW2G RMII Timing Conditions

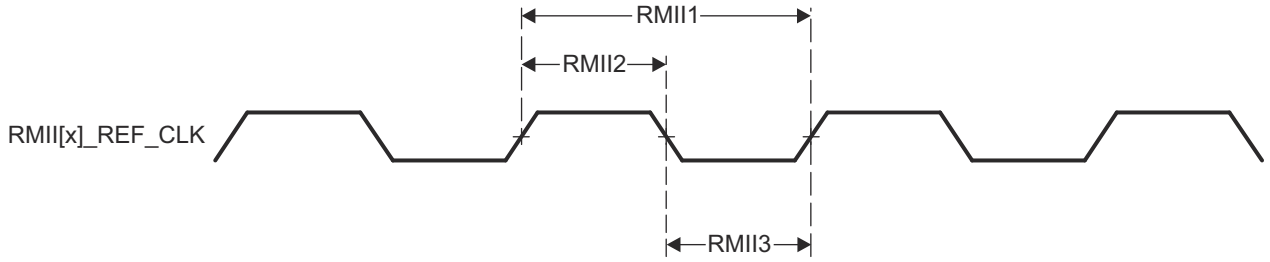
PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input signal slew rate	VDD(1) = 1.8 V	0.108	0.54	V/ns
		VDD(1) = 3.3 V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the Pin Attributes

6.10.5.2.2.1 CPSW2G RMII[x]_REF_CLK Timing Requirements – RMII Mode

see Figure 6-38

NO.			MIN	MAX	UNIT
RMII1	$t_{c(ref\_clk)}$	Cycle time, RMII[x]_REF_CLK	19.999	20	ns
RMII2	$t_{w(ref\_clkH)}$	Pulse Duration, RMII[x]_REF_CLK high	7	13	ns
RMII3	$t_{w(ref\_clkL)}$	Pulse Duration, RMII[x]_REF_CLK low	7	13	ns



A. x = 1 in MCU domain.

Figure 6-38. CPSW2G RMII[x]_REFCLK Timing Requirements – RMII Mode

6.10.5.2.2.2 CPSW2G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

NO.			MIN	MAX	UNIT
RMII4	$t_{su(rxdV-ref\_clkH)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK rising edge	4		ns
	$t_{su(crs\_dvV-ref\_clkH)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK rising edge	4		ns
	$t_{su(rx\_erV-ref\_clkH)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK rising edge	4		ns
RMII5	$t_{h(ref\_clkH-rxdV)}$	Hold time, RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK rising edge	2		ns
	$t_{h(ref\_clkH-crs\_dvV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK rising edge	2		ns
	$t_{h(ref\_clkH-rx\_erV)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK rising edge	2		ns

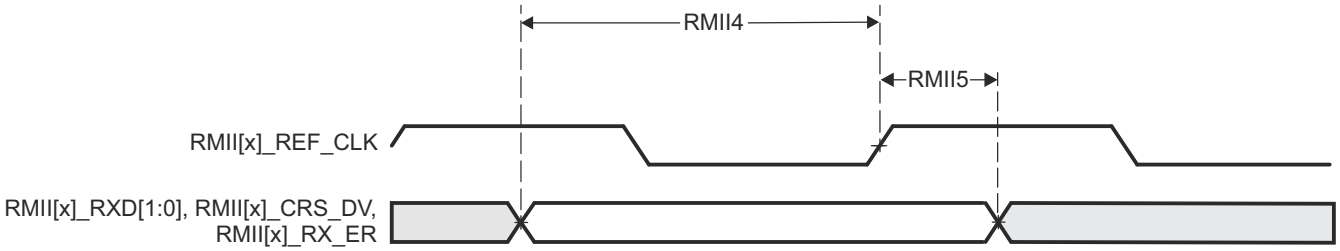


Figure 6-39. CPSW2G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

Section 6.10.5.2.2.3, and Figure 6-40 present switching characteristics for CPSW2G RMII Transmit.

6.10.5.2.2.3 CPSW2G RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see Figure 6-40

NO.	PARAMETER		MIN	MAX	UNIT
RMII6	$t_{d(ref\_clkH-txdV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(ref\_clkH-tx\_enV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TX_EN valid	2	10	ns

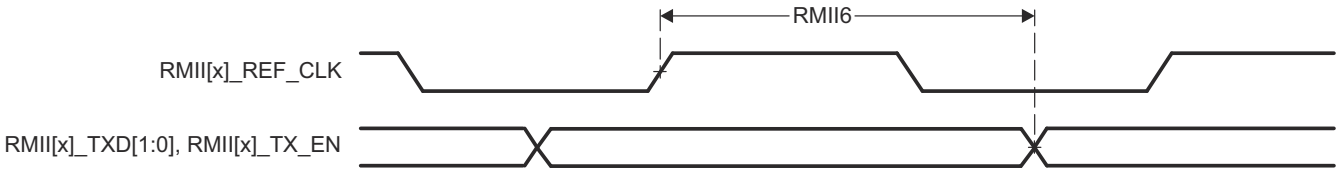


Figure 6-40. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

6.10.5.2.3 CPSW2G RGMII Timings

Section 6.10.5.2.3.1, Section 6.10.5.2.3.2, and Figure 6-42 present timing requirements for receive RGMII operation.

For more information, see *Gigabit Ethernet MAC (MCU_CPSW0)* section in *Peripherals* chapter in the device TRM.

Table 6-32. CPSW2G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8 V	1.44	5	V/ns
		VDD(1) = 3.3 V	2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the Pin Attributes.

6.10.5.2.3.1 RGMII[x]_RXC Timing Requirements – RGMII Mode

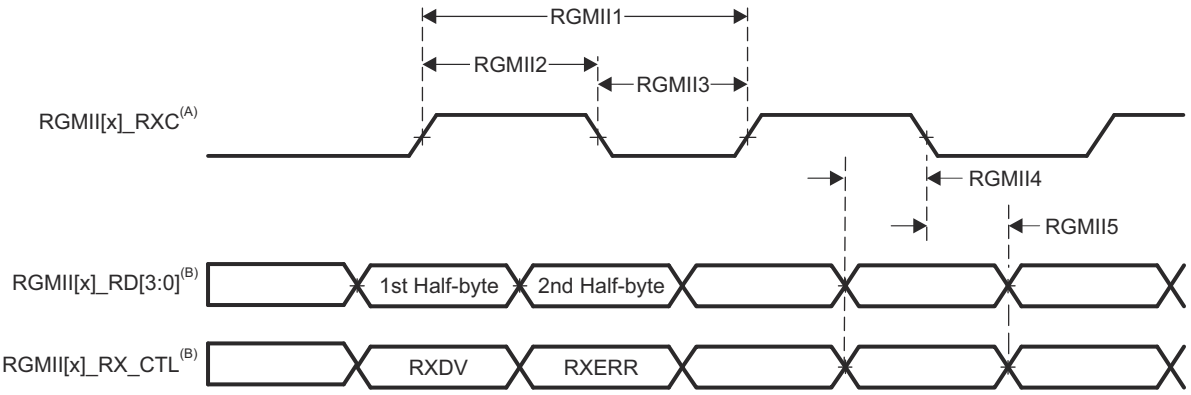
see Figure 6-41

NO.			MODE	MIN	MAX	UNIT
RGMII1	$t_{c(rxc)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(rxcH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(rxcL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.10.5.2.3.2 CPSW2G Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL – RGMII Mode

see Figure 6-41

NO.			MODE	MIN	MAX	UNIT
RGMII4	$t_{su(rdV-rxcV)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(rx\_ctlV-rxcV)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(rxcV-rdV)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(rxcV-rx\_ctlV)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII_RXC must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII_RXC and data bits 7-4 on the falling edge of RGMII_RXC. Similarly, RGMII_RXCTL carries RXDV on rising edge of RGMII_RXC and RXERR on falling edge of RGMII_RXC.

Figure 6-41. CPSW2G Receive Interface Timing, RGMII Operation

Section 6.10.5.2.3.3, Section 6.10.5.2.3.4 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

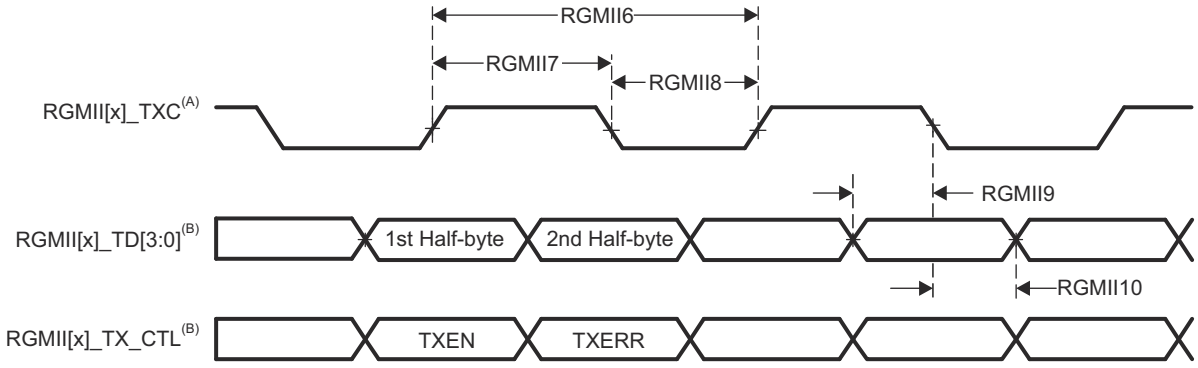
6.10.5.2.3.3 CPSW2G RGMII[x]_TXC Switching Characteristics – RGMII Mode

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RGMII6	$t_{c(txc)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(txcH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(txcL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.10.5.2.3.4 RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see Figure 6-42

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(tdV-txcV)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(tx\_ctlV-txcV)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(tdV-txcV)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(tx\_ctlV-txcV)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.
B. Data and control information is received using both edges of the clocks. RGMII_TD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TX_CTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

Figure 6-42. CPSW2G Transmit Interface Timing RGMII Mode

6.10.5.3 CSI-2

Note

For more information, see the Camera Streaming Interface Receiver (CSI_RX_IF) chapter in the device TRM.

The CSI_RX_IF deals with the processing of the pixel data coming from an external image sensor and data from memory. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The CSI_RX_IF has a primary serial interface (CSI-2 port) compliant with the MIPI D-PHY RX specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane in synchronous mode, double data rate. Refer to the specification for timing details.

- 2.5 Gbps (1.25 GHz) for each lane.

6.10.5.4 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interfaces, see the corresponding sections within Signal Descriptions and *Detailed Description*.

The device has dedicated interface to LPDDR4. It supports JEDEC JESD209-4B standard compliant LPDDR4 SDRAM devices with the following features:

- 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 8GB address space available over two chip selects (4GB per rank)
- No support for byte mode LPDDR4 memories, or memories with more than 17 row address bits

Table 6-33 and Figure 6-43 present switching characteristics for DDRSS.

Table 6-33. Switching Characteristics for DDRSS

NO.	PARAMETER		DDR TYPE	MIN	MAX	UNIT
1	$t_{c(DDR\_CKP/DDR\_CKN)}$	Cycle time, DDR0_CKP and DDR0_CKN	LPDDR4	0.4681	3.003	ns

1. Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the Jacinto 7 DDR Board Design and Layout Guidelines for details.

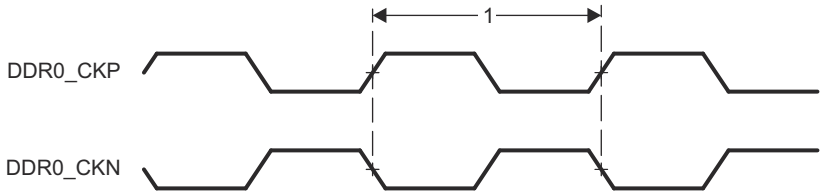


Figure 6-43. DDRSS Memory Interface Clock Timing

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

6.10.5.5 DSS

For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-34 represents DPI timing conditions.

Table 6-34. DPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.44	26.4	V/ns

Table 6-34. DPI Timing Conditions (continued)

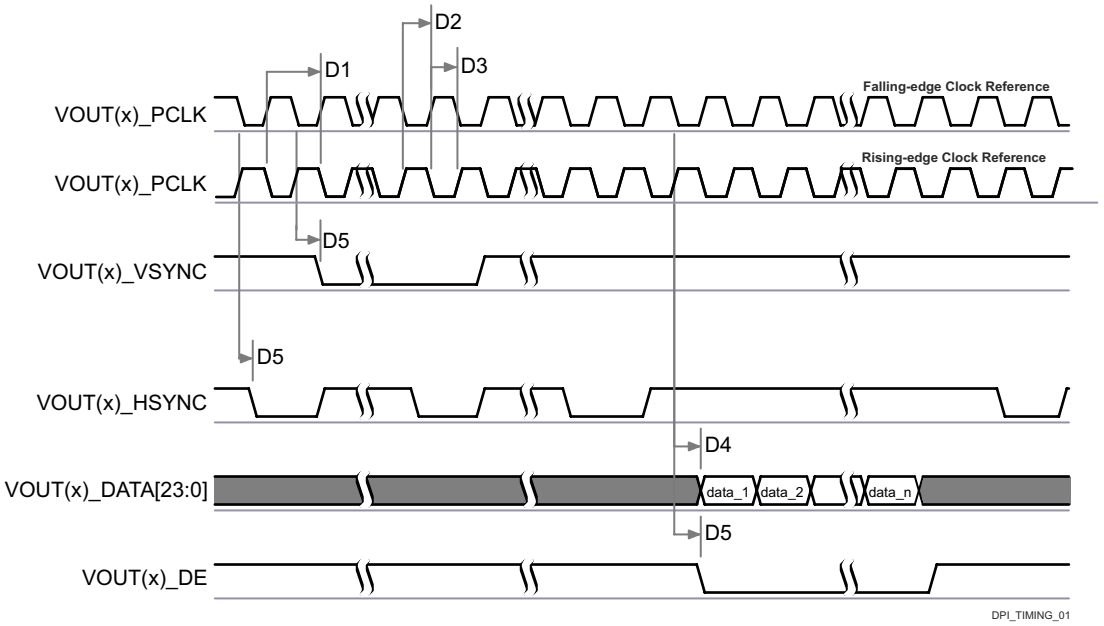
PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

Table 6-35, Table 6-36, Figure 6-44 and Figure 6-45 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-35. DPI Video Output Switching Characteristics

NO.(2)	PARAMETER		MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, VOUT(x)_PCLK	6.06		ns
D2	$t_{w(pclkL)}$	Pulse duration, VOUT(x)_PCLK low	0.475×P(1)		ns
D3	$t_{w(pclkH)}$	Pulse duration, VOUT(x)_PCLK high	0.475×P(1)		ns
D4	$t_{d(pclkV\text{-}dataV)}$	Delay time, VOUT(x)_PCLK transition to VOUT(x)_DATA[23:0] transition	-0.68	1.78	ns
D5	$t_{d(pclkV\text{-}ctrlL)}$	Delay time, VOUT(x)_PCLK transition to control signals VOUT(x)_VSYNC, VOUT(x)_HSYNC, VOUT(x)_DE falling edge	-0.68	1.78	ns

(1) P = output VOUT(x)_PCLK period in ns.
(2) x in VOUT(x) = 1 or 2



A. The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
B. The polarity and the pulse width of VOUT(x)_HSYNC and VOUT(x)_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
C. The VOUT(x)_PCLK frequency can be configured, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.
D. x in VOUT(x) = 1 or 2.

Figure 6-44. DPI Video Output

Table 6-36. DPI External Pixel Clock Timing Requirements

NO.(2)			MIN	MAX	UNIT
D6	$t_{c(extpclkin)}$	Cycle time, VOUT(x)_EXTPCLKIN	6.06		ns
D7	$t_{w(extpclkinL)}$	Pulse duration, VOUT(x)_EXTPCLKIN low	0.45×P (1)		ns
D8	$t_{w(extpclkinH)}$	Pulse duration, VOUT(x)_EXTPCLKIN high	0.45×P (1)		ns

(1) P = output VOUT(x)_PCLK period in ns.
(2) x in VOUT(x) = 1 or 2

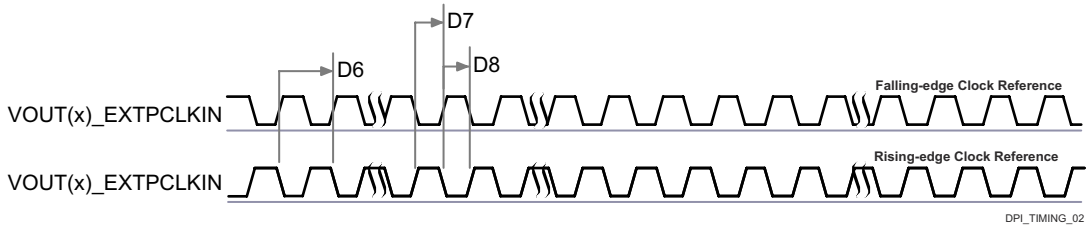


Figure 6-45. DPI External Pixel Clock Input

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

6.10.5.6 eCAP

The supported features by the device ECAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

Table 6-37 represents ECAP timing conditions.

Table 6-37. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Section 6.10.5.6.1 and Section 6.10.5.6.2 present timing and switching characteristics for eCAP (see Figure 6-46 and Figure 6-47).

6.10.5.6.1 Timing Requirements for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(cap)}$	Pulse duration, CAP (asynchronous)	2 + 2P(1)		ns

(1) P = sysclk

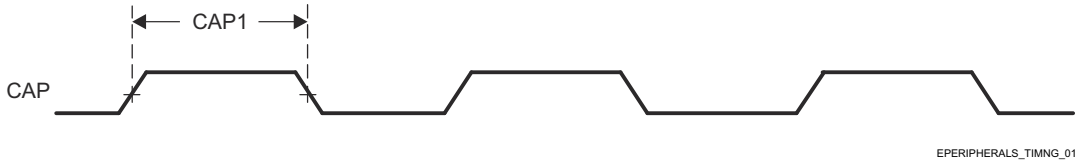


Figure 6-46. eCAP Input Timings

6.10.5.6.2 Switching Characteristics for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(apwm)}$	Pulse duration, APWM	–2 + 2P(1)		ns

(1) P = sysclk

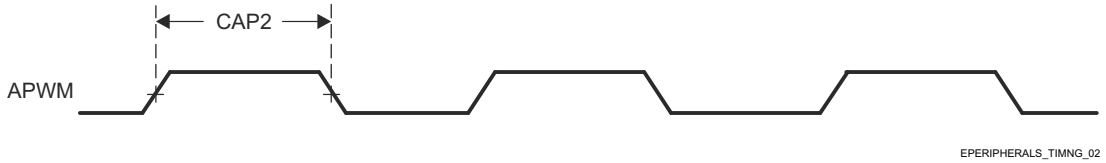


Figure 6-47. eCAP Output Timings

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

6.10.5.7 EPWM

The supported features by the device EPWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

Table 6-38 represents EPWM timing conditions.

Table 6-38. EPWM Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Section 6.10.5.7.2, Section 6.10.5.7.1 and present timing and switching characteristics for eHRPWM (see Figure 6-49, Figure 6-50, Figure 6-51, and Figure 6-48).

6.10.5.7.1 Timing Requirements for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(synci)}$	Pulse duration, EHRPWM_SYNCI	2 + 2P(1)		ns
PWM7	$t_{w(tz)}$	Pulse duration, EHRPWM_TZn_IN low	2 + 3P(1)		ns

(1) P = sysclk

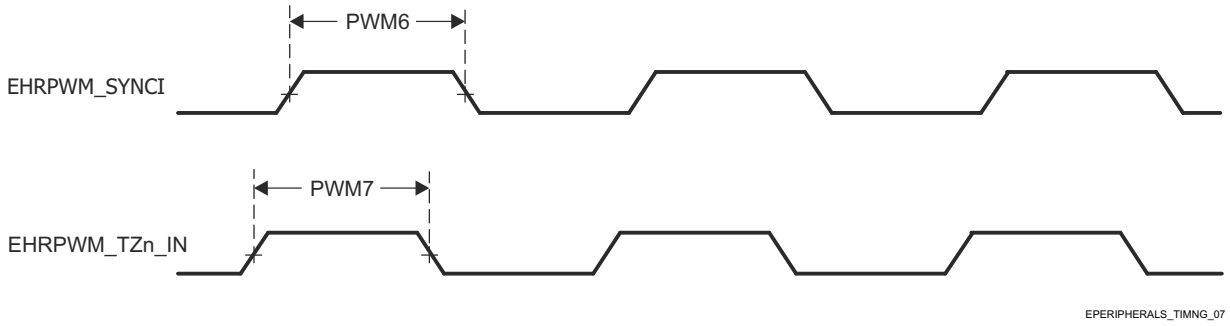


Figure 6-48. ePWM_SYNCI and ePWM_TZn_IN Output Timings

For more information, see *Camera Subsystem* section in *Peripherals* chapter in the device TRM.

6.10.5.7.2 Switching Characteristics for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(pwm)}$	Pulse duration, EHRPWM_A/B, high or low	P-3(1)		ns
PWM2	$t_{w(syncout)}$	Pulse duration, EHRPWM_SYNCO	P-3(1)		ns
PWM3	$t_{d(tzL-pwmV)}$	Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B valid		11	ns
PWM4	$t_{d(tzL-pwmZ)}$	Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B Hi-Z		11	ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM5	$t_{w(soc)}$	Pulse duration, EHRPWM_SOCA/B	P-3(1)		ns

(1) P = sysclk

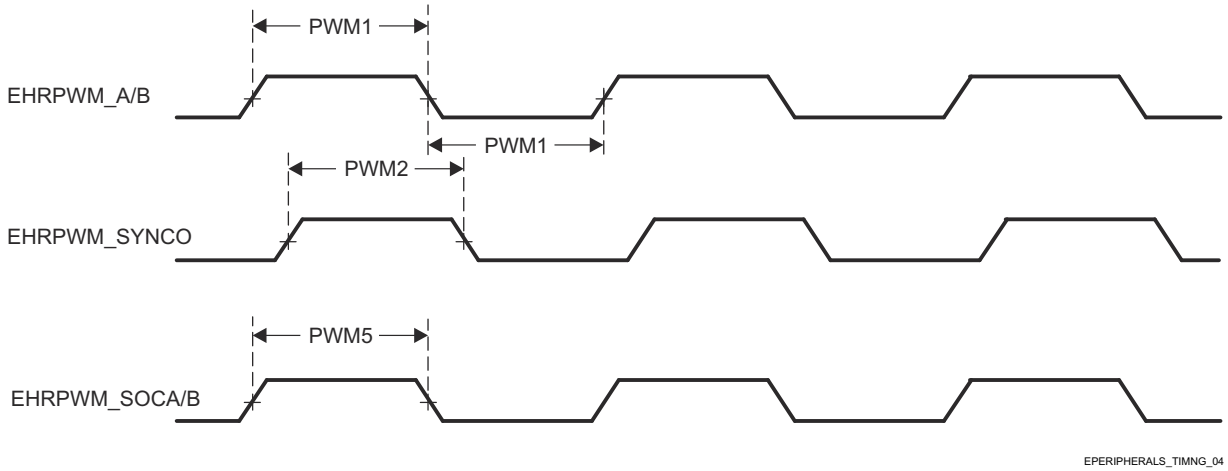


Figure 6-49. EPWM_A/B_out, ePWM_SYNCO, and ePWM_SOCA/B Input Timings

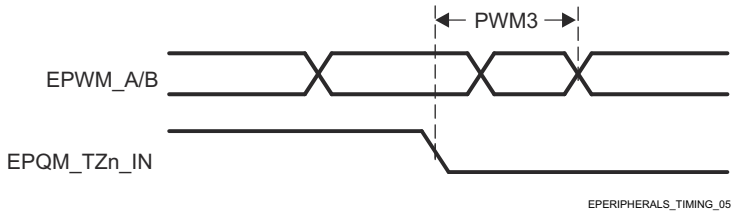


Figure 6-50. EPWM_A/B and ePWM_TZn_IN Forced High/Low Input Timings

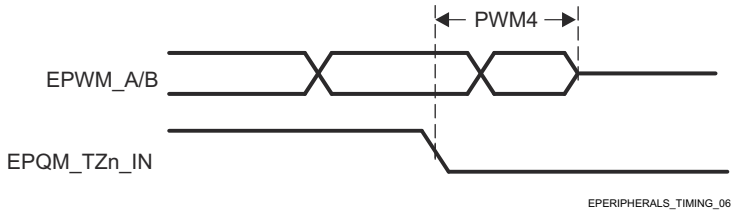


Figure 6-51. EPWM_A/B and ePWM_TZn_IN Hi–Z Input Timings

6.10.5.8 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

Table 6-39 represents EQEP timing conditions.

Table 6-39. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Section 6.10.5.8.1 and Section 6.10.5.8.2 present timing requirements and switching characteristics for eQEP (see Figure 6-52).

6.10.5.8.1 Timing Requirements for eQEP

NO.			MIN	MAX	UNIT
QEP1	$t_{w(qep)}$	Pulse duration, QEP_A/B	2 + 2P(1)		ns
QEP2	$t_{w(qepiH)}$	Pulse duration, QEP_I high	2 + 2P(1)		ns
QEP3	$t_{w(qepiL)}$	Pulse duration, QEP_I low	2 + 2P(1)		ns
QEP4	$t_{w(qepsH)}$	Pulse duration, QEP_S high	2 + 2P(1)		ns
QEP5	$t_{w(qepsL)}$	Pulse duration, QEP_S low	2 + 2P(1)		ns

(1) P = sysclk

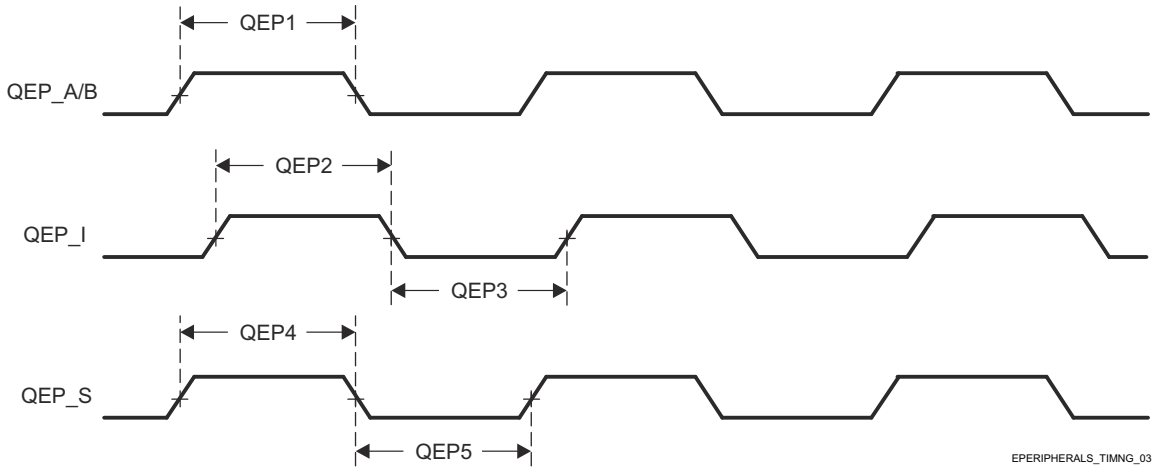


Figure 6-52. eQEP Input Timings

6.10.5.8.2 Switching Characteristics for eQEP

NO.	PARAMETER		MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

6.10.5.9 GPIO

For more details about features and additional description information on the device GPIO, see the device-specific Technical Reference Manual (TRM) and the corresponding sections within Signal Descriptions of this data sheet.

Table 6-40, Section 6.10.5.9.1, and Section 6.10.5.9.2 present timing conditions, requirements, and switching characteristics for GPIO.

Table 6-40. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	LVCMOS (VDD(1) = 1.8V)	0.0018	6.6	V/ns
		LVCMOS (VDD(1) = 3.3V)	0.0033	6.6	V/ns
		I2C OD FS (VDD(1) = 1.8V)	0.0018	6.6	V/ns
		I2C OD FS (VDD(1) = 3.3V)	0.0033	0.08	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the Pin Attributes table.

6.10.5.9.1 GPIO Timing Requirements

NO.			BUFFER TYPE	MIN	MAX	UNIT
GPIO1	$t_{w(gpio\_in)}$	Pulse width, GPIOn_x	1.8 V	2P + 2.6(1)		ns
			3.3 V	2P + 3.4(1)		ns

(1) P = functional clock period in ns.

6.10.5.9.2 GPIO Switching Characteristics

NO.	PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
GPIO3	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width	LVCMOS	–3.6 + 0.975P(1)		ns
GPIO4	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width Low	I2C Open Drain	160		ns
GPIO5	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width High	I2C Open Drain	60		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

6.10.5.10 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-41 represents GPMC timing conditions.

Note

The IO timings provided in this section are applicable for all combinations of signals for GPMC0. However, the timings are only valid for GPMC0 if signals within a single IOSET are used. The IOSETs are defined in the GPMC0_IOSET, *GPMC0_IOSET* table.

Table 6-41. GPMC Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Input Conditions				
SR_I	Input slew rate	1.65	4	V/ns
Output Conditions				
C_L	Output load capacitance	5	20	pF
PCB Connectivity Requirements				

Table 6-41. GPMC Timing Conditions (continued)

PARAMETER	DESCRIPTION		MIN	MAX	UNIT
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation mismatch across all traces			200	ps

6.10.5.10.1 GPMC and NOR Flash — Synchronous Mode

Section 6.10.5.10.1.1 and Section 6.10.5.10.1.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-53 through Figure 6-57).

6.10.5.10.1.1 GPMC and NOR Flash Timing Requirements — Synchronous Mode

NO.	PARAMETER	DESCRIPTION[2]	MODE[3]	MIN MAX 100 MHz[4]	MIN MAX 133 MHz[4]	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81	1.11	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.78	2.28	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.78		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j] valid before output clock GPMC_CLK high[1]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81	1.11	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high[1]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.78	2.28	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.78		ns

(1) In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
(2) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.
(3) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100 MHz
- For TIMEPARAGRANULARITY_X1:
  - GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(4) For 100 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = MAIN_PLL2_HSDIV1_CLKOUT / 3

For 133 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT

6.10.5.10.1.2 GPMC and NOR Flash Switching Characteristics – Synchronous Mode

NO.[2]	PARAMETER	DESCRIPTION	MODE[19]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[20]		133 MHz[20]		
F0	tc(clk)	Period, output clock GPMC_CLK[18]	div_by_1_mode; ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475*P[15]- 0.3		0.475*P[15]- 0.3		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475*P[15]- 0.3		0.475*P[15]- 0.3		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition[14]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	F[6]- 2.2	F+3.75	F[6]- 2.2	F[6]+ 3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid[14]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	E[5]- 2.2	E[5]+ 3.75	E[5]- 2.2	E[5]+ 3.75	ns
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B[2]-2.3	B[2]+4.5	B[2]-2.3	B[2]+4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	–2.3	4.5	–2.3	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B[2]-2.3	B[2]+1.9	B[2]-2.3	B[2]+1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid[11]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[12]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F7	$t_{d(clkL-be[x]nIV).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[13]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	G[7]-2.3	G[7]+4.5	G[7]-2.3	G[7]+4.5	ns

NO.[2]	PARAMETER	DESCRIPTION	MODE[19]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[20]		133 MHz[20]		
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	D[4]-2.3	D[4]+4.5	D[4]-2.3	D[4]+4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	H[8]-2.3	H[8]+3.5	H[8]-2.3	H[8]+3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	E[8]-2.3	E[8]+3.5	E[8]-2.3	E[8]+ 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1 no extra_delay	I[9]- 2.3	I[9]+4.5	I[9]- 2.3	I[9]+4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition[11]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[12]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F15	$t_{d(clkL-do).}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[13]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition[11]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[12]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F17	$t_{d(clkL-be[x]n).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[13]	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i] low[14]	Read	A[1]		A[1]		ns
			Write	A[1]		A[1]		ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C[3]		C[3]		ns
			Write	C[3]		C[3]		ns
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K[16]		K[16]		ns
			Write	K[16]		K[16]		ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
With n being the page burst access number.
(2) B = ClkActivationTime × GPMC_FCLK[17]
(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[17]

For burst read: C = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For burst write: C = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
With n being the page burst access number.

(4) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)

(5) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)

(6) For csn falling edge (CS activated):

- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(17) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(17) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(17) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK (17)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(17) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(17) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) J = GPMC_FCLK(17)
(11) First transfer only for CLK DIV 1 mode.
(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(13) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(14) In GPMC_CSn[i], i is equal to 0, 1, 2, or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
(15) P = GPMC_CLK period in ns
(16) For read: K = (ADVRdOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
For write: K = (ADVWrOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(17)
(17) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(18) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(19) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100 MHz
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra_delay:

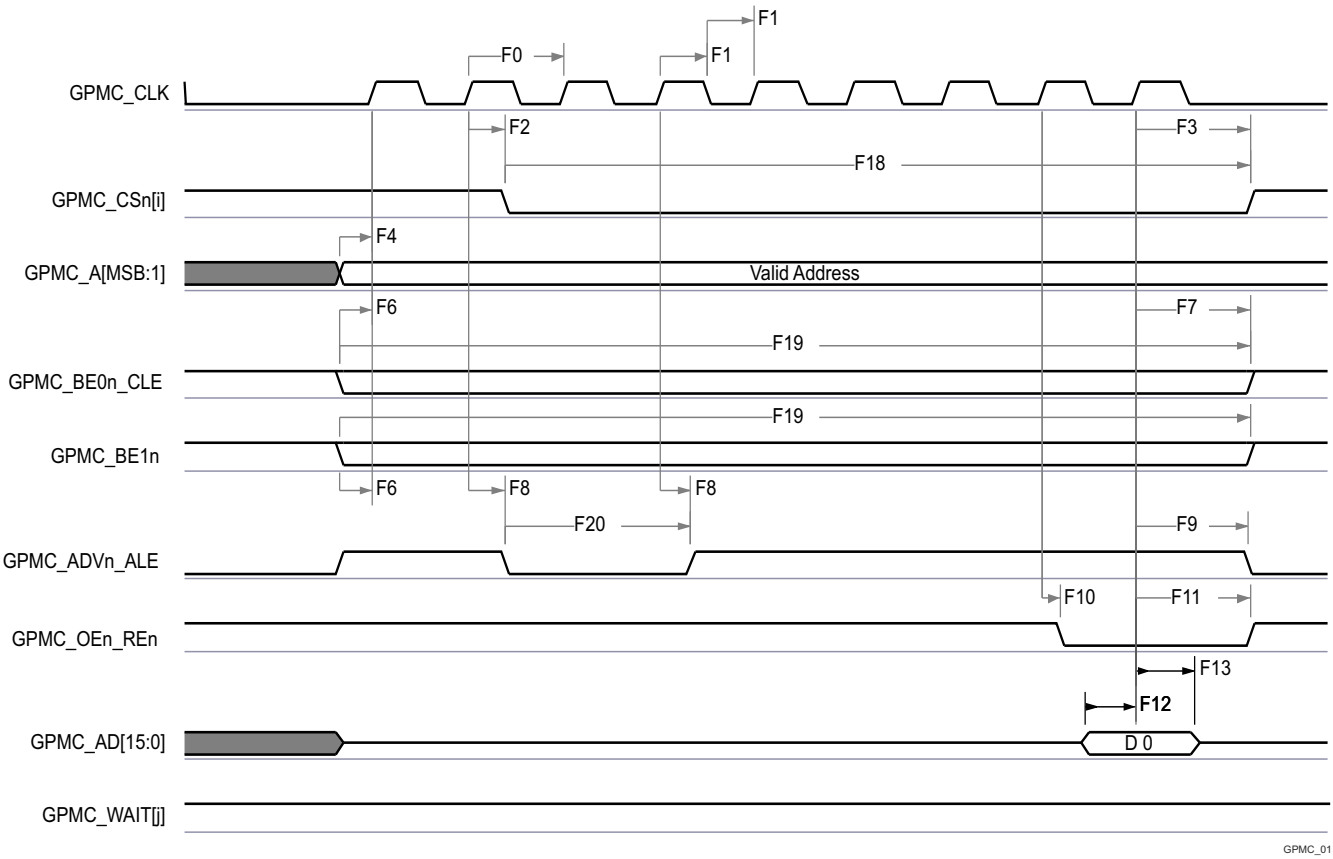
- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed

(20) For 100 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = MAIN_PLL2_HSDIV1_CLKOUT / 3

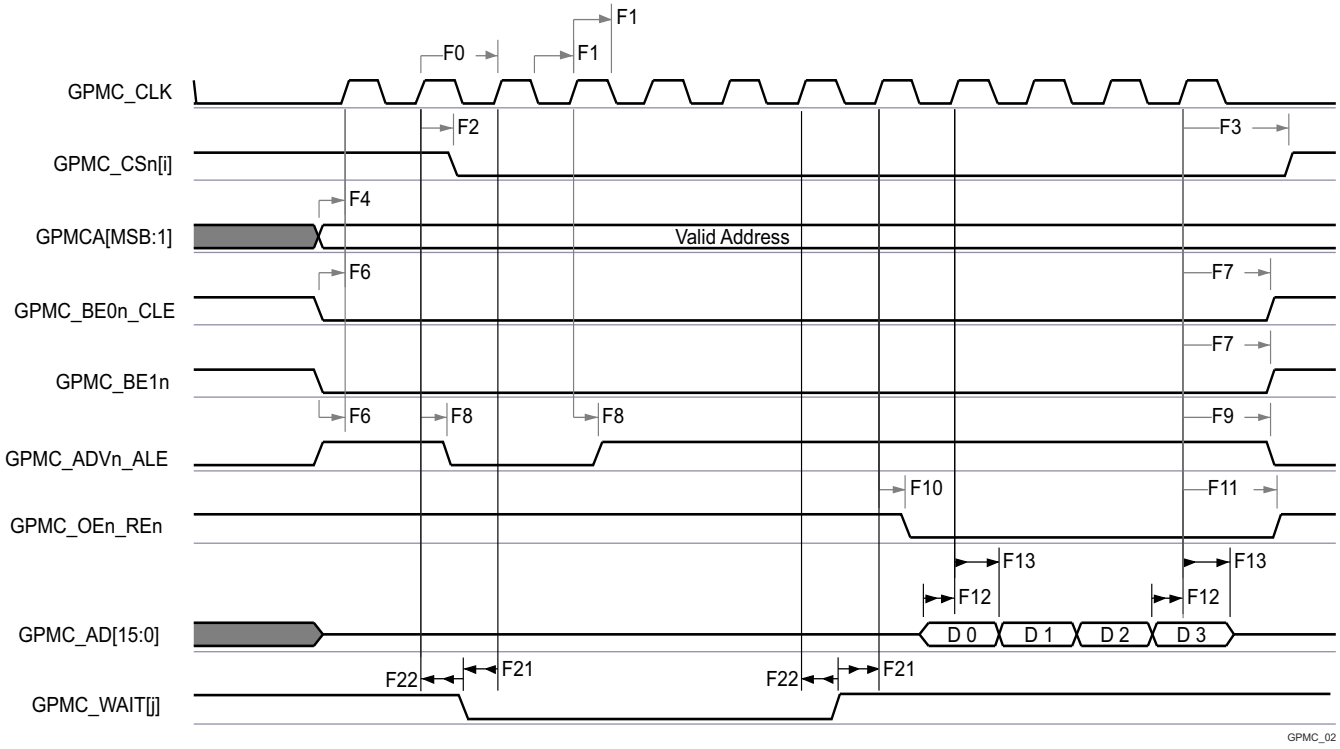
For 133 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



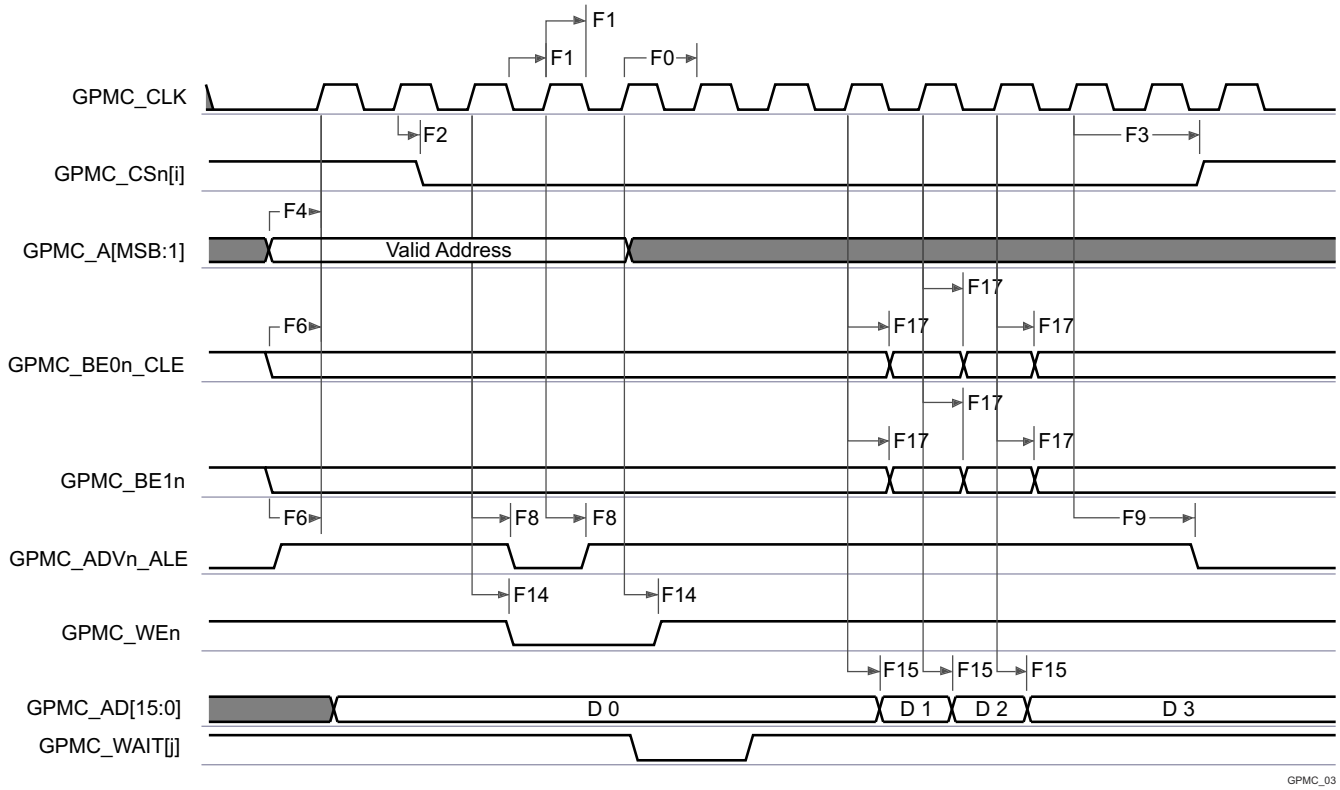
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-53. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

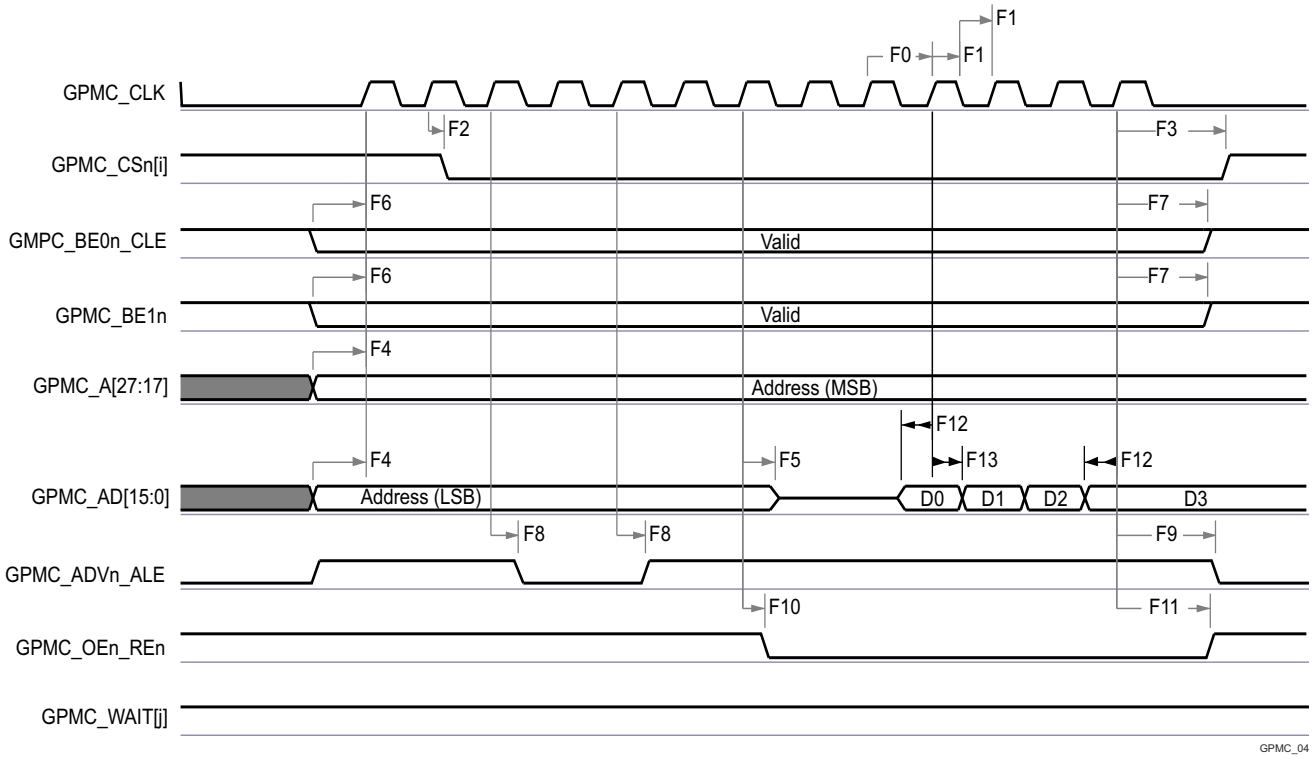
Figure 6-54. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

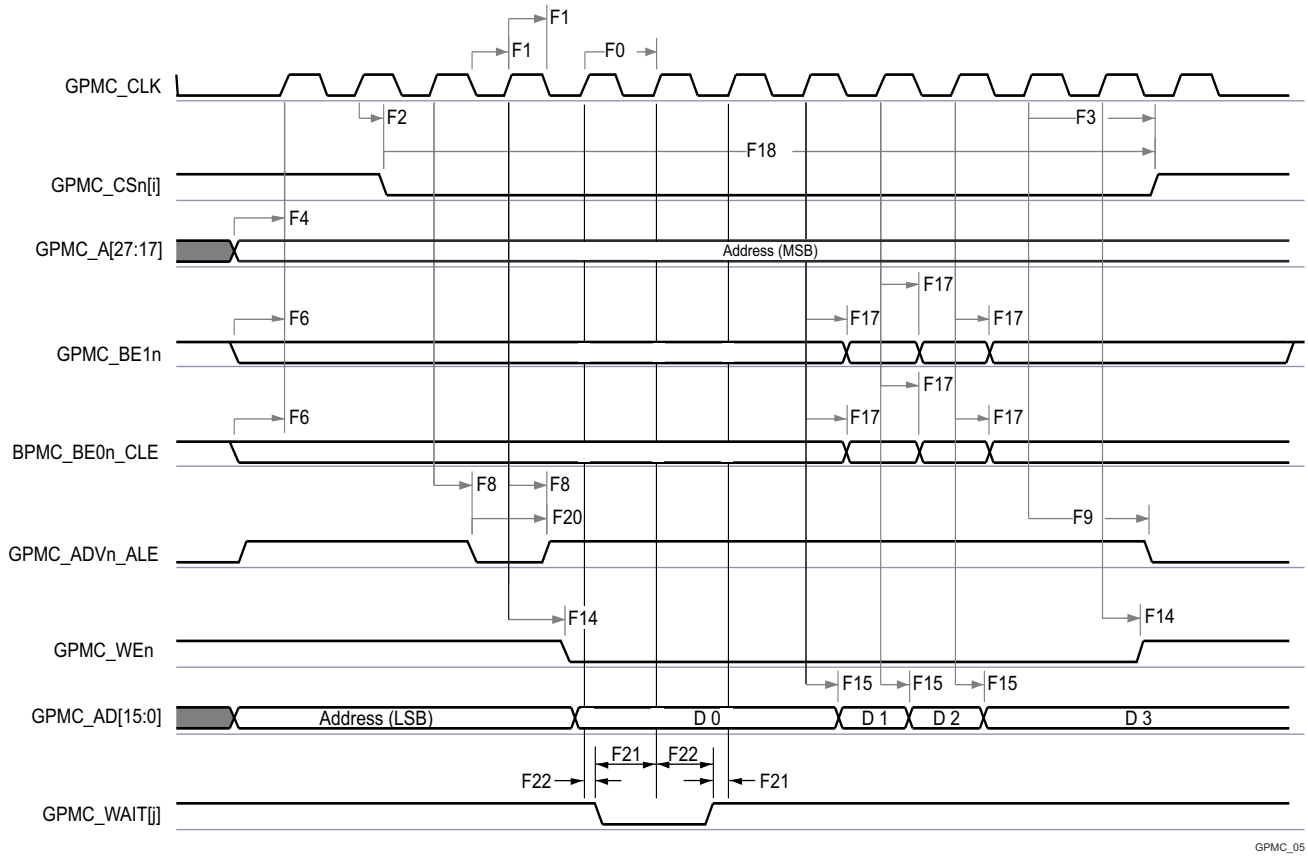
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-55. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-56. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-57. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

6.10.5.10.2 GPMC and NOR Flash — Asynchronous Mode

Section 6.10.5.10.2.1 and Section 6.10.5.10.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-58 through Figure 6-63).

6.10.5.10.2.1 GPMC and NOR Flash Timing Requirements – Asynchronous Mode

NO.			MODE[7]	MIN	MAX	UNIT
FA5[1]	$t_{acc(d)}$	Data access time	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X 1		H[5]	ns
FA20[2]	$t_{acc1\text{-}pgmode(d)}$	Page mode successive data access time	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X 1		P[4]	ns
FA21[3]	$t_{acc2\text{-}pgmode(d)}$	Page mode first data access time	div_by_1_mode ; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X 1		H[5]	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

(3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
(4) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(6)
(5) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(6)
(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(7) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

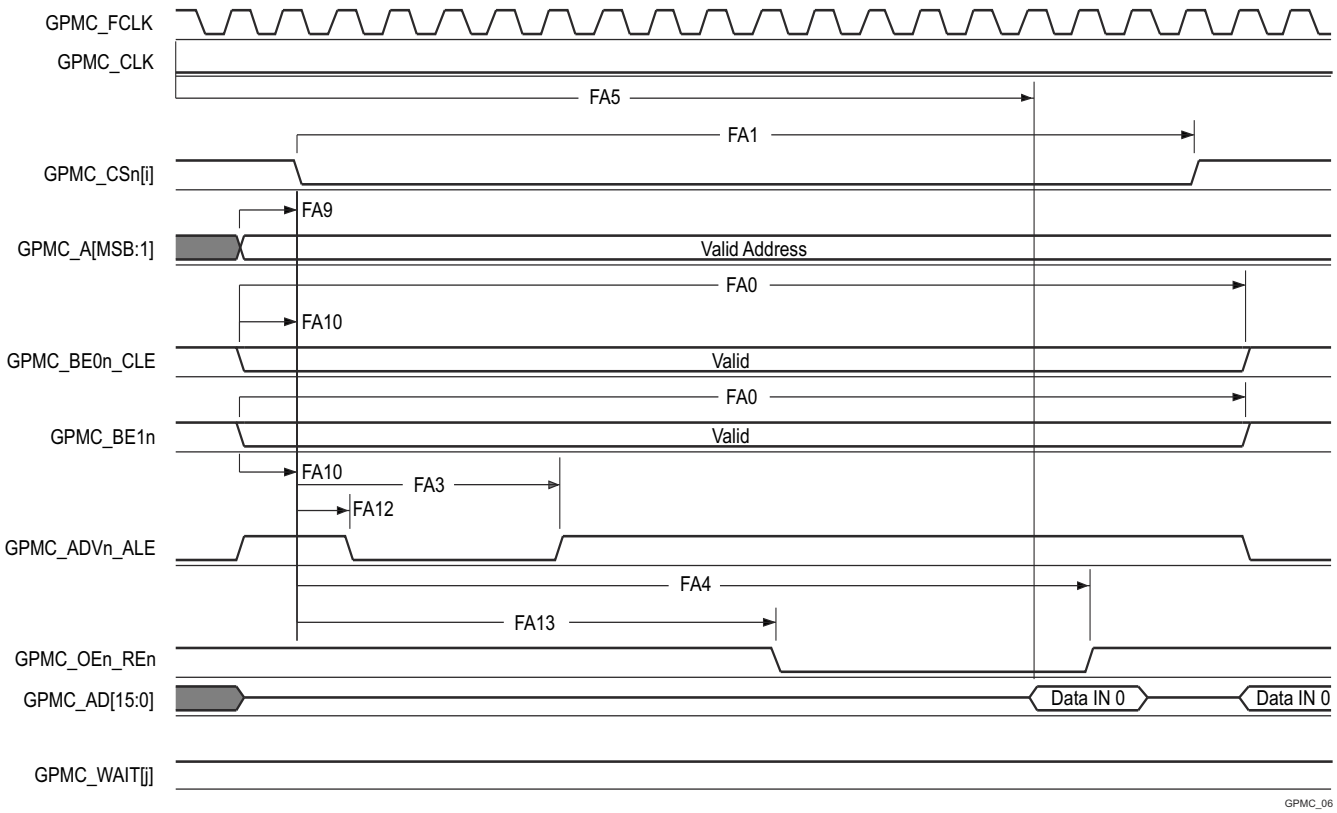
6.10.5.10.2.2 GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE(15)	MIN MAX 133 MHz(16)	UNIT
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read	N(12)	ns
			Write	N(12)	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read	A(1)	ns
			Write	A(1)	
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B(2)- 2.55 B(2)+ 2.65	ns
			Write	B(2)- 2.55 B(2)+ 2.65	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C(3)- 2.55 C(3)+ 2.65	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J(9)- 2.55 J(9)+ 2.65	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J(9)- 2.55 J(9)+ 2.65	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K(10)- 2.55 K(10)+ 2.65	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L(11)- 2.55 L(11)+ 2.65	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G(7)	ns
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I(8)- 2.55 I(8)+ 2.65	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D(4)	ns

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN MAX 133 MHz[16]	UNIT
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E[5]- 2.55 E[5]+ 2.65	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F[6]- 2.55 F[6]+ 2.65	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.65	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[9]- 2.55 J[9]+ 2.65	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.65	ns

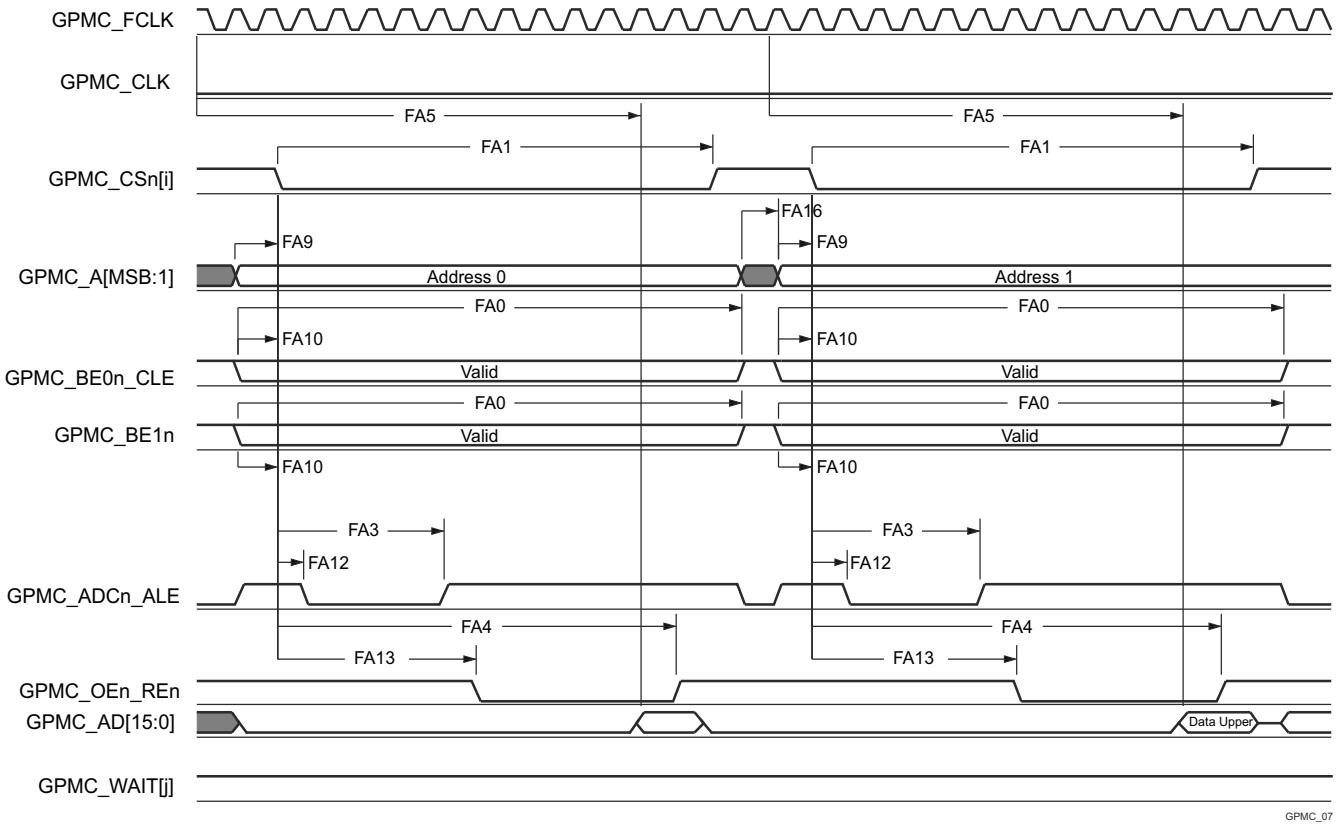
(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(7) G = Cycle2CycleDelay × GPMC_FCLK[14]
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK[14]
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(16) For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



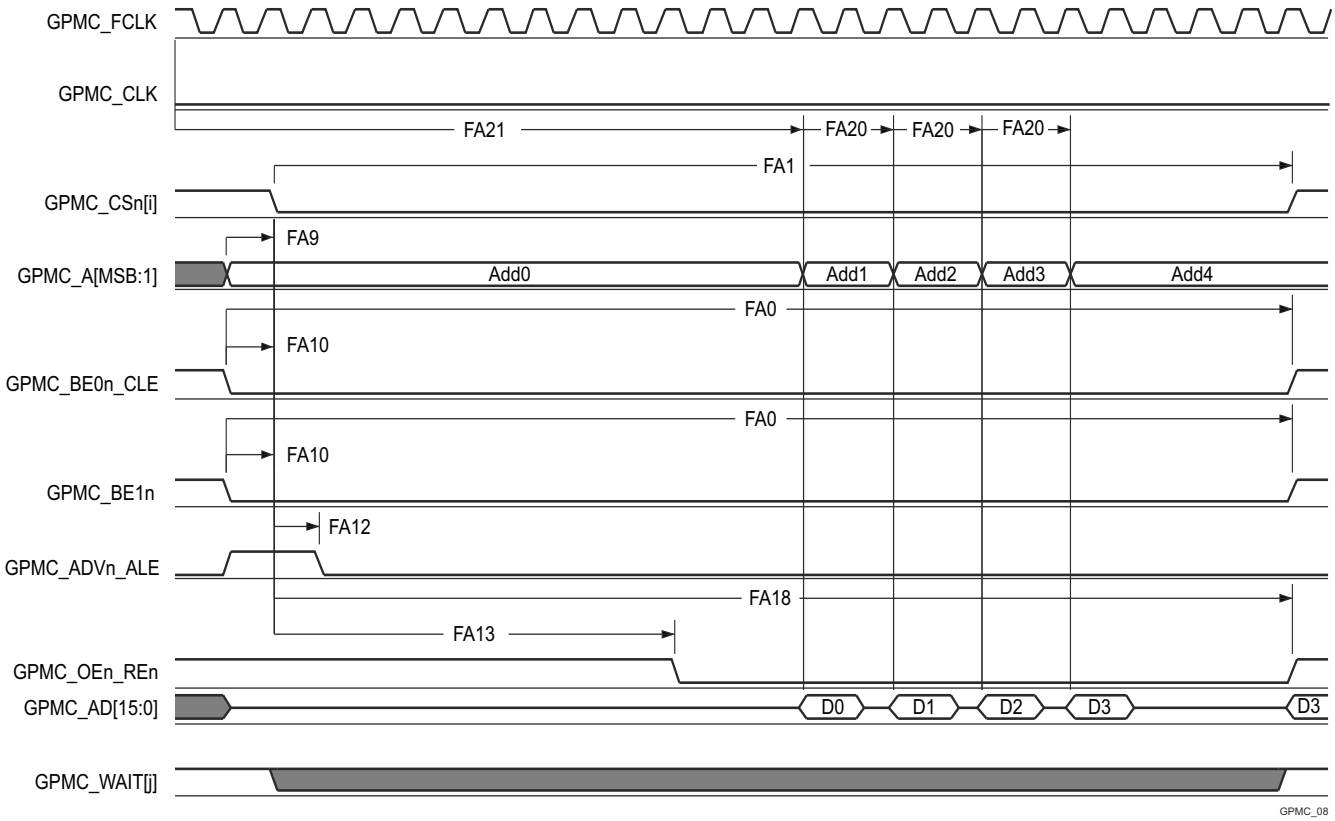
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-58. GPMC and NOR Flash — Asynchronous Read — Single Word



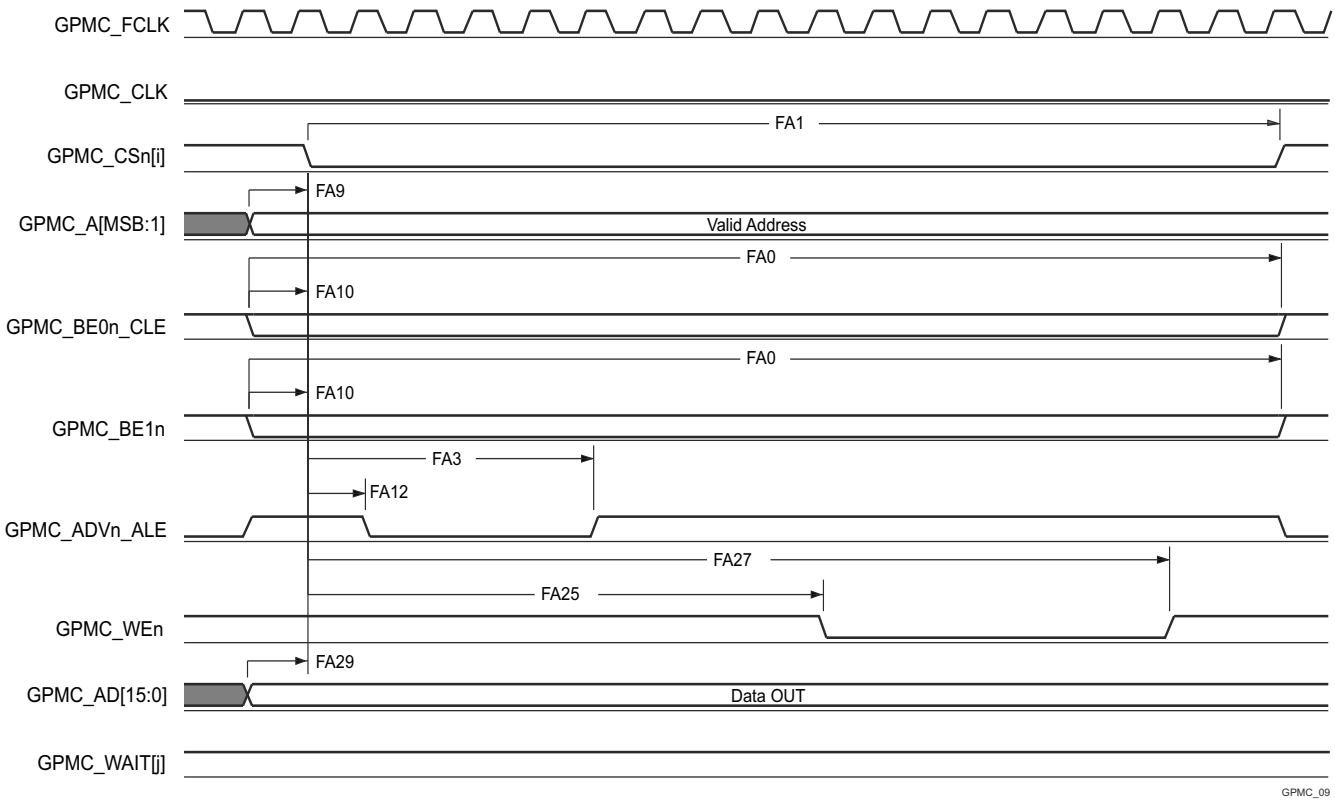
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-59. GPMC and NOR Flash — Asynchronous Read — 32–Bit



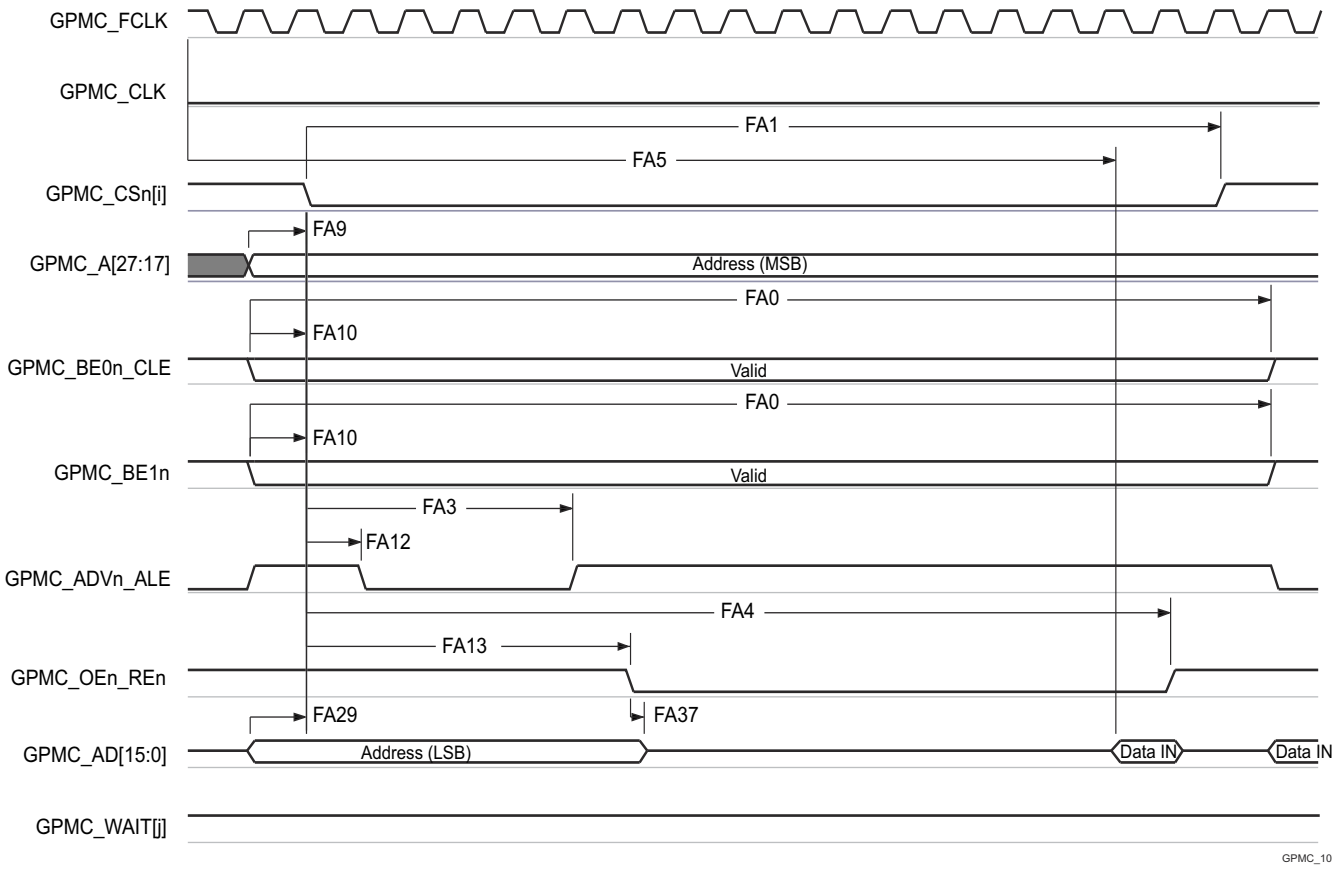
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-60. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



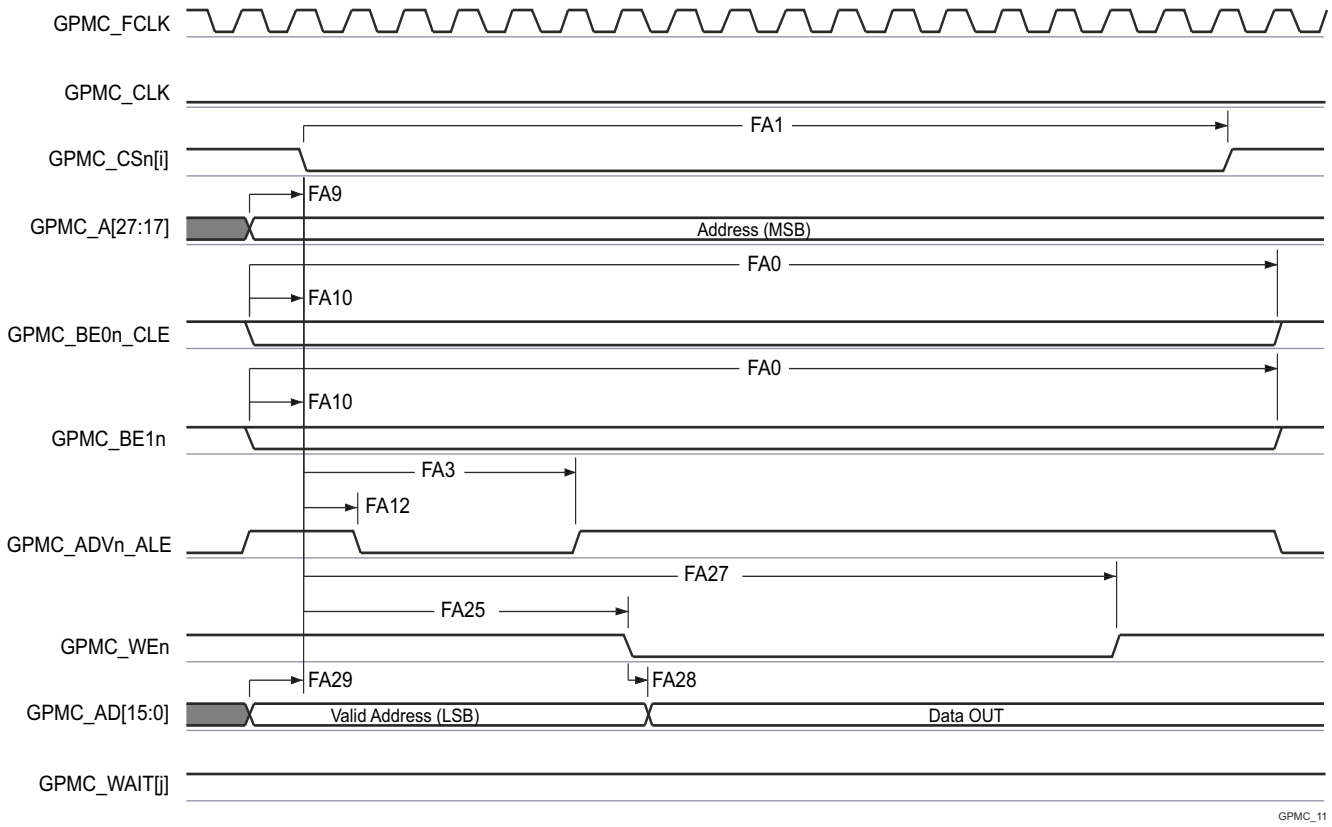
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-61. GPMC and NOR Flash — Asynchronous Write — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-62. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-63. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

6.10.5.10.3 GPMC and NAND Flash — Asynchronous Mode

Section 6.10.5.10.3.1 and Section 6.10.5.10.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-64 through Figure 6-67).

6.10.5.10.3.1 GPMC and NAND Flash Timing Requirements – Asynchronous Mode

NO.			MODE[4]	MIN / MAX 133 MHz[5]	UNIT
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(5) For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT

6.10.5.10.3.2 GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

NO.	PARAMETER		MODE[15]	MIN	MAX	UNIT
				133 MHz[16]		
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A[1]		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B[2] - 2.55	B[2]+ 2.65	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C[3] - 2.55	C[3]+ 2.65	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D[4] - 2.55	D[4]+ 2.65	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E[5] - 2.55	E[5]+ 2.65	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F[6] - 2.55	F[6]+ 2.65	ns

NO.	PARAMETER		MODE[15]	MIN	MAX	UNIT
				133 MHz[16]		
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i][13] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G[7] - 2.55	G[7]+ 2.65	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C[3] - 2.55	C[3]+ 2.65	ns
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F[6] - 2.55	F[6]+ 2.65	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H[8]	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I[9] - 2.55	I[9]+ 2.65	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K[10]	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L[11]		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][13] invalid	div_by_1_mode;	M[12] - 2.55	M[12]+ 2.65	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(2) B = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((WEOnTime - ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - ADVExtraDelay)) × GPMC_FCLK[14]
(4) D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK[14]
(5) E = ((WrCycleTime - WEOffTime) × (TimeParaGranularity + 1) - 0.5 × WEExtraDelay) × GPMC_FCLK[14]
(6) F = ((ADVWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - WEExtraDelay)) × GPMC_FCLK[14]
(7) G = ((CSWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - WEExtraDelay)) × GPMC_FCLK[14]
(8) H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(9) I = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(10) K = (OEOffTime - OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(11) L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(12) M = ((CSRdOffTime - OEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - OEExtraDelay)) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

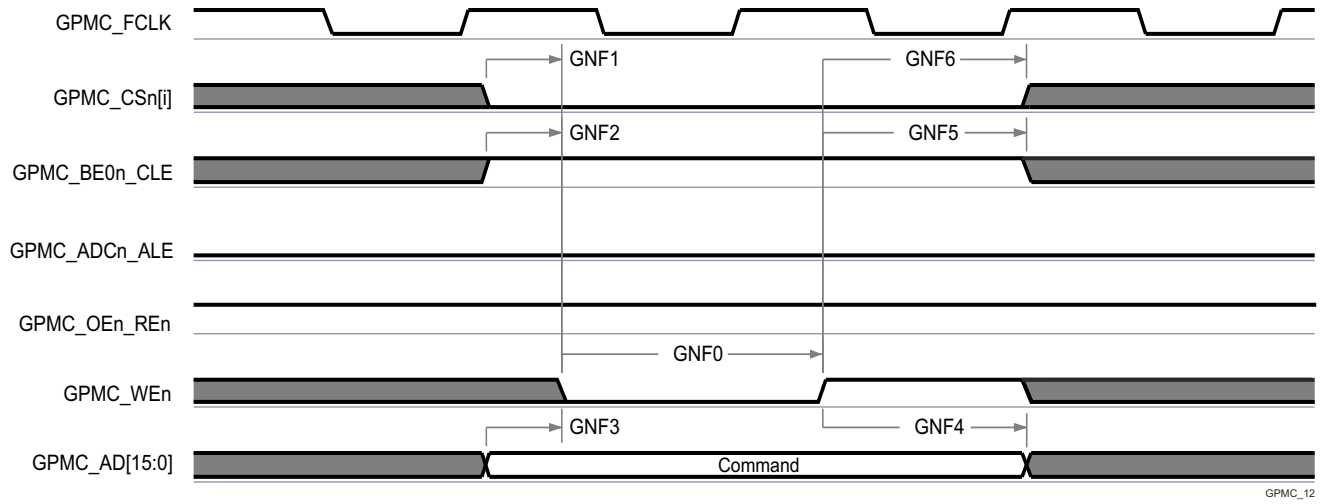
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

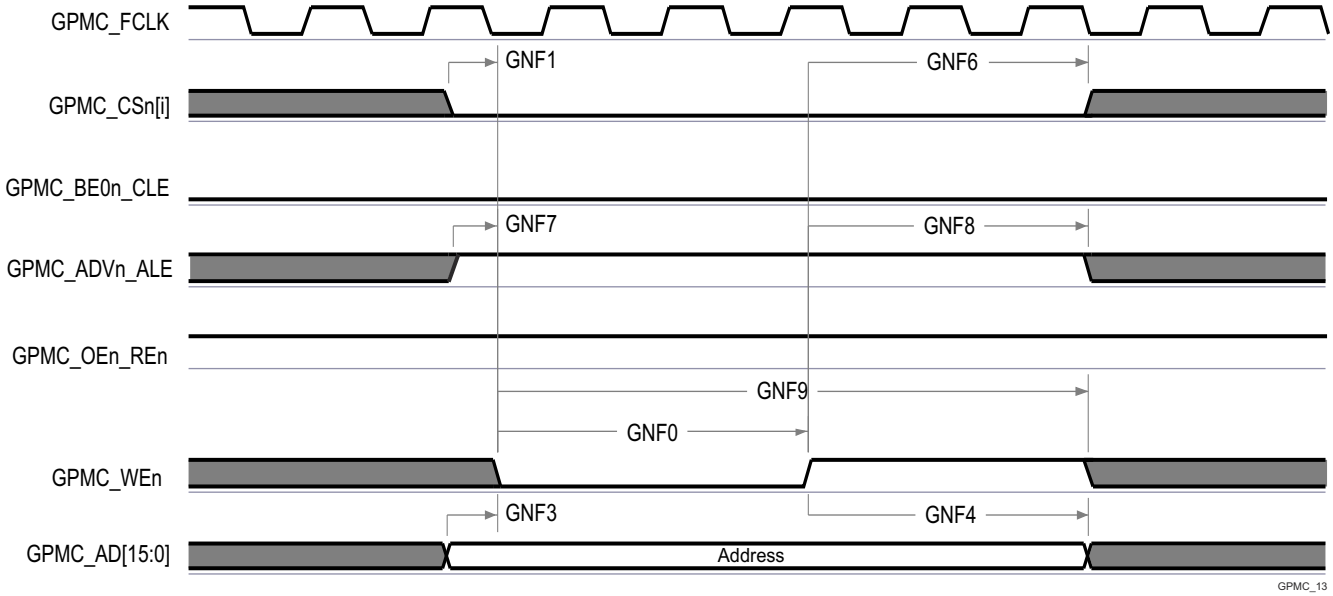
(16) For 133 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



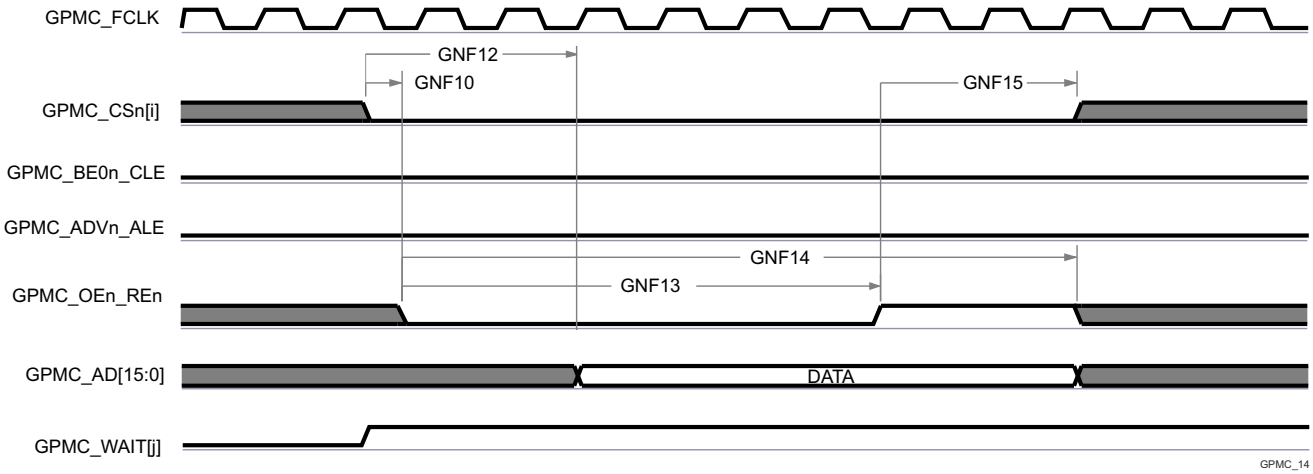
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-64. GPMC and NAND Flash — Command Latch Cycle



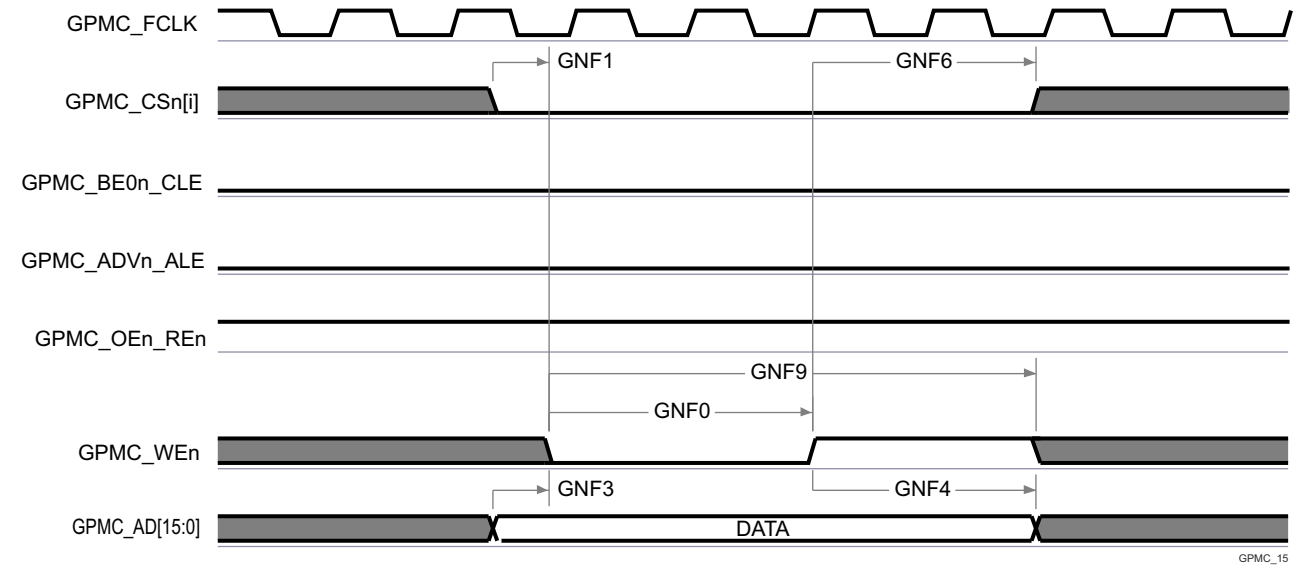
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-65. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

Figure 6-66. GPMC and NAND Flash — Data Read Cycle



A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-67. GPMC and NAND Flash — Data Write Cycle

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

6.10.5.10.4 GPMC0 IOSET

Table 6-42 present the specific groupings of signals (IOSET) for use with GPMC0.

Table 6-42. GPMC0 IOSET

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
GPMC0_WAIT2	MDIO0_MDC	8	MDIO0_MDC	8

Table 6-42. GPMC0 IOSET (continued)

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
GPMC0_BE1n	PRG1_PRU0_GPO0	8	RGMII6_RD1	8
GPMC0_WAIT0	PRG1_PRU0_GPO1	8	PRG1_PRU0_GPO1	8
GPMC0_WAIT1	PRG1_PRU0_GPO2	8	PRG1_PRU0_GPO2	8
GPMC0_DIR	PRG1_PRU0_GPO3	8	PRG1_PRU0_GPO3	8
GPMC0_CSn2	PRG1_PRU0_GPO4	8	PRG1_PRU0_GPO4	8
GPMC0_WEn	PRG1_PRU0_GPO5	8	PRG1_PRU0_GPO5	8
GPMC0_CSn3	PRG1_PRU0_GPO6	8	PRG1_PRU0_GPO6	8
GPMC0_OEn_REn	PRG1_PRU0_GPO8	8	PRG1_PRU0_GPO8	8
GPMC0_ADVn_ALE	PRG1_PRU0_GPO9	8	PRG1_PRU0_GPO9	8
GPMC0_BE0n_CLE	PRG1_PRU0_GPO10	8	PRG1_PRU0_GPO10	8
GPMC0_WPn	PRG1_PRU1_GPO5	8	PRG1_PRU1_GPO5	8
GPMC0_CSn1	PRG1_PRU1_GPO8	8	PRG1_PRU1_GPO8	8
GPMC0_CSn0	PRG1_PRU1_GPO9	8	PRG1_PRU1_GPO9	8
GPMC0_CLKOUT	PRG1_PRU1_GPO10	8	PRG1_PRU1_GPO10	8
GPMC0_AD0	PRG0_PRU0_GPO5	8	PRG0_PRU0_GPO5	8
GPMC0_AD1	PRG0_PRU0_GPO7	8	PRG0_PRU0_GPO7	8
GPMC0_AD2	PRG0_PRU0_GPO8	8	PRG0_PRU0_GPO8	8
GPMC0_AD3	PRG0_PRU0_GPO9	8	PRG0_PRU0_GPO9	8
GPMC0_AD4	PRG0_PRU0_GPO10	8	PRG0_PRU0_GPO10	8
GPMC0_AD5	PRG0_PRU0_GPO17	8	PRG0_PRU0_GPO17	8
GPMC0_AD6	PRG0_PRU0_GPO18	8	PRG0_PRU0_GPO18	8
GPMC0_AD7	PRG0_PRU0_GPO19	8	PRG0_PRU0_GPO19	8
GPMC0_AD8	PRG0_PRU1_GPO5	8	PRG0_PRU1_GPO5	8
GPMC0_AD9	PRG0_PRU1_GPO7	8	PRG0_PRU1_GPO7	8
GPMC0_AD10	PRG0_PRU1_GPO8	8	PRG0_PRU1_GPO8	8
GPMC0_AD11	PRG0_PRU1_GPO9	8	PRG0_PRU1_GPO9	8
GPMC0_AD12	PRG0_PRU1_GPO10	8	PRG0_PRU1_GPO10	8
GPMC0_AD13	PRG0_PRU1_GPO17	8	PRG0_PRU1_GPO17	8
GPMC0_AD14	PRG0_PRU1_GPO18	8	PRG0_PRU1_GPO18	8
GPMC0_AD15	PRG0_PRU1_GPO19	8	PRG0_PRU1_GPO19	8
GPMC0_A0	PRG0_MDIO0_MDC	8	PRG0_MDIO0_MDC	8
GPMC0_A1	RGMII5_TX_CTL	8	RGMII5_TX_CTL	8
GPMC0_A2	RGMII5_RX_CTL	8	RGMII5_RX_CTL	8
GPMC0_A3	RGMII5_TD3	8	RGMII5_TD3	8
GPMC0_A4	RGMII5_TD2	8	RGMII5_TD2	8
GPMC0_A5	RGMII5_TD1	8	RGMII5_TD1	8
GPMC0_A6	RGMII5_TD0	8	RGMII5_TD0	8
GPMC0_A7	RGMII5_TXC	8	RGMII5_TXC	8
GPMC0_A8	RGMII5_RXC	8	RGMII5_RXC	8
GPMC0_A9	RGMII5_RD3	8	RGMII5_RD3	8
GPMC0_A10	RGMII5_RD2	8	RGMII5_RD2	8
GPMC0_A11	RGMII5_RD1	8	RGMII5_RD1	8
GPMC0_A12	RGMII5_RD0	8	RGMII5_RD0	8
GPMC0_A13	RGMII6_TX_CTL	8	RGMII6_TX_CTL	8

Table 6-42. GPMC0 IOSET (continued)

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
GPMC0_A14	RGMII6_RX_CTL	8	RGMII6_RX_CTL	8
GPMC0_A15	RGMII6_TD3	8	RGMII6_TD3	8
GPMC0_A16	RGMII6_TD2	8	RGMII6_TD2	8
GPMC0_A17	RGMII6_TD1	8	RGMII6_TD1	8
GPMC0_A18	RGMII6_TD0	8	RGMII6_TD0	8
GPMC0_A19	RGMII6_TXC	8	RGMII6_TXC	8
GPMC0_A20	RGMII6_RXC	8	RGMII6_RXC	8
GPMC0_A21	RGMII6_RD3	8	RGMII6_RD3	8
GPMC0_A22	RGMII6_RD2	8	RGMII6_RD2	8
GPMC0_A23	PRG0_PRU1_GPO2	8	PRG0_PRU1_GPO2	8
GPMC0_A24	PRG0_PRU1_GPO4	8	PRG0_PRU1_GPO4	8
GPMC0_A25	PRG0_PRU1_GPO6	8	PRG0_PRU1_GPO6	8
GPMC0_A26	PRG0_PRU1_GPO11	8	PRG0_PRU1_GPO11	8
GPMC0_A27	PRG0_MDIO0_MDIO	8	PRG0_MDIO0_MDIO	8
GPMC0_WAIT3	MDIO0_MDIO	8	MDIO0_MDIO	8

6.10.5.11 HyperBus

For more details about features and additional description information on the device HyperBus, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Section 6.10.5.11, Section 6.10.5.11.2, and Section 6.10.5.11.3 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 6-68, Figure 6-69, and Figure 6-70).

Table 6-43 represents HyperBus timing conditions.

Table 6-43. HyperBus Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	8	pF

6.10.5.11.1 Timing Requirements for HyperBus

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D1	$t_{w(RESETn)}$	Pulse width, RESETn	200		ns
D2	$t_{w(csL)}$	Pulse width, Chip Select	1000		ns
D3	$t_{d(RESETnH-csL)}$	Delay time, RESETn inactive to CSn active	200.34		ns
D4	$t_{d(csL-RWDSL)}$	Delay time, CSn active to RWDS falling	115		ns

6.10.5.11.2 HyperBus 166 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	-0.46	0.46	ns
D6	$t_{c(clk/clkn)}$	CLK period, CLK/CLKn	6		ns
D7	$t_{w(clk/clkn)}$	Pulse width, CLK/CLKn	2.7		ns
D8	$t_{w(cslV)}$	Pulse width, CS0 invalid between operations	6		ns
D9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising/ CLKn falling		-3.34	ns
D10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK/ rising CLKn edge to CS0 inactive	0.41		ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	1.01	2.08	ns
D12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:D7 valid	0.84	2.17	ns

6.10.5.11.3 HyperBus 100 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LFD5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	-0.81	0.81	ns
LFD6	$t_{c(clk)}$	CLK period, CLK	10		ns
LFD7	$t_{w(clk)}$	Pulse width, CLK	4.75		ns
LFD8	$t_{w(csIV)}$	Pulse width, CS0 invalid between operations	10		ns
LFD9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising		-3.51	ns
LFD10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK edge to CS0 inactive	0.51		ns
LFD11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	1.51	3.49	ns
LFD12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:D7 valid	1.34	3.66	ns

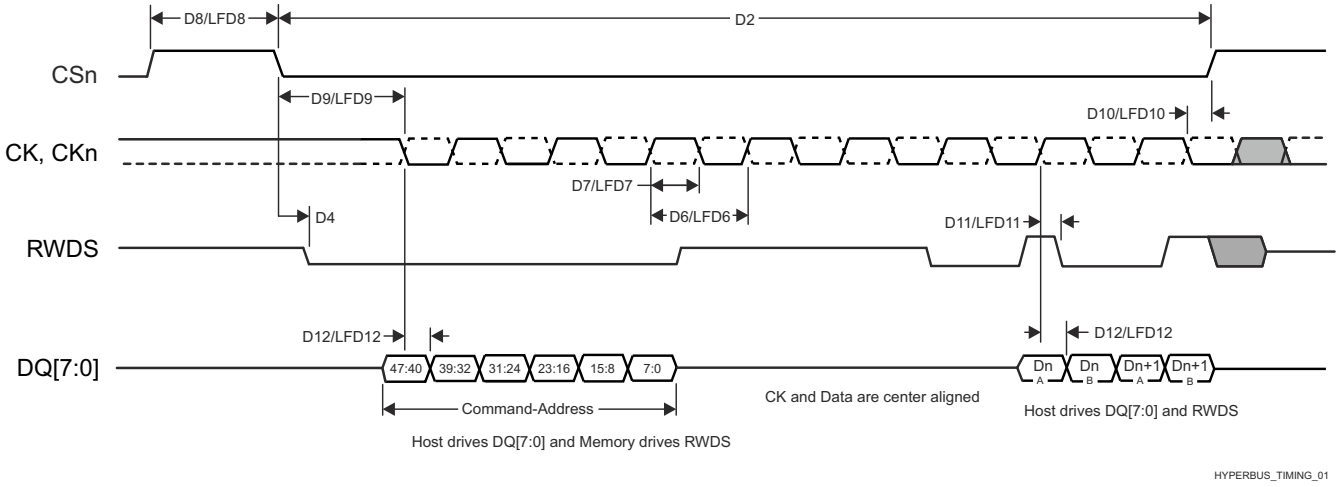


Figure 6-68. HyperBus Timing Diagrams – Transmitter Mode

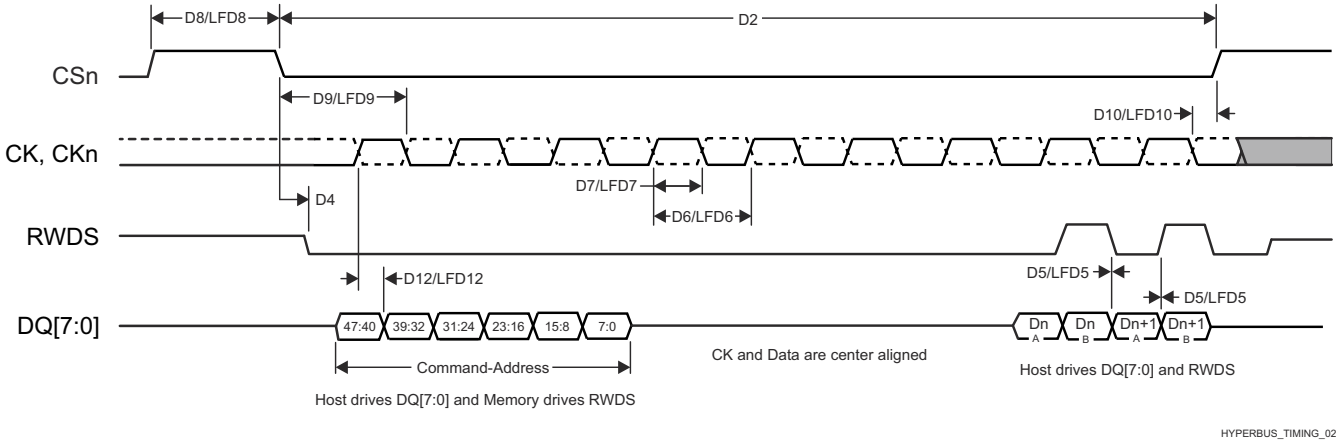


Figure 6-69. HyperBus Timing Diagrams – Receiver Mode

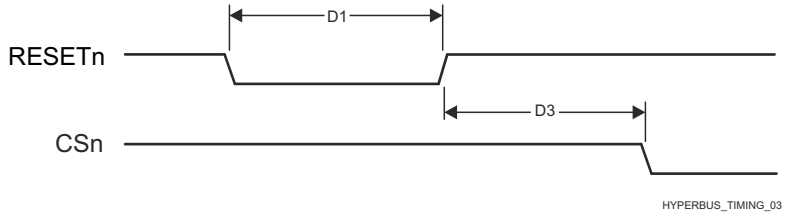


Figure 6-70. HyperBus Timing Diagrams – Reset

For more information, see *HyperBus Interface* section in *Peripherals* chapter in the device TRM.

6.10.5.12 I2C

The device contains **several** multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I2C-bus™ specification version 2.1. However, the device **IO Buffers** are not fully compliant to the I2C electrical specification. **Some I2C instances use the LVCMOS Buffer Type, while other instances use the I2S OD FS Buffer type. See the Pin Attributes table to determine the IO Buffer Type used for each I2C instance on this device.** The **I2C** speeds supported and exceptions are described per **IO Buffer Type** below:

- I2C instances that use the LVCMOS buffer type
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the Absolute Maximum Ratings section of this data sheet.
- I2C instances that use the I2C OD FS buffer type
  - Speeds:
    - Standard-mode (up to 100Kbits/s)
      - 1.8V
      - 3.3V
    - Fast-mode (up to 400Kbits/s)
      - 1.8V
      - 3.3V
    - Hs-mode (up to 3.4Mbit/s)
      - 1.8V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.08V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C

specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.08V/ns.

- The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the Absolute Maximum Ratings section of this data sheet.

Note

I2C3, I2C4, and I2C6 have one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within Section 5.3 and *Detailed Description*.

6.10.5.13 I3C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-44, Table 6-45, Figure 6-71, Table 6-46, and Figure 6-72 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-44. I3C Open Drain Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.2276	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance		50	pF

Table 6-45. I3C Open Drain Timing Parameters

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	t_{LOW_OD}	Low Period of SCL Clock	Controller	200		ns
	$t_{DIG\_OD\_L}$			$t_{LOW\_OD\ MIN}$ + $t_{FDA\_OD\ MIN}$		ns
D2	t_{HIGH}	High Period of SCL Clock	Controller		41	ns
	t_{DIG_H}				t_{HIGH} + t_{CF}	ns
D3	t_{fDA_OD}	Fall Time of SDA Signal	Controller, Target	t_{CF}	12	ns
D4	t_{SU_OD}	SDA Data Setup Time During Open Drain Mode	Controller, Target	3		ns
D5	t_{CAS}	Clock After START (S) Condition	Controller, ENTAS0	38.4	1000	ns
			Controller, ENTAS1	38.4	100000	ns
			Controller, ENTAS2	38.4	2000000	ns
			Controller, ENTAS3	38.4	50000000	ns
D6	t_{CBP}	Clock Before STOP (P) Condition	Controller	$t_{CAS\ MIN}$ / 2		ns
D7	$t_{MMOVERLAP}$	Current Controller to Secondary Controller Overlap time during handoff	Controller	$t_{DIG\_OD\_L\ min}$		ns
D8	t_{AVAL}	Bus Available Condition	Controller	1000		ns

Table 6-45. I3C Open Drain Timing Parameters (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D9	t_{IDLE}	Bus Idle Condition	Controller	1000000		ns
D10	t_{MMLOCK}	Time Internal Where New Controller Not Driving SDA Low	Controller	$t_{AVALmin}$		ns

1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.
2. The Controller may use a shorter Low period if the Controller knows that this is safe, when SDA is already above V_{IH}.
3. Based on t_{SPIKE}, rise and fall times, and interconnect.
4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (for example: a short Bus).
5. On a Legacy Bus where I2C Devices need to see Start, the t_{CAS} Min value is further constrained.
6. Targets that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3.
7. On a Mixed Bus with Fm Legacy I2C Devices, t_{AVAL} is 300ns shorter than the Fm Bus Free Condition time (t_{BUF}).

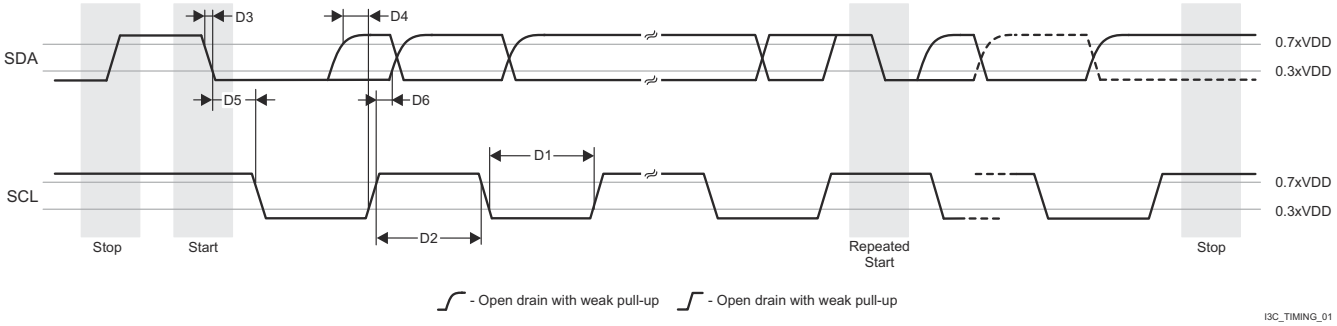


Figure 6-71. I3C Open Drain Timing

Table 6-46. I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	f_{SCL}	SCL Clock Period	Controller	80	100000	ns
D2	t_{LOW}	SCL Clock Low Period	Controller	24		ns
	t_{DIG_L}			32		ns
D3	t_{HIGH_MIXED}	SCL Clock High Period of Mixed Bus (Mixed Bus Topology Not Supported)	Controller	24		ns
	$t_{DIG\_H\_MIXED}$			32	45	ns
D4	t_{HIGH}	SCL Clock High Period	Controller	24		ns
	t_{DIG_H}			32		ns
D5	t_{SCO}	Clock in to Data Out for Target	Target	12		ns
D6	t_{CR}	SCL Clock Rise Time	Controller	150 × 1 / f_{SCL}	60	ns
D7	t_{CF}	SCL Clock Fall Time	Controller	150 × 1 / f_{SCL}	60	ns
D8	t_{HD_PP}	SDA Signal Data Hold in Push Pull Mode	Controller	t_{CR} + 3 and t_{CF} + 3		ns
			Target	0		ns
D9	t_{SU_PP}	SDA Signal Data Setup In Push-Pull Mode	Controller, Target	3		ns
D10	t_{CASr}	Clock After Repeated START (Sr)	Controller	$t_{CAS\ MIN}$		ns
D11	t_{CBSr}	Clock Before Repeated START (Sr)	Controller	$t_{CAS\ MIN}$ / 2		ns

1. FSCL = 1 / (t_{DIG_L} + t_{DIG_H})
2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.
4. As both edges are used, the hold time needs to be satisfied for the respective edges; t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.
5. Clock Frequency Minimum 0.01 MHz, Maximum 12.5 MHz

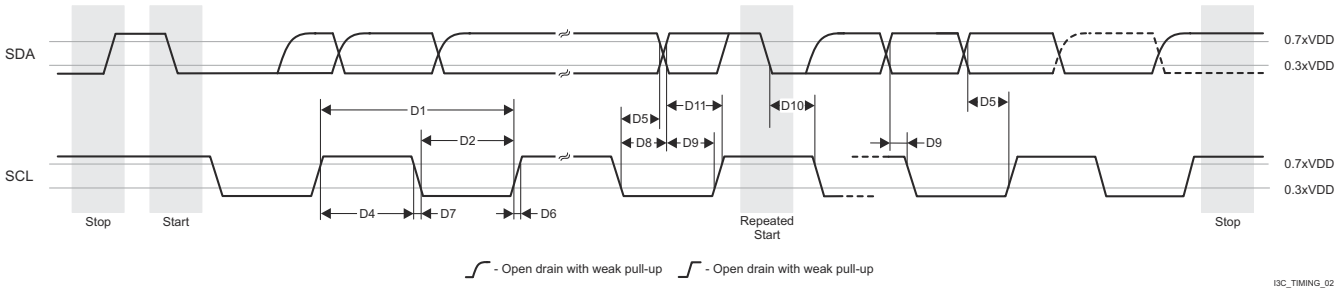


Figure 6-72. I3C Push-Pull Timing (SDR and HDR-DDR Modes)

6.10.5.14 MCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

Table 6-47. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

Table 6-48. MCAN Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
MCAN1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX pin(1)		10	ns
MCAN2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX pin to receive shift register(1)		10	ns

(1) n is [0:13] in MCANn_* or [0:1] in MCU_MCANn_*

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

6.10.5.15 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-50 and Figure 6-73 present timing requirements for MCASP0 to MCASP11.

Table 6-49 represents MCASP timing conditions.

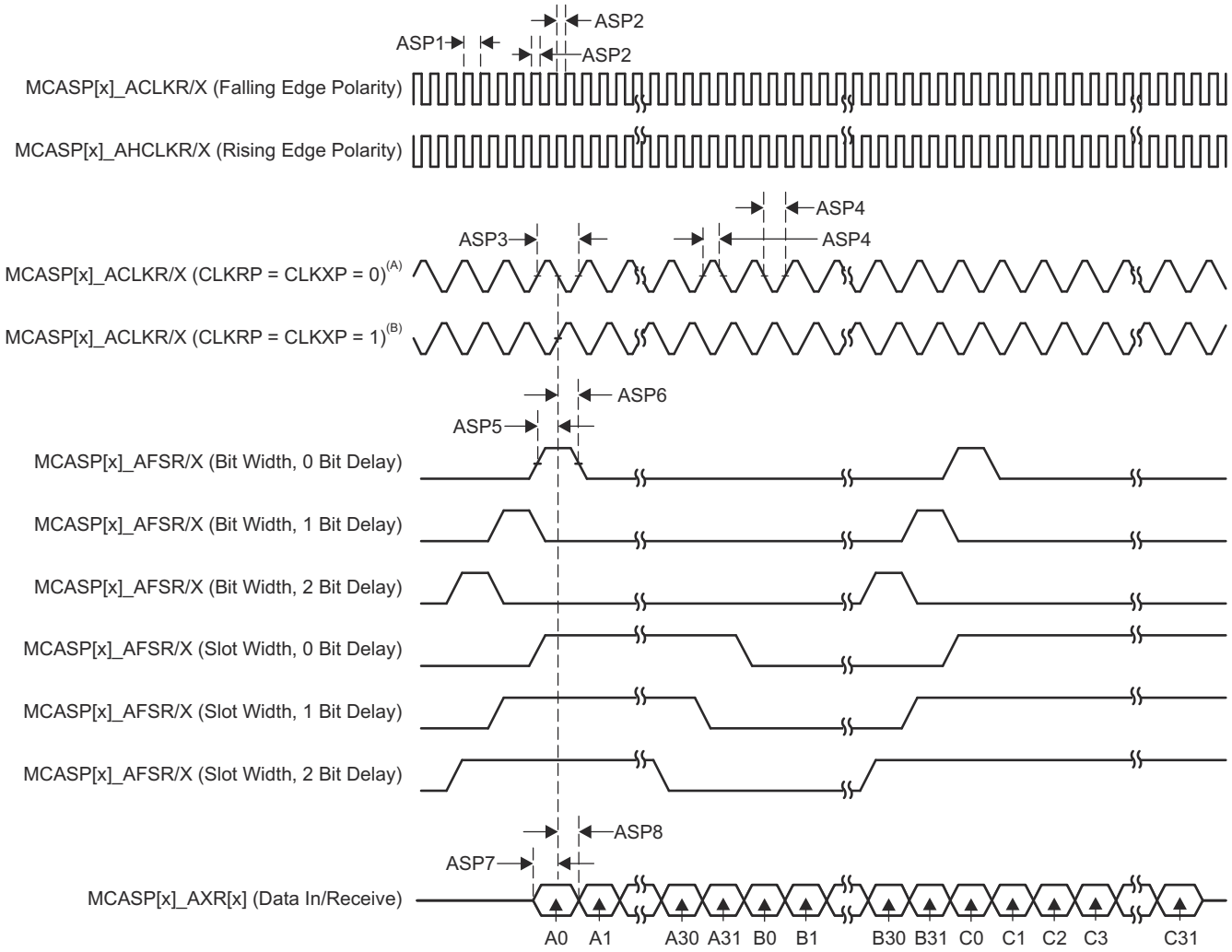
Table 6-49. MCASP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

Table 6-50. MCASP Timing Requirements

NO.			MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X		15.26		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X high or low		0.5P(2) - 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X		15.26		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X high or low		0.5R(3) - 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X input valid before MCASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in/out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X input valid after MCASP[x]_ACLKR/X	ACLKR/X int	–1		ns
			ACLKR/X ext in/out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR input valid before MCASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in/out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR input valid after MCASP[x]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns.
(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

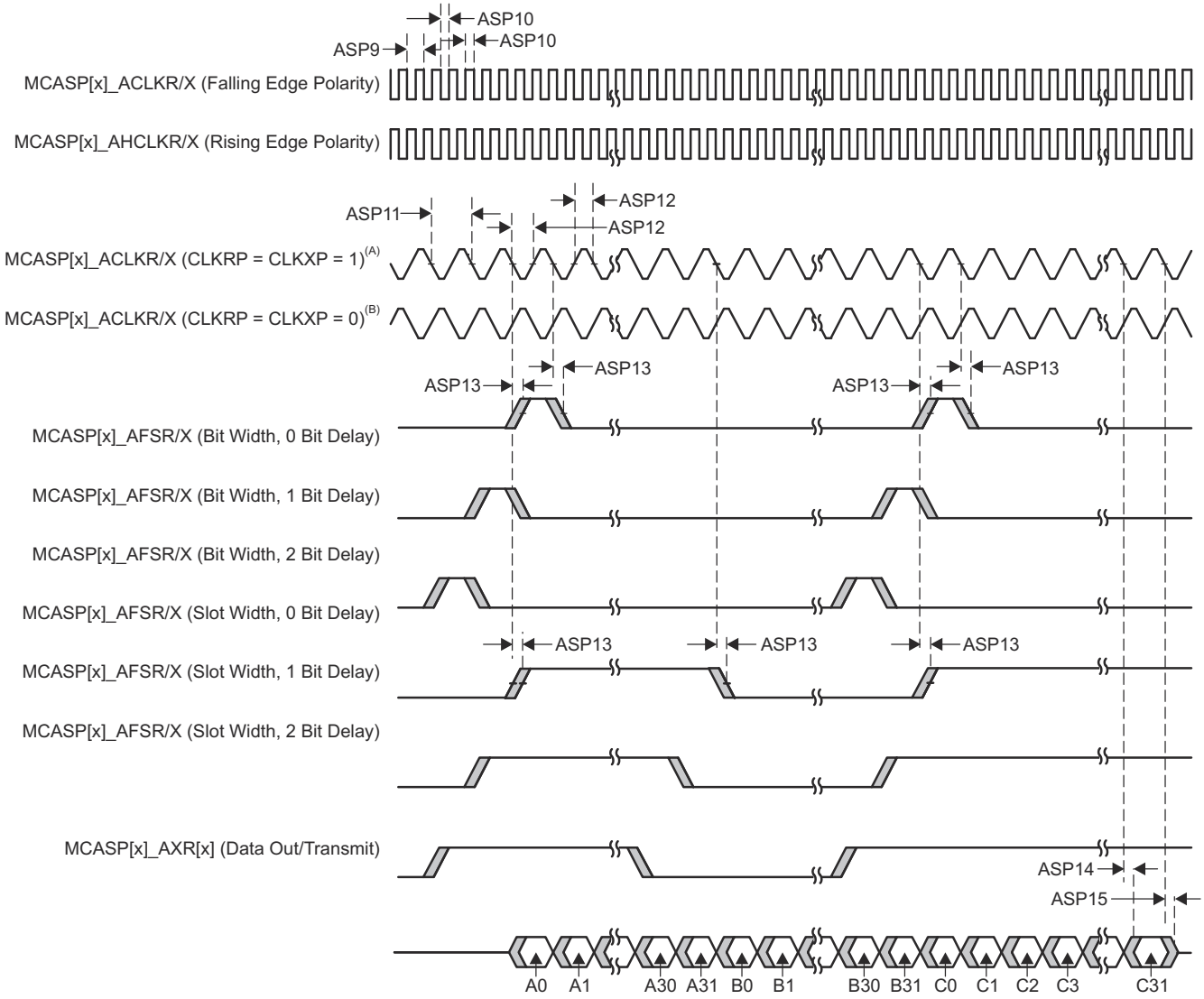
Figure 6-73. MCASP Input Timing

Table 6-51 and Figure 6-74 present switching characteristics over recommended operating conditions for MCASP0 to MCASP11.

Table 6-51. MCASP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X high or low		0.5P(2) - 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X high or low		0.5R(3) - 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X transmit edge to MCASP[x]_AFSR/X output valid	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	–15.28	12.84	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output valid	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	–15.28	12.84	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output high impedance	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	–14.9	14	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns.
(3) R = ACLKR/X period in ns.



A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

Figure 6-74. MCASP Output Timing

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

6.10.5.16 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within Signal Descriptions and *Detailed Description*.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

Table 6-52 represents MCSPI timing conditions.

Note

The IO timings provided in this section are applicable for all combinations of signals for MCU_SPI0 and MCU_SPI1. However, the timings are only valid for MCU_SPI0 and MCU_SPI1 if signals within a single IOSET are used. The IOSETs are defined in the Table 6-57 and Table 6-58 tables.

Table 6-52. MCSPI Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2	8.5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	CLK	6	24	pF
		D[x], CSi	6	12	pF

6.10.5.16.1 MCSPI — Controller Mode

Table 6-53, Figure 6-75, Table 6-54, and Figure 6-76 present timing requirements and switching characteristics for MCSPI – Controller Mode.

Table 6-53. MCSPI Timing Requirements - Controller Mode

see Figure 6-75

NO.			MIN	MAX	UNIT
SM4	$t_{su(misoV-spiclkV)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge	2.9		ns
SM5	$t_{h(spiclkV-misoV)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge	2		ns

Table 6-54. MCSPI Switching Characteristics - Controller Mode

see Figure 6-76

NO.	PARAMETER		MODE	MIN	MAX	UNIT
SM1	$t_{c(spiclk)}$	Cycle time, SPI_CLK		20		ns
SM2	$t_{w(spiclkL)}$	Pulse duration, SPI_CLK low		0.5P - 1[(1)]		ns
SM3	$t_{w(spiclkH)}$	Pulse duration, SPI_CLK high		0.5P - 1[(1)]		ns
SM6	$t_{d(spiclkV-simoV)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition		–2	2	ns
SM7	$t_{d(csV-simoV)}$	Delay time, SPI_CSi active edge to SPI_D[x] transition		5		ns
SM8	$t_{d(csV-spiclk)}$	Delay time, SPI_CSi active to SPI_CLK first edge	PHA = 0[(2)]	B - 4[(3)]		ns
			PHA = 1 [(2)]	A - 4[(4)]		ns
SM9	$t_{d(spiclkV-csV)}$	Delay time, SPI_CLK last edge to SPI_CSi inactive	PHA = 0[(2)]	A - 4[(4)]		ns
			PHA = 1[(2)]	B - 4[(3)]		ns

(1) P = SPI_CLK period in ns
(2) SPI_CLK phase is programmable with the PHA bit of the MCSPI_CHCONF_0/1/2/3 register
(3) B = (TCS + .5) * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register and Fratio = Even >= 2.
(4) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register.

When P > 20.8 ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register.

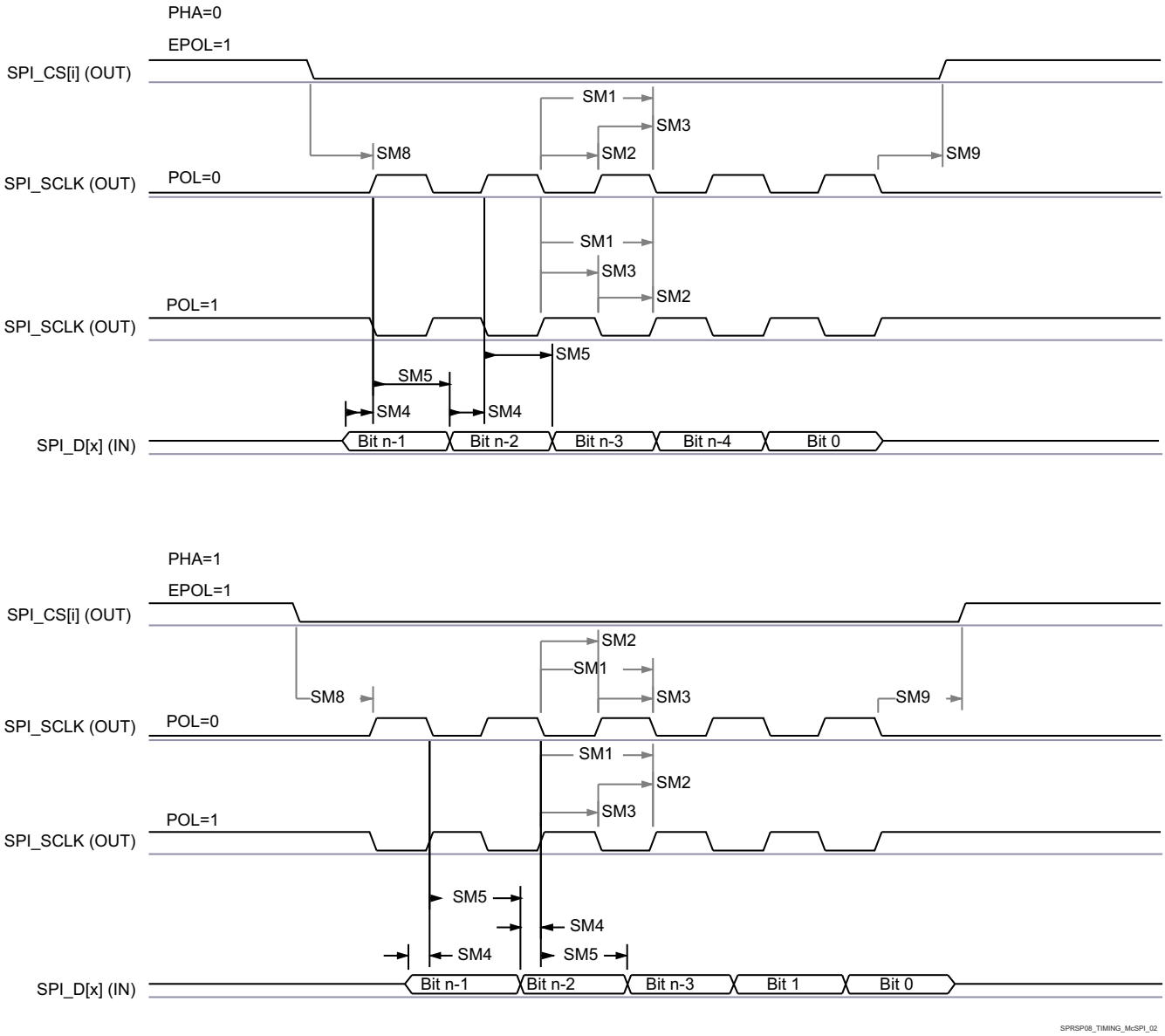


Figure 6-75. SPI Controller Mode Receive Timing

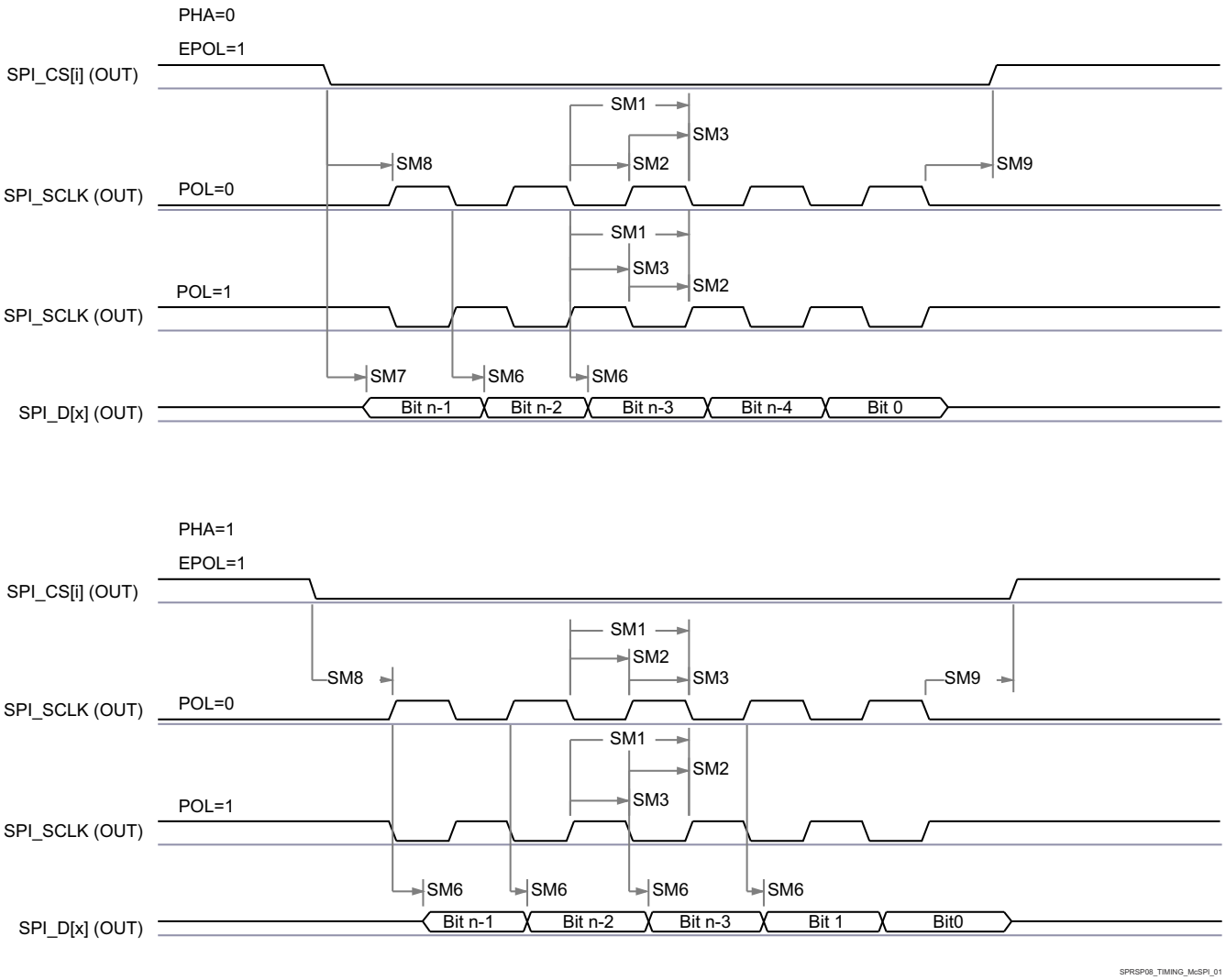


Figure 6-76. MCSPI Controller Mode Transmit Timing

6.10.5.16.2 MCSPI — Peripheral Mode

Table 6-55, Table 6-56, Figure 6-77, and Figure 6-78 present timing requirements and switching characteristics for MCSPI – Peripheral Mode.

Table 6-55. MCSPI Timing Requirements - Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1	$t_{c(spiclk)}$	Cycle time, SPI_CLK		20		ns
SS2	$t_{w(spiclkL)}$	Pulse duration, SPI_CLK low		0.45P[(1)]		ns
SS3	$t_{w(spiclkH)}$	Pulse duration, SPI_CLK high		0.45P[(1)]		ns
SS4	$t_{su(simoV-spiclkV)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge		5		ns
SS5	$t_{h(spiclkV-simoV)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge		5		ns
SS8	$t_{su(csV-spiclkV)}$	Setup time, SPI_CSi valid before SPI_CLK first edge		5		ns
SS9	$t_{h(spiclkV-csV)}$	Hold time, SPI_CSi valid after SPI_CLK last edge		5		ns

Table 6-56. MCSPI Switching Characteristics - Peripheral Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(spiclkV-somiV)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition	2	17.12	ns
SS7	$t_{sk(csV-somiV)}$	Delay time, SPI_CSi active edge to SPI_D[x] transition	20.95		ns

(1) P = SPI_CLK period in ns.

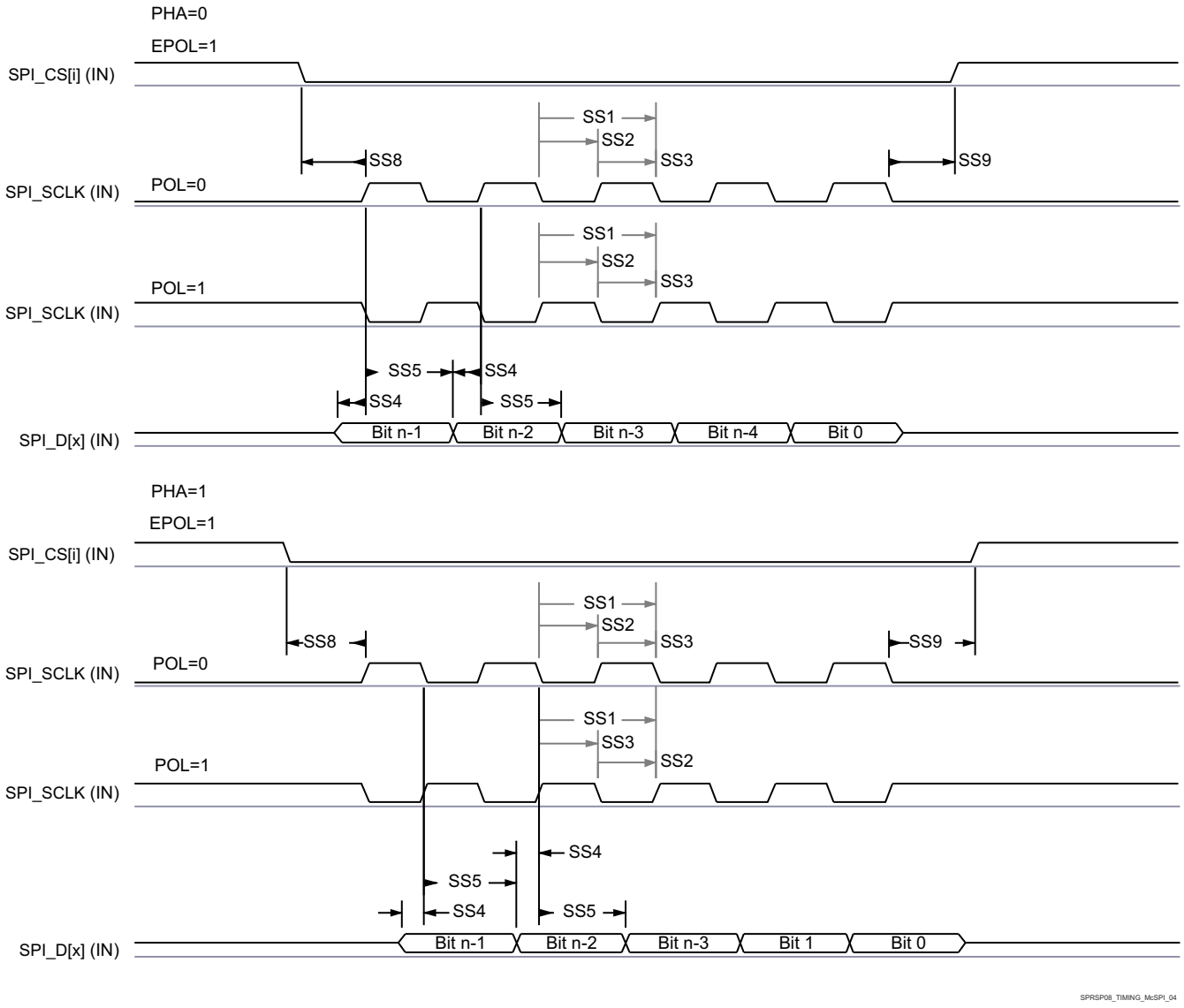


Figure 6-77. SPI Peripheral Mode Receive Timing

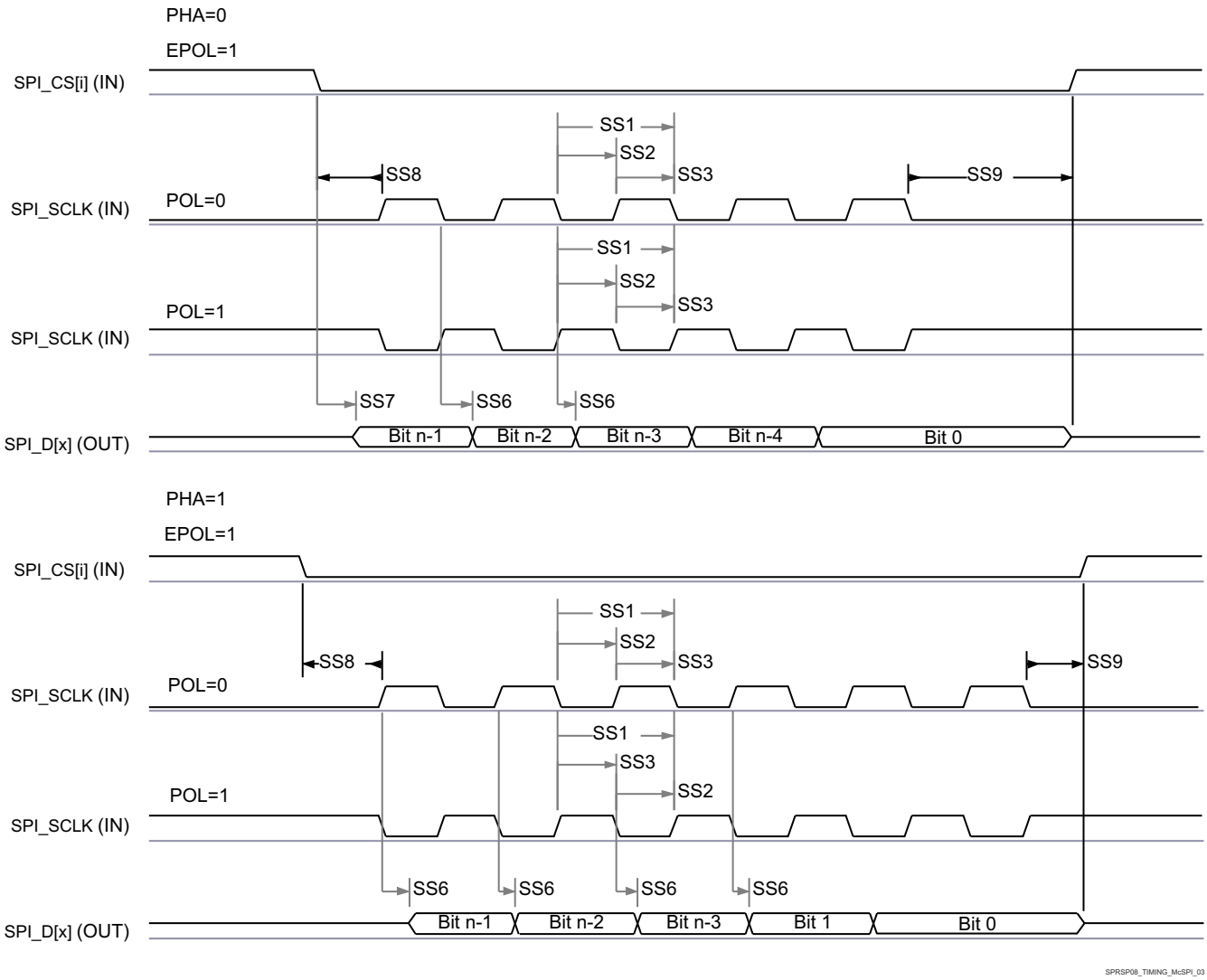


Figure 6-78. MCSPI Peripheral Mode Transmit Timing

Table 6-57 and Table 6-58 present the specific groupings of signals (IOSET) for use with MCU_SPI0 and MCU_SPI1.

Table 6-57. MCU_SPI0 IOSETs

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
MCU_SPI0_CLK	MCU_SPI0_CLK	0	MCU_SPI0_CLK	0
MCU_SPI0_D0	MCU_SPI0_D0	0	MCU_SPI0_D0	0
MCU_SPI0_D1	MCU_SPI0_D1	0	MCU_SPI0_D1	0
MCU_SPI0_CS0	MCU_SPI0_CS0	0	MCU_SPI0_CS0	0
MCU_SPI0_CS1	MCU_OSPI1_D3	5	WKUP_GPIO0_12	1
MCU_SPI0_CS2	MCU_OSPI1_CSn1	5	WKUP_GPIO0_14	1

Table 6-58. MCU_SPI1 IOSET

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
MCU_SPI1_CLK	MCU_SPI1_CLK	0	MCU_SPI1_CLK	0
MCU_SPI1_D0	MCU_SPI1_D0	0	MCU_SPI1_D0	0
MCU_SPI1_D1	MCU_SPI1_D1	0	MCU_SPI1_D1	0
MCU_SPI1_CS0	MCU_SPI1_CS0	0	MCU_SPI1_CS0	0
MCU_SPI1_CS1	MCU_OSPI1_D1	5	WKUP_GPIO0_13	1
MCU_SPI1_CS2	MCU_OSPI1_D2	5	WKUP_GPIO0_15	1

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

6.10.5.17 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 sections within

Signal Descriptions and *Detailed Description*.

Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in Table 6-59 and Table 6-71.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.10.5.17.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- High Speed HS200
- High Speed HS400

Table 6-59 presents the required DLL software configuration settings for MMC0 timing modes.

Table 6-59. MMC0 DLL Delay Mapping for All Timing Modes

REGISTER NAME		MMCSD0_MMC_SSCFG_PHY_CTRL_x_REG								
		x = 1	x = 4					x = 5		
BIT FIELD		[1]	[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]
BIT FIELD NAME		ENDLL	STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL
MODE	DESCRIPTION	ENABLE DLL	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL/ DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION
Legacy SDR	8-bit PHY operating 1.8V, 25MHz	0x0	0x0	0x0	NA(1)	0x1	0x10	0x1 or 0x3(2)	NA(3)	0x7
High Speed SDR	8-bit PHY operating 1.8V, 50MHz	0x0	0x0	0x0	NA(1)	0x1	0xA	0x1 or 0x3(2)	NA(3)	0x7
High Speed DDR	8-bit PHY operating 1.8V, 50MHz	0x1	0x0	0x1	0x6	0x1	Tuning(5)	0x0	0x4	NA(4)
HS200	8-bit PHY operating 1.8V, 200MHz	0x1	0x0	0x1	0x8	0x1	Tuning(5)	0x0	0x0	NA(4)
HS400	8-bit PHY operating 1.8V, 200MHz	0x1	0x66	0x1	0x5	0x1	Tuning(5)	0x0	0x0	NA(4)

(1) NA means this register field has no function when operating with half-cycle timing, which is required for this mode.
(2) The SELDLYTXCLK bit has no function when operating with half-cycle timing, which is required for this mode.
(3) NA means this register field has no function when ENDLL is set to 0x0.
(4) NA means this register field has no function when ENDLL is set to 0x1.
(5) Tuning means this mode requires a tuning algorithm to be used to determine optimal input timing

Table 6-60 presents timing conditions for MMC0.

Table 6-60. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR	0.14	1.44	V/ns
		High Speed SDR	0.3	0.90	V/ns
		High Speed DDR (CMD)	0.3	0.90	V/ns
		High Speed DDR (DAT[7:0])	0.45	0.90	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	HS200, HS400	1	6	pF
		All other modes	1	12	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	134	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	Legacy SDR, High Speed SDR, High Speed DDR		100	ps
		HS200, HS400		8	ps

6.10.5.17.1.1 Legacy SDR Mode

Table 6-61, Figure 6-79, Table 6-62, and Figure 6-80 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

Table 6-61. MMC0 Timing Requirements – Legacy SDR Mode

see Figure 6-79

NO.			MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.5		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	6.5		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.5		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	6.5		ns

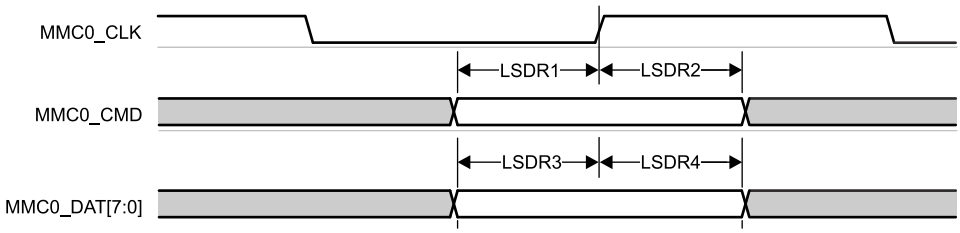


Figure 6-79. MMC0 – Legacy SDR – Receive Mode

Table 6-62. MMC0 Switching Characteristics – Legacy SDR Mode

see Figure 6-80

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	–3.2	3.8	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	–3.2	3.8	ns

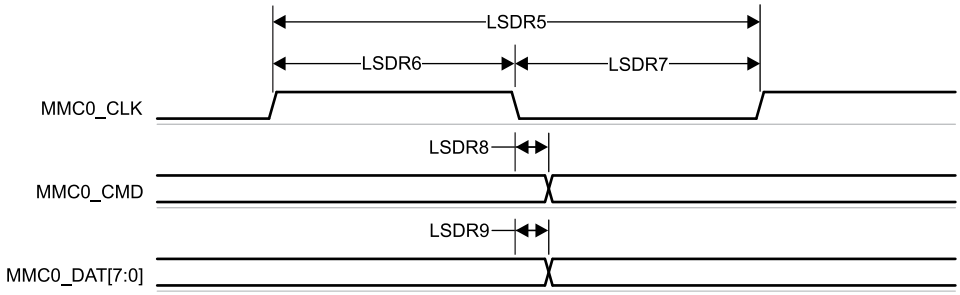


Figure 6-80. MMC0 – Legacy SDR – Transmit Mode

6.10.5.17.1.2 High Speed SDR Mode

Table 6-63, Figure 6-81, Table 6-64, and Figure 6-82 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

Table 6-63. MMC0 Timing Requirements – High Speed SDR Mode

see Figure 6-81

NO.			MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.99		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.99		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	2.67		ns

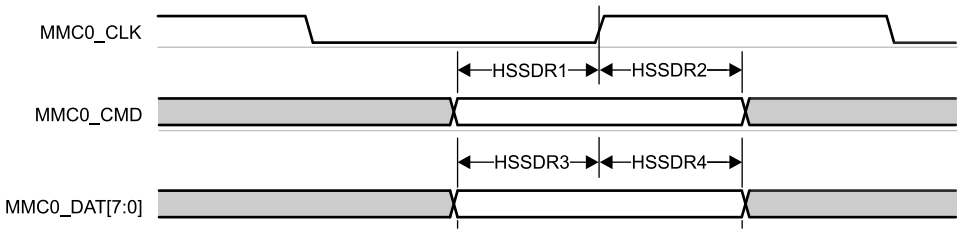


Figure 6-81. MMC0 – High Speed SDR Mode – Receive Mode

Table 6-64. MMC0 Switching Characteristics – High Speed SDR Mode

see Figure 6-82

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	–3.2	3.8	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	–3.2	3.8	ns

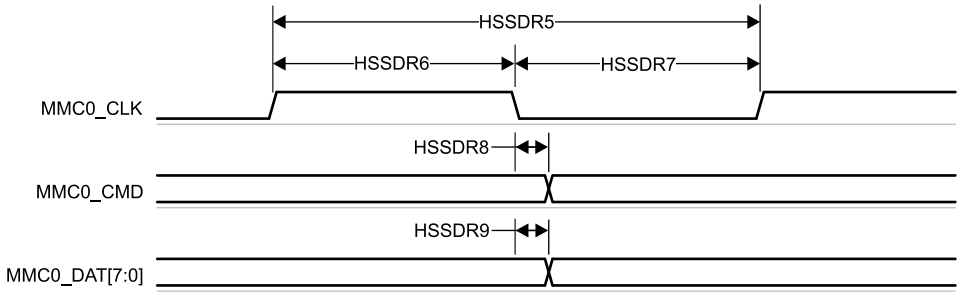


Figure 6-82. MMC0 – High Speed SDR Mode – Transmit Mode

6.10.5.17.1.3 High Speed DDR Mode

Table 6-65, Figure 6-83, Table 6-66, and Figure 6-84 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

Table 6-65. MMC0 Timing Requirements – High Speed DDR Mode

see Figure 6-83

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	3.79		ns
HSDDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSDDR3	$t_{su(dV-clkV)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.74		ns
HSDDR4	$t_{h(clkV-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.67		ns

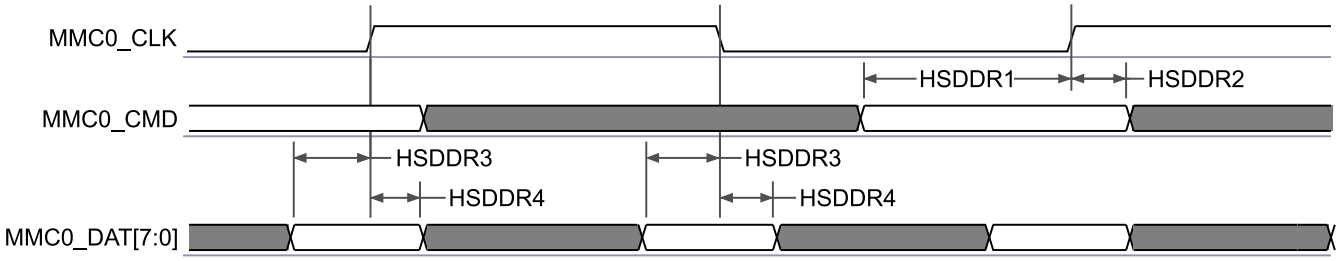


Figure 6-83. MMC0 – High Speed DDR Mode – Receive Mode

Table 6-66. MMC0 Switching Characteristics – High Speed DDR Mode

see Figure 6-84

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSDDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSDDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSDDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSDDR8	$t_{d(clkH-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	3.4	9.8	ns
HSDDR9	$t_{d(clkV-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	2.9	6.85	ns

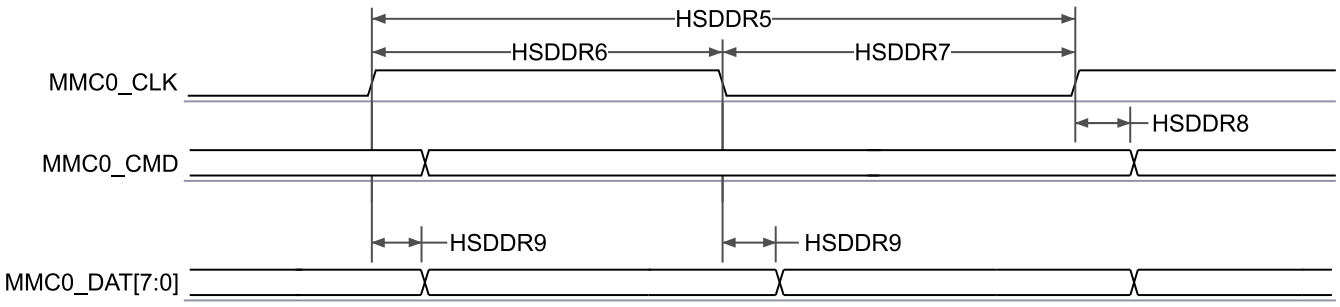


Figure 6-84. MMC0 – High Speed DDR Mode – Transmit Mode

6.10.5.17.1.4 HS200 Mode

Table 6-67, Figure 6-85, Table 6-68 and Figure 6-86 present both timing requirements and switching characteristics for MMC0 – HS200 Mode.

Table 6-67. MMC0 Timing Requirements – HS200 Mode

see Figure 6-85

NO.			MIN	MAX	UNIT
HS2004	t_{DVW}	Input data valid window, MMC0_CMD and MMC0_DAT[7:0]	2.0(1)		ns

(1) This parameter defines the minimum data valid window required by the host, where any data valid window presented to the host greater than this value ensures the host is able to capture valid data. The value defined by this parameter is smaller than the smallest possible data valid window defined for any eMMC device operating in HS200 mode.

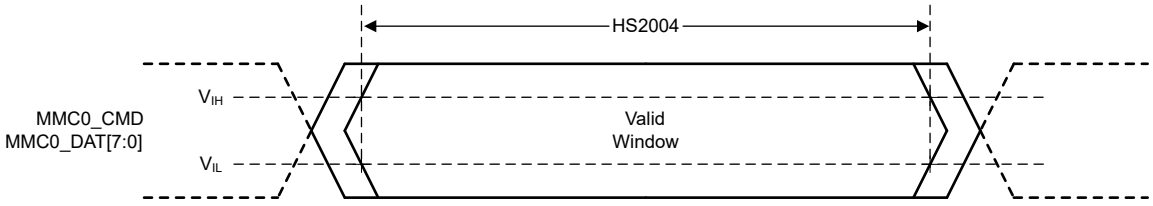


Figure 6-85. MMC0 – HS200 – Receive Mode

Table 6-68. MMC0 Switching Characteristics – HS200 Mode

see Figure 6-86

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.08		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.08		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	0.99	3.16	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	0.99	3.16	ns

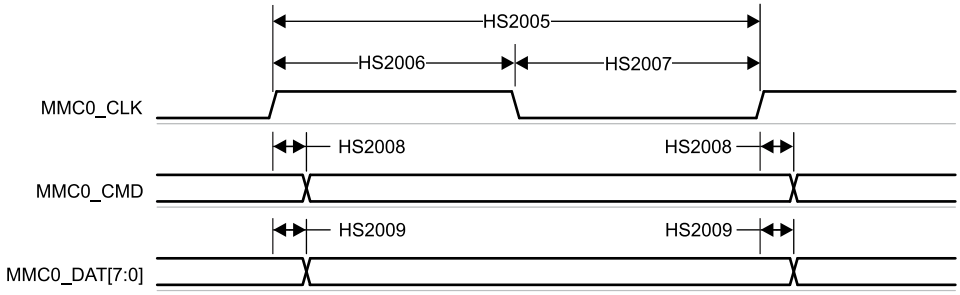


Figure 6-86. MMC0 – HS200 Mode – Transmit Mode

6.10.5.17.1.5 HS400 Mode

Table 6-69, Figure 6-87, Table 6-70, and Figure 6-88 present switching characteristics for MMC0 – HS400 Mode.

Table 6-69. MMC0 Timing Requirements – HS400 Mode

see Figure 6-87

NO.			MIN	MAX	UNIT
HS4000	t_{DSMPW}	Pulse width, MMC0_DS	1.95		ns
HS4001	t_{RQ_DAT}	Input skew, MMC0_DS to MMC0_DAT valid		475	ps
HS4002	t_{RQH_DAT}	Input skew hold, MMC0_DAT invalid to MMC0_DS		475	ps
HS4003	t_{RQ_CMD}	Input skew, MMC0_DS to MMC0_CMD valid		475	ps

Table 6-69. MMC0 Timing Requirements – HS400 Mode (continued)

see Figure 6-87

NO.			MIN	MAX	UNIT
HS4004	t_{RQH_CMD}	Input skew hold, MMC0_CMD invalid to MMC0_DS		475	ps

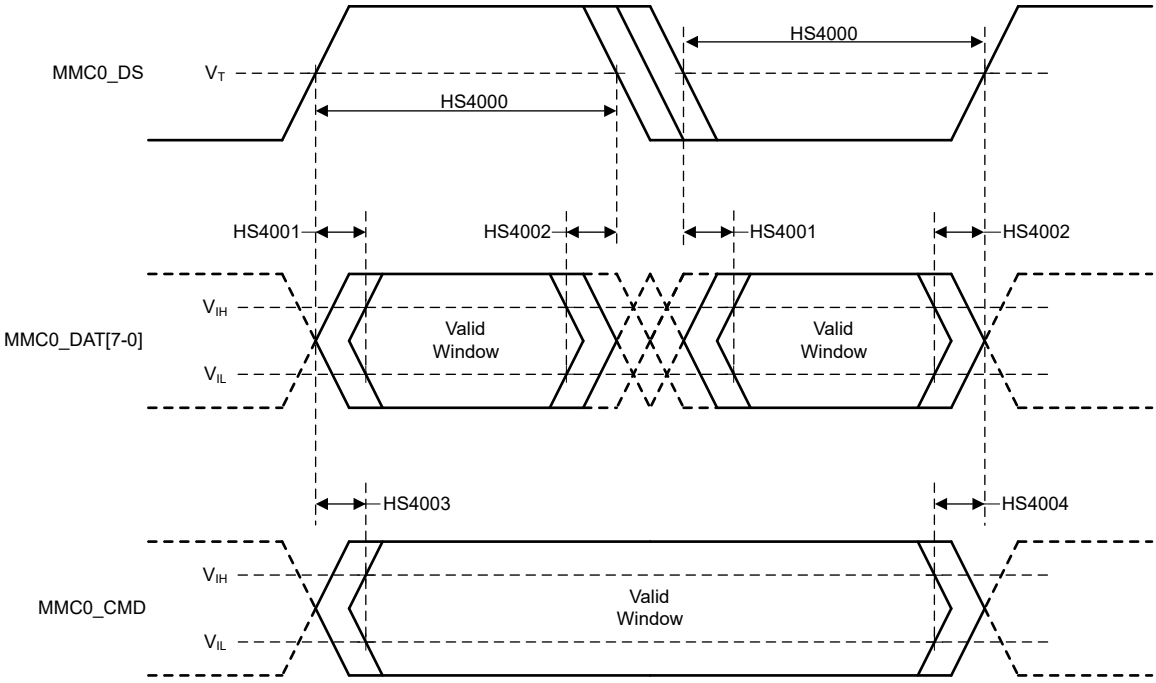


Figure 6-87. MMC0 – HS400 – Receive Mode

Table 6-70. MMC0 Switching Characteristics – HS400 Mode

see Figure 6-88

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS4005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS4006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.23		ns
HS4007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.23		ns
HS4008	$t_{osu(cmdV-clkH)}$	Output setup time, MMC0_CMD valid to MMC0_CLK rising edge(1)	2.54		ns
HS4009	$t_{osu(dV-clk)}$	Output setup time, MMC0_DAT[7:0] valid to MMC0_CLK rising or falling edge(1)	0.63		ns
HS4010	$t_{oh(clkH-cmdIV)}$	Output hold time, MMC0_CLK rising edge to MMC0_CMD invalid(2)	0.98		ns
HS4011	$t_{oh(clk-dIV)}$	Output hold time, MMC0_CLK rising or falling edge to MMC0_DAT[7:0] invalid(2)	0.72		ns

(1) This parameter defines the output setup time provided to the attached device. This time is relative to the next capture clock edge. The timing references for this parameter are from mid-supply of the DAT or CMD signal transition to mid-supply of the CLK signal transition. The eMMC standard defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to mid-supply of the CLK signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from mid-supply to VIL or VIH does not erode the setup time margin.

(2) This parameter defines the output hold time provided to the attached device. This time is relative to the previous launch clock edge. The timing references for this parameter are from mid-supply of the CLK signal transition to mid-supply of the DAT or CMD signal transition. The eMMC standard defines the hold timing references from mid-supply of the CLK signal transition to VIL or VIH of the DAT or CMD signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from VIL or VIH to mid-supply does not erode the hold time margin.

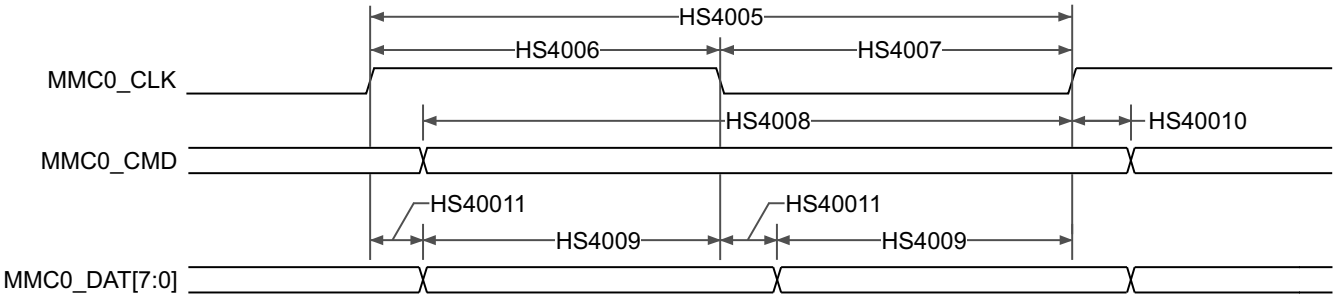


Figure 6-88. eMMC in – HS400 Mode – Transmitter Mode

6.10.5.17.2 MMC1 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and they support the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I SDR104
- UHS–I DDR50

Table 6-71 presents the required DLL software configuration settings for MMC1/2 timing modes.

Table 6-71. MMC1 DLL Delay Mapping for All Timing Modes

REGISTER NAME		MMCSD1_MMC_SSCFG_PHY_CTRL_4_REG			
BIT FIELD		[20]	[15:12]	[8]	[4:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE
Default Speed	4-bit PHY operating 3.3V, 25MHz	NA(1)	NA(1)	0x0	0x0
High Speed	4-bit PHY operating 3.3V, 50MHz	NA(1)	NA(1)	0x0	0x0
UHS-I SDR12	4-bit PHY operating 1.8V, 25MHz	0x1	0xF	0x0	0x0
UHS-I SDR25	4-bit PHY operating 1.8V, 50MHz	0x1	0xF	0x0	0x0
UHS-I SDR50	4-bit PHY operating 1.8V, 100MHz	0x1	0xC	0x1	Tuning(2)
UHS-I DDR50	4-bit PHY operating 1.8V, 50MHz	0x1	0xC	0x1	Tuning(2)
UHS-I SDR104	4-bit PHY operating 1.8V 200MHz	0x1	0x5	0x1	Tuning(2)

(1) NA means this register field has no function when operating with half-cycle timing, which is required for this mode.
(2) Tuning means this mode requires a tuning algorithm to be used to determine optimal input timing

Table 6-72 presents timing conditions for MMC1.

Table 6-72. MMC1 Timing Conditions

PARAMETER	MIN	MAX	UNIT
INPUT CONDITIONS			

Table 6-72. MMC1 Timing Conditions (continued)

PARAMETER			MIN	MAX	UNIT
SR_I	Input slew rate	Default Speed, High Speed	0.69	2.06	V/ns
		UHS–I SDR12, UHS–I SDR25	0.34	1.34	V/ns
		USH-1 DDR50	1.00	2.00	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	All modes	1	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	240.03	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	UHS–I DDR50		20	ps
		UHS–I SDR104		8	ps
		All other modes		100	ps

6.10.5.17.2.1 Default Speed Mode

Table 6-73, Figure 6-89, Table 6-74, and Figure 6-90 present timing requirements and switching characteristics for MMC1/2 – Default Speed Mode.

Table 6-73. MMC1/2 Timing Requirements – Default Speed Mode

see Figure 6-89

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	4.56		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	4.56		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

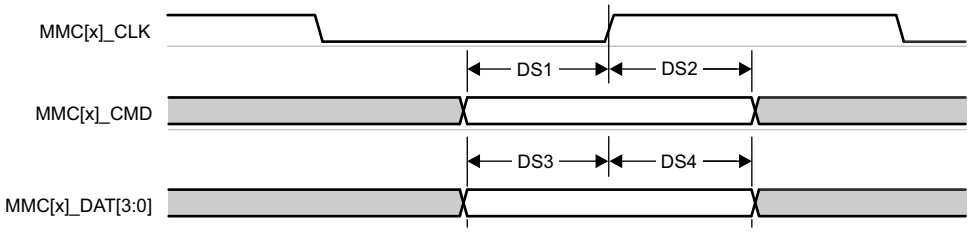


Figure 6-89. MMC1/2 – Default Speed – Receive Mode

Table 6-74. MMC1/2 Switching Characteristics – Default Speed Mode

see Figure 6-90

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition	–3.53	3.53	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition	–3.53	3.53	ns

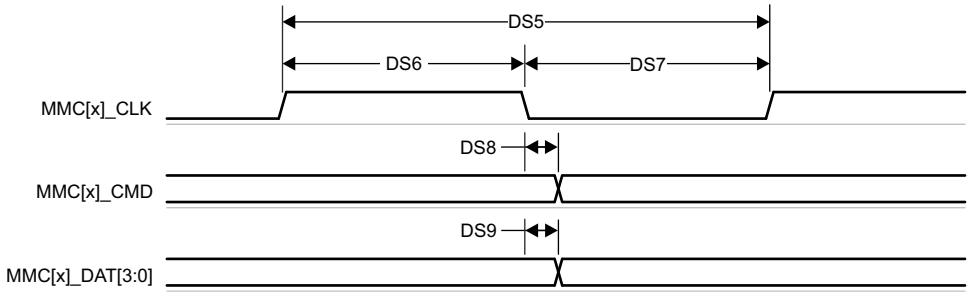


Figure 6-90. MMC1/2 – Default Speed – Transmit Mode

6.10.5.17.2.2 High Speed Mode

Table 6-75, Figure 6-91, Table 6-76, and Figure 6-92 present timing requirements and switching characteristics for MMC1/2 – High Speed Mode.

Table 6-75. MMC1/2 Timing Requirements – High Speed Mode

see Figure 6-91

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.15		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	2.26		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.15		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	2.26		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

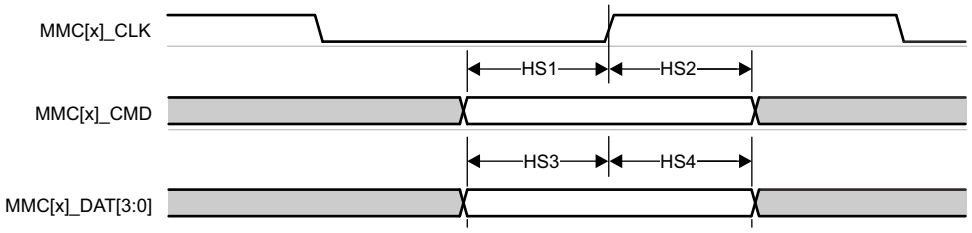


Figure 6-91. MMC1 /2– High Speed – Receive Mode

Table 6-76. MMC1/2 Switching Characteristics – High Speed Mode

see Figure 6-92

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMC[x]_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition	–2.07	2.07	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition	–2.07	2.07	ns

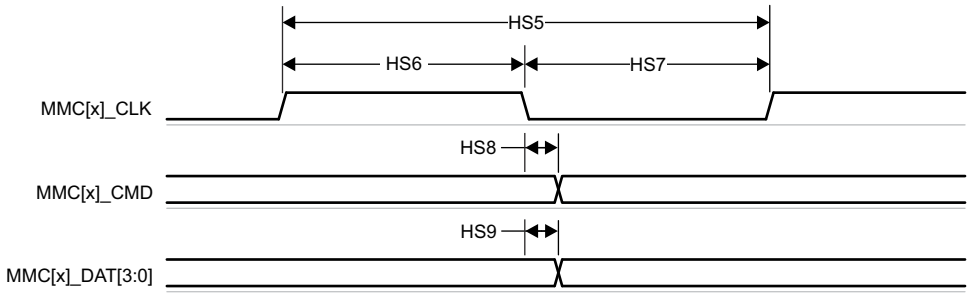


Figure 6-92. MMC1/2 – High Speed – Transmit Mode

6.10.5.17.2.3 UHS–I SDR12 Mode

Table 6-77, Figure 6-93, Table 6-78, and Figure 6-94 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR12 Mode.

Table 6-77. MMC1/2 Timing Requirements – UHS-I SDR12 Mode

see Figure 6-93

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	5.46		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	1.67		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	5.46		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	1.67		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

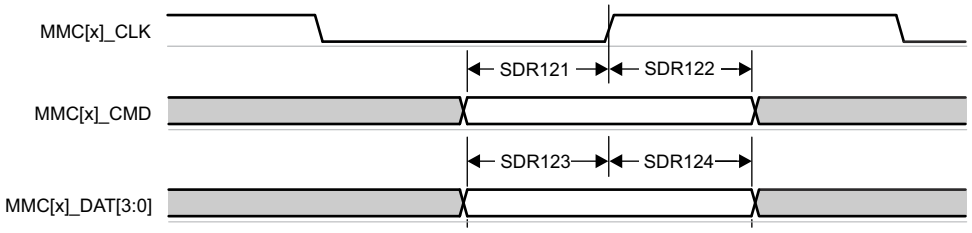


Figure 6-93. MMC1/2 – UHS-I SDR12 – Receive Mode

Table 6-78. MMC1/2 Switching Characteristics – UHS-I SDR12 Mode

see Figure 6-94

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	18.7		ns
SDR128	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.2	13.55	ns
SDR129	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.2	13.55	ns

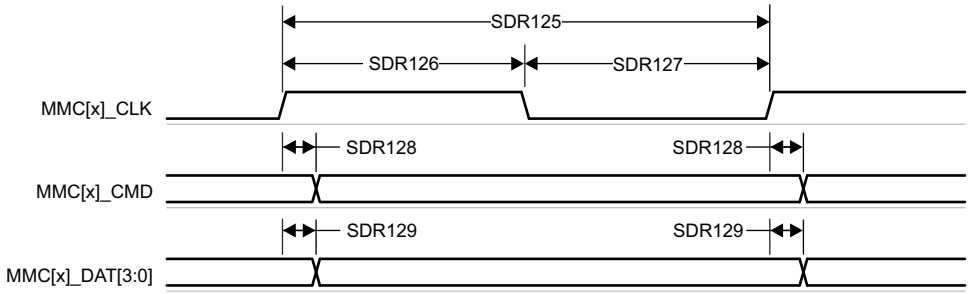


Figure 6-94. MMC1/2 – UHS-I SDR12 – Transmit Mode

6.10.5.17.2.4 UHS–I SDR25 Mode

Table 6-79, Figure 6-95, Table 6-80, and Figure 6-96 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR25 Mode.

Table 6-79. MMC1/2 Timing Requirements – UHS-I SDR25 Mode

see Figure 6-95

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.1		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	1.67		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.1		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	1.67		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

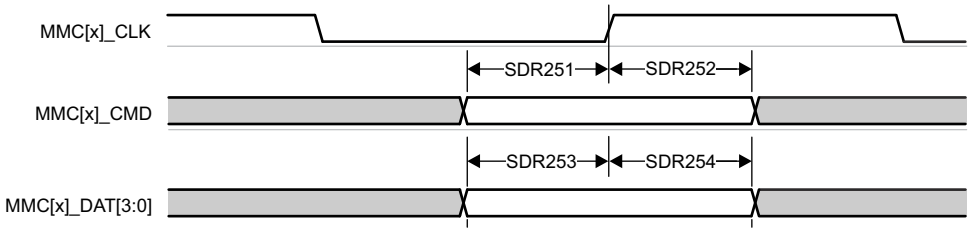


Figure 6-95. MMC1/2 – UHS-I SDR25 – Receive Mode

Table 6-80. MMC1/2 Switching Characteristics – UHS-I SDR25 Mode

see Figure 6-96

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
SDR258	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	2.4	9.37	ns
SDR259	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	2.4	9.37	ns

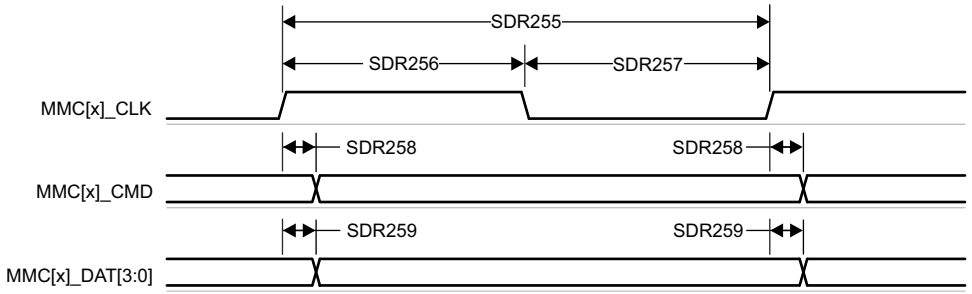


Figure 6-96. MMC1/2 – UHS-I SDR25 – Transmit Mode

6.10.5.17.2.5 UHS–I SDR50 Mode

Table 6-81, and Figure 6-97 presents switching characteristics for MMC1/2 – UHS-I SDR50 Mode.

Table 6-81. MMC1/2 Switching Characteristics – UHS-I SDR50 Mode

see Figure 6-97

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	4.45		ns
SDR508	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.2	6.35	ns

A. x = 1, 2 for MMC1 and MMC2

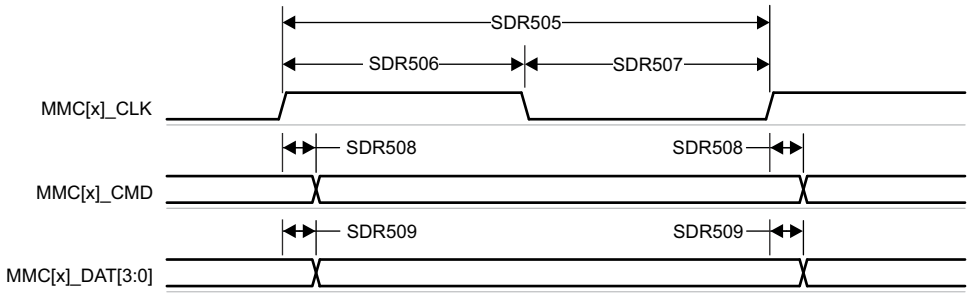


Figure 6-97. MMC1/2 – UHS-I SDR50 – Transmit Mode

6.10.5.17.2.6 UHS–I DDR50 Mode

Table 6-82 and Figure 6-98 present switching characteristics for MMC1/2 – UHS-I DDR50 Mode.

Table 6-82. MMC1/2 Switching Characteristics – UHS-I DDR50 Mode

see Figure 6-98

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
DDR508	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.12	3.46	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMC[x]_CLK transition to MMC[x]_DAT[3:0] transition	1.12	6.12	ns

A. x = 1, 2 for MMC1 and MMC2

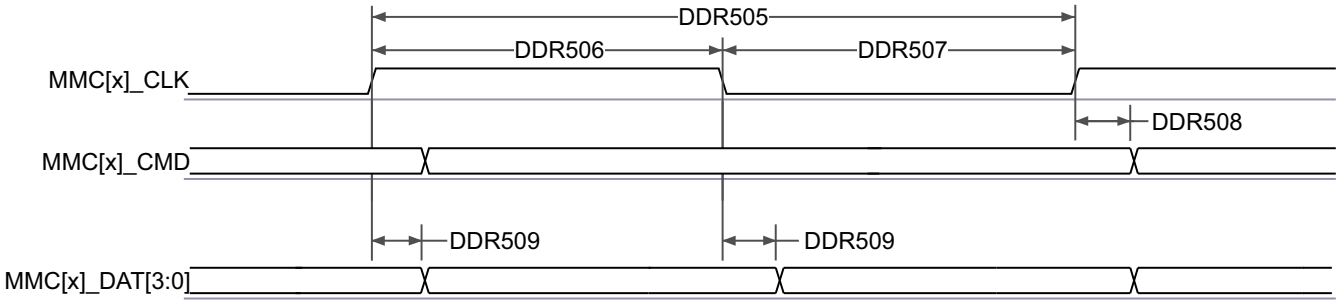


Figure 6-98. MMC1/2 – UHS-I DDR50 – Transmit Mode

6.10.5.17.2.7 UHS–I SDR104 Mode

Table 6-83, and Figure 6-99 present switching characteristics for MMC1/2 – UHS-I SDR104 Mode.

Table 6-83. MMC1/2 Switching Characteristics – UHS-I SDR104 Mode

see Figure 6-99

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	2.12		ns
SDR1048	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.07	3.21	ns

A. x = 1, 2 for MMC1 and MMC2

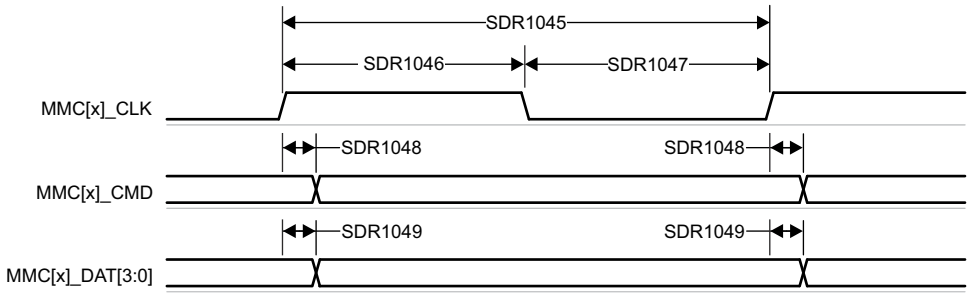


Figure 6-99. MMC1/2 – UHS-I SDR104 – Transmit Mode

6.10.5.18 CPTS

Table 6-84 represents CPTS timing conditions.

Table 6-84. CPTS Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

Section 6.10.5.18.1, Section 6.10.5.18.2, Figure 6-100, and Figure 6-101 present timing requirements and switching characteristics of the CPTS interface.

6.10.5.18.1 CPTS Timing Requirements

see Figure 6-100

NO.			MIN	MAX	UNIT
T1	$t_{w(HWnTSPUSHH)}$	Pulse duration, HWnTSPUSH(2) high	12P + 2(1)		ns
T2	$t_{w(HWnTSPUSHL)}$	Pulse duration, HWnTSPUSH(2) low	12P + 2(1)		ns
T3	$t_{c(RFT\_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT\_CLKH)}$	Pulse duration, RFT_CLK high	0.45 * T(3)		ns
T5	$t_{w(RFT\_CLKL)}$	Pulse duration, RFT_CLK low	0.45 * T(3)		ns

(1) P = functional clock period in ns.
(2) In HWnTSPUSH, n = 1 to 2.
(3) T = RFT_CLK period in ns.

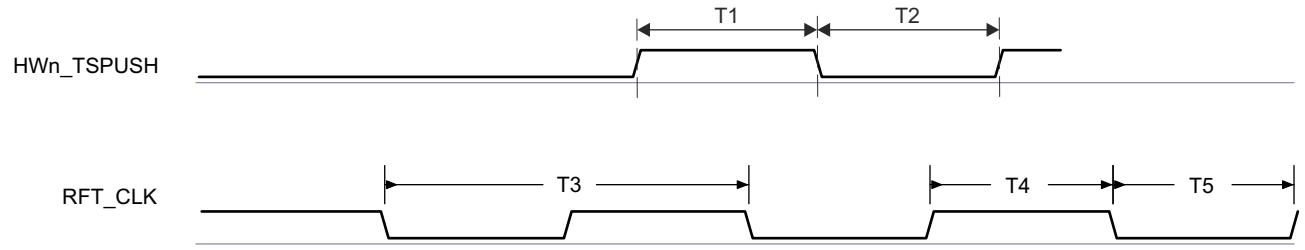


Figure 6-100. CPTS Timing Requirements

6.10.5.18.2 CPTS Switching Characteristics

see Figure 6-101

NO.	PARAMETER		SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS\_COMPH)}$	Pulse duration, TS_COMP high		36P - 2[1]		ns
T7	$t_{w(TS\_COMPL)}$	Pulse duration, TS_COMP low		36P - 2[1]		ns
T8	$t_{w(TS\_SYNCH)}$	Pulse duration, TS_SYNC high		36P - 2[1]		ns
T9	$t_{w(TS\_SYNCL)}$	Pulse duration, TS_SYNC low		36P - 2[1]		ns
T10	$t_{w(SYNC\_OUTH)}$	Pulse duration, SYNCn_OUT[2] high	TS_SYNC	36P - 2[1]		ns
			TS_GENF	5P - 2[1]		ns
T11	$t_{w(SYNC\_OUTL)}$	Pulse duration, SYNCn_OUT[2] low	TS_SYNC	36P - 2[1]		ns
			TS_GENF	5P - 2[1]		ns

(1) P = functional clock period in ns.
(2) n = 0 to 3 in SYNCn_OUT

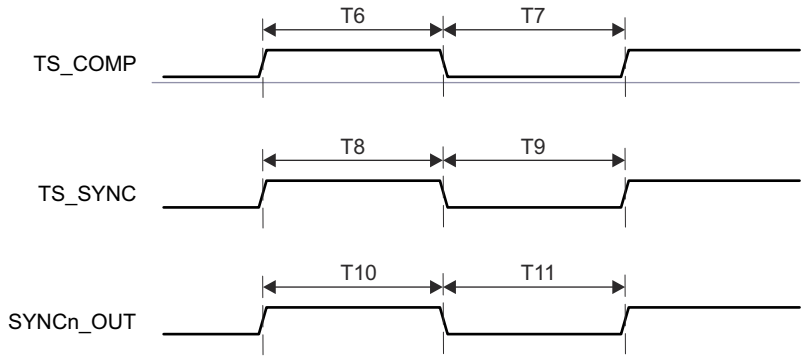


Figure 6-101. CPTS Switching Characteristics

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

6.10.5.19 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-85 represents OSPI timing conditions.

Table 6-85. OSPI Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	3.3V, all modes	2	6	V/ns
		1.8V, PHY Data Training DDR with DQS	0.75	6	V/ns
		1.8V, all other modes	1	6	V/ns

Table 6-85. OSPI Timing Conditions (continued)

PARAMETER			MIN	MAX	UNIT
OUTPUT CONDITIONS					
C_L	Output load capacitance	All modes	3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay OSPI_CLK trace	No Loopback; Internal Pad Loopback		450	ps
	Propagation delay OSPI_LBCLKO trace	External Board Loopback	2*L-30(2)	2*L+30(2)	ps
	Propagation delay OSPI_DQS trace	DQS	L-30(2)	L+30(2)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch OSPI_D[i:0](1), OSPI_CSn relative to OSPI_CLK	All modes		60	ps

(1) i in D[i:0] = 0 to 7 for OSPI0; i in [i:0] = 3 for OSPI1
(2) L = Propagation delay of OSPI_CLK trace

6.10.5.19.1 OSPI0/1 PHY Mode

6.10.5.19.1.1 OSPI0/1 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

Table 6-86 defines DLL delays required for OSPI0/1 with Data Training. Table 6-87, Figure 6-102, Figure 6-103, Table 6-88, Figure 6-104, and Figure 6-105 present timing requirements and switching characteristics for OSPI0/1 with Data Training.

Table 6-86. OSPI0/1 DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

Table 6-87. OSPI0 Timing Requirements – PHY Data Training

see Figure 6-102, and Figure 6-103

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	SDR with Internal PHY Loopback	(1)		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	SDR with Internal PHY Loopback	(1)		ns
	t_{DVW}	Data valid window (O15 + O16)	1.8V, DDR with DQS	1.4		ns
		Data valid window (O21 + O22)	1.8V, SDR with Internal PHY Loopback	1.7		ns

(1) Minimum setup and hold time requirements for OSPI0/1_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window. The t_{DVW} parameter defines the minimum data invalid window required. This parameter is provided in lieu of minimum setup and minimum hold times, where it must be used to check compatibility with the data valid window provided by an attached device.

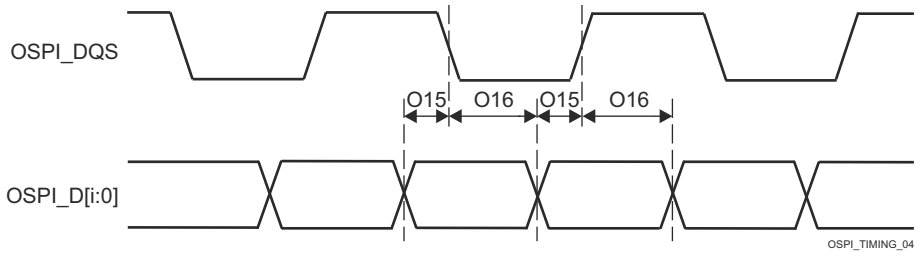


Figure 6-102. OSPI0/1 Timing Requirements – PHY Data Training, DDR with DQS

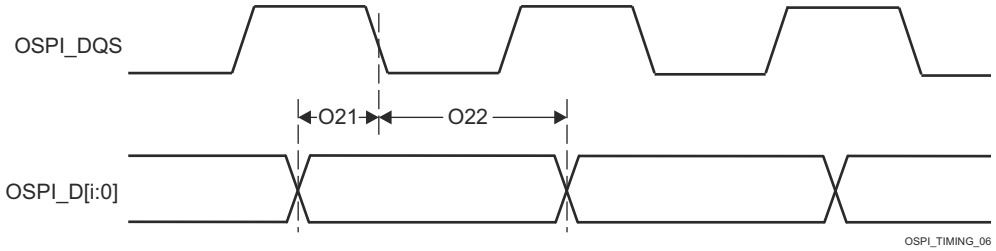


Figure 6-103. OSPI0/1 Timing Requirements – PHY Data Training, SDR with Internal PHY Loopback

Table 6-88. OSPI/1 Switching Characteristics – PHY Data Training

See Figure 6-104 and Figure 6-105

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0/1_CLK	1.8V, DDR	6.0	6.0	ns
O7			1.8V, SDR	6.0	6.0	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0/1_CLK low	DDR	((0.475P(1)) - 0.3)		ns
O8			SDR			
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0/1_CLK high	DDR	((0.475P(1)) - 0.3)		ns
O9			SDR			
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge	DDR	((0.475P(1)) + (0.975M(2)R(4)) + (0.028TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.055TD(5)) + 1)	ns
O10			SDR			
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge	DDR	((0.475P(1)) + (0.975N(3)R(4)) - (0.055TD(5)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) - (0.028TD(5)) + 1)	ns
O11			SDR			
O6	$t_{d(CLK-D)}$	Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition	DDR	(6)	(6)	ns
O12			SDR			
	t_{DIVW}	Data invalid window (O6 Max - Min)	DDR		1	ns
		Data invalid window (O12 Max - Min)	SDR			

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window. The t_{DIVW} parameter defines the maximum data invalid window. This parameter is provided in lieu of minimum and maximum delay times, where it must be used to check compatibility with the data valid window requirements of an attached device.

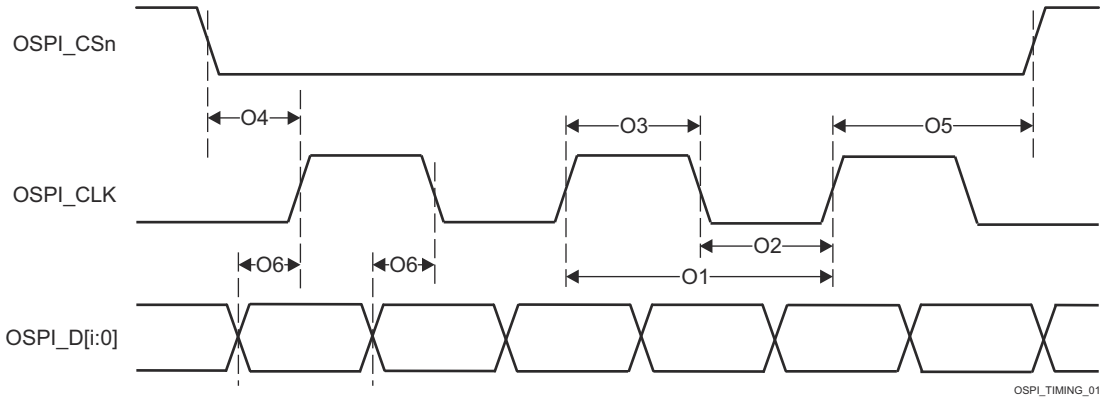


Figure 6-104. OSPI0/1 Switching Characteristics – PHY DDR Data Training

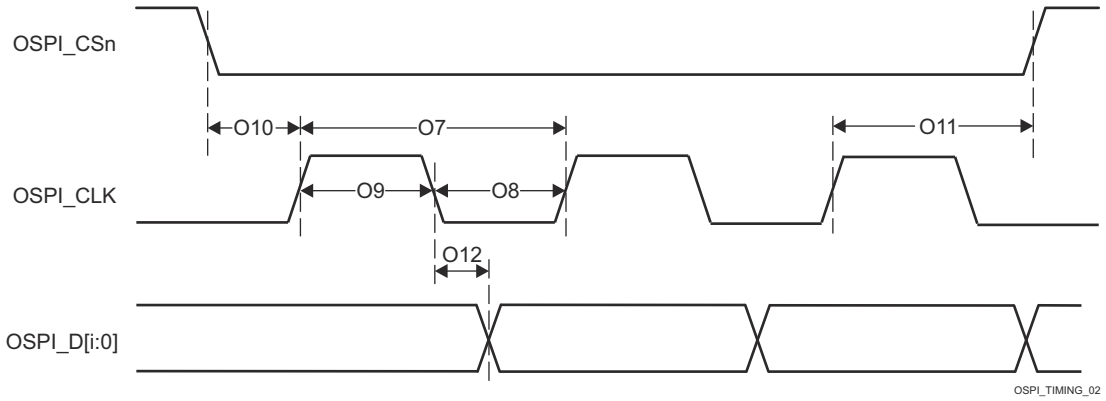


Figure 6-105. OSPI0/1 Switching Characteristics – PHY SDR Data Training

6.10.5.19.1.2 OSPI Without Data Training

Note

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in Table 6-89 found in this section.

Section 6.10.5.19.1.2.4, Section 6.10.5.19.1.2.2, Section 6.10.5.19.1.2, and Section 6.10.5.19.1.2 present switching characteristics for OSPI DDR and SDR Mode.

6.10.5.19.1.2.1 OSPI Timing Requirements – SDR Mode

Table 6-89. OSPI DLL Delay Mapping - SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	0x0
	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

Table 6-90. OSPI Timing Requirements – SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O21	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK input (DQS) edge(1)	1.8V, External Board Loopback	0.6		ns
			3.3V, External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK input (DQS) edge(1)	1.8V, External Board Loopback	1.7		ns
			3.3V, External Board Loopback	2		ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

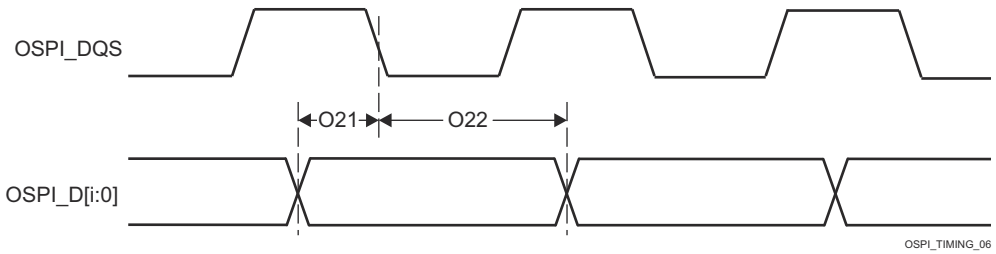


Figure 6-106. OSPI Timing Requirements – SDR, External Loopback Clock

6.10.5.19.1.2.2 OSPI Switching Characteristics – SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, CLK	1.8V	7		ns
			3.3V	7.5		ns

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O8	$t_{w(CLKL)}$	Pulse duration, CLK low		((0.475P[1]) - 0.3)		ns
O9		Pulse duration, CLK high		((0.475P[1]) - 0.3)		ns
O10	$t_{td(CSn-CLK)}$	Delay time, CSn active edge to CLK rising edge	1.8V	((0.475P[1]) + (0.975M[2]R[4]) + (0.028TD[5]) - 1)	((0.525P[1]) + (1.025M[2]R[4]) + (0.055TD[5]) + 1)	ns
			3.3V	((0.475P[1]) + (0.975M[2]R[4]) + (0.028TD[5]) - 1)	((0.525P[1]) + (1.025M[2]R[4]) + (0.055TD[5]) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	1.8V	((0.475P[1]) + (0.975N[3]R[4]) - (0.055TD[5]) - 1)	((0.525P[1]) + (1.025N[3]R[4]) - (0.028TD[5]) + 1)	ns
			3.3V	((0.475P[1]) + (0.975N[3]R[4]) - (0.055TD[5]) - 1)	((0.525P[1]) + (1.025N[3]R[4]) - (0.028TD[5]) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, CLK active edge to D[i:0] transition[6]	1.8V	–1.16	1.25	ns
			3.3V	–1.33	1.51	ns

(1) P = CLK cycle time = SCLK period
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = refclk
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

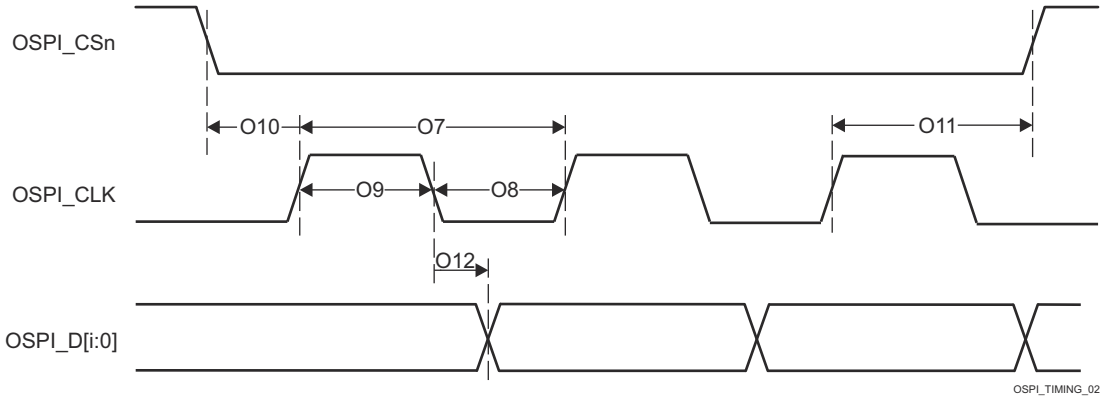


Figure 6-107. OSPI Switching Characteristics – SDR

Section 6.10.5.19.1.2.3, Section 6.10.5.19.1.2.1, Section 6.10.5.19.1.2.2, Section 6.10.5.19.1.2.2, and Figure 6-106 presents timing requirements for OSPI DDR and SDR Mode.

6.10.5.19.1.2.3 OSPI Timing Requirements – DDR Mode

Table 6-91. OSPI DLL Delay Mapping - DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	OSPI0	OSPI1
		DELAY VALUE	
TRANSMIT			
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x54	0x54

Table 6-91. OSPI DLL Delay Mapping - DDR Timing Modes (continued)

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	OSPI0	OSPI1
		DELAY VALUE	
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x55	0x5C
RECEIVE			
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x23	0x29
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x47	0x42
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0	0x0

Table 6-92. OSPI Timing Requirements – DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK (DQS) edge(1)	1.8V, External Board Loopback	0.52		ns
			3.3V, External Board Loopback	1.97		ns
O16	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK (DQS) edge(1)	1.8V, External Board Loopback	1.24 (2)		ns
			3.3V, External Board Loopback	1.44 (2)		ns
O17	$t_{su(D-DQS)}$	Setup time, DQS edge to D[i:0] transition(1)	1.8V, DQS	–0.46		ns
			3.3V, DQS	–0.66		ns
O18	$t_{h(DQS-D)}$	Hold time, DQS edge to D[i:0] transition(1)	1.8V, DQS	3.59		ns
			3.3V, DQS	8.89		ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. Refer to OSPI and QSPI Board Design and Layout Guidelines for more details.

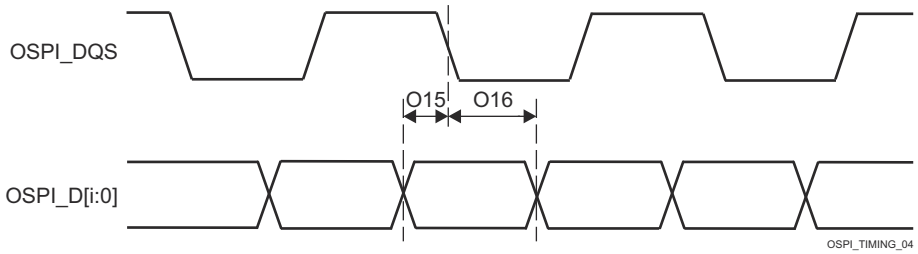


Figure 6-108. OSPI Timing Requirements – DDR, External Loopback Clock and DQS

6.10.5.19.1.2.4 OSPI Switching Characteristics – PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, CLK	1.8V	19		ns
			3.3V	19		ns
O2	$t_{w(CLKL)}$	Pulse duration, CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CLK-CSn)}$	Delay time, CSn active edge to CLK rising edge	1.8V	((0.475P(1)) + (0.975M(2)R(4)) + (0.028TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.055TD(5)) + 1)	ns
			3.3V	((0.475P(1)) + (0.975M(2)R(4)) + (0.028TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.055TD(5)) + 1)	ns

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O5	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	1.8V	((0.475P[1]) + (0.975N[3]R[4]) + (0.055TD[5]) - 1)	((0.525P[1]) + (1.025N[3]R[4]) + (0.028TD[5]) + 1)	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	((0.475P[1]) + (0.975N[3]R[4]) + (0.055TD[5]) - 1)	((0.525P[1]) + (1.025N[3]R[4]) + (0.028TD[5]) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, CLK active edge to D[i:0] transition[6]	1.8V, OSPI0 DDR TX; 1.8V, OSPI1 DDR TX	–7.71	–1.56	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	–7.71	–1.56	ns

(1) P = CLK cycle time = SCLK period
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

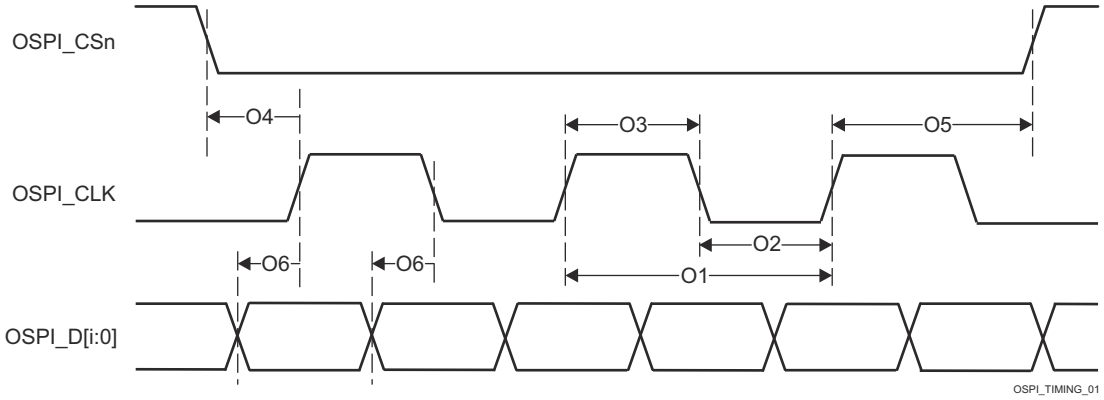


Figure 6-109. OSPI Switching Characteristics – DDR

6.10.5.19.2 OSPI0/1 Tap Mode

6.10.5.19.2.1 OSPI0 Tap SDR Timing

Table 6-93, Figure 6-110, Table 6-94, and Figure 6-111 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

Table 6-93. OSPI0/1 Timing Requirements – Tap SDR Mode

see Figure 6-110

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge	No Loopback	(15.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge	No Loopback	(–5.2 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

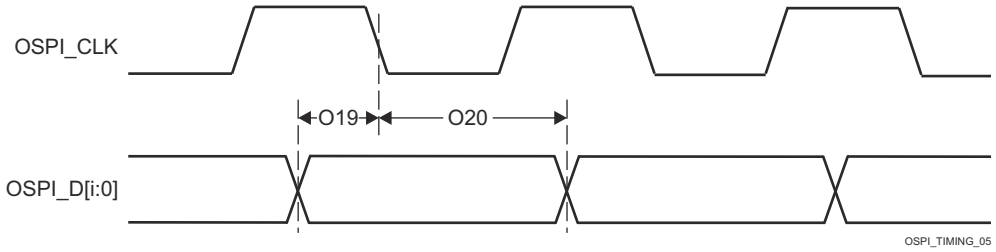


Figure 6-110. OSPI0/1 Timing Requirements – Tap SDR, No Loopback

Table 6-94. OSPI0/1 Switching Characteristics – Tap SDR Mode

see Figure 6-111

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0/1_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0/1_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0/1_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition		–2	2	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

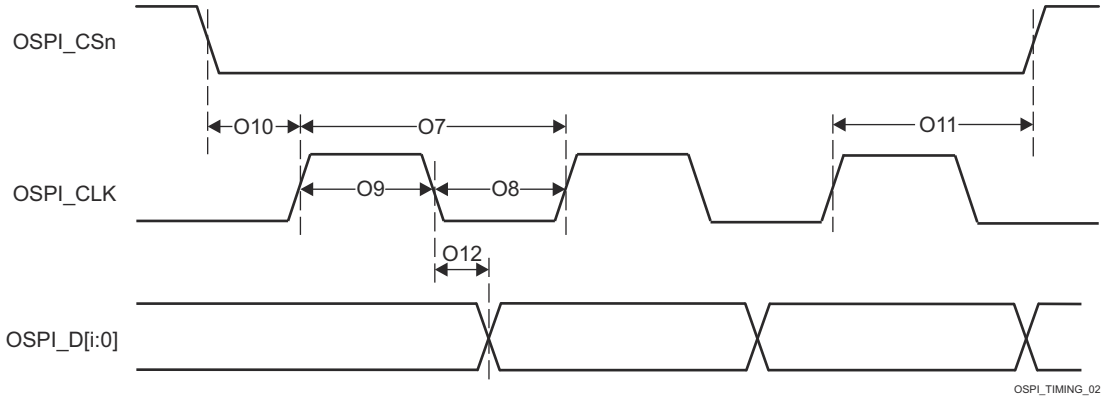


Figure 6-111. OSPI0/1 Switching Characteristics – Tap SDR, No Loopback

6.10.5.19.2.2 OSPI0 Tap DDR Timing

Table 6-95, Figure 6-112, Table 6-96, and Figure 6-113 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

Table 6-95. OSPI0/1 Timing Requirements – Tap DDR Mode

see Figure 6-112

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge	No Loopback	(17.04 - (0.975T(1)R(2)))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge	No Loopback	(–3.16 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

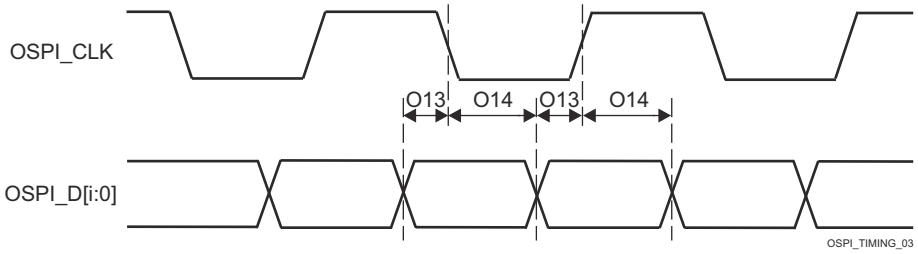


Figure 6-112. OSPI0/1 Timing Requirements – Tap DDR, No Loopback

Table 6-96. OSPI0/1 Switching Characteristics – Tap DDR Mode

see Figure 6-113

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0/1_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0/1_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0/1_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge		((0.475P(1)) + ((0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition		(–5.04 + (0.975(T(5) + 1)R(4)) - (0.525P(1)))	(3.64 + (1.025(T(5) + 1)R(4)) - (0.475P(1)))	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]

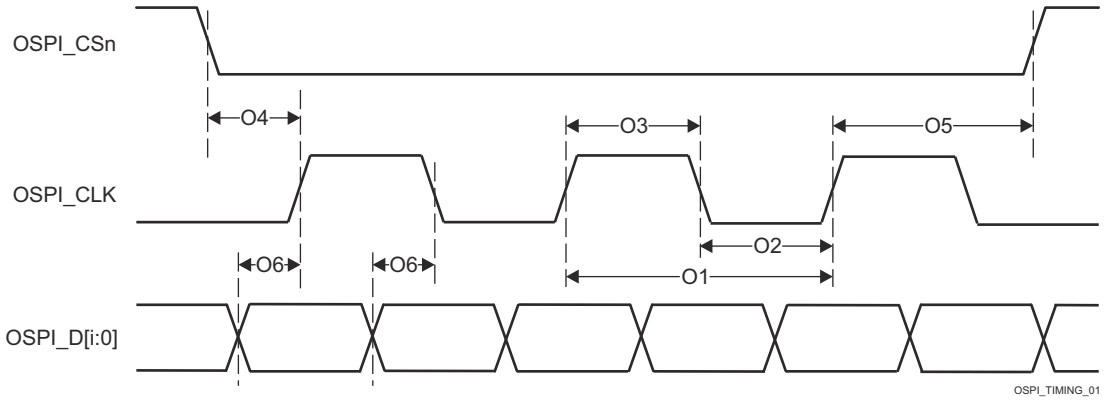


Figure 6-113. OSPI0/1 Switching Characteristics – Tap DDR, No Loopback

6.10.5.20 OLDI

6.10.5.20.1 OLDI Switching Characteristics

NO.	PARAMETER	MODE	MIN	MAX	UNIT
O1	LVDS Low-to-High Transition Time max	IOSET1	0.18	0.5	ns
O2	LVDS high-to-low Transition Time max	IOSET1	0.18	0.5	ns
O3	Transmitter Output Bit Width min	IOSET1	1	1	UI
O4	Transmitter Pulse Positions – Normalized	IOSET1	0.25	0.75	ns
O5	Variation in transmitter pulse position across Bit 7:0 pulse positions	IOSET1	-0.06	0.06	ns
O6	TxOut Channel to Channel Skew	IOSET1		110	ns
O7	Transmitter Jitter Cycle-to-Cycle	IOSET1	0.028	0.035	ns
O8	Input Total Jitter Tolerance (Includes data to clock skew, pulse position variation.)	IOSET1		0.25	ns

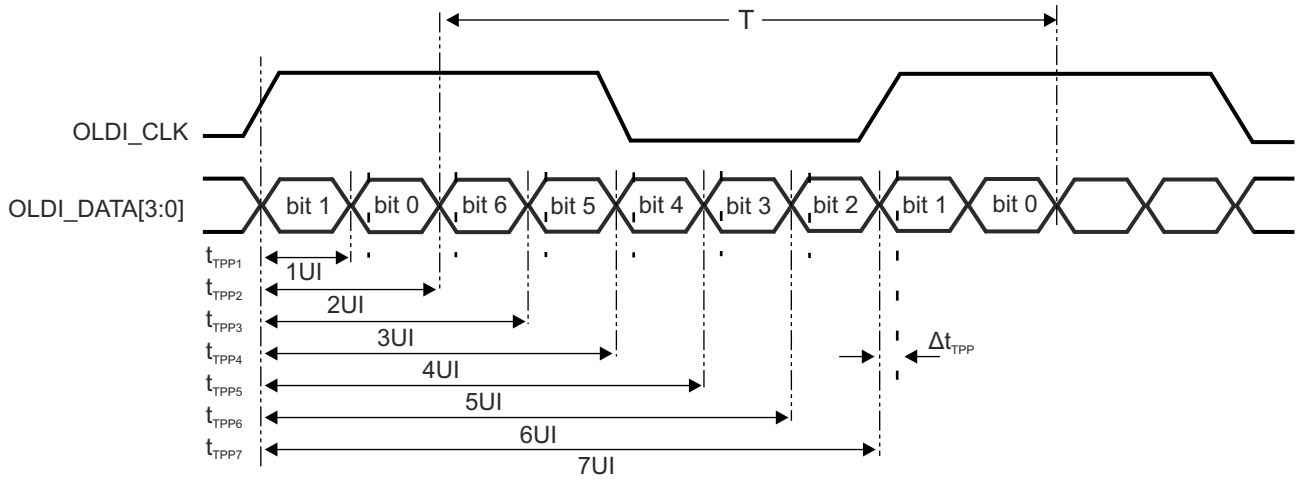


Figure 6-114. OLDI Transmitter Pulse Positions

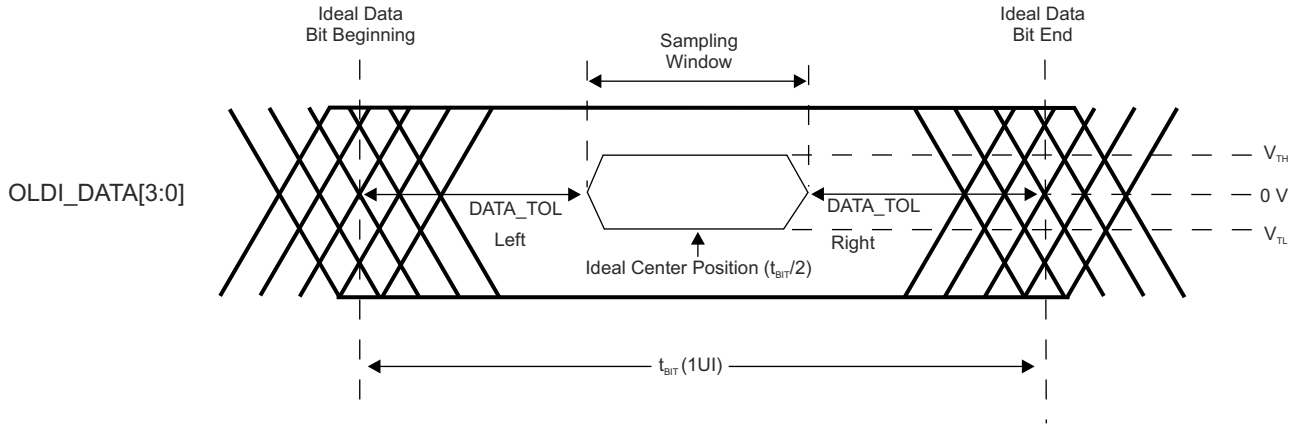


Figure 6-115. OLDI Data Output Jitter

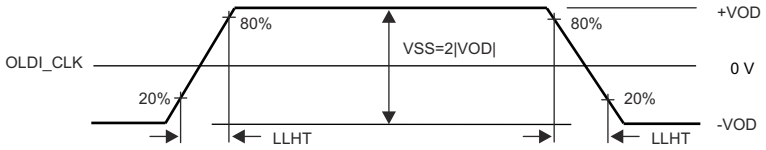


Figure 6-116. LVDS Output Transition Times

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

6.10.5.21 PCIE

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within Signal Descriptions and *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

6.10.5.22 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Table 6-97 represents Timers timing conditions.

Table 6-97. Timers Timing Conditions

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	CAPTURE	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	PWM	2	10	pF

Section 6.10.5.22.1, Section 6.10.5.22.2 and Figure 6-117 present timings and switching characteristics of the Timers.

6.10.5.22.1 Timing Requirements for Timers

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	2.5 + 4P (1)		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	2.5 + 4P (1)		ns

(1) P = functional clock period in ns.

6.10.5.22.2 Switching Characteristics for Timers

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	-2.5 + 4P (1)		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	-2.5 + 4P (1)		ns

(1) P = functional clock period in ns.

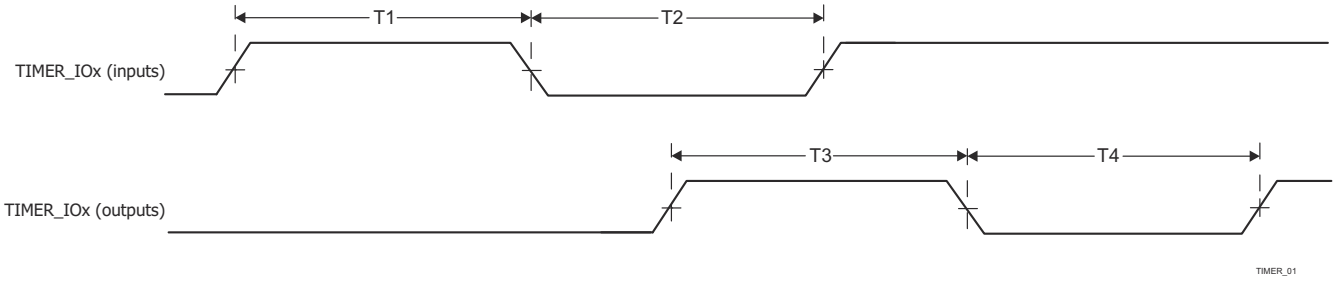


Figure 6-117. Timer Timing

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

6.10.5.23 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within , Signal Descriptions and *Detailed Description*.

Table 6-98 represents UART timing conditions.

Table 6-98. UART Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				

Table 6-98. UART Timing Conditions (continued)

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

Section 6.10.5.23.1, Section 6.10.5.23.2, and Figure 6-118 present timing requirements and switching characteristics for UART interface.

6.10.5.23.1 Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
4	$t_{w(rxd)}$	Pulse width, receive data bit, high or low		0.95U(1) (2)	1.05U(1) (2)	ns
5	$t_{w(rxdS)}$	Pulse width, receive start bit, low		0.95U(1) (2)		ns

(1) U = UART baud time = 1/Programmed baud rate
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

6.10.5.23.2 UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Maximum programmable baud rate		12	Mbps
2	$t_{w(TX)}$	Pulse width, transmit data bit, high or low	U - 2(1)	U + 2(1)	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, high or low	U - 2(1)		ns

(1) U = UART baud time = 1/Programmed baud rate

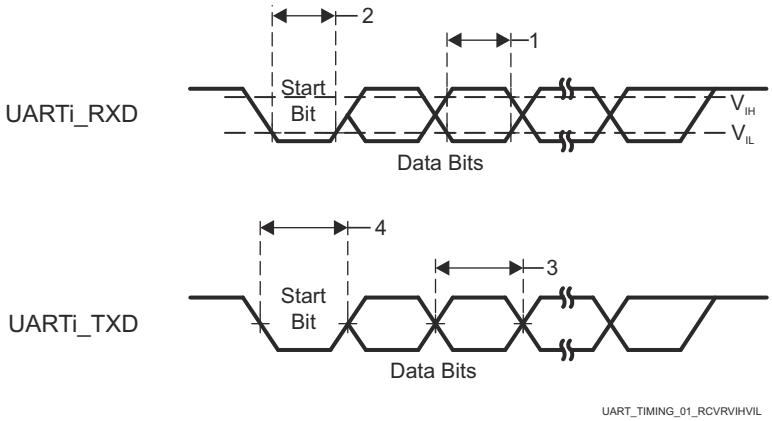


Figure 6-118. UART Timing

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

6.10.5.24 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within Signal Descriptions and *Detailed Description*.

6.10.6 Emulation and Debug

6.10.6.1 Trace

Note

DEBUG0 has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Table 6-99. Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces		200	ps

Table 6-100 and Figure 6-119 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 6-100. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8 V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.50		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.50		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.50		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.81		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.81		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.81		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.81		ns
3.3 V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	9.75		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	4.13		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	4.13		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.22		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.22		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.22		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.22		ns

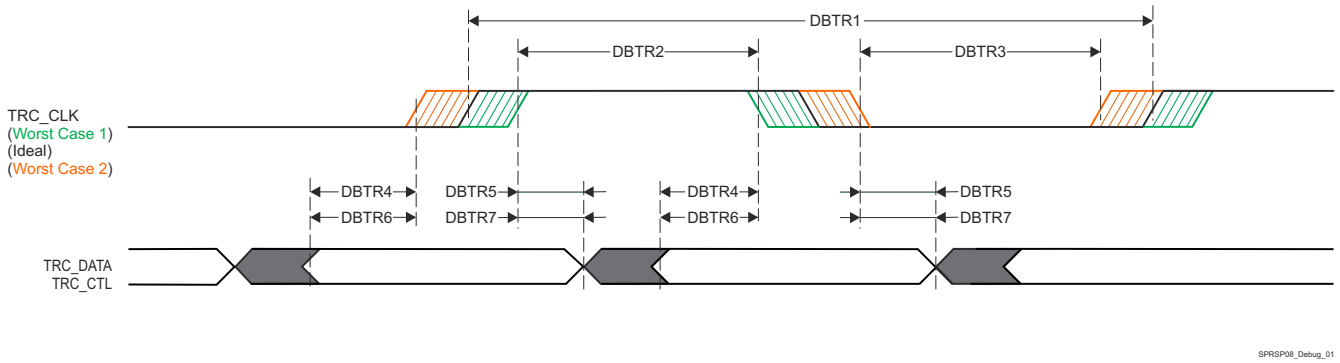


Figure 6-119. Trace Switching Characteristics

6.10.6.2 JTAG

For more details about features and additional description information on the device IEEE 1149.1 Standard–Test–Access Port, see the corresponding sections within Signal Descriptions and *Detailed Description*.

Note

The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this section only apply when the two IO power domains are operating at the same voltage and level-shifters are not inserted into the signal path. Values for the following timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8 V while others are operating at 3.3 V. This effectively reduces timing margin beyond the values defined in this section. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level-shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

Table 6-101. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
Input Conditions				
SR_I	Input slew rate	0.50	2.00	V/ns
Output Conditions				
C_L	Output load capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

6.10.6.2.1 JTAG Electrical Data and Timing

Section 6.10.6.2.1.1, Section 6.10.6.2.1.2, and Figure 6-120 assume testing over the recommended operating conditions and electrical characteristic conditions.

6.10.6.2.1.1 JTAG Timing Requirements

See Figure 6-120

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	46.5(1)		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	18.6(2)		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	18.6(2)		ns

See Figure 6-120

NO.			MIN	MAX	UNIT
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	4.5		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	4.5		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	2		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	2		ns

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 4.6 ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of –16.5 ns to 14.0 ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

6.10.6.2.1.2 JTAG Switching Characteristics

See Figure 6-120

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		12	ns

1. The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this table only apply when the two IO power domains are operating at the same voltage. Values for these timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this table. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

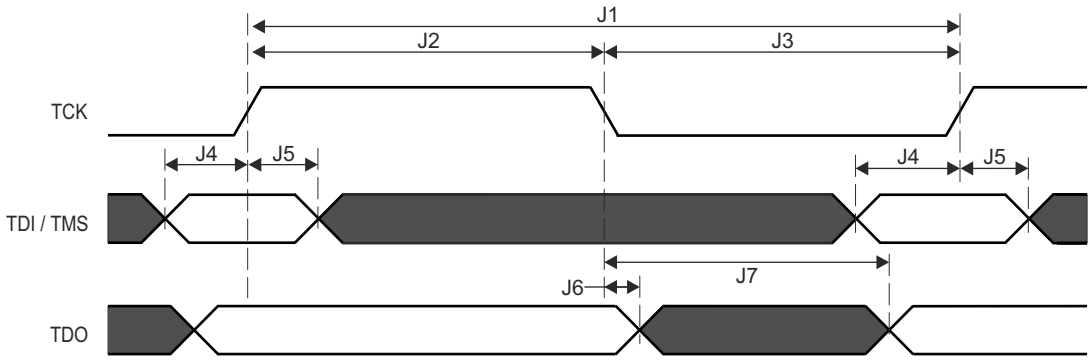


Figure 6-120. JTAG Timing Requirements and Switching Characteristics

7 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

7.1.1 Power Supply Decoupling and Bulk Capacitors

7.1.1.1 Power Distribution Network Implementation Guidance

The Powering Jacinto™ J7 SoC Family For Isolated Power Groups With TPS6594133A-Q1 PMIC and Dual HCPS Converters User's Guide provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

7.1.2 External Oscillator

For more information about External Oscillators, see Clock Specifications.

7.1.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For more recommendations on EMU routing, see Emulation and Trace Headers Technical Reference Manual

7.1.4 Reset

The device incorporates four external reset pins (MCU_PORz, MCU_RESETz, PORz, and RESET_REQz) and two reset status pins (MCU_RESETSTATz and RESETSTATz). These pins can be driven by an external power good circuitry or Power Management IC (PMIC). MCU_PORz and Main PORz pins should be held active low during the entire power-up phase, and until all power supplies as well as the HFOSC0 clock are stable.

All MCU domain resets act as master resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets).

7.1.5 Unused Pins

For more information about Unused Pins, see Pin Connectivity Requirements.

7.1.6 Hardware Design Guide for Jacinto™ 7 Devices

The Hardware Design Guide for Jacinto™ 7 Devices document describes hardware system design considerations for the Jacinto™ 7 family of processors.This design guide is intended to be used as an aid during the development of application hardware.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 LPDDR4 Board Design and Layout Guidelines

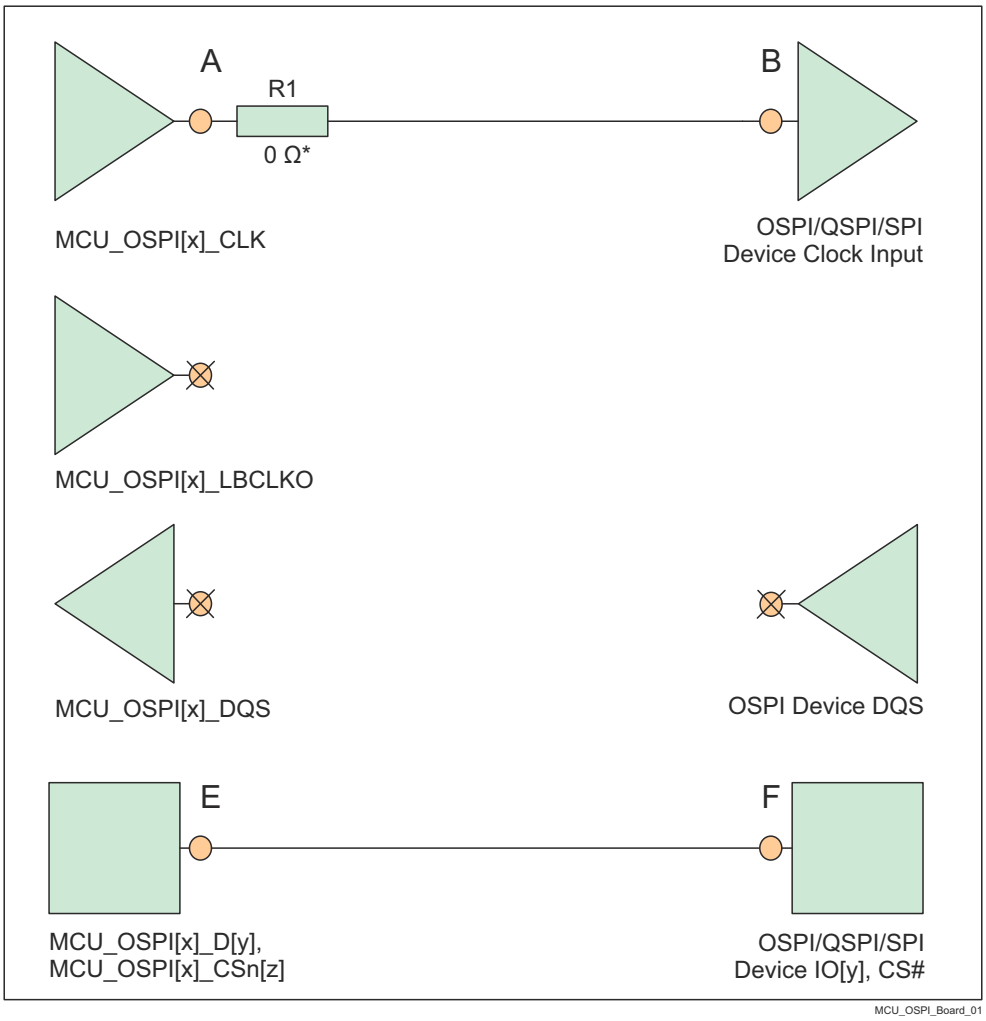
The goal of the Jacinto 7 DDR Board Design and Layout Guidelines is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

7.2.2 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

7.2.2.1 No Loopback and Internal Pad Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU_OSPI[x]_CLK signal to the flash device must be < 450 ps (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 7-1
- Propagation delays and matching:
  - A to B < 450 ps
  - Matching skew: < 60 ps



* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

Figure 7-1. OSPI Interface High Level Schematic

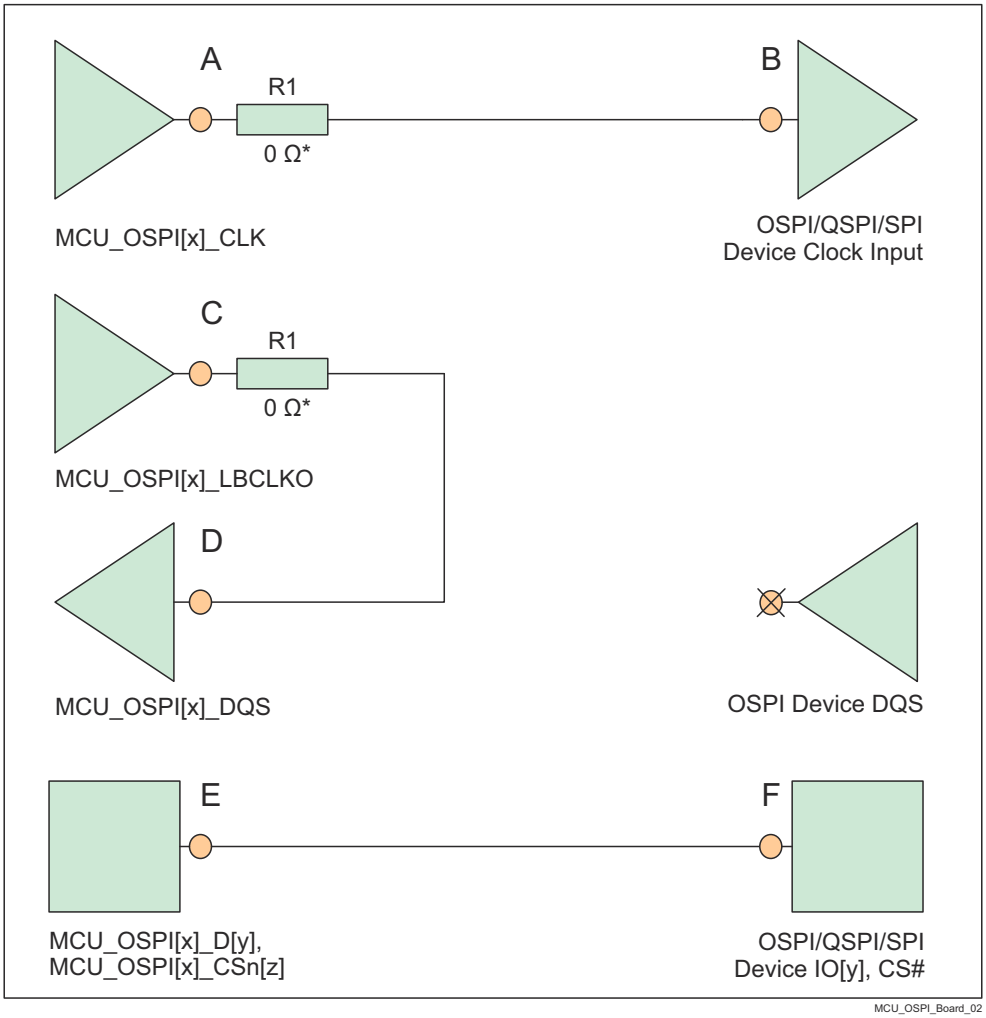
7.2.2.2 External Board Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The MCU_OSPI[x]_LBCLKO output signal must be looped back into the MCU_OSPI[x]_DQS input

- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU_OPSI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 7-2
- Propagation delays and matching:
  - A to B = E to F = (C to D) / 2
  - Matching skew: < 60 ps

Note

The OSPI Board Loopback Hold time requirement (described in OSPI) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU_OPSI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin (C to D) can be shortened to compensate.

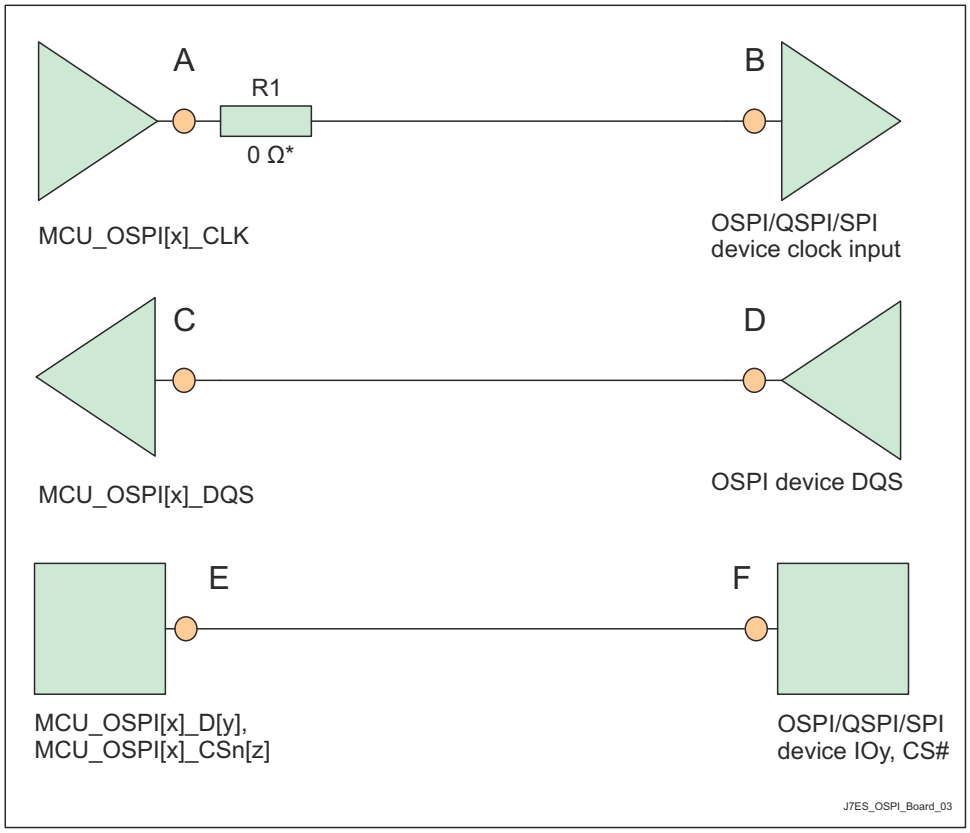


* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK and MCU_OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

Figure 7-2. OSPI Interface High Level Schematic

7.2.2.3 DQS (only available in Octal Flash devices)

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU_OSPI[x]_DQS signal
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU_OSPI[x]_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 7-3
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60 ps



* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

Figure 7-3. OSPI Interface High Level Schematic

7.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the Figure 7-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.(1)

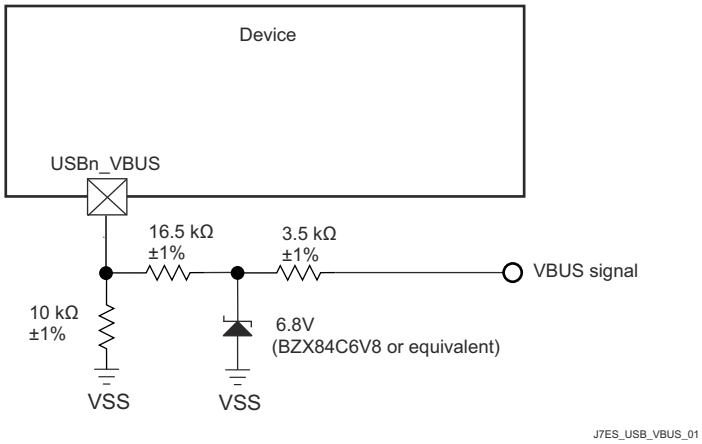


Figure 7-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in Figure 7-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

7.2.4 System Power Supply Monitor Design Guidelines using VMON/POK

The VMON1_ER_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON1_ER_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit. When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON1_ER_VSYS input threshold which has a nominal value of 0.45 V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON1_ER_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON1_ER_VSYS input leakage current may be in the range of 10 nA to 2.5 µA when applying 0.45 V.

Note

The resistor voltage divider shall be designed such that its output voltage never exceeds the maximum value defined in Recommended Operating Conditions during normal operating conditions.

Figure 7-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON1_ER_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON1_ER_VSYS pin is 2.5 µA. When implementing a resistor divider where R1 = 4.81 KΩ and R2 = 40.2 KΩ, the result is a maximum trigger threshold of 4.523 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input

leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON1_ER_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100 mV of this range is introduced by loading error when VMON1_ER_VSYS input leakage current is 2.5 µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON1_ER_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in Figure 7-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

Figure 7-5 presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V.

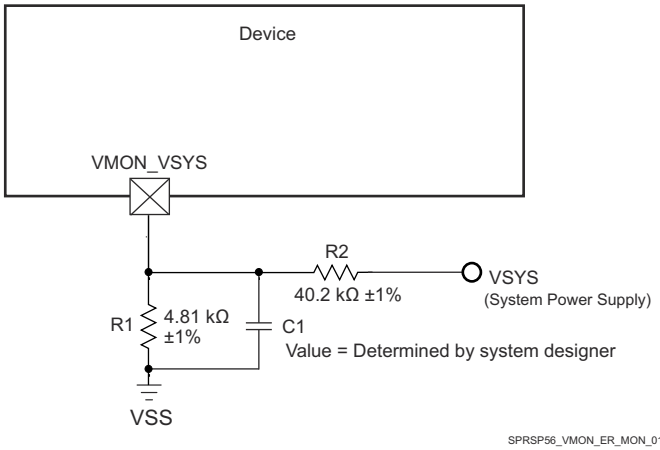


Figure 7-5. System Supply Monitor Voltage Divider Circuit

The **VMON2_IR_VCPU** pin provides a way to monitor VDD_CPU power supply. TI recommends that **VMON2_IR_VCPU** pin be externally connected as close as possible to VDD_CPU pin on the board. SoCs that have a **VMON6_IR_VEXT0P8** can optionally monitor other domains such as VDD_CORE or VDD_MCU. Similarly, those signals should be as close as possible to VDD_CORE or VDD_MCU pin on the board.

The **VMON3_IR_VEXT1P8** and **VMON4_IR_VEXT1P8** pins provide a way to monitor an external 1.8-V power supply. The **VMON5_IR_VEXT3P3** pin provides a way to monitor an external 3.3-V power supply. An internal resistor divider with software control is implemented inside the SoC. Software can program the internal resistor divider to create appropriate under voltage and over voltage interrupts. These pins should not be sourced from an external resistor divider. If the monitored voltage requires adjustment, be sure to buffer the divided voltage prior connecting to monitor pin.

7.2.5 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

7.2.6 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA4APE6T5AANDRQ1). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA4VM devices in the ALF package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

8.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

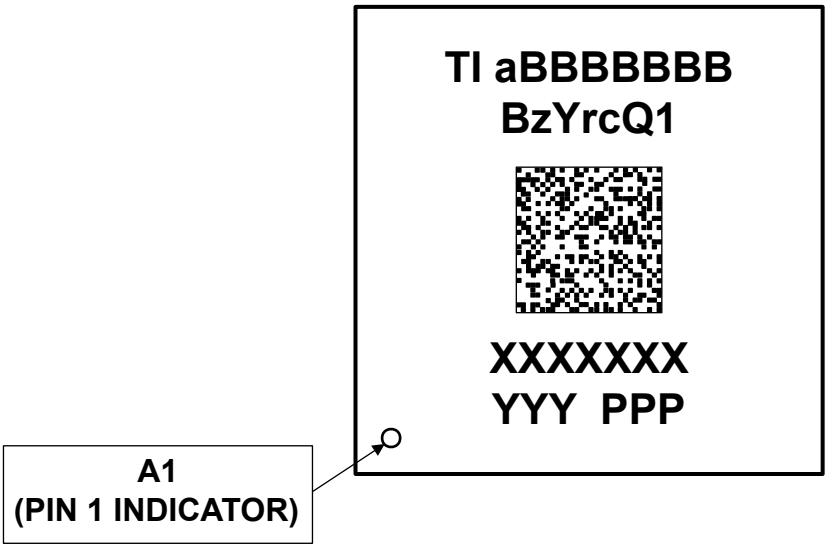


Figure 8-1. Printed Device Reference

8.1.2 Device Naming Convention

Table 8-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
x	Device evolution stage(1)	X		Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK		Production
BBBBBBBB(2)	Base production part number	J742S2(2)		Preproduction superset device
		TDA4VPE6		See Table 4-1, *Device Comparison*
		TDA4VPE4		
		TDA4APE6		
		TDA4APE4		
z	Device Speed	T		See Table 6-1, *Speed Grade Maximum Frequency*.
		OTHER		Alternate speed grade
Y	Device type	G		General purpose
		C		General purpose, R5F Lockstep capable
		0		High Security(3) capable
		5		High Security(3) capable, R5F Lockstep capable
		D		High Security(3) capable, R5F Lockstep capable, Customer Dev Keys. Only available on preproduction devices.
r	Device revision	A or BLANK		SR 1.0
PPP	Package designator	AND		AND FCBGA (27mm x 27mm) Package
c	Carrier designator	N/A	BLANK	Tray
		N/A	R	Tape and Reel
Q1	Automotive Designator	BLANK		Not automotive qualified. Supports T_J = –40°C to 105°C
		Q1		Meet AEC-Q100 qualification requirements, with exceptions as specified in this document (data sheet). Supports T_J = –40°C to 125°C
	2D Barcode	Varies		Optional 2D barcode, provides additional device information
		BLANK		
XXXXXXX	Lot Trace Code	As Marked	N/A	Lot Trace Code (LTC)
YYY	Production Code	As Marked	N/A	Production Code, for TI use only
O	Pin One	As Marked	N/A	Pin one designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) J742S2 is the base part number for the preproduction superset device. Software should constrain the features used to match the intended production device.

(3) For HS device support, TI recommends the 0, 5, or D device types.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

8.2 Tools and Software

The following products support development for TDA4VPE-Q1/TDA4APE-Q1 platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin mux tool The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

eMMC™ is a trademark of MultiMediaCard Association.
Jacinto™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
PCI-Express® is a registered trademark of PCI-SIG.
Secure Digital® is a registered trademark of SD Card Association.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from December 13, 2024 to September 16, 2025 (from Revision A (DECEMBER 2024) to Revision B (SEPTEMBER 2025)) **Page**

- (Features): Updated/Changed the Functional Safety bullets to include the received Functional Safety-Compliant certification.... 1
- (Features): Updated/Changed the Arm® Cortex®-R5F MCUs I-Cache and D-Cache memory from "16K" to "32K".... 1
- (Recommended Operating Conditions): Added VPP_*, eFuse ROM programming supply row; plus, associated footnotes.... 118
- (SERDES Electrical Characteristics): Updated the "USXGMII supports … "Note.... 126
- Added VDD_CPU row.... 127
- Updated VPP_CORE and VPP_MCU rows.... 127
- (Impact to Your Hardware Warranty): Updated/Changed the paragraph, including the "Consequently, TI will have no …" sentence.... 128
- (Combined MCU and Main Domains Power- Down Sequencing - Option 1): Added "Option 1".... 135
- (Combined MCU and Main Domains Power- Down Sequencing - Option 2): Added "Option 2" section (*new*).... 135
- (Isolated MCU and Main Domains Power- Down Sequencing - Option 1): Added "Option 1".... 141
- (Isolated MCU and Main Domains Power- Down Sequencing - Option 2): Added "Option 2" section (*new*). 141
- (System Timing): Deleted the "System Timing Conditions" table and moved to the lower sections: Reset, Safety Signal, and Clock timing.... 147
- (Reset Timing): Added Reset Timing Conditions table to define conditions specific to reset inputs and outputs.... 147
- (System Timing): Added a timing conditions table.... 155
- (System Timing): Added a timing conditions table.... 156
- (GPIO): Updated/Changed the GPIO Timings Conditions table and added an associated footnote.... 183
- (I2C): Added an IOSET note that explains timing limitations associated with valid pin combinations.... 209
- (MMC0 DLL Delay Mapping for all Timing Modes): Updated/Changed the **FRQSEL** ([10:8]) and **CLKBUFSEL** ([2:0]) values for Legacy SDR, High Speed SDR, and High Speed DDR *and* HS200 and HS400 modes in the MMCSD0_MMC_SSCFG_PHY_CTRL_5_REG; plus, added associated footnotes.... 222
- (HS200 Mode):Added MMC0 timing requirements parameter information.... 227
- (MMC1 DLL Delay Mapping for all Timing Modes): Updated/Changed the register names for "… CTRL_4_REG".... 229
- (MMC1 DLL Delay Mapping for all Timing Modes): Updated/Changed the OTAPDLYENA and OTAPDLYSEL values for both Default Speed and High Speed modes *and* changed the ITAPDLYSEL value for the UHS-I DDR50 mode.... 229
- (MMC1 DLL Delay Mapping for All Timing Modes): Deleted the CLKBUFSEL column because this "… CTRL_5_REG" register bit field doesn't provide any function.... 229
- (I2C): Added an IOSET note that explains timing limitations associated with valid pin combinations.... 254

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDA4APE4T5AANDRQ1	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-	TI TDA4APE 4T5A Q1
TDA4APE4T5AANDRQ1.B	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	See TDA4APE4T5AANDRQ1	TI TDA4APE 4T5A Q1
TDA4APE6T5AANDRQ1	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4APE 6T5A Q1
TDA4APE6T5AANDRQ1.B	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4APE 6T5A Q1
TDA4VPE4T5AANDRQ1	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4VPE 4T5A Q1
TDA4VPE4T5AANDRQ1.B	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4VPE 4T5A Q1
TDA4VPE6T5AANDRQ1	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4VPE 6T5A Q1
TDA4VPE6T5AANDRQ1.B	Active	Production	FCBGA (AND) | 1063	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TI TDA4VPE 6T5A Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

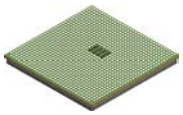
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

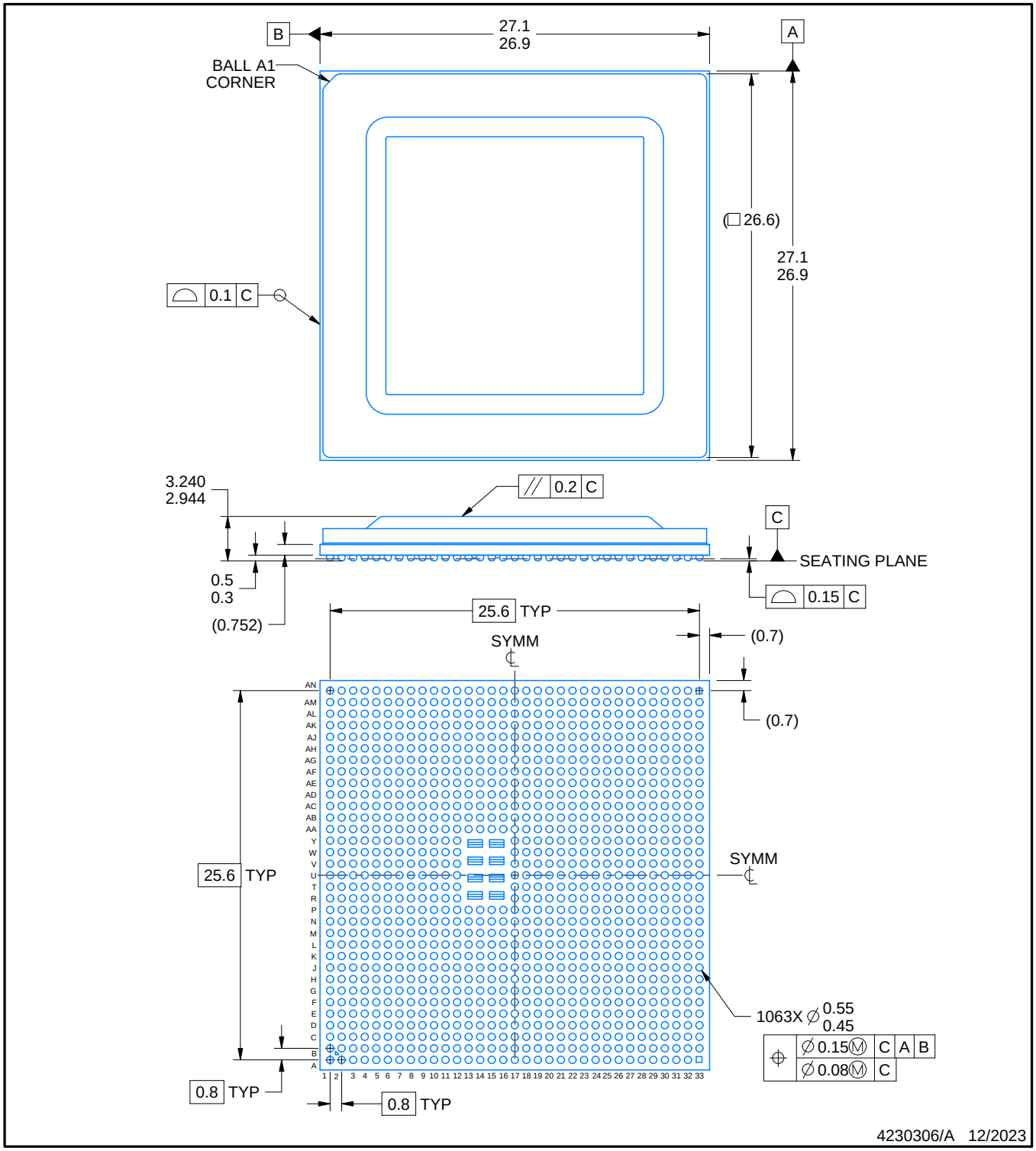
AND1063A



PACKAGE OUTLINE

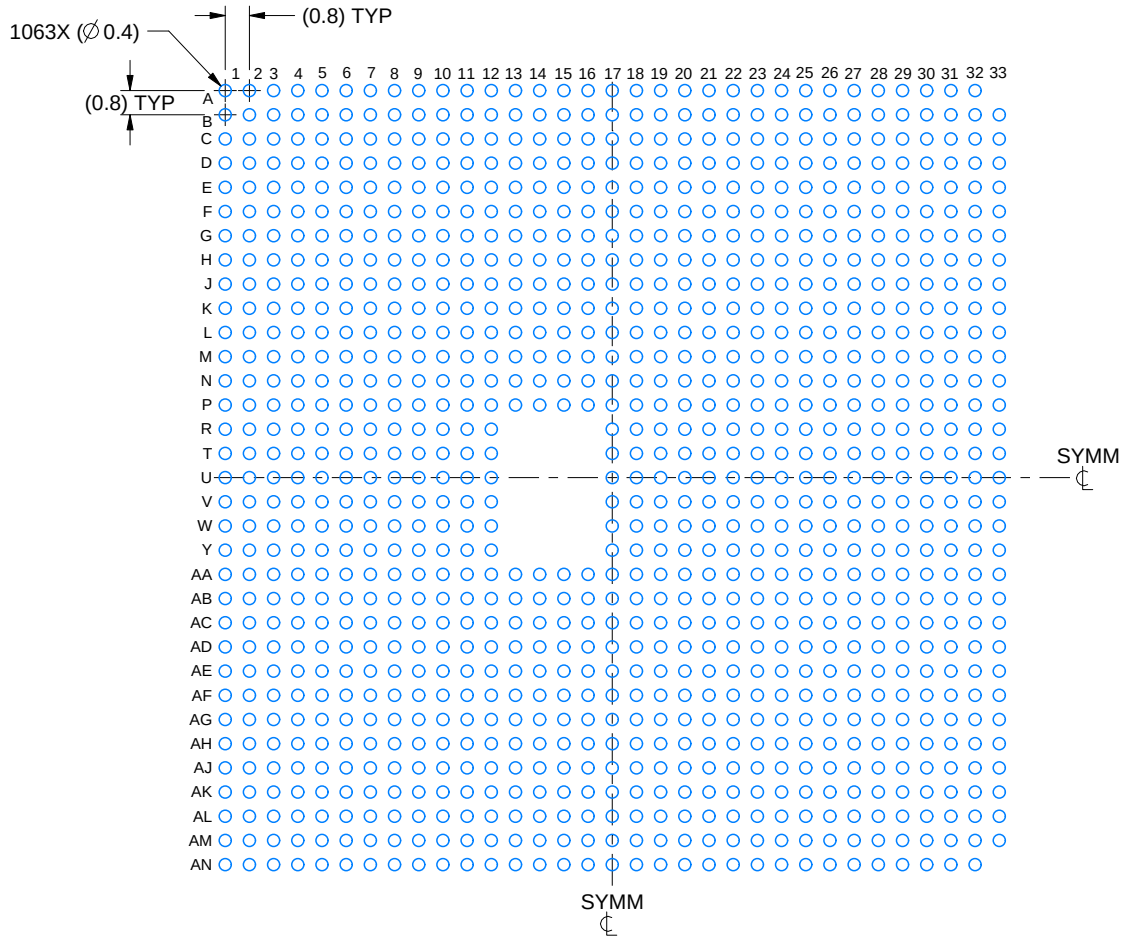
FCBGA - 3.24 mm max height

BALL GRID ARRAY

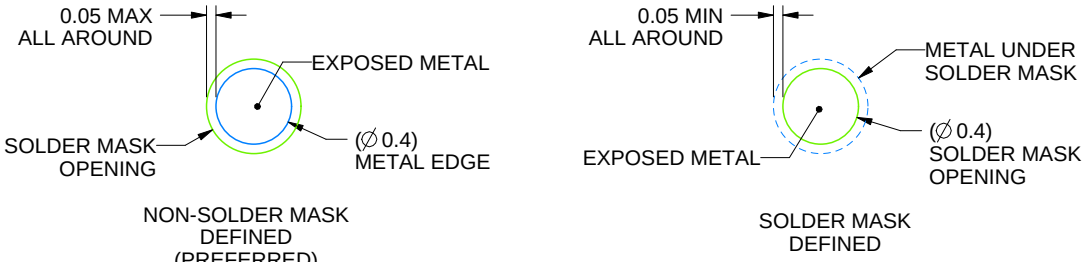


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 4X



SOLDER MASK DETAILS
NOT TO SCALE

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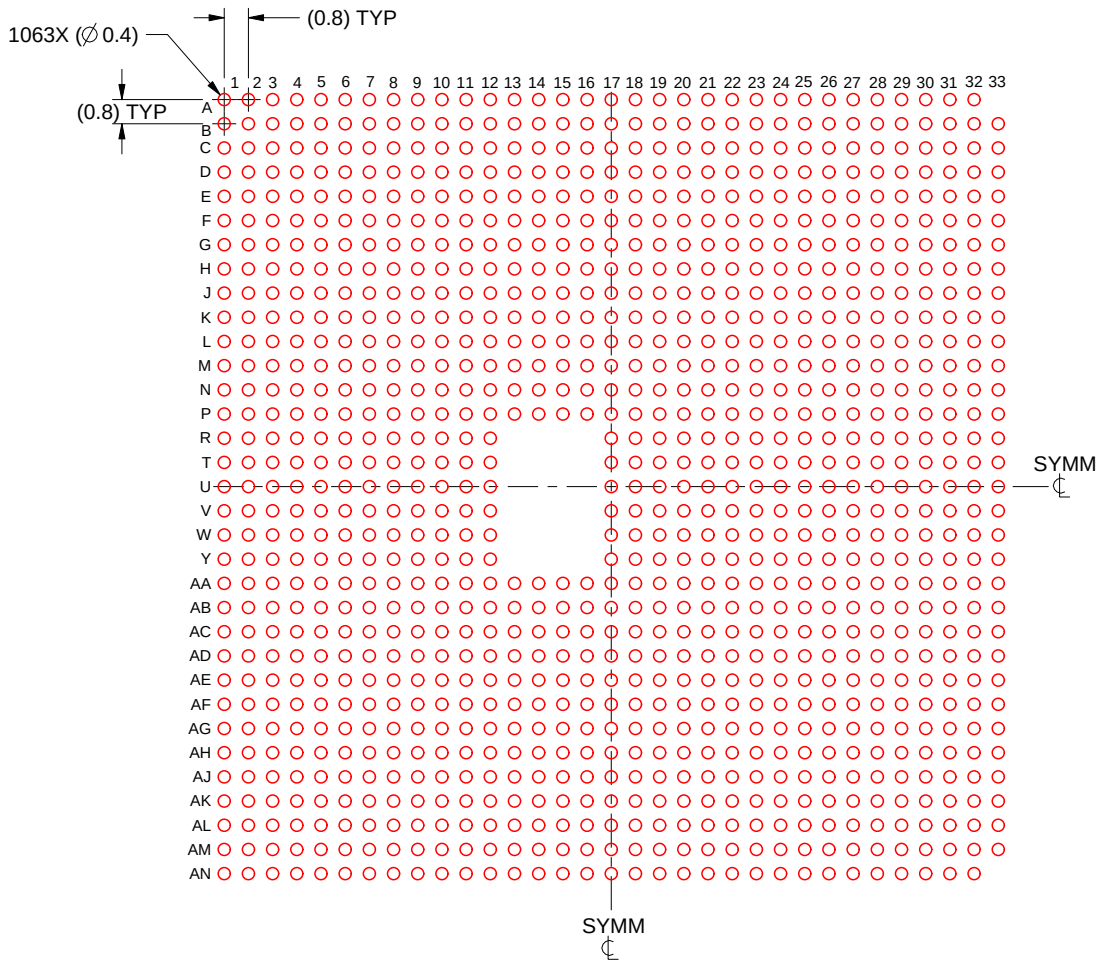
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 4X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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