AM62A Low-Power Starter Kit Evaluation Module

Description

The SK-AM62A-LP starter kit (SK) evaluation module (EVM) is built around our AM62A artificial intelligence (AI) vision processor, which includes an image signal processor (ISP) supporting up to 5MP at 60fps, a 2 tera-operations-per-second (TOPS) AI accelerator, a quad-core 64-bit Arm® Cortex®-A53 microprocessor, a single-core Arm Cortex-R5F and an H.264/H.265 video encode/decode. SK-AM62A-LP is an excellent choice when developing low-power smart camera, dashcam, machine-vision camera and automotive front-camera applications.

Get Started

1. Order the EVM at SK-AM62A-LP
2. Download the latest libraries.
3. Download the comprehensive reference design files at SK-AM62A-LP.
4. Read this technical user's guide.

Features

- Processing
  - AM62A74 with four Arm Cortex-A53
  - Cortex-R5F
  - Deep-learning accelerator
- Display
  - One High-Definition Multimedia Interface (HDMI™) connector over RGB888 with audio CODEC TLV320AIC3106
- M.2 key E interface support for Wi-Fi® and *Bluetooth*® modules, four-lane MIPI CSI-2 camera connector, up to two gigabit Ethernet
- Connectivity
  - One USB Type-A 2.0
  - One USB Type-C® dual-role device (DRD) 2.0 supports USB booting
  - Onboard XDS110 Joint Test Action Group (JTAG) emulator
  - Four Universal Asynchronous Receiver/ Transmitters (UARTs) using USB Type-B 2.0
- Storage
  - 4GB LPDDR4
- Bootable interfaces on SK [microSD, USB, QSPI, Ethernet, UART]
- Software
  - TI processor SDK Linux®
  - RT-Linux

Applications

- Machine vision camera
- Dashcam
- Automotive front camera system
- Smart camera

This design incorporates HDMI® technology.

1 Evaluation Module Overview

1.1 Introduction

This evaluation module user's guide is an excellent resource for engineers looking to develop applications with TI's AM62A Low-Power SK EVM. This low-cost Starter Kit is built around TI's AM62A AI Vision processor which includes an image signal processor (ISP) supporting 5MP at 60FPS, 2 tera-operations-per-second (TOPS) AI Accelerator, Quad-Core 64-bit Arm-Cortex A53 microprocessor, Single-Core Arm Cortex-R5F, and H.264/H.265 video encode/decode. The SK-AM62A-LP is an excellent choice when developing smart camera, dashcam, machine vision camera, and automotive front camera applications.

The starter kit also includes both a MIPI CSI-2 camera connector for one camera and additional expansion connector for up to four cameras, making this kit a good choice for a variety of embedded vision and AI applications on the edge. For a variety of applications, TI's ISP can handle different lighting conditions in video streams by using HDR encoding and RBG-IR camera support. With the help of edge AI, Deep Learning on video streams like image classification and object detection have greatly improved performance on AM62A's AI accelerator. Therefore, giving significant improvement in frame rate, latency, and performance to allow offloading intensive processes from general-purpose cores.

Furthermore, the starter kit supports Linux development with feature rich EdgeAI SDK. On-chip emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ from TI.

Note

This evaluation board is a pre-production release and has a few known issues that must not be copied into a production system.

SK-AM62A-LP also includes both a mobile industry processor interface MIPI® CSI-2 camera connector for one camera and an additional expansion connector for up to four cameras, making the SK-AM62A-LP good for a variety of embedded vision and AI applications on the edge. For a variety of applications, the ISP can handle different lighting conditions in video streams by using high dynamic range (HDR) encoding and RGB-IR camera support. With edge AI, deep learning on video streams like image classification and object detection have greatly improved performance on the AM62A AI accelerator, therefore giving significant improvement in frame rate, latency and performance to allow offloading intensive processes from general-purpose cores.

Furthermore, the SK-AM62A-LP supports Linux® development with a feature-rich edge AI software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio™ integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation.

During custom board design, customers tend to reuse the SK design files and make edits to the design file. Alternatively customers reuse some of the common implementations including the SOC, memory and communication interfaces. Because the SK is expected to have additional functionalities, customers optimize the SK implementation to suit the board design requirements. While optimizing the SK schematics, errors get introduced into the custom design that can cause functional, performance or reliability issues. When optimizing customers have queries regarding the SK implementation resulting in design errors. Many of the optimization and design errors are common across designs. Based on the learnings and datasheet pin connectivity recommendations, comprehensive Design Notes (D-Note:), Review Notes (R-Note:) and Cad Notes (Cad Note:) have been added near each section of the SK schematic that customers can review and follow to minimize errors. Additional files as part of the design downloads have been included to support customer evaluation.

1.2 Kit Contents

Included:

- EVM
- Quick Start Guide

Note

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- USB-C 5V to 15V and 3A power supply and cable
- MicroSD card
- USB micro-B cable for UART serial communication

1.3 Specification

1.3.1 Key Features

The AM62A Low Power SK EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for Texas Instrument's AM62A System-on-Chip (SoC).

The following sections discuss the key features of the SK EVM.

1.3.1.1 Processor

AM62A SOC,18mm × 18mm, 0.8mm pitch, 484-pin FCBGA and FCCSP.

1.3.1.2 Memory

- 4GB LPDDR4 supporting data rate up to 3733Mb/s
- Micro SD Card slot with UHS-1 support
- 1Gbit Octal SPI Flash memory
- 512Kbit board ID EEPROM
- 16GB eMMC Flash

1.3.1.3 JTAG Emulator

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator

1.3.1.4 Supported Interfaces and Peripherals

- 1x USB2.0 Type C Interface, support DFP and UFP modes(Data) and DRP mode(Power)
- 1x USB2.0 Host Interfaces, Type A
- 1x HDMI Interface
- Audio Line In and MIC + Headphone out
- M.2 Key E interface support for both Wi-Fi and Bluetooth modules
- 2x Gigabit Ethernet port supporting 10/100/1000Mbps data rate on RJ45 connector
- Quad port UART to USB circuit over microB USB connector
- User Test LEDs
- INA devices for current monitoring
- 2x Temperature Sensors near SoC and LPDDR4 for thermal monitoring

1.3.1.5 Expansion Connectors Headers to Support Application Specific Add On Boards

- CSI 22 Pin Camera flex connector
- CSI MIPI connector
- User Expansion connector
- MCU Header

1.4 Device Information

The Design built around AM62A processor, which integrates ARM cortex cores and support high-performance computing with low power consumption Power management is handled throughTPS65988 USB PD controller and PMIC, DC/DC convertor to provide stable power rails for the SoC and peripherals. The system features a wide range of connectivity including Gigabit Ethernet, USB 2.0 and SD/eMMC interface. Multimedia support is enabled using an HDMI transmitter, audio codec with headphone/microphone interface. and expansion for CSI camera input. Additional peripherals include UART I2C SPI and GPIO's making the platform flexible for industrial automotive and consumer application. The board also integrates debugging and expansion connector and system integration

2 Hardware

2.1 EVM Revisions and Assembly Variants

The various AM62A SK EVM PCB design revisions, and assembly variants are listed in Table 2-1. Specific PCB revision is indicated in silkscreen on the PCB. Specific assembly variant is indicated with additional sticker label.

Table 2-1. SK EVM PCB Design Revisions, and Assembly Variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
SK-AM62A-LP	PROC135E1	N/A (single variant produced)	First prototype, early release revision of the AM62A SK EVM. Implements the Sitara™ AM62A MPU with a PMIC power device
SK-AM62A-LP	PROC135E2	N/A	Second prototype, early release revision of the AM62A SK EVM. Implements many changes and bug fixes.
SK-AM62A-LP	PROC135E3	N/A	Third prototype. Added 2nd onboard Ethernet port and support for dual core voltage (0.85V and 0.75V)
SK-AM62A-LP	PROC135A	N/A	Production version.
SK-AM62A-LP	PROC135A1	N/A	Production version with updated SoC part number (AM62A74AVMSIANFRQ1). Functionally equivalent to PROC135A (AM62A74AUMSIAMBRQ1) with only package change. No PCB Design modification
SK-AM62A-LP	PROC135B	N/A	Revision B derived from PROC135A1 design; adjusted Resistor and capacitor tolerances, modified pull-up values for OSPI/MMC, added decoupling for VBUS, added series resistors for all GPIO Reset signals and an updated VMON_VSYS monitoring voltage.

2.2 System Description

2.2.1 Board Image With Markings

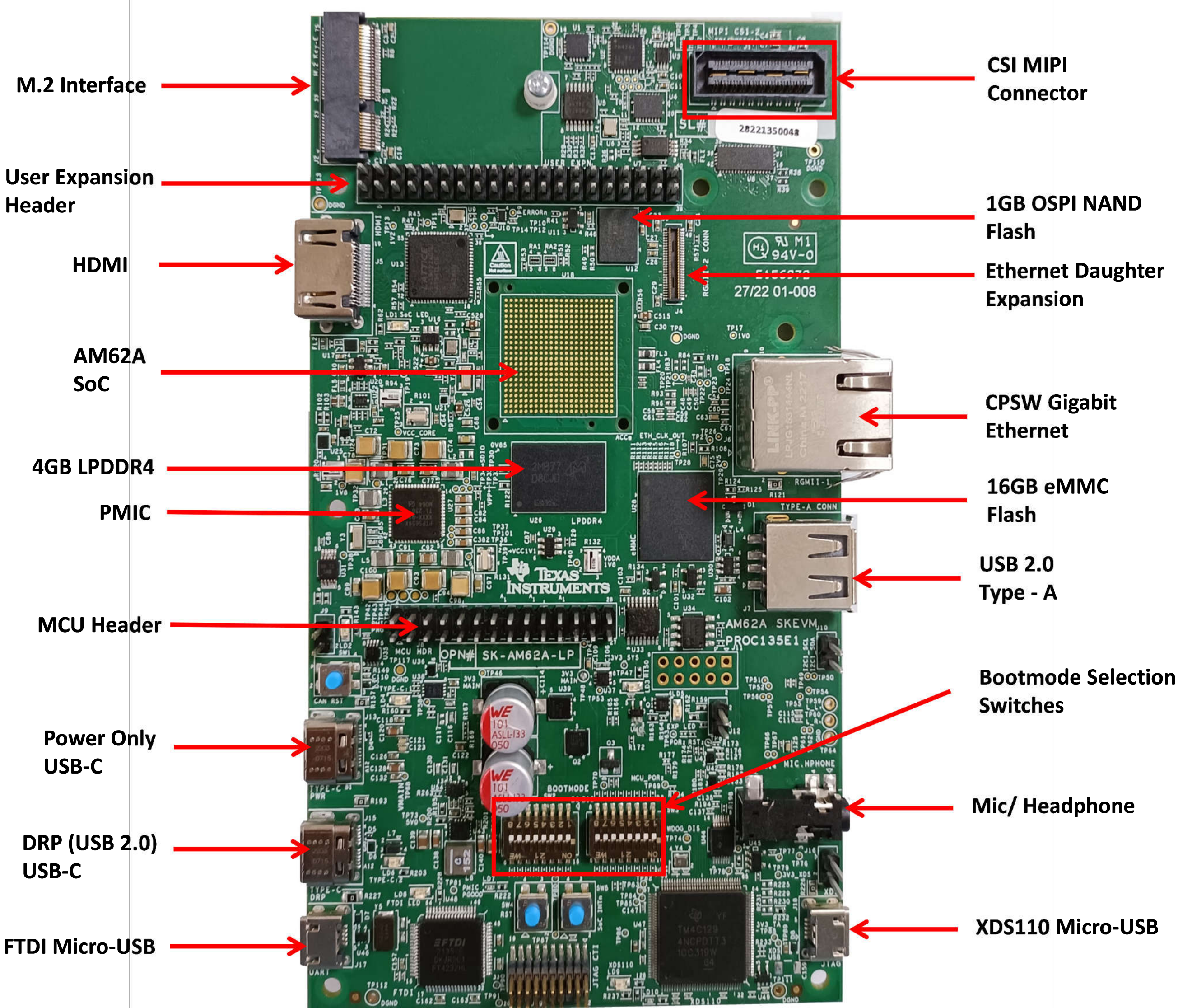

Figure 2-1. Top Side - Rev E1 and E2

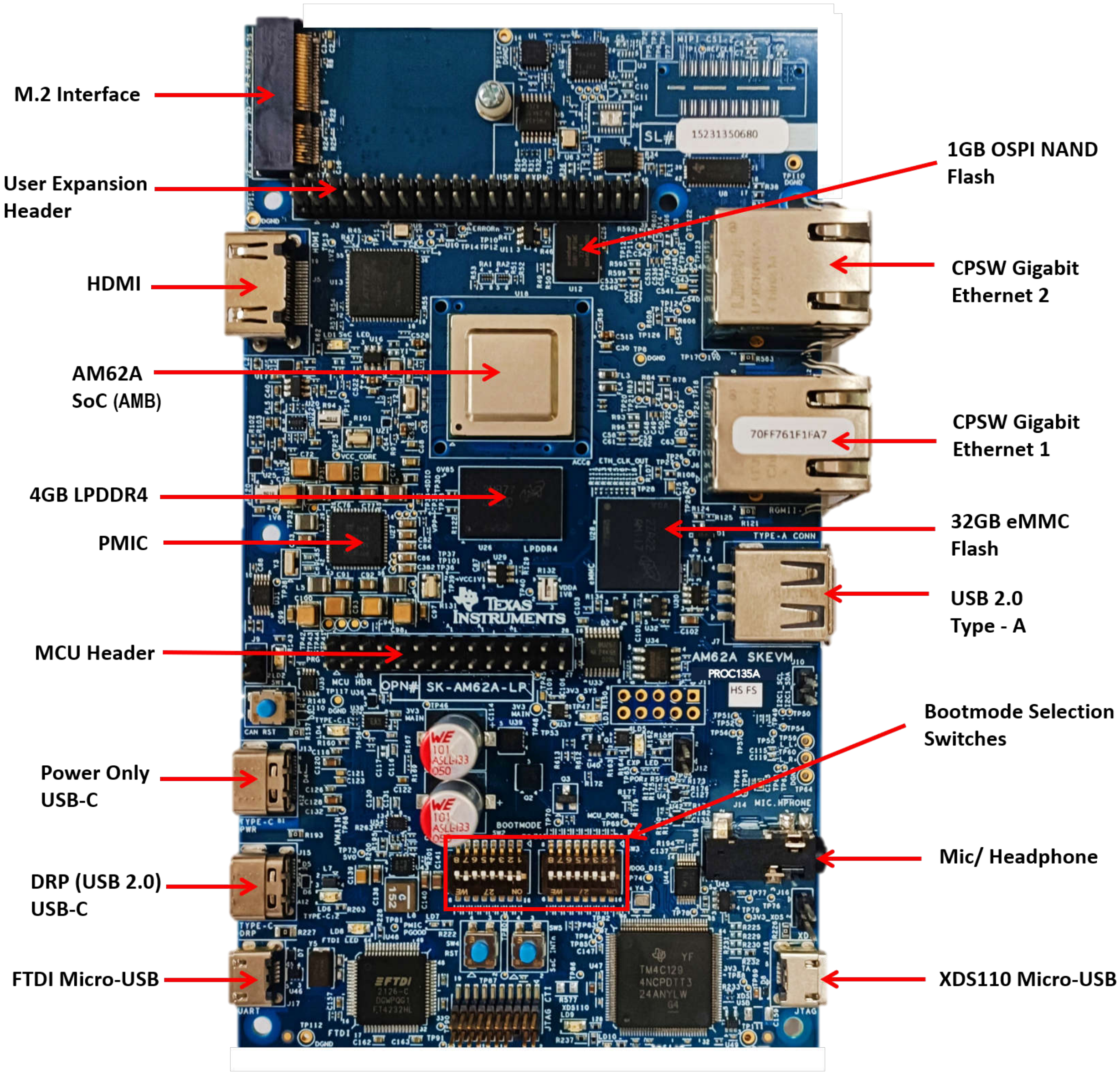

Figure 2-2. Top Side - Rev E3 and A

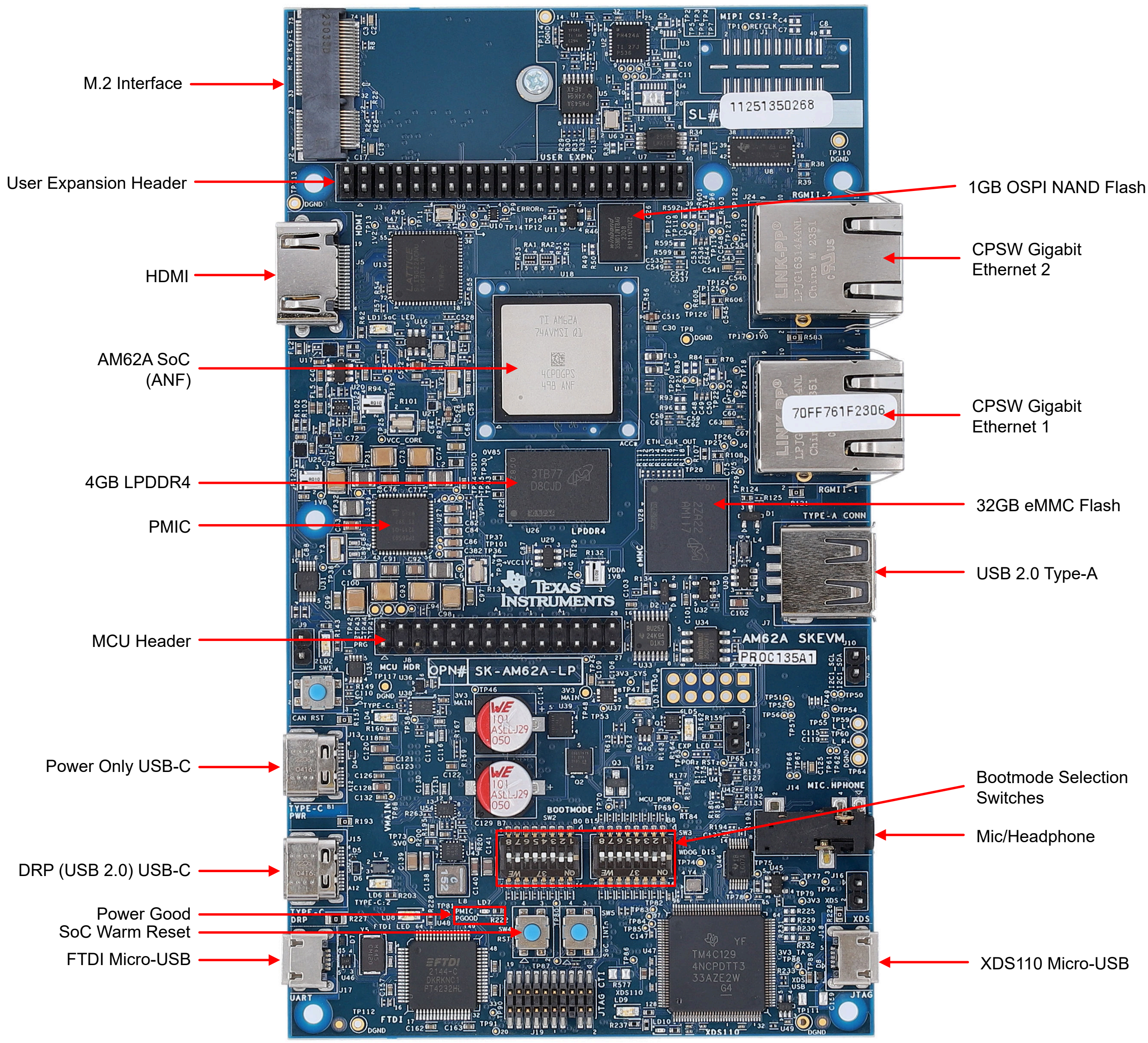

Figure 2-3. Top Side - Rev A1

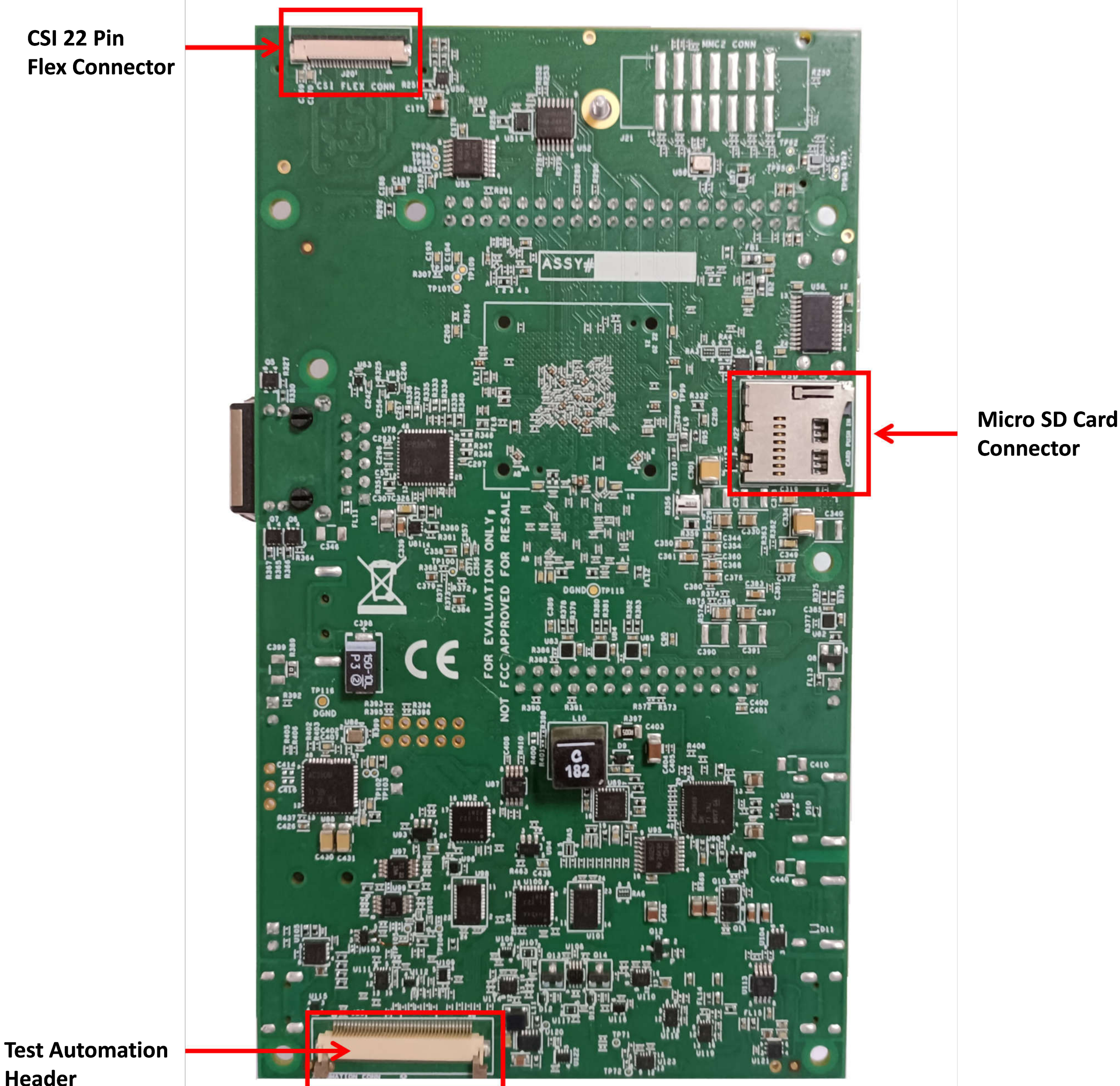

Figure 2-4. Bottom Side - Rev E1 and E2

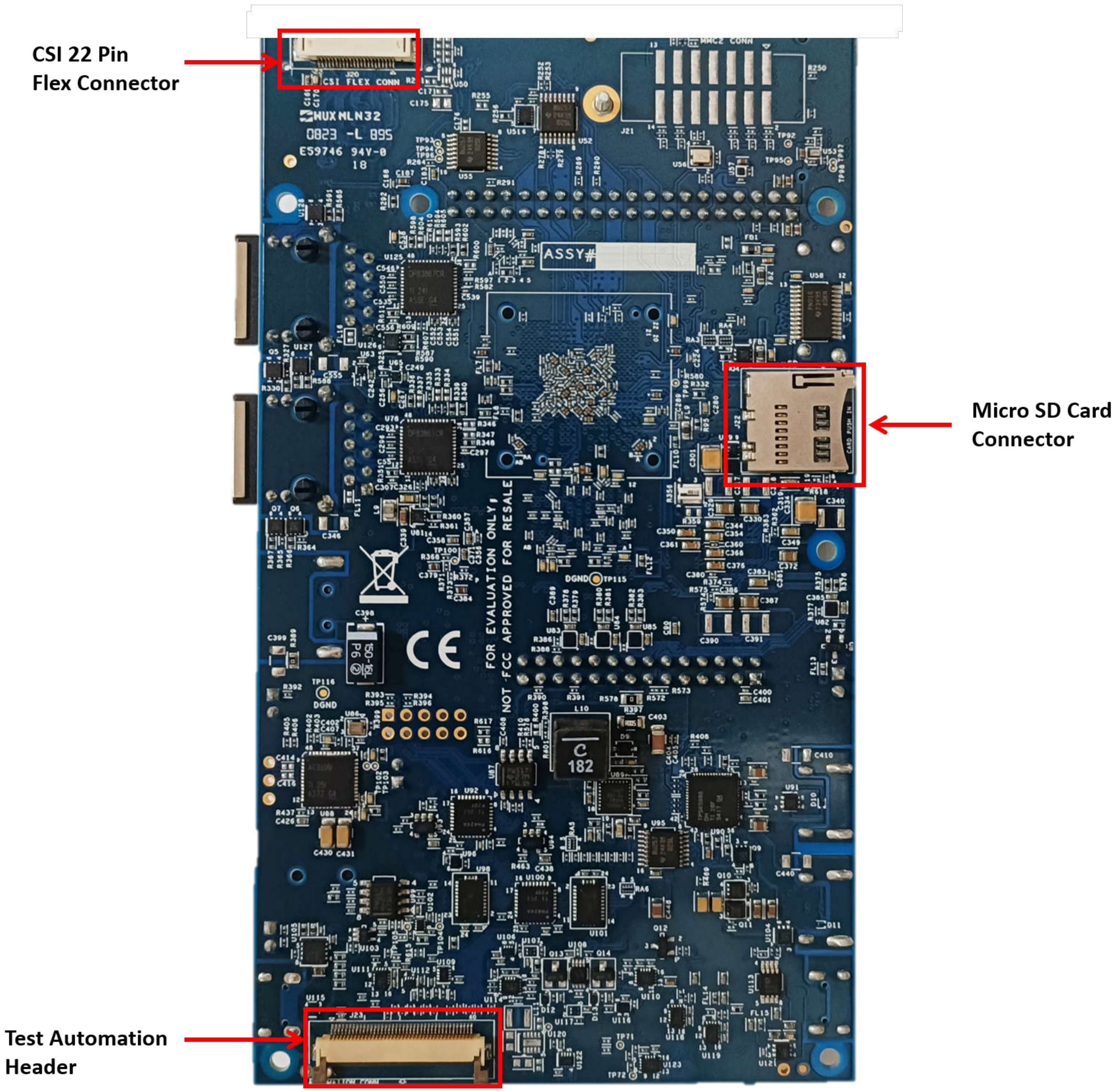

Figure 2-5. Bottom Side - Rev E3 and A

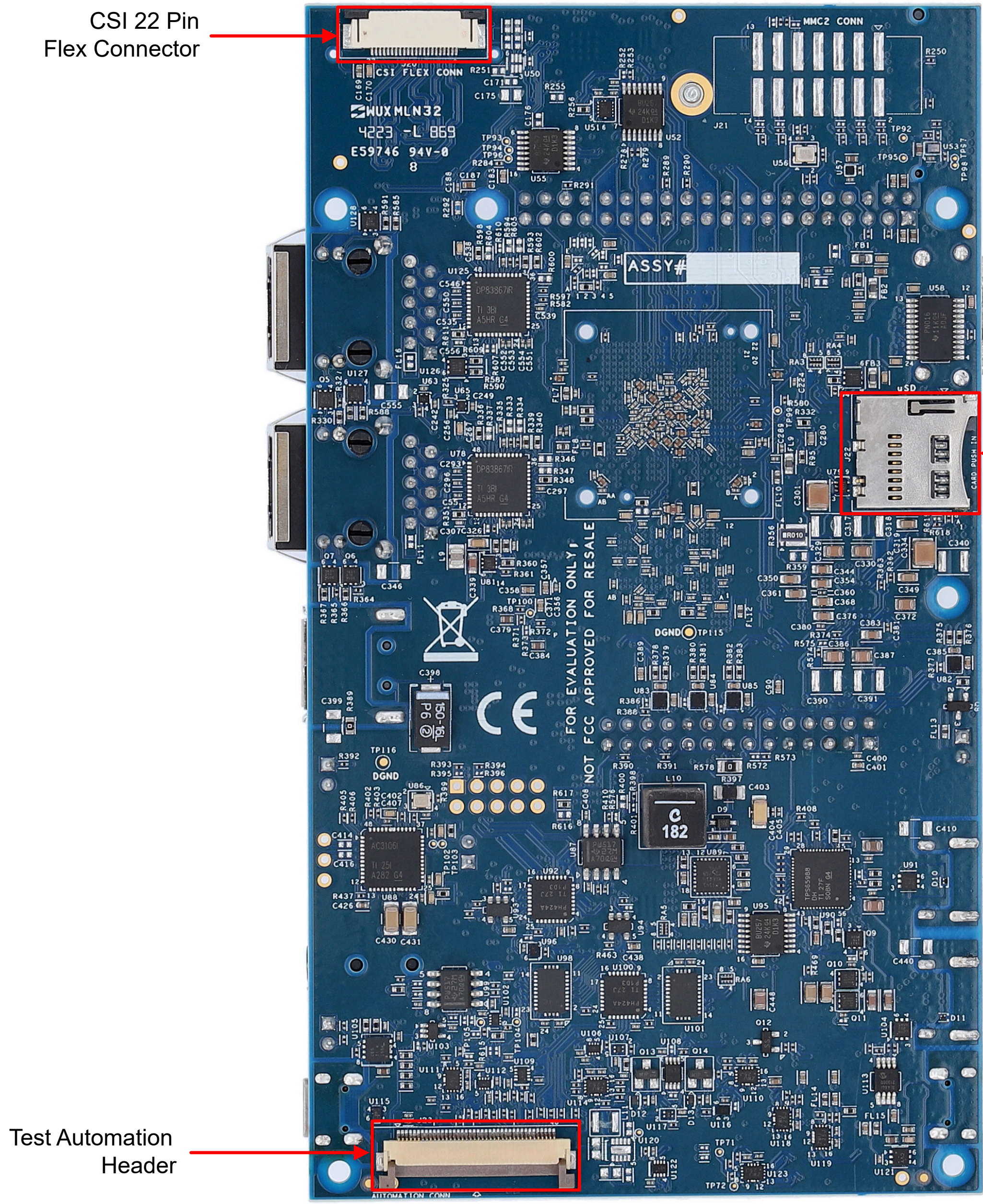

Figure 2-6. Bottom Side - Rev A1

2.2.2 Functional Block Diagram

The functional block diagram of the AM62A Low Power SKEVM Board is shown in Figure 2-7 and Figure 2-8.

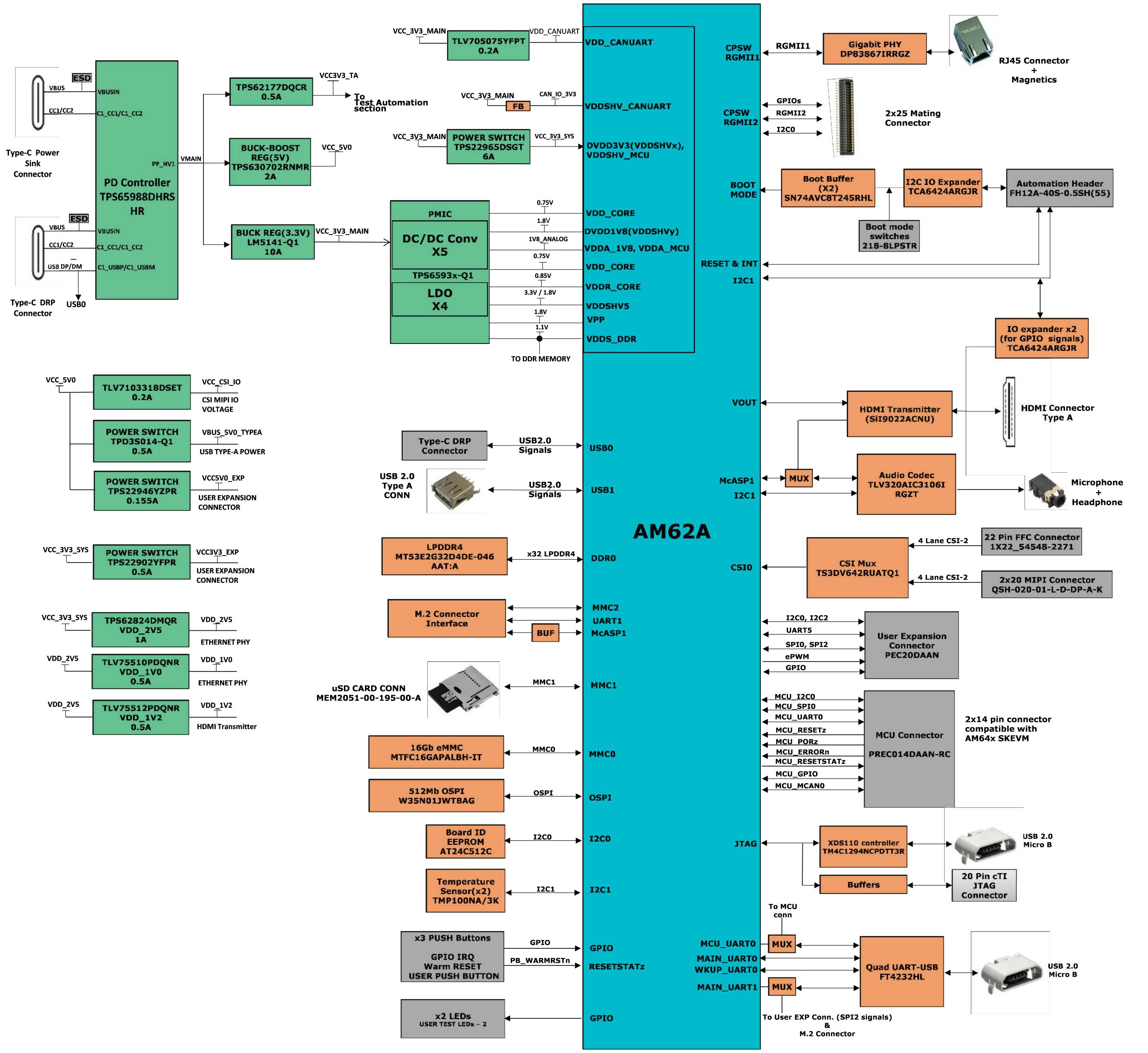

Figure 2-7. Block Diagram - Rev E1 and E2

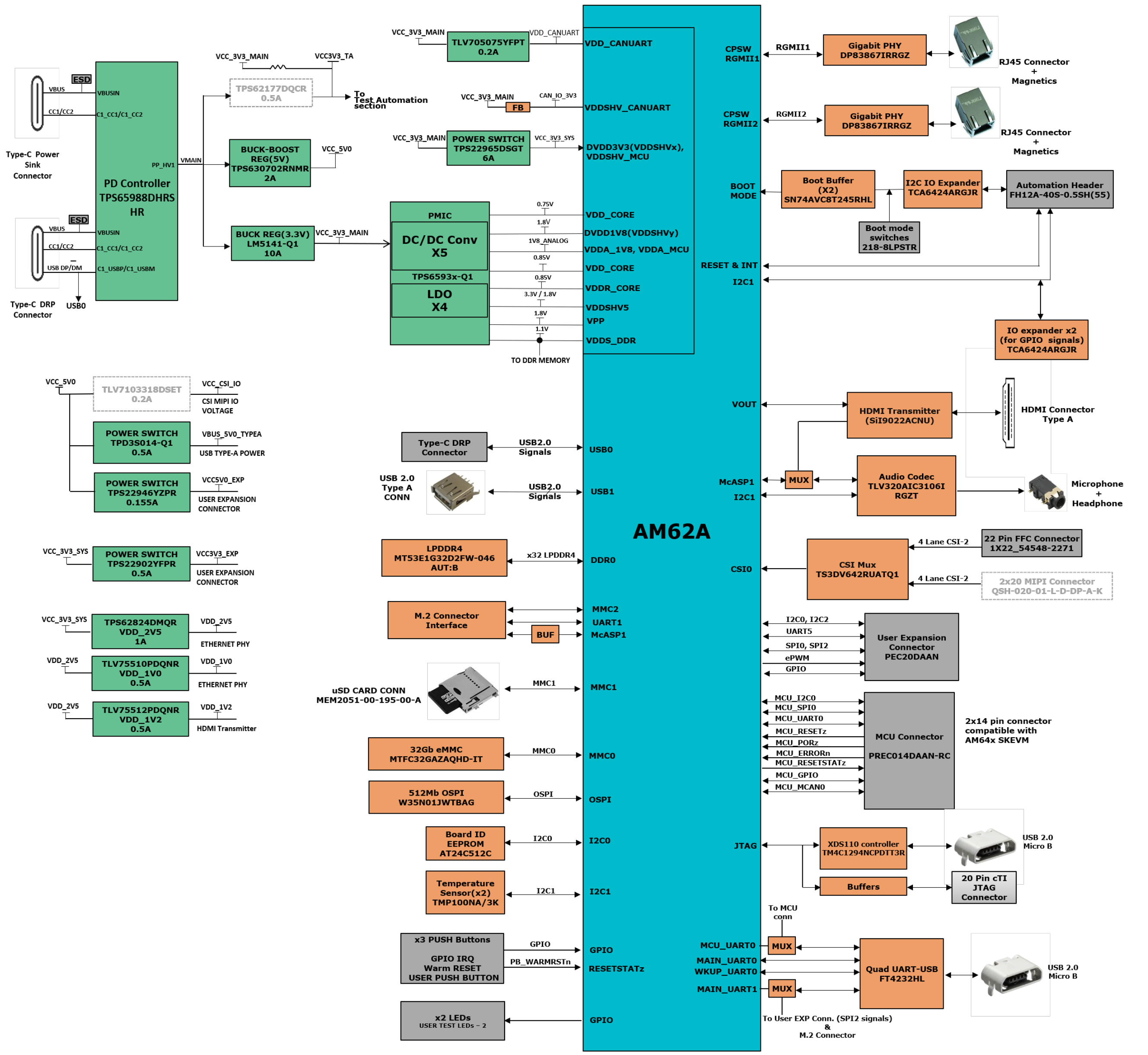

Figure 2-8. Block Diagram - Rev E3 and A

2.2.3 Power Requirements

AM62A Low Power SK EVM can be powered through either of the two USB Type C Connectors –

- Connector1(J13) - Power role – SINK, No Data role
- Connector2(J15) - Power role – DRP, Data role – USB 2.0 DFP or UFP

The AM62A SK EVM supports voltage input ranges of 5V - 15V and 3A of current. A USB PD controller (manufacturer part number: TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, so the connector can act as DFP only when Connector 1 powers the board. When both the connectors are connected to external power supply, the port with highest PD power contract is selected to power the board.

Table 2-2. Type-C Power Roles

J13 (UFP)	J15 (DRP)	BoardPower	Remarks
Plugged in	NC	ON - J13	J13 is UFP and can only sink power and J15 can act as DFP if a peripheral is connected
NC	Plugged in	ON - J15	J15 is UFP and can only sink power
Plugged in	Plugged in	ON- J13 or J15	Board is powered by the port with highest PD power contract

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so the PD IC can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J11. Once the EEPROM is programmed, the PD obtains the configuration files using SPI communication. Upon loading the configuration files the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is pre-programmed with the configuration file for the operation of the PD controller.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SKEVM Board. Anexternal power supply (Type-C output) can be used to power the EVM but is not included as part of the SKEVM kit.

The external power supply requirements (Type-C) are:

Minimum Voltage: 5VDC, Recommended Minimum Current: 3000mA

Maximum Voltage: 15VDC, Maximum current: 5000mA

Table 2-3. Recommended Power Supplies

Manufacturer	Manufacturer Part Number
GlobTek, Inc.	TR9CZ3000USBCG2R6BF2
Qualtek	QADC-65-20-08CB

Note

Because SK-AM62A implements USB PD for power, the device can negotiate to the highest voltage and current combination supported by the device and power adapter. Exceeding the maximum voltage and current requirements listed above is acceptable as long as the power adapter is compliant with the USB-C® PD specification.

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

CAUTION

It has been observed that the Raspberry Pi USB Type-C® AC Adapter (Model: KSA-15E-051300HU, Output: 5.1V DC 3.0A) does not power the SK-AM62A-LP EVM correctly. This adapter uses a passive USB Type-C® cable, which does not implement USB Power Delivery (USB-PD) negotiation. As a result, the EVM can fail to boot or behave unexpectedly when powered from this adapter.

Power supply designs that are compatible with the SK-AM62A-LP EVM:

- Power delivery enabled power adapter with USB-C® receptacle
- Power delivery enabled power adapter with captive USB-C® cable
- PC USB Type-C® port that has power delivery classification

  - Thunderbolt
  - Battery behind USB logo

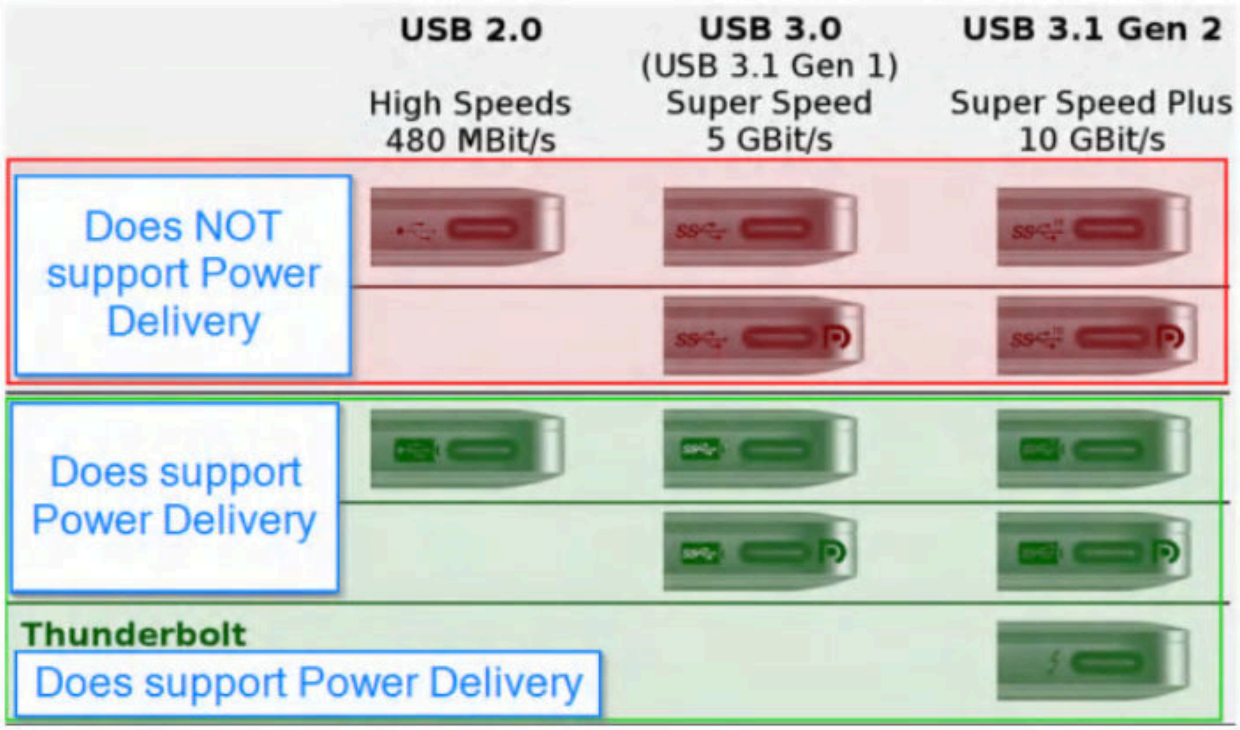

Figure 2-9. USB Type-C® Port Capabilities

Power supply designs that are NOT compatible with the SK-AM62A-LP EVM:

- Any USB adapter cables such as:
  - Type-A to Type-C
  - micro-B to Type-C
  - DC barrel jack to Type-C
- 5V, 1.5A power adapter with USB-C® captive cable or receptacle
- PC USB Type-C® port not capable of 3A

2.2.4 Power ON/OFF Procedures

Power to the EVM is provided through an external power supply with PD capability to either of the two USB Type-C Ports.

2.2.4.1 Power-On Procedure

1. Place the SKEVM boot switch selectors (SW2, SW3) into selected boot mode. Example boot-mode for SD card is shown in Figure 2-10.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the SKEVM Type-C (J13 or J15) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a Laptop computer).
5. Visually inspect that either LD4 or LD6 LED is illuminated.
6. XDS110 JTAG and UART debug console outputs are routed to micro-USB ports J18 and J17, respectively.

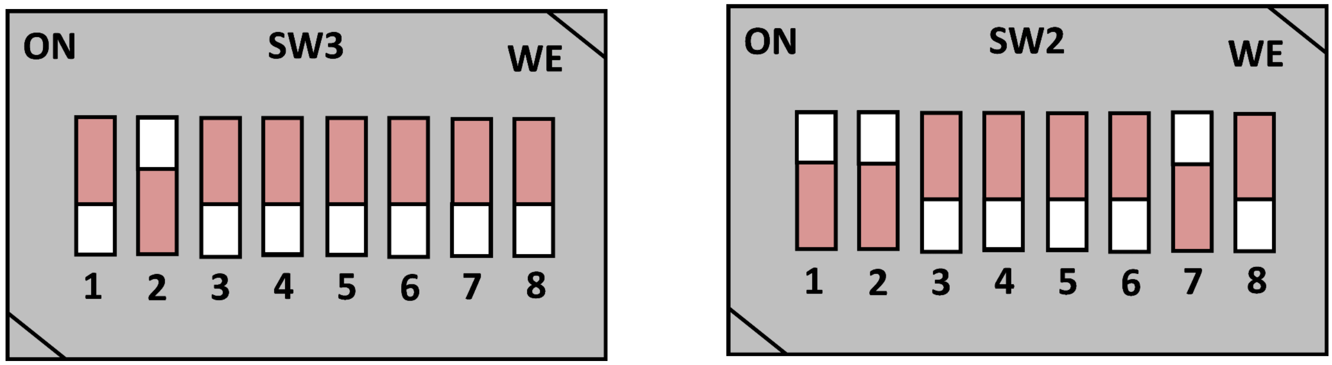

Figure 2-10. Example Boot Mode (SD Boot)

2.2.4.2 Power-Off Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the SKEVM.

2.2.4.3 Power Indication LED

The power indication LED's are mentioned in Table 2-4.

Table 2-4. Power Indication LED

SL Number	Power Indication	LED	Color
1	POWER INDICATION LED: VBUS_TYPEC1	LD4	GREEN
2	POWER INDICATION LED: VBUS_TYPEC2	LD6	GREEN
3	PMIC POWER GOOD INDICATION LED	LD7	GREEN
4	POWER INDICATION LED: VCC_3V3_SYS	LD3	GREEN
5	FT4232 USB TO UART BRIDGE POWER ENABLE	LD8	GREEN

2.2.4.4 Power Test Points

Test points for each power output on the board are mentioned in Table 2-5.

Table 2-5. Power Test Points

Sl Number	Power Supply	Test Point	Voltage
1	VDD_1V2	TP13	1.2
2	VDDSHV_SDIO	TP34	3.3/ 1.8
3	VPP_1V8	TP35	1.8
4	VDDA1V8	TP40	1.8
5	VCC_0V85	TP30	0.85
6	VCC1V8_SYS	TP32	1.8
7	VCC_CORE	TP25	0.75
8	VCC1V1	TP39	1.1
9	VMAIN	TP68	12
10	VCC_5V0	TP73	5
11	VCC3V3_TA	TP88	3.3
12	VCC3V3_XDS	TP79	3.3
13	VCC_3V3_SYS	TP47	3.3
14	VCC_3V3_MAIN	TP46	3.3
15	VDD_2V5	TP29	2.5
16	VDD_1V0	TP17	1
17	VINT_PMIC_1V8	TP101	1.8
18	VRTC_PMIC_1V8	TP37	1.8
19	VDD_CANUART	C507.1	0.75
20	VDD_MMC1	FL5.1	3.3
21	XDS_USB_VBUS	TP89	5
22	VCC3V3_EXP	J3.1	3.3
23	VCC5V0_EXP	J3.2	5
24	VBUS_5V0_TYPEA	U30.4	5
25	VCC_CSI_IO	C8.1	1.8/ 3.3
26	VBUS_TYPEC1	C118.1	12
27	VBUS_TYPEC2	R203.1	12
28	VCC_3V3_FT4232	C152.2	3.3
29	LDO_3V3	U34.8	3.3
30	LDO_1V8	C122.1	1.8
31	FT4232_USB_VBUS	J17.1	5
32	VCC_5V0_HDMICONN	J5.18	5
33	VCC_1V8_FT4232	C157.2	1.8

2.2.5 AM62A Low Power SK EVM Interface Mapping

Table 2-6. Interface Mapping

Interface Name	Port on SoC	DevicePart Number
Memory – LPDDR4	DDR0	MT53E2G32D4DE-046 AAT:A
Memory –OSPI	OSPI0	W35N01JWTBAG
Memory –Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory –eMMC	MMC0	MTFC16GAPALBH-IT
Memory –Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1– RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2– RGMII	SoC_RGMII2	DP83867IRRGZ

Table 2-6. Interface Mapping (continued)

Interface Name	Port on SoC	DevicePart Number
GPIO Port Expander1	SoC_I2C1	TCA6424ARGJR
User Expansion Connector – 2x20 HDR	SPI0,SPI2, UART5, SoC_I2C0, SoC_I2C2, McASP1 and GPIOs	PEC20DAAN
MCU Header – 2x14 HDR	MCU MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
USB– 2.0 Type C	USB0	2012670005
USB– 2.0 Type A	USB1	629104151021
CSI Interface	CSI0	54548-2271
		QSH-020-01-L-D-DP-A-K
HDMI	VOUT0, McASP1and SoC_I2C1	SiI9022ACNU+ TPD12S016PWR + 10029449-001RLF
Audio Codec	McASP1and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO Port Expander2	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UAR SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test Automation Header	SoC_I2C1	FH12A-40S-0.5SH
Temperature Sensors	SoC_I2C1	TMP100NA/3K
Current Monitors	SoC_I2C1	INA231AIYFDR
Connectivity– M.2 Key E	MMC2,McASP1 and SoC_UART1	2199119-4

2.2.6 Peripheral and Major Component Description

The following sections provide an overview of the different interfaces and circuits on the AM62A Low Power SK EVM.

2.2.6.1 Clocking

Figure 2-11 shows the clock architecture of the AM62A-Low Power SK EVM.

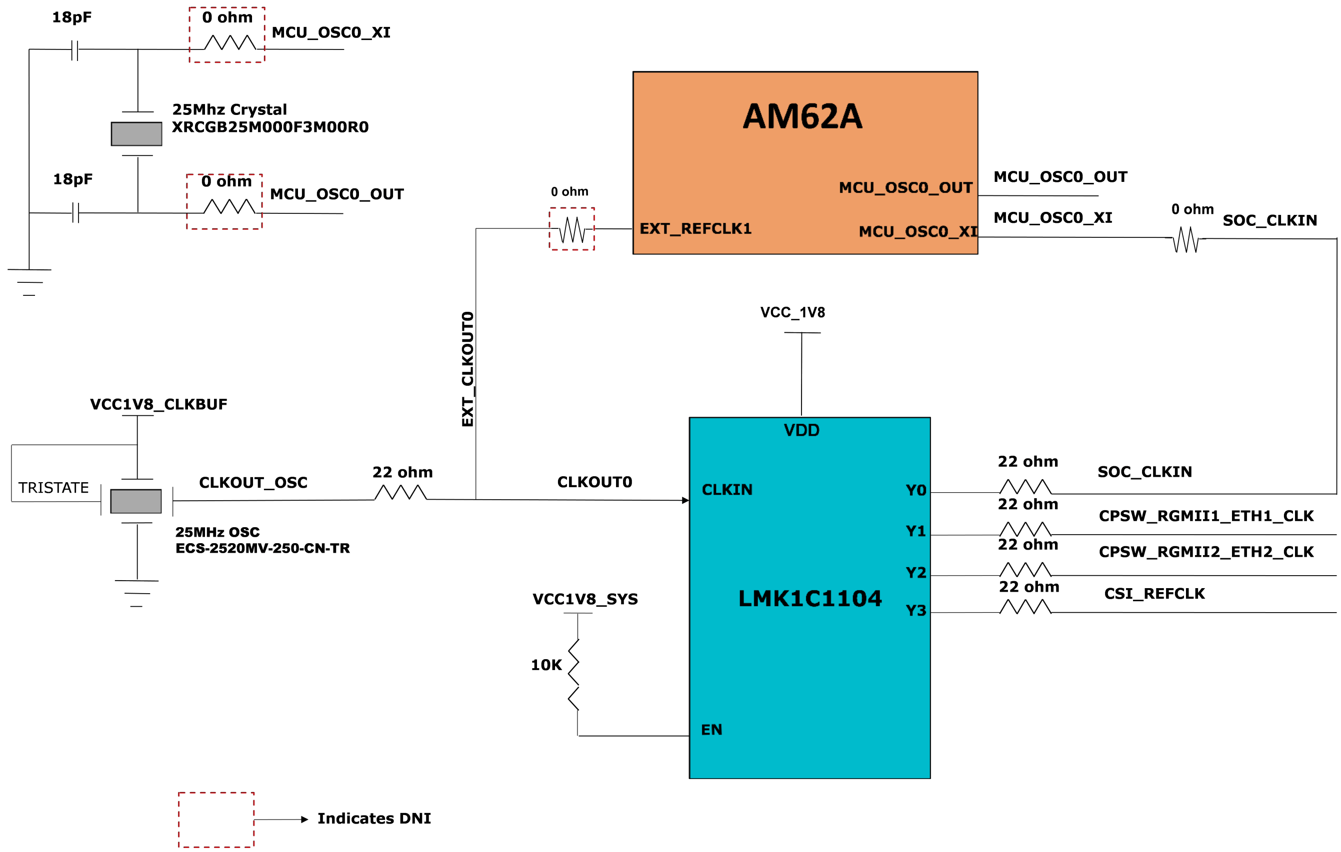

Figure 2-11. Clock Architecture

A clock generator of part number LMK1C1104PWR is used to drive the 25MHz clock to the SOC, two Ethernet PHYs and CSI Camera devices. LMK1C1104PWR is a 1:4 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides four 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SOC or a 25MHz oscillator, the selection of which is made using a set of resistors. By default, an oscillator is used as an input to the clock buffer on the AM62A-Low Power SK EVM. Output Y1 and Y2 of the clock buffer are used as reference clock inputs for the two Gigabit Ethernet PHYs. Output Y3 of the clock buffer is used as a reference clock input for CSI Camera interface.

There is one external crystal (32.768KHz) attached to the AM62A SOC to provide clock to the WKUP domain.

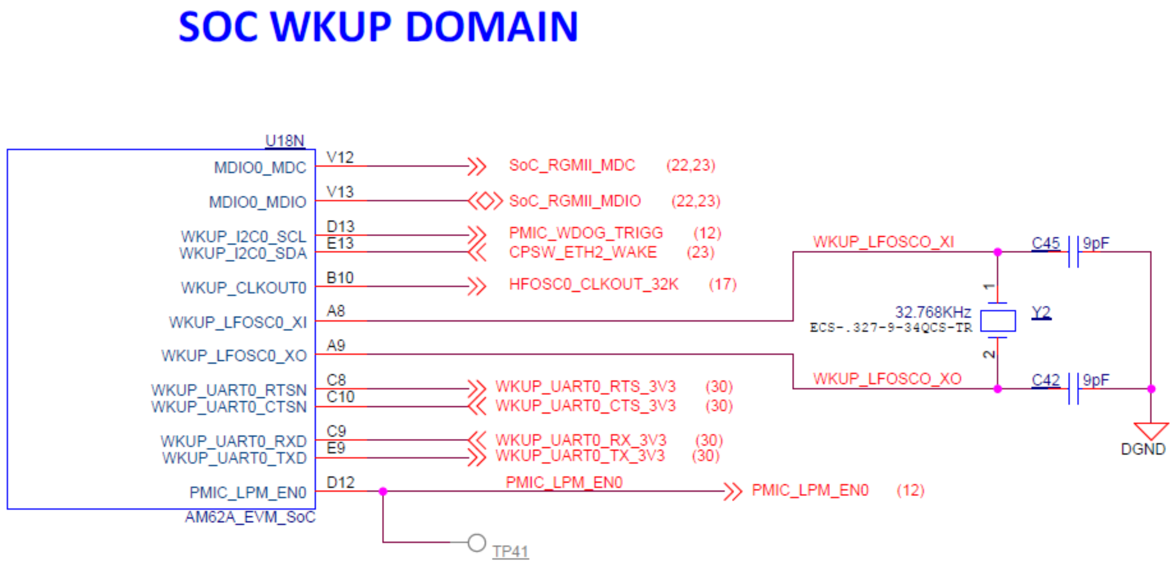

Figure 2-12. SoC WKUP Domain Clock

2.2.6.1.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, M.2 Interface, HDMI Transmitter and Audio Codec are generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in Table 2-7.

Table 2-7. Clock Table

Peripheral	Part Number	Description	Frequency
XDS110 emulator (Y4)	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge (Y5)	445I23D12M00000	CRY12.000MHz 18pF SMD	12.000MHz
M.2 Interface (U56)	ECS-327MVATX-2-CN-TR	OSC 32.768KHz CMOS SMD	32.768KHz
Audio Codec (U86)	MC2016Z12.2880C19XSH	OSC12.288MHz CMOS SMD	12.288MHz
HDMI Transmitter (U9)	MC2016Z12.2880C19XSH	OSC12.288MHz CMOS SMD	12.288MHz

The clock required by the HDMI transmitter can be provided by either the on board oscillator or the SOC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. SOC's EXT_REFCLK1 is used to provide clock to the User Expansion Connector on the SKEVM. The 32.768KHz clock to the M.2 module is provided by default from WKUP_CLKOUT0 ball of AM62A SOC.

2.2.6.2 Reset

Figure 2-13 shows the Reset Architecture of AM62A Low Power SK EVM. The SOC has the following resets:

- RESETSTATz is the Main domain warm reset status output
- PORz_OUT is the Main domain power ON reset status output
- RESET_REQz is the Main domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon Power on Reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

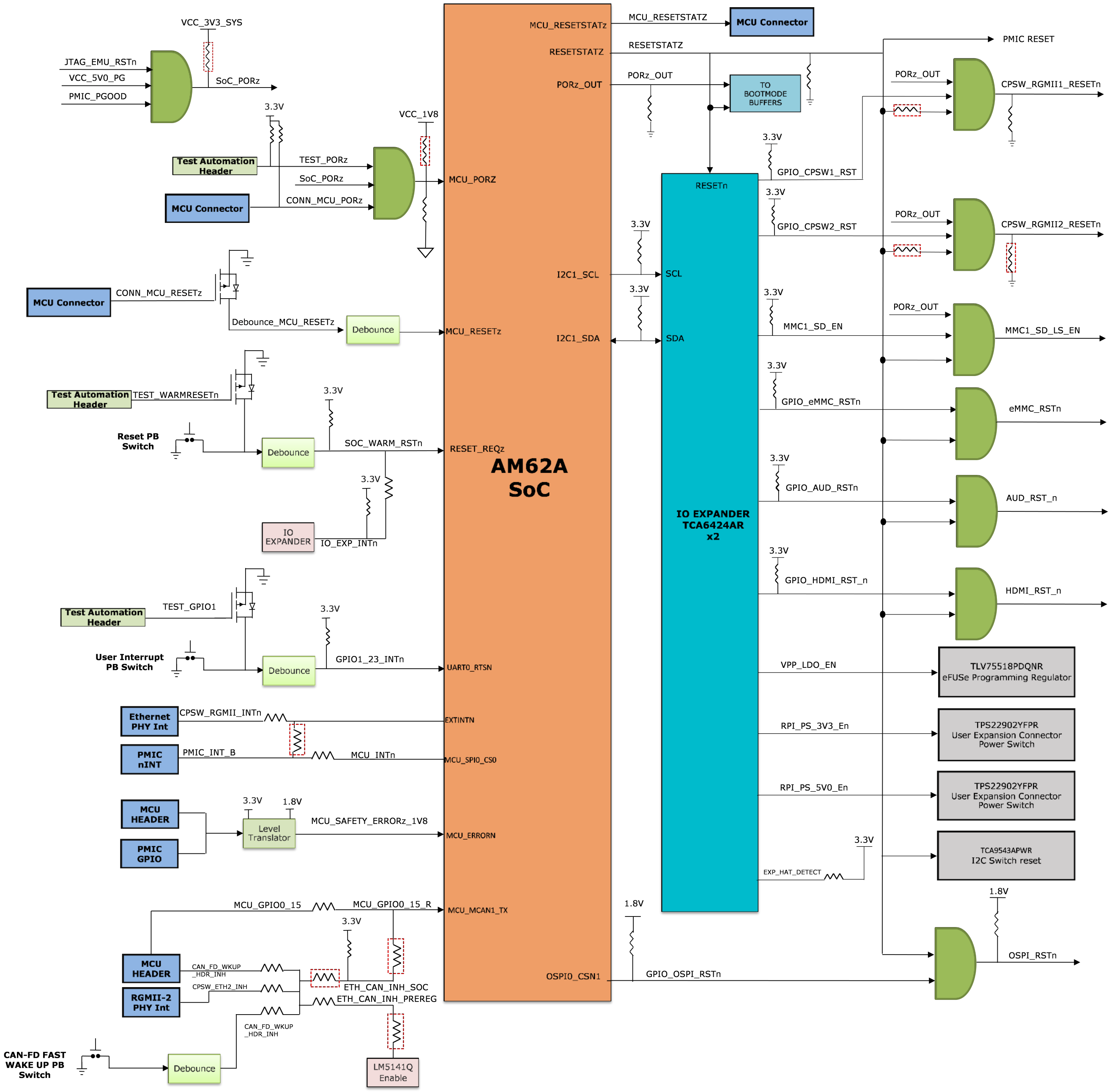

Figure 2-13. Reset Block Diagram

2.2.6.3 CSI Interface

The CSI-2 signals from the AM62A SOC can be connected to a 22 pin FFC connector to interface a CSI-2 standard Camera Card/Module or to a MIPI Connector for FPD Link interface through a 12 Bit Mux/Demux. The FFC and the MIPI connector shares some common auxiliary inputs from the IO Expander.

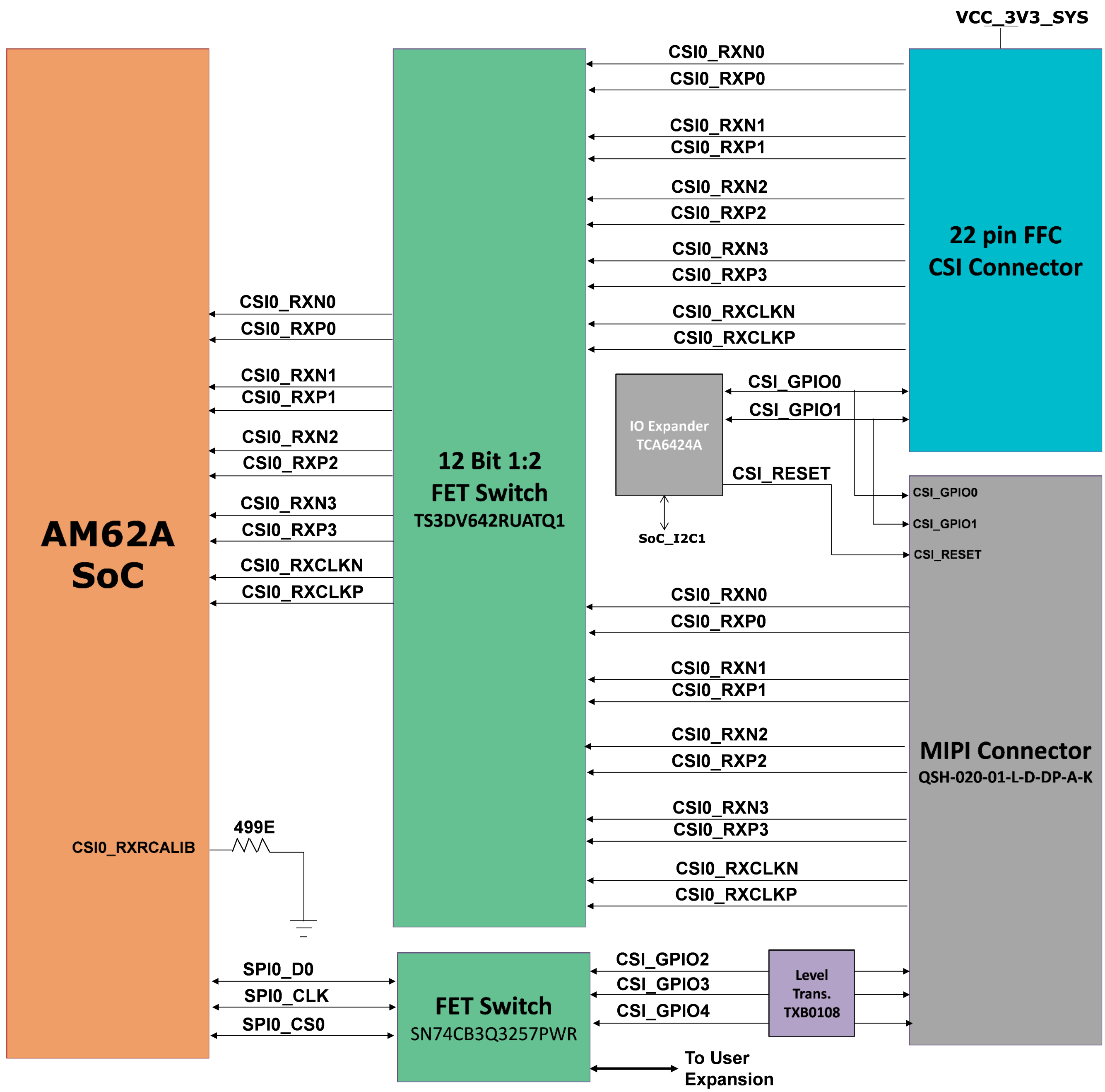

Figure 2-14. CSI Interface Block Diagram

Table 2-8 contains 40 pin Camera MIPI connector pin-out.

Table 2-8. CSI Camera Connector (J1) Pinout

Pin No	Pin Description	Pin No	Pin Description
1	NC	21	CSI0_MIPI_RXP3
2	CSI_MIPI_I2C2_SCL	22	CSI_MIPI_GPIO4
3	NC	23	CSI0_MIPI_RXN3
4	CSI_MIPI_I2C2_SDA	24	Ground
5	CSI0_MIPI_RXCLKP	25	NC
6	CSI_MIPI_GPIO0	26	NC
7	CSI0_MIPI_RXCLKN	27	NC
8	CSI_MIPI_GPIO1	28	NC
9	CSI0_MIPI_RXP0	29	NC
10	CSI_REFCLK	30	VCC_3V3_SYS
11	CSI0_MIPI_RXN0	31	NC
12	Ground	32	VCC_3V3_SYS
13	CSI0_MIPI_RXP1	33	NC
14	CSI_MIPI_RSTz	34	VCC_3V3_SYS
15	CSI0_MIPI_RXN1	35	NC
16	Ground	36	VCC_3V3_SYS
17	CSI0_MIPI_RXP2	37	NC
18	CSI_MIPI_GPIO2	38	VCC_CSI_IO
19	CSI0_MIPI_RXN2	39	NC
20	CSI_MIPI_GPIO3	40	VCC_CSI_IO

2.2.6.4 Audio Codec Interface

AM62A Low Power SK EVM houses TI's TLV320AIC3106 Stereo Audio Codec to interface with AM62A through the McASP1 group of signals.

TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic gain control (AGC) with mix and Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz.

One standard 3.5mm TRRS audio jack connector (J14) (manufacturer part number: SJ-43514) is provided for MIC IN and headphone output. Line inputs from the audio codec are terminated to test points.

The codec can be configured over I2C with device address set to 0x1B.

The controller clock input, MCLK to the audio codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock (BCLK) and Audio serial data bus input and output (DIN and DOUT) are connected to SOC's MCASP1_AXR0 and MCASP1_AXR2 through a Mux or Demux. An AND output of RESETSTATz and a GPIO sourced through the IO expander is used to reset the Audio codec.

The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply of 3.3V.

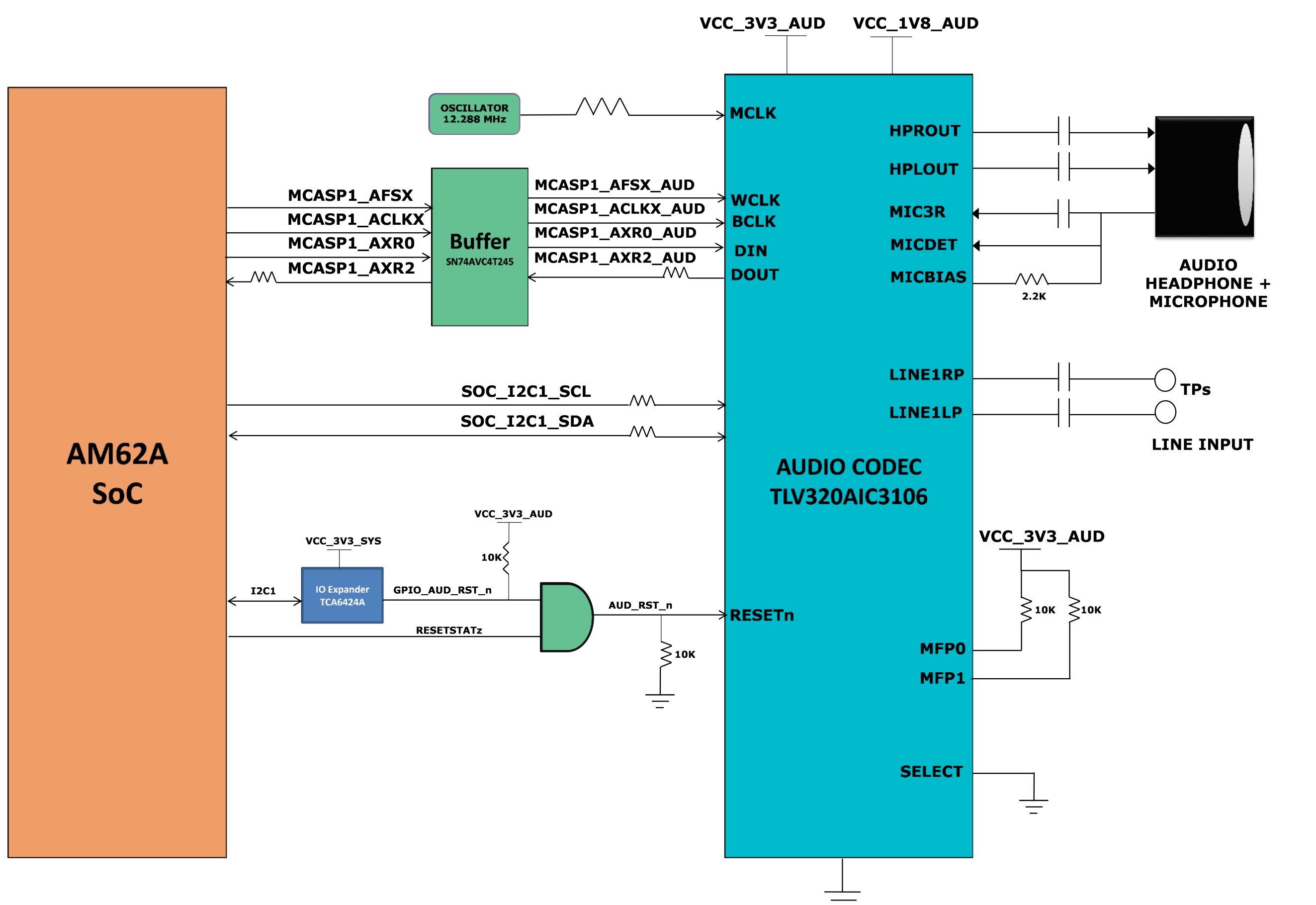

Figure 2-15. Audio Codec Interface Block Diagram

2.2.6.5 HDMI Display Interface

The DSS (Display Sub system) interface from AM62A SOC is used on the SKEVM to provide a HDMI Interface through a standard Type-A Connector. The SKEVM features a SiI9022A HDMI Transmitter from Lattice semiconductors to convert the 24bit Parallel RGB DSS output stream as well as McASP1 signals to a HDMI-compliant digital audio and video signal.

The Data mapping format used is RGB888. The data bus width is 24-bits.

To use the SiI9022A, the SOC needs to setup the device. Set up the device using the I2C1 interface between the SOC and the SiI9022A. SoC_I2C1 instance connected to the HDMI Transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. Audio Data is sent from the SOC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device.

TMDS Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through the HDMI ESD device (manufacturer part number: TPD12S016PWR). This device also acts as a load switch to limit current supplied to the HDMI connector from board 5V supply.

The HDMI Framer is powered using 3.3V Board IO Supply and 1.2V for the AVCC and DVCC supply by a dedicated LDO.

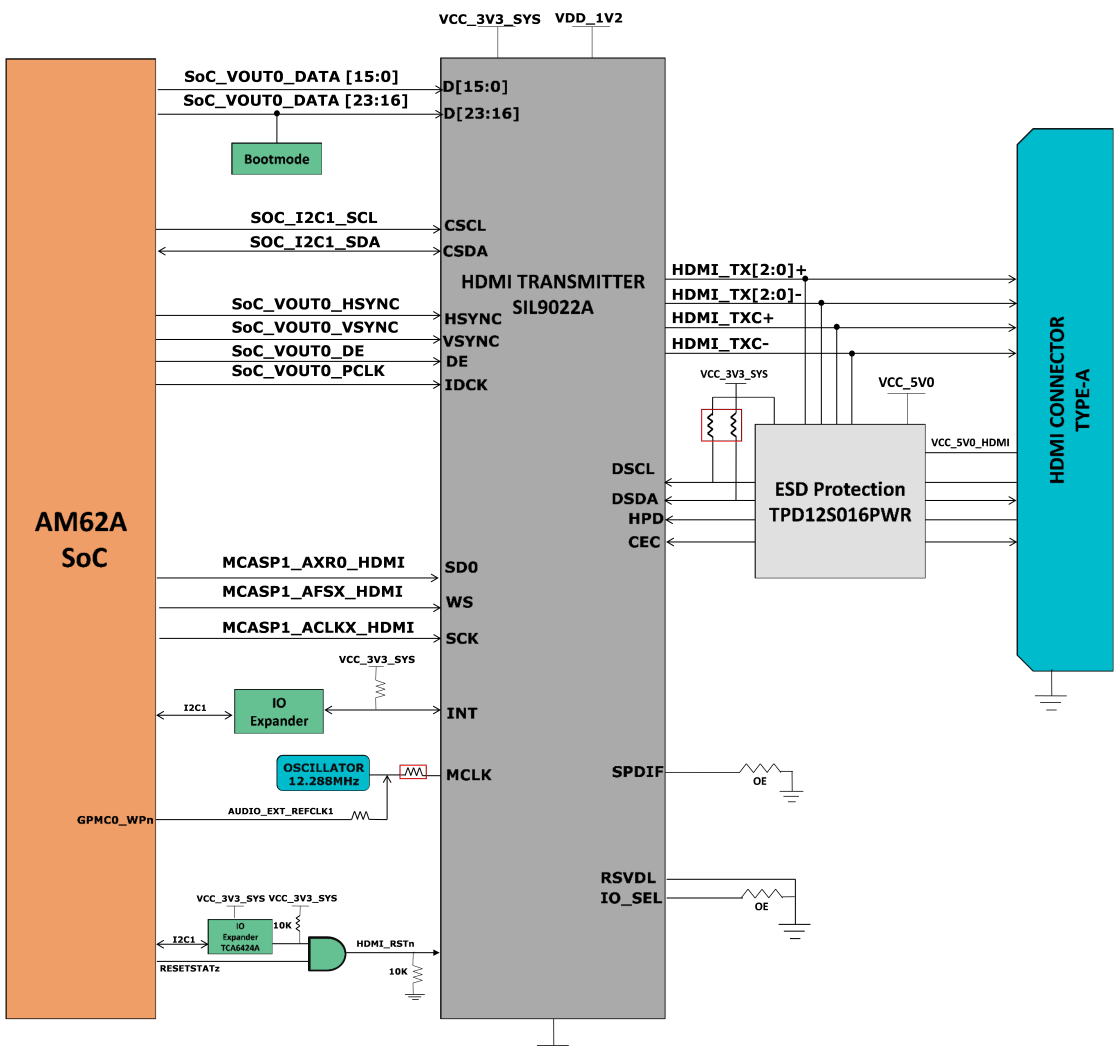

Figure 2-16. HDMI Interface Block Diagram

2.2.6.6 JTAG Interface

The AM62A Low Power SK EVM board includes XDS110 class on board emulation. The connection for this emulator uses an USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SKEVM.

Optionally, the JTAG Interface on SKEVM is also provided through a 20 pin Standard JTAG cTI Header J19. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals of cTI header from the rest of the SKEVM. The output of the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to the AM62A JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using an auto presence detect circuit, the mux routes the 20 pin signals from the cTI connector to the AM62A SoC in place of the on-board emulation circuit.

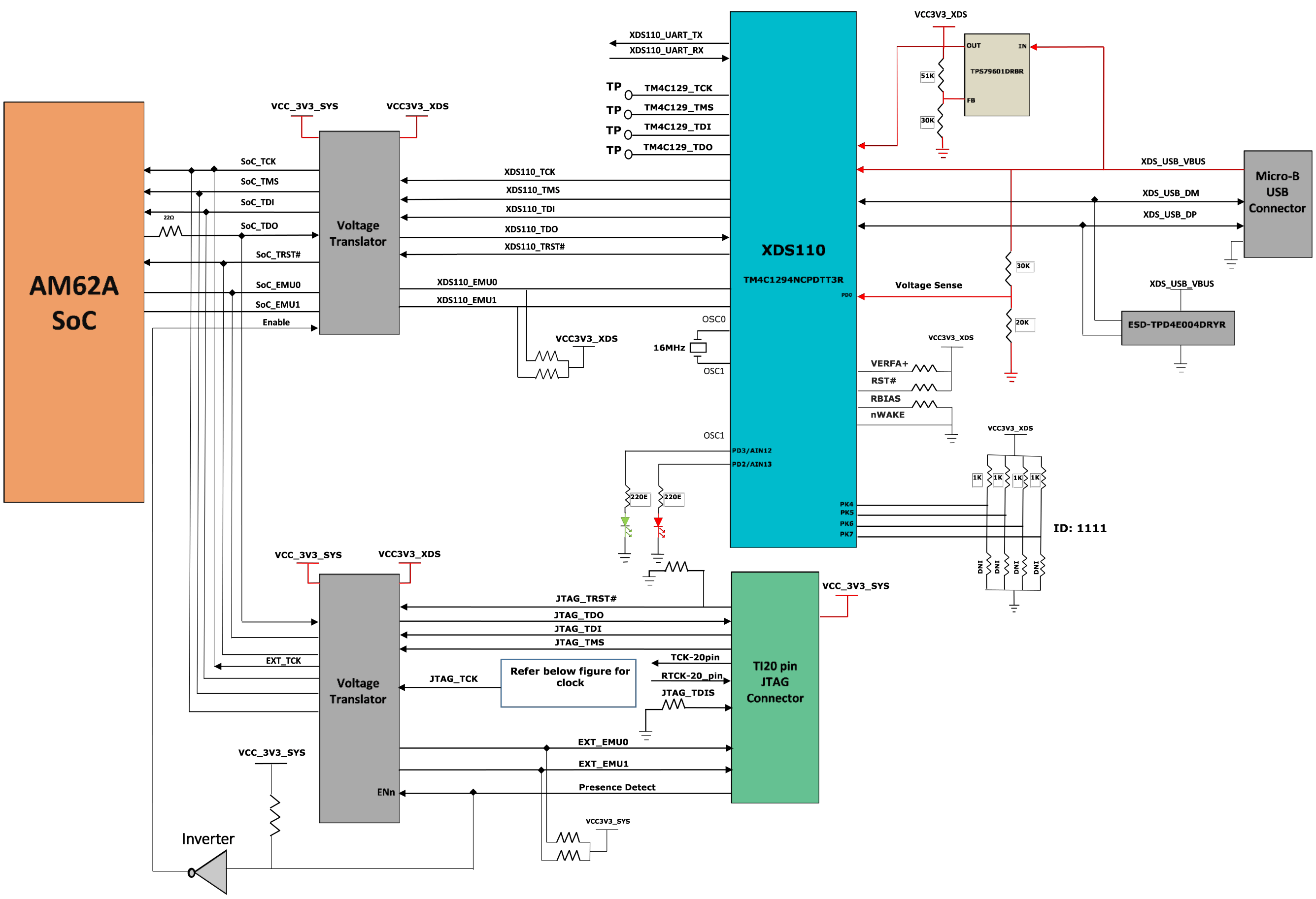

Figure 2-17. JTAG Interface Block Diagram

The pin-out of the cTI 20 pin JTAG connector are provided in Table 2-9. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap discharge.

Table 2-9. JTAG Connector (J19) Pin-Out

Pin Number	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.2.6.7 Test Automation Header

AM62A Low Power SK EVM has a 40 pin test automation header (FH12A-40S-0.5SH) to allow an external controller to manipulate some basic operations like Power Down, POR, Warm Reset, Boot Mode control, and so forth.

The test automation circuit is powered by the 3.3V supply generated by a dedicated *Always On* regulator (manufacturer part number: TPS62177DQCR). The I2C1 instance of the SOC is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the test automation header is connected to the 24 bit I2C boot mode IO Expander of TCA6424ARGJR to allow control of the boot modes for the AM62A SOC.

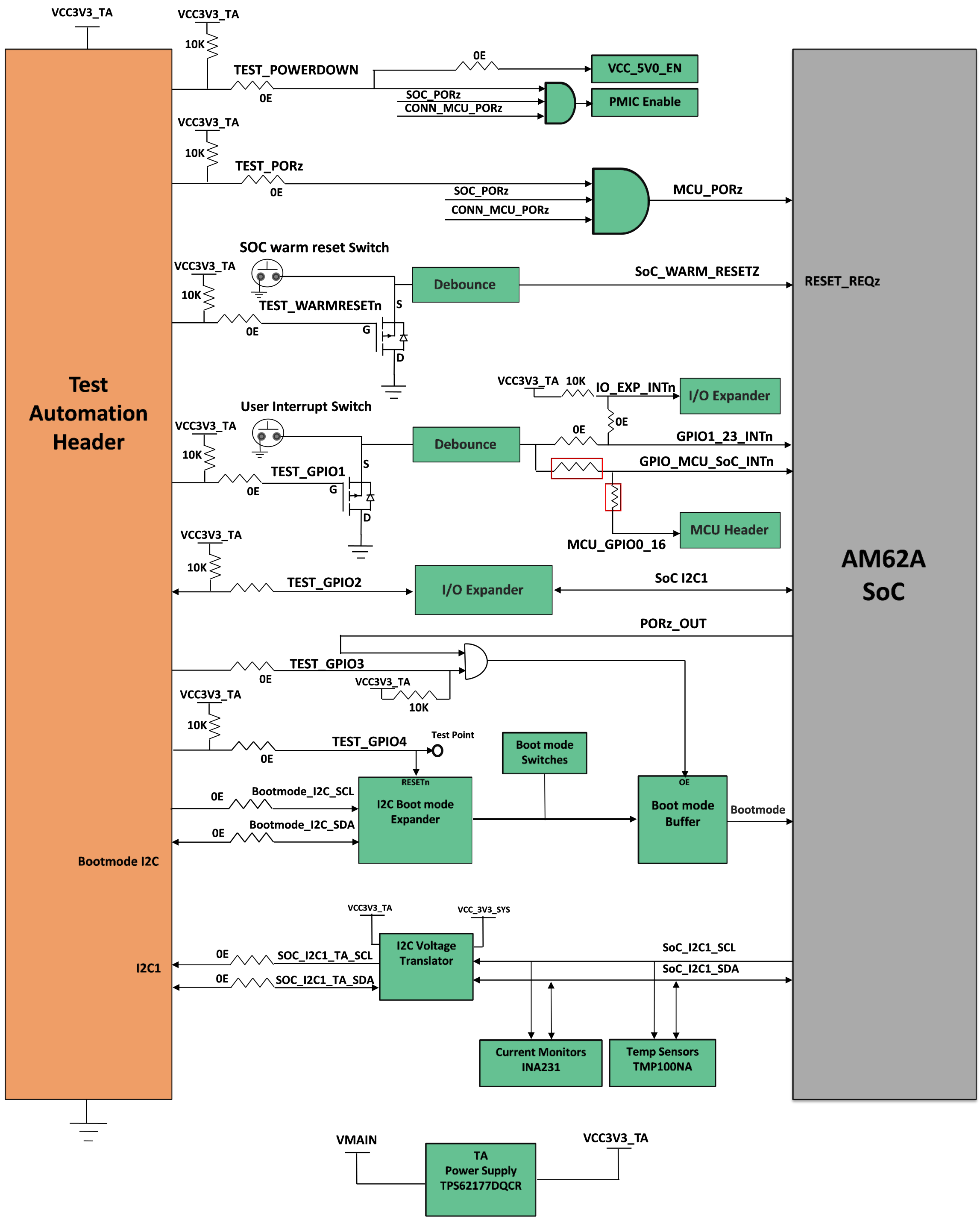

Figure 2-18. Test Automation Interface Block Diagram

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM62A. Boot mode for the AM62A can be user controlled by either using DIP Switches or the test automation header through the I2C IO Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C IO Expander. The boot mode can be set using two 8-bit DIP switches on the board, which connect a pull-up resistor to the output of a buffer when the switch is set to the ON position and to a weaker pull-down resistor when set to the OFF position. The output of the buffer is connected to the boot mode pins on the AM62A SOC and the output is enabled when the boot mode is needed during a reset cycle.

When boot mode is set through Test Automation header, the required switch values are set at the I2C IO expander output, which overwrites the DIP switch values to give the desired boot values to the SOC. The pins used for boot mode also have other functions which are automatically isolated by disabling the boot mode buffer during normal operation.

The power down signal from the Test automation header instructs the SKEVM to power down all the rails except for dedicated power supplies on the board. Similarly PORZn signal provides a hard reset to the SOC and WARM_RESETn for a warm reset to the SOC.

Pin Number	Signal	IO Direction	Pin Number	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESETn	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Input
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.2.6.8 UART Interface

The four UART ports of the SOC (MCU UART0, WKUP UART0, SOC UART0 and SOC UART1) are interfaced with an FTDI Bridge FT4232HL for UART-to-USB functionality and then terminated on a USB micro-B connector (J17) on board. When the AM62A Low Power SK EVM is connected to a Host using USB cable, the computer can establish a Virtual COM Port that can be used with any terminal emulation application. The FT4232HL device is bus powered.

Since the circuit is powered through the USB BUS, the connection to the COM port is not lost when the SKEVM power is removed.

Table 2-10. UART Interface

UART Port	USB to UART Bridge	USB Connector	COM Port
SOC_UART0	FT4232HL	J17	COM1
SOC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in 'Single chip USB to four channel UART' mode using the configuration file from an external SPI EEPROM connected to the chip. The EEPROM (93LC46B) supports 1Mbit/s clockrate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from the FTDI website. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

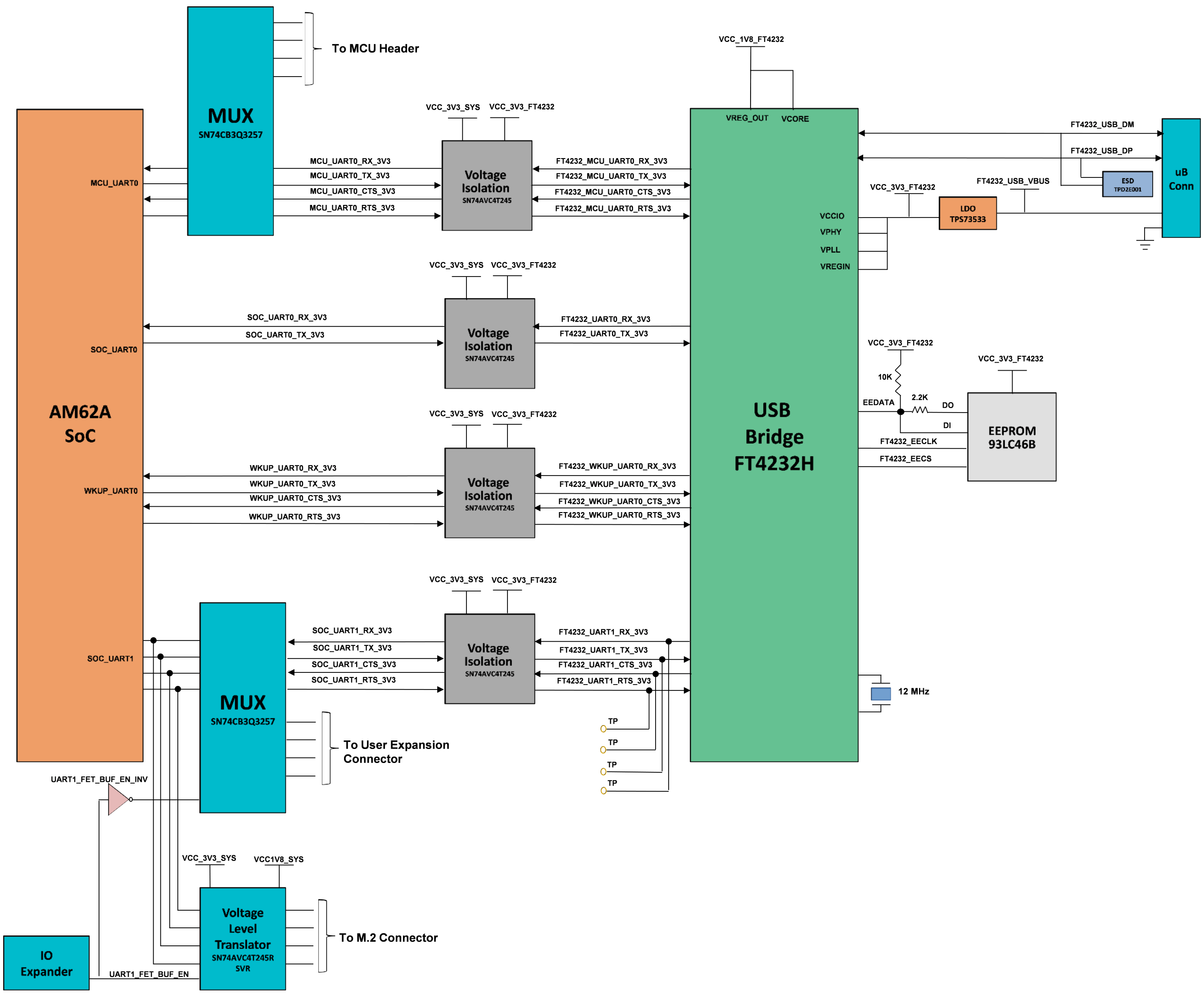

Figure 2-19. UART Interface Block Diagram

2.2.6.9 USB Interface

2.2.6.9.1 USB 2.0 Type A Interface

USB2.0 data lines from Type A connector J7 are connected to the USB1 interface of the AM62A SOC to provide USB high-speed/full-speed communication. USB1_VBUS to the SOC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1_DRVVBUS from SOC is connected to the enable pin of Load switch (manufacturer part number: TPD3S014DBVR) to allow on board 5V supply to power the VBUS.

A common mode choke of (manufacturing part number DLW21SZ900HQ2B) is provided on USB data lines for EMI and EMC reduction. USB Data lines from Type-A connectors are also connected to the Current Limit Load Switch and ESD Protection IC (manufacturer part number: TPD3S014DBVR. This switch limits the current to 500mA and dissipates the ESD strikes above the maximum level specified in the IEC 61000-4-2.

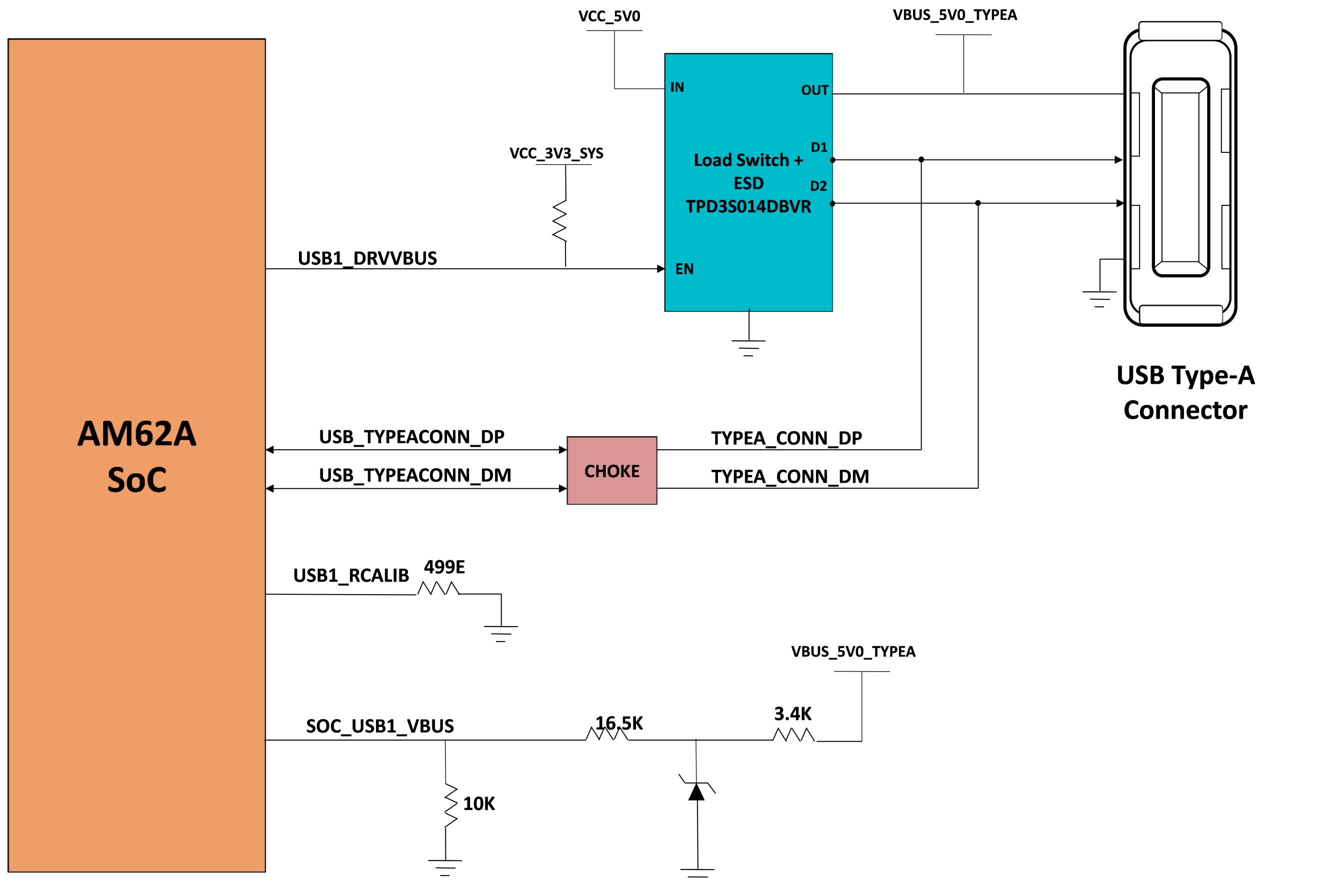

Figure 2-20. USB Type A Interface Block Diagram

2.2.6.9.2 USB 2.0 Type C Interface

On SK EVM, USB 2.0 Interface is offered through USB Type-C Connector J15 (manufacturer part number: 2012670005) which supports data rate up to 480Mbps. J15 can be used for data communication and also as a power connector sourcing supply to the low power SK EVM. J15 is configured as a DRP port using PD controller TPS65988DHRSHR IC, so J15 can act as either a Host or Device. The role of the port depends on the type of the device getting connected on the connector and the ability to either sink or source. When the port is acting as DFP, the port can source up to 5V at 500mA.

USB2.0 Data lines from J15 are provided with a choke and an ESD protection device. USB0_VBUS to the SOC is provided through a resistor divider network to support (5V to 30V) VBUS operation.

A common mode choke of DLW21SZ900HQ2B is provided on USB Data lines for EMI and EMC reduction. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP or DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J15 to dissipate ESD strikes.

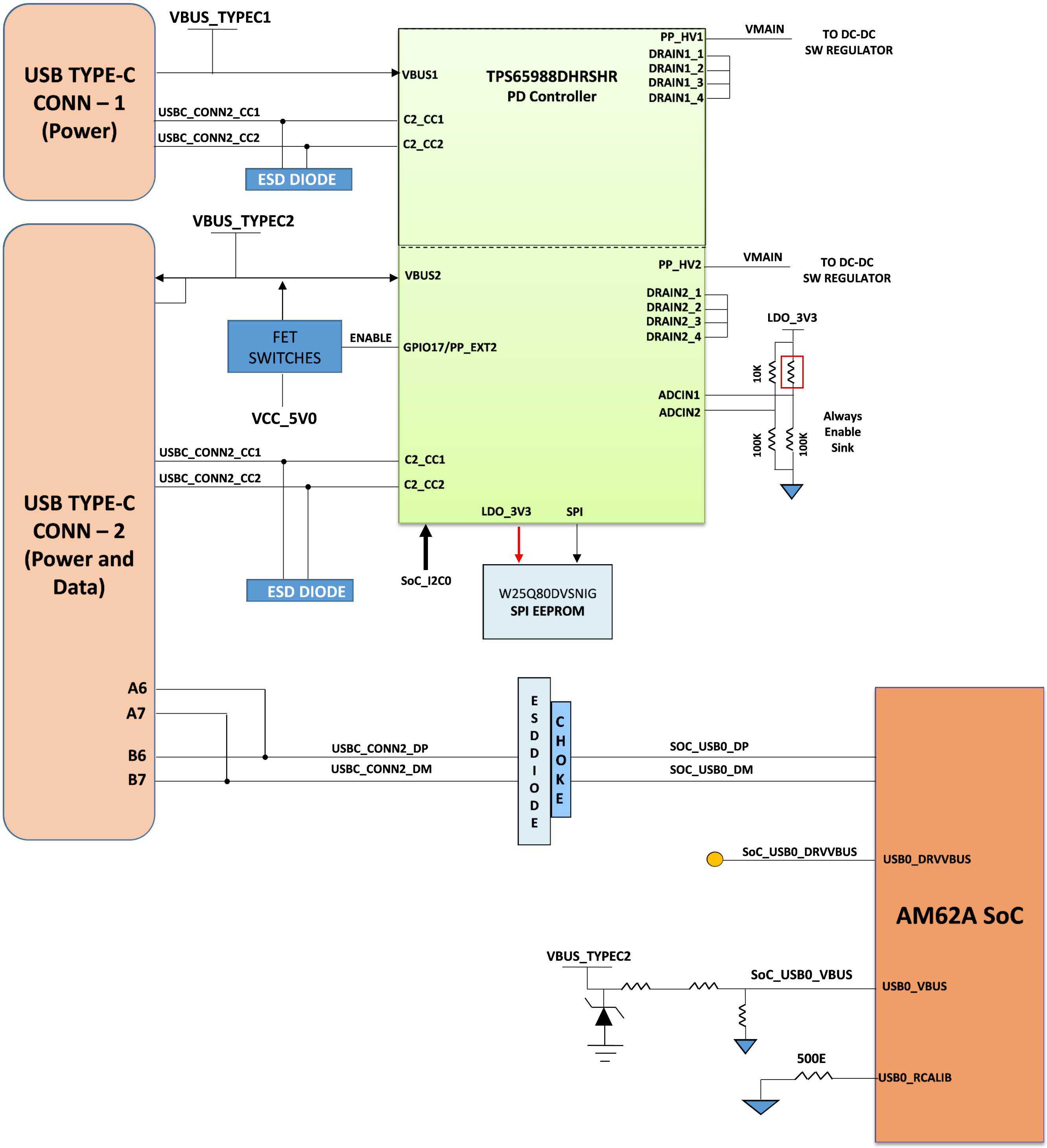

Figure 2-21. USB2.0 Type C Interface Block Diagram

2.2.6.10 Memory Interfaces

2.2.6.10.1 LPDDR4 Interface

AM62A Low Power SK EVM houses a MT53E2G32D4DE-046 from Micron which is a dual rank dual die 4GB, 32 bit wide LPDDR4 memory supporting data rates up to 4266Mb/s. The LPDDR4 memory is placed and routed to the DDR0 group of SOC to support point to point communication.

The LPDDR4 memory requires 1.8V for the core supply, thus reducing power demand. The I/Os are supplied from a 1.1V supply output from the PMIC. LPDDR4 reset (Active low) controlled by the AM62A SOC is pulled down to set the default active state. The provision for mounting a pull up resistor is also provided.

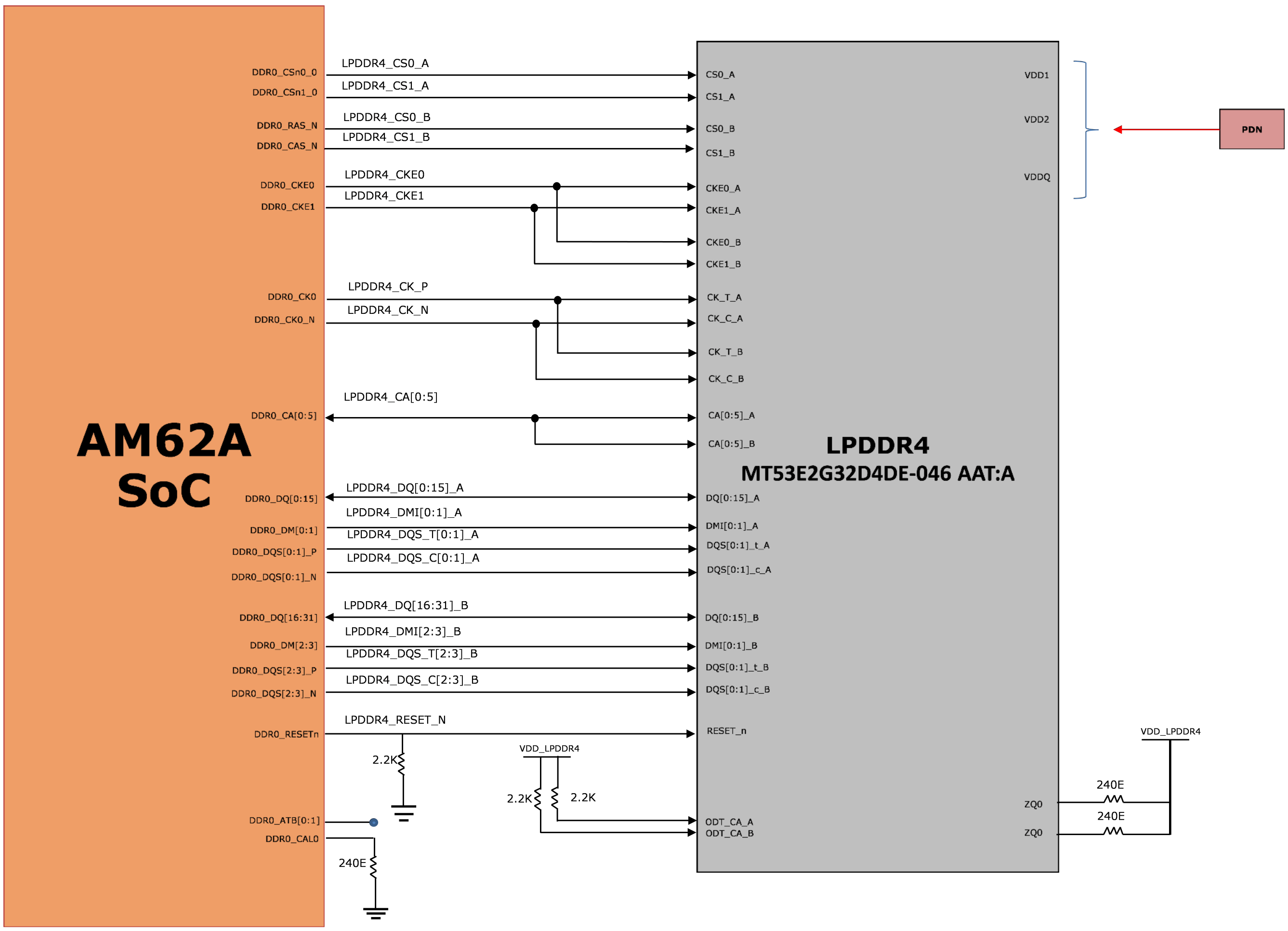

Figure 2-22. LPDDR4 Interface Block Diagram

2.2.6.10.2 Octal Serial Peripheral Interface (OSPI)

AM62A Low Power SK EVM board features a 1Gbit OSPI memory device from Cypress part number W35N01JWTBAG which is connected to the OSPI0 interface of the AM62A SOC. The OSPI supports single and double data rates with clock speeds up to 166Mhz STR and 120Mhz DTR.

OSPI and QSPI implementation: 0Ω resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0Ω series resistors provided for pins OSPI_DATA[4:7] can be removed if a QSPI Flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62A SOC with the signal GPIO_OSPI_RSTn from the SOC. A pull-up resistor is provided on GPIO_OSPI_RSTn to set the default active state.

Power: Both VCC and VCCQ pins of the OSPI Flash memory is supplied through an on board 1.8V system power. The OSPI I/O group is powered by the VDDSHV1 domain of SOC and is also connected to 1.8V system power.

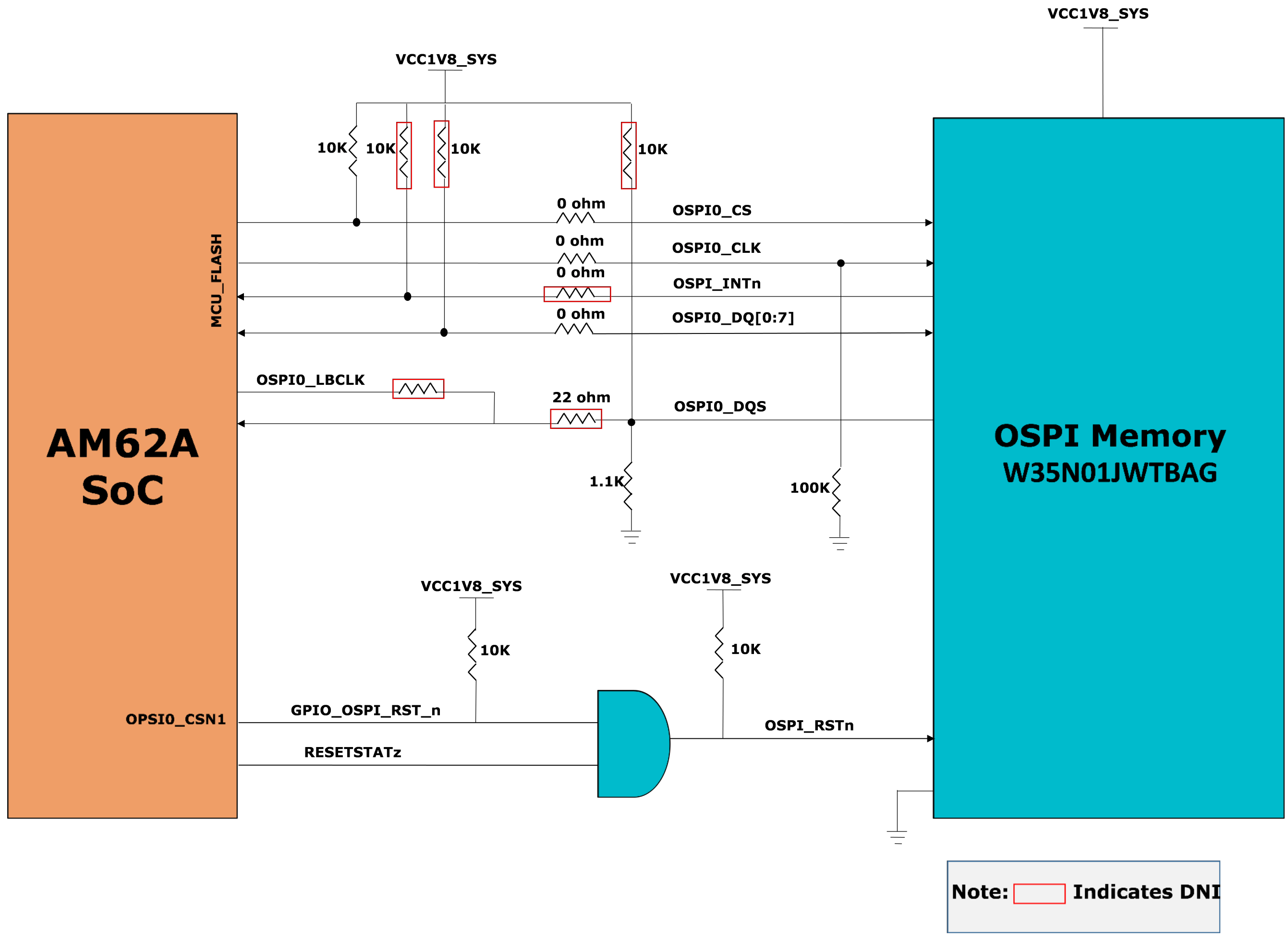

Figure 2-23. OSPI Block Diagram

2.2.6.10.3 MMC Interfaces

The AM62A SOC features three MMC ports (MMC0, MMC1 and MMC2). MMC0 is connected to eMMC, MMC1 is interfaced with a Micro SD Card connector and MMC2 is terminated to a connector for M.2 form factored Wi-Fi and BT Module Interface.

2.2.6.10.3.1 MMC0 - eMMC Interface

The SKEVM board contains 16GB of eMMC flash memory from Micron, part number MTFC16GAPALBH-IT, connected to MMC0 port of the AM62A SOC.

The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200MHz. The Micron eMMC is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component. Option to mount external pull up resistors are provided on DAT[7:1] to prevent bus floating and series resistor is provided for CLK signal close to SOC pad to match the characteristic impedance of PCB.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0interface of the SOC is powered by the VDDSHV4 power domain, which is connected to 1.8V IO supply.

eMMC device requires active low reset from host. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use this register byte. The External Reset is provided by ANDing RESETSTATz from SOC and a GPIO from IO Expander. A pull up is provided on GPIO pin to set the default active state.

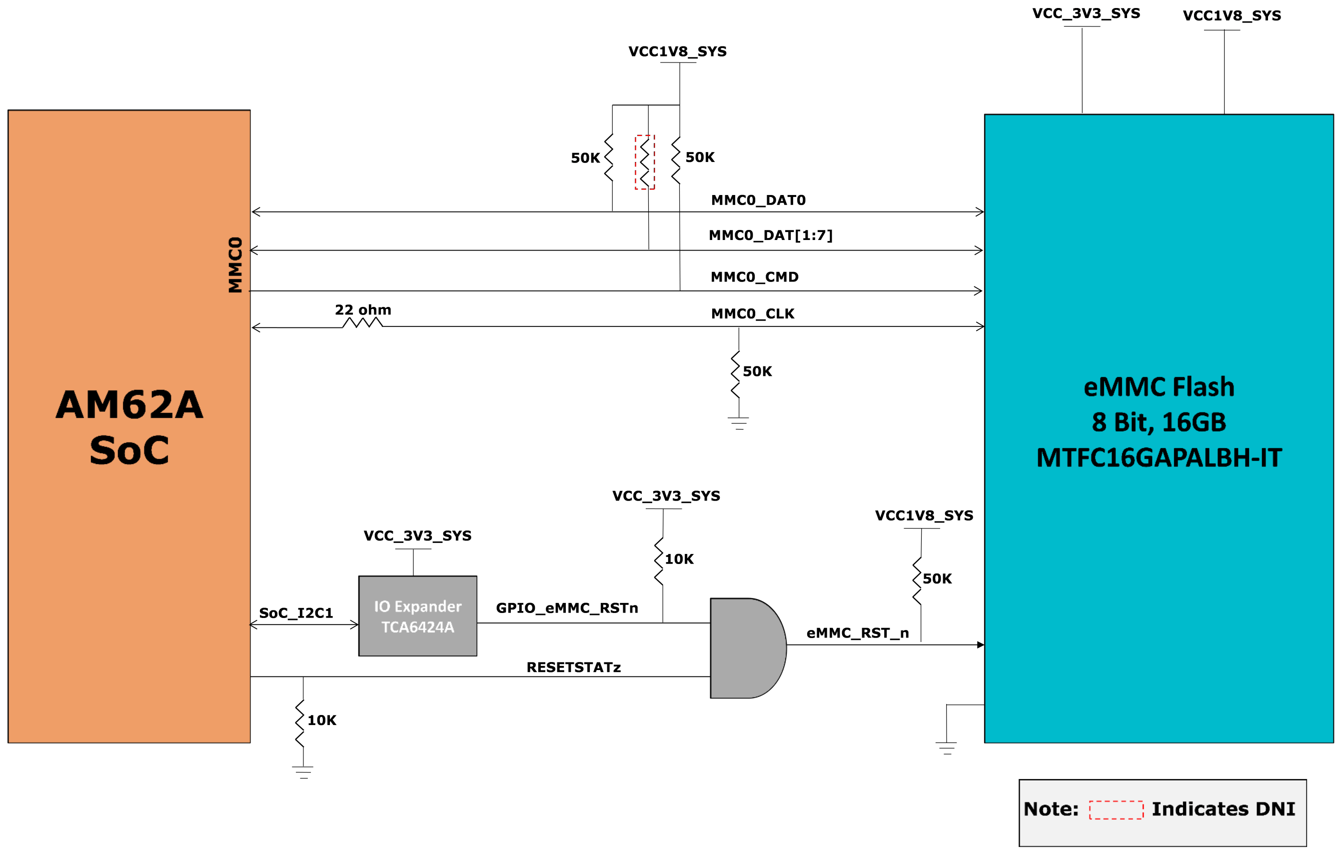

Figure 2-24. EMMC Interface Block Diagram

2.2.6.10.3.2 MMC1 - Micro SD Interface

The SKEVM board provides a micro SD card interface connected to the MMC1 port of the AM62A SOC. The MicroSD card socket of MEM2051-00-195-00-A is used to support this interfacing. UHS1 operation is supported, including IO operations at both 1.8V and 3.3V. The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SOC tries to find the fastest speed that the card and controller can support and then have a transition to 1.8V through a VSEL_SD_SOC signal.

The SD Card connector power is provided using a load switch of TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from IO Expander.

An ESD protection device, TPD6E001RSE, is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8kV contact discharge and ± 15kV air-gap discharge.

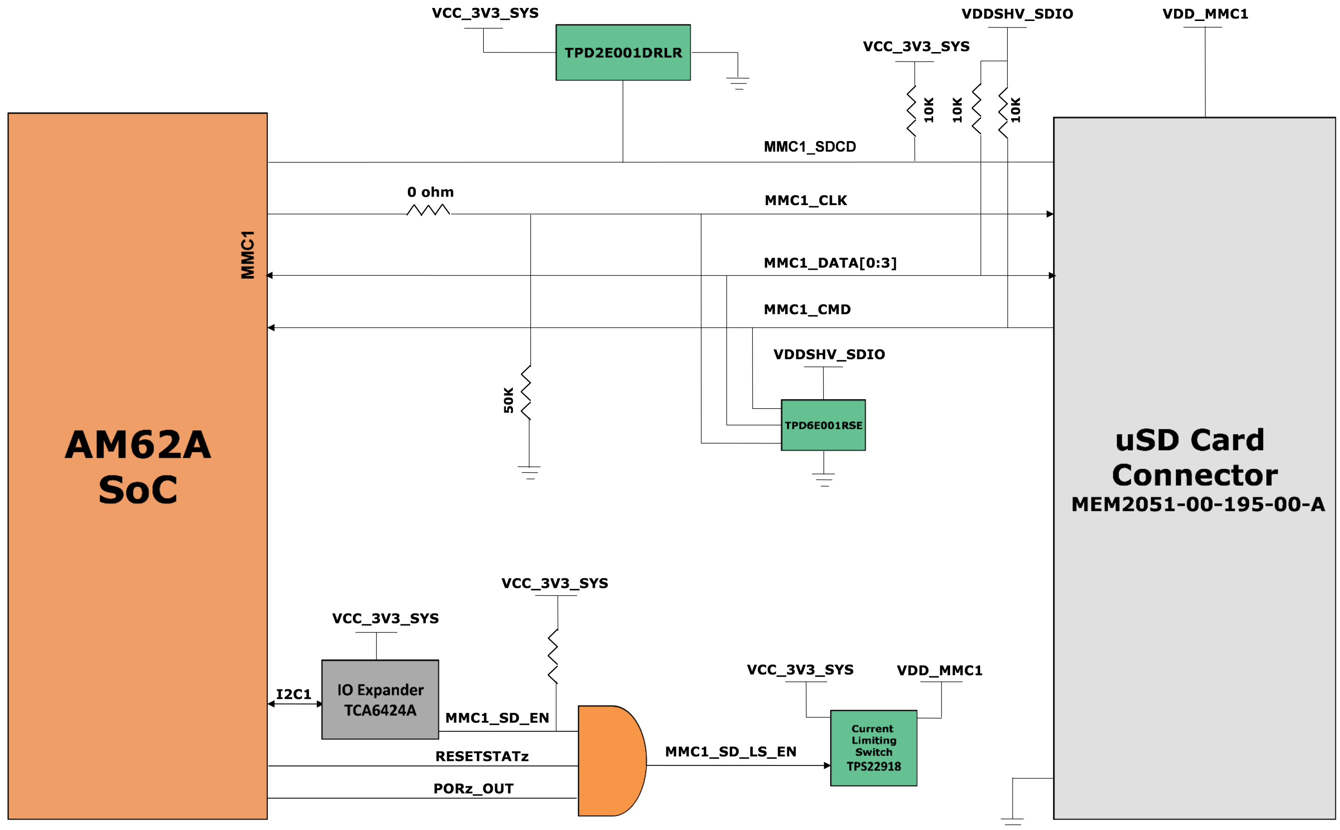

Figure 2-25. Micro SD Interface Block Diagram

2.2.6.10.3.3 MMC2 - M.2 Key E Interface

AM62A Low Power SK EVM has a M.2 Key E interface for connecting WiFi BT modules connected to MMC2, UART2 instances and McASP1 interface through buffers. This can be used to interface with a Wi-Fi, dual-band, 2.4 and 5GHz module with antennas supporting Industrial temperature grade. The M.2 is provided with 4-bit IO of the MMC2 interface supporting IEEE standard 802.11a/b/g/n data. The M.2 connector can be interfaced with modules that can offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence for a power-optimized design.

The M.2 Connector is provided with a 3.3V on board power supply to meet the power supply requirements of the interfacing modules. The MMC2 interface of the SOC is powered by the VDDSHV6 power domain, which is connected to 1.8V IO supply.

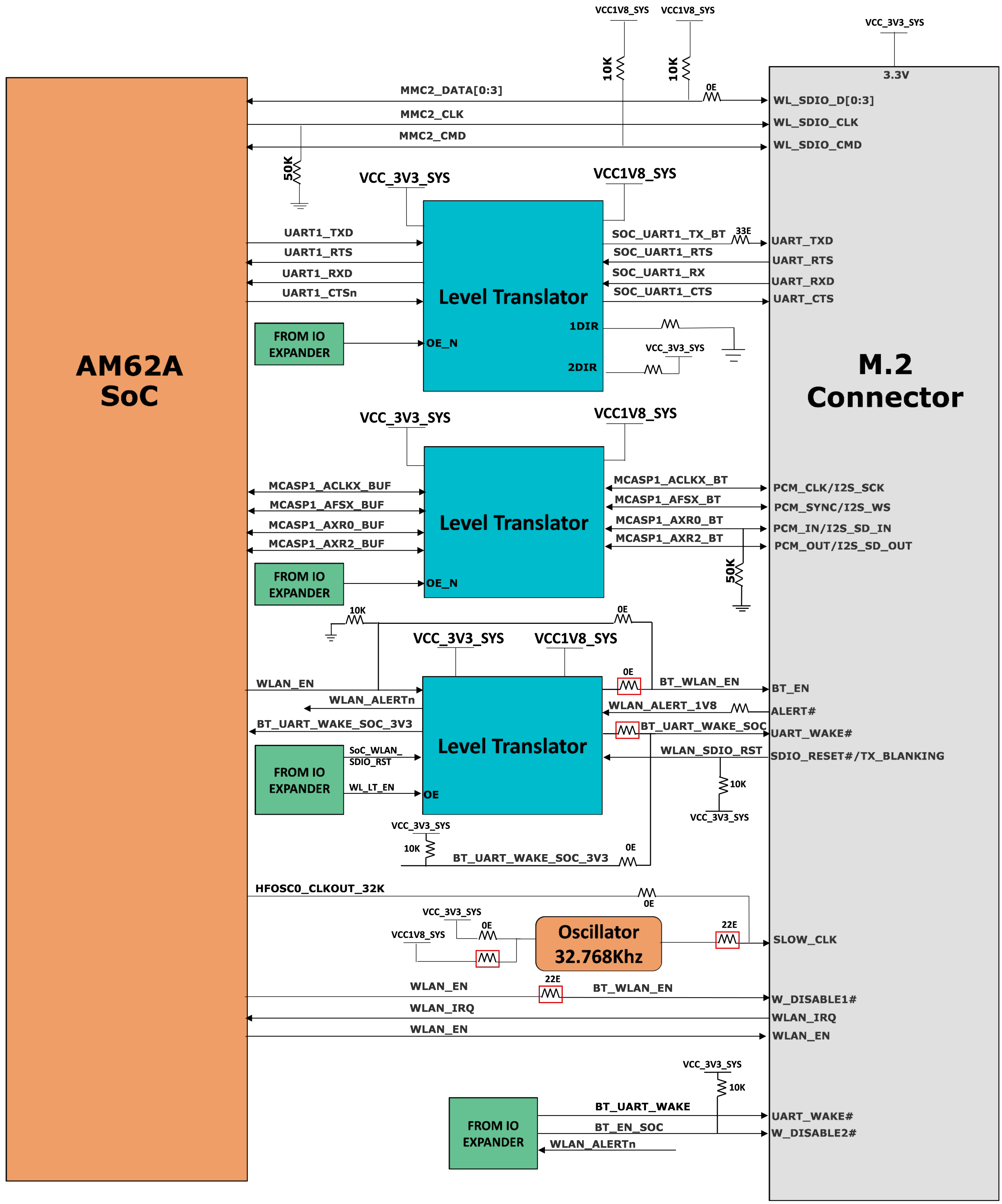

Figure 2-26. M.2 Key E Interface block diagram

2.2.6.10.4 Board ID EEPROM

AM62A Low Power SK EVM boards can be identified remotely from the version and serial number data stored on the onboard EEPROM.

Board ID memory AT24C512C-MAHM-T from Microchip is interfaced to the I2C0 port of the SOC and is configured to respond to address 0x51 programmed with the header description. I2C address of the EEPROM can be modified by driving the A0 pin to high and A1, A2 pins to LOW. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

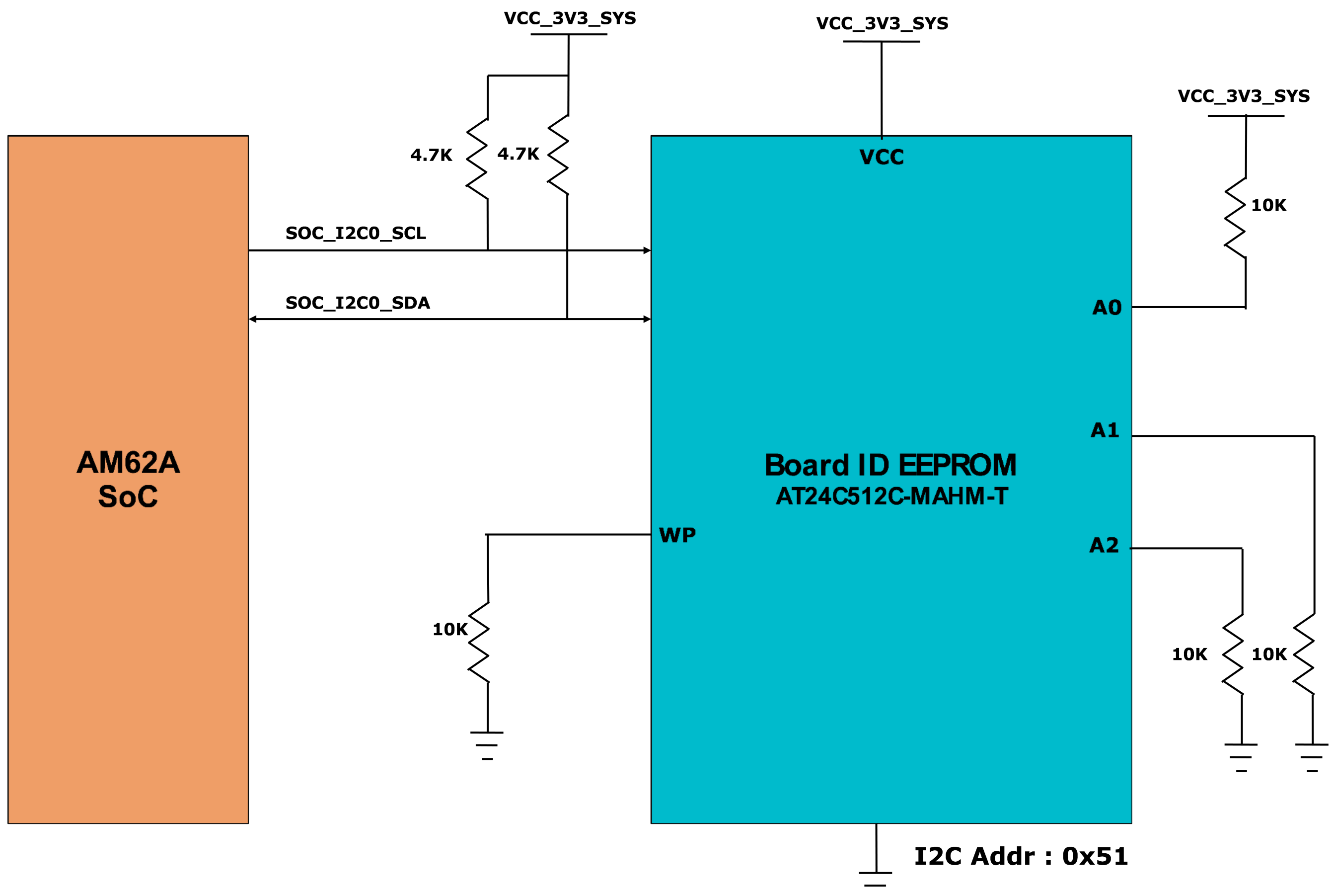

Figure 2-27. Board ID EEPROM Block Diagram

2.2.6.11 Ethernet Interface

The AM62A Low Power SK EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication.

RGMII1 and RGMII2 Gigabit Ethernet CPSW Port from AM62A SOC is connected to the On-Board PHY Transceiver DP83867.

CPSW_RGMII1and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

Note

RGMII2 modular connector in E1 and E2 version EVM is descoped.

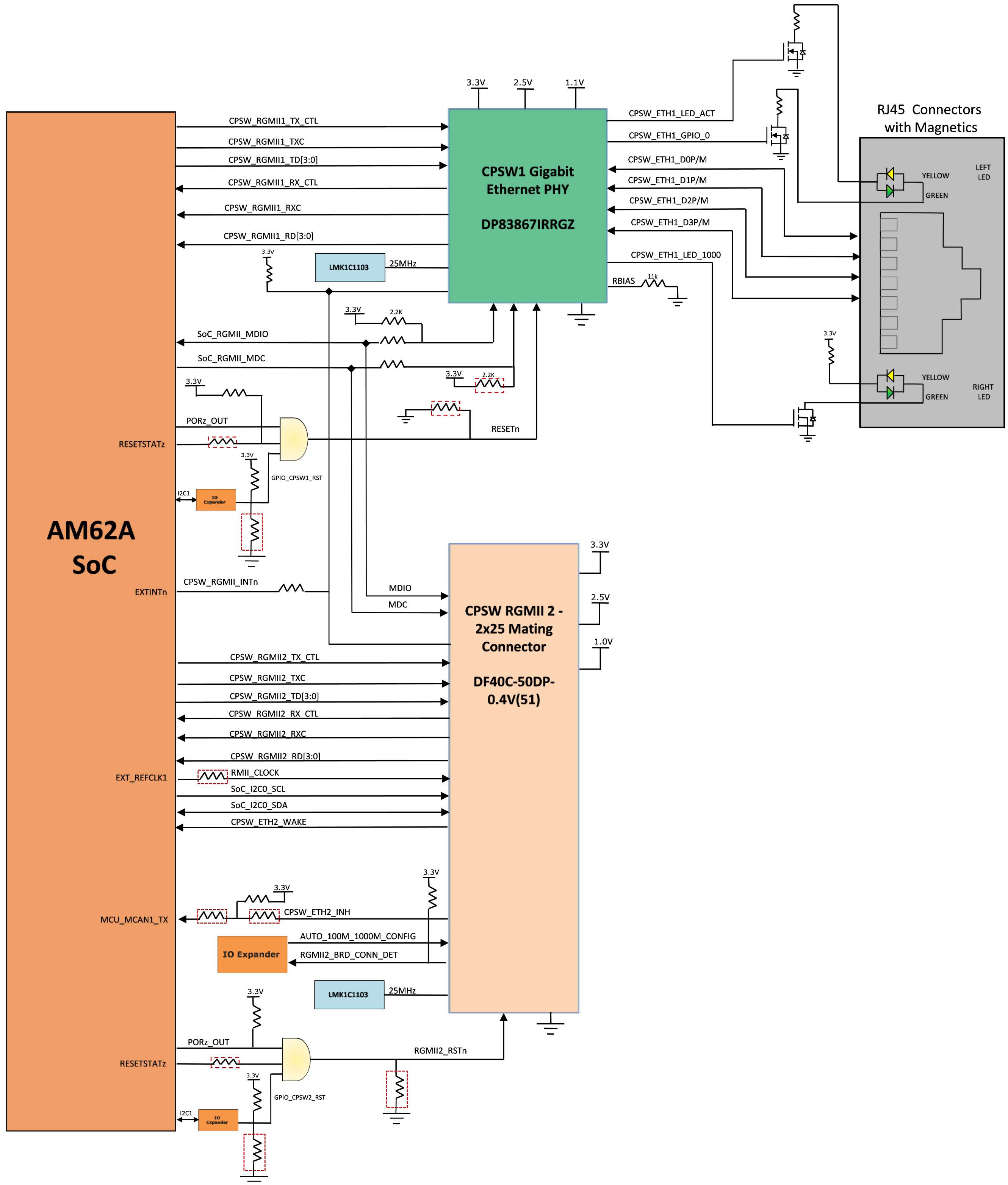

Figure 2-28. Ethernet Interface block diagram - Rev E1 and E2

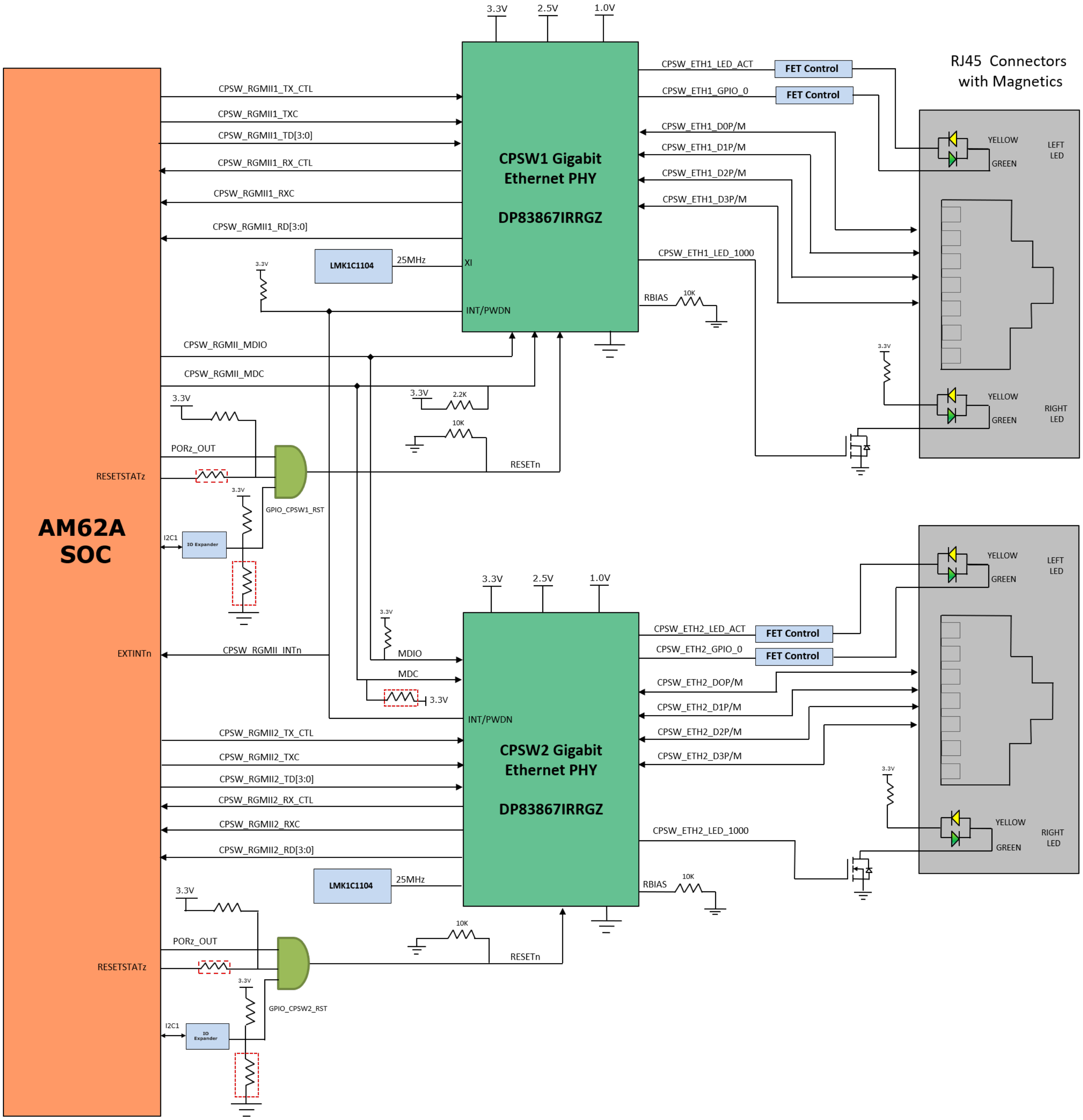

Figure 2-29. Ethernet Interface block diagram - Rev E3 and A

2.2.6.11.1 CPSW Ethernet PHY Default Configuration

The default configuration of the DP83867 is determined using several resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. The AM62A Low Power SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltages ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

Mode1 - 0V to 0.3V

Mode 2 – 0.462V to 0.6303V

Mode3 – 0.7425V to 0.9372V

Mode4 – 2.2902V to 2.9304V

Footprints for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to Mode1 by default, Mode4 is not applicable and Mode2, Mode3 option is not desired. The PHY is resistor strapped for the below configurations:

PHY ADDR: 00000

Auto_neg: Enabled

ANG_SEL : 10/100/1000

RGMII TXCLK skew : 0ns

RGMII RXCLK skew : 2ns

Table 2-11. CPSW Ethernet Strap Settings

Strap Setting	Pin Name	Strap Function	Mode	Value of Strap Function	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0000
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	1	0	
		PHY_AD0	1	0	
Auto Negotiation	RX_DV/ RX_CTRL	Auto- neg	3	0	Autoneg Disable=0
Modes of Operation	LED2	RGMII Clock Skew TX[1]	5	0	RGMIITX Clock Skew is set to 0ns
		RGMII Clock Skew TX[0]	5	0	
	LED_1	RGMIIClock Skew TX[2]	5	1	
		ANEG_SEL	1	0	Advertiseability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMIIRX Clock Skew is set to 2ns
		RGMII Clock Skew TX[1]	1	0	
	GPIO_0	RGMII Clock Skew RX[0]	1	0	

2.2.6.12 GPIO Port Expander

The I/O expanders used in the AM62A Low Power SKEVM is a 24-Bit I2C based I/O expander that is used for daughter cards plug-in detection and for generating resets and enable signals to various peripheral devices that are connected. The SoC_I2C1 bus of the AM62A SOC is used to interface with the I/O expanders. The I2C device addresses of the I/O Expander are 0x21 and 0x23.

Table 2-12. IO EXPANDER - 01

Pin No	SIGNAL	DIRECTION	PURPOSE
P00	NC	-	-
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P02	BT_EN_SOC	OUTPUT	M.2 Module Bluetooth Enable
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_EN	OUTPUT	SOC eFuse Voltage(VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P10	GPIO_AUD_RSTn	OUTPUT	Audio Codec Reset Control GPIO
P11	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO
P12	UART1_FET_BUF_EN	OUTPUT	SOC UART1 Mux Select
P13	BT_UART_WAKE_SOC_3V3	INPUT	BT UART WKUP Signal
P14	GPIO_HDMI_RSTN	OUTPUT	HDMI Transmitter Reset Control GPIO
P15	CSI_GPIO0	NA	CSI0 GPIO1
P16	CSI_GPIO1	NA	CSI0 GPIO2
P17	WLAN_ALERTn	INPUT	M.2 Module WLAN Alert
P20	HDMI_INTN	INPUT	HDMI Interrupt
P21	TEST_GPIO2	INPUT	TEST GPIO2 from Test Automation Connector
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction Control
P23	MCASP1_BUF_BT_EN	OUTPUT	
P24	MCASP1_FET_SEL	OUTPUT	
P25	UART1_FET_SEL	OUTPUT	UART1 Mux/Demux Selection control
P26	PD_I2C_IRQ	INPUT	Interrupt Request from PD Controller
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2

Table 2-13 shows the list of signals being controlled by the expander.

Table 2-13. IO EXPANDER - 02

Pin No	SIGNAL	DIRECTION	DEVICE
P10	WL_LT_EN	OUTPUT	M.2 Interface Level Translator Enable
P11	CSI_RSTZ	OUTPUT	CSI Reset control GPIO
P20	SPI0_FET_SEL	OUTPUT	SOC SPI0 MUX Selection
P21	SPI0_FET_OE	OUTPUT	SOC SPI0 MUX Enable
P22	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P23	CSI_SEL2	OUTPUT	CSI Mux/Demux Selection Control
P24	CSI_EN	OUTPUT	CSI Mux/Demux Enable
P25	AUTO_100M_1000M_CONFIG	OUTPUT	WLAN Reset control GPIO
P26	CSI_VLDO_SEL	OUTPUT	CSI I/O Voltage selection control (VCC_CSI_IO)
P27	SOC_WLAN_SDIO_RST	OUTPUT	M.2 Module WLAN/SDIO Reset

2.2.6.13 GPIO Mapping

Table 2-14 describes the detailed GPIO mapping of AM62A SOC with AM62A Low Power SK EVM peripherals.

Table 2-14. Mapping of AM62A SoC with AM62A Low Power SK EVM Peripherals

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction With Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPI0_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH								
10	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
11	Interrupt Signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	Watchdog trigger input signal for Watchdog Trigger mode	PMIC_WDOG_TRIGG	ENABLE	MCU_GPIO0_19	WKUP_I2C0_SCL	IPNUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
14	WKUP Signal from RGMII2	CPSW_ETH2_WAKE	INTERRUPT	MCU_GPIO0_20	WKUP_I2C0_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1P8
19	PMIC Standby Disable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	LOW	HIGH	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	eMMC Reset control GPIO	GPIO_EMMC_RSTN	RESET	IO_EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO_EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO_EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO_EXPANDER-P03		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	SOC eFuse Voltage (VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO_EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V PowerSwitch Enable	EXP_PS_3V3_EN	ENABLE	IO_EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V PowerSwitch Enable	EXP_PS_5V0_EN	ENABLE	IO_EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTN	RESET	IO_EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO_EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
10	SOC UART1 Mux Select	UART1_FET_BUF_EN	SELECT	IO_EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	BT UART WKUP Signal	BT_UART_WAKE_SOC	INTERRUPT	IO_EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS

Table 2-14. Mapping of AM62A SoC with AM62A Low Power SK EVM Peripherals (continued)

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction With Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
12	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTN	RESET	IO_EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
13	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO_EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO_EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
15	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO_EXPANDER-P17		INPUT	LOW	HIGH		VCC_3V3_SYS
16	HDMI Interrupt	HDMI_INTN	INTERRUPT	IO_EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
17	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO_EXPANDER-P21		INPUT	HIGH	LOW		VCC_3V3_SYS
18	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO_EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
19		MCASP1_BUF_BT_EN	ENABLE	IO_EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
20		MCASP1_FET_SEL	DIRECTION CONTROL	IO_EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
21		UART1_FET_SEL	DIRECTION CONTROL	IO_EXPANDER-P25		OUTPUT	HIGH	LOW		
22	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO_EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
23	IO EXPANDER - 01	IO_EXP_TEST_LED	GPIO	IO_EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	SoC SPI0 MUX Selection	SPI0_FET_SEL	ENABLE	IO_EXPANDER-P20		OUTPUT	LOW	HIGH		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPI0_FET_OE	CONTROL	IO_EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CSI Regulator Enable (VCC_CSI_IO)	CSI_VLDO_SEL	ENABLE	IO_EXPANDER-P26		OUTPUT	LOW	HIGH		VCC_3V3_SYS
4	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO_EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
5	Wilink Enable	WL_LT_EN	ENABLE	IO_EXPANDER-P10		OUTPUT	LOW	LOW		VCC_3V3_SYS
6	CSI Reset control GPIO	CSI_RSTZ	RESET	IO_EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	CSI flex and mipi MUX Selection	CSI_SEL2	ENABLE	IO_EXPANDER-P23		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	CSI MUX Enable	CSI_EN	ENABLE	IO_EXPANDER-P24		OUTPUT	HIGH	HIGH		VCC_3V3_SYS

2.2.6.14 Power

2.2.6.14.1 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a dual PD controller (manufacturer part number: TPS65988). The TPS65988is a stand-alone USB Type-C and power delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17 and PP_EXT2 of the PD controller along with a resistor option to also enable using USB0 DRVVBUS from AM62A SOC. TPS65988 PD controller can provide an output of 3A (15V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is supplied to on board buck-boost and buck regulators to generate fixed 5V and 3.3V supply for the SKEVM board.

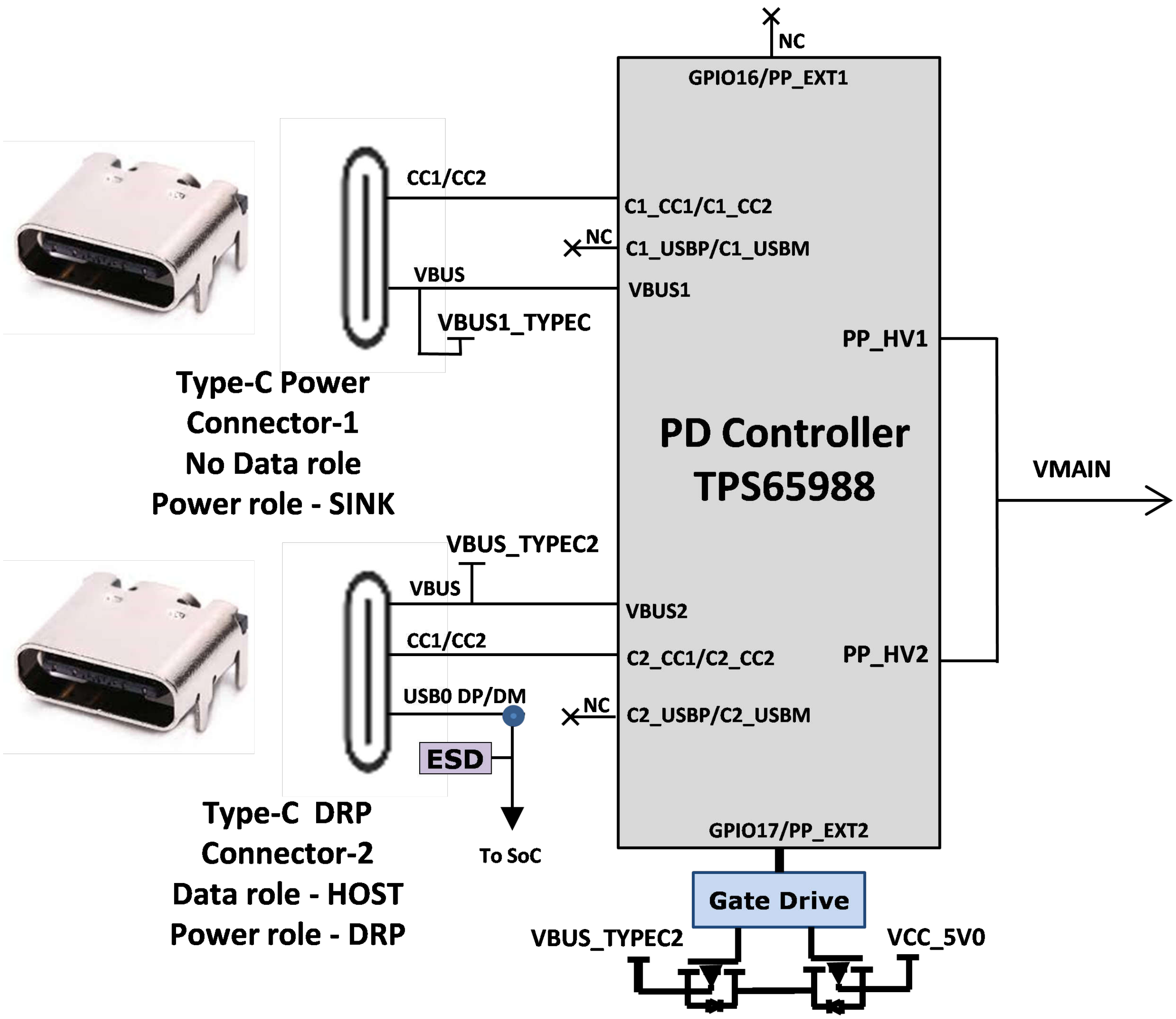

Figure 2-30. Power Input Block Diagram

2.2.6.14.2 Power Supply

AM62A Low Power SK EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SOC and other components on the board with the necessary voltage and the power required.

Figure 2-31 shows the various discrete regulators, PMIC and LDOs used to generate power rails and the current consumption of each peripheral on AM62A Low Power SK EVM board.

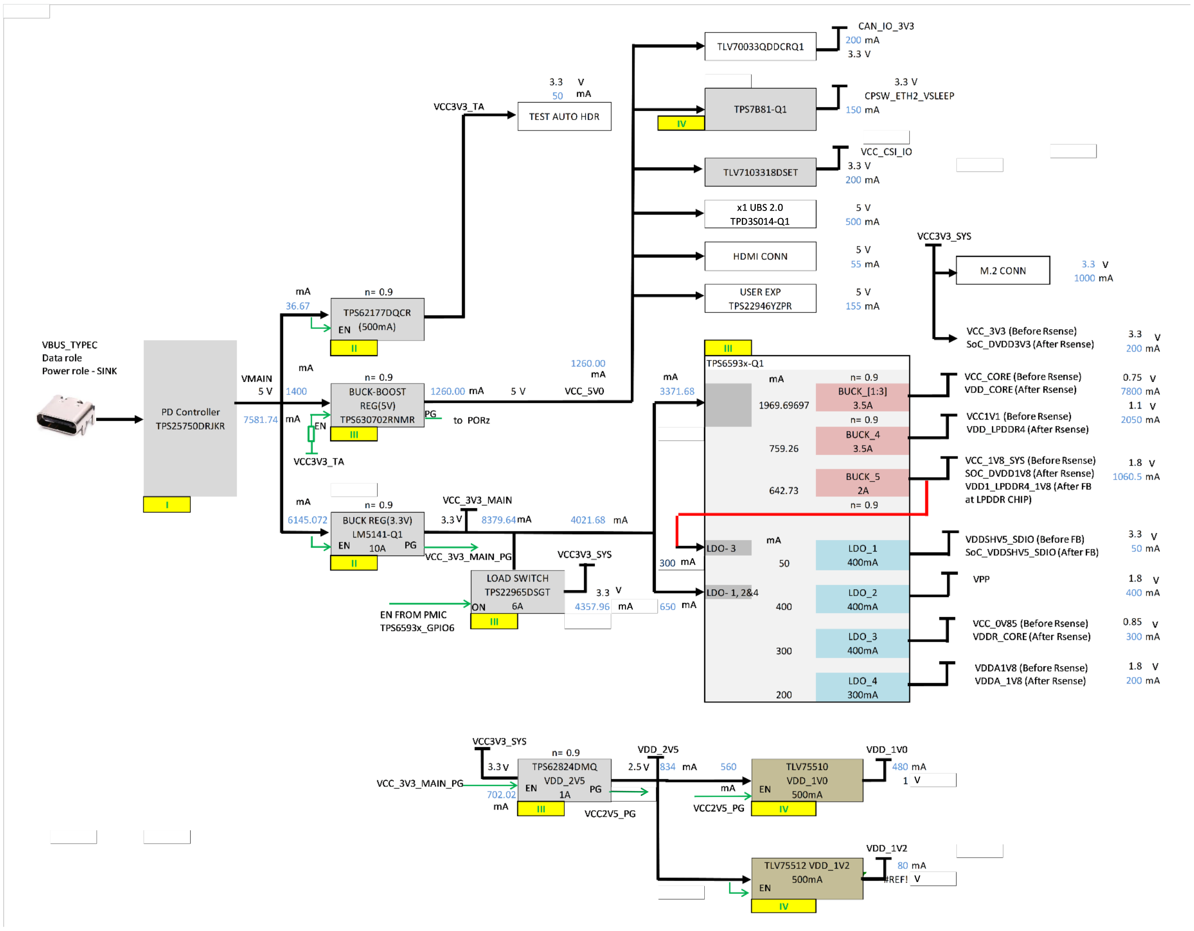

Figure 2-31. Power Architecture

The following sections describe the power distribution network topology that supplies the SKEVM board, supporting components and reference voltages.

The AM62A Low Power SK EVM board includes a power device based on combination of PMIC and discrete power supply components. The initial stage of the power supply is the VBUS voltage from either of the two USB Type-C connectors J13 and J15. USB Type-C Dual PD controller of TPS65988DHRSHR is used for negotiation of the required power to the system.

Buck-Boost controller TPS630702RNMR and buck converter LM5141-Q1 are used for the generation of 5V and 3.3V respectively and the input to the regulators is the PD output. These 3.3V and 5V are the primary voltages for the AM62A Low Power SK EVM Board power resources. The 3.3V supply generated from the Buck regulator LM5141-Q1 is the input supply to the PMIC, various SOC regulators and LDOs. The 5V supply generated from the buck boost regulator TPS630702RNMR is used for powering the onboard peripherals. The discrete regulators and LDOs used on the board are:

- TPS62824DMQR – To generate VDD_2V5 rail for PHY and DDR peripherals
- TLV75510PDQNR – To generate VDD_1V0 for Ethernet PHYs
- TLV75512PDQNR – To generate VDD_1V2 for HDMI Framer
- TPS65931-Q1 (PMIC) – To generate various SoC and Peripheral supplies
- TPS62177 Regulator – Powering the always on circuits of Test Automation Section

- TLV705075YFPT LDO – VDD_CANUART power of SoC
- TPS79601LDO – XDS110 On board emulator
- TPS73533LDO - FT4232 UART to USB Bridge
- TLV7103318DSET LDO – CSI IO supply for MIPI camera boards

Additionally, GPIO from the test automation header is connected to the nPWRON and ENABLE pin of PMIC to turn the SKEVM on and off using the test automation board. GPIO only disables the VCC_5V0 output of TPS630702RNMR from which several other power supplies are derived.

2.2.6.14.3 AM62A SoC Power

The core voltage of the AM62A SOC can be 0.75V or 0.85V based on the PMIC Configuration and on the power optimization requirement. By default, the PMIC is configured to supply VDD_CORE to 0.75V. Change the core voltage to 0.85V by changing the PMIC configuration register. Current monitors are provided on all the SOC Power rails.

The SOC has different IO groups. Each IO group is powered by specific power supplies as listed in Table 2-15.

Table 2-15. Soc Power Supply

Sl.No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB	USB	0.75 or 0.85
		VDDA_CORE_CSI	CSI	
		VDD_CANUART	CANUART	
		VDD_CORE	CORE	
2	VDDR_CORE	VDDR_CORE	CORE	0.85
3	VDDA_1V8	VDDA_1V8_CSIRX	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU	MCU GENERAL	
		VDDA_1V8_OSCO	OSCO	
		VDDA_PLL[0:4]		
4	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		
5	CAN_IO_3V3	VDDSHV_CANUART	CANUART	3.3
6	VPP_1V8	VPP_1V8		1.8
7	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3/ 1.8
8	SOC_DVDD1V8	VDDSHV1	OSPI	1.8
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
9	SOC_DVDD3V3	VDDSHV0	GENERAL	3.3
		VDDSHV2	RGMII	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU GENERAL	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.2.6.14.4 Current Monitoring

INA231 power monitor devices are used to monitor current and voltage of various power rails of AM62A Low Power processor.The INA231 interfaces to the AM62A Low Power through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-16. INA I2C Device Addresses

Source	Supply net	Device Address	Value of the Shunt Connected to the Supply Rail	Sense Resistor
VCC_CORE	VDD_CORE	0x40	1mΩ± 1%	R101
VCC_0V85	VDDR_CORE	0x41	10mΩ± 1%	R356
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ± 1%	R94
VCC1V8_SYS	SoC_DVDD1V8	0x45	10mΩ± 1%	R120
VDDA1V8	VDDA_1V8	0x4D	10mΩ± 1%	R132
VCC1V1	VDD_LPDDR4	0x47	1mΩ± 1%	R131

2.2.6.15 AM62A Low Power SK EVM User Setup and Configuration

2.2.6.15.1 Boot Modes

The boot mode for the SK EVM board is defined by two banks of switches SW2 and SW3 or by the I2C buffer connected to the Test automation connector. This allows for AM62A SOC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW2 and SW3) have weak pull down resistor and a strong pull up resistor as shown in Figure 2-32. Note that OFF setting provides a low logic level (‘0’) and an ON setting provide a high logic level (‘1’).

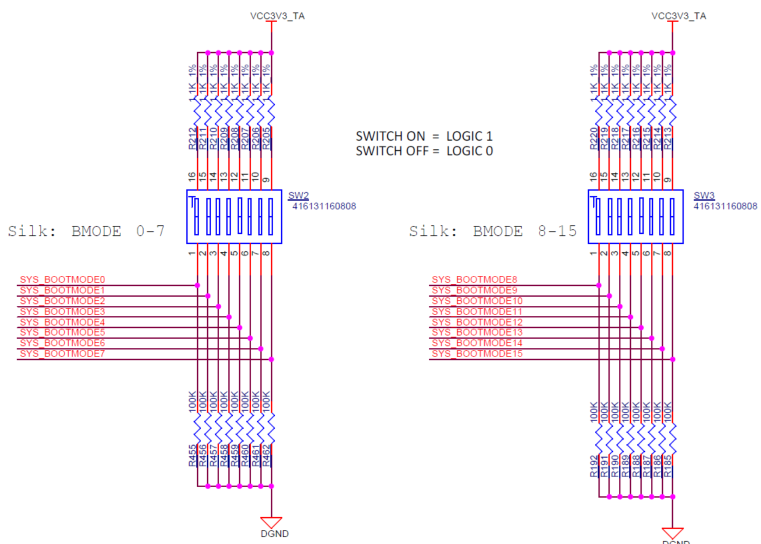

Figure 2-32. Bootmode Switches

The boot mode pins of the SOC have associated alternate functions during normal operation. Hence, isolation is provided using Buffer ICs to cater for alternate pin functionality. The output of the buffer is connected to the boot mode pins on the AM62A SOC and the output is enabled only when the boot mode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C IO Expander set by the test automation circuit. If the test automation circuit controls the boot mode, all the switches can be manually set to the OFF position. The boot mode buffer is powered by an always ON power supply to make sure that the boot mode remains present even if the SOC is power cycled.

Switch SW2 and SW3 bits [15:0] are used to set the SOC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-17. Bootmode Pin Strapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode				PLL Configuration		

Table 2-18. PLL Reference Clock Selection BOOTMODE[2:0]

SW2.3 (B2)	SW2.2 (B1)	SW2.1 (B0)	PLL REF CLK (MHz)
OFF	OFF	OFF	19.2
OFF	OFF	ON	20
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	27
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

Table 2-19. Boot Device Selection BOOTMODE[6:3]

SW2.7 (B6)	SW2.6 (B5)	SW2.5 (B4)	SW2.4 (B3)	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII
OFF	ON	OFF	ON	Ethernet RMII
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

Table 2-20. Primary Boot Mode Configuration[9:7]

SW4.2 (B9)		SW4.1 (B8)		SW3.8 (B7)		Primary Boot Mode
RVSD		Read Mode2	0: RSVD (Read mode is taken from Read Mode 1)	Read Mode1	0: OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)	Serial NAND
			1: SPI / 1-1-1 Mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)		1: OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)	
RVSD		RVSD		Csel	0: Boot Flash is on CS 0	OSPI
					1: Boot Flash is on CS 1	
RVSD		RVSD		Csel	0: Boot Flash is on CS 0	QSPI
					1: Boot Flash is on CS 1	
RVSD		Mode	0: SPI Mode 0	Csel	0: Boot Flash is on CS 0	SPI
			1: SPI Mode 3		1: Boot Flash is on CS 1	
0		0		Link stat	0: Phy scan used for speed/ duplex setup	RGMII1
					1: RGMII status register used for speed/ duplex setup	
CLKOUT	0: 50MHz clock not generated on CLKOUT0	CLK SRC	0: External clock source	0		RMII1
	1: 50MHz clock generated on CLKOUT0		1: Internal clock source			
Bus reset	0: Hung bus reset attempt after 1ms	RSVD		Addr	0: 0x50	I2C0
	1: No hung Bus reset attempted				1: 0x51	
RSVD		RSVD		RSVD		UART0
1		RSVD		Fs/Raw	0: FileSystem Mode	MMC/SD Card
					1: Raw Mode	
RSVD		RSVD		RSVD		eMMC
Core Volt	0: 0.85V Core Voltage	Mode	0: DFU (Device)	Lane Swap	0: No swapping of DP/DM	USB
	1: 0.75V Core Voltage		1: MSC (Host)		1: DP/DM is swapped	
RSVD		RSVD		RSVD		GPMC NAND
RSVD		RSVD		RSVD		GPMC NOR
RSVD		RSVD		RSVD		RSVD
SFDP	0: SFDP disabled	Read Cmd	0: 0x0B Read Command	Mode	0: 1S-1S-1S mode at 50MHz	xSPI
	1: SFDP enabled		1: 0xEE Read Command		1:8D-8D-8D mode at 25MHz	
RSVD		ARM/ Thumb	0: ARM mode	No/Dev	0: Development Boot	No-boot/Dev boot
			1: Thumb mode		1: No Boot	

Table 2-21. Backup Bootmode Selection BOOTMODE[12:10]

SW3.5 (B12)	SW3.4 (B11)	SW3.3 (B10)	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI

Table 2-21. Backup Bootmode Selection BOOTMODE[12:10] (continued)

SW3.5 (B12)	SW3.4 (B11)	SW3.3 (B10)	Backup Boot Device Selected
ON	ON	ON	I2C

Table 2-22. Backup Boot Mode Configuration BOOTMODE[13]

SW4.6 (B13)		Backup Boot Mode	Defaulted Values for Back up Boot Mode
RSVD		None	
Mode	0: DFU (Device)	USB	Core Volt bit = 0 Lane Swap bit = 0
	1: MSC (Host)		
RSVD		RSVD	
RSVD		UART	
Interface	0: RGMII with internal Delay	Ethernet	Link Stat bit = 0 (If RGMII)
	1: RGMII with external clock source		ClkOut bit= 0 and Clksrc bit = 1 (If RMII)
1		MMC	Mode bit = 0
RSVD		SPI	Csel bit = 0 Mode = 0
RSVD		I2C	Addr = 0 Bus Rest = 0

2.2.6.15.2 User Test LEDs

The AM62A Low Power SK EVM board contains two LEDs for user defined functions.

Table 2-23 indicates the user test LEDs and the associated GPIOs used to control the LEDs.

Table 2-23. User Test LEDs and the Associated GPIOs

Sl Number	LED	GPIO used	SCHNet Names
1	LD1	GPIO1_49	SOC_GPIO1_49
2	LD5	U92.24(P27)	IO_EXP_TEST_LED

2.2.6.16 Expansion Headers

The AM62A Low Power SK EVM features two expansion Headers, 40 pin User expansion connector & 28 pin MCU Header.

2.2.6.16.1 User Expansion Connector

The AM62A Low Power SK EVM supports RPi expansion interface using a 40-pin User expansion connector (manufacturing part number PEC20DAAN).Three mounting holes are oriented with the connector to allow for connection of these HAT boards.

The following interfaces and IOs are included on to the 40-pin user expansion connector:

- 2x SPI : SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B
- 1x CLK: CLKOUT0
- 10x GPIO: GPIOs from main domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5V and 3.3V are current limited to 155mA and 500mA, respectively. Use two individual load switch (TPS22902YFPR and TPS22946YZPR) to limit the power supply. Enable for the load switches are controllable by an I2C based GPIO Port expander.

Table 2-24 lists the signals routed from user expansion connectors.

Table 2-24. 40 Pin Power Connector Pinout

Pin Number	SoC Ball	Net Name
1	-	VCC3V3_EXP
2	-	VCC5V0_EXP
3	M20	EXP_I2C2_SDA
4	-	VCC5V0_EXP
5	M22	EXP_I2C2_SCL
6	-	DGND
7	B16	EXP_CLKOUT0
8	C18	EXP_UART5_TXD
9	-	DGND
10	B17	EXP_UART5_RXD
11	A19	EXP_SPI2_CS1
12	A21	EXP_SPI2_CLK
13	M21	EXP_GPIO0_42
14	-	DGND
15	F14	EXP_GPIO1_22
16	R17	EXP_GPIO0_38
17	-	VCC3V3_EXP
18	K17	EXP_GPIO0_39
19	B15	EXP_SPI0_D0
20	-	DGND
21	E15	EXP_SPI0_D1
22	G20	EXP_GPIO0_14
23	A17	EXP_SPI0_CLK
24	D16	EXP_SPI0_CS0
25	-	DGND
26	C16	EXP_SPI0_CS1
27	E16	SoC_I2C0_SDA
28	D17	SoC_I2C0_SCL
29	M18	EXP_GPIO0_36
30	L18	EXP_GPIO0_32
31	L17	EXP_GPIO0_33
32	K18	EXP_GPIO0_40/ PR0_ECAP0_IN_APWM_OUT
33	B20	EXP_EHRPWM1_B
34	-	DGND
35	B21	EXP_SPI2_CS0 and EHRPWM0_A
36	B18	EXP_SPI2_CS2
37	M19	EXP_GPIO0_41
38	B19	EXP_SPI2_D1/ECAP2_IN_APWM_OUT
39	-	EXP_HAT_DETECT
40	C19	EXP_SPI2_D0

2.2.6.16.2 MCU Connector

AM62A Low Power SK EVM has a 14 × 2 standard 0.1” spaced MCU connector which includes signals connected to the MCU Domain of the SOC. The connected signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals. Additional control signals connected on the Header includes CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO supply and GND. MCU_UART0 signals from AM62A SOC are connected to both MCU Header and FT4232 bridge through a MUX (manufacturing part number SN74CB3Q3257PWR). The MCU Header does not include the board ID memory interface. The allowed current limit is 100mA on 3.3V rail.

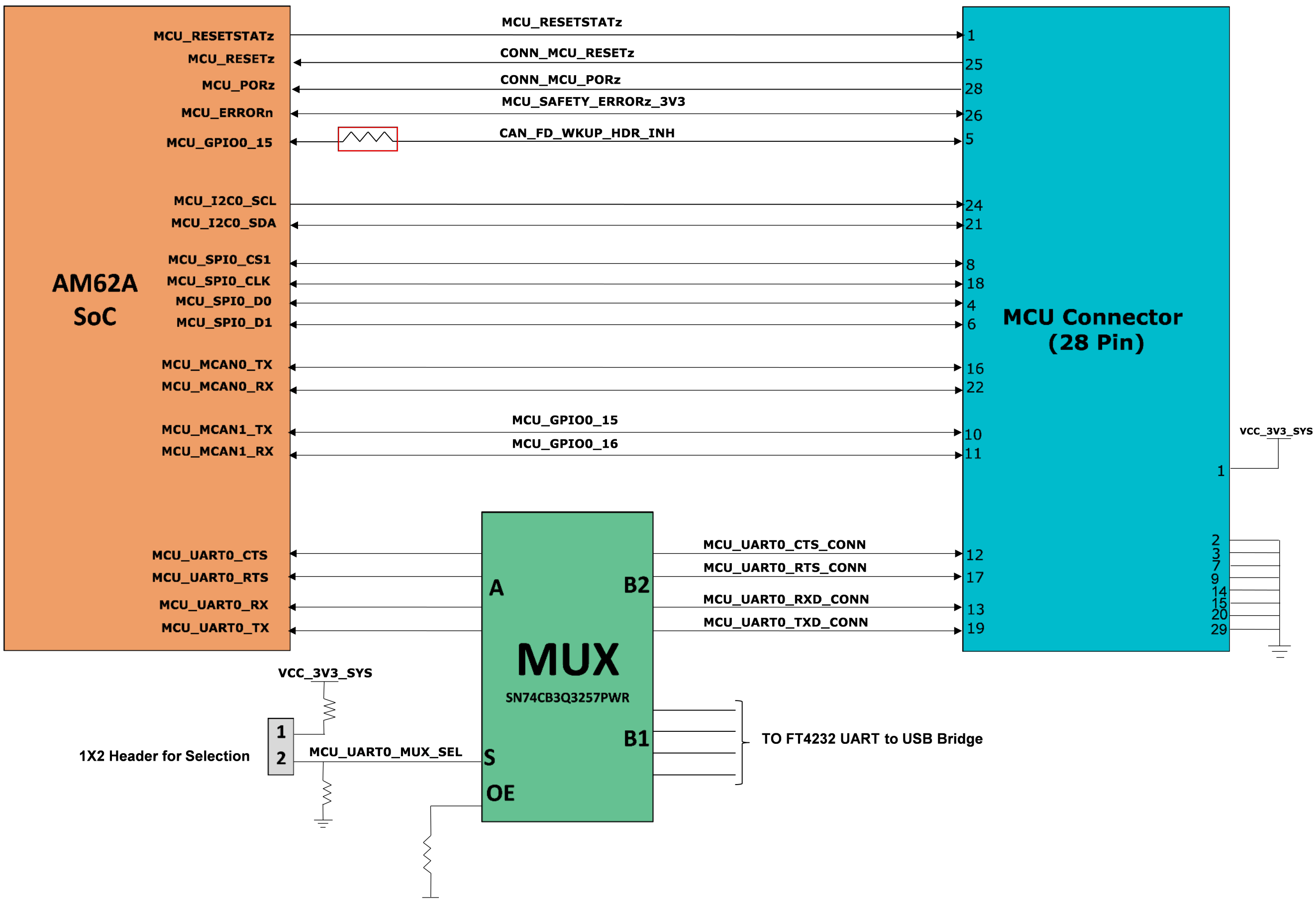

Figure 2-33. MCU Connector Interface

Table 2-25. MCU Table Connector

Pin Number	SoCBall Number	Netname
1	-	VCC_3V3_SYS
2	-	DGND
3	-	DGND
4	B12	MCU_SPI0_D1
5	D7	CAN_FD_WKUP_HDR_INH
6	A15	MCU_SPI0_D0
7	-	DGND
8	C11	MCU_SPI0_CS1
9	-	DGND
10	D7	MCU_GPIO0_15
11	B9	MCU_GPIO0_16
12	B11	MCU_UART0_CTS_CONN

Table 2-25. MCU Table Connector (continued)

Pin Number	SoCBall Number	Netname
13	D8	MCU_UART0_RXD_CONN
14	-	DGND
15	-	DGND
16	C7	MCU_MCAN0_TX
17	D10	MCU_UART0_RTS_CONN
18	B13	MCU_SPI0_CLK
19	F8	MCU_UART0_TXD_CONN
20	-	DGND
21	D9	MCU_I2C0_SDA
22	E8	MCU_MCAN0_RX
23	D14	MCU_RESETSTATz
24	E12	MCU_I2C0_SCL
25	C12	CONN_MCU_RESETz
26	B8	MCU_SAFETY_ERRORz_3V3
27	-	DGND
28	A7	CONN_MCU_PORz

2.2.6.17 I2C Address Mapping

There are four I2C interfaces used in SK EVM board:

- SoC_I2C0 Interface: SoC I2C[0] is connected to Board ID EEPROM, User Expansion Connector Header, USB PD controller and PMIC
- SOCI2C1 Interface: SoC I2C[1] is connected to Test Automation Header, Current Monitors (x6), Temperature Sensors (x2), Audio Codec, HDMI Transmitter and GPIO Port Expander (x2).
- SOCI2C2 Interface: SoC I2C[2] is connected to the User Expansion Connector Header and both the CSI Camera connectors (Flex and MIPI).
- MCUI2C0 Interface: MCU I2C[0] is connected to the MCU Header and PMIC.

Figure 2-34 depicts the I2C tree, and Table 2-26 provides the complete I2C address mapping details present on the AM62A Low Power SK EVM.

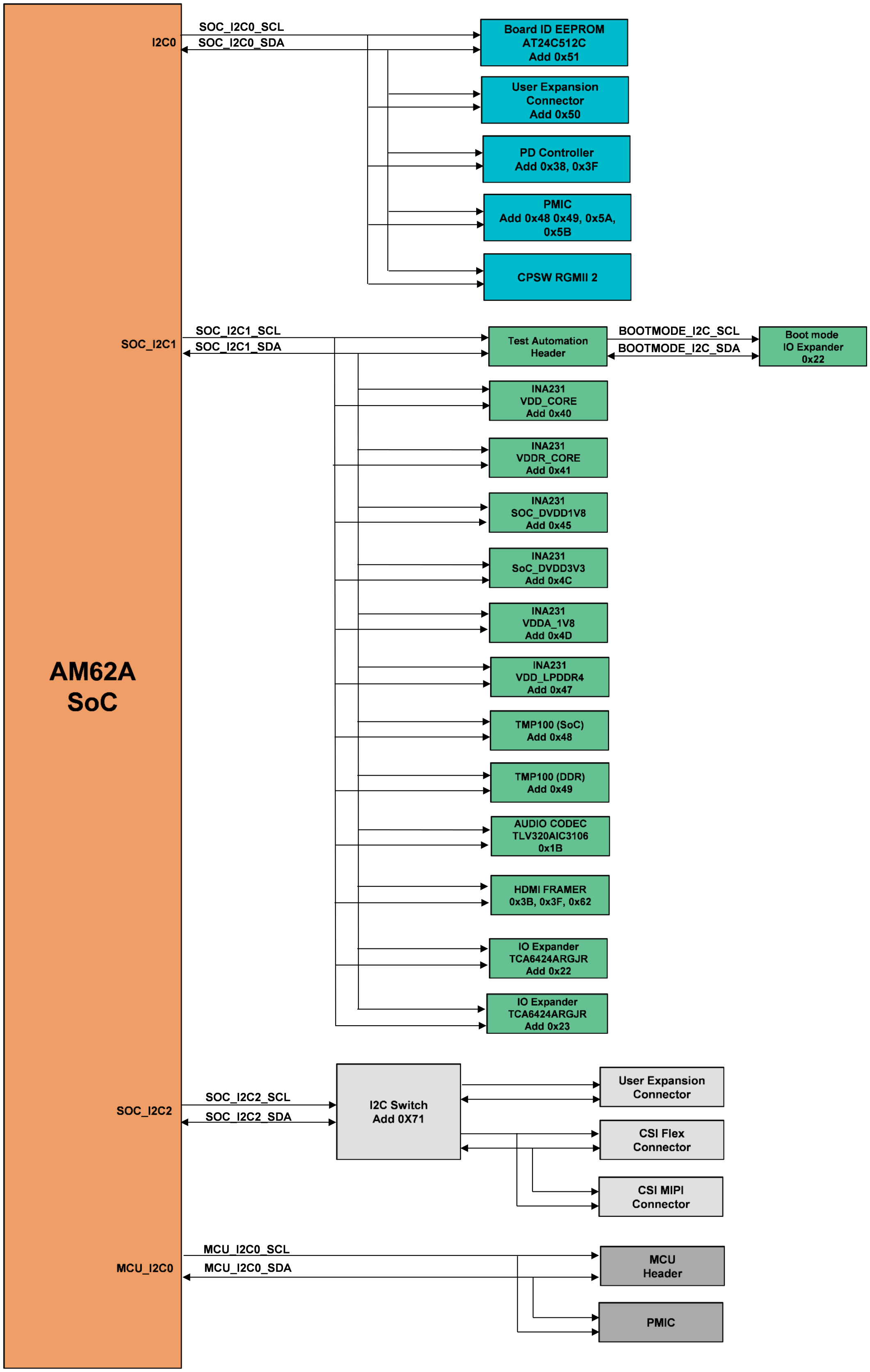

Figure 2-34. AM62A LP SK EVM I2C Tree - Rev E1 and E2

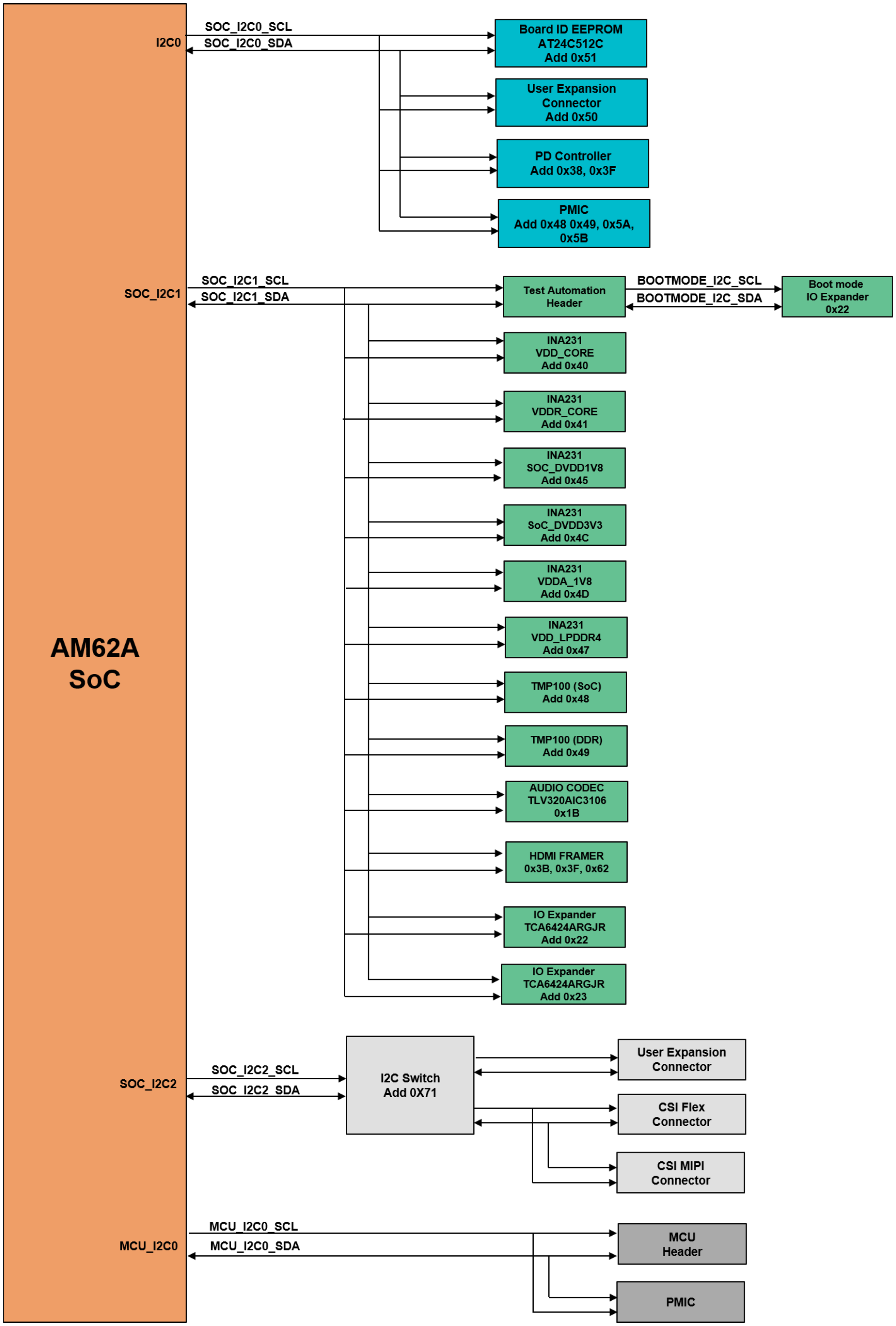

Figure 2-35. AM62A LP SK EVM I2C Tree - Rev E3 and A

Table 2-26. I2C Mapping Table

I2C Port	Device/Function	Part Number	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PMIC	TPS65931-Q1	0x48, 0x49, 0x5A, 0x5B
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x41, 0x4C, 0x45, 0x4D & 0x47
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48, 0x49
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
SoC_I2C2	CSI MIPI Connector	<connector interface>	
	CSI Flex Connector		
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	PMIC	TPS65931-Q1	
MCU_I2C0	MCU Header	<connector interface>	
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

3 Hardware Design Files

3.1 Schematics, PCB Layout and BOM

- Design files Engineering Revision E1, E2, E3: https://www.ti.com/lit/zip/SPRR459
- Design files for AMB package: https://www.ti.com/lit/zip/SPRR491
- Design files for ANF package: https://www.ti.com/lit/zip/SPRCAM0

4 Additional Information

4.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Issue Number	Issue Title	Issue Description	Variants Affected
1	eMMC operation	eMMC does not function in 4 bit mode	E1
2	Test Automation	Test automation does not work	E1
3	WiFi Enable	WiFi module with 3.3V enable does not work	E1
4	Ethernet (RGMII2) modular connector	Ethernet (RGMII2) modular connector is descoped	E1, E2
5	Low power mode	Low power modes sometimes do not work as expected	E1, E2
6	LPDDR4 part number	LPDDR4 part number is not correct in schematics and BOM	E1, E2
7	Test Automation	Test automation through XDS110 sometimes does not work	E2
8	Wake-up Through MCU and WKUP UART Not Functioning	Wake-up functionality does not operate correctly when triggered through the FT4232 chip to the MCU UART and WAKEUP UART interfaces	E1, E2, E3, A

4.1.1 Issue 8 – Wake-up Through MCU and WKUP UART Not Functioning

Applicable EVM Revisions: E1, E2, E3, A

Issue Description: Wake-up functionality does not operate correctly when triggered through the FT4232 chip to the MCU UART and WAKEUP UART interfaces.

Workaround: To resolve this issue, perform the following hardware modifications, cut the trace between U110 pin 3 and U118 pin 3 connected to VCC_3V3_SYS, Remove C467, C490, R516, R541 and resolder these components rotated 90 degrees from the original orientation (for the correct placement, see Figure 4-1). Then solder a wire from U110.3 to the following connection points C467.2, R516.2, R523.1 and from U118.3 to the following connection points C490.2, R541.2, R535.1. Additionally, solder a wire from R140.2 to C103.2 on the PCB as shown in Figure 4-2. Lift the U33.16 pin and solder a wire from Lifted Pin16 to C103.2 other side pin as per Figure 4-2. For visual guidance on component locations and wire routing, see Figure 4-1 and Figure 4-2

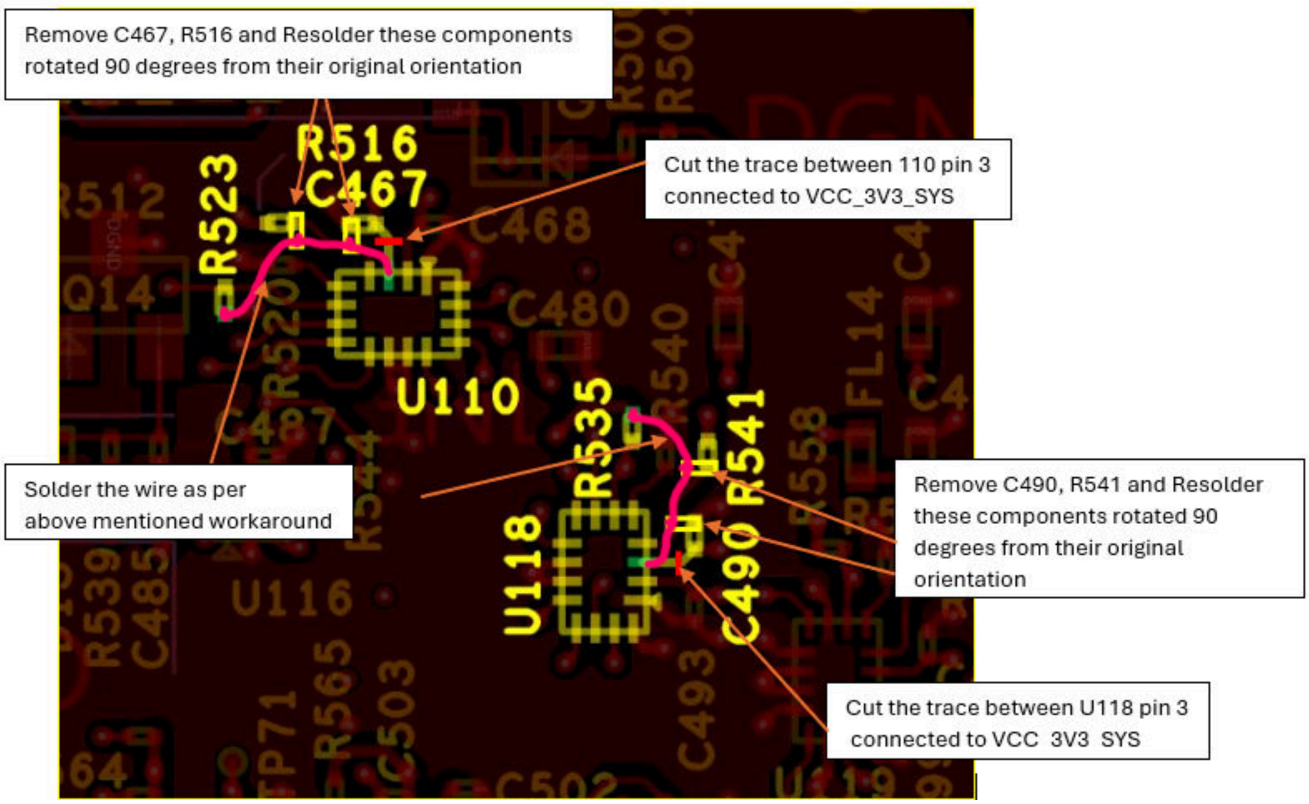

Figure 4-1. SK-AM62A-LP PCBA Bottom Side

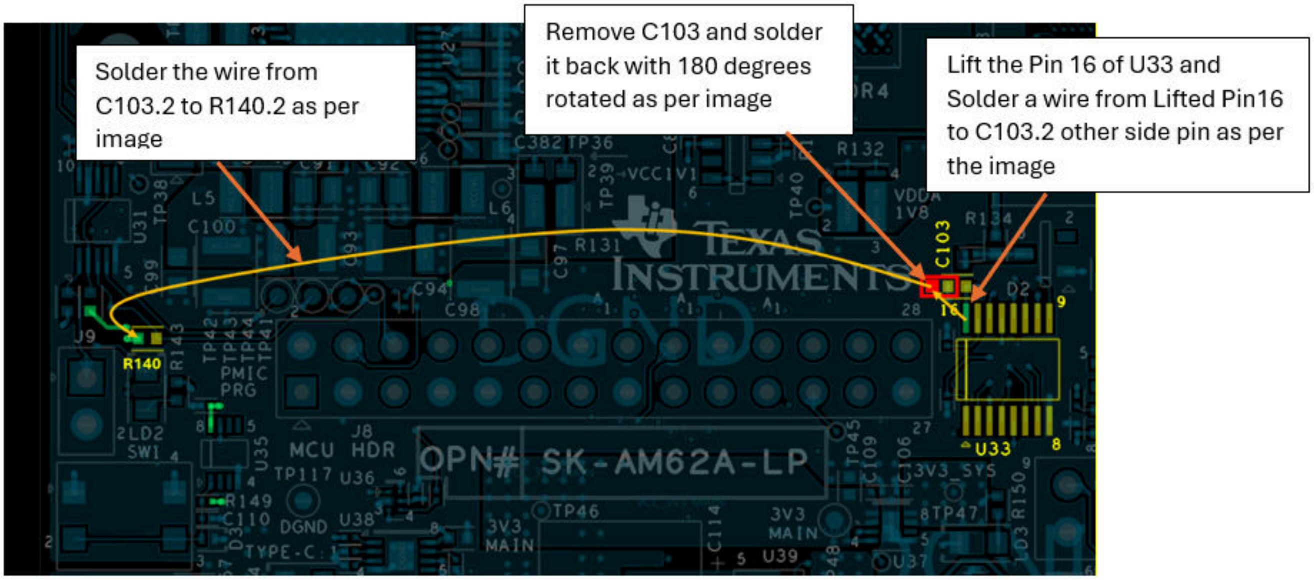

Figure 4-2. SK-AM62A-LP PCBA Top Side

4.2 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). Only use this product in an ESD controlled environment such as a temperature or humidity controlled environment to limit the buildup of ESD. Always use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

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5 References

1. Texas Instruments, *[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 - Custom board hardware design - Design and Review notes for Reuse of SK-AM62A-LP Schematics* forums post
2. Texas Instruments, *[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit* forums post
3. Texas Instruments, *[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 and AM62D-Q1 Design Recommendations / Custom board hardware design - Custom board schematics self-review* forums post
4. Texas Instruments, *[FAQ] AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1 - Collaterals for reference during different phases of custom board design, self-review and bring-up* forums post
5. Texas Instruments, *[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families* forums post

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 29, 2026 to September 30, 2026 (from Revision C (July 2026) to Revision D (September 2026)) **Page**

- Add RevB revision details in Section 2.1..4