Errata

AM62Lx Sitara™ Processors Silicon Errata, Silicon Revision 1.0, 1.1

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

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1 Usage Notes and Advisories Matrices

Table 1-1 lists all usage notes and the applicable silicon revision(s). Table 1-2 lists all advisories, modules affected, and the applicable silicon revision(s).

Table 1-1. Usage Notes Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED	
		AM62Lx 1.0	AM62Lx 1.1
DDR	i2330 DDRSS Register Configuration Tool Updates	YES	YES
OSPI	i2351 OSPI: Direct Access Controller (DAC) does not support Continuous Read mode with NAND Flash	YES	YES

Table 1-2. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED	
		AM62Lx 1.0	AM62Lx 1.1
BCDMA	i2431 BCDMA: RX Channel can lockup in certain scenarios	YES	YES
Boot	i2435 Boot: ROM timeout for eMMC boot too long	YES	NO
Boot	i2462 Boot: ROM xSPI-SFDP boot mode fails	YES	YES
Boot	i2463 Boot: Possible boot failure with SD cards	YES	NO
Boot	i2464 Boot: ROM is unable to boot from SD cards with incorrect formatting	YES	YES
Boot	i2465 Boot: EMMC boot mode is slower than expected	YES	NO
Boot	i2466 Boot: ROM boot fails for large file sizes	YES	YES
Boot	i2467 Boot: ROM UART boot fails with large image	YES	NO
Boot	i2469 Boot: ROM NOBOOT boot mode is not functional	YES	YES
Boot	i2470 Boot: USB-DFU primary boot mode fails to transition to backup boot mode	YES	NO
Boot	i2471 Boot: Certain primary/backup boot mode combinations fail	YES	NO
Boot	i2473 Boot: eMMC boot may fail	YES	NO
Boot	i2474 Boot: Certain second stage binaries fail for block based boot modes	YES	NO
Boot	i2481 Boot: eMMC alternate boot fails if partition is not reprogrammed every time	YES	NO
Boot	i2482 Boot: ROM does not provide enough clocks during SD card initialization	YES	NO
Boot	i2484 Boot: ROM fails to parse X509 certificates using GENERALIZED time format	YES	NO
CPSW	i2208 CPSW: ALE IET Express Packet Drops	YES	YES
CPSW	i2401 CPSW: Host Timestamps Cause CPSW Port to Lock up	YES	YES
DDR	i2160 DDR: Valid VRef Range Must be Defined During LPDDR4 Command Bus Training	YES	YES
Debug	i2461 Debug: Wait-In-Reset (WIR) mode is not functional	YES	NO
LPM	i2487 LPM: Low power modes may inadvertently corrupt DDR contents	YES	NO
MCAN	i2278 MCAN: Message Transmit order is not ensured from dedicated Tx Buffers configured with same Message ID	YES	YES
MCAN	i2279 MCAN: Specification Update for dedicated Tx Buffers and Tx Queues configured with same Message ID	YES	YES
MMCHS	i2312 MMCSD: HS200 and SDR104 Command Timeout Window Too Small	YES	YES
MMCHS	i2493 MMCSD: HS200 write failures	YES	YES
OSPI	i2189 OSPI: Controller PHY Tuning Algorithm	YES	YES
OSPI	i2249 OSPI: Internal PHY Loopback and Internal Pad Loopback clocking modes with DDR timing inoperable	YES	YES
OSPI	i2383 OSPI: 2-byte address is not supported in PHY DDR mode	YES	YES
PRG	i2253 PRG: CTRL_MMR STAT registers are unreliable indicators of POK threshold failure	YES	YES
USART	i2310 USART: Erroneous clear/trigger of timeout interrupt	YES	YES
USART	i2311 USART Spurious DMA Interrupts	YES	YES
USB	i2409 USB: USB2 PHY locks up due to short suspend	YES	YES

1.1 Devices Supported

This document supports the following devices:

- AM62Lx

Reference documents for the supported devices are:

- AM62Lx Processors Technical Reference Manual (SPRUJB4)
- AM62Lx Processors Data Sheet (SPRSPA1)

2 Silicon Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

2.1 Silicon Usage Notes

i2330 *DDRSS Register Configuration Tool Updates*

Details:

The DDR Register Configuration Tool provides custom register settings based on system level details such as the architecture (density, data width, ranks) of the DDR device, frequency of operation, and IO settings determined through board simulations. This tool may be updated over time to support new devices and/or features, fix issues identified with the tool, and most importantly, capture work-arounds of errata or recent updates identified to register calculations which improve performance, signal integrity, or timing relationships between signals.

Workaround(s):

In order to ensure that parameters are set appropriately based on lessons learned and reduce the risk of functional failure, the latest DDR register configuration tool should always be used to generate register values. As the DDR register configuration tool can periodically be updated, the revision history of the tool should be reviewed and evaluated whether tool changes apply to existing systems. When applicable, the configuration of an existing system should be updated appropriately. The latest version of the tool can be found at http://dev.ti.com/sysconfig, and choosing DDR Configuration under Software Product drop down for the applicable device that is being used.

i2351 *OSPI: Direct Access Controller (DAC) does not support Continuous Read mode with NAND Flash*

Details:

The OSPI Direct Access Controller (DAC) doesn’t support Continuous Read mode with NAND Flash since the OSPI controller can deassert the CSn signal (by design intent) to the Flash memory between internal DMA bus requests to the OSPI controller.

The issue occurs because “Continuous Read” mode offered by some OSPI/QSPI NAND Flash memories requires the Chip Select input to remain asserted for an entire burst transaction.

The SoC internal DMA controllers and other initiators are limited to 1023 B or smaller transactions, and arbitration/queuing can happen both inside of the various DMA controllers or in the interconnect between any DMA controller and the OSPI peripheral. This results in delays in bus requests to the OSPI controller that result in the external CSn signal being deasserted.

NOR Flash memories are not affected by CSn de-assertion and Continuous Read mode works as expected.

Workaround(s):

Software can use page/buffered read modes to access NAND flash.

2.2 Silicon Advisories

i2189 *OSPI: Controller PHY Tuning Algorithm*

Details:

The OSPI controller uses a DQS signal to sample data when the PHY Module is enabled. However, there is an issue in the module which requires that this sample must occur within a window defined by the internal clock. Read operations are subject to external delays, which change with temperature. To ensure valid reads at any temperature, a special tuning algorithm must be implemented which selects the most robust TX, RX, and Read Delay values.

Workaround(s):

The workaround for this bug is described in detail in SPRACT2. To sample data under some PVT conditions, users are required to increment the Read Delay field to shift the internal clock sampling window. This allows sampling of the data anywhere within the data eye. However, this has these side effects:

1. PHY Pipeline mode must be enabled for all read operations. Because PHY Pipeline mode must be disabled for writes, reads and writes must be handled separately.
2. Hardware polling of the busy bit is broken when the workaround is in place, so SW polling must be used instead. Writes must occur through DMA accesses, within page boundaries, to prevent interruption from either the host or the flash device. Software must poll the busy bit between page writes. Alternatively, writes can be performed in non-PHY mode with hardware polling enabled.
3. STIG reads must be padded with extra bytes, and the received data must be right-shifted.

i2208 *CPSW: ALE IET Express Packet Drops*

Details:

This issue impacts the following Module:

The issue with ALE is due to CPSW frequency and IET operation with short express traffic and pre-empted packets that get pre-empted between 60-69 bytes on non-10G capable ports.

If an IET pre-emptible packet get interrupted at 60-69 bytes, the lookup will occur when the next chunk arrives. The CPSW only gives the ALE 64 bytes from the pre-emptible MAC.

As a result, a short express traffic lookup will start at the end of a 64 byte express traffic, but when the pre-empted queue continues, the pre-empted traffic will complete the 64 bytes and attempt a lookup for the pre-empt packet. But this lookup is less that 64 clocks from the express lookup start, so the express lookup will be aborted(express traffic dropped) and start the new lookup for the pre-empted traffic.

Rules to induce the issue:

1. You are in IET (Interspersed Express Traffic) mode on ports not capable of 5/10G operation
2. Remote express packets can be preempt packets as low as 60 bytes
3. Pre-empt packet traffic that is 128 bytes or more.
4. Express traffic that interrupts the pre-empt traffic between 60-69 bytes.
5. A short express traffic immediately followed by the continuation of the pre-empt traffic.
    a. Gap between express frame and pre-empt frame be its minimum.

i2208 (continued) *CPSW: ALE IET Express Packet Drops*

6. The CPSW frequency is at its lowest capability for the speeds required.

Workaround(s):

During IET negotiation, tell the remote to fragment at 128 bytes.

i2249 *OSPI: Internal PHY Loopback and Internal Pad Loopback clocking modes with DDR timing inoperable*

Details

The OSPI Internal PHY Loopback mode and Internal Pad Loopback mode uses “launch edge as capture edge” (same edge capture, or 0-cycle timing).

The programmable receive delay line (Rx PDL) is used to compensate for the round trip delay (Tx clock to Flash device, Flash clock to output and Flash data to Controller).

In the case of internal and IO loopback modes, the total delay of the Rx PDL is not sufficient to compensate for the round trip delay, and thus these modes cannot be used.

The table below describes the recommended clocking topologies in the OSPI controller. All other modes not described here are affected by the advisory in DDR mode and are not recommended clocking topologies.

Table 2-1. OSPI Clocking Topologies

Clocking Mode Terminology	CONFIG_REG.PHY_MODE_ENABLE	READ_DATA_CAPTURE.BYPASS	READ_DATA_CAPTURE.DQS_EN	Board implementation
No Loopback, no PHY	0 (PHY disabled)	1 (disable adapted loopback clock)	X	None. Relying on internal clock. Max freq 50MHz.
External Board Loopback with PHY	1 (PHY enabled)	0 (enable adapted loopback clock)	0 (DQS disabled)	External Board Loopback (OSPI_LOOPBACK_CLK_SEL = 0)
DQS with PHY	1 (PHY enabled)	X (DQS enable has priority)	1 (DQS enabled)	Memory strobe connected to SOC DQS pin

Workaround

None. Please use one of the unaffected clocking modes based on the table in the description

i2253 *PRG: CTRL_MMR STAT registers are unreliable indicators of POK threshold failure*

Details

The POK overvoltage and undervoltage flags in the CTRL_MMR PRG STAT registers are unreliable indicators of whether the POK has seen a failure. As a result, they are being marked as Reserved in the device Technical Reference Manual (TRM).

Workaround

The filtered POK output updates ESM flags.

Upon POK initialization (i.e. enable), the ESM flags should be cleared (due to comparisons carried out during the bandgap and / or the POK settling time). After this initial clear, the ESM flags can be used as a reliable indicator of failure (or no failure) from the POKs.

i2278 *MCAN: Message Transmit order is not ensured from dedicated Tx Buffers configured with same Message ID*

Details

The erratum is limited to the case when multiple Tx Buffers are configured with the same Message ID (TXBC.NDTB > 1).

Under the following conditions, a message may be transmitted out of order:

- Multiple Tx Buffers configured with the same Message ID
- Tx requests for these Tx Buffers are submitted sequentially with delays between each

Workaround

Workaround #1:

After writing the Tx messages with same Message ID to the Message RAM, request transmission of all these message concurrently by single write access to TXBAR. Make sure none of these messages have a pending Tx request before making the concurrent request.

Workaround #2:

Use the Tx FIFO instead of dedicated Tx Buffers (set bit MCAN_TXBC[30] TFQM = 0 to use Tx FIFO) for the transmission of several messages with the same Message ID in a specific order.

i2279 *MCAN: Specification Update for dedicated Tx Buffers and Tx Queues configured with same Message ID*

Details

The erratum updates the descriptions in Section 3.5.2 Dedicated Tx Buffers and 3.5.4 Tx Queue of the M_CAN User’s Manual related to message transmission from multiple dedicated Tx Buffers configured with the same Message ID.

Workaround

Workaround #1:

After writing the Tx messages with same Message ID to the Message RAM, request transmission of all these message concurrently by single write access to TXBAR. Make sure none of these messages have a pending Tx request before making the concurrent request.

Workaround #2:

Use the Tx FIFO instead of dedicated Tx Buffers (set bit MCAN_TXBC[30] TFQM = 0 to use Tx FIFO) for the transmission of several messages with the same Message ID in a specific order.

i2310 *USART: Erroneous clear/trigger of timeout interrupt*

Details:

The USART may erroneously clear or trigger the timeout interrupt when RHR/MSR/LSR registers are read.

Workaround(s):

For CPU use-case.

- If the timeout interrupt is erroneously cleared:
  - This is Valid since the pending data inside the FIFO retriggers the timeout interrupt

i2310 (continued) ***USART: Erroneous clear/trigger of timeout interrupt***

- If timeout interrupt is erroneously set, and the FIFO is empty, use the following SW workaround to clear the interrupt:
  - Set a high value of timeout counter in TIMEOUTH and TIMEOUTL registers
  - Set EFR2 bit 6 to 1 to change timeout mode to periodic
  - Read the IIR register to clear the interrupt
  - Set EFR2 bit 6 back to 0 to change timeout mode back to the original mode

For DMA use-case.

- If timeout interrupt is erroneously cleared:
  - This is valid since the next periodic event retriggers the timeout interrupt
  - User must ensure that RX timeout behavior is in periodic mode by setting EFR2 bit6 to 1
- If timeout interrupt is erroneously set:
  - This causes DMA to be torn down by the SW driver
  - Valid since next incoming data causes SW to setup DMA again

i2311 *USART Spurious DMA Interrupts*

Details:

Spurious DMA interrupts may occur when DMA is used to access TX/RX FIFO with a non-power-of-2 trigger level in the TLR register.

Workaround(s):

Use power of 2 values for TX/RX FIFO trigger levels (1, 2, 4, 8, 16, and 32).

i2312 *MMCSD: HS200 and SDR104 Command Timeout Window Too Small*

Details:

Under high speed HS200 and SDR104 modes, the functional clock for MMC modules will reach up to 192 MHz. At this frequency, the maximum obtainable timeout through of MMC host controller using MMCSD_SYSCTL[19:16] DTO = 0xE is (1/192MHz)*2^27 = 700ms. Commands taking longer than 700ms may be affected by this small window frame.

Workaround(s):

If the command requires a timeout longer than 700ms, then the MMC host controller command timeout can be disabled (MMCSD_CON[6] MIT=0x1) and a software implementation may be used in its place. Detailed steps as follows (in Linux):

1. During MMC host controller probe function (omap_hsmmc.c:omap_hsmmc_probe()), inform processor that the host controller is incapable of supporting all the necessary timeouts.

2. Modify the MMC core software layer functionality so the core times out on its own when the underlying MMC host controller is unable to support the required timeout.

i2493 *MMCSD: HS200 write failures*

Details:

The MMC0 interface has the potential for write failures when issuing multiple block writes operating in HS200 mode with excessive IO supply noise.

i2493 (continued) ***MMCSD: HS200 write failures***

To minimize IO supply noise follow below best practices and refer to the linked application note:

- Use wide power planes/pours adjacent to ground layers with a thin dielectric between them.
- Place power planes/pours and adjacent ground planes as close to the surface of the powered components as possible.
- Use a wide variety of decoupling capacitor values and place low ESL capacitors as close to the decoupled device as possible.
- Use one decoupling capacitor per power pin.
- Use short and wide traces to decoupling capacitors and power/ground vias.
- Sitara™ Processor Power Distribution Networks: Implementation and Analysis

Workaround(s):

Implement a software recovery mechanism that re-issues the failed multiple block write with minimum 5μs delay between blocks to reduce noise. One way to achieve this delay is using single block writes for the failed multiple block write.

i2383 *OSPI: 2-byte address is not supported in PHY DDR mode*

Details:

When the OSPI controller is configured for 2-byte addressing in PHY DDR Mode, an internal state machine mis-compares the number of address bytes transmitted to a value of 1 (instead of 2). This results in a state machine lockup in the address phase, rendering PHY DDR mode non-operable.

This issue does not occur when using any Tap mode or PHY SDR mode. This issue also doesn't occur when using 4 byte addressing in PHY DDR mode.

Workaround(s):

For compatible OSPI memories that have programmable address byte settings, set the amount of address bytes required from 2 to 4 on the flash. This may involve sending a specific command to change address bytes and/or writing a configuration register on the flash. Once done, update the amount of address bytes sent in the controller settings from 2 to 4.

For compatible OSPI memories that only support 2-byte addressing and cannot be re-programmed, PHY DDR mode will not be compatible with that memory. Alternative modes include:

- PHY SDR mode
- TAP (no-PHY) DDR mode
- TAP (no-PHY) SDR mode

i2401 *CPSW: Host Timestamps Cause CPSW Port to Lock up*

Details:

The CPSW offers two mechanisms for communicating packet ingress timestamp information to the host.

The first mechanism is via the CPTS Event FIFO which records timestamps when triggered by certain events. One such event is the reception of an Ethernet packet with a specified EtherType field. Most commonly this is used to capture ingress timestamps for PTP packets. With this mechanism the host must read the timestamp (from the CPTS FIFO) separately from the packet payload which is delivered via DMA. This mode is supported and is not affected by this errata.

The second mechanism is to enable receive timestamps for all packets, not just PTP packets. With this mechanism the timestamp is delivered alongside the packet payload via DMA. This second mechanism is the subject of this errata.

When the CPTS host timestamp is enabled, every packet to the internal CPSW port FIFO requires a timestamp from the CPTS. When the packet preamble is corrupted due to EMI or any other corruption mechanism a timestamp request may not be sent to the CPTS. In this case the CPTS will not produce the timestamp which causes a lockup condition in the CPSW port FIFO. When the CPTS host timestamp is disabled by clearing the tstamp_en bit in the CPTS_CONTROL register the lockup condition is prevented from occurring.

Workaround(s):

Ethernet to host timestamps must be disabled.

CPTS Event FIFO timestamping can be used instead of CPTS host timestamps.

i2409 USB: USB2 PHY locks up due to short suspend

Details:

The USB 2.0 PHY may hang in response to a USB wake-up event that occurs within 3 microseconds of the USB controller entering suspend. This PHY hang can only be recovered via a power cycle as warm reset is ineffectual.

Workaround(s):

Note: this workaround is only applicable if USB is not the primary boot mode. If USB is the primary boot mode, no workaround is available.

In order to prevent this issue from occurring, a specific order of operations must be observed during the USB controller initialization process:

i2431 BCDMA: RX Channel can lockup in certain scenarios

Details:

BCDMA RX chan Teardown can lockup channel and cannot be used for subsequent transfers if none of the TRs have EOP flag set in configuration specific flags field. Subsequently when channel is re-enabled, transfer does not not complete and terminates with various errors in TR response.

Workaround(s):

a) When receiving data from a PSIL/PDMA peripheral, EOP flag needs to be set in the each TR's configuration specific flag field and PDMA's 1 X-Y FIFO Mode Static TR "Z" parameter should be set to non zero value for channel teardown to function properly and cleanup the internal state memory. Otherwise it leads to channel lockups on subsequent runs. The PDMA Z count should also match the TR size, so that PDMA delineates each transfer as an individual packet. This is especially problematic in cases like where TRPD has infinite reload count set to perform cyclic transfer using a single set of TRs in streaming mode, in which case each TR could potentially be the last one.

b) If the usecase doesn't allow for PDMA Z count to be set in advance or packet EOP cannot be set then alternate is to use PKTDMA in single buffer mode instead of BCDMA.

i2435 Boot: ROM timeout for eMMC boot too long

Details:

Due to a bug in ROM, if attempting to boot in eMMC boot mode (ie, from eMMC boot partitions, sometimes referred to as eMMC alternative mode) from an eMMC device that is empty or erased (or factory fresh), the normal boot timeout to switch to backup boot mode takes 10 seconds.

Workaround(s):

Need to boot from another boot mode if this timeout considered too long in the system.

i2461 Debug: Wait-In-Reset (WIR) mode is not functional

Details:

The 16nm IO cells for 1.8V only and dual-voltage (1.8V/3.3V) glitch while transitioning from reset. Glitch occurs when input is logic 1.

This prevents the device from entering WIR mode after power-up.

i2461 (continued) — *Debug: Wait-In-Reset (WIR) mode is not functional*

Workaround(s):

None

i2462 — *Boot: ROM xSPI-SFDP boot mode fails*

Details:

xSPI-SFDP boot fails to boot second stage image. ROM assumes access to flash device is in 1S-1S-1S mode for second stage image, but flash is left in 8D-8D-8D mode after first stage image is booted.

Workaround(s):

1st stage image should reset the flash into 1S-1S-1S mode.

i2463 — *Boot: Possible boot failure with SD cards*

Details:

SD card boot may fail on some SD cards. ROM is incorrectly setting the SD card interface frequency too high during initialization, and this can this can cause the data on the card to be read incorrectly, leading to a boot failure. Behavior can change if choosing a card from a different manufacturer, or for different board designs. SD card backup boot may be successful, or subsequent boots after reset may be successful.

Workaround(s):

Choose another SD card manufacturer or a different card type from the same manufacturer for more consistent results. Choosing SD card backup boot may also work on affected cards.

i2464 — *Boot: ROM is unable to boot from SD cards with incorrect formatting*

Details:

MMCSD boot mode may be unable to boot from SD cards if the filesystem is formatted incorrectly during the creation of the filesystem.

Workaround(s):

When creating the SD from Ubuntu 22.04 system, add "-a" argument to the mkfs.vfat command to generate correct boot partitioning.

i2465 — *Boot: EMMC boot mode is slower than expected*

Details:

The MMC0_CLK clock signal during eMMC boot mode is 5MHz during boot instead of the expected 25MHz

Workaround(s):

None. MMC boot will be slower than expected, but still functional

i2466 — *Boot: ROM boot fails for large file sizes*

Details:

For any filesystem based boot mode (ie. MMCSD, USB MSC), boot fails for file sizes greater than 2MB .

Workaround(s):

Use file size less than described

i2467 — *Boot: ROM UART boot fails with large image*

Details:

ROM UART timeout value is not large enough. Thus, UART boot will time out during dual stage boot if the boot image is greater than 800KBytes

Workaround(s):

Use a boot image that is less than 800KBytes

i2469 — *Boot: ROM NOBOOT boot mode is not functional*

Details:

When booting with NoBoot boot mode, SMS hangs and is not recoverable

Workaround(s):

None. Do not use NoBoot boot mode. It may be possible to use DevBoot boot mode in certain situations.

i2470 — *Boot: USB-DFU primary boot mode fails to transition to backup boot mode*

Details:

When USB-DFU primary boot mode is selected with any backup boot mode, ROM will fail to transition to the backup boot mode if primary boot mode times out. This will generally occur when no image is present for USB-DFU boot mode. Note that this boot sequence is works if USB-DFU primary boot fails before timeout (eg, if image is read by the ROM but is unbootable).

Workaround(s):

None.

i2471 — *Boot: Certain primary/backup boot mode combinations fail*

Details:

Certain primary/backup boot order combinations will fail dual stage boot in the backup boot mode

If primary boot has an offset based start point (eg, O/Q/SPI, Serial NAND, GPMC NAND, eMMC boot)

and backup boot mode is filesystem based (eg, SD card, eMMC with UDA, USB MSC), then boot will fail in the backup boot mode (during second stage processing), if primary boot is not successful

OR

If primary boot is filesystem based (eg, SD card, eMMC with UDA, USB MSC),

and backup boot mode has an offset based start point (eg, O/Q/SPI, Serial NAND, GPMC NAND, eMMC boot), then boot will fail in the backup boot mode (during second stage processing), if primary boot is not successful

Workaround(s):

None. Do not select the affected boot combinations.

i2473 — *Boot: eMMC boot may fail*

Details:

eMMC boot using boot partitions is unreliable. This issue is still under investigation. Note, this advisory does not apply to eMMC Boot using UDA.

i2473 (continued) — *Boot: eMMC boot may fail*

Workaround(s):

None. Recommend to use eMMC boot using UDA or a different boot media.

i2474 — *Boot: Certain second stage binaries fail for block based boot modes*

Details:

ROM fails to boot on SD, eMMC, USB-DFU, Serial NAND, GPMC NAND, and UART if certificate size is aligned to 128 Bytes.

Workaround(s):

Certificate size must not be aligned to 128 bytes, however, individual components must be aligned to 128 bytes.

i2160 — *DDR: Valid VRef Range Must be Defined During LPDDR4 Command Bus Training*

Details:

The DDR PHY updates VREF(ca) for the command/address bus during LPDDR4 Command Bus Training (CBT). If VREF(ca) search range is set to invalid values such as no working settings can be found during CBT, the training process could fail or hang.

Workaround(s):

Set the following fields to known valid working values before enabling CBT.

For frequency set 0: PI_CALVL_VREF_INITIAL_START_POINT_F0 and PI_CALVL_VREF_INITIAL_STOP_POINT_F0

For frequency set 1: PI_CALVL_VREF_INITIAL_START_POINT_F1 and PI_CALVL_VREF_INITIAL_STOP_POINT_F1

For frequency set 2: PI_CALVL_VREF_INITIAL_START_POINT_F2 and PI_CALVL_VREF_INITIAL_STOP_POINT_F2

Recommendation is to use the nominal VRef value (based on the device programming of drive strength on the processor and termination in the memory) +/- 4%. Please use the online DDR Register Configuration Tool at http://dev.ti.com/sysconfig to program these registers and check the Revision History to ensure this workaround has been addressed in the version of the tool being used.

i2481 — *Boot: eMMC alternate boot fails if partition is not reprogrammed every time*

Details:

For eMMC boot (ie, boot from eMMC boot partitions), boot will fail if partition is not reprogrammed into the EXT_CSD register. This renders eMMC boot inoperable after any subsequent resets. Note this does not apply to eMMC boot using UDA mode.

Workaround(s):

None

i2482 — *Boot: ROM does not provide enough clocks during SD card initialization*

Details:

ROM code is not providing 74 clocks before sending first command as specified in the SD Card Physical Layer Specification ver. 2.00. This may cause SD card boot to fail, however, a failure has never been observed due to this errata on affected devices.

i2482 (continued) *Boot: ROM does not provide enough clocks during SD card initialization*

Workaround(s):

None

i2484 *Boot: ROM fails to parse X509 certificates using GENERALIZED time format*

Details:

If the initial bootloader tiboot3.bin contains an end date in a generalized format, ROM will fail to parse the X509 certificates and fail to boot.

Workaround(s):

Use UTC format for end date.

i2487 *LPM: Low power modes may inadvertently corrupt DDR contents*

Details:

During entry to the Deep Sleep or RTC+IO+DDR low-power modes, the device may not properly transition the attached DDR into retention mode, which will lead to corruption of the DDR data.

Affected devices should not utilize these low power modes.

Workaround(s):

None

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 30, 2025 to October 2, 2025 (from Revision A (May 2025) to Revision B (October 2025)) **Page**

- Removed SR1.1 table note under Table 1-2. Advisories Matrix as advisories fixes have been validated. Changed i2462, SR 1.1 to YES.......... 2
- Added Advisory i2493; MMCSD: HS200 Write Failures.......... 8

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