

# CC2340R SimpleLink™ Family of 2.4GHz Wireless MCUs

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## ABSTRACT

This document describes the known exceptions to functional specifications (advisories) to the CC2340R SimpleLink™ Family of 2.4GHz Wireless MCUs.

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## 1 Advisories Matrix

Table 1-1 lists all advisories, modules affected, and the applicable silicon revisions.

**Table 1-1. Advisories Matrix**

Module	Description	Device Part Number			
		CC2340R53	CC2340R52	CC2340R22	CC2340R21
		Revision Affected <sup>(1)</sup>			
SPI	<a href="#">Advisory SPI_04</a> —Hang scenario with SPI waiting for CPU intervention forever	B	B	B	A
ADC	<a href="#">Advisory ADC_08</a> —ADC BUSY bit not cleared in repeat single, sequence, and repeat sequence conversion modes	B	B	B	A
ADC	<a href="#">Advisory ADC_09</a> —ADC can have random conversion errors.	B	B	B	A
BATMON	<a href="#">Advisory BATMON_01</a> —Incorrect temperature measurement	B	B	B	A
CKM	<a href="#">Advisory CLK_01</a> —Bluetooth® Low Energy link not being maintained when using LFOSC only	B	B	B	A
CKM	<a href="#">Advisory CKM_01</a> — Tracking loop issues during standby-wake	B	B	B	A
I2C	<a href="#">Advisory I2C_02</a> —SDA and SCL open-drain output buffer issue	B	B	B	A
GPIO	<a href="#">Advisory GPIO_01</a> —Open-drain configuration can drive a short high pulse	B	B	B	A
PMU	<a href="#">Advisory PMU_01</a> —Slow Transition Across Brown-Out Detect (BOD) Threshold Might Cause the Device to Hang	B	B	B	A

(1) Also affects all previous revisions unless otherwise noted.

Table 1-2 lists the latest revision for each of the device part numbers referenced in this errata.

**Table 1-2. Latest Revision by Part Number**

Part Number	Revision
CC2340R53	B
CC2340R52	B
CC2340R22	B
CC2340R21	A

## 2 Nomenclature, Package Symbolization, and Revision Identification

### 2.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all SimpleLink Wireless devices. Each SimpleLink Wireless part number has one of two prefixes: CC or XC. These prefixes represent evolutionary stages of product development from engineering prototypes (XC) through fully qualified production devices (CC).

Device development evolutionary flow:

- XC** Experimental device that is not necessarily representative of the final device electrical specifications and may not use production assembly flow.
- CC** Production version of the silicon die that is fully qualified.

XC devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices are not used in any production system because the expected end-use failure rate is still undefined. Only qualified production devices are to be used.

### 2.2 Devices Supported

This document supports the following device:

- [CC2340R5x](#)
- [CC2340R2x](#)

### 2.3 Package Symbolization and Revision Identification

Figure 2-1 and Table 2-1 describe package symbolization and the device revision code.

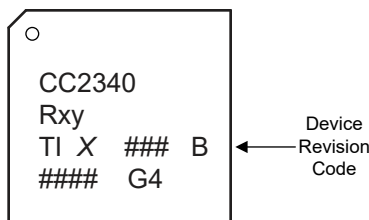


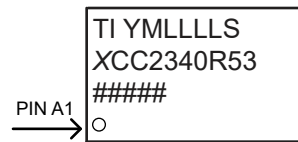
Figure 2-1. Package Symbolization QFN

Table 2-1. Revision Identification

Device Revision Code	Version <sup>(1)</sup>
A	0
B	1 or 2 <sup>(2)</sup>

- (1) See *CC2340xx Technical Reference Manual* for the description of the SYS0:DEVICEID[31:28] VERSION bit field.
- (2) CC2340R52 only

The device marking includes the part number CC2340Rxy where x denotes the amount of flash and y denotes the amount of RAM. ##### is the lot trace code. Optionally, 'X' following the TI letters indicates an experimental device. G4 is the environmental classification.



**Figure 2-2. Package Symbolization WCSP**

The device marking includes the part number CC2340R53. YM is the year/month code, LLLL is the assembly lot code, and S is the assembly site code. ##### is the wafer and die location information. Optionally, 'X' preceding the part number indicates an experimental device.

### 3 Advisories

**SPI\_04** *A hang scenario with the SPI waiting continuously for the CPU to intervene*

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**Revisions Affected** See [Table 1-1](#)

**Details** When the CPU is reading or writing the SPI FIFO using FIFO level triggers to generate interrupts, the system can hang. After the first interrupt is serviced, the FIFO level can permanently be below or above the configured threshold and not generate a subsequent CPU interrupt. This can lead to a hang scenario with SPI waiting for CPU intervention forever.

**Workaround**

1. Use polling of FIFO status within SPI and do not rely on FIFO level configured interrupts, or
2. Use only empty/overflow interrupts and do not use FIFO level configured interrupts, or
3. Use FIFO level configured interrupts along with empty (for TXFIFO) and overflow (for RXFIFO) as a failsafe to avoid hang scenarios.

**ADC\_08** *The ADC BUSY bit is not cleared in repeat single, sequence, and repeat sequence conversion modes.*

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**Revisions Affected** See [Table 1-1](#)

**Description** When the ADC is configured in repeat single, sequence, or repeat sequence conversion modes with trigger policy as trigger next in the MEMCTLx register, software attempting to stop the conversion sequence by clearing the ENC bit does not clear the BUSY bit in the STATUS register. In the case of sequence conversion mode with trigger next policy, the BUSY bit is cleared at the end of the conversion sequence.

**Workaround** To stop the conversions and to clear the BUSY bit in the above-mentioned ADC operating scenario, the following software sequence can be followed.

1. Write CTL0.ENC = 0
2. Change CTL1.TRIGSRC to SOFTWARE
3. Write CTL1.SC=1

**ADC\_09*****The ADC can have random conversion errors.***

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**Revisions Affected**See [Table 1-1](#)**Description**

ADC can have errors at a rate as high as 1 in 400 million ADC conversions. When a conversion error occurs, the error results in a jump in the digital output of the ADC without a corresponding change in the ADC input voltage, otherwise known as a 'sparkle code'. The magnitude of the jump is 64 LSBs higher or lower than the expected ADC output when ADC is used in 12-bit resolution setting. The magnitude of the jump decreases to +/-16 LSBs for 10-bit resolution and +/-4 LSBs when set to 8-bit resolution.

**Workaround**

The error rate can be reduced to 1 error in 100 billion ADC conversions by setting ADC.DEBUG1:CTRL[10:9] bits high.

Other software workarounds like a best-out-of-three, where out of three consecutive samples, the one with the highest standard deviation is discarded and the other two averaged to generate the ADC output can also be considered.

Software averaging of 16 consecutive ADC outputs decreases the deviation of the ADC output to +/- 4 LSBs when set to 12-bit resolution.

These workarounds would be incorporated into future releases of SimpleLink™ Low Power F3 software development kit (SDK).

**BATMON\_01** *Incorrect temperature measurement*

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**Revisions Affected** See [Table 1-1](#)

**Description** BATMON can report incorrect temperatures when hysteresis is enabled. To prevent potential incorrect temperature reports, the user must always disable BATMON hysteresis.

**Workaround** Hysteresis is controlled by the PMUD.CLT[2] HYST\_EN bit.

Hysteresis is enabled by default (reset value = 1) and, therefore, must actively be disabled during boot.

Hysteresis can be disabled by clearing the PMUD.CLT[2] HYST\_EN bit using the following command:

```
HWREG( PMUD_BASE + PMUD_O_CTL ) = ( PMUD_CTL_CALC_EN |
PMUD_CTL_MEAS_EN )
```

This workaround is incorporated into the SimpleLink™ Low Power F3 software development kit (SDK) version 8.10 and newer.

**CLK\_01** *Bluetooth Low Energy link not being maintained when using LFOSC only*

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**Revisions Affected** See [Table 1-1](#)

**Description** A small percentage of devices do not maintain a Bluetooth Low Energy link if LFOSC is used as a sleep clock due to random timing error above 500PPM.

**Workaround** A software workaround are available in the SimpleLink F3 SDK >= 8.10.xx to allow devices to operate in the broadcaster, observer and peripheral roles when using LFOSC only. When the software workaround is used, the device can see short periods of operation with reduced throughput and increased power consumption when the timing error occurs. This software workaround does not support the central role. To completely avoid the consequences of increased power consumption and connection throughput or support the Central role, TI recommends using an external 32.768kHz crystal.

**CKM\_01**      ***Tracking loop issues during standby-wake***

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**Revisions Affected**      See [Table 1-1](#)**Details**

In a few corner cases, the HFOSC tracking loop stops working out of standby, with TRACKREFLOSS getting set, indicating that the selected reference clock of the tracking loop is lost.

**Workaround**

The standby entry sequence includes disabling software override and clearing CKM LDO control bits. These writes have to be sequenced such that the software override is cleared first, and then the LDOCTL bits are all set to zero.

If these settings occur in parallel, the tracking loop is seen to get stuck in a few cases.

The workaround has been implemented within the power drivers and is a part of the 9.10 SDK release.



## I2C\_01

### *SDA and SCL open-drain output buffer issue*

Revisions Affected See [Table 1-1](#)

#### Description

The SDA and SCL outputs are implemented with push-pull 3-state output buffers rather than open-drain output buffers as required by I<sup>2</sup>C. While it is possible for the push-pull 3-state output buffers to behave as open-drain outputs, an internal timing skew issue causes the outputs to drive a logic-high for a duration of approximately 1ns–2ns before the outputs are disabled. The unexpected high-level pulse only occurs when the SCL or SDA outputs transition from a driven low state to a high-impedance state.

This short high-level pulse injects energy into the I<sup>2</sup>C signal traces, which causes the I<sup>2</sup>C signals to sustain a period of ringing as a result of multiple transmission line reflections. This ringing does not typically cause an issue on the SDA signal because the ringing only occurs at times when SDA is expected to be changing logic levels and the ringing has time to damp before data is latched by the receiving device. The ringing can have enough amplitude to cross the SCL input buffer switching threshold several times during the first few nanoseconds of this ringing period, which can cause clock glitches. This ringing does not typically cause a problem if the amplitude is damped within the first 50ns because I<sup>2</sup>C devices are required to filter the SCL inputs to remove clock glitches. Therefore, it is important to design the PCB signal traces to limit the duration of the ringing to less than 50ns. One possible way to reduce the ringing is to insert series termination resistors near the SCL and SDA terminals to attenuate transmission line reflections.

This issue can also cause the SDA output to be in contention with the target SDA output for the duration of the unexpected high-level pulse when the target begins an ACK cycle. This occurs because the target can already be driving SDA low before the unexpected high-level pulse occurs. The glitch that occurs on SDA as a result of this short period of contention does not cause any I<sup>2</sup>C protocol issue, but the peak current applies unwanted stress to both I<sup>2</sup>C devices and potentially increases power supply noise. Therefore, a series termination resistor located near the respective SDA terminal is required to limit the current during the short period of contention.

A similar contention problem can occur on SCL when connected to I<sup>2</sup>C target devices that support clock stretching. This occurs because the target is driving SCL low before the unexpected high-level pulse occurs. The glitch that occurs on SCL as a result of this short period of contention does not cause any I<sup>2</sup>C protocol issue because I<sup>2</sup>C devices are required to apply a glitch filter to the SCL inputs. However, the peak current applies unwanted stress to both I<sup>2</sup>C devices and potentially increases power supply noise. Therefore, a series termination resistor located near the respective SCL terminal is required to limit the current during the short period of contention.

If another controller is connected, the unexpected high-level pulses on the SCL and SDA outputs can cause contention during clock synchronization and arbitration. The series termination resistors described above also limit the contention current in this use case without creating any I<sup>2</sup>C protocol issue.

#### Workaround

Insert series termination resistors on the SCL and SDA signals and locate them near the SCL and SDA terminals, along with the SCL and SDA pullup resistors.

The ringing can also be reduced by controlling the output to use minimum drive strength and a reduced slew rate. These options are only configurable on pins that support high drive output. Standard drive pins have no configuration options.

## GPIO\_01 *Open-drain configuration can drive a short high pulse.*

**Revisions Affected** See [Table 1-1](#)

### Description

Each DIO can be configured to an open-drain mode using the IOCx register.

However, an internal device timing issue can cause the GPIO to drive a logic-high for approximately 1ns–2ns during the transition into or out of the high-impedance state. This undesired high level can cause the GPIO to be in contention with another open-drain driver on the line if the other driver is simultaneously driving low. The contention is undesirable because the contention applies stress to both devices and results in a brief intermediate voltage level on the signal. This intermediate voltage level can be incorrectly interpreted as a high level if there is not sufficient logic filtering present in the receiver logic to filter this brief pulse.

### Workaround

If contention is a concern, do not use the open-drain functionality of the GPIOs; instead, emulate open-drain mode in the software. Open-drain emulation can be achieved by setting the GPIO data (DOUT31\_0.DIOx) to a static 0 and driving the GPIO output enable (DOE31\_0.DIOx) to enable or disable the drive low. For an example implementation, see the code below.

```
#include <ti/devices/cc23x0r5/driverlib/gpio.h>
/* Call driver init functions */
GPIO_init();

//Set GPIO data (DOUT31_0.DIOx) to static 0
GPIOClearDio(CONFIG_GPIO_LED_0);
while(1) //loop below toggles the LED on and off every 1 second
{
    GPIOSetOutputEnabledDio(CONFIG_GPIO_LED_0, 1);
    sleep(1);
    GPIOSetOutputEnabledDio(CONFIG_GPIO_LED_0, 0);
    sleep(1);
}
```

**PMU\_01**

***A slow transition across the brown-out detect (BOD) threshold might cause the device to hang.***

**Revisions Affected**

See [Table 1-1](#)

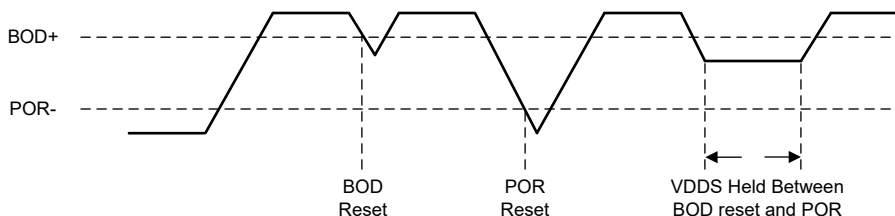
**Details**

If the VDD5 supply voltage is held in the BOD threshold region (approximately 1.68V), the device might, on rare occasions, enter a lock-up state. In this state, the device draws approximately 2.25mA of current and will not recover even if the VDD5 supply voltage is subsequently increased above the BOD threshold. Recovery from this state requires either a pin reset or reducing the VDD5 supply voltage below the power-on reset (POR) threshold (1.0V), thereby triggering a POR reset.

The lock-up state is triggered if a brown-out-detect (BOD) event occurs during specific stages of boot code execution. There are two critical narrow time windows, each of approximately 10 ns duration, and both of these time windows occur within 100 μs to 1 ms after the reset event that initiates the boot code. The issue typically arises when the supply voltage ramps slowly across the BOD threshold. In such cases, supply resistance in combination with device startup current may cause the VDD5 voltage to repeatedly dip below the BOD threshold as the device resets, increasing the likelihood of entering the lock-up state.

For Li-Ion and NiMH rechargeable batteries, a first-level protection disconnecting the chip VDD5 supply would typically prevent the device from entering this state during battery discharge, as the device power supply would fall below the POR threshold.

Even with non-rechargeable (primary) batteries, this issue may still occur, particularly as the battery approaches end-of-life and the voltage slowly decreases. In these cases, a workaround may not always be necessary, as the device will eventually require battery replacement, which would also trigger a power-on reset. However, the risk of lock-up cannot be ruled out.



**Figure 3-1. Diagram Showing Occurrence**

**Workaround**

The following workarounds must be implemented:

The specified operating supply voltage range for the device is 1.72V to 3.8V. When using rechargeable batteries, the battery protection system must ensure one of the following:

- The device supply voltage remains at or above the minimum operating supply voltage (1.72V) once powered on, or
- If the device supply is discharged below the minimum operating supply voltage (1.72V), the device must be reset (pin or power-on reset) when the supply is charged above the minimum operating supply voltage (1.72V) again.

**4 Trademarks**

SimpleLink™ is a trademark of Texas Instruments.  
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## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from October 30, 2024 to September 11, 2025 (from Revision E (August 2024) to Revision F (September 2025))

	Page
• Added Advisory CKM_01 and Advisory PMU_01.....	2
• Updated the naming convention.....	3
• Updated device revision information.....	3
• Updated device marking details.....	3
• Updated description.....	5
• Updated description.....	6
• Updated description.....	7

### Changes from August 11, 2024 to October 30, 2024 (from Revision D (August 2024) to Revision E (October 2024))

	Page
• Merged CC2340R21, CC2340R22, CC2340R52, and CC2340R53 erratas.....	1
• Updated nomenclature and part marking descriptions.....	3

### Changes from February 24, 2024 to August 11, 2024 (from Revision C (February 2024) to Revision D (August 2024))

	Page
• Added Advisory I2C_02.....	2
• Added Advisory GPIO_01.....	2
• Added Advisory ADC_09.....	2

### Changes from October 24, 2023 to February 24, 2024 (from Revision B (October 2023) to Revision C (February 2024))

	Page
• Fixed typos throughout the document.....	1
• Added Advisory CLK_01.....	2

### Changes from April 1, 2023 to October 23, 2023 (from Revision A (April 2023) to Revision B (October 2023))

	Page
• Added Advisory BATMON_01.....	2

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