

mmWave Diagnostic and Monitoring for High-End Corner Radar Reference Design



Description

This reference design features the built-in autonomous monitoring functionality in the mmWave Radar sensors that enhances design efficiency by minimizing the processing load on the host. This reference design uses Safety Diagnostic Library (SDL) to perform a diagnostic test at programmable digital cores, peripherals, and memories. The design also configures and enables radio frequency (RF) and Analog Monitor features of different hardware components. By assisting in the implement of ASIL-B SIL2 compliant products with the various safety resources, this reference design accelerates overall development time and time to market.

Resources

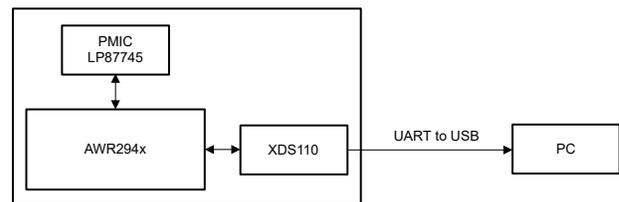
TIDEP-01030	Design Folder
AWR2944	Product Folder
AWR2944EVM	Tool Folder
mmWave MCUPLUS SDK	Tool Folder

Features

- Demonstrates the usage of inbuilt Diagnostic and Monitor features of mmWave Radar Sensors to improve system performance and robustness
- Use of safety resources to build ASIL-B SIL2 mmWave sensors across different devices and applications to make system implementation efficient
- Based on proven EVM hardware designs enabling quick time-to-market

Applications

- [Long range radar](#)
- [Medium and short range radar](#)
- [Ultra short range radar](#)



1 System Description

The TIDEP-01030 provides a reference for creating a diagnostic and monitoring application using TI's AWR2944 based on 77GHz mmWave radio-frequency complementary metal-oxide semiconductor (RF-CMOS) technology. mmWave sensing technology detects vehicles, such as cars, motorcycles, and bicycles, at extended ranges regardless of environmental conditions, such as rain, fog, or dust. TI's mmWave sensing devices integrate a 76–81GHz mmWave radar front end with Arm® microcontroller (MCU) and TI DSP cores for single-chip systems.

TI mmWave system on chip (SOC) has built-in circuits for diagnostic and monitoring which enables the detection of both the systematic and random faults. These safety mechanisms significantly reduce system complexity and cost in safety-critical applications. It is important to test these diagnostic mechanisms using SafeTI diagnostic Library (SDL).

TI's radar mmWave integrated chips (ICs) include hardware and firmware elements to enable monitoring of the mmWave analog and digital subsystems. These built-in features of RadarSS are exposed to the application through firmware APIs.

This reference design demonstrates the use of inbuilt diagnostic and monitoring functionality of mmWave Radar Sensor. The design provides a list of required hardware, schematics, and reference software to quickly begin ASIL-B SIL2 compliance product development. This reference design describes the example use case as well as the design principle, implementation details, and engineering tradeoffs made in the development of this application. High-level instructions for replicating the design are provided. A few of the key diagnostic features of the device are listed below:

- Self-test controller (STC)
- Programmable built-in self-test (PBIST)
- Error Correction Code (ECC)
- Bus Safety
- PARITY on miscellaneous memories or peripherals

The details are covered in the Safety Manual.

Note

For the remainder of this document *mmWave Sensor* implies AWR2944 and *EVM* implies AWR2944EVM, unless otherwise mentioned.

2 System Overview

TI's radar mmWave integrated chips (ICs) include hardware and firmware elements to enable monitoring of the mmWave, analog and digital sections. Most of the digital elements of the device have built-in diagnostic capability.

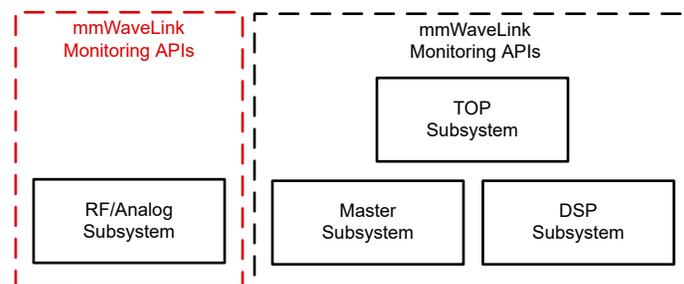


Figure 2-1. mmWave Sensor Monitor and Diagnostic

The analog subsystem contains the Analog and RF functionality of the device. The AWR294x has three or four transmitters and four receiver chains along with the clock oscillator and frequency modulated continuous wave (FMCW) signal generation circuitry (Cleanup APLL, Synthesizer, frequency multipliers, and so forth). The *Radar Subsystem* is responsible for initializing and calibrating the Analog and RF modules. The subsystem periodically monitors the Analog and RF functionality to make sure all the Analog and RF modules work in the defined

limits. This functionality can be configured through mmWavelink Monitoring APIs by MSS or DSS application with various mode and reporting options.

TOP, Master, and DSP subsystems contain various memory and digital components which have safety diagnostic features. These features can be configured and verified using the Safety Diagnostic Library to manage both systematic and random faults of the device.

2.1 Block Diagram

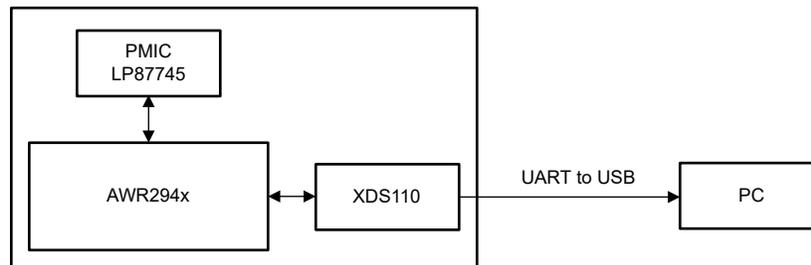


Figure 2-2. TIDEP-01030 Block Diagram

2.2 Design Considerations

This reference design shows the use of the Diagnostic and Monitoring feature. Diagnostic tests are implemented through the SDL whereas Monitoring features are enabled on RadarSS through the mmWaveLink library. Some sets of the Diagnostic tests are destructive which can cause a soft or warm reset, so within this reference design those tests are part of the Secondary Bootloader (SBL). This way main application flow does not get hampered due to the execution of these destructive Diagnostic tests. Apart from these DIAG tests, remaining DIAG are executed on MSS as well DSS core during the application initialization. See [Section 2.4.2](#) for further implementation details.

2.3 Highlighted Products

2.3.1 LP87745

The LP87745-Q1 helps meet the power management requirements of the latest platforms, particularly in automotive radar and camera and industrial radar applications. The device contains three step-down DC/DC converters, and a 5V boost converter switch and bypass switch. To support safety critical applications, the device integrates two voltage monitoring inputs for external power supplies, and a window watchdog.

2.3.1.1 LP87745 Features

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature
- Functional safety-compliant device
 - Developed for functional safety applications
 - Documentation available to aid ISO 26262 functional safety system design up to ASIL-C and SIL-2
 - Input supply overvoltage and undervoltage monitoring
 - Regulator output overvoltage and undervoltage monitoring
 - Overvoltage and undervoltage monitoring for one external rail
 - Q and A watchdog
 - Level or PWM error signal monitor (ESM)
 - BIST and CRC
- Input voltage: 3.3V nominal (3V to 4V range)
- Three low-noise step-down DC/DC converters:
 - Output voltage: 0.9V to 1.9V, 0.8V (BUCK3), 0.82V (BUCK3)
 - Maximum output current: 3A, 3A, 3A
 - Switching frequency: 4.4MHz, 8.8MHz, and 17.6MHz
- 5V boost converter
 - Maximum output current: 350mA

- 150mA LDO
 - Output voltage 1.8V or 3.3V
- Output short-circuit and overload protection
- Input overvoltage protection (OVP) and undervoltage lockout (UVLO)
- Overtemperature warning and protection
- Serial peripheral interface (SPI)

2.3.1.2 Safety Features

The LP8774x-Q1 device is an ISO26262 functional safety-compliant power management IC (PMIC) to aid safety system designs up to ASIL-C, SIL-2 with the following key functional safety features. See the [LP87745-Q1 Three Buck Converters and 5-V Boost for AWR and IWR Radar Sensors](#) data sheet specification and the LP87745-Q1 Functional Safety Manual [SFFS159](#) for more details about the safety mechanisms and how to integrate this device in a functional safety system.

- **Monitoring of VCCA Input, Regulator Outputs, and VMON Inputs**

The LP8774x-Q1 device monitors the undervoltage (UV) and overvoltage (OV) conditions of the output voltage of the bucks, the boost, VIO_LDO, VMON1 (general purpose voltage monitor) input and the VCCA input through independent voltage monitors. In addition, regulator outputs are monitored by short-circuit and current limit comparators. Regulator monitors are enabled when the corresponding regulator is enabled and OV, UV self-test is completed.

- **Finite state machine (FSM) and Safing outputs: NRSTOUT, nINT, CAN_DIS**

The LP8774x-Q1 device integrates a finite state machine (FSM) engine which manages the state of the device during operating state transitions. The device supports NVM configurable power-up, power-down sequences and error handling. In the case of severe errors, the main processor reset signal (NRSTOUT) is pulled low and all the supply rails are turned off to keep the system in safe state. If moderate error events occur, depending on the NVM configuration, PMIC can notify the processor of these events through the interrupt signal (nINT) and through software interrupts and can disable Controller Area Network (CAN) communication with nINT or CAN_DIS signal.

- **Q&A watchdog**

The watchdog monitors the correct operation of the MCU. The Question Answer (Q&A) mode watchdog in LP8774x-Q1 requires specific messages from the MCU in specific time intervals to detect correct operation of the MCU. During operation, the device provides a question for the MCU through the SPI. The MCU performs a fixed series of arithmetic operations on this question to calculate the required 32-bit answer. This answer is split into four answer bytes: Answer-3, Answer-2, Answer-1, and Answer-0 and the MCU must send these answers in a correct sequence and timing through the SPI. If the MCU answer or the answer sequence is not correct, the device detects the error and the response to the error depends on the NVM, OTP configuration and in if there are persistent errors, PMIC error counter overflows and all the supply rails are shut down to keep the system in safe state.

- **Error signal monitor (ESM)**

The LP8774x-Q1 device has an Error Signal Monitor (ESMs) to monitor the MCU error output signal at the nERR input pin. By default, ESM is disabled at start-up of the LP8774x-Q1 device. To start ESM, the MCU sets the start bit.

ESM_MCU_START initiates through software after the system is powered up and the LP8774x-Q1 configuration is completed by MCU. The device supports either Level mode or PWM mode. If the device detects the ESM error and the response to the error depends on the NVM, OTP configuration and in the case of persistent errors, the PMIC error counter overflows and all the supply rails are shut down to keep the system in safe state.

- **ABIST, LBIST and CRC**

The device has analog build in self-test (ABIST) which checks the health of voltage monitors and TSD compactors and logic built-in self-test (LBIST) which checks the digital features during the device start-up and notification is sent to the processor. Device trim registers, configuration registers and SPI communication are protected with CRC to detect the bit errors.

2.3.2 AWR294x mmWave Sensor

The mmWave sensor is an integrated single-chip, frequency-modulated continuous wave (FMCW) sensor capable of operation in the 76–81GHz frequency band. The device is built with TI's low-power, 45nm RFCMOS processor and enables unprecedented levels of analog and digital integration in an extremely small form factor. The device has four receivers and three, four transmitters with a closed-loop phase-locked loop (PLL) for precise and linear chirp synthesis.

The sensor includes a built-in radio processor (BIST) for RF calibration and safety monitoring. Based on real baseband architecture, the sensor device supports an IF bandwidth of 15MHz with reconfigurable output sampling rates. The presence of Arm® Cortex® R5F and Texas Instruments C66xx Digital Signal Processor (DSP) (fixed and floating point) along with 4MB of on-chip RAM enables high-level algorithm development. This device is ASIL-B certified and an excellent choice for low power, self-monitored, and ultra-accurate radar systems in the automotive space.

2.4 System Design

2.4.1 Hardware Block Diagram

The TIDEP-01030 is implemented using the AWR2944BOOST EVM. The EVM needs to be connected to a host PC through universal asynchronous receiver-transmitter (UART) for Meta Image load and log collection.

The AWR2944EVM includes the following features:

1. AWR2944 Radar Device on AWR2944EVM
2. Power management circuit to provide all the required supply rails from a single 5V input
3. Four onboard TX antennas and four RX antennas
4. Onboard XDS110 that provides a JTAG interface, UART for sending Diagnostic test and Monitor report from mmWave device

2.4.2.1 Secondary Bootloader (SBL)

The secondary bootloader is primarily responsible for updating the application meta image in the sFlash by receiving the image over a serial interface. The SBL then loads and runs the updated application meta image.

The ROM (primary) bootloader always loads the SBL. Applications can choose to either update or load and run the application meta image.

For safety applications, the SBL can be used to perform some of destructive tests like PBIST and STC that need to be run during boot time. These DIAG can cause core reset during the execution which is the main reason to move these tests to SBL. These tests are validated before loading the main application. In the case of a failure, the SBL aborts and exits.

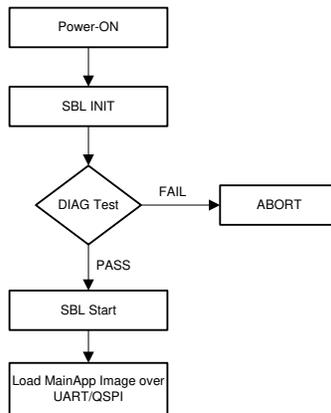


Figure 2-6. SBL Flow Diagram

2.4.2.2 mmWaveLink APIs

mmWaveLink library provides miscellaneous APIs to communicate with RadarSS over the mailbox interface. In this application, monitoring features are configured by MSS/DSS application through mmWaveLink APIs. Later applications receive monitoring reports through mmWaveLink callback in the form of an asynchronous event from RadarSS.

2.4.2.3 mmWave Safety Diagnostic Library (SDL)

The mmWave SafeTI Diagnostic Library (SDL) is a collection of functions for access to safety functions and response handlers for various safety mechanisms for TI mmWave sensors. These functions assist in the development of software applications involving functional safety.

The SDL provides a collection of diagnostic APIs and low-level driver functions to access the diagnostic features. These safety mechanisms are defined in the *mmWave Device Safety Manual*.

Diagnostics Library (DIAG) is the Software diagnostics library that provides APIs to access Safety functions and inject or detect faults.

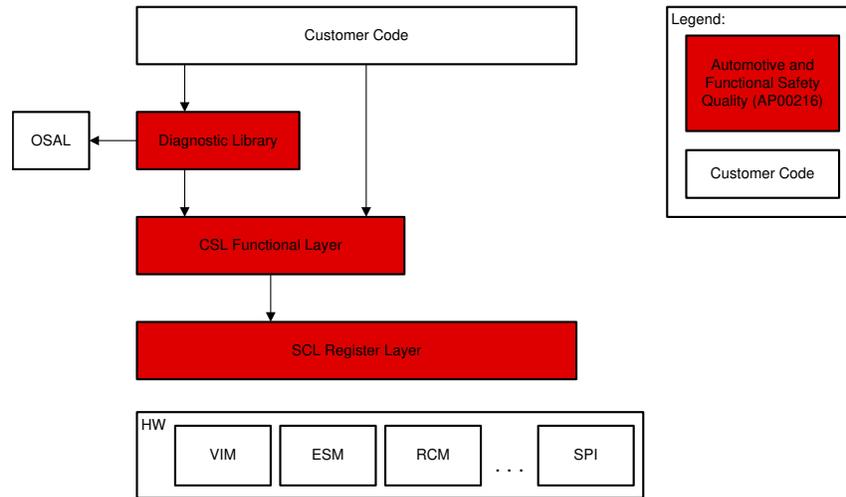


Figure 2-7. SDL Layer Architecture

In [Figure 2-7](#), the red blocks are Functional safety quality, all relevant documents and reports are provided in SDL package.

The Diagnostic Library provides the implementation of the diagnostics specified in the mmWave Device Safety Manual.

Diagnostic test categories (based on time duration):

- Single-shot diagnostics
- Periodic diagnostics
- Fault insertion diagnostics: ECC, Parity, MPU diagnostics.
- Self test diagnostics: LBIST, PBIST, DCC, CCM diagnostics.
- Peripheral IO diagnostics: peripheral loopback, Nerror In or Out diagnostics
- Readback of static configuration registers: diagnostics to periodically check static configuration registers

Typical DIAG Test Flow

- Operating System Adaptation Layer (OSAL) defines the ability to add and delete hooks. Hooks can be added to ESM error and CPU exceptions
- HW Configuration – HW IP registers which need to be configured to execute the diagnostic
- CPU Exception, ESM Error – Diagnostic generate ESM error, CPU exceptions
- All diagnostic handlers are internal to the diagnostic layer

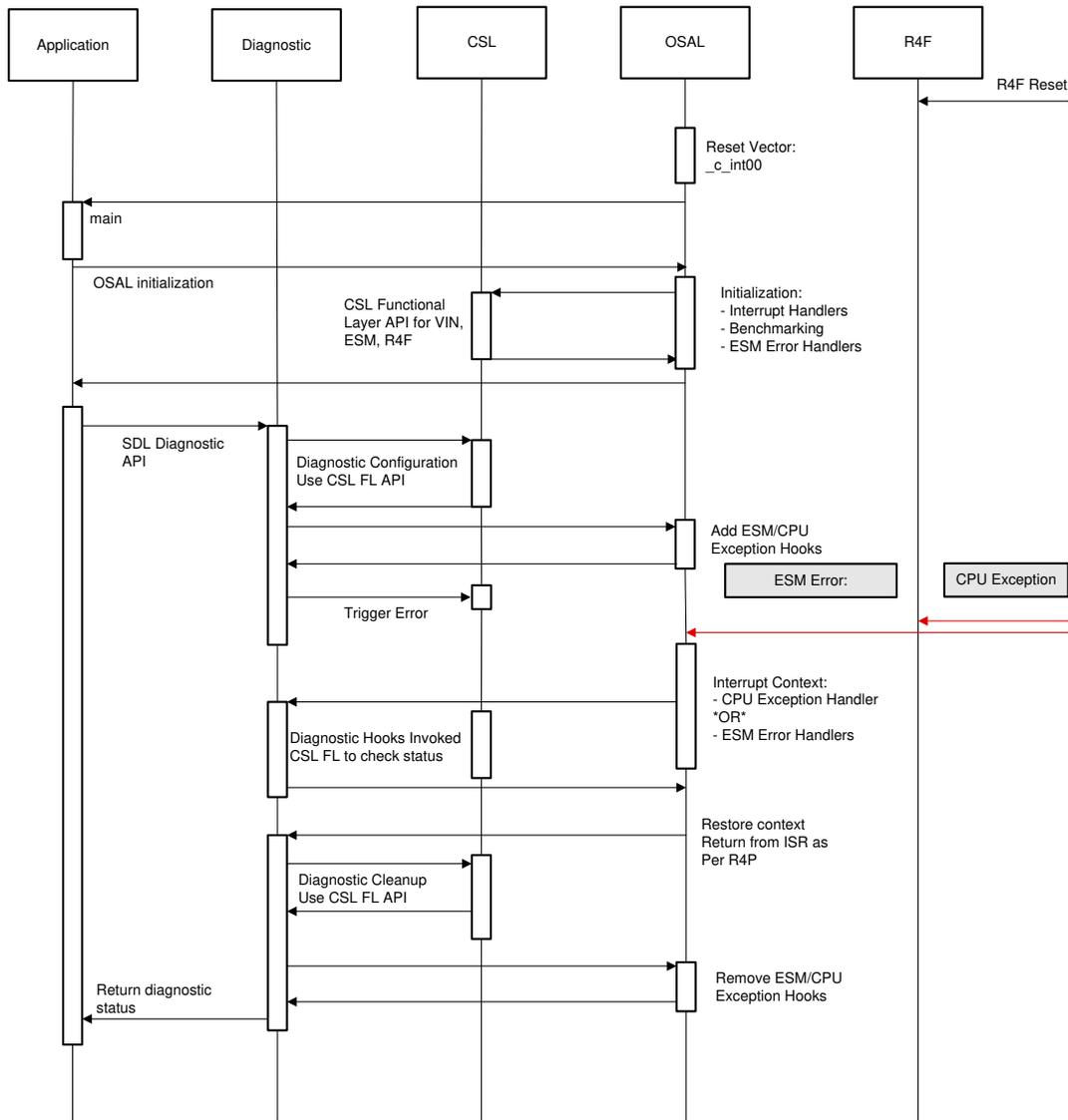


Figure 2-8. DIAG Test Flow

2.4.2.4 mmWave SDK Software Block Diagram

The mmWave software development kit (SDK) enables the development of mmWave sensor applications using the mmWave EVM. The SDK provides foundational components that help designers focus on the applications. In addition, the SDK provides several demonstration applications, which serve as a guide for integrating the SDK into end-user mmWave applications. This reference design is developed on the SDK framework and uses the SDL library.

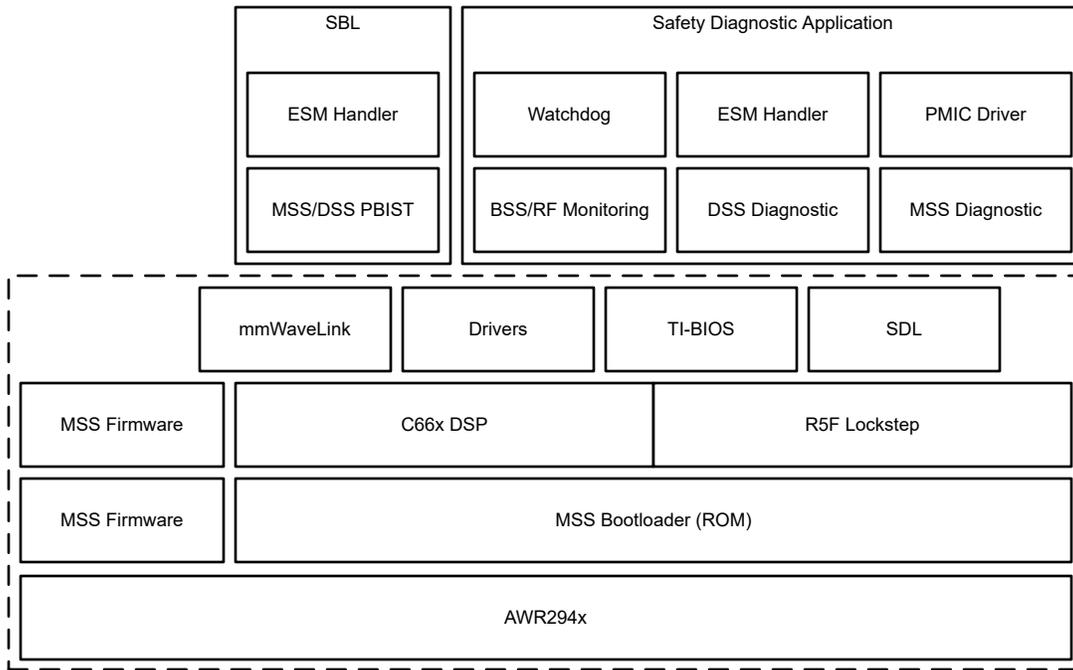


Figure 2-9. SBL and App Block Diagram

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Texas Instruments' AWR2944EVM is an easy-to-use evaluation board for the AWR2944 mmWave sensing device.

This reference design requires AWR2944EVM to execute the reference application. However, customers can run this on the board as well.

3.2 Test Setup

The test setup contains AWR2944EVM that is connected with the PC over a USB cable.

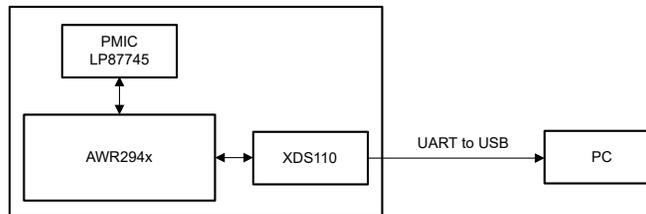


Figure 3-1. Test Setup

Figure 3-2 is the typical test flow for a reference design application.

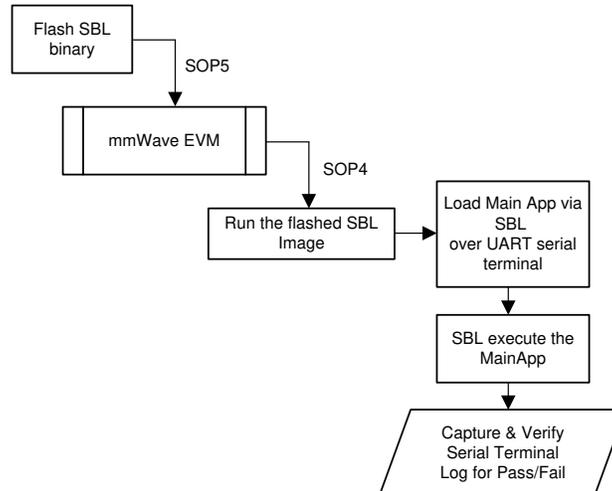


Figure 3-2. Typical Test Flow

3.3 Test Results

AWR2944EVM is connected with the PC over a USB cable. The SBL image is flashed first then the main application. Refer to the *Getting started* document in the software package for the exact steps to execute this application.

Figure 3-3, Figure 3-4, and Figure 3-5 show the test results of a Diagnostic test result performed by SBL as well as the Main application.

```

*****
**
DSS Safety Mechanims Logs
HWA Parity Test Application
HWA TEST START : starting
All test passed for HWA Parity Application
ECC Test Application for HWA Memory
ECC UC-1 and UC-2 Test
UC-1: Injected 1-bit error and got ESM Interrupt
UC-2: Injected 2-bit error and got ESM Interrupt
All Use_Cases have passed for ECC Test Application for HWA Memory.
ECC Test Application for L3 Memory
ECC UC-1 and UC-2 Test
UC-1: Injected 1-bit error and got ESM Interrupt
UC-2: Injected 2-bit error and got ESM Interrupt
All Use_Cases have passed for ECC Test Application for L3 Memory.
ECC Test Application for DSS Mailbox memory
ECC UC-1 and UC-2 Test
UC-1: Injected 1-bit error and got ESM Interrupt
UC-2: Injected 2-bit error and got ESM Interrupt
All Use_Cases have passed for ECC Test Application for DSS Mailbox memory.
DSS TPCC PARITY Example : Started
All tests have passed for TPCC Parity Test Application.
*****
**
MSS Safety Mechanims Logs
TCM Parity Test Application Startring
TCM PARITY Test Appliaiction : Started
ESM_Test_init: Init MSS ESM complete
MSS TCM PARITY: ATCM0 Started
MSS ATCM0 Parity : Completed
ESM_Test_init: Init MSS ESM complete
MSS TCM PARITY: ATCM1 Started
MSS ATCM1 Parity : Completed
ESM_Test_init: Init MSS ESM complete
MSS TCM PARITY: BOTCM0 Started
MSS BOTCM0 Parity : Completed
ESM_Test_init: Init MSS ESM complete
MSS TCM PARITY: BOTCM1 Started
MSS BOTCM1 Parity : Completed
ESM_Test_init: Init MSS ESM complete
MSS TCM PARITY: BITCM0 Started
  
```

Figure 3-3. Diagnostic Test Results 1

```

COM88 - Tera Term VT
File Edit Setup Control Window Help
All tests have passed for ECC Bus Safety Appliaiction.
MCRC Test Application
MCRC AUTO CPU mode on Channel 1: Transfer Test Started...
Calculating Reference MCRC signature Value.
MCRC signature value : 0xc1c13adab4dd50fu
MCRC Full Mode Computation Time: 5293us
Sector signature matches - Passed
Calculated MCRC signature value : 0x01c13adab4dd50fu
EDMA Data transfer completed !!
MCRC Auto Mode Computation Time: 17us
MCRC AUTO CPU mode on Channel 2: Transfer Test Started...
Using Pre-Defined Reference MCRC signature Value.
Pre-defined MCRC signature value : 0xc1c13adab4dd50fu
Sector signature matches - Passed
Calculated MCRC signature value : 0x01c13adab4dd50fu
EDMA Data transfer completed !!
MCRC Auto Mode Computation Time: 15us
TPCC Parity Test Application for MSS Instance
MSS TPCC PARITY Example : Started
ESM_Test_init: Init MSS ESM complete
MSS TPCCB Parity
Paran Register - 8200000?
MSS TPCCB Parity : Completed
ESM_Test_init: Init MSS ESM complete
MSS TPCCB Parity
Paran Register - 8200000?
MSS TPCCB Parity : Completed
All tests have passed for TPCC Parity Test Application.
Debug: ADCBUF Instance 10292CE0 has been reopened successfully
*****
Debug: Launching the mmWaveLink
*****
Debug: CRC Channel 1 has been opened successfully
mmWave Link Initialization Pass
Debug: BootupStatus = 0x3b3b7ffa
Debug: Finished get radarSS bootup status to BSS
Get radarSS bootup status Pass
Debug: Finished r1RFSetDeviceCfg
Set Async event config status Pass
Debug: Set HSI1 clock successfully
  
```

Figure 3-4. Diagnostic Test Results 2

```

ti COMS0 - Yes Sem VT
File Edit Setup Control Window Help

Debug: Finished information related to GPADC Internal Analog Signals monitoring
configurations to BSS
Set mmWave Link GPADC Internal Analog Signals Config
Debug: Finished information related to APLL and Synthesizer's control voltage si
gnals monitoring configurations to BSS
Set mmWave Link MmuaveLink_setRFPLLContrWoltMonConfig Config
Debug: Finished information related to the DCC based clock frequency monitoring
configurations to BSS
Set mmWave Link Dual Clk Config
Debug: Finished r1HfAnaMonConfig configurations to BSS

-----
Start Monitoring Pass
Sensor Start
Debug: Frames are already stopped [21]
Sensor Stop

-----
Monitoring results Pass
-----Debug: Monitoring Report-----
RL_RF_AE_MON_TEMPERATURE_REPORT_SB [0x13]
RL_RF_AE_MON_RX_GAIN_PHASE_REPORT [0xf]
RL_RF_AE_MON_RX_IF_STAGE_REPORT [0x5]
RL_RF_AE_MON_TX0_POWER_REPORT [0x3]
RL_RF_AE_MON_TX1_POWER_REPORT [0x3]
RL_RF_AE_MON_TX2_POWER_REPORT [0x3]
RL_RF_AE_MON_TX3_POWER_REPORT [0x3]
RL_RF_AE_MON_TX0_BALLBREAK_REPORT [0x1]
RL_RF_AE_MON_TX1_BALLBREAK_REPORT [0x1]
RL_RF_AE_MON_TX2_BALLBREAK_REPORT [0x1]
RL_RF_AE_MON_TX3_BALLBREAK_REPORT [0x1]
RL_RF_AE_MON_Adc_IX_GAIN_MISMATCH_REPORT [0x3]
RL_RF_AE_MON_SYNTHESIZER_FREQ_REPORT [0x1]
RL_RF_AE_MON_TX0_INT_ANA_SIG_REPORT [0x3]
RL_RF_AE_MON_TX1_INT_ANA_SIG_REPORT [0x3]
RL_RF_AE_MON_TX2_INT_ANA_SIG_REPORT [0x3]
RL_RF_AE_MON_RX_INT_ANALOG_SIG_REPORT [0xff]
RL_RF_AE_MON_PPCLALO_INT_ANA_SIG_REPORT [0x3]
RL_RF_AE_MON_GPADC_INT_ANA_SIG_REPORT [0x7]
RL_RF_AE_MON_PLL_CONTROL_VOLT_REPORT [0x37]
RL_RF_AE_MON_DCC_CLK_FREQ_REPORT [0x3f]

-----
All tests have completed!!

```

Figure 3-5. Diagnostic Test Results 3

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at [TIDEP-01030](#).

4.1.2 BOM

To download the bill of materials (BOM), see the design files at [TIDEP-01030](#).

4.2 Tools and Software

Tools

Serial Terminal This application takes input and streams the log over the UART COM port. The Serial Terminal tool is required to connect to the device over the COM port.

Software

Diagnostic and Monitoring Reference Application Application source code and binary files are available at TI-Rex Radar Toolbox. Refer to the Getting Started document available in the same package for SW installation and execution steps.

4.3 Documentation Support

1. Texas Instruments, [Enabling Functional Safety in TI mmWave Devices Seminar Presentation](#)
2. Texas Instruments, [LP87745-Q1 Three Buck Converters and 5-V Boost for AWR and IWR Radar Sensors Data Sheet](#)
3. Texas Instruments, [AWR2943/44 Single-Chip 76- and 81-GHz FMCW Radar Sensor Data Sheet](#)

4.4 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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