LMH0034 SMPTE 292M / 259M Adaptive Cable Equalizer

Check for Samples: LMH0034

FEATURES

- **SMPTE 292M, SMPTE 344M and SMPTE 259M Compliant**
- **Supports DVB-ASI at 270 Mbps**
- **Data Rates: 125 Mbps to 1.485 Gbps**
- **Equalizes up to 200 Meters of Belden 1694A at 1.485 Gbps or up to 400 Meters of Belden 1694A at 270 Mbps**
- **Manual Bypass, Cable Length Indicator, and Output Mute with a Programmable Threshold**
- **Single-Ended or Differential Input**
- **50Ω Differential Outputs**
- **Single 3.3V Supply Operation**
- **208 mW Typical Power Consumption with 3.3V Supply**
- **Replaces the GS1524 and GS1524A**

APPLICATIONS

- **SMPTE 292M, SMPTE 344M, and SMPTE 259M Serial Digital Interfaces**
- **Serial Digital Data Equalization and Reception**
- **Data Recovery Equalization**

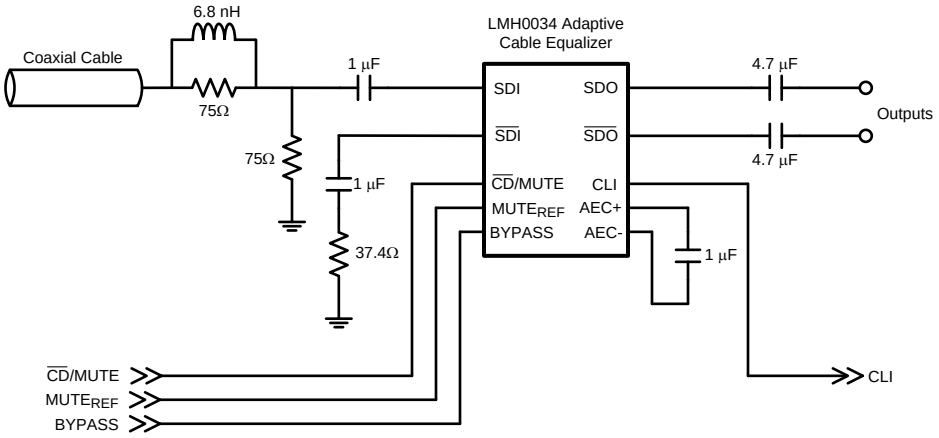
DESCRIPTION

The LMH0034 SMPTE 292M / 259M adaptive cable equalizer is a monolithic integrated circuit for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 1.485 Gbps and supports SMPTE 292M, SMPTE 344M and SMPTE 259M.

The LMH0034 implements DC restoration to correctly handle pathological data conditions. DC restoration can be bypassed for low data rate applications. The equalizer is flexible in allowing either single-ended or differential input drive.

Additional features include a combined carrier detect and output mute pin which mutes the output when no signal is present. A programmable mute reference is used to mute the output at a selectable level of signal degradation. A cable length indicator is provided to determine the amount of cable being equalized.

Typical Application



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage		−0.5V to 3.6V
Input Voltage (all inputs)		−0.3V to V_{CC}+0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C
Lead Temperature (Soldering 4 Sec)		+260°C
Package Thermal Resistance	θ_{JA} 16-pin SOIC	+115°C/W
	θ_{JC} 16-pin SOIC	+105°C/W
ESD Rating (HBM)		8 kV
ESD Rating (MM)		250V

(1) Absolute Maximum Ratings are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of Electrical Characteristics specifies acceptable device operating conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	0°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$		1.9		V
V_{SDI}	Input Voltage Swing	At LMH0034 input(3)(4)		720	800	950	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, $\overline{SDO}$		V_{CC} – V_{SDO}/2		V
V_{SDO}	Output Voltage Swing	50Ω load, differential			750		mV_{P-P}
	CLI DC Voltage	0m cable(5)	CLI		2.5		V
		Max cable(5)			1.9		V
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.7		V
	$\overline{CD}$/MUTE Output Voltage	Carrier not present	$\overline{CD}$/MUTE	2.6			V
		Carrier present				0.4	V
	$\overline{CD}$/MUTE Input Voltage	Min to mute outputs		3.0			V
		Max to force outputs active				2.0	V
I_{CC}	Supply Current	(6)			63	77	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(3) Specification is ensured by characterization.
(4) The maximum input voltage swing assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.
(5) Input signal must be present for valid CLI. Refer to Figure 2 for typical results.
(6) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Refer to Figure 3 and Figure 4.

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AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{MIN}	Minimum Input Data Rate		SDI, $\overline{SDI}$		125		Mbps
BR_{MAX}	Maximum Input Data Rate					1485	Mbps
	Jitter for various cable lengths (with equalizer pathological)	270 Mbps, Belden 1694A, 400 meters(2)			0.2		UI
		270 Mbps, Belden 8281, 280 meters(2)			0.2		UI
		1.485 Gbps, Belden 1694A, 140 meters(2)			0.25		UI
		1.485 Gbps, Belden 8281, 100 meters(2)			0.25		UI
		1.485 Gbps, Belden 1694A, 200 meters(2)			0.3		UI
t_r,t_f	Output Rise Time, Fall Time	20% – 80%(2)	SDO, $\overline{SDO}$		100	220	ps
	Mismatch in Rise/Fall Time	(2)			2	15	ps
t_{OS}	Output Overshoot	(2)			1	5	%
R_{OUT}	Output Resistance	single-ended(3)			50		Ω
RL_{IN}	Input Return Loss	(4)	SDI, $\overline{SDI}$	15	18-20		dB
R_{IN}	Input Resistance	single-ended			1.3		kΩ
C_{IN}	Input Capacitance	single-ended(3)			1		pF

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(2) Specification is ensured by characterization.
(3) Specification is ensured by design.
(4) Input return loss is dependent on board design. The LMH0034 meets this specification on the SD034 evaluation board from 5MHz to 1.5GHz.

Connection Diagram

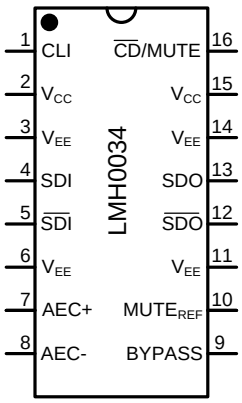

Figure 1. 16-Pin SOIC
See D Package

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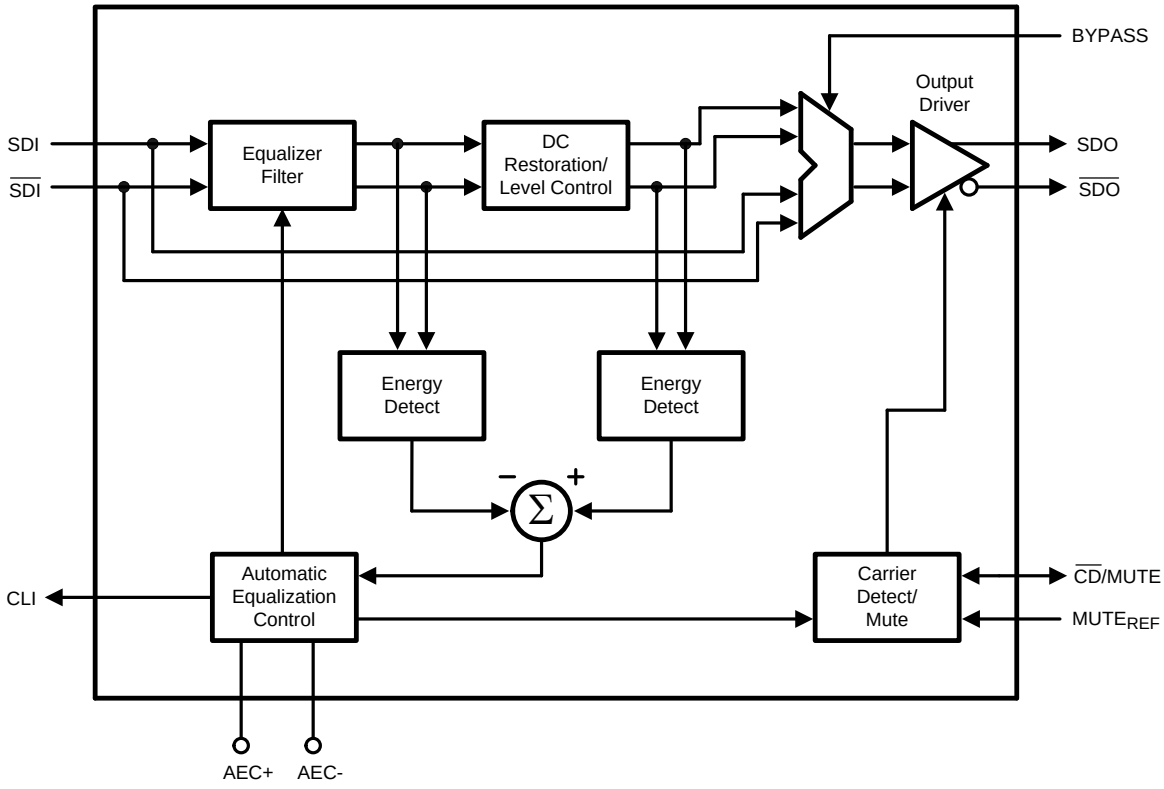
PIN DESCRIPTIONS

Pin #	Name	Description
1	CLI	Cable length indicator. Provides a voltage inversely proportional to the cable length being equalized.
2	V_{CC}	Positive power supply (+3.3V).
3	V_{EE}	Negative power supply (ground).
4	SDI	Serial data true input.
5	$\overline{SDI}$	Serial data complement input.
6	V_{EE}	Negative power supply (ground).
7	AEC+	AEC loop filter external capacitor (1µF) positive connection.
8	AEC-	AEC loop filter external capacitor (1µF) negative connection.
9	BYPASS	Bypasses equalization and DC restoration when high. No equalization occurs in this mode.
10	$MUTE_{REF}$	Mute reference. Determines the maximum cable to be equalized before muting. May be unconnected for maximum equalization.
11	V_{EE}	Negative power supply (ground).
12	$\overline{SDO}$	Serial data complement output.
13	SDO	Serial data true output.
14	V_{EE}	Negative power supply (ground).
15	V_{CC}	Positive power supply (+3.3V).
16	$\overline{CD}$/MUTE	Bi-directional carrier detect and output mute. $\overline{CD}$/MUTE is high when no signal is present. If unconnected, MUTE is controlled automatically by carrier detect. To force MUTE on, tie to V_{CC}. To disable MUTE, tie to GND. $\overline{CD}$/MUTE has no function in BYPASS mode.

Block Diagram



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DEVICE OPERATION

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1µF capacitor placed across the AEC+ and AEC- pins. **Cable Length Indicator (CLI)** is derived from this block.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the bi-directional **$\overline{\text{CD}}$/MUTE** signal along with **Mute Reference (MUTE_{REF})**.

The **Output Driver** produces SDO and $\overline{\text{SDO}}$.

CABLE LENGTH INDICATOR (CLI)

The cable length indicator provides a voltage to indicate the length of cable being equalized. The CLI voltage decreases as the cable length increases. Figure 2 shows the typical CLI voltage vs. Belden 1694A cable length. Note: CLI is only valid when an input signal is present.

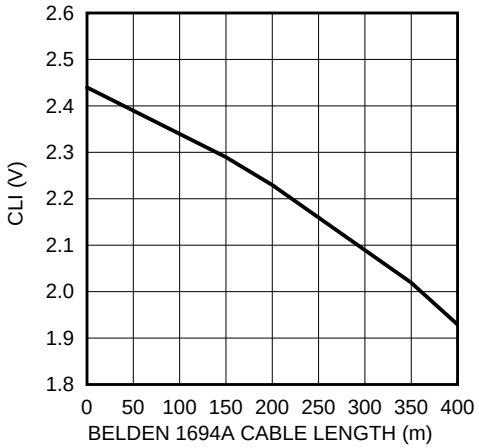

Figure 2. CLI vs. Belden 1694A Cable Length

MUTE REFERENCE (MUTE_{REF})

The mute reference determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE_{REF} voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE_{REF} may be left unconnected for maximum equalization before muting.

CARRIER DETECT / MUTE ($\overline{\text{CD}}$/MUTE)

Carrier Detect / Mute is bi-directional, serving as both a carrier detect (output function) and mute (input function).

When used as an output, $\overline{\text{CD}}$/MUTE determines if a valid signal is present at the LMH0034 input. If MUTE_{REF} is used, the carrier detect threshold will be altered accordingly. $\overline{\text{CD}}$/MUTE provides a high voltage when no signal is present at the LMH0034 input, and the outputs are automatically muted. $\overline{\text{CD}}$/MUTE is low when a valid input signal has been detected, and the outputs are automatically enabled.

As an input, $\overline{\text{CD}}$/MUTE can be used to override the carrier detect and manually mute or enable the LMH0034 outputs. Applying a high input to $\overline{\text{CD}}$/MUTE will mute the LMH0034 outputs. Applying a low input will force the outputs to be active regardless of the length of cable or the state of MUTE_{REF}.

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INPUT INTERFACING

The LMH0034 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The LMH0034 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The SDO and $\overline{\text{SDO}}$ outputs are internally loaded with 50Ω. They produce a 750 mV_{P-P} differential output, or a 375 mV_{P-P} single-ended output.

APPLICATION INFORMATION

PCB LAYOUT RECOMMENDATIONS

Please refer to the following Application Note: AN-1372 (SNLA071) “LMH0034 PCB Layout Techniques.”

REPLACING THE GENNUM GS1524

The LMH0034 is form-fit-function compatible with the Gennum GS1524 and GS1524A.

SUPPLY CURRENT VS. CABLE LENGTH

The supply current (I_{CC}) depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Figure 3 shows supply current vs. Belden 1694A cable length for 1.485 Gbps data and Figure 4 shows supply current vs. Belden 1694A cable length for 270 Mbps data.

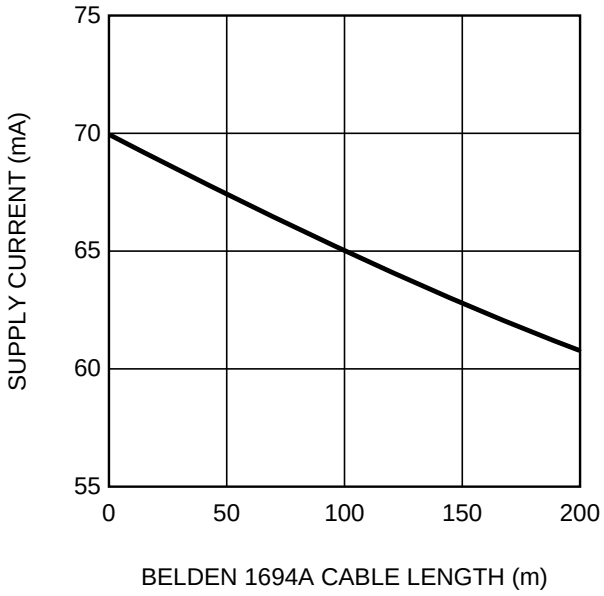

Figure 3. Supply Current vs. Belden 1694A Cable Length, 1.485 Gbps

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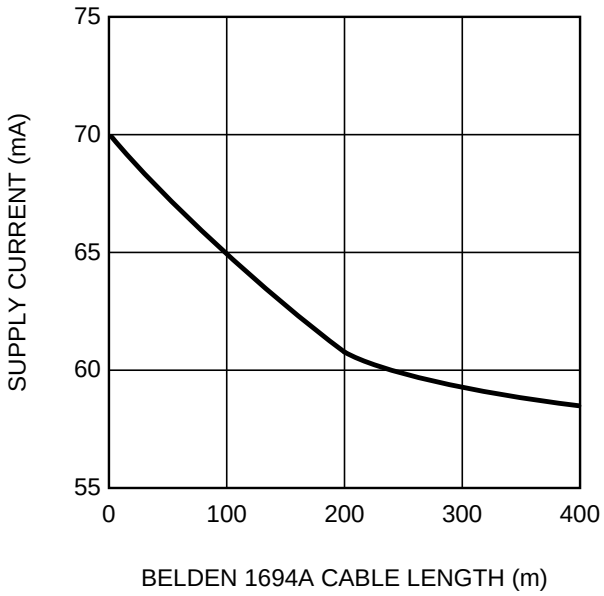

Figure 4. Supply Current vs. Belden 1694A Cable Length, 270 Mbps

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REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	7

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH0034MA/NOPB	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 85	L034
LMH0034MA/NOPB.A	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	0 to 85	L034
LMH0034MAX/NOPB	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 85	L034
LMH0034MAX/NOPB.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	0 to 85	L034

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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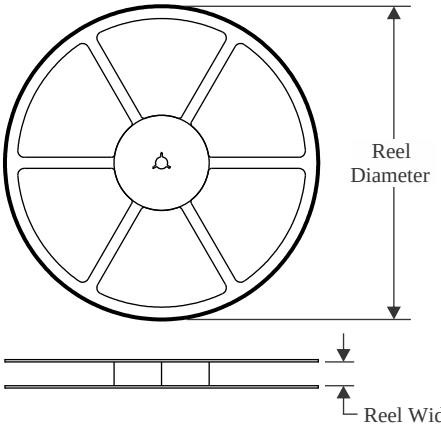
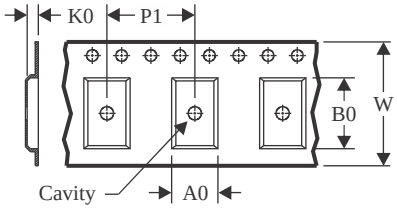
TAPE AND REEL INFORMATION

REEL DIMENSIONS

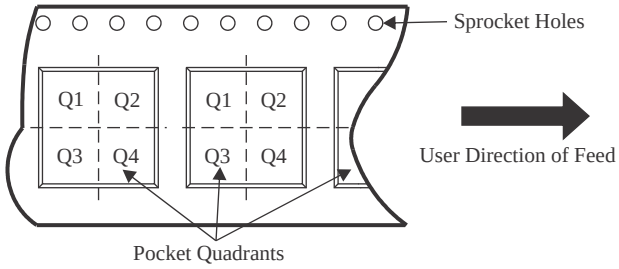


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

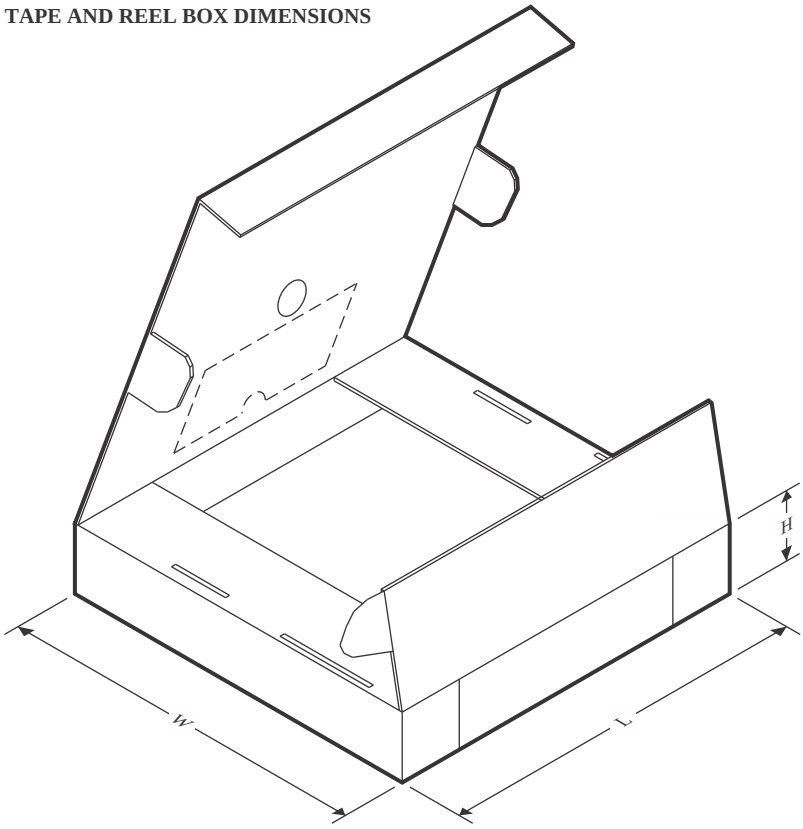
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0034MAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

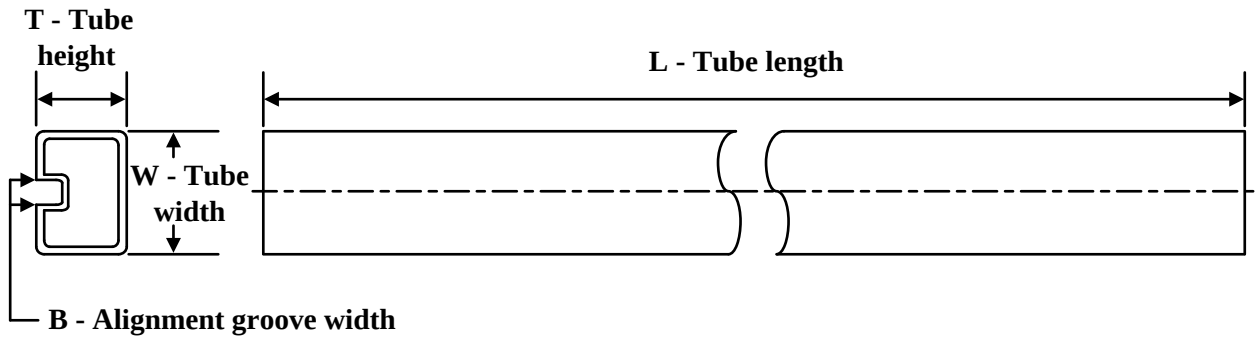
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0034MAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

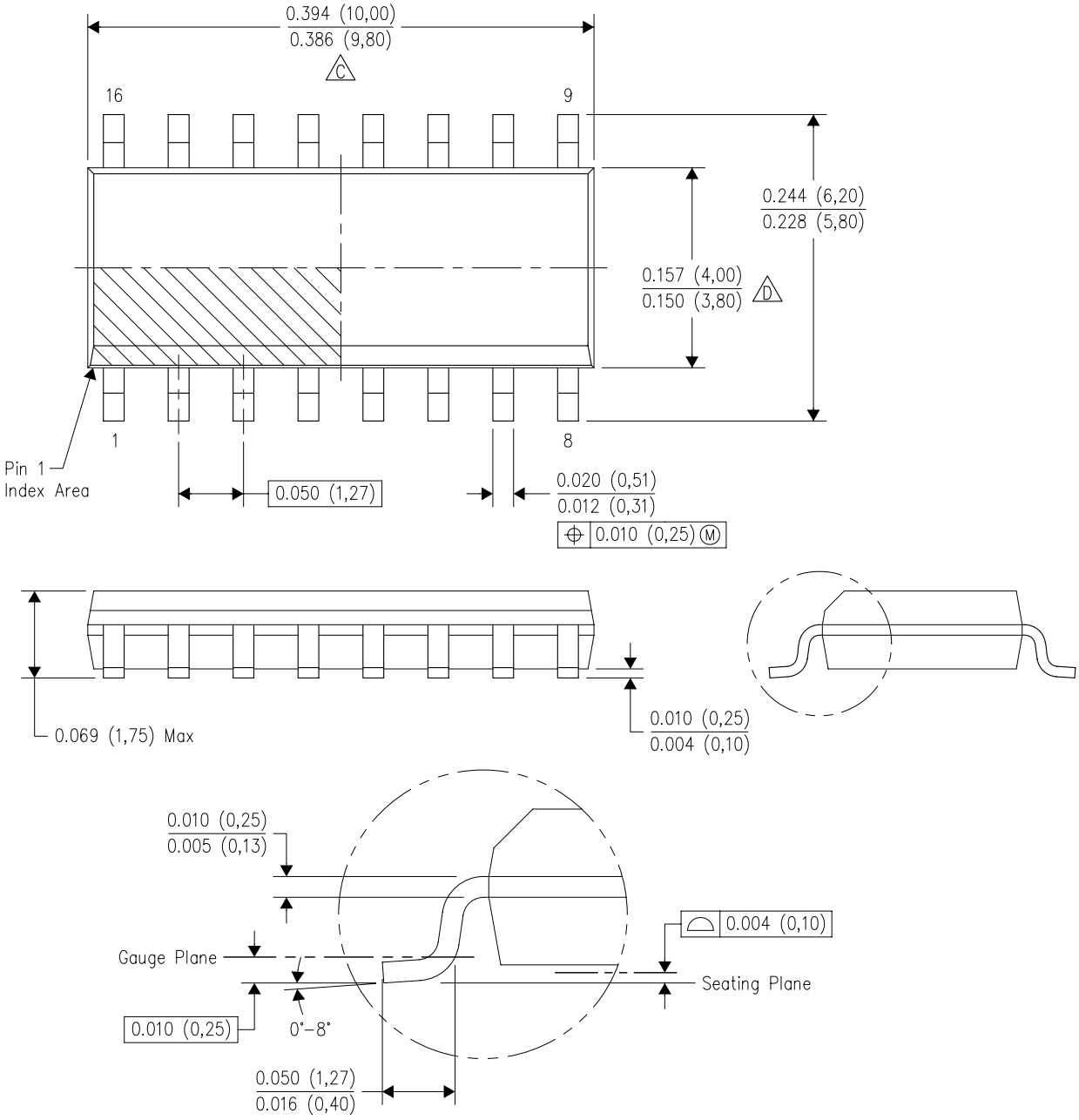
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH0034MA/NOPB	D	SOIC	16	48	495	8	4064	3.05
LMH0034MA/NOPB.A	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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