

## 14.2-Gbps Quad Channel, Dual Mode Linear Equalizer

Check for Samples: [SN65LVCP1414](#)

### FEATURES

- **Quad Channel, Uni-Directional, Multi-Rate, Dual-Mode Linear Equalizer with Operation up to 14.2Gbps Serial Data Rate for Backplane and Cable Interconnects**
- **Linear Equalization Increases Link Margin for Systems Implementing Decision Feedback Equalizers (DFE)**
- **17dB Analog Equalization at 7.1GHz with 1dB Step Control for Backplane Mode or Cable Mode**
- **Output Linear Dynamic Range: 1200mV**
- **Bandwidth: >20GHz – Typical**
- **Better than 15dB Return Loss at 7.1GHz**
- **Supports Out-of-Band (OOB) Signaling**
- **Low Power, Typically 80mW per Channel at 2.5V VCC**
- **38-Terminal QFN (Quad Flatpack, No-Lead) 5 mm x 7 mm x 0.75 mm, 0.5 mm Terminal Pitch**
- **Excellent Impedance Matching to 100Ω Differential PCB Transmission Lines**
- **GPIO or I<sup>2</sup>C Control**
- **2.5V and 3.3V±5% Single Power Supply**
- **2kV ESD (HBM)**
- **Flow-Through Pin-Out Provides Ease of Routing**
- **Small Package Size Saves Board Space**
- **Low Power**

### APPLICATIONS

- **High Speed Links in Telecommunication and Data Communication**
- **Backplane and Cable Interconnects for 10GbE, 16GFC, 10G SONET, SAS, SATA, CPRI, OBSAI, Infiniband, 10GBase-KR, and XFI/SFI**

### DESCRIPTION

The SN65LVCP1414 is an asynchronous, protocol-agnostic, low latency, four-channel linear equalizer optimized for use up to 14.2Gbps and compensates for losses in backplane or active cable applications. The architecture of the SN65LVCP1414 is designed to work with an ASIC or FPGA with digital equalization employing Decision Feedback Equalizers (DFE). The SN65LVCP1414 linear equalizer preserves the shape of the transmitted signal ensuring optimum DFE performance. The SN65LVCP1414 provides a low power solution while at the same time extending the effectiveness of DFE.

The SN65LVCP1414 is configurable via I<sup>2</sup>C or GPIO interface. Using the I<sup>2</sup>C interface of the SN65LVCP1414 enables the user to control independently the Equalization, Path Gain, and Output Dynamic Range for each individual channel. In GPIO mode, Equalization, Path Gain, and Output Dynamic Range can be set for all channels using the GPIO Input pins.

The SN65LVCP1414 outputs can be disabled independently via I<sup>2</sup>C.

The SN65LVCP1414 operates from a single 2.5V or 3.3V power supply.

The package for the SN65LVCP1414 is a 38 pin 5-mm x 7-mm x 0.75-mm QFN (Quad Flat-pack No-lead) lead-free package with 0.5mm pitch and is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

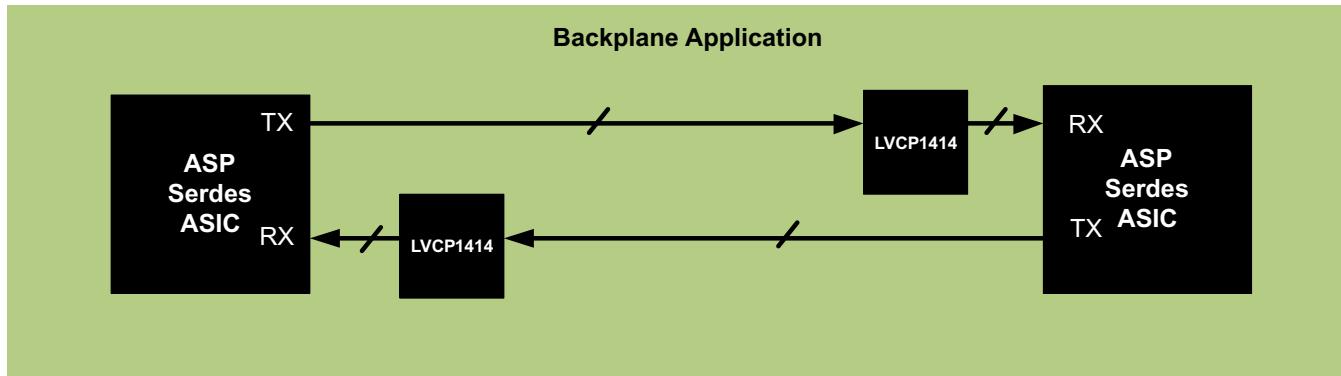


Figure 1. Typical Backplane Application – Trace Mode

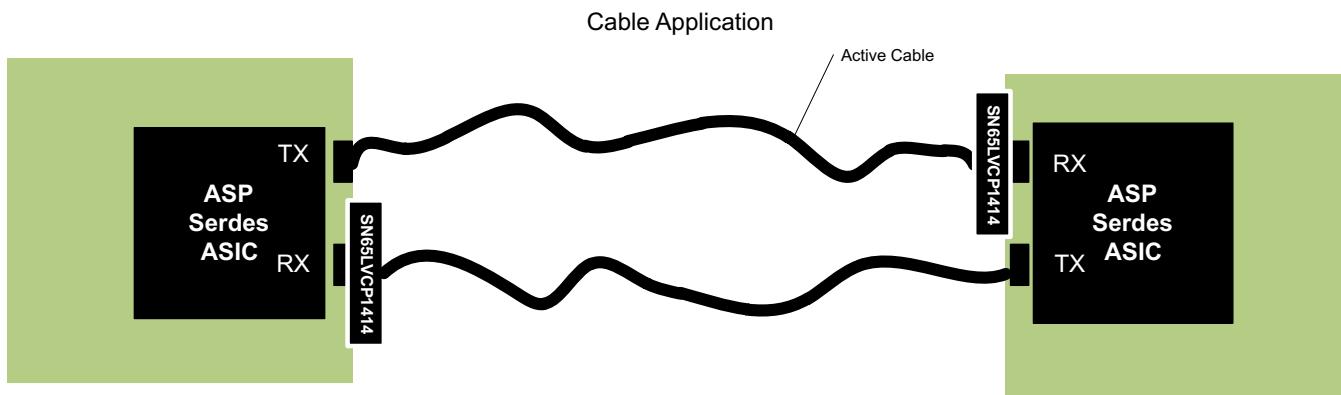
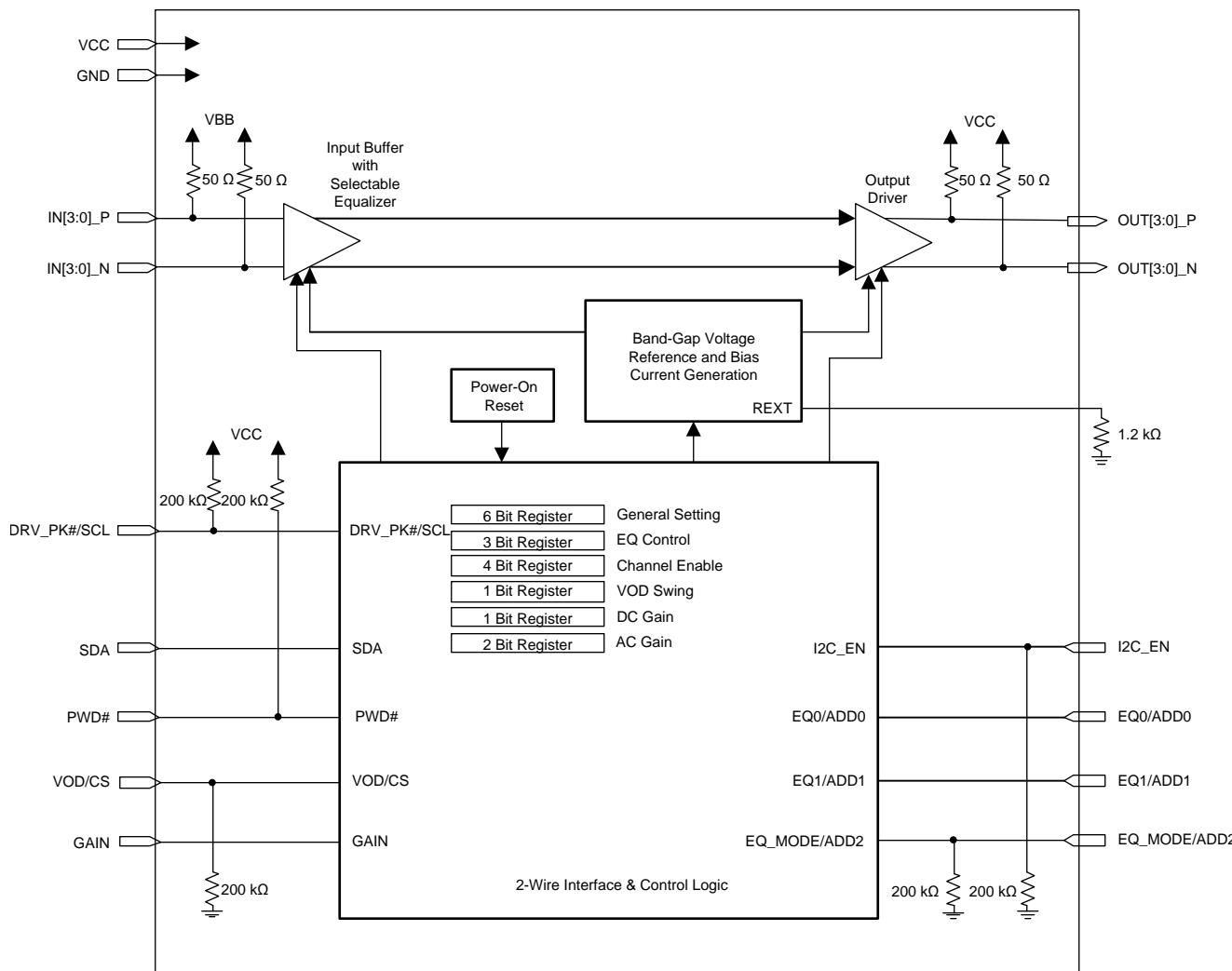


Figure 2. Typical Cable Application – Cable Mode

## Block Diagram (GPIO or I<sup>2</sup>C Mode)

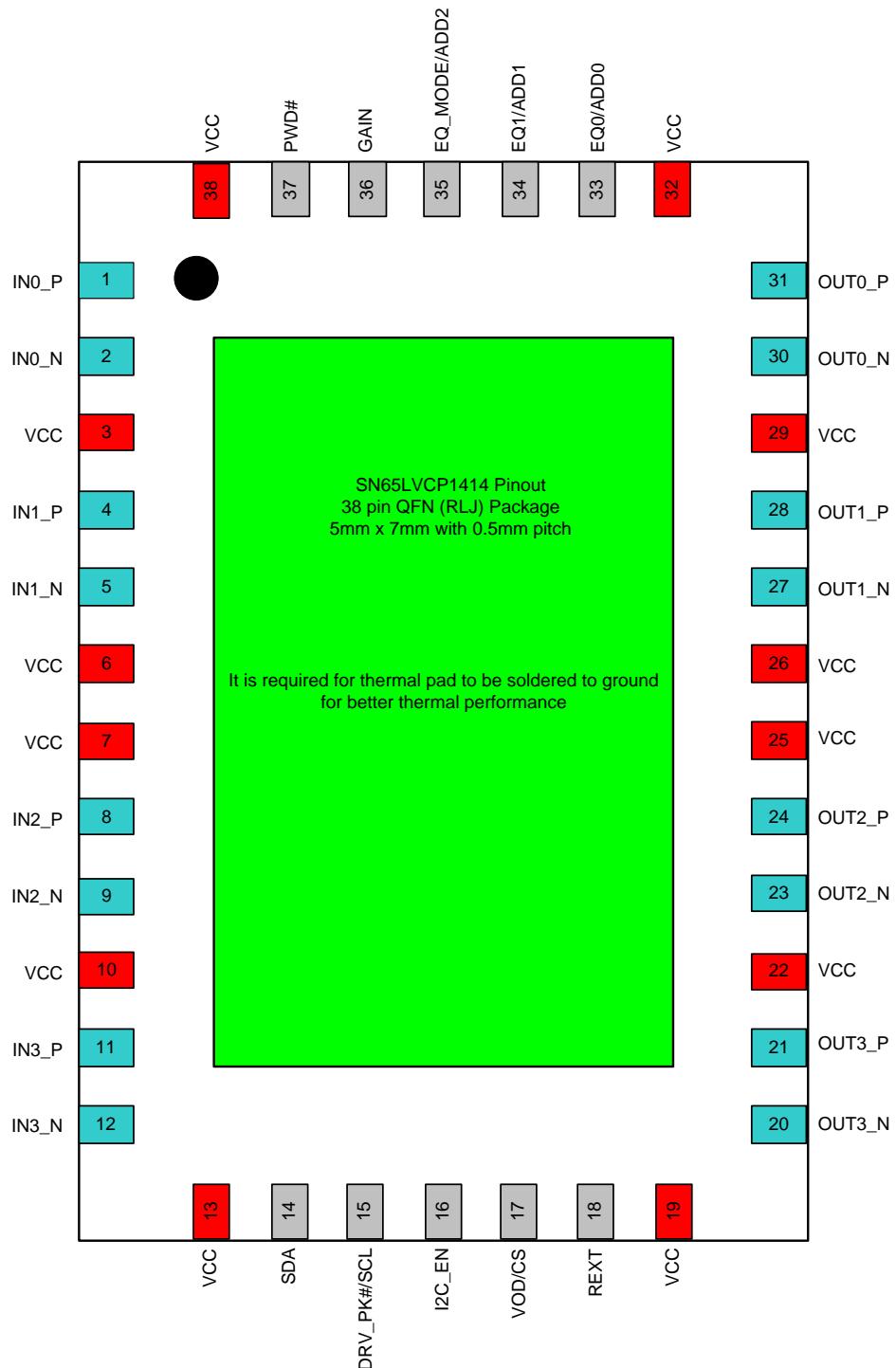
A simplified block diagram of the SN65LVCP1414 is shown in [Figure 3](#) for GPIO or I<sup>2</sup>C input control mode. This compact, low power, 14.2Gbps quad-channel dual-mode linear analog equalizer consists of four high-speed data paths and an input GPIO pin logic-control block and a two-wire interface with a control-logic block.



**Figure 3. Simplified Block Diagram of the SN65LVCP1414**

## Package

The package pin locations and assignments are shown in [Figure 4](#). The SN65LVCP1414 is packaged in a 5mm x 7mm x 0.75mm, 38 pin, 0.5mm pitch lead-free QFN.



**Figure 4. Package Drawing (Top View)**

**Pin Descriptions**

PINS		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	NO.			
<b>DIFFERENTIAL HIGH-SPEED I/O</b>				
IN0_P IN0_N	1 2	Input, (with 50 Ω termination to input common mode)	Differential input, lane 0	
IN1_P IN1_N	4 5	Input, (with 50 Ω termination to input common mode)	Differential input, lane 1	
IN2_P IN2_N	8 9	Input, (with 50 Ω termination to input common mode)	Differential input, lane 2	
IN3_P IN3_N	11 12	Input, (with 50 Ω termination to input common mode)	Differential input, lane 3	
OUT0_P OUT0_N	31 30	Output	Differential output, lane 0	
OUT1_P OUT1_N	28 27	Output	Differential output, lane 1	
OUT2_P OUT2_N	24 23	Output	Differential output, lane 2	
OUT3_P OUT3_N	21 20	Output	Differential output, lane 3	
<b>CONTROL SIGNALS</b>				
SDA	14	Input Output, Open drain	<b>GPIO mode</b> No action needed	<b>I<sup>2</sup>C mode</b> I <sup>2</sup> C data. Connect a 10kΩ pull-up resistor externally
DRV_PK#/SCL	15	Input. (with 200kΩ pull-up)	<b>GPIO mode</b> HIGH: disable Driver peaking LOW: enables Driver 6dB AC peaking	<b>I<sup>2</sup>C mode</b> I <sup>2</sup> C clock. Connect a 10kΩ pull-up resistor externally
I <sup>2</sup> C_EN	16	Input, (with 200kΩ pull-down) 2.5V/3.3V CMOS	Configures the device operation for I <sup>2</sup> C or GPIO mode: HIGH: enables I <sup>2</sup> C mode LOW: enables GPIO mode	
VOD/CS	17	Input, (with 200kΩ pull-down) 2.5V/3.3V CMOS	<b>GPIO mode</b> HIGH: set high VOD range LOW: set low VOD range	<b>I<sup>2</sup>C mode</b> HIGH: acts as Chip Select LOW: disables I <sup>2</sup> C interface
REXT	18	Input, Analog	External Bias Resistor: 1,200 Ω to GND	
EQ0/ADD0	33	Input, 2.5V/3.3V CMOS - 3-state	<b>GPIO mode</b> Working with EQ1 to determine input EQ gain.	<b>I<sup>2</sup>C mode</b> ADD0 along with pins ADD1 and ADD2 comprise the three bits of I <sup>2</sup> C slave address. ADD2:ADD1:ADD0:XXX

## Pin Descriptions (continued)

PINS		DIRECTION TYPE SUPPLY	DESCRIPTION																																
NAME	NO.																																		
EQ1/ADD1	34	Input, 2.5V/3.3V CMOS - 3-state	<b>GPIO mode</b> Working with EQ0 to determine input EQ gain steps of approximately 2dB <table border="1" data-bbox="605 388 899 734"> <tr> <th>EQ1</th> <th>EQ0</th> <th>EQ GAIN</th> </tr> <tr><td>GND</td><td>GND</td><td>000</td></tr> <tr><td>GND</td><td>HiZ</td><td>000</td></tr> <tr><td>GND</td><td>VCC</td><td>001</td></tr> <tr><td>HiZ</td><td>GND</td><td>010</td></tr> <tr><td>HiZ</td><td>HiZ</td><td>011</td></tr> <tr><td>HiZ</td><td>VCC</td><td>100</td></tr> <tr><td>VCC</td><td>GND</td><td>101</td></tr> <tr><td>VCC</td><td>HiZ</td><td>110</td></tr> <tr><td>VCC</td><td>VCC</td><td>111</td></tr> </table>	EQ1	EQ0	EQ GAIN	GND	GND	000	GND	HiZ	000	GND	VCC	001	HiZ	GND	010	HiZ	HiZ	011	HiZ	VCC	100	VCC	GND	101	VCC	HiZ	110	VCC	VCC	111	<b>I<sup>2</sup>C mode</b> ADD1 along with pins ADD0 and ADD2 comprise the three bits of I <sup>2</sup> C slave address ADD2:ADD1:ADD0:XXX	
EQ1	EQ0	EQ GAIN																																	
GND	GND	000																																	
GND	HiZ	000																																	
GND	VCC	001																																	
HiZ	GND	010																																	
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HiZ	VCC	100																																	
VCC	GND	101																																	
VCC	HiZ	110																																	
VCC	VCC	111																																	
			EQ1 and EQ0 works with AC_GAIN and DC_GAIN to determine final EQ gain as this: <table border="1" data-bbox="605 798 1008 967"> <tr> <th>EQ1/ EQ0</th> <th>GAIN</th> <th>DC GAIN (dB)</th> <th>EQ GAIN (dB)</th> </tr> <tr><td>000 ~ 111</td><td>LOW</td><td>-6</td><td>1 ~ 9</td></tr> <tr><td>000 ~ 111</td><td>HiZ</td><td>-6</td><td>7 ~ 17</td></tr> <tr><td>000 ~ 111</td><td>HiGH</td><td>0</td><td>1 ~ 9</td></tr> </table>	EQ1/ EQ0	GAIN	DC GAIN (dB)	EQ GAIN (dB)	000 ~ 111	LOW	-6	1 ~ 9	000 ~ 111	HiZ	-6	7 ~ 17	000 ~ 111	HiGH	0	1 ~ 9																
EQ1/ EQ0	GAIN	DC GAIN (dB)	EQ GAIN (dB)																																
000 ~ 111	LOW	-6	1 ~ 9																																
000 ~ 111	HiZ	-6	7 ~ 17																																
000 ~ 111	HiGH	0	1 ~ 9																																
EQ_MODE/ ADD2	35	Input, (with 200kΩ pull-down), 2.5V/3.3V CMOS	<b>GPIO mode</b> HIGH: Trace mode LOW: Cable mode	<b>I<sup>2</sup>C mode</b> ADD2 along with pins ADD1 and ADD0 comprise the three bits of I <sup>2</sup> C slave address. ADD2:ADD1:ADD0:XXX																															
GAIN	36	Input, 2.5V/3.3V CMOS - 3-state	<b>GPIO mode</b> Work with EQ1/EQ0 to set total EQ Gain. See table above.	<b>I<sup>2</sup>C mode</b> No action needed																															
PWD#	37	Input, (with 200kΩ pull-up), 2.5V/3.3V CMOS	HIGH: Normal Operation LOW: Power downs the device, inputs off and outputs disabled, resets I <sup>2</sup> C																																
<b>POWER SUPPLY</b>																																			
VCC	3, 6, 7, 10, 13, 19, 22, 25, 26, 29, 32, 38	Power	Power supply 2.5V±5%, 3.3V±5%																																
GND Center Pad		Ground	The ground center pad is the metal contact at the bottom of the package. This pad must be connected to the GND plane. At least 15 PCB vias are recommended to minimize inductance and provide a solid ground. Refer to the package drawing (RLJ-package) for the via placement.																																

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUES	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	-0.3 to 4	V
$V_{IN,DIFF}$	Differential voltage between $IN_x_P$ and $IN_x_N$	$\pm 2.5$	V
$V_{IN+}, V_{IN-}$	Voltage at $IN_x_P$ and $IN_x_N$	-0.5 V to $V_{CC}+0.5$	V
$V_{IO}$	Voltage on control IO pins	-0.5 V to $V_{CC}+0.5$	V
$I_{IN+}, I_{IN-}$	Continuous current at high speed differential data inputs (differential)	-25 to 25	mA
$I_{OUT+}, I_{OUT-}$	Continuous current at high speed differential data outputs	-25 to 25	mA
ESD	Human Body Model <sup>(3)</sup> (All Pins)	2.0	kV
	Charged-Device Model <sup>(4)</sup> (All Pins)	500	V
Moisture sensitivity level		3	
Reflow temperature package soldering, 4 sec		260	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65LVCP1414	UNITS
	RLJ (38 PINS)		°C/W
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	36.9	
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	22.3	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	10.7	
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	0.3	
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	10.6	
$\theta_{JCbot}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	1.9	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\Psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\Psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
dR	Operating data rate			14.2	Gbps
V <sub>CC</sub>	Supply voltage	2.375	2.5	2.625	V
V <sub>CC</sub>	Supply voltage	3.135	3.3	3.465	V
TC	Junction temperature	-10		125	°C
TB	Maximum board temperature			85	°C
<b>CMOS DC SPECIFICATIONS</b>					
V <sub>IH</sub>	High-level input voltage	0.8×V <sub>CC</sub>			V
V <sub>MID</sub>	Mid-level input voltage	V <sub>CC</sub> ×0.4	V <sub>CC</sub> ×0.6		V
V <sub>IL</sub>	Low-level input voltage	-0.5	0.2×V <sub>CC</sub>		V
PSNR BG	Bandgap circuit PSNR	20			dB

## Electrical Characteristics (VCC 2.5V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>POWER CONSUMPTION</b>					
PD <sub>L</sub>	Device power dissipation	317	475		mW
PD <sub>H</sub>	Device power dissipation	485	675		mW
PD <sub>OFF</sub>	Device power with all 4 channels switched off	10			mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

## Electrical Characteristics (VCC 3.3V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>POWER CONSUMPTION</b>					
PD <sub>L</sub>	Device power dissipation	450	625		mW
PD <sub>H</sub>	Device power dissipation	697	925		mW
PD <sub>OFF</sub>	Device power with all 4 channels switched off	10			mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

## Electrical Characteristics (VCC 2.5V ±5%, 3.3V ±5%)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>CMOS DC SPECIFICATIONS</b>					
I <sub>IH</sub>	VIN = 0.9 × V <sub>CC</sub>	-40	17	40	µA
I <sub>IL</sub>	VIN = 0.1 × V <sub>CC</sub>	-40	17	40	µA
<b>CML INPUTS (IN[3:0]_P, IN[3:0]_N)</b>					
r <sub>IN</sub>	INx_P to INx_N	100			Ω
V <sub>IN</sub>	Gain = 0.5	1200			mV <sub>pp</sub>
V <sub>ICM</sub>	Internally biased	V <sub>CC</sub> -0.8			V
SCD11	Input differential to common mode conversion	-20			dB
SDD11	Differential input return loss	-15			dB

(1) All typical values are at 25°C and with 2.5V and 3.3V supply unless otherwise noted.

## Electrical Characteristics (VCC 2.5V $\pm$ 5%, 3.3V $\pm$ 5%) (continued)

over operating free-air temperature range, all parameters are referenced to package pins (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)</b>					
V <sub>OD</sub>	R <sub>L</sub> = 100 $\Omega$ , V <sub>OD</sub> = HIGH		1200		mV <sub>pp</sub>
	R <sub>L</sub> = 100 $\Omega$ , V <sub>OD</sub> = LOW		600		mV <sub>pp</sub>
V <sub>OS</sub>	R <sub>L</sub> = 100 $\Omega$ , 0 V applied at inputs		10		mV <sub>pp</sub>
V <sub>OCM</sub>	See <a href="#">Figure 5</a>		V <sub>CC</sub> -0.4		V
V <sub>CM,RIP</sub>	K28.5 pattern at 14.2Gbps on all 4 channels, No interconnect loss, VOD = HIGH		10	20	mV <sub>RMS</sub>
V <sub>OD,RIP</sub>	K28.5 pattern at 14.2Gbps on all channels, No interconnect loss, VIN = 1200mVpp.			20	mV <sub>pp</sub>
V <sub>OC(ss)</sub>	Change in steady-state common-mode output voltage between logic states		$\pm$ 10		mV
t <sub>R</sub>	Rise time <sup>(2)</sup>	Input signal with 30ps rise time, 20% to 80%, See <a href="#">Figure 7</a>	31		ps
t <sub>F</sub>	Fall time <sup>(2)</sup>	Input signal with 30ps fall time, 20% to 80%, See <a href="#">Figure 7</a>	32		ps
SDD22	Differential output return loss	100MHz to 7.1GHz		-15	dB
SCC22	Common-mode output return loss	100MHz to 7.1GHz		-5	dB
t <sub>PLH</sub>	Low-to-high propagation delay	See <a href="#">Figure 6</a>	65		ps
t <sub>PHL</sub>	High-to-low propagation delay		65		ps
t <sub>SK(O)</sub>	Inter-Pair (lane to lane) output skew <sup>(3)</sup>	All outputs terminated with 100 $\Omega$ , See <a href="#">Figure 8</a>	8		ps
t <sub>SK(PP)</sub>	Part-to-part skew <sup>(4)</sup>	All outputs terminated with 100 $\Omega$		50	ps
r <sub>OT</sub>	Single ended output resistance	Single ended on-chip termination to VCC, Outputs will be AC coupled		50	$\Omega$
r <sub>OM</sub>	Output termination mismatch at 1MHz	$\Delta r_{OM} = 2 \times \frac{rp - rn}{rp + rn} \times 100$		5	%
Ch <sub>iso</sub>	Channel-to-channel isolation	Frequency at 7.1GHz	35	45	dB
OUT <sub>NOISE</sub>	Output referred noise <sup>(5)</sup>	10MHz to 7.1GHz, No other noise source present, VOD = LOW		400	$\mu$ VRMS
		10MHz to 7.1GHz, No other noise source present, VOD = HIGH		500	$\mu$ VRMS
<b>EQUALIZATION</b>					
EQ <sub>Gain</sub>	At 7.1GHz input signal	Equalization Gain, EQ = MAX	15	17	dB
V <sub>pre</sub>	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measure it on the output signal, Refer <a href="#">Figure 9</a> . V <sub>pre</sub> = 20log(V3/V2)		3.75	dB
V <sub>pst</sub>	Output post-cursor pre-emphasis	Input signal with 12dB post-cursor and measure it on the output signal, Refer <a href="#">Figure 9</a> , V <sub>pst</sub> = 20log(V1/V2)		12	dB
DJ1	Residual deterministic jitter at 10.3125 Gbps	Transmit Side application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel $\rightarrow$ 0", See <a href="#">Figure 11</a>		0.016	Ulp-p
DJ2	Residual deterministic jitter at 10.3125 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel $\rightarrow$ 12" (9dB loss at 5GHz), See <a href="#">Figure 10</a>		0.11	Ulp-p
DJ3	Residual deterministic jitter at 14.2 Gbps	Transmit Side Application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel $\rightarrow$ 0", See <a href="#">Figure 11</a>		0.041	Ulp-p
DJ4	Residual deterministic jitter at 14.2 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel $\rightarrow$ 8" (9dB loss at 7GHz), See <a href="#">Figure 10</a>		0.13	Ulp-p

(2) Rise and Fall measurements include board and channel effects of the test environment, refer to [Figure 10](#) and [Figure 11](#).

(3) t<sub>SK(O)</sub> is the magnitude of the time difference between the channels.

(4) t<sub>SK(PP)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(5) All noise sources added.

### Parameter Measurement Information

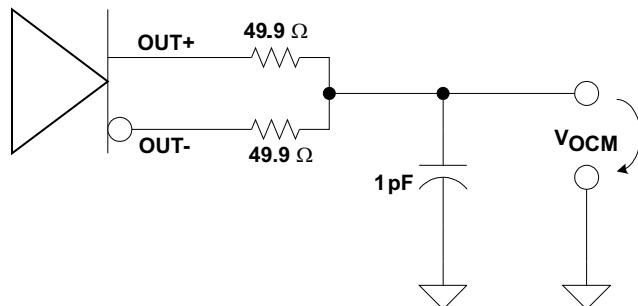


Figure 5. Common Mode Output Voltage Test Circuit

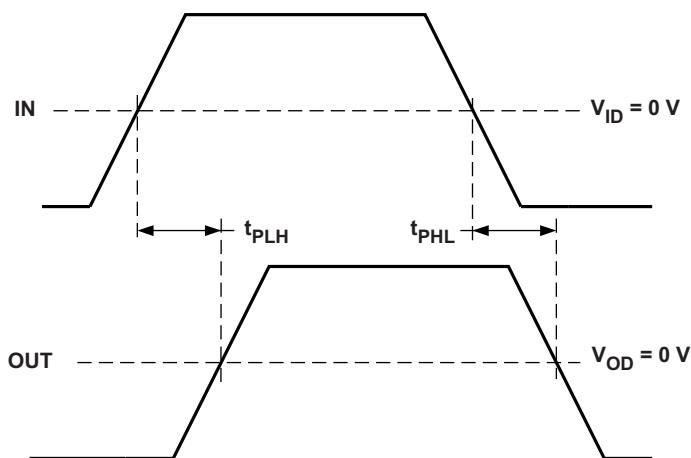


Figure 6. Propagation Delay Input to Output

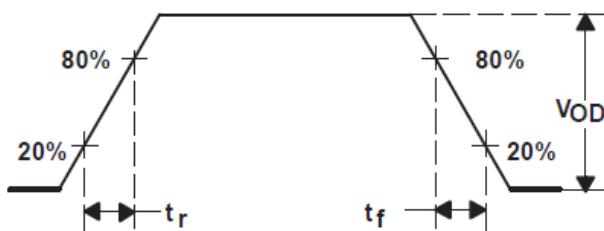


Figure 7. Output Rise and Fall Times

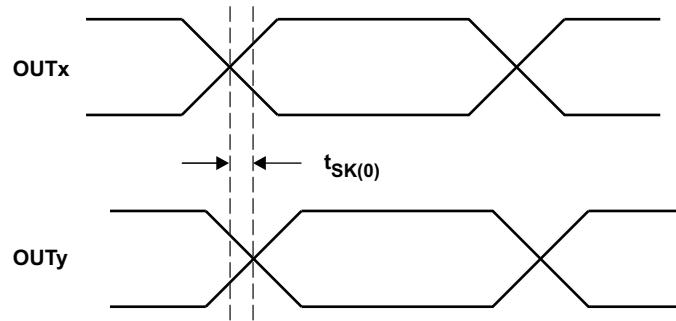


Figure 8. Output Inter-Pair Skew

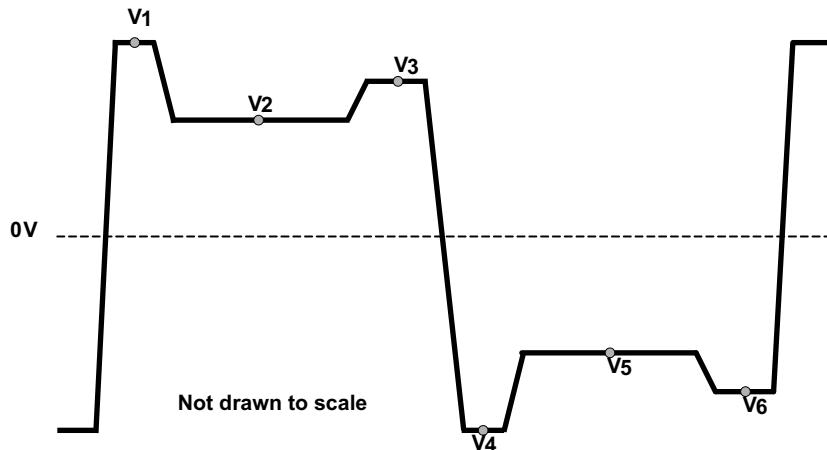
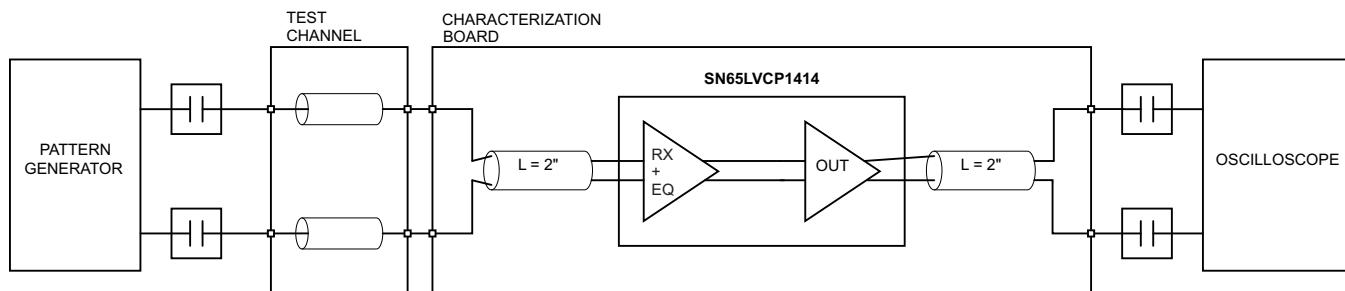
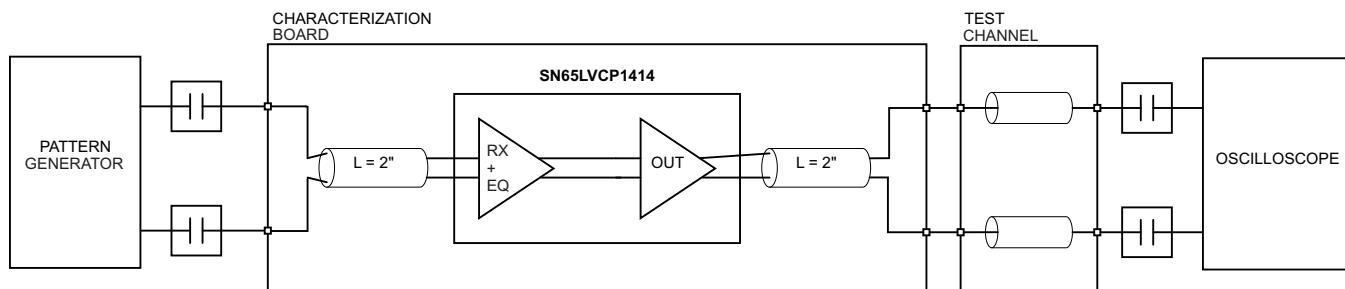


Figure 9. Vpre and Vpost (test pattern is 1111111100000000 (8-1s, 8-0s))



**Figure 10. Receive Side Performance Test Circuit**



**Figure 11. Transmit Side Performance Test Circuit**

## Equivalent Input and Output Schematic Diagrams

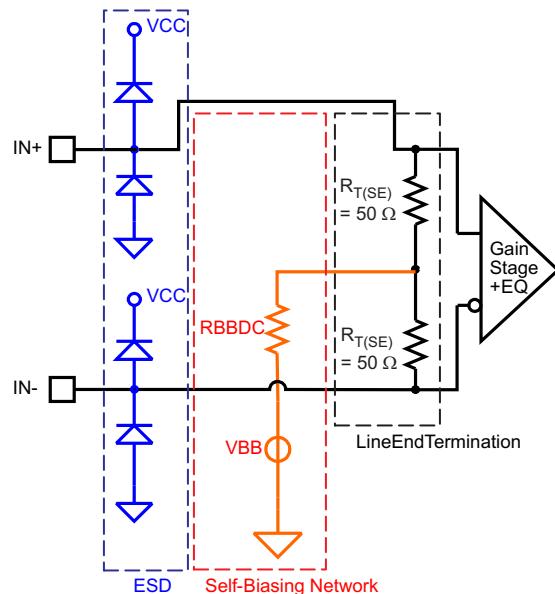


Figure 12. Equivalent Input Circuit Design

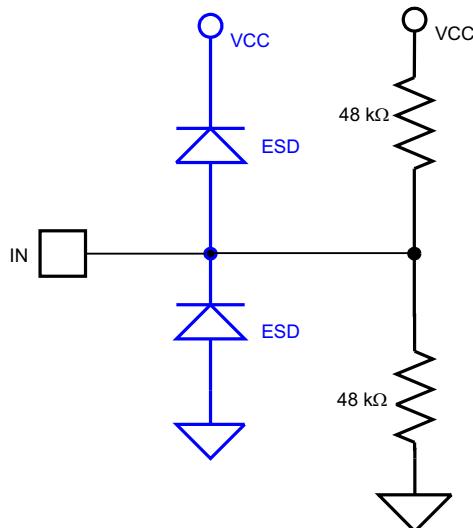
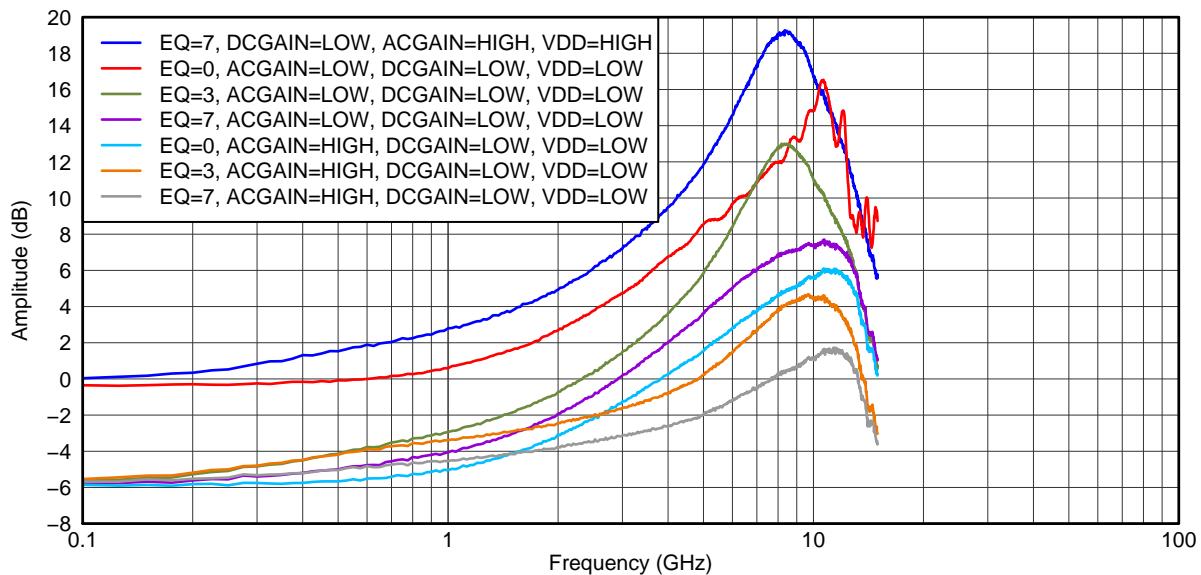


Figure 13. 3-Level Input Biasing Network

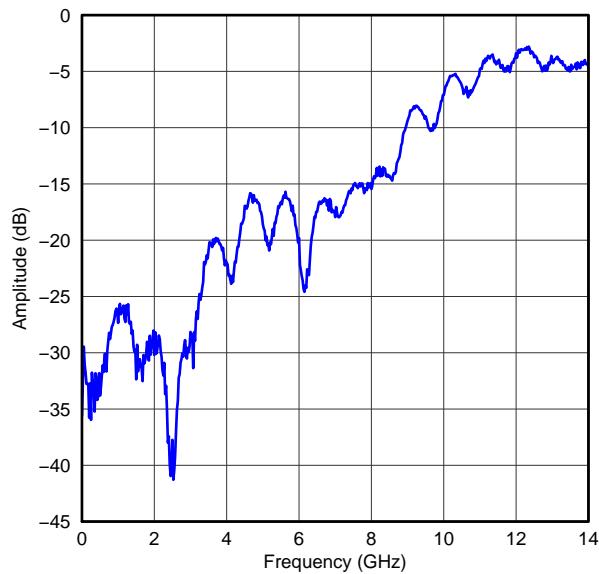
### Typical Characteristics

Typical operating condition is at  $V_{CC} = 2.5V$  and  $T_A = 25^\circ C$ , no interconnect line at the output, and with default device settings (unless otherwise noted).



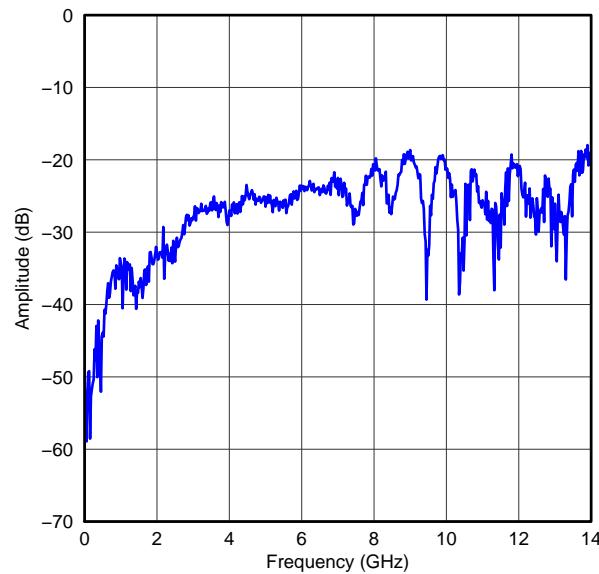
**Figure 14. Typical EQ Gain Profile Curve**

G001



**Figure 15. Differential Input Return Loss**

G002

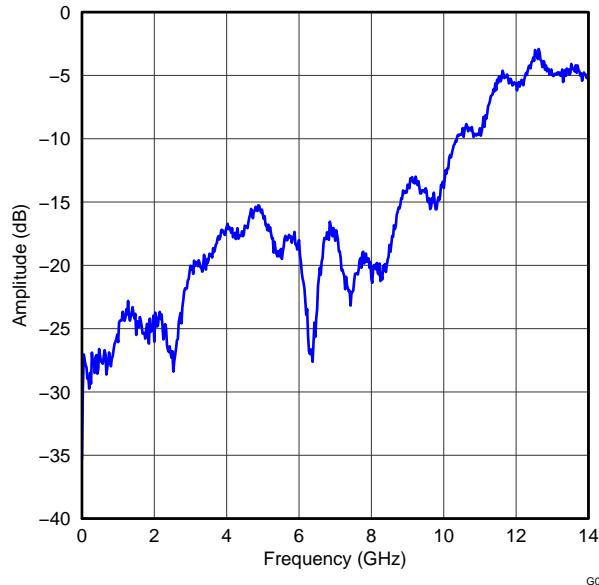


**Figure 16. Differential to Common Mode Conversion**

G003

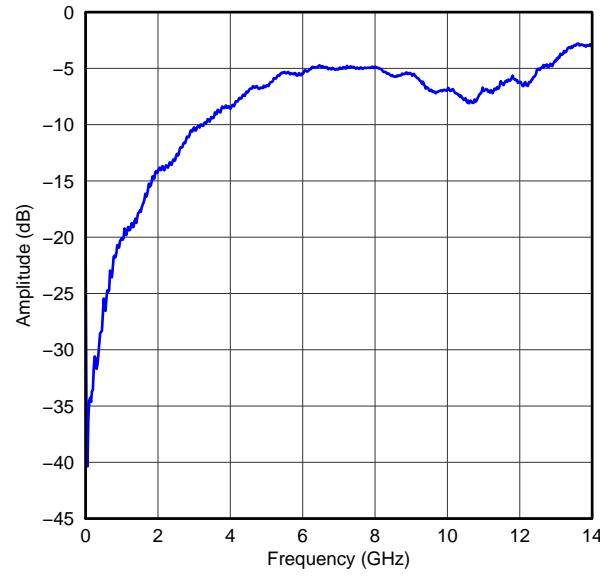
### Typical Characteristics (continued)

Typical operating condition is at  $V_{CC} = 2.5V$  and  $T_A = 25^\circ C$ , no interconnect line at the output, and with default device settings (unless otherwise noted).



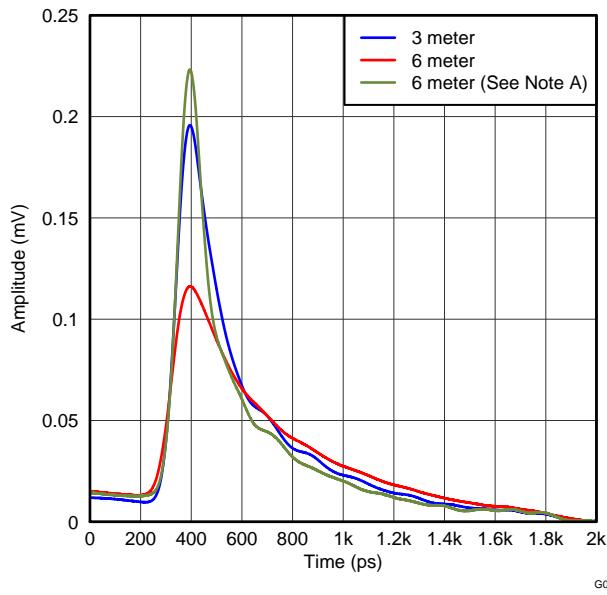
G004

Figure 17. Differential Output Return Loss



G005

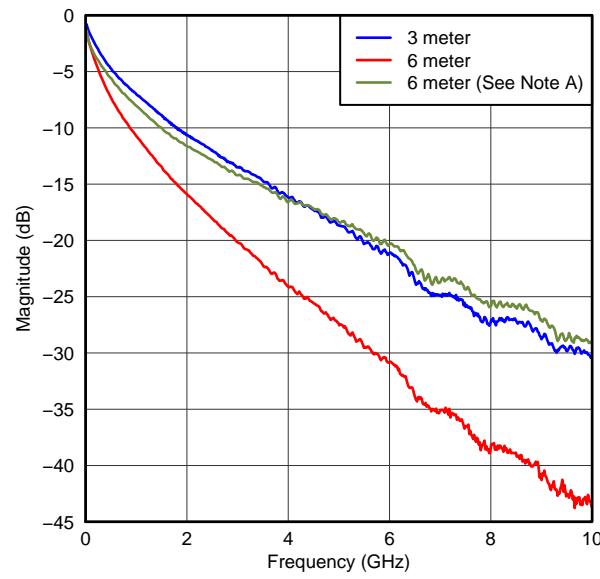
Figure 18. Common Mode Output Return Loss



G006

A. With SN65LVCP1414 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 19. Cable Mode – Symbol Response



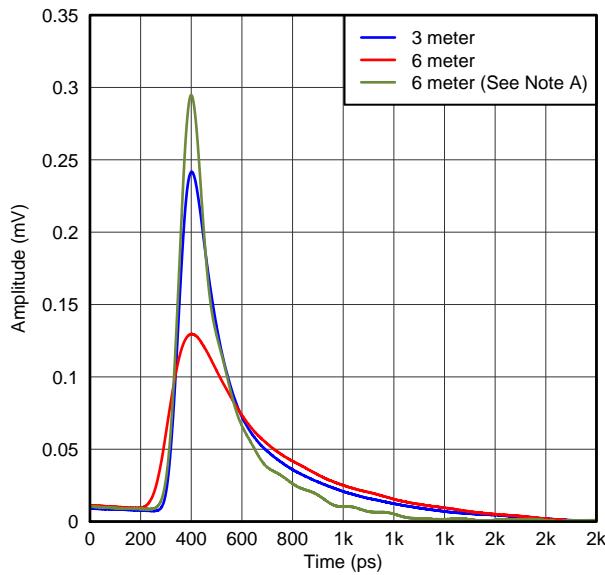
G007

A. With SN65LVCP1414 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 20. Cable Mode – Frequency Domain

### Typical Characteristics (continued)

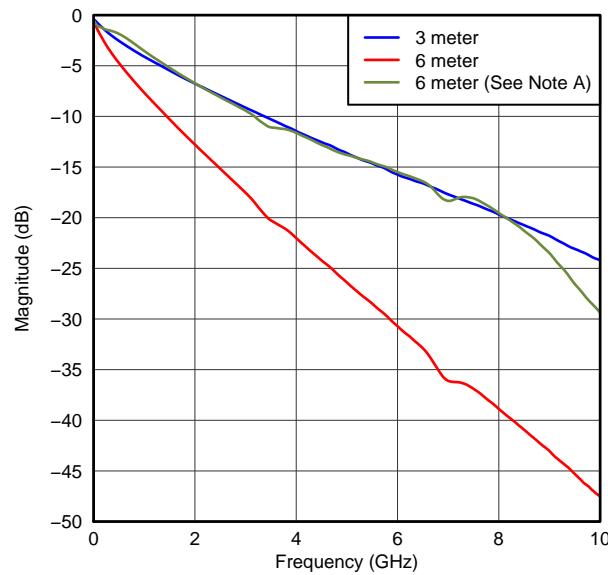
Typical operating condition is at  $V_{CC} = 2.5V$  and  $T_A = 25^\circ C$ , no interconnect line at the output, and with default device settings (unless otherwise noted).



G008

A. With SN65LVCP1414 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 21. Trace Mode – Symbol Response



G009

A. With SN65LVCP1414 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 22. Trace Mode - Frequency Domain

**Table 1. Control Settings Descriptions**

MODE	DCGAIN	ACGAIN<1:0>	EQ<2:0>	DC GAIN (dB)	EQ GAIN (dB)	APPLICATION
0	0	0	000 to 111	-6	1 to 9	Short Input Trace; Large Input Swing
0	0	11	000 to 111	-6	7 to 17	Long Input Trace; Large Input Swing
0	1	1	000 to 111	0	1 to 9	Short Input Trace; Small Input Swing
0	1	11	000 to 111	0	2 to 10	Short Input Trace; Small Input Swing
1	0	0	000 to 111	-6	1 to 9	Short Input Cable; Large Input Swing
1	0	11	000 to 111	-6	7 to 17	Long Input Cable; Large Input Swing
1	1	1	000 to 111	0	1 to 9	Short Input Cable; Small Input Swing
1	1	11	000 to 111	0	2 to 10	Short Input Cable; Small Input Swing

**Table 2. Control Settings Descriptions**

GAIN	DC GAIN	ACGAIN<1:0>
Low	0	00
HighZ	0	11
High	1	01

## Two-Wire Serial Interface and Control Logic

The SN65LVCP1414 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. The SDA and SCK pins require external  $10\text{k}\Omega$  pull-ups to VCC.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The SN65LVCP1414 is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0000ADD[2:0]) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7 bit slave address is 0000000.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the SN65LVCP1414 is I<sup>2</sup>C compatible. The typical timing is shown in [Figure 9](#) and a complete data transfer is shown in [Figure 10](#). Parameters for [Figure 9](#) are defined in [Table 3](#).

**Bus Idle:** Both SDA and SCL lines remain HIGH

**Start Data Transfer:** A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

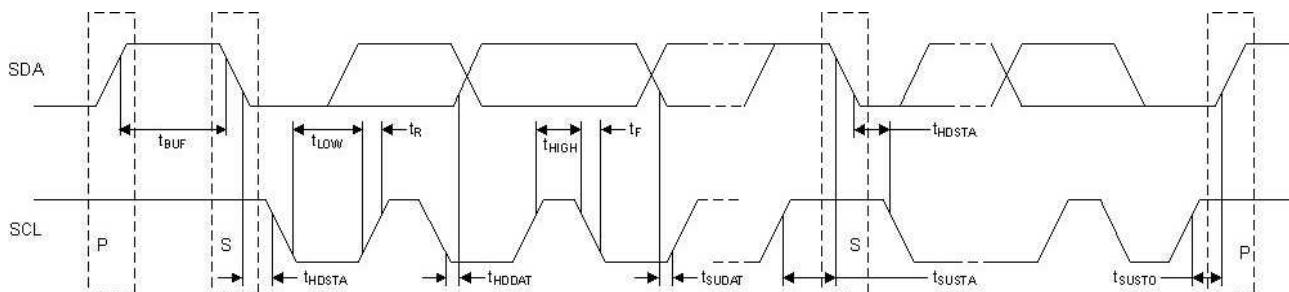
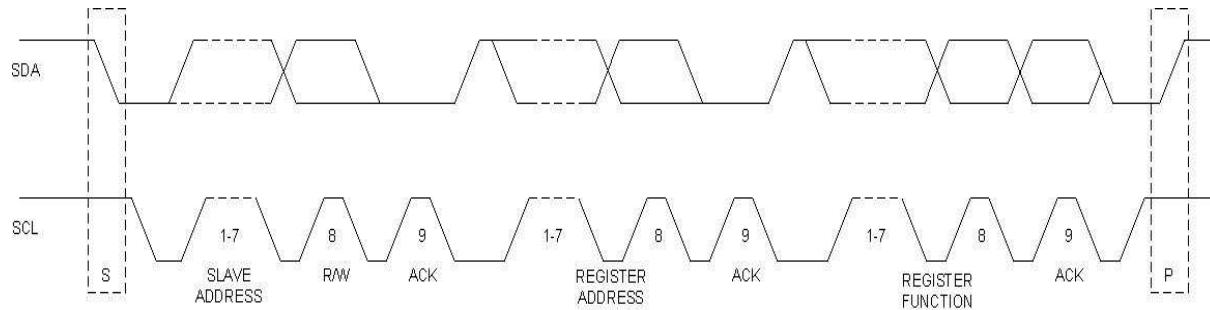


Figure 23. Two-Wire Serial Interface Timing Diagram

**Table 3. Two-Wire Serial Interface Timing Diagram Definitions**

SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{SCL}$	SCL clock frequency		400	kHz
$t_{BUF}$	Bus free time between START and STOP conditions	1.3		$\mu$ s
$t_{HDSTA}$	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		$\mu$ s
$t_{LOW}$	Low period of the SCL clock	1.3		$\mu$ s
$t_{HIGH}$	High period of the SCL clock	0.6		$\mu$ s
$t_{SUSTA}$	Setup time for a repeated START condition	0.6		$\mu$ s
$t_{HDDAT}$	Data HOLD time	0		$\mu$ s
$t_{SUDAT}$	Data setup time	100		ns
$t_R$	Rise time of both SDA and SCL signals		300	ns
$t_F$	Fall time of both SDA and SCL signals		300	ns
$t_{SUSTO}$	Setup time for STOP condition	0.6		$\mu$ s


**Figure 24. Two-Wire Serial Interface Data Transfer**

## Register Mapping

The register mapping for read/write register addresses 0 (0x00) through 22 (0x18) are shown in [Table 4](#). [Table 5](#) describes the circuit functionality based on the register settings.

**Table 4. SN65LVCP1414 Register Mapping Information**

Register 0x00 (General Device Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SW_GPIO	PWRDOWN	SYNC_01	SYNC_23	SYNC_ALL	EQ_MODE		RSVD
Register 0x01 (Channel Enable) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
				LN_EN_CH3	LN_EN_CH2	LN_EN_CH1	LN_EN_CH0
Register 0x02 (Channel 0 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x03 (Channel 0 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x05 (Channel 1 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x06 (Channel 1 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x08 (Channel 2 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x09 (Channel 2 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x0B (Channel 3 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0
Register 0x0C (Channel 3 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN
Register 0x0F Read Only							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Register 0x11 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	RSVD						
Register 0x12 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD							

**Table 5. SN65LVCP1414 Register Description**

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT	
0x00	7	SW_GPIO	Switching logic is controlled by GPIO or I <sup>2</sup> C: 0 = I <sup>2</sup> C control 1 = GPIO control	00000000	
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Powerdown		
	5	SYNC_01	All settings from channel 1 will be used for channel 0 and 1: 0 = Channel 0 tracking channel 1 settings 1 = No tracking tracking		
	4	SYNC_23	All settings from channel 2 will be used for channel 2 and 3: 0 = Channel 3 tracking channel 2 settings 1 = No channel tracking		
	3	SYNC_ALL	All settings from channel 1 will be used on all channels: 0 = All channels tracking channel 1 1 = No channel tracking Overwrites SYNC_01 and SYNC_23		
	2	EQ_MD	Set EQ mode: 0 = Cable mode 1 = Trace mode		
	1				
	0	RSVD	For TI use only		
0x01	7			00000000	
	6				
	5				
	4				
	3	LN_EN_CH3	Channel 3 enable: 0 = Enable 1 = Disable		
	2	LN_EN_CH2	Channel 2 enable: 0 = Enable 1 = Disable		
	1	LN_EN_CH1	Channel 1 enable: 0 = Enable 1 = Disable		
	0	LN_EN_CH0	Channel 0 enable: 0 = Enable 1 = Disable		
0x02 0x05 0x08 0x0B	7	RSVD		00000000	
	6	EQ2	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting		
	5	EQ1			
	4	EQ0			
	3	VOD_CTRL	Channel [x] VOD control: 0 = Low VOD range 1 = High VOD range		
	2	DC_GAIN_CTRL	Channel [x] EQ DC gain: 0 = Set EQ DC gain to 0.5x 1 = Set EQ DC gain to 1x		
	1	AC_GAIN_CTRL1	AC Gain Control: 00 = Low 01 = HiZ 11 = High		
	0	AC_GAIN_CTRL0			

Table 5. SN65LVCP1414 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x03 0x06 0x09 0x0C	7			00000000
	6			
	5			
	4			
	3			
	2	DRV_PEAK	Channel [x] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6db AC Peaking	
	1	EQ_EN	Channel [x] EQ stage enable: 0 = Enable 1 = Disable	
	0	DRV_EN	Channel [x] driver stage enable: 0 = Enable 1 = Disable	
	7	RSVD	For TI use only	
	6	RSVD	For TI use only	
0x0F	5	RSVD	For TI use only	00110000
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	
	7			
	6	RSVD	For TI use only	
0x11	5			00000000
	4			
	3			
	2			
	1			
	0			
	7	RSVD	For TI use only	
	6			
0x12	5			00000000
	4			
	3			
	2			
	1			
	0			

## REVISION HISTORY

<b>Changes from Original (August 2012) to Revision A</b>	<b>Page</b>
• Changed OUT2_P pin number from 23 to 24 .....	5
• Changed OUT2_N pin number from 24 to 23 .....	5
• Changed OUT3_P pin number from 20 to 21 .....	5
• Changed OUT3_N pin number from 21 to 20 .....	5

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVCP1414RLJT	Obsolete	Production	WQFN (RLJ)   38	-	-	Call TI	Call TI	-40 to 85	LVCP 1414

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

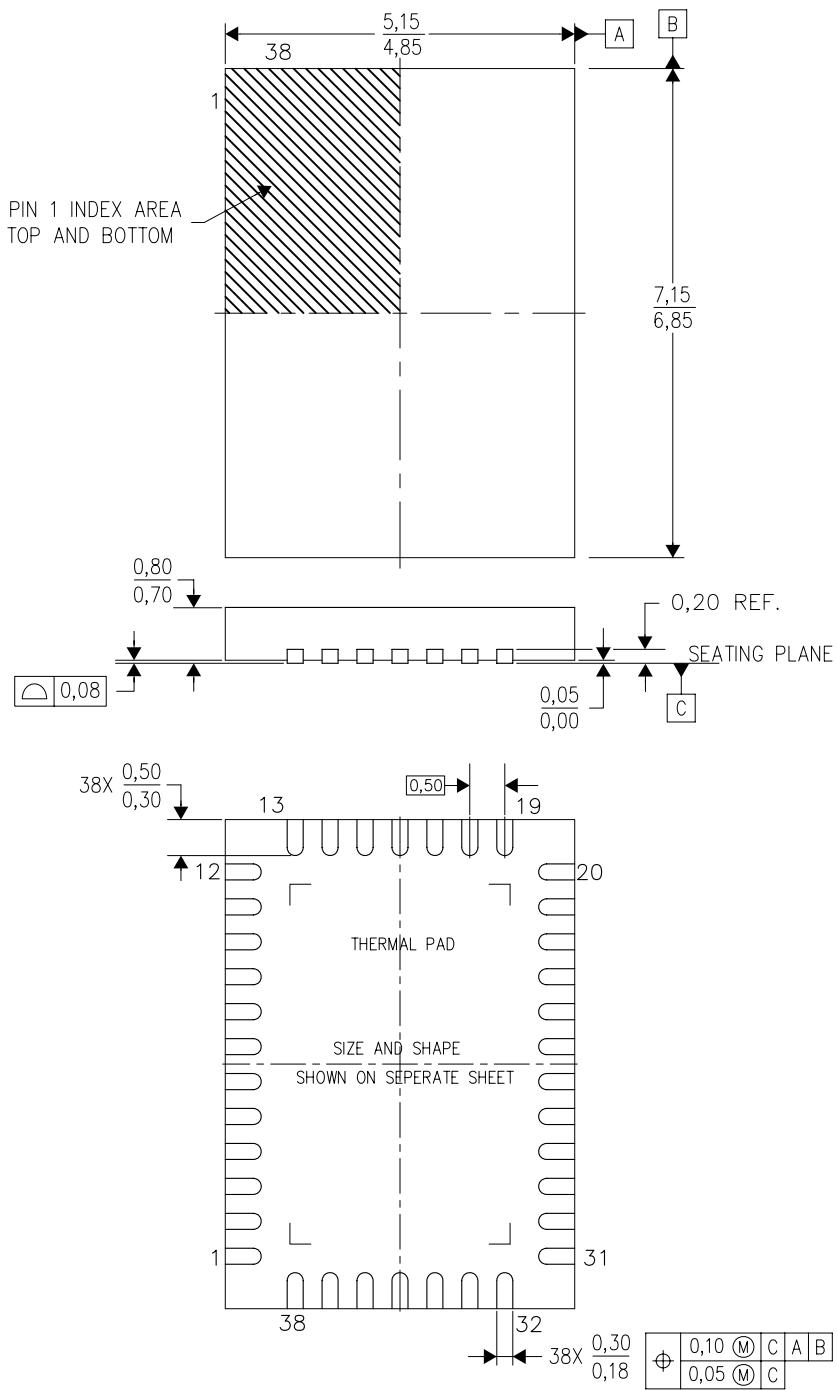
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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RLJ (R-PWQFN-N38)

PLASTIC QUAD FLATPACK NO-LEAD



4212454/A 01/12

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

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