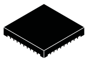


Dual Phase, D-CAP+™, Eco-mode™ Step-Down Controller with 8-Bit DAC

Check for Samples: TPS53624

FEATURES

- **Selectable Dual-or Single-Phase**
- **Minimum External Parts Count**
- **8-Bit DAC Supports Wide Range of Applications**
- **Optimized Efficiency at Light and Heavy Loads**
- **Patented Output Overshoot Reduction (OSR) Reduces Output Capacitance**
- **Accurate, Adjustable Voltage Positioning**
- **Selectable 200, 300, 400 and 500 kHz Frequency**
- **Pat. Pending AutoBalance Phase Balancing**
- **Selectable 8-Level Current Limit**
- **3-V to 28-V Conversion Voltage Range**
- **Fast MOSFET Driver with Integrated Boost Diode**
- **Integrated Overvoltage Protection (OVP)**
- **Small 6 × 6, 40-Pin QFN PowerPAD™ Package**

APPLICATIONS

- **High-Current, Low-Voltage ASIC or Microprocessor Core Regulator**

DESCRIPTION

The TPS53624 is a dual-phase step down controller with integrated gate drivers. The PCNT pin enables operation in dual or single-phase mode to optimize efficiency depending on the load requirements. Advanced control features such as D-CAP+™ architecture and OSR provides fast transient response with low output capacitance. The DAC supports VID-on-the-fly to optimize the output voltage to the operating state of the system to reduce quiescent power. The auto-skip feature of the TPS53624 optimizes light-load efficiency in single phase operation. System management features include adjustable thermal monitor input and output (THRM, THAL), output current monitoring (IMON), and complimentary power good signals (PG and PGD). Adjustable control of the output voltage slew rate and voltage positioning are provided. In addition, the TPS53624 includes two high-current FET gate drivers to drive high and low side N-channel FETs with exceptionally high speed and low switching loss. All logic input and output pins have flexible LV input and output thresholds that enable interface with logic voltages from 1 V to 3.6 V.

The TPS53624 is packaged in a space saving, thermally enhanced, RoHS compliant 40-pin QFN and is rated to operate from –10°C to 105°C.

ORDERING INFORMATION(1)

T_A	PACKAGE	DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–10°C to 105°C	Plastic Quad Flat Pack (QFN)	TPS53624RHAT	40	Tape-and-reel	250
		TPS53624RHAR			2500

(1) For the most current package and ordering information, see the packaging information at the end of this document, or see the TI website at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND.) (1)

		VALUE		UNIT
		MIN	MAX	
Input voltage range (2)	VBST1, VBST2	–0.3	36	V
	VBST1to LL1. VBST2 to LL2	–0.3	6	
	CSP1, CSN1, CSP2, CSN2, MODE, OSRSEL, PCNT, SLEW, THRM, TRIPSEL, TONSEL, V5FILT, V5IN, VID0, VID1, VID2, VID3, VID4, VID5, VID6, VID7, VFB, EN, $\overline{\text{THAL}}$	–0.3	6	
Output voltage range (2)	LL1, LL2	–5	30	V
	DRVH1, DRVH2	–5	36	
	DRVH1, DRVH2 to LL1 or LL2	–0.3	6	
	VREF, DROOP, DRVL1, DRVL2, IMON, $\overline{\text{PG}}$, PGD	–0.3	6	
	PGND, GFB	–0.3	0.3	
Operating junction temperature, T_J		–40	125	°C
Storage junction temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC (1)		RHA (40 PIN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32	°C/W
θ_{JB}	Junction-to-board thermal resistance	10	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, all voltages wrt GND (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltages	Conversion voltage (no pin assigned)	3		28	V
	V5IN, V5FILT	4.5		5.5	
Voltage range, conversion pins	VBST1, VBST2	–0.1		34	V
	DRVH1, DRVH2	–0.8		34	
	LL1, LL2	–0.8		28	
Voltage range, 5-V pins	CSN1, CSN2, CSP1, CSP2, DROOP, DRVL1, DRVL2, IMON, MODE, OSRSEL $\overline{\text{PG}}$, PGD, SLEW, THRM, TONSEL, TRIPSEL, VREF, VFB	–0.1		5.5	V
Voltage range, 3.3-V pins	EN	–0.1		3.6	V
Voltage range, VCCP I/O pins	PCNT, VID0, VID1, VID2, VID3, VID4, VID5, VID6, VID7, $\overline{\text{THAL}}$	–0.1		1.3	V
Ground pins	PGND, GFB	–0.1		0.1	
Electrostatic Discharge Protection (ESD)	Human body model (HBM)	2			kV
	Charged device model (CDM)	1.5			
Operating free air temperature, T_A		–10		105	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V_{V5FILT} = V_{V5IN} = 5.0 V, GFB = PGND = GND, V_{VFB} = V_{OUT} (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: CURRENTS, UVLO AND POWER-ON RESET						
I_{V5}	V5IN + V5FILT supply current	V_{DAC} < V_{VFB} < V_{DAC} + 100 mV, EN = HI		2.3	4	mA
I_{V5STBY}	V5IN + V5FILT standby current	EN = LO			1	μA
V_{UVLOH}	V5FILT UVLO OK threshold	V_{V5FILT} = V_{V5IN}, V_{VFB} < 200 mV, Ramp up; V_{EN} = HI; Switching begins	4.25	4.4	4.5	V
V_{UVLOL}	V5FILT UVLO fault threshold	V_{V5FILT} = V_{V5IN}. Ramp down; V_{EN} = HI, V_{VFB} = 100 mV, Restart if 5 V falls below V_{POR} then rises > V_{UVLOH} is toggled with 5 V > V_{UVLOH}	4	4.2	4.3	V
V_{POR}	V5FILT fault latch reset threshold	V_{V5FILT} = V_{V5IN}, Ramp Down, EN = HI, Can restart if 5-V goes up to V_{UVLOH} and no other faults present	1.4	1.9	2.3	V
REFERENCES: DAC, VREF, VBOOT AND DRVL DISCHARGE						
V_{VIDSTP}	VID step size	Change VID0 HI to LO to HI		6.25		mV
V_{DAC1}	VFB no load active	0.750 V ≤ V_{VFB} ≤ 1.250 V	-1.35%		1.35%	
V_{DAC2}	VFB no load active/sleep	0.500 V ≤ V_{VFB} ≤ 0.750 V	–11		11	mV
V_{DAC3}	VFB deeper sleep	0.300V ≤ V_{VFB} ≤ 0.500 V	–14		14	mV
V_{DAC4}	VFB above microcontroller VID	1.250 V ≤ V_{VFB} ≤ 1.6 V	–1.35%		1.35%	
V_{VREF}	VREF output	4.5 V ≤ V_{V5FILT} ≤ 5.5 V, I_{REF} = 0	1.665	1.700	1.750	V
$V_{VREFSRC}$	VREF output source	I_{REF} = 0 μA to 250 μA	–9	–3		mV
$V_{VREFSNK}$	VREF output sink	I_{REF} = –250 μA to 0 μA		10	35	mV
V_{VBOOT}	Internal VFB initial boot voltage	Initial DAC boot voltage	0.99	1.00	1.01	V
VOLTAGE SENSE: VFB AND GNDSNS						
I_{VFB}	VFB input bias current	Not in fault, disable or UVLO; V_{VFB} = 2 V, GFB = 0 V		9	40	μA
I_{VFBDQ}	VFB input bias current, discharge	Fault, disable or UVLO, V_{VFB} = 100 mV	90	125	175	μA
I_{GFB}	GNDSNS input bias current	Not in fault, disable or UVLO; V_{VFB} = 2 V, GSNS = 0 V	–40	–8		μA
V_{DELGND}	GNDSNS differential			±300		mV
$A_{GAINGND}$	GNDSNS/GND gain		0.995	1.000	1.011	V/V
V_{VFBCOM}	VFB common mode input		–0.3		2	V
CURRENT MONITOR						
V_{IMONLK}	Zero-level current output	ΣΔCS = 0 mV, R_{IMON} = 12.7 kΩ	0	5	150	mV
V_{IMONLO}	Low-level current output	ΣΔCS = 10 mV, R_{IMON} = 12.7 kΩ	202	250	302	mV
$V_{IMINMID}$	Mid-level current output	ΣΔCS = 20 mV, R_{IMON} = 12.7 kΩ	460	500	538	mV
V_{IMONHI}	High-level current output	ΣΔCS = 40 mV, R_{IMON} = 12.7 kΩ	958	1000	1058	mV
K_{IMON}	Gain factor			2		μA/mV
$I_{IMONSRC}$	Current monitor source	ΣΔCS = 60 mV	108		130	μA
$V_{IMONSNK}$	Current monitor clamp	ΣΔCS = 40 mV, R_{IMON} = OPEN	1.02		1.11	V

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V_{V5FILT} = V_{V5IN} = 5.0 V, GFB = PGND = GND, V_{VFB} = V_{OUT} (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE: OVERCURRENT, ZERO CROSSING, VOLTAGE POSITIONING AND PHASE BALANCING						
V_{OCPP}	OCP voltage set (valley current limit)	$V_{TRIPSEL}$ = GND, R_{SLEW} to GND	8.2		13.5	mV
		$V_{TRIPSEL}$ = REF, R_{SLEW} to GND	11.4		16.8	
		$V_{TRIPSEL}$ = 3.3 V, R_{SLEW} to GND	14.5		20.3	
		$V_{TRIPSEL}$ = V_{V5FILT}, R_{SLEW} to GND	19.3		25.3	
		$V_{TRIPSEL}$ = GND, R_{SLEW} to VREF	24.0		30.5	
		$V_{TRIPSEL}$ = REF, R_{SLEW} to VREF	30.2		37	
		$V_{TRIPSEL}$ = 3.3 V, R_{SLEW} to VREF	38.1		45.5	
		$V_{TRIPSEL}$ = V_{V5FILT}, R_{SLEW} to VREF	48.9		57	
V_{OCPN}	Negative OCP voltage (minimum magnitude)	$V_{TRIPSEL}$ = GND, R_{SLEW} to GND	12.5		17.7	mV
		$V_{TRIPSEL}$ = REF, R_{SLEW} to GND	15.8		21.5	
		$V_{TRIPSEL}$ = 3.3 V, R_{SLEW} to GND	19.2		25	
		$V_{TRIPSEL}$ = V_{V5FILT}, R_{SLEW} to GND	25.5		31.5	
		$V_{TRIPSEL}$ = GND, R_{SLEW} to VREF	32.1		38.3	
		$V_{TRIPSEL}$ = REF, R_{SLEW} to VREF	40.5		46.7	
		$V_{TRIPSEL}$ = 3.3 V, R_{SLEW} to VREF	51.9		58.5	
		$V_{TRIPSEL}$ = V_{V5FILT}, R_{SLEW} to VREF	64.9		71.8	
V_{OCPCC}	Channel-to-channel OCP matching	(CSP1–CSN1) – (CSP2–CSN2) at OCP for each channel		±1.0		mV
I_{CS}	CS pin input bias current	CSPx and CSNx	–1	0.2	1	μA
$g_{M\text{-}DROOP}$	Droop amplifier transconductance	V_{VSNS} = 1 V	482	500	522	μs
I_{DROOP}	Droop amplifier sink/source current		50	100	150	μA
$V_{DCLAMPN}$	Droop amplifier clamp voltage (negative)	(V_{VREF} – V_{DROOP})		46		mV
$V_{DCLAMPP}$	Droop amplifier clamp voltage (positive)	(V_{DROOP} – V_{VREF})		1.2		V
I_{BAL_TOL}	Internal current share tolerance	V_{DAC} = 0.750 V; V_{CSP1} – V_{CSN1} = V_{CSP2} – V_{CSN2} = V_{OCPP_MIN}	–3%		3%	
A_{CSINT}	Internal current sense gain	Gain from CSPx – CSNx to PWM comparator	5.93		6.11	V/V
DRIVERS: HIGH-SIDE, LOW-SIDE, CROSS CONDUCTION PREVENTION AND BOOST RECTIFIER						
R_{DRVH}	DRVH on-resistance	(V_{VBSTx} – V_{LLx}) = 5 V, HI state, (V_{VBST} – V_{DRVH}) = 0.1 V		1.2	2.5	Ω
		(V_{VBSTx} – V_{LLx}) = 5 V, LO state, (V_{DRVH} – V_{LL}) = 0.1 V		0.8	2.5	
I_{DRVH}	DRVH sink/source current(1)	V_{DRVHx} = 2.5 V, (V_{VBSTx} – V_{LLx}) = 5 V, source		2.2		A
		V_{DRVHx} = 2.5 V, (V_{VBSTx} – V_{LLx}) = 5 V, sink		2.2		
t_{DRVH}	DRVH transition time	DRVHx 10% to 90% C_{DRVHx} = 3 nF		17	30	ns
		DRVHx 90% to 10% C_{DRVHx} = 3 nF		13	30	
R_{DRVL}	DRVL on-resistance	HI state, (V_{V5IN} – V_{DRVL}) = 0.1 V		0.9	2	Ω
		LO state, (V_{DRVL} – V_{PGND}) = 0.1 V		0.4	1	
I_{DRVL}	DRVL sink/source current(1)	V_{DRVLx} = 2.5 V, source		2.7		A
		V_{DRVLx} = 2.5 V, sink		8		
t_{DRVL}	DRVL transition time	DRVLx 90% to 10%, CDRVLx = 3 nF		10	30	ns
		DRVLx 10% to 90%, CDRVLx = 3 nF		14	30	
$t_{NONOVLP}$	Driver non-overlap time	LLx falls to 1V to DRVLx rises to 1 V	14	19	29	ns
		DRVLx falls to 1V to DRVHx rises to 1 V	21	29	40	
V_{FBST}	BST rectifier forward voltage	V_{V5IN} – V_{VBST}, I_F = 5 mA, T_A = 25°C	0.6	0.7	0.8	V
I_{BSTLK}	BST rectifier leakage current	V_{VBST} = 34 V, V_{LL} = 28 V		0.1	1	μA

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, $V_{V5FILT} = V_{V5IN} = 5.0$ V, GFB = PGND = GND, $V_{VFB} = V_{OUT}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERSHOOT REDUCTION (OSR) THRESHOLD SETTING						
V_{OSR}	OSR voltage set	V_{OSRSEL} = GND	78	106	135	mV
		V_{OSRSEL} = REF	111	140	174	
		V_{OSRSEL} = 3.3 V	151	186	224	
		V_{OSRSEL} = V5FILT		OFF		
V_{OSRHYS}	OSR voltage Hysteresis(2)	All settings		20		mV
TIMERS: SLEW RATE, SLEW, ON-TIME AND I/O TIMING						
$I_{SLEW\ 1}$	R_{SLEW} to GND current	R_{SLEW} = 125 kΩ from SLEW to GND	9.9	10	10.2	µA
$I_{SLEW\ 2}$	R_{SLEW} to VREF current	R_{SLEW} = 45 kΩ from VREF to SLEW	9.5	10.2	10.8	µA
$t_{STARTUP}$	VFB startup time	I_{SLEW} = |10 µA|, No Faults, Time from EN to VSNS = VBOOT – 12%	0.60	0.80	0.90	ms
SL_{STRT}	VFB slew soft-start	I_{SLEW} = |10 µA|, EN goes HI (soft-start)	1.3	1.6	1.9	mV/µs
SR	VFB slew rate	I_{SLEW} = |10 µA|	10	12.5	15	mV/µs
t_{PGDPO}	PGD power-on delay time	Time from $\overline{\text{PG}}$ going low to PG going high	0.4	0.7	1	ms
$t_{PGDDGLTO}$	PGD deglitch time	Time from VFB out of +300 mV V_{DAC} boundary to PGOOD low	40	74	100	µs
$t_{PGDDGLTU}$	PGD deglitch time	Time from VFB out of –300 mV V_{DAC} boundary to PGOOD low	50	105	150	µs
t_{TON}	On-time control	V_{TON} = GND, V_{LLx} = 12 V, V_{VFB} = 1 V	315	400	465	ns
		$V_{TON} = V_{REF}$, V_{LLx} = 12 V, V_{VFB} = 1 V	215	260	300	
		V_{TON} = 3.3 V, V_{LLx} = 12 V, V_{VFB} = 1 V	170	200	230	
		$V_{TON} = V_{V5FILT}$, V_{LLx} = 12 V, V_{VFB} = 1	145	170	190	
t_{MIN}	Controller minimum OFF time	Fixed value	70	102	125	ns
$t_{VIDDBNC}$	VID debounce time(2)		100			ns
$t_{PSIDBNC}$	PCNT debounce Time(2)		100			ns
t_{VCCVID}	VID change to VFB Change(2)				600	ns
$t_{VRONPGD}$	EN low to PGD low		20	74	100	ns
t_{PGDVCC}	PGD low to VFB change(2)				100	ns
$t_{VRTDGLT}$	$\overline{\text{THAL}}$ deglitch time		0.3	1	3	ms
PROTECTION: OVP, PGOOD, VR, $\overline{\text{VR\_TT}}$ FAULTS OFF AND INTERNAL THERMAL SHUTDOWN						
V_{OVPH}	Fixed OVP voltage	VFB > V_{OVPH} for 1 µs, DRVL turns ON	1.6		1.8	V
V_{PGDH}	PGD high threshold	Measured at the VFB pin wrt / VID code, device latches OFF, begins soft-stop	180		258	mV
V_{PGDL}	PGD low threshold	Measured at the VFB pin wrt / VID code, device latches off, begins soft-stop	–367		–273	mV
V_{THRM}	Thermal shutdown voltage	Measured at THERM; $\overline{\text{THAL}}$ goes LO	0.69	0.75	0.81	V
I_{THRM}	THERM current	Measure I_{THERM} to GND	57.5	61	67.5	µA
V_{NOFLT}	All faults OFF	THRM > V5FILT + V_{TH}; not latched	4.75	4.9	5	V
TH_{INT}	Internal controller thermal shutdown(2)	Latch off controller		160		°C

(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V_{V5FILT} = V_{V5IN} = 5.0 V, GFB = PGND = GND, V_{VFB} = V_{OUT} (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{VRTTL}	$\overline{\text{THAL}}$ pull-down voltage	Pul- down voltage with 20-mA sink current		0.15	0.40	V
I_{VRTTLK}	$\overline{\text{THAL}}$ leakage current	Hi-Z leakage current, Apply 5-V in off state	–2	0.2	2	μA
V_{CLKPGL}	$\overline{\text{PG}}$, PG pull-down voltage	Pull-down voltage with 3-mA sink current		0.1	0.4	V
$I_{CLKPGLK}$	$\overline{\text{PG}}$, PGOOD leakage current	Hi-Z leakage current, Apply 5-V in off state	–2	0.1	2	μA
V_{VCCPH}	I/O LV logic high	PCNT, EN, VID0, VID1, VID2, VID3, VID4, VID5, VID6, VID7	0.83			V
V_{VCCPL}	I/O LV logic low				0.3	V
I_{VCCPLK}	I/O LV leakage	Leakage current, V_{VID} = V_{PCNT} = 1 V; V_{EN} = 0 V	–1.00	0.01	1.00	μA
I_{VIDLK}	I/O LV leakage	Leakage current, V_{VID} = V_{PCNT} = 1 V; EN = 3.3 V	5	10	15	μA
I_{ENH}	I/O 3.3-V leakage	Leakage current, V_{EN} = 3.3 V	10		25	μA
I_{VIDL}		V_{VID0} = V_{VID1}= V_{VID2}= V_{VID3}= V_{VID4}= V_{VID5}= V_{VID6}= V_{VID7} = 0 V, V_{EN} = 3.3 V	–3	–1.5	1	μA
I_{SELECT}		$V_{TRIPSEL}$ = V_{OSRSEL} = V_{TONSEL} = 5 V	–2	1.5	5	μA
I_{CTRL}		V_{PCNT} = 0 V; V_{EN} = 3.3 V	–1		1	μA
I_{MODEL}		V_{MODE} = 0 V	–5		5	μA
I_{MODEH}		V_{MODE} = 5 V	10		40	μA

DEVICE INFORMATION

RHA PACKAGE
40 PINS
(TOP VIEW)

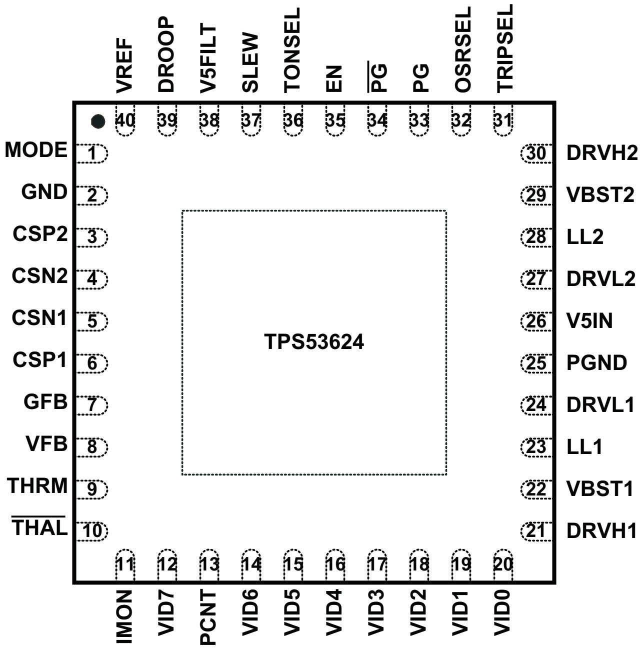


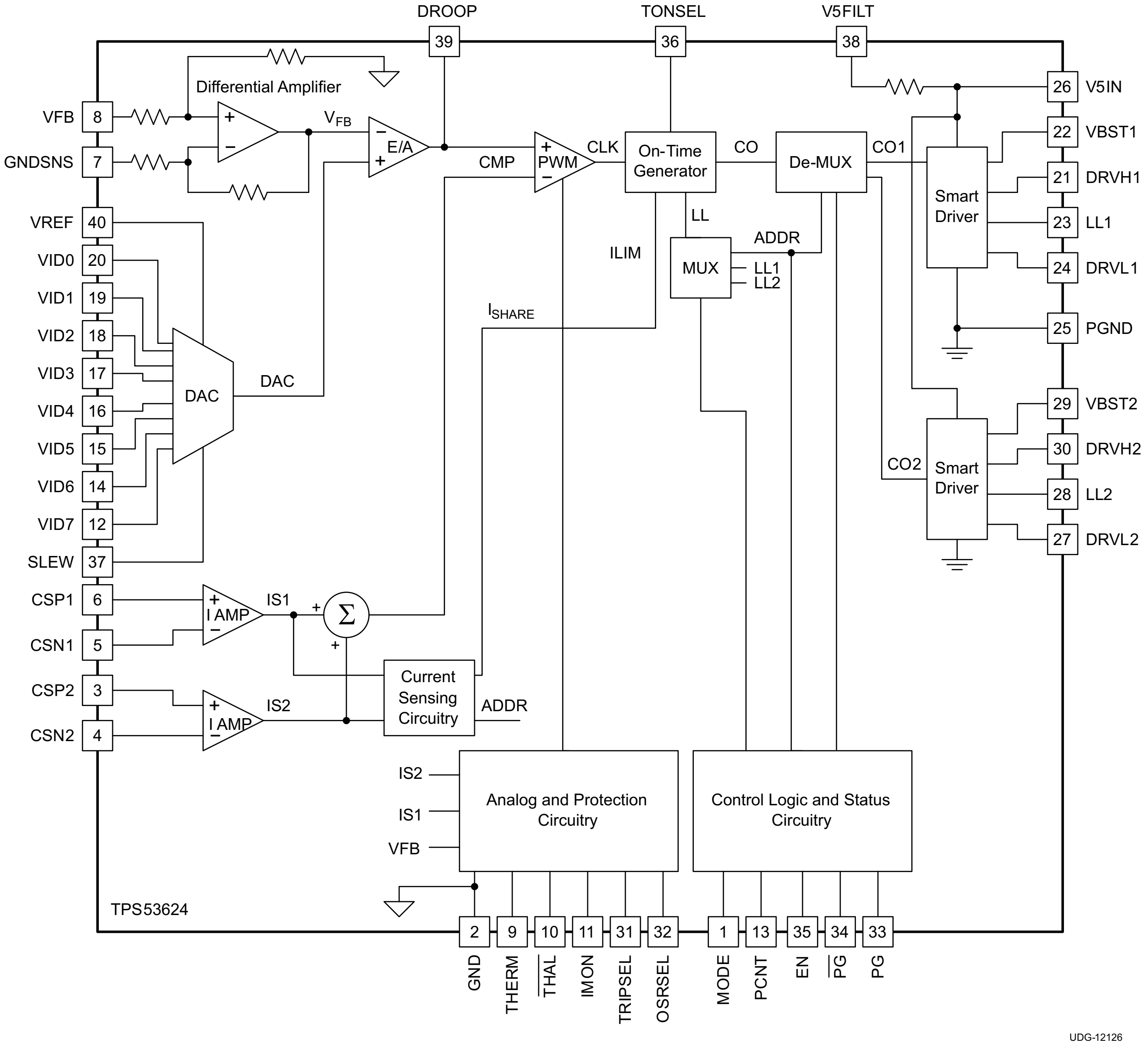
Table 1. PIN FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CSP1	6	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense R-C network.
CSP2	3	I	
CSN1	5	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense RC network.
CSN2	4	I	
DROOP	39	O	Output of g_M error amplifier. A resistor to VREF sets the droop gain. A capacitor to VREF helps shape the transient response.
DRVH1	21	O	High-side N-channel MOSFET gate drive outputs.
DRVH2	30	O	
DRVL1	24	O	Synchronous N-channel MOSFET gate drive outputs.
DRVL2	27	O	
EN	35	I	Controller enable. 3.3-V I/O level; 100-ns de-bounce. Logic high 3.3-V enables the controller. Logic low stops the controller.
GND	2	—	Return for analog circuits.
GFB	7	I	Voltage sense return tied directly to GND of the microprocessor. Tie to GND with a 100-Ω resistor to close feedback when the microprocessor is not in the socket.
IMON	11	O	Current monitor output. $V_{IMON} = \Sigma V_{ISENSE} \times K \times R_{IMON}$. Reference R_{IMON} to GNDSNS. Voltage is clamped at 1.1-V maximum.
LL1	23	I/O	High-side N-channel MOSFET gate drive return. Also, input for adaptive gate drive timing.
LL2	28	I/O	
MODE	1	—	Tie to GND to select CPU mode.
OSRSEL	32	O	Overshoot reduction (OSR) setting. The OSR threshold can be selected or OSR can be disabled.
$\overline{PG}$	34	O	Negative active power good output; Open drain. Transitions low of approximately 50 ms after VOUT reaches the VID level. Leave open if unused.

Table 1. PIN FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
PGND	25	—	Synchronous N-channel MOSFET gate drive return.
PG	33	O	Power good output; Open-drain. 6ms delay from voltage reaching the power good threshold. Leave open if unused
PCNT	13	I	Single or dual phase control. 1-V I/O level. A low is single phase mode.
SLEW	37	I	Precision current set-point for slew rate control. Tie the R_{SLEW} resistor to GND for the low OCP range; tie R_{SLEW} to VREF for the high OCP range.
$\overline{\text{THAL}}$	10	O	Thermal flag open drain output - active low. Fall time < 100ns with 56Ω pull-up to 1V. 1ms de-glitch filter.
THRM	9	I/O	Thermal sensor input. An internal, 60-μA current source flows into an NTC thermistor connected to GND. The voltage threshold is 0.75 V. Also is a *faults off* input, (THERM = V5FILT) for debug mode.
TONSEL	36	I	On-time selection pin. The operating frequency can be set between 200 kHz and 500 kHz in 100 kHz steps. Frequency can be changed during operation.
TRIPSEL	31	I	Overcurrent protection (OCP) setting. TRIPSEL is set with the R_{SLEW} connection. The valley current limit at the CS inputs can be selected in a range from approximately 10 mV to approximately 50 mV.
VBST1	22	I	High-side N-channel MOSFET bootstrap voltage inputs.
VBST2	29	I	
VID0	20	I	VID bits (MSB to LSB). 1-V I/O level; 100ns de-bounce
VID1	19		
VID2	18		
VID3	17		
VID4	16		
VID5	15		
VID6	14		
VID7	12		
V5FILT	38	I	5-V power input for control circuitry. Has internal 3-Ω resistor to 5VIN; bypass to GND with a ≥1-μF ceramic capacitor.
V5IN	26	I	5-V power input for drivers; bypass to PGND with ≥2.2 μF ceramic capacitor.
VREF	40	O	1.7-V, 250-μA voltage reference. Bypass to GND with a 0.22-μF ceramic capacitor.
VFB	8	I	Voltage sense line tied directly to V_{CORE} of the microprocessor. Tie to V_{OUT} with a 100-Ω resistor to close feedback when the microprocessor is not in the socket.
Thermal Pad			Connect directly to system GND plane with multiple vias.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION DIAGRAMS

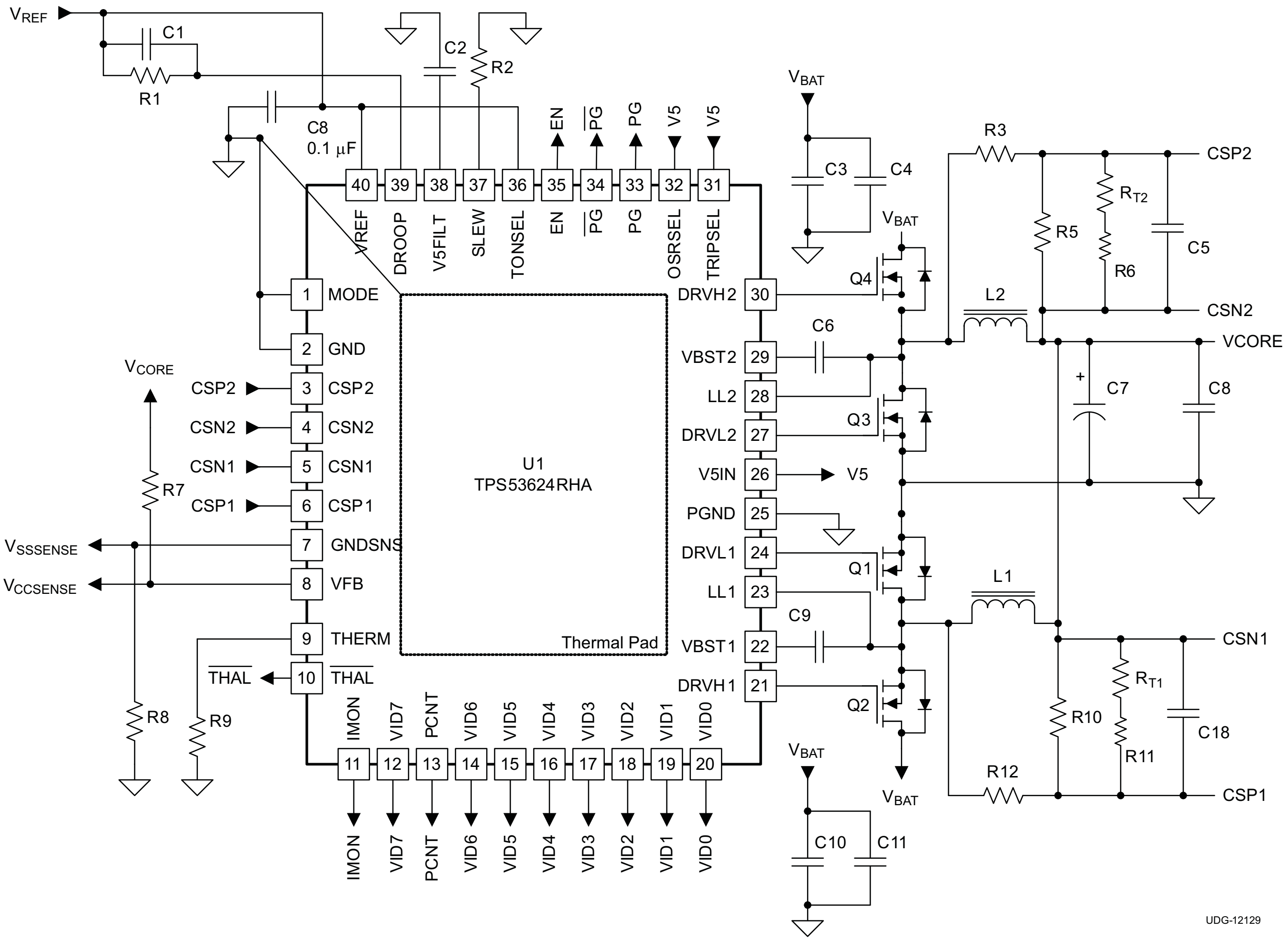


Figure 1. Inductor DCR Current Sense Application Diagram

Application Circuit List of Materials

Recommended part numbers for key external components for the circuits in Figure 1 is listed in Table 2. These components have passed applications tests.

Table 2. Key External Component Recommendations

FUNCTION	MANUFACTURER	COMPONENT NUMBER
High-side MOSFET	Infineon	BSC080N03MSG
Low-side MOSFET (x2)	Infineon	BSC030N03MSG
Inductors	Panasonic	ETQP4LR36AFC
	Tokin	MPCG1040LR36
	Toko	FDUE10140D-R36M
Bulk Output Capacitors	Panasonic	EEFLX0D331R4
	Sanyo	2TPLF330M5
	Kemet	T528Z337M2R5ATE005-6666
Ceramic Output Capacitors	Panasonic	ECJ2FB0J106K
	Murata	GRM21BR60J106KE19L
NTC Thermistors	Panasonic	ERTJ1VV154J
	Murata	NCP18XF151J03RB

DETAILED DESCRIPTION

FUNCTIONAL OVERVIEW

The TPS53624 is a D-CAP+™ mode adaptive on-time converter. The output voltage is set using a DAC that outputs a reference in accordance with the 8-bit VID code defined in Table 5. *VID-on-the-fly* transitions are supported with the slew rate controlled by a single resistor on the SLEW pin. Two powerful integrated drivers support output currents in excess of 50 A. The converter enters single phase mode under PCNT control to optimize light-load efficiency. Four switching frequency selections are provided in 100-kHz increments from 200 kHz to 500 kHz per phase to enable optimization of the power chain for the cost, size and efficiency requirements of the design. (See Table 3)

Table 3. Frequency Selection Table

TONSEL VOLTAGE (V_{TONSEL}) (V)	FREQUENCY (kHz)
GND (0)	200
VREF (1.7)	300
3.3	400
5	500

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53624, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the DAC voltage and the feedback voltage.

This approach has two advantages:

1. The amplifier DC gain sets an accurate linear load-line; this is required for CPU core applications.
2. The error voltage input to the PWM comparator is filtered to improve the noise performance.

In a steady-state condition, the two phases of the TPS53624 switch 180° out-of-phase. The phase displacement is maintained both by the architecture (which does not allow both hig-side gate drives to be on in any condition) and the current ripple (which forces the pulses to be spaced equally). The controller forces current sharing adjusting the on-time of each phase. Current balancing requires no user intervention, compensation, or extra components.

Multi-Phase, PWM Operation

Referring to the Functional Block Diagram and , in dual-phase steady state, continuous conduction mode, the converter operates as follows:

Starting with the condition that both high-side MOSFETs are off and both low-side MOSFETs are on, the summed current feedback (V_{CMP}) is higher than the error amplifier output (V_{DROOP}). V_{CMP} falls until it hits V_{DROOP}, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

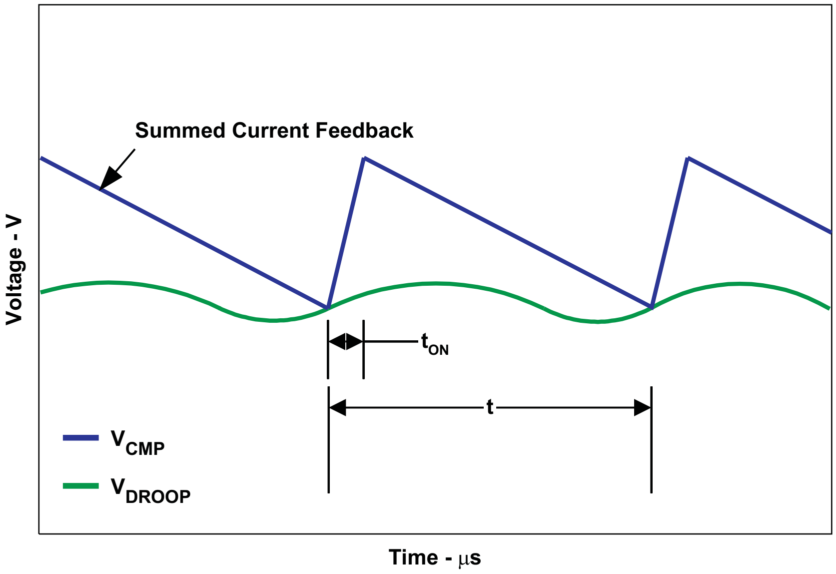


Figure 2. D-CAP+ Mode Basic Waveforms

The summed current feedback is an amplified and filtered version of the CSPx and CSNx inputs. The TPS53624 provides dual independent channels of current feedback to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture.

PWM Frequency and Adaptive on Time Control

The on-time (at the LL node) is determined by Equation 1.

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SEL}}\right) + 30\,ns$$

where

- f_{SEL} is the frequency selected by the connection of the TONSEL pin (1)

The on-time pulse is sent to the high-side MOSFET. The inductor current and summed current feedback rise to their maximum value, and the multiplexer and de-multiplexer switch to the next phase. Each ON pulse is latched to prevent double pulsing.

The current sharing circuitry compares the average values of the individual phase currents, then adds or subtracts a small amount from each on-time in order to bring the phase currents into line. No user design is required.

Accurate droop is provided by the finite gain of the droop amplifier. The calculation for output voltage droop, V_{DROOP} is shown in Equation 2.

$$V_{DROOP} = \frac{R_{CS} \times A_{CS} \times \sum I(L)}{R_{DROOP} \times G_M}$$

where

- R_{CS} is the effective current sense resistance, regardless if a sense resistor or inductor DCR is used
- A_{CS} is the gain of the current sense amplifier
- ΣI(L) is the DC sum of inductor currents
- R_{DROOP} is the value of resistor from the DROOP pin to VREF
- G_M(droop) is the GM of the droop amplifier (2)

The capacitor in parallel with R_{DROOP} matches the slew rate of the DROOP pin with the current feedback signals to prevent *ring-back* during transient load conditions.

$$C_{DROOP} = \frac{R_{LL} \times \Delta I_{OUT} \times g_M \times L}{R_{CS} \times A_{CS} \times D_{MAX} \times V(L)} - 30\,pF$$

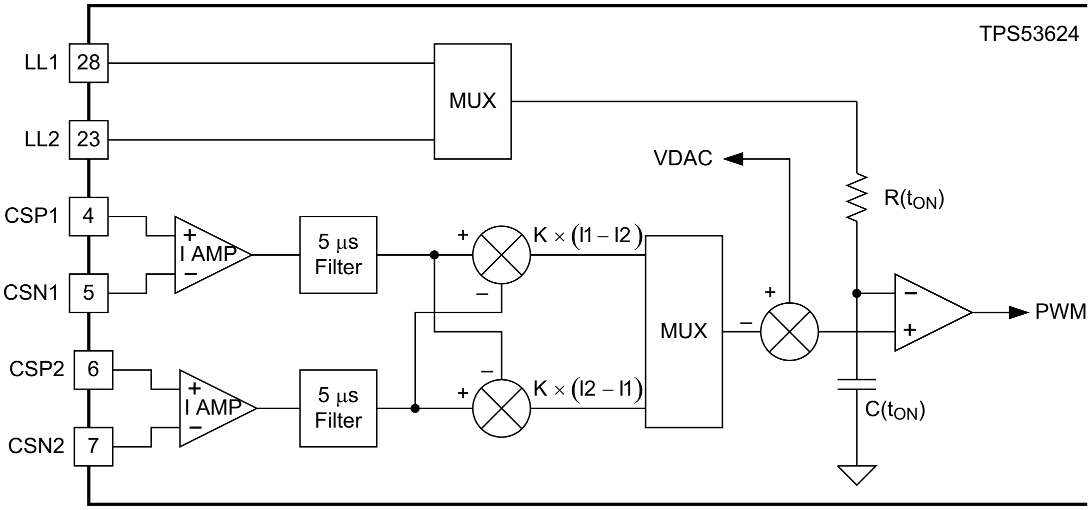
where

- R_{LL} is load-line slope defined by proicessor mnufacturer
- ΔI_{OUT} is maximum dynamic load current for the processor
- $D_{MAX} = t_{ON} / t_{ON} + t_{OFF(min)}$
- V(L) is the voltage across the inductor ($V_{BAT} - V_{CORE}$). (3)

The 30-pF term accounts for the slew rate limit of the amplifier without external capacitance.

AutoBalance Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase. The block diagram is shown in Figure 3.



UDG-12128

Figure 3. Current Sharing Block Diagram

Figure 3 also shows the TI D-CAP+™ constant on-time modulator. The PWM comparator (not shown) starts a pulse when the feedback voltage meets the reference. This pulse turns on the gate of the high-side MOSFET. After the MOSFET turns on, the LL voltage for that phase is driven up to the battery input. This charges $C(t_{ON})$ through $R(t_{ON})$. The pulse is terminated when the voltage at $C(t_{ON})$ matches the t_{ON} reference, normally the DAC voltage (V_{DAC}).

The circuit operates in the following fashion, using Figure 3 as the block diagram and to show the circuit action at the level of an individual pulse (PWM1). First assume that the 5 µs averaged value of I1 = I2. In this case, the PWM modulator terminates at VDAC, and the normal pulse width is delivered to the system. If instead, I1 > I2, then an offset is subtracted from VDAC, and the pulse width for phase one is shortened, reducing the current in phase one to compensate. If I1 < I2, then a longer pulse is produced, again compensating on a pulse-by-pulse basis.

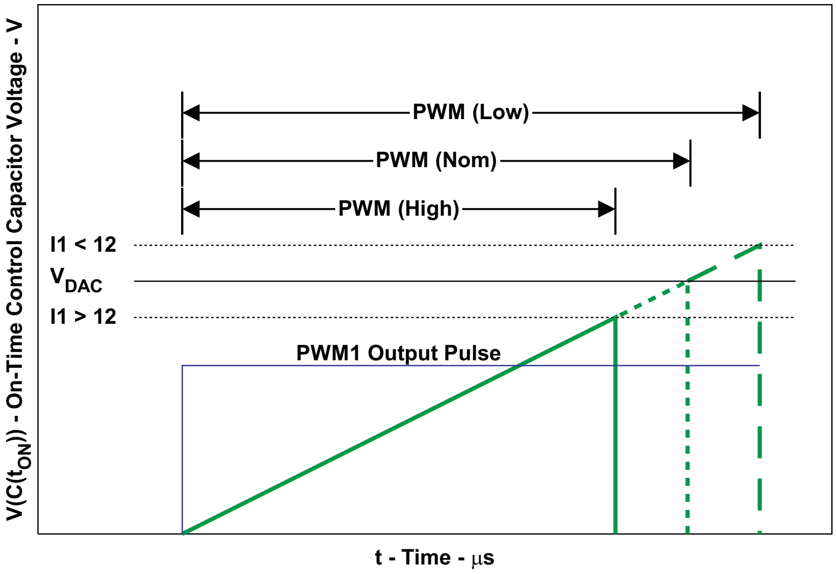


Figure 4.

Because the increase in pulse width is proportional to the difference between the actual phase current and the ideal current, the system converges smoothly to equilibrium. Because the filtering is so much lighter than conventional current sharing schemes, the settling time is very fast. Analysis shows the response to be single pole with a bandwidth of approximately 60 kHz.

The speed advantage of the TPS53624 is beneficial because processors quickly move from full speed to idle and back to save power when processing light and moderate loads. A multi-phase converter that takes milliseconds to implement current sharing is never in equilibrium and thermal hot-spots can result. The TPS53624 allows rapid dynamic current and output voltage changes while maintaining current balance.

Overshoot Reduction (OSR) Feature

The problem of overshoot in low duty-cycle synchronous buck converters results from the output inductor having a small voltage (V_{CORE}) with which to respond to a transient load release.

In Figure 5, a single phase converter is shown for simplicity. In an ideal converter, with the common values of 12-V input and 1.2-V output, the inductor has 10.8 V (12 V – 1.2 V) to respond to a transient step, and 1.2 V to respond once the load releases.

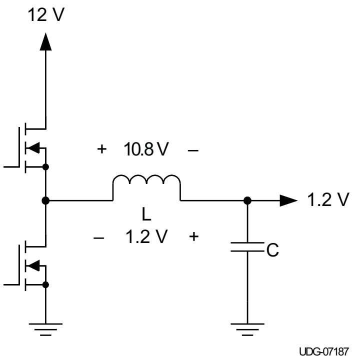


Figure 5. Synchronous Converter

Figure 6 shows a two-phase converter. The energy in the inductor is transferred to the capacitance on the V_{CORE} node above and the output voltage (green trace) overshoots the desired level (lower cursor, also green). In this case, the magnitude of the overshoot is approximately 40 mV. The LLx waveforms (yellow and blue traces) remain flat during the overshoot, indicating the DRVLx signals are on.

The performance of the same dual phase circuit, but with OSR enabled is shown in Figure 7. In this case, the low side FETs shut off when overshoot is detected and the energy in the inductor is partially dissipated by the body diodes. The overshoot is reduced by 25 mV. The dips in the LLx waveforms show the DRVLx signals are OFF only long enough to reduce the overshoot.

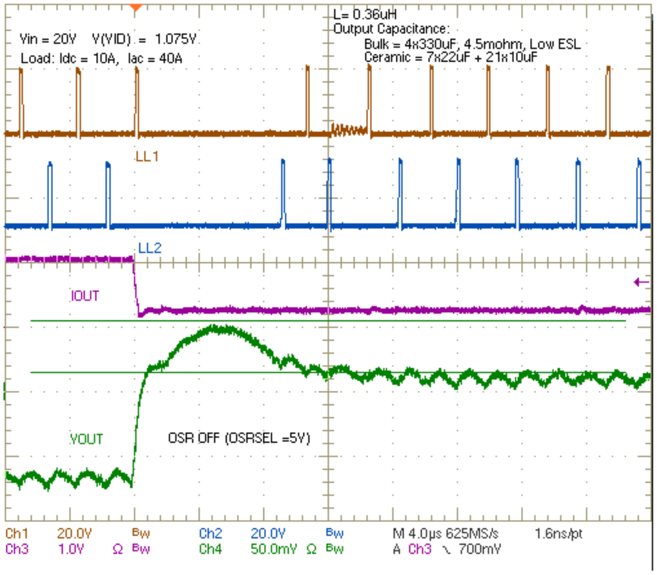


Figure 6. Circuit Performance Without Overshoot Reduction

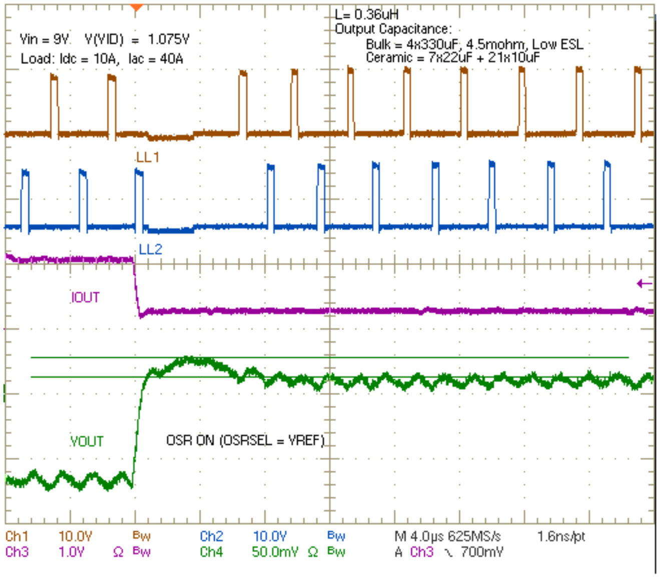


Figure 7. Transient Release Performance Improved with Overshoot Reduction

Implementation

OSR is implemented using a comparator between the DROOP and ISUM nodes. To implement OSR, simply terminate the OSRSEL pin to the desired voltage to set the threshold voltage for the comparator. The settings are:

- GND = Minimum voltage (Maximum reduction)
- VREF = Medium voltage
- +3.3V = Maximum voltage
- 5V = OSR off

Use the highest setting that provides the desired level of overshoot reduction to eliminate the possibility of false OSR operation.

Light Load Power Saving Features

The TPS53624 has several power saving features to provide excellent efficiency over a very large load range. This feature is implemented with PCNT pin.. This pin is a VCCP I/O level. A LO on this pin puts the converter into single phase mode, thus eliminating the quiescent power of phase two when high power is not needed.

In addition, the TPS53624 has an automatic pulse skipping *skip* mode. Regardless of the state of the logic inputs, the converter senses negative inductor current flow and prevents it by shutting off the low-side MOSFET(s). This saves power by eliminating recirculating current.

MOSFET Drivers

The TPS53624 incorporates a pair of strong, high-performance gate drives with adaptive cross-conduction protection. The driver uses the state of the DRVLx and LLx pins to be sure the high-side or low-side MOSFET is off before turning the other on. Fast logic and high drive currents (up to 8 A typical!) quickly charge and discharge MOSFET gates to minimize dead-time to increase efficiency. The high-side gate driver also includes an internal P-N junction *boost* diode, decreasing the size and cost of the external circuitry. For maximum efficiency, this diode can be bypassed externally by connecting Schottky diodes from V5IN (anode) to VBSTx (cathode).

Voltage Slewing

The TPS53624 ramps the internal DAC up and down as the VID is changing. These timings are independent of switching frequency, as well as output resistive and capacitive loading. The slew rate is set by a resistor from the SLEW pin to AGND (R_{SLEW}). R_{SLEW} sets both the slew rate and the soft-start rate.

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR}$$

where

- $K_{SLEW} = 1.25 \times 10^9$
- V_{SLEW} is equal to the slew reference $V_{SLEWREF}$when R_{SLEW} is tied to GND (4)

Connecting R_{SLEW} to VREF enables the high range of overcurrent protection and changes V_{SLEW} in Equation 4 to 0.45 V (VREF – $V_{SLEWREF}$). The soft-start rate is 1/8 the slew rate.

At start-up the VID code should be stable at the time EN goes high. For example, the V_{VID} for IMVP6.5 is 1.1 V. The soft-start time to V_{BOOT} is shown in Equation 5.

$$t_{SS} = \frac{1.1V \times 8}{SR} (s) \tag{5}$$

Protection Features

The TPS53624 features full protection of the converter power chain as well as the system electronics.

Input Undervoltage Protection (UVLO)

The TPS53624 continuously monitors the voltage on the V5FILT pin to ensure the value is high enough to bias the devices properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. This function is not latched, therefore removing and restoring 5-V power to the device resets it. The power input (V_{IN}) does not include a UVLO function, so the circuit runs with power inputs down to approximately 3 × V_{CORE}.

Power Good Signals

The TPS53624 has two open-drain powergood pins. PGD and $\overline{\text{PG}}$ have the following nominal thresholds:

- High: V_{DAC} + 200 mV
- Low : V_{DAC} – 300 mV

The differences are:

- $\overline{\text{PG}}$ transitions active low shortly (approxiimately 50 µs) after V_{OUT} reaches the V_{ID} voltage on power-up.
- PGD rises at the same time as $\overline{\text{PG}}$ reaches the power good threshold defined above. PGD is high when power is good and low when power is not good.

Both power good signals go inactive when the EN pin is pulled low or an undervoltage condition on V5IN is detected. Both are also *masked* during DAC transitions to prevent false triggering during voltage slewing.

Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS53624 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when VOUT is > 200 mV greater than V_{DAC}. In this case, the converter sets PGD signals inactive and then latches OFF. The converter remains in this state until the device is reset by cycling either V5IN or EN

However, because of the dynamic nature of VR systems, the +200 mV OVP threshold is *blanked* much of the time. In order to provide protection to the processor 100% of the time, there is a second OVP level fixed at 1.55 V which is always active. If the fixed OVP condition is detected, the PGD signals are forced inactive and the DRVLx signals are driven HI. The converter remains in this state until either V5IN or EN are cycled.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described below. If VOUT drops below the low PGD threshold for 80 µs, then the drivers are turned OFF until either V5IN or EN are cycled.

Current Protection

Two types of current protection are provided in the TPS53624.

- Overcurrent protection (OCP)
- Negative overcurrent protection

Overcurrent Protection (OCP)

The TPS53624 uses a *valley* current limiting scheme, so the ripple current must be considered. The DC current value at OCP is the OCP limit value plus half of the ripple current. Current limiting occurs on a phase-by-phase and pulse-by-pulse basis. If the voltage between CSPx and CSNx is above the OCP value (selected by combination of TRIPSEL pin connection and R_{SLEW} termination), the converter holds off the next ON pulse until it drops below the OCP limit. For inductor current sensing circuits, the voltage between CSPx and CSNx is the inductor DCR value multiplied by the resistor divider which is part of the NTC compensation network. As a result, a wide range of OCP values can be obtained by changing the resistor divider value. In general, use the highest TRIPSEL setting possible with the least attenuation in the resistor divider to provide as much signal to the device as possible. This provides the best performance for all parameters related to current feedback.

In OCP mode, the voltage droops until the UVP limit is reached. Then, the converter sets the PGD pins inactive, and the drivers are turned OFF. The converter remains in this state until the device is reset by the EN or the V5IN pin.

Settings use both the TRIPSEL pin and the R_{SLEW} termination. The eight possible OCP settings are shown in Table 4. For the levels in mV for a specific setting, see the *Electrical Characteristics* table.

Table 4. TRIPSEL Settings

OCP	R_{SLEW} Tied to GND				R_{SLEW} Tied to VREF			
TRIPSEL	GND	VREF	3.3V	5V	GND	VREF	3.3V	5V
Setting Level	1	2	3	4	5	6	7	8

Negative Overcurrent Protection

The negative OCP circuit acts when the converter is sinking current. The converter continues to act in a *valley* mode, so to have a similar negative DC limit, the absolute value of the negative OCP set point is typically 50% higher than the positive OCP set point.

Thermal Protection

Two types of thermal protection are provided in the TPS53624

- Thermal flag open drain ouptut signal ($\overline{\text{THAL}}$)
- Thermal shutdown

Thermal Flag Open Drain Ouptut Signal $\overline{\text{THAL}}$

The $\overline{\text{THAL}}$ signal is an Intel-defined open-drain signal that is used to protect the power chain. To use $\overline{\text{THAL}}$, place an NTC thermistor at the hottest area of the PC board and connect it to the THRM pin. THRM sources a precise 60-μA current, and $\overline{\text{THAL}}$ goes LO when the voltage on THERM reaches 0.7 V. Therefore, the NTC thermistor needs to be 11.7 kΩ at the trip level. A series or parallel resistor can be used to trim the resistance to the desired value at the trip level.

$\overline{\text{THAL}}$ signal does not change the operation of TPS53624

Thermal Shutdown

The TPS53624 also has an internal temperature sensor. When the temperature reaches a nominal 160°C, the device shuts down. The converter remains in this state until either V5IN or EN is cycled.

Current Monitor

The TPS53624 includes a power monitor function. The power monitor puts out an analog voltage proportional to the output power on the IMON pin.

$$V_{IMON} = A_{CS} \times GM_{IMON} \times \sum V_{CS} = K_{IMON} \times \sum V_{CS}$$

where

- K_{IMON} is given in the *Electrical Characteristics* table
- $\Sigma\ V_{CS}$ is the sum of the voltages at the inputs to the current sense amplifiers (6)

Single-Phase Operation

The TPS53624 is a two-phase controller. This controller can also be configured for single-phase operation. There are two ways the controller operates in single-phase mode.

- PCNT = 0 V. In this case, the controller starts up as dual-phase but goes into single-phase after start-up is completed. This mode is used for improving efficiency of a two-phase converter while operating under light load conditions.
- PCNT = 5 V. In this case, the controller operates in a complete single-phase mode. The drivers for Phase 2 are totally disabled in this mode.

In order to use the controller purely as a single-phase controller, connect PCNT to V5FILT. Also, the current sense input pins of the second phase (CSN2, CSP2) must be grounded. All the other pins of the second phase must be left open.

VID Table

The TPS53624 incorporates the 8-bit VID table shown in Table 5.

Table 5. VID Table

VID									VDAC
Hex	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0	0	0	0	0	0	0	0	0	OFF
1	0	0	0	0	0	0	0	1	OFF
2	0	0	0	0	0	0	1	0	1.60000
3	0	0	0	0	0	0	1	1	1.59375
4	0	0	0	0	0	1	0	0	1.58750
5	0	0	0	0	0	1	0	1	1.58125
6	0	0	0	0	0	1	1	0	1.57500
7	0	0	0	0	0	1	1	1	1.56875
8	0	0	0	0	1	0	0	0	1.56250
9	0	0	0	0	1	0	0	1	1.55625
A	0	0	0	0	1	0	1	0	1.55000
B	0	0	0	0	1	0	1	1	1.54375
C	0	0	0	0	1	1	0	0	1.53750
D	0	0	0	0	1	1	0	1	1.53125
E	0	0	0	0	1	1	1	0	1.52500
F	0	0	0	0	1	1	1	1	1.51875
10	0	0	0	1	0	0	0	0	1.51250
11	0	0	0	1	0	0	0	1	1.50625
12	0	0	0	1	0	0	1	0	1.50000
13	0	0	0	1	0	0	1	1	1.49375
14	0	0	0	1	0	1	0	0	1.48750
15	0	0	0	1	0	1	0	1	1.48125
16	0	0	0	1	0	1	1	0	1.47500
17	0	0	0	1	0	1	1	1	1.46875
18	0	0	0	1	1	0	0	0	1.46250
19	0	0	0	1	1	0	0	1	1.45625
1A	0	0	0	1	1	0	1	0	1.45000
1B	0	0	0	1	1	0	1	1	1.44375
1C	0	0	0	1	1	1	0	0	1.43750
1D	0	0	0	1	1	1	0	1	1.43125
1E	0	0	0	1	1	1	1	0	1.42500
1F	0	0	0	1	1	1	1	1	1.41875
20	0	0	1	0	0	0	0	0	1.41250
21	0	0	1	0	0	0	0	1	1.40625
22	0	0	1	0	0	0	1	0	1.40000
23	0	0	1	0	0	0	1	1	1.39375
24	0	0	1	0	0	1	0	0	1.38750
25	0	0	1	0	0	1	0	1	1.38125
26	0	0	1	0	0	1	1	0	1.37500
27	0	0	1	0	0	1	1	1	1.36875
28	0	0	1	0	1	0	0	0	1.36250
29	0	0	1	0	1	0	0	1	1.35625
2A	0	0	1	0	1	0	1	0	1.35000
2B	0	0	1	0	1	0	1	1	1.34375
2C	0	0	1	0	1	1	0	0	1.33750
2D	0	0	1	0	1	1	0	1	1.33125
2E	0	0	1	0	1	1	1	0	1.32500
2F	0	0	1	0	1	1	1	1	1.31875
30	0	0	1	1	0	0	0	0	1.31250
31	0	0	1	1	0	0	0	1	1.30625
32	0	0	1	1	0	0	1	0	1.30000
33	0	0	1	1	0	0	1	1	1.29375
34	0	0	1	1	0	1	0	0	1.28750
35	0	0	1	1	0	1	0	1	1.28125
36	0	0	1	1	0	1	1	0	1.27500
37	0	0	1	1	0	1	1	1	1.26875
38	0	0	1	1	1	0	0	0	1.26250
39	0	0	1	1	1	0	0	1	1.25625
3A	0	0	1	1	1	0	1	0	1.25000
3B	0	0	1	1	1	0	1	1	1.24375
3C	0	0	1	1	1	1	0	0	1.23750
3D	0	0	1	1	1	1	0	1	1.23125
3E	0	0	1	1	1	1	1	0	1.22500
3F	0	0	1	1	1	1	1	1	1.21875
40	0	1	0	0	0	0	0	0	1.21250
41	0	1	0	0	0	0	0	1	1.20625
42	0	1	0	0	0	0	1	0	1.20000
43	0	1	0	0	0	0	1	1	1.19375
44	0	1	0	0	0	1	0	0	1.18750
45	0	1	0	0	0	1	0	1	1.18125
46	0	1	0	0	0	1	1	0	1.17500
47	0	1	0	0	0	1	1	1	1.16875
48	0	1	0	0	1	0	0	0	1.16250
49	0	1	0	0	1	0	0	1	1.15625
4A	0	1	0	0	1	0	1	0	1.15000
4B	0	1	0	0	1	0	1	1	1.14375
4C	0	1	0	0	1	1	0	0	1.13750

Table 5. VID Table (continued)

VID									VDAC
Hex	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
4D	0	1	0	0	1	1	0	1	1.13125
4E	0	1	0	0	1	1	1	0	1.12500
4F	0	1	0	0	1	1	1	1	1.11875
50	0	1	0	1	0	0	0	0	1.11250
51	0	1	0	1	0	0	0	1	1.10625
52	0	1	0	1	0	0	1	0	1.10000
53	0	1	0	1	0	0	1	1	1.09375
54	0	1	0	1	0	1	0	0	1.08750
55	0	1	0	1	0	1	0	1	1.08125
56	0	1	0	1	0	1	1	0	1.07500
57	0	1	0	1	0	1	1	1	1.06875
58	0	1	0	1	1	0	0	0	1.06250
59	0	1	0	1	1	0	0	1	1.05625
5A	0	1	0	1	1	0	1	0	1.05000
5B	0	1	0	1	1	0	1	1	1.04375
5C	0	1	0	1	1	1	0	0	1.03750
5D	0	1	0	1	1	1	0	1	1.03125
5E	0	1	0	1	1	1	1	0	1.02500
5F	0	1	0	1	1	1	1	1	1.01875
60	0	1	1	0	0	0	0	0	1.01250
61	0	1	1	0	0	0	0	1	1.00625
62	0	1	1	0	0	0	1	0	1.00000
63	0	1	1	0	0	0	1	1	0.99375
64	0	1	1	0	0	1	0	0	0.98750
65	0	1	1	0	0	1	0	1	0.98125
66	0	1	1	0	0	1	1	0	0.97500
67	0	1	1	0	0	1	1	1	0.96875
68	0	1	1	0	1	0	0	0	0.96250
69	0	1	1	0	1	0	0	1	0.95625
6A	0	1	1	0	1	0	1	0	0.95000
6B	0	1	1	0	1	0	1	1	0.94375
6C	0	1	1	0	1	1	0	0	0.93750
6D	0	1	1	0	1	1	0	1	0.93125
6E	0	1	1	0	1	1	1	0	0.92500
6F	0	1	1	0	1	1	1	1	0.91875
70	0	1	1	1	0	0	0	0	0.91250
71	0	1	1	1	0	0	0	1	0.90625
72	0	1	1	1	0	0	1	0	0.90000
73	0	1	1	1	0	0	1	1	0.89375
74	0	1	1	1	0	1	0	0	0.88750
75	0	1	1	1	0	1	0	1	0.88125
76	0	1	1	1	0	1	1	0	0.87500
77	0	1	1	1	0	1	1	1	0.86875
78	0	1	1	1	1	0	0	0	0.86250
79	0	1	1	1	1	0	0	1	0.85625
7A	0	1	1	1	1	0	1	0	0.85000
7B	0	1	1	1	1	0	1	1	0.84375
7C	0	1	1	1	1	1	0	0	0.83750
7D	0	1	1	1	1	1	0	1	0.83125
7E	0	1	1	1	1	1	1	0	0.82500
7F	0	1	1	1	1	1	1	1	0.81875
80	1	0	0	0	0	0	0	0	0.81250
81	1	0	0	0	0	0	0	1	0.80625
82	1	0	0	0	0	0	1	0	0.80000
83	1	0	0	0	0	0	1	1	0.79375

Table 5. VID Table (continued)

VID									VDAC
Hex	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
84	1	0	0	0	0	1	0	0	0.78750
85	1	0	0	0	0	1	0	1	0.78125
86	1	0	0	0	0	1	1	0	0.77500
87	1	0	0	0	0	1	1	1	0.76875
88	1	0	0	0	1	0	0	0	0.76250
89	1	0	0	0	1	0	0	1	0.75625
8A	1	0	0	0	1	0	1	0	0.75000
8B	1	0	0	0	1	0	1	1	0.74375
8C	1	0	0	0	1	1	0	0	0.73750
8D	1	0	0	0	1	1	0	1	0.73125
8E	1	0	0	0	1	1	1	0	0.72500
8F	1	0	0	0	1	1	1	1	0.71875
90	1	0	0	1	0	0	0	0	0.71250
91	1	0	0	1	0	0	0	1	0.70625
92	1	0	0	1	0	0	1	0	0.70000
93	1	0	0	1	0	0	1	1	0.69375
94	1	0	0	1	0	1	0	0	0.68750
95	1	0	0	1	0	1	0	1	0.68125
96	1	0	0	1	0	1	1	0	0.67500
97	1	0	0	1	0	1	1	1	0.66875
98	1	0	0	1	1	0	0	0	0.66250
99	1	0	0	1	1	0	0	1	0.65625
9A	1	0	0	1	1	0	1	0	0.65000
9B	1	0	0	1	1	0	1	1	0.64375
9C	1	0	0	1	1	1	0	0	0.63750
9D	1	0	0	1	1	1	0	1	0.63125
9E	1	0	0	1	1	1	1	0	0.62500
9F	1	0	0	1	1	1	1	1	0.61875
A0	1	0	1	0	0	0	0	0	0.61250
A1	1	0	1	0	0	0	0	1	0.60625
A2	1	0	1	0	0	0	1	0	0.60000
A3	1	0	1	0	0	0	1	1	0.59375
A4	1	0	1	0	0	1	0	0	0.58750
A5	1	0	1	0	0	1	0	1	0.58125
A6	1	0	1	0	0	1	1	0	0.57500
A7	1	0	1	0	0	1	1	1	0.56875
A8	1	0	1	0	1	0	0	0	0.56250
A9	1	0	1	0	1	0	0	1	0.55625
AA	1	0	1	0	1	0	1	0	0.55000
AB	1	0	1	0	1	0	1	1	0.54375
AC	1	0	1	0	1	1	0	0	0.53750
AD	1	0	1	0	1	1	0	1	0.53125
AE	1	0	1	0	1	1	1	0	0.52500
AF	1	0	1	0	1	1	1	1	0.51875
B0	1	0	1	1	0	0	0	0	0.51250
B1	1	0	1	1	0	0	0	1	0.50625
B2	1	0	1	1	0	0	1	0	0.50000
B3	1	0	1	1	0	0	1	1	0.49375
B4	1	0	1	1	0	1	0	0	0.48750
B5	1	0	1	1	0	1	0	1	0.48125
B6	1	0	1	1	0	1	1	0	0.47500
B7	1	0	1	1	0	1	1	1	0.46875
B8	1	0	1	1	1	0	0	0	0.46250
B9	1	0	1	1	1	0	0	1	0.45625
BA	1	0	1	1	1	0	1	0	0.45000

Table 5. VID Table (continued)

VID									VDAC
Hex	7	6	5	4	3	2	1	0	
BB	1	0	1	1	1	0	1	1	0.44375
BC	1	0	1	1	1	1	0	0	0.43750
BD	1	0	1	1	1	1	0	1	0.43125
BE	1	0	1	1	1	1	1	0	0.42500
BF	1	0	1	1	1	1	1	1	0.41875
C0	1	1	0	0	0	0	0	0	0.41250
C1	1	1	0	0	0	0	0	1	0.40625
C2	1	1	0	0	0	0	1	0	0.40000
C3	1	1	0	0	0	0	1	1	0.39375
C4	1	1	0	0	0	1	0	0	0.38750
C5	1	1	0	0	0	1	0	1	0.38125
C6	1	1	0	0	0	1	1	0	0.37500
C7	1	1	0	0	0	1	1	1	0.36875
C8	1	1	0	0	1	0	0	0	0.36250
C9	1	1	0	0	1	0	0	1	0.35625
CA	1	1	0	0	1	0	1	0	0.35000
CB	1	1	0	0	1	0	1	1	0.34375
CC	1	1	0	0	1	1	0	0	0.33750
CD	1	1	0	0	1	1	0	1	0.33125
CE	1	1	0	0	1	1	1	0	0.32500
CF	1	1	0	0	1	1	1	1	0.31875
D0	1	1	0	1	0	0	0	0	0.31250
D1	1	1	0	1	0	0	0	1	0.30625
D2	1	1	0	1	0	0	1	0	0.30000
D3	1	1	0	1	0	0	1	1	0.29375(1)
D4	1	1	0	1	0	1	0	0	0.28750(1)
D5	1	1	0	1	0	1	0	1	0.28125(1)
D6	1	1	0	1	0	1	1	0	0.27500(1)
D7	1	1	0	1	0	1	1	1	0.26875(1)
D8	1	1	0	1	1	0	0	0	0.26250(1)
D9	1	1	0	1	1	0	0	1	0.25625(1)
DA	1	1	0	1	1	0	1	0	0.25000(1)
DB	1	1	0	1	1	0	1	1	0.24375(1)
DC	1	1	0	1	1	1	0	0	0.23750(1)
DD	1	1	0	1	1	1	0	1	0.23125(1)
DE	1	1	0	1	1	1	1	0	0.22500(1)
DF	1	1	0	1	1	1	1	1	0.21875(1)

Table 5. VID Table (continued)

VID									VDAC
Hex	7	6	5	4	3	2	1	0	
E0	1	1	1	0	0	0	0	0	0.21250(1)
E1	1	1	1	0	0	0	0	1	0.20625(1)
E2	1	1	1	0	0	0	1	0	0.20000(1)
E3	1	1	1	0	0	0	1	1	0.19375(1)
E4	1	1	1	0	0	1	0	0	0.18750(1)
E5	1	1	1	0	0	1	0	1	0.18125(1)
E6	1	1	1	0	0	1	1	0	0.17500(1)
E7	1	1	1	0	0	1	1	1	0.16875(1)
E8	1	1	1	0	1	0	0	0	0.16250(1)
E9	1	1	1	0	1	0	0	1	0.15625(1)
EA	1	1	1	0	1	0	1	0	0.15000(1)
EB	1	1	1	0	1	0	1	1	0.14375(1)
EC	1	1	1	0	1	1	0	0	0.13750(1)
ED	1	1	1	0	1	1	0	1	0.13125(1)
EE	1	1	1	0	1	1	1	0	0.12500(1)
EF	1	1	1	0	1	1	1	1	0.11875(1)
F0	1	1	1	1	0	0	0	0	0.11250(1)
F1	1	1	1	1	0	0	0	1	0.10625(1)
F2	1	1	1	1	0	0	1	0	0.10000(1)
F3	1	1	1	1	0	0	1	1	0.09375(1)
F4	1	1	1	1	0	1	0	0	0.08750(1)
F5	1	1	1	1	0	1	0	1	0.08125(1)
F6	1	1	1	1	0	1	1	0	0.07500(1)
F7	1	1	1	1	0	1	1	1	0.06875(1)
F8	1	1	1	1	1	0	0	0	0.06250(1)
F9	1	1	1	1	1	0	0	1	0.05625(1)
FA	1	1	1	1	1	0	1	0	0.05000(1)
FB	1	1	1	1	1	0	1	1	0.04375(1)
FC	1	1	1	1	1	1	0	0	0.03750(1)
FD	1	1	1	1	1	1	0	1	0.03125(1)
FE	1	1	1	1	1	1	1	0	OFF
FF	1	1	1	1	1	1	1	1	OFF

(1) Device operating characteristics and tolerances below 0.3 V are not specified.

APPLICATION INFORMATION

Design Procedure

The TPS53624 has the simplest design procedure of any IMVP6.5 $_{\text{CORE}}$ controller on the market.

Choosing Initial Parameters

Step One

Determine the processor specifications. For the purposes of this document, the Intel® Auburndale 45-V Processor from Table 2 of the RS – Intel® IMVP-6.5 Mobile Processor and Mobile Chipset Voltage Regulation Specification, Reference Number 24779, Revision 1.0 is used.

The processor requirements provide the following key parameters.

- V_{HFM} = 1.075 V
- R_{IMVP} = -1.9 mΩ
- $I_{CC(max)}$ = 50 A
- $I_{DYN(max)}$ = 35 A
- $I_{CC(tdc)}$ = 37 A
- Slew rate = 5 mV/µs (minimum)

The last requirement shows that the converter must support a 25% overcurrent for 10 µs without going out of tolerance. The TPS53624 is designed to support the momentary OCP requirement internally, so only the DC OCP limit needs to be considered when calculating OCP levels. This also means that the power-chain does not have to be over-designed to meet Intel requirements.

Step Two

Determine system parameters.

The input voltage range and operating frequency are of primary interest.

For example

- $V_{IN(max)}$ = 20 V
- $V_{IN(min)}$ = 9 V
- f_{SW} = 300 kHz

Step Three

Determine current sensing method.

The TPS53624 supports both resistor sensing and inductor DCR sensing. Inductor DCR sensing is chosen.

For resistor sensing, substitute the resistor value (1 mΩ recommended for a 50-A application) for R_{CS} in the subsequent equations and skip Step Five.

Step Four

Determine inductor value and choose inductor.

Smaller inductor values have better transient performance but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to between 30% and 50% of the maximum current per phase. In this case, use 40%:

$$I_{P-P} = \frac{50\,A}{2\,\text{phases}} \times 0.4 = 10\,A \tag{7}$$

At f_{SW} = 300 kHz, with a 20-V input and a 1.075-V output.

$$L = \frac{V \times dT}{I_{P-P}}$$

where

- $V = \left(V_{IN(max)} - V_{HFM}\right)$
- $dT = \left(\frac{V_{HFM}}{\left(f \times V_{IN(max)}\right)}\right)$ (8)

L=0.34 µH

An inductance value of 0.36 µH is chosen. Ensure that the inductor does not saturate during peak loading conditions.

$$I_{SAT} = \left(\frac{I_{CC(max)}}{N_{PHASE}} + \frac{I_{P-P}}{2}\right) \times 1.2 \times 1.25 = 45\,A \tag{9}$$

The factor of 1.2 is included to allow for current sensing and current limiting tolerances. The factor of 1.25 is due to Intel’s 25% momentary OCP requirement described above.

The chosen inductor should have the following characteristics:

- As flat an inductance vs. current curve as possible. Inductor DCR sensing is based on the idea L/DCR is approximately a constant through the current range of interest.
- Either high saturation or *soft saturation*
- Low DCR for improved efficiency, but at least 0.7 mΩ for proper signal levels.
- DCR tolerance as low as possible for load-line accuracy.

For this application, a 0.36-µH, 1.0-mΩ inductor is chosen.

Step Five

Design the thermal compensation network.

In most designs, NTC thermistors are used to compensate thermal variations in the resistance of the inductor winding. This winding is generally copper, and therefore has a resistance coefficient of 3900 PPM/°C. NTC thermistors, however, have very non-linear characteristics and need two or three resistors to linearize them over the range of interest. The typical DCR circuit is shown in Figure 8.

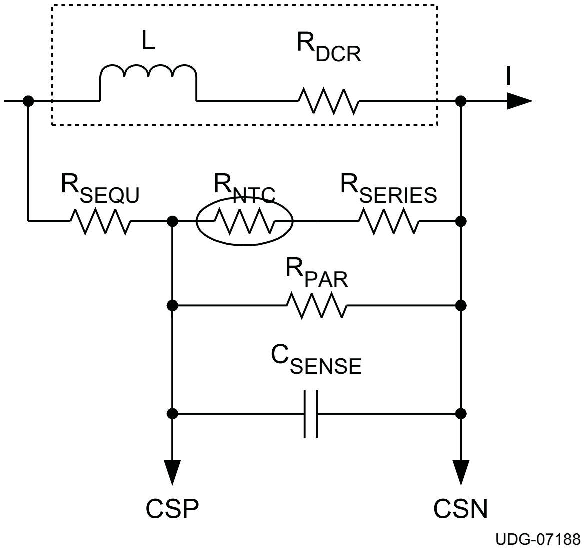


Figure 8. Typical DCR Sensing Circuit

In this circuit, good performance is obtained when:

$$\frac{L}{R_{DCR}} = C_{SENSE} \times R_{EQ} \tag{10}$$

In Equation 10, all of the parameters are defined in Figure 8 except R_{EQ}, which is the series/parallel combination of the other four discrete resistors. C_{SENSE} should be a capacitor type which is stable over temperature. Use X7R or better dielectric (C0G preferred).

Because calculating these values by hand is difficult, TI offers a spreadsheet using the Excel *Solver* function. Contact your local TI representative to get a copy of the spreadsheet.

In the reference design, the following values are input to the spreadsheet:

- L = 0.36 µH
- R_{DCR} = 1 mΩ
- Load Line (typically -1.9 mΩ for SV processors)
- Minimum overcurrent limit = 56 A
- Thermistor R_{25} and “B” value = 4700 kΩ

The spreadsheet then calculates the TRIPSEL setting and the values of:

- R_{SEQU}
- R_{SERIES}
- R_{PAR}
- C_{SENSE}

In this case, the TRIPSEL setting is TRIPSEL = 5 V with R_{SLEW} to GND and the nearest standard component values are:

- R_{SERIES} = 43.2 kΩ
- R_{PAR} = 143 kΩ
- R_{SEQU} = 24.3 kΩ
- C_{SENSE} = 18 nF

Note the effective divider ratio for the inductor DCR. The effective current sense resistance ($R_{CS(eff)}$) is shown in Equation 11.

$$R_{CS(eff)} = R_{DCR} \times \frac{R_{P\_N}}{R_{SEQU} + R_{P\_N}}$$

where

- R_{P_N} is the series/parallel combination of $R_{NTC}R_{SERIES}$ and R_{PAR} (11)

$$R_{P\_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \tag{12}$$

$R_{CS(eff)}$ is 0.77 mΩ.

Step Six

Determine the output capacitor configuration.

Intel has several recommended configurations in the specifications. The TPS53624 meets every requirement with margin using the minimum configuration given in the Intel specification (Option 3). Depending on the layout, it is possible to reduce the output capacitance further, or to use alternate capacitor technologies. A good rule of thumb is that a successful design has a combination of bulk and ceramic capacitance totaling at least 1600 µF.

Step Seven

Set the load line.

The load line is set by the droop resistor using R_{IMVP} and $R_{CS(eff)}$.

$$R_{DROOP} = \frac{R_{CS(eff)} \times A_{CS}}{G_M \times R_{IMVP}} = 4.75\,k\Omega \tag{13}$$

Step Eight

Calculate the droop capacitor value.

$$C_{DROOP} = \frac{R_{LL} \times \Delta I_{OUT} \times g_M \times L}{R_{CS} \times A_{CS} \times D_{MAX} \times V(L)} - 30\,pF = 105\,pF \tag{14}$$

Because better overall transient performance is obtained by allowing a small ring-back, a small value capacitor (between 33 pF and 68 pF) is used. This capacitor also helps in eliminating any noise that may be present at the DROOP pin.

Step Nine

Calculate R_{SLEW}.

R_{SLEW} sets the slew rate and the soft-start rate. The soft-start rate is 1/8 of the slew rate. Given the Intel requirements, the slew rate minimum requirement is 5 mV/µs.

$$R_{SLEW} = \frac{K_{SLEW} \times V_{SLEW}}{SR}$$

here

- From the overcurrent limit setting in Step Five, R_{SLEW} is terminated to GND
- $K_{SLEW} = 1.25 \times 10^9$
- $V_{SLEW} = 1.25$ V (15)

Taking into account the tolerance on K_{SLEW}, R_{SLEW} = 250 kΩ.

Step Ten

Calculate R_{IMON}.

R_{IMON} is calculated to set the voltage on the IMON pin to approximately 1.0 V at maximum processor current.

$$R_{IMON} = \frac{V_{IMON}}{K_{IMON} \times I_{CC(max)} \times R_{CS(eff)}} \; (\Omega)$$

here

- V_{IMON} = 1.0 V
- K_{IMON} = 2 µA/mV
- $I_{CC(max)}$ = 50 A
- $R_{CS(eff)}$ = 0.77 mΩ
- R_{IMON} = 13.1 kΩ
- C_{IMON} = 3300pF and is added in parallel to R_{IMON} to give a smooth response on IMON pin. (16)

Step Eleven

Calculate THAL pin components.

The THERM pin produces a nominal 61 µA current. The trip voltage is 0.75 V. Therefore, the resistance at the trip point needs to be 0.75V / 61 µA = 12.3 kΩ. For a trip temperature of 85°C, the recommended 150 kΩ NTC thermistor is 10.3 kΩ. To move the trip point to the correct resistance, we add a series resistance of 2.0 kΩ. Depending on the thermistors selection and desired trip point, adding a parallel resistance to obtain the correct resistance at the trip point is also possible. In order to keep the sensing as accurate as possible in both cases, the contribution of the fixed resistance at the trip point should be as small as possible.

- V5IN decoupling ≥ 2.2 µF, ≥ 10 V
- V5FILT decoupling ≥ 1 µF, ≥ 10 V
- VREF decoupling 0.22 µF to 1 µF, ≥ 4 V
- Bootstrap capacitors ≥ 0.22 µF, ≥ 10 V Bootstrap diodes (optional) 30 V Schottky diode, BAT-54 or better
- Pull-up resistors on PGOOD, $\overline{\text{PG}}$, THAL, and PCNT pins per Intel guidelines

For power chain and other component selection, see Table 2.

Step Twelve

Select decoupling and peripheral components.

For peripheral capacitors use the following minimum values of ceramic capacitance. A capacitor with an X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

- V5IN decoupling ≥ 2.2 µF, ≥ 10V
- V5FILT decoupling ≥ 1 µF, ≥ 10V
- VREF decoupling 0.22 µF to 1 µF, ≥ 4 V
- Bootstrap capacitors ≥ 0.22 µF, ≥ 10 V
- Bootstrap diodes (optional) 30 V Schottky diode, BAT-54 or better
- Pull-up resistors on PGOOD, $\overline{\text{PG}}$, THAL, and PCNT pins per Intel guidelines

Layout Guidelines

The TPS53624 has fully differential current and voltage feedback. As a result, no special layout considerations are required. However, all high-performance multi-phase power converters, like the TPS53624, require a certain level of care in layout.

Schematic Review

Because the voltage and current feedback signals are fully differential it is a good idea to double check the polarity.

- CSP1 / CSN1
- CSP2 / CSN2
- VCCSENSE to VFB / VSSSENSE to GSNS

Specific Guidelines

Separate Noisy Driver Interface Lines from Sensitive Analog Interface Lines

The TPS53624 makes this as easy as possible, as the two sets of pins are on opposite sides of the device. In addition, the CPU interface signals are grouped on one side of the device, and the MCH and platform interface signals are grouped on the opposite side. This arrangement is shown in Figure 9.

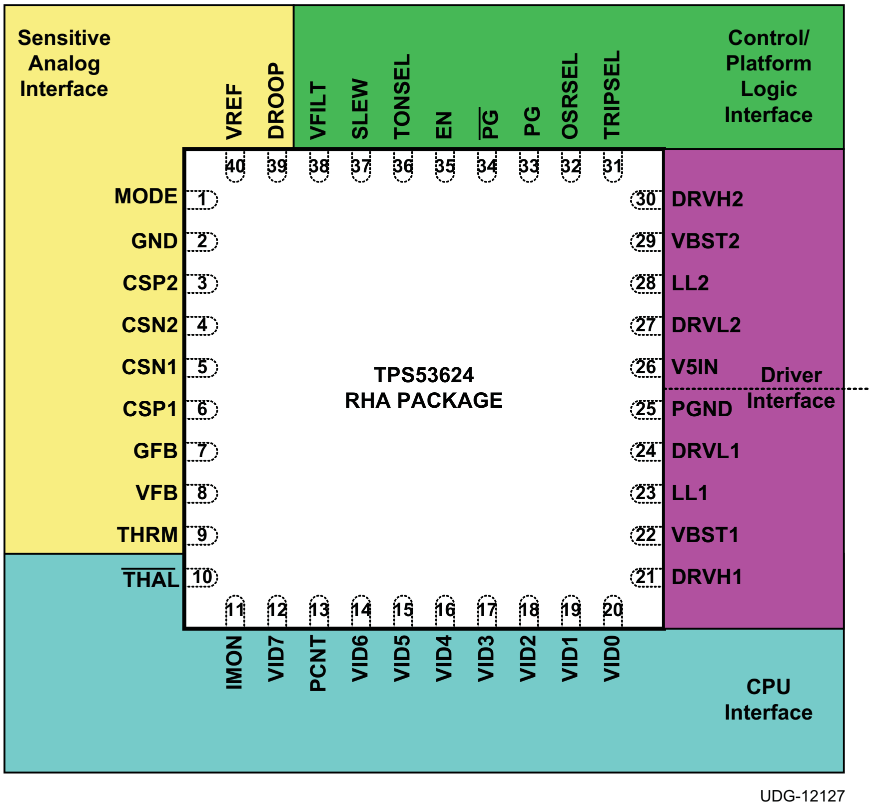


Figure 9. Device Layout by Pin Function

Given the physical layout of most systems, the current feedback (CSPx, CSNx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS53624. This requires the designer take the following precautions.

- Make a Kelvin connection to the pads of the resistor or inductor used for current sensing. See Figure 10 for a layout example.
- Lay out the current feedback signals as a differential pair to the device.
- Lay out the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane.

- Design the compensation capacitor for DCR sensing (C_{SENSE}) as close to the CS pins as possible.
- Place R_{PAR} near C_{SENSE}.
- Place any noise filtering capacitors directly under the TPS53624 and connect to the CS pins with the shortest trace length possible.

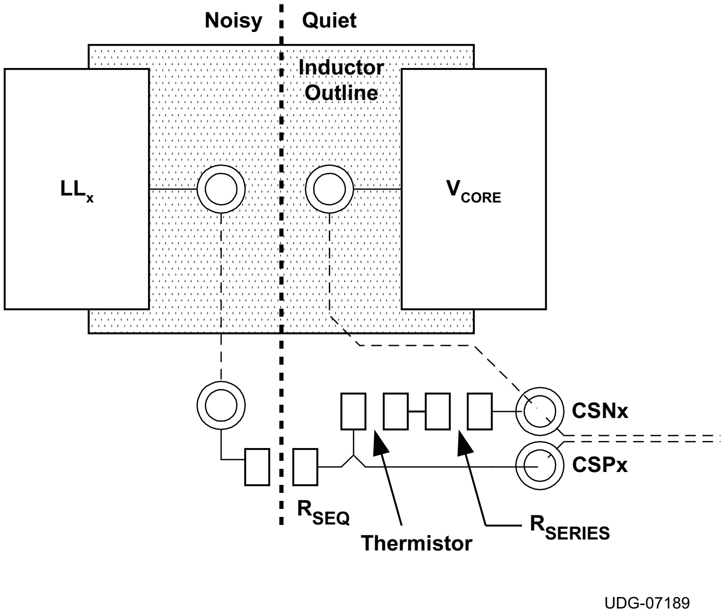


Figure 10. Make Kelvin Connections to the Inductor for DCR Sensing

- Ensure that all vias in the CSPx and CSNx traces are isolated from all other signals
- Lay out the dotted signal traces in internal planes
- If possible, change the name of the CSNx trace to prevent unintended connections to the V_{CORE} plane
- Design CSPx and CSNx as a differential pair in a quiet layer
- Design the capacittor as near to the device pins as possible

Minimize High Current Loops

Figure 11 shows the primary current loops in each phase, numbered in order of importance. The most important loop to minimize the area of is Loop 1, the path from the input capacitor through the high and low-side MOSFETs, and back to the capacitor through ground.

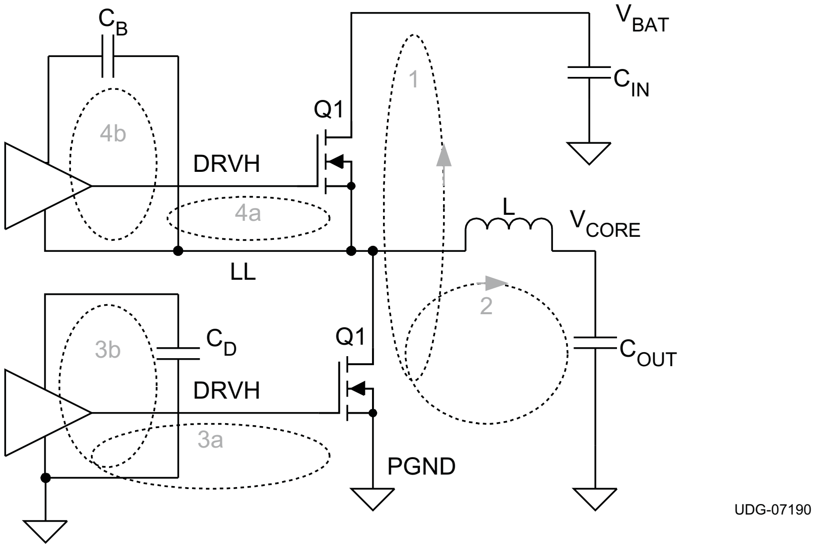


Figure 11. Major Current Loops Requiring Minimization

Loop 2 is from the inductor through the output capacitor, ground and Q2. The layout of the low-side gate drive (Loops 3a and 3b) is important. The guidelines for gate drive layout are:

- Make the low side gate drive as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible
- If changing layers is necessary, use at least two vias

Power Chain Symmetry

The TPS53624 does not require special care in the layout of the power chain components, because independent isolated current feedback is provided. Make every effort to lay out the phases in a symmetrical manner. The current feedback from each phase must be free of noise and have the same effective current sense resistance. A value of 1 mΩ of current feedback resistance is recommended.

Place Analog Components as Close to the Device as Possible

Place components close to the device in the following order.

1. CS pin noise filtering components
2. DROOP pin compensation component
3. Decoupling capacitor
4. SLEW resistor (R_{SLEW})

Grounding Recommendations

The TPS53624 has separate analog and power grounds, and a thermal pad. The normal procedure for connecting these is:

1. Connect the thermal pad to PGND.
2. Tie the thermal pad to the system ground plane with at least 4 small vias or one large via.
3. GND can be connected to any quiet space. A quiet space is defined as a spot where no power supply switching currents are likely to flow. This applies to both the VCORE regulator and other regulators. Use a single point connection to the point, and pour a GND island around the analog components.
4. Make sure the low-side MOSFET source connection and the decoupling capacitors have plenty of vias.

Decoupling Recommendations

- Decouple V5 to PGND with at least a 2.2-μF ceramic capacitor. This fits best on the opposite side of the device.
- Use double vias to connect to the device.
- Decouple V5FILT with 1-μF to AGND with leads as short as possible.
- Decouple VREF to AGND with 0.22-μF, with short leads as short as possible.

Conductor Widths

- Follow Intel guidelines with respect to the voltage feedback and logic interface connection requirements.
- Maximize the widths of power, ground and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers.
- Use a minimum of 1 via per ampere of current

TYPICAL CHARACTERISTICS

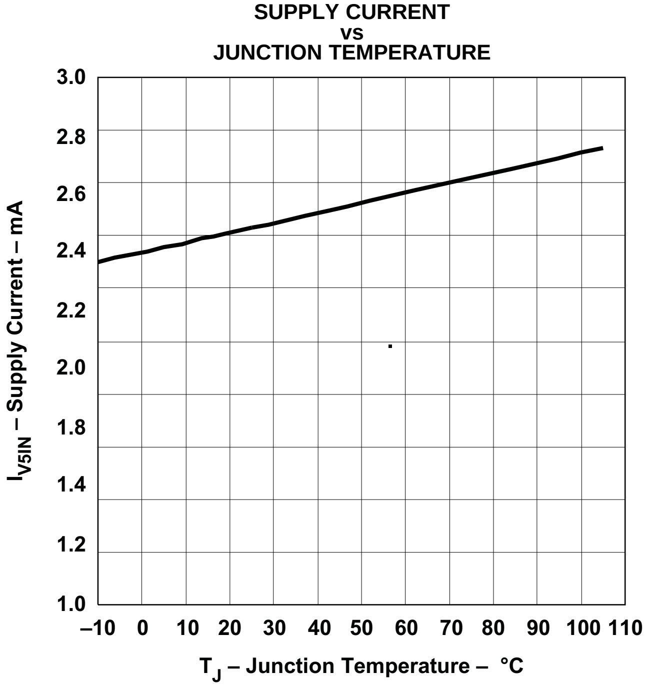


Figure 12.

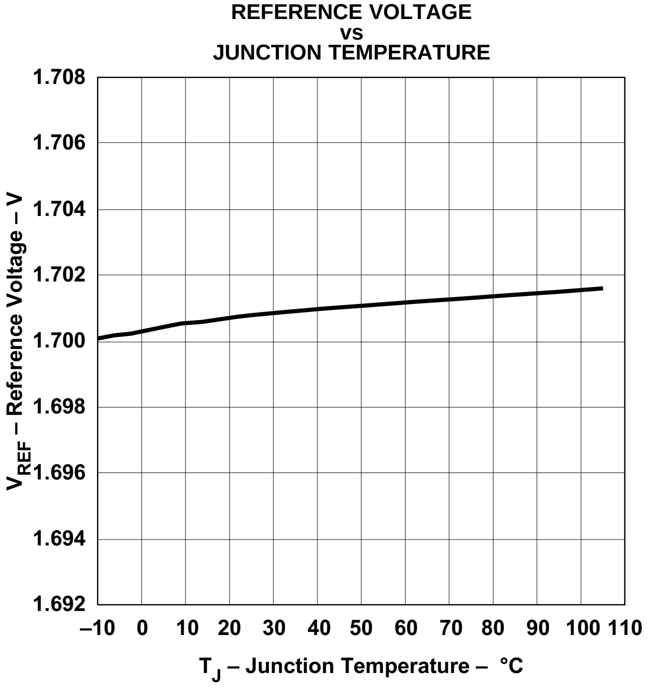


Figure 13.

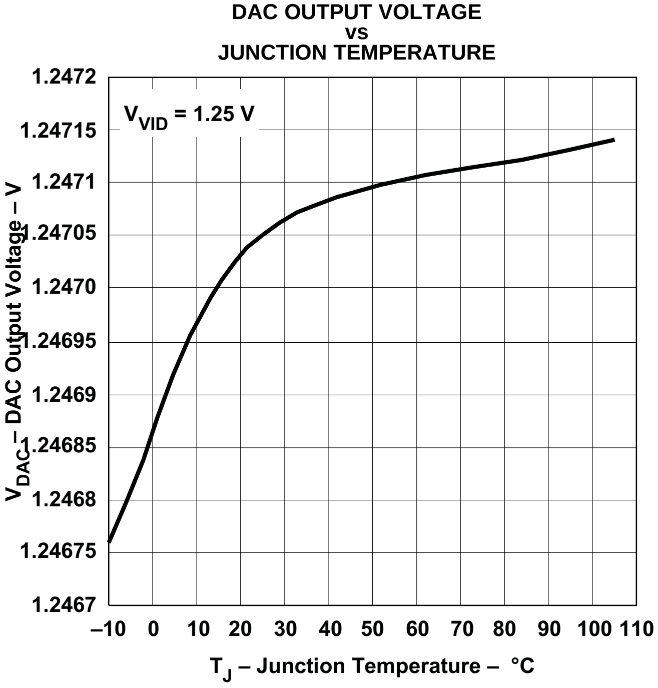


Figure 14.

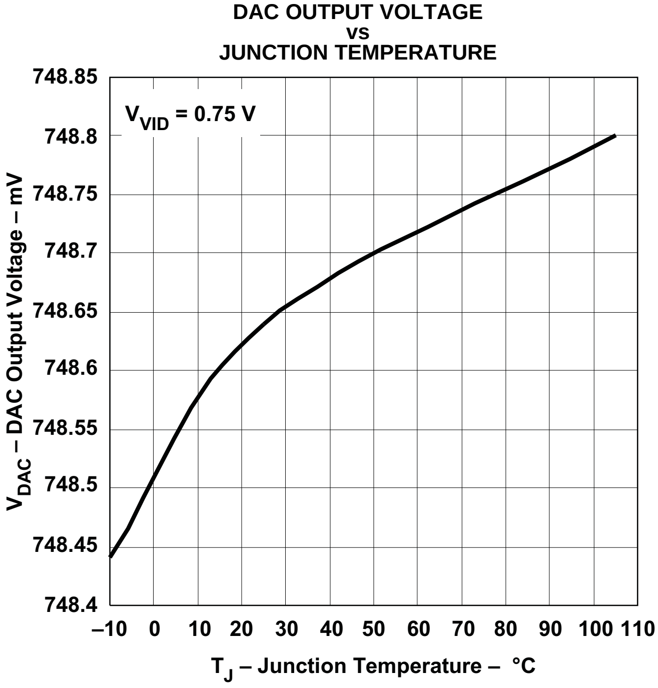


Figure 15.

TYPICAL CHARACTERISTICS (continued)

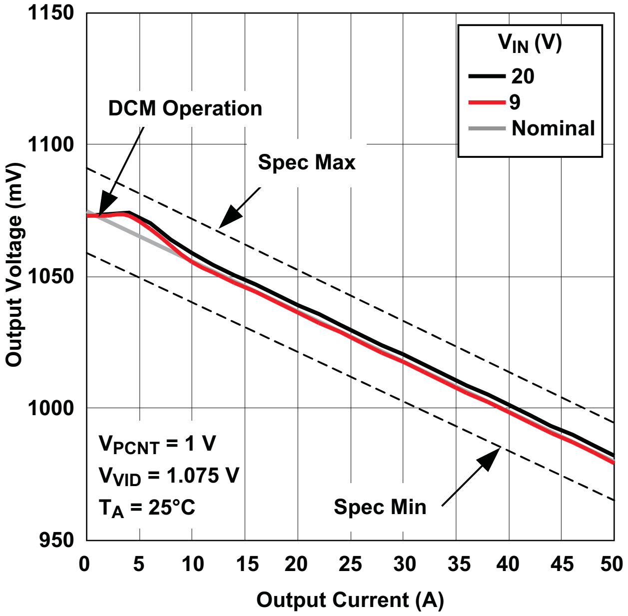

HIGH FREQUENCY OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 16.

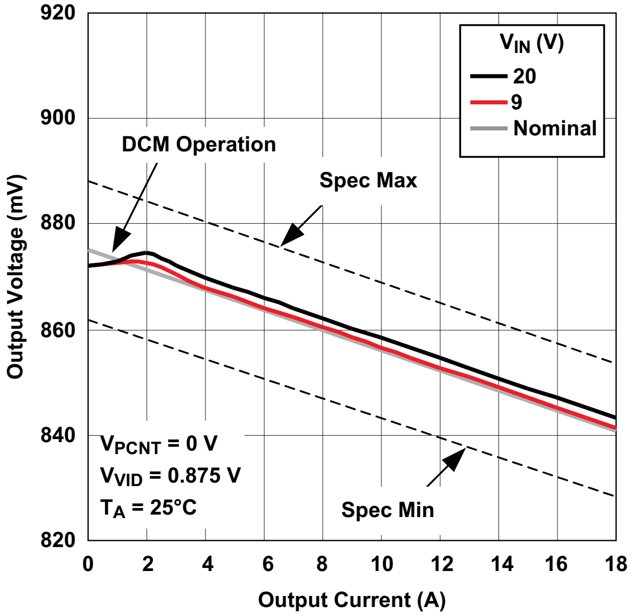

LOW FREQUENCY OUTPUT VOLTAGE
vs
OUTPUT CURRENT

Figure 17.

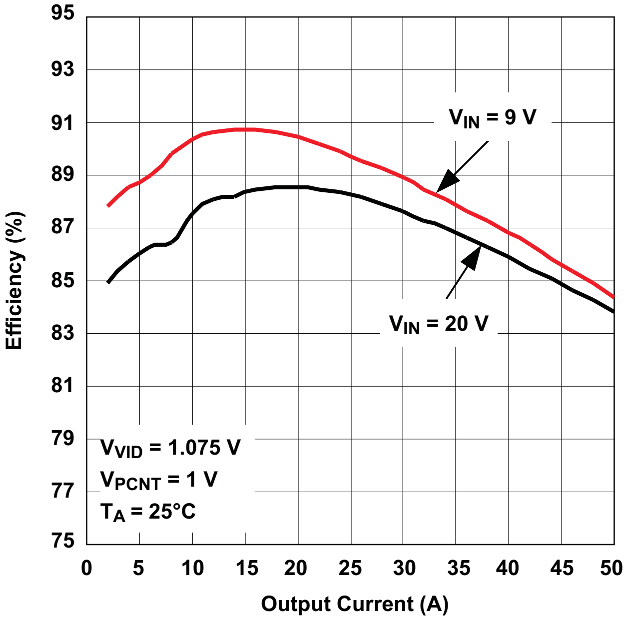

HIGH FREQUENCY MODE (HFM) EFFICIENCY
vs
OUTPUT CURRENT

Figure 18.

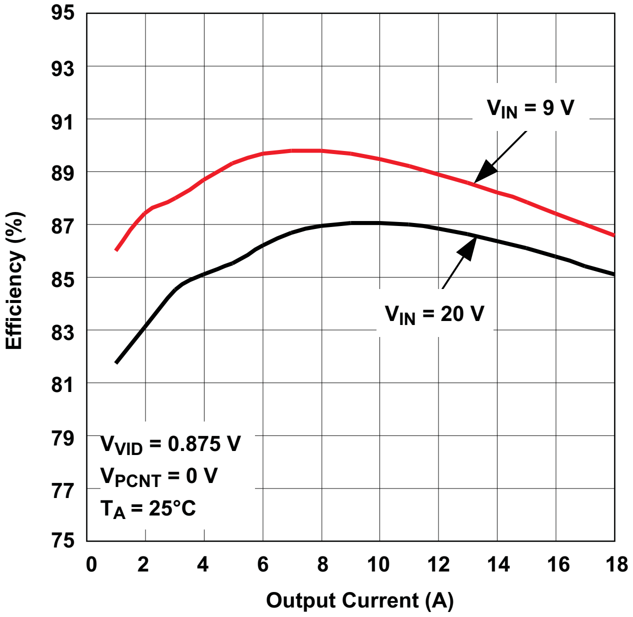

LOW FREQUENCY MODE (LFM) EFFICIENCY
vs
OUTPUT CURRENT

Figure 19.

TYPICAL CHARACTERISTICS (continued)

CURRENT SHARE IMBALANCE vs OUTPUT CURRENT

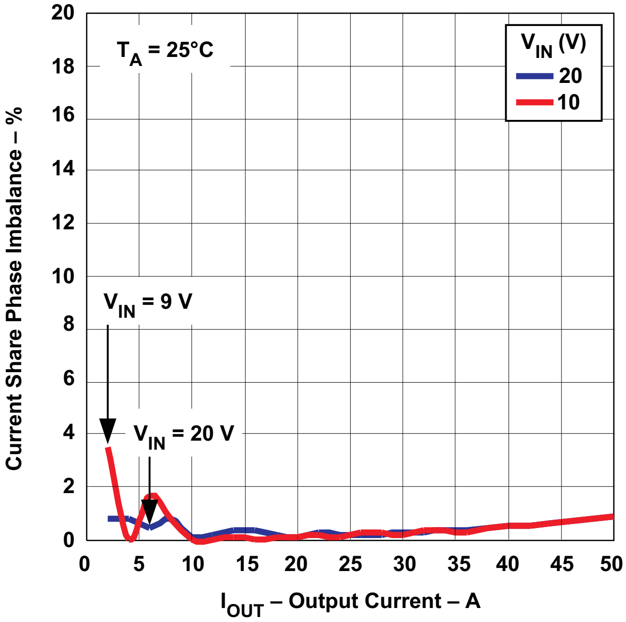


Figure 20.

CURRENT MONITOR VOLTAGE vs OUTPUT CURRENT

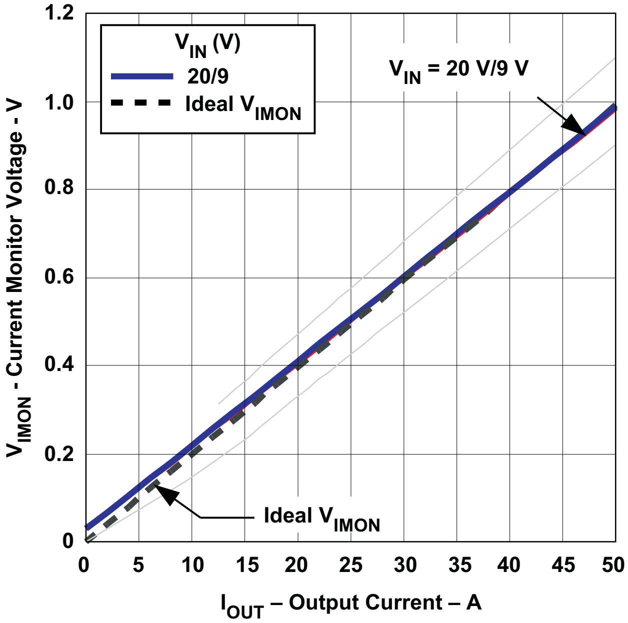


Figure 21.

VOLTAGE REFERENCE vs OUTPUT CURRENT

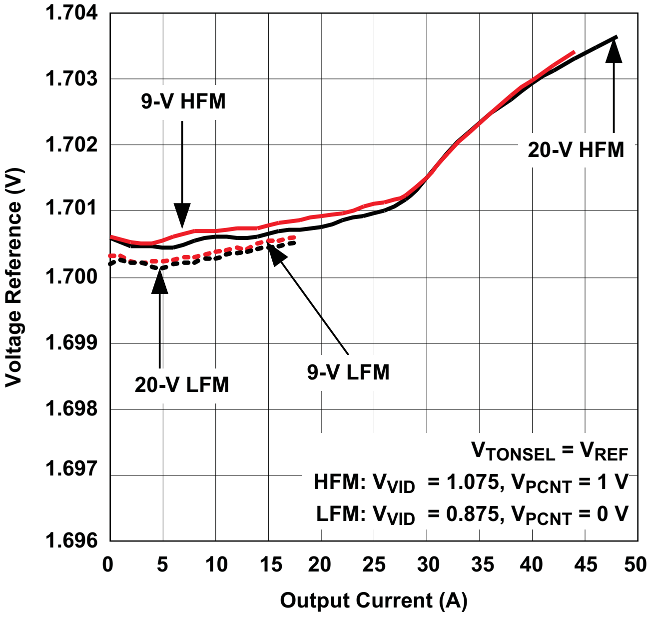


Figure 22.

OPERATING FREQUENCY vs OUTPUT CURRENT

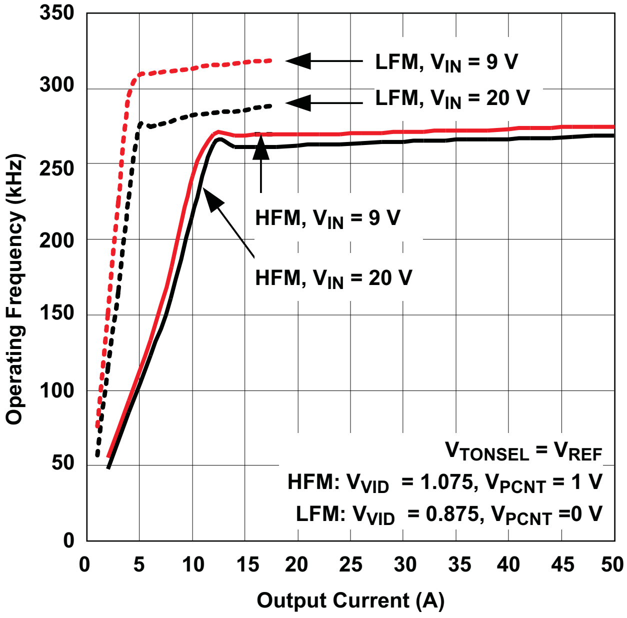


Figure 23.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
OUTPUT VOLTAGE

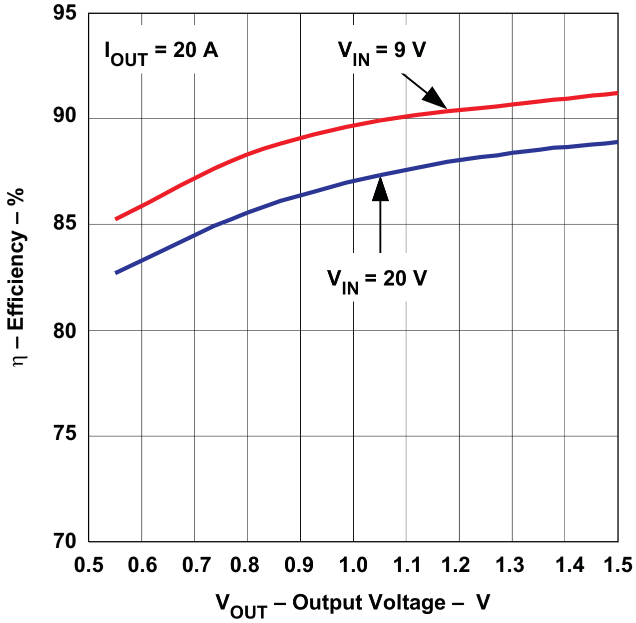


Figure 24.

EFFICIENCY
vs
INPUT VOLTAGE

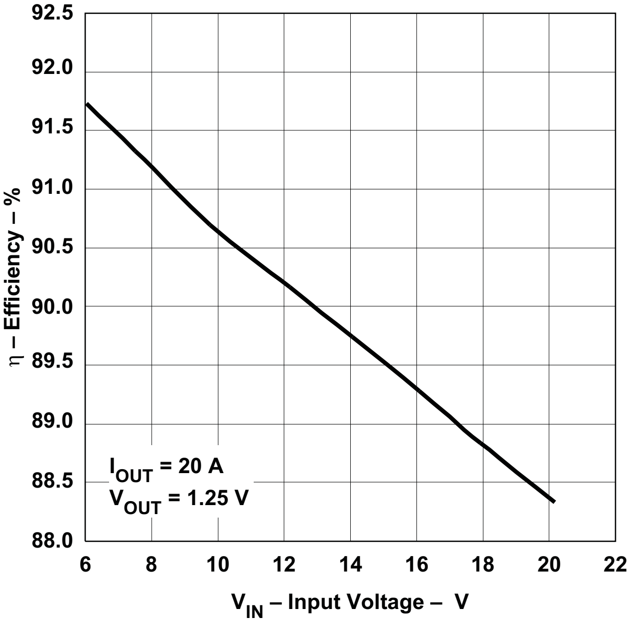


Figure 25.

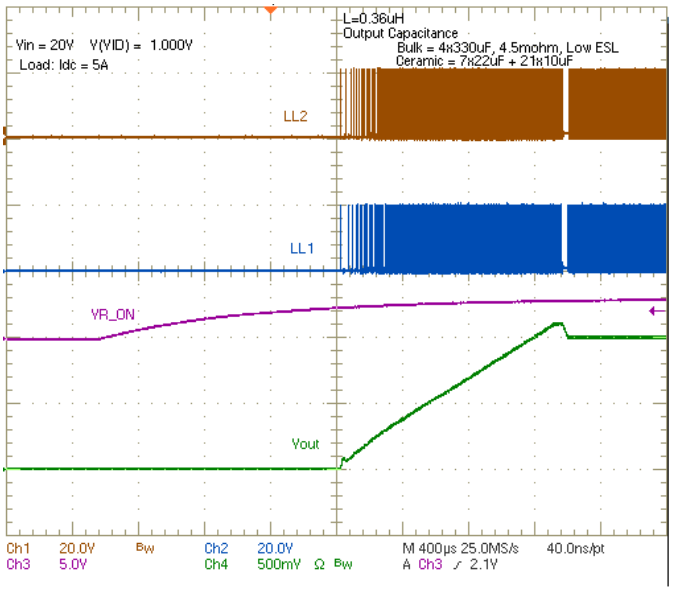


Figure 26. Start-Up, V_{IN} = 20 V

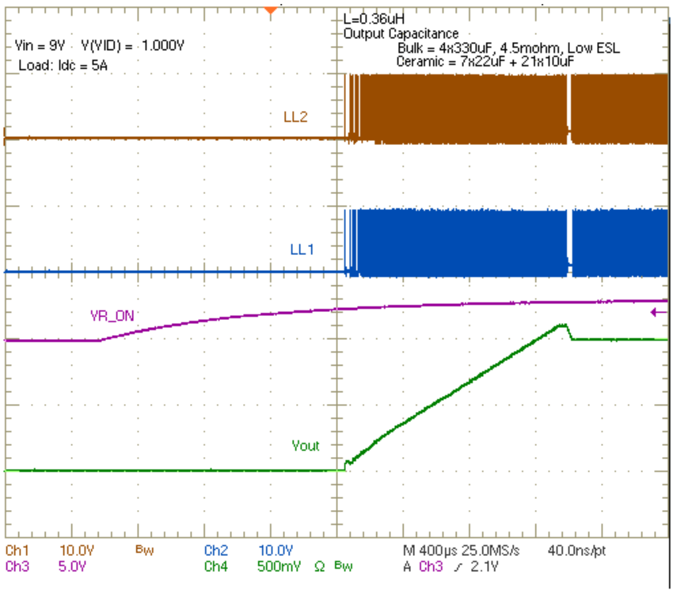


Figure 27. Start-Up, V_{IN} = 9 V

TYPICAL CHARACTERISTICS (continued)

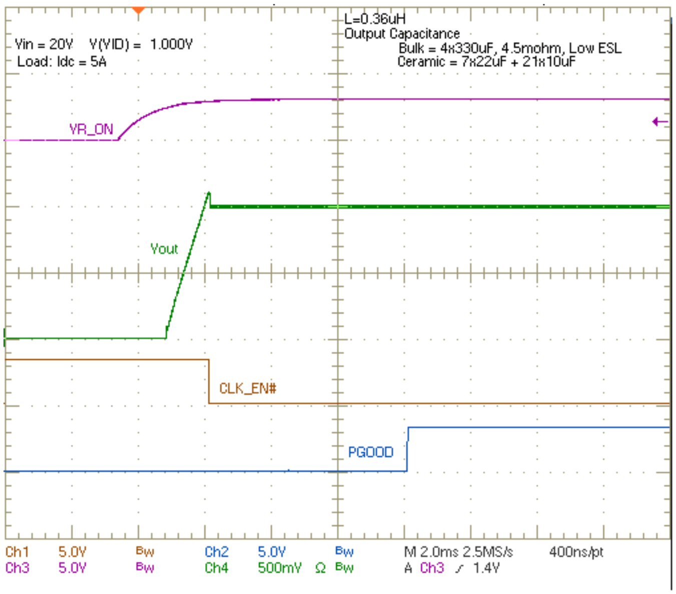


Figure 28. $\overline{PG}$ and PGOOD, V_{IN} = 20 V

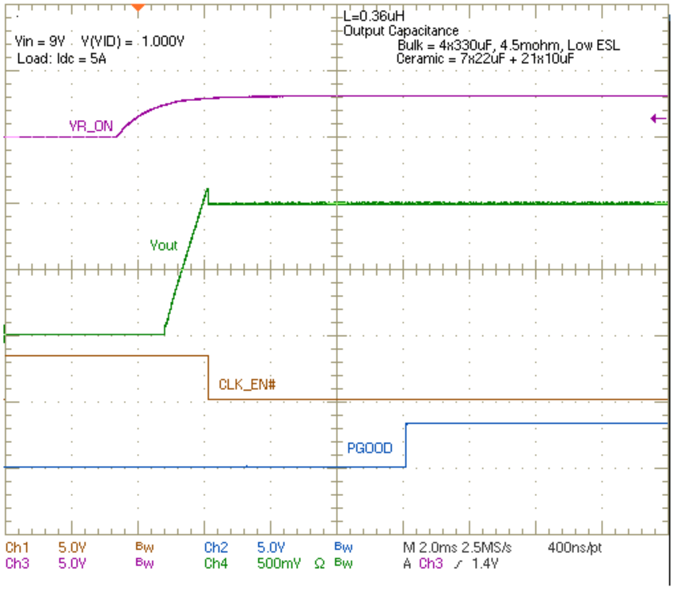


Figure 29. $\overline{PG}$ and PGOOD, V_{IN} = 9 V

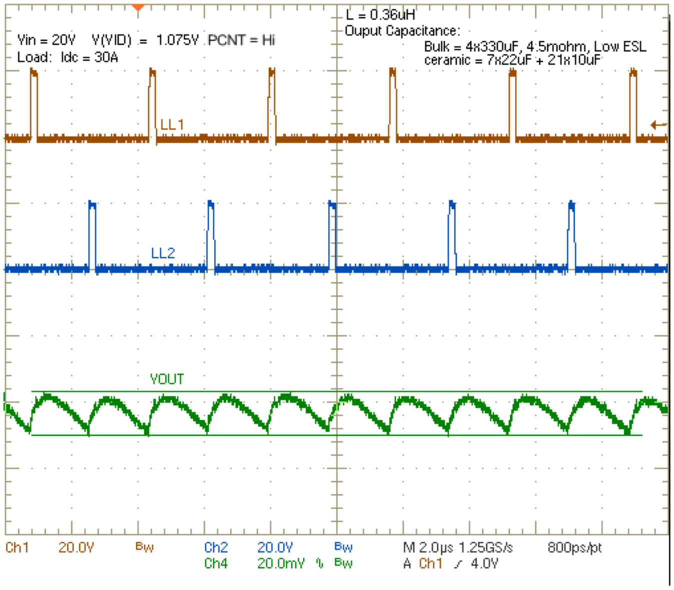


Figure 30. Output Ripple, V_{IN} = 20 V

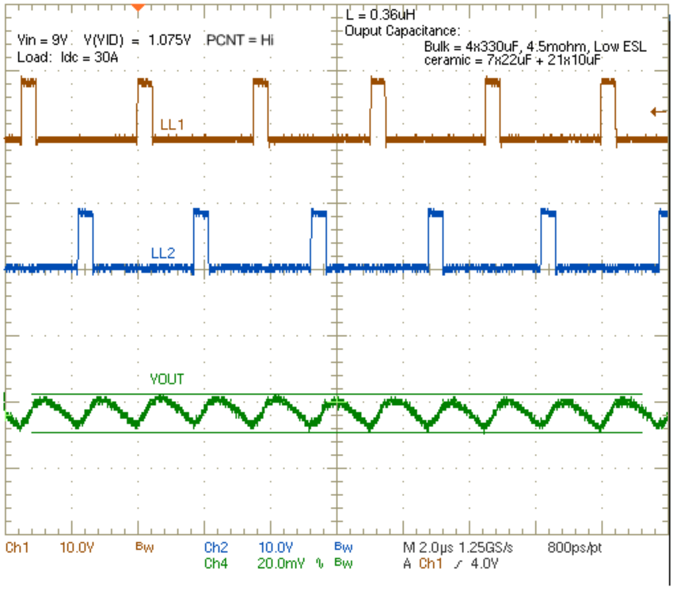


Figure 31. Output Ripple, V_{IN} = 9 V

TYPICAL CHARACTERISTICS (continued)

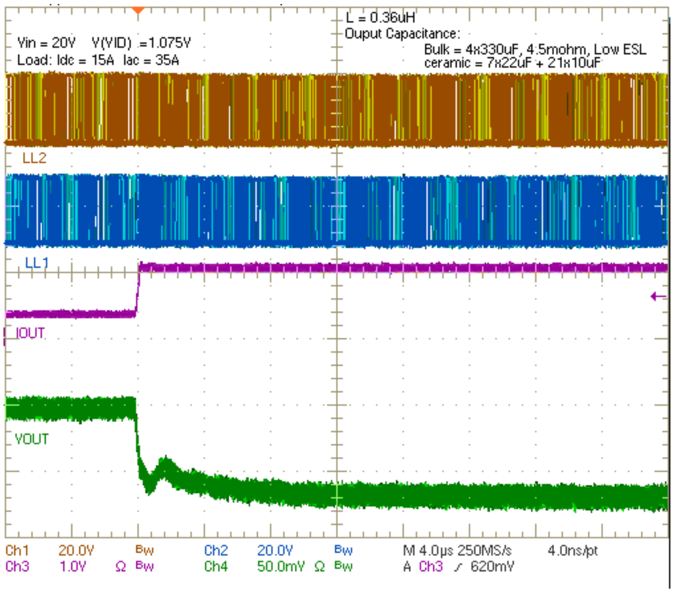


Figure 32. Load Insertion, V_{IN} = 20 V, I_{DC} = 15 A, I_{AC} = 35 A, Persistence Mode

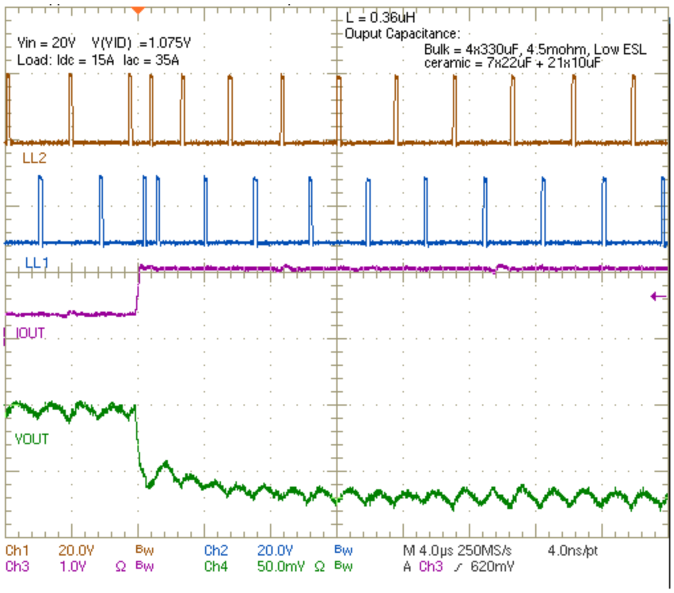


Figure 33. Load Insertion, V_{IN} = 20 V, I_{DC} = 15 A, I_{AC} = 35 A

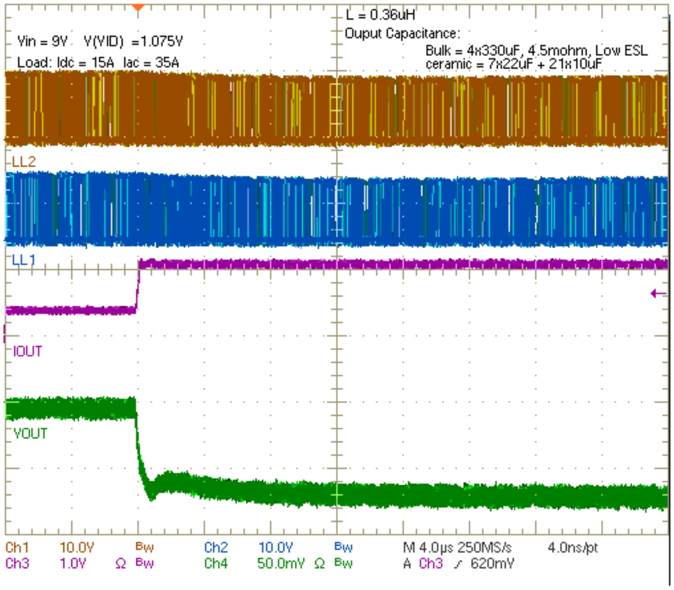


Figure 34. Load Insertion, V_{IN} = 9 V, I_{DC} = 15 A, I_{AC} = 35 A, Persistence Mode

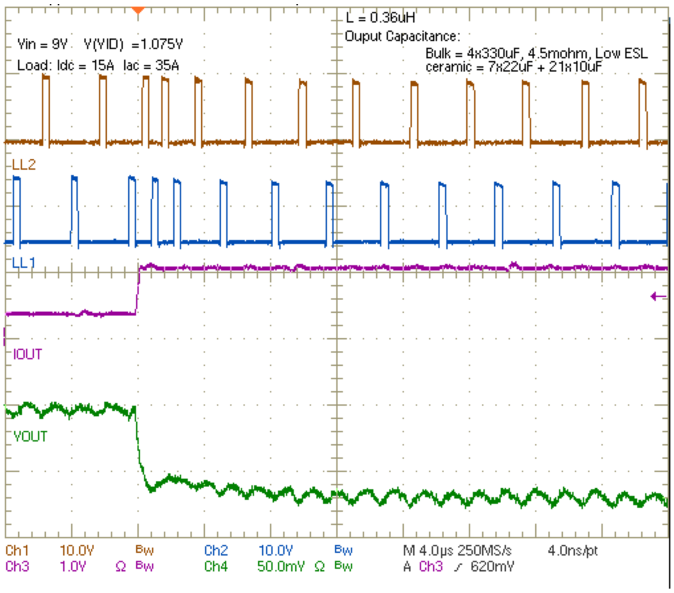


Figure 35. Load Insertion, V_{IN} = 9 V, I_{DC} = 15 A, I_{AC} = 35 A

TYPICAL CHARACTERISTICS (continued)

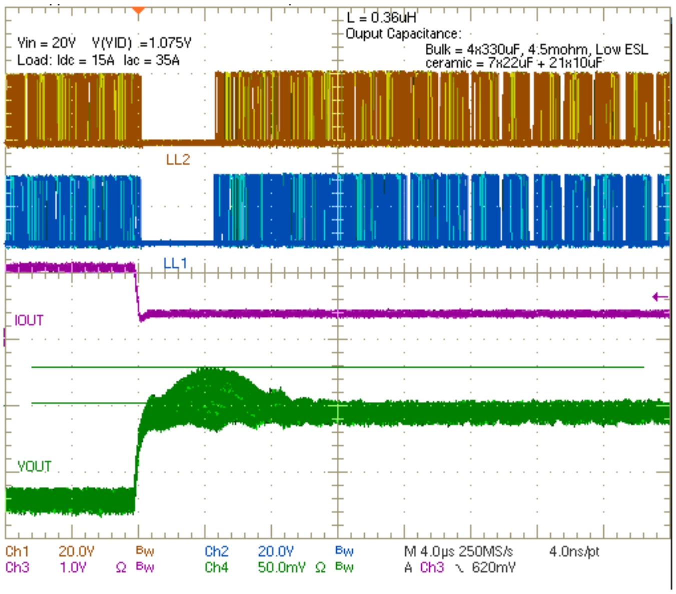


Figure 36. Load Release, V_{IN} = 20 V, I_{DC} = 15 A, I_{AC} = 35 A, Persistence Mode

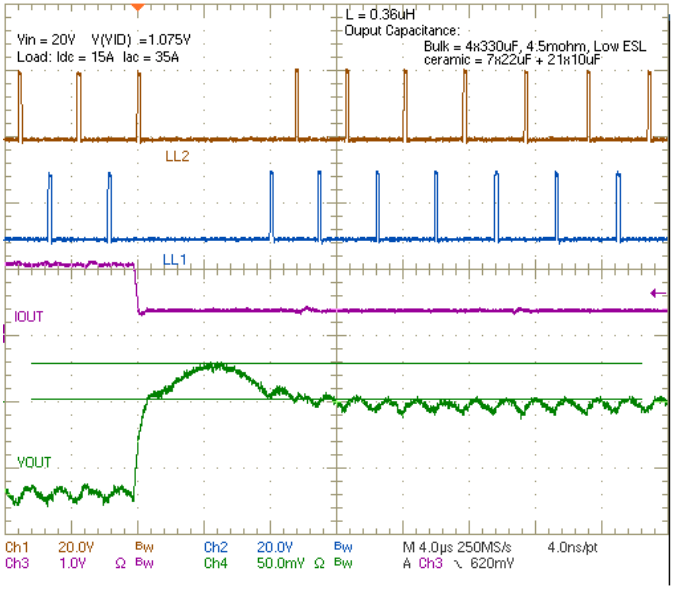


Figure 37. Load Release, V_{IN} = 20 V, I_{DC} = 15 A, I_{AC} = 35 A

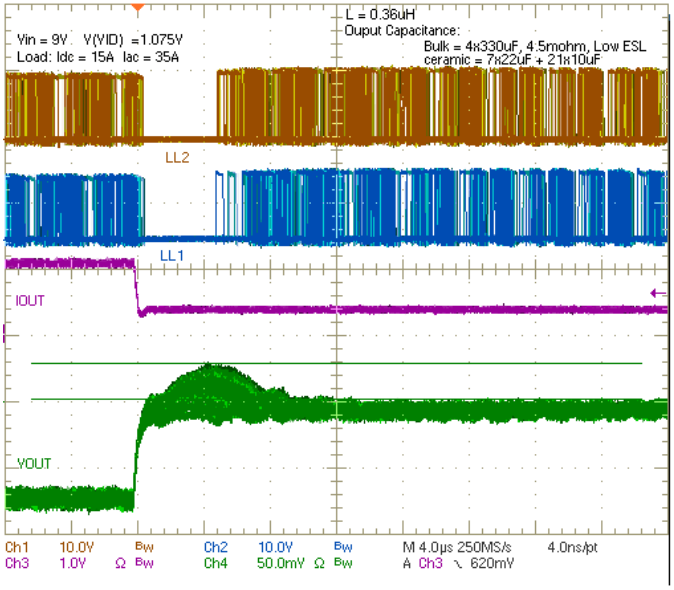


Figure 38. Load Release, V_{IN} = 9 V, I_{DC} = 15 A, I_{AC} = 35 A, Persistence Mode

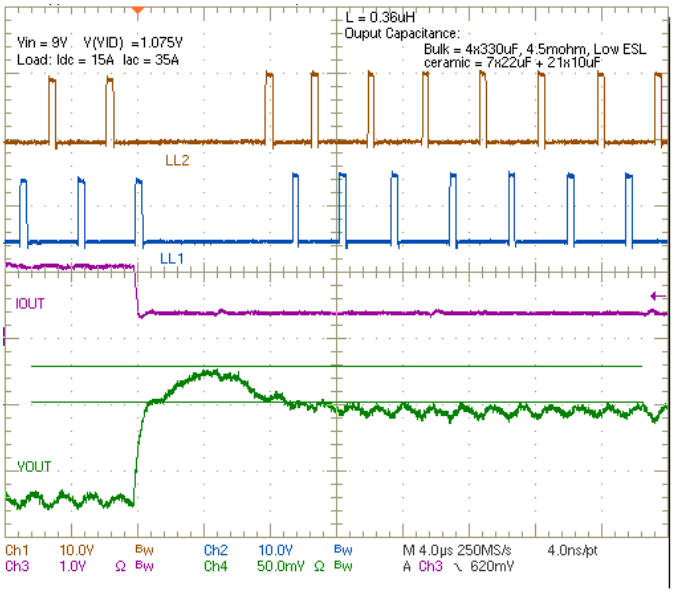


Figure 39. Load Release, V_{IN} = 9 V, I_{DC} = 15 A, I_{AC} = 35 A,

TYPICAL CHARACTERISTICS (continued)

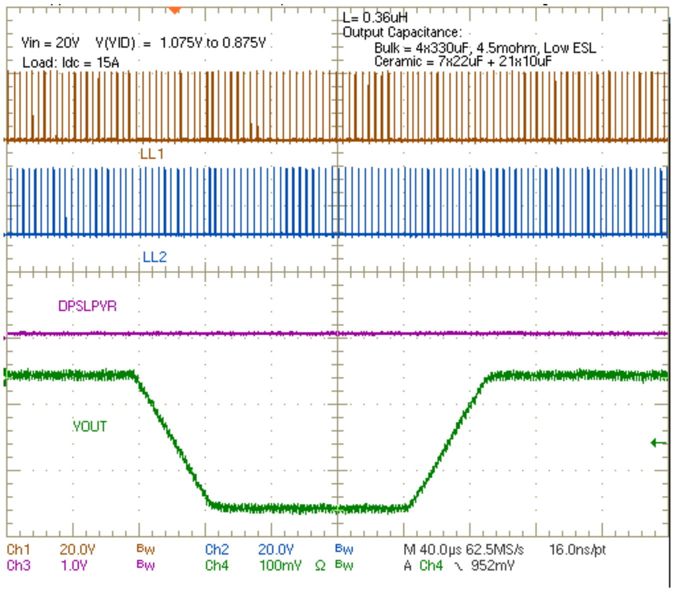


Figure 40. VID Change from 1.075 V to 0.875 V, I_{DC} = 15 A

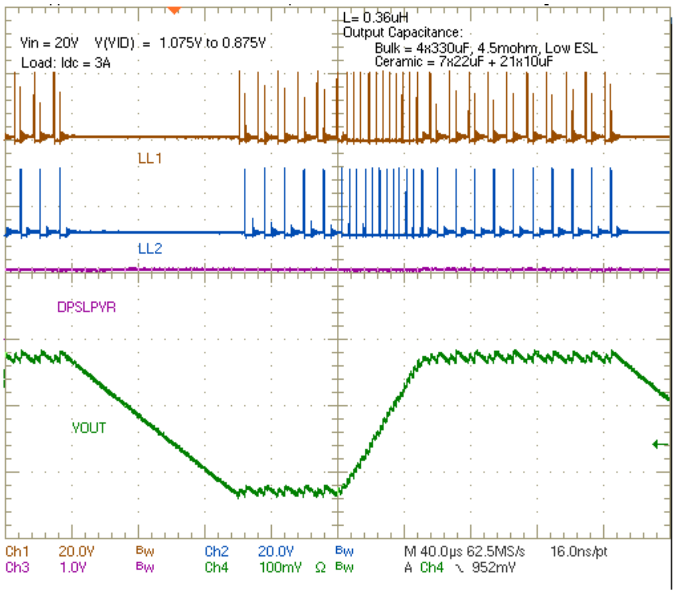


Figure 41. VID Change from 1.075 V to 0.875 V, I_{DC} = 3 A

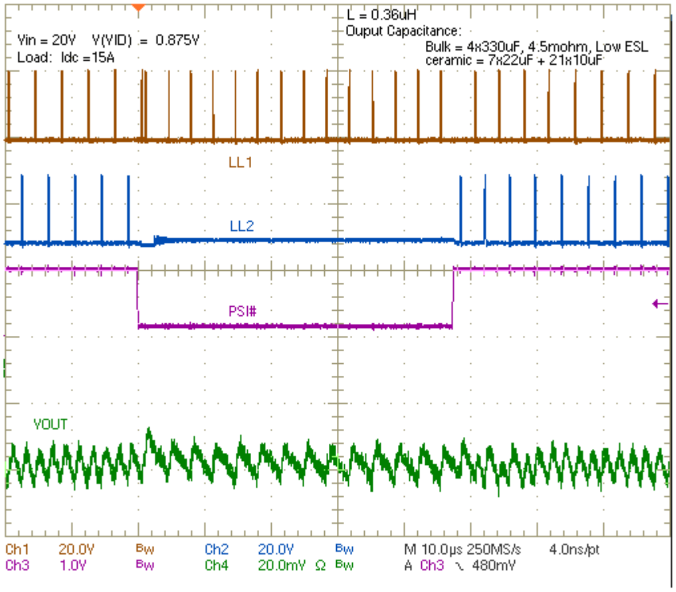


Figure 42. PCNT Toggle: V_{IN} = 20 V

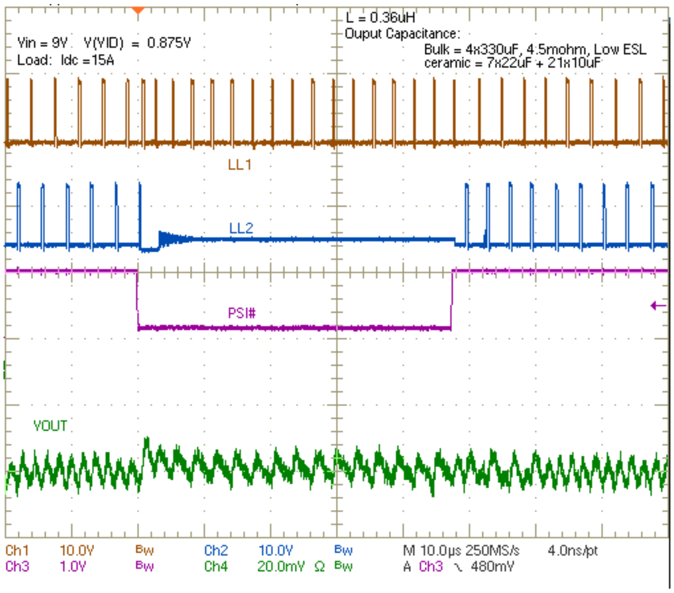


Figure 43. PCNT Toggle: V_{IN} = 9 V

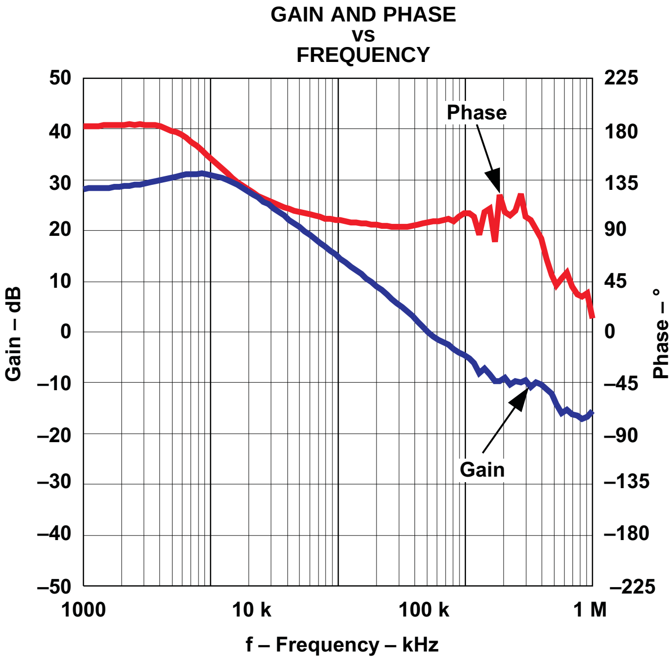


Figure 44.

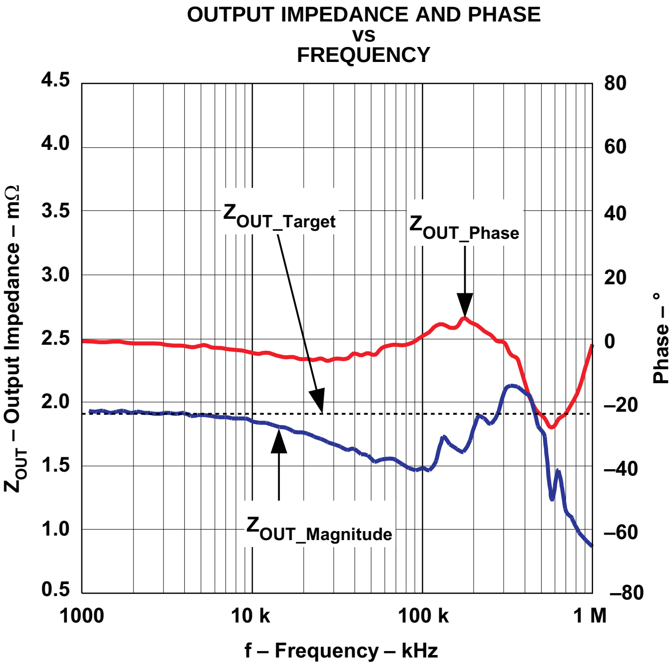


Figure 45.

In Figure 44 and Figure 45

- Output bulk capacitance = 4 × 330 µF, 4.5 mΩ, Low ESL
- Output MLCC capacitance = 7 × 22 µF + 21 × 10 µF
- V_{IN} = 20 V
- V_{VID} = 1.075 V

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53624RHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 53624
TPS53624RHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 53624
TPS53624RHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 53624
TPS53624RHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 53624

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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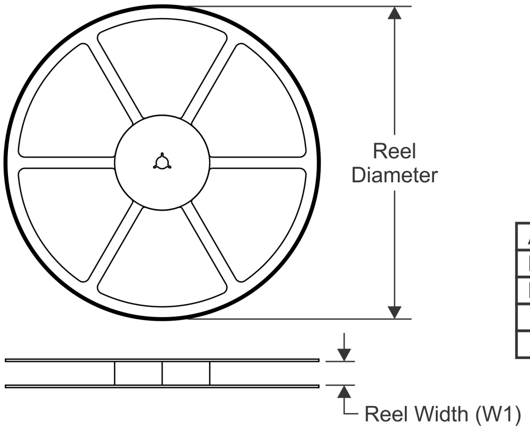
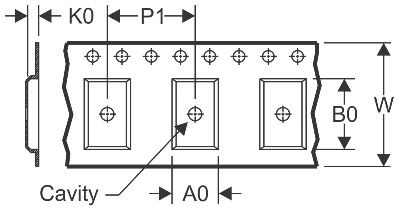
TAPE AND REEL INFORMATION

REEL DIMENSIONS

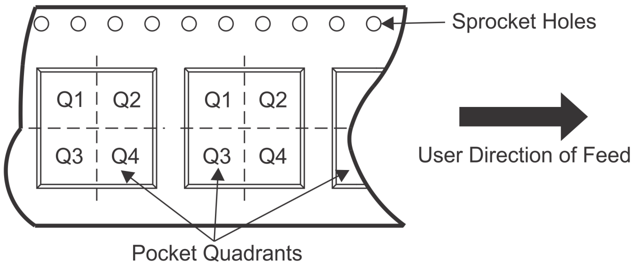


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

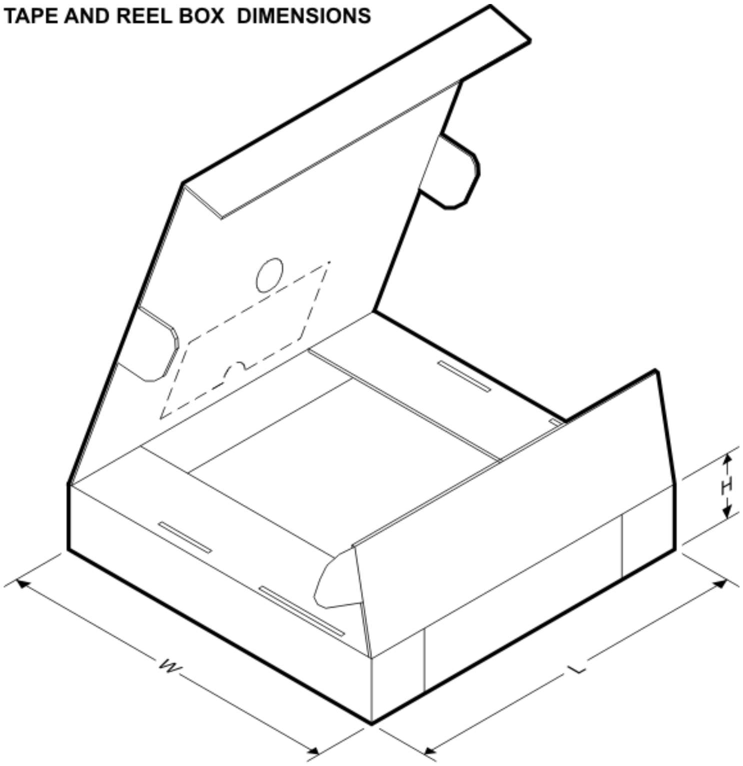
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53624RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS53624RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53624RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS53624RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

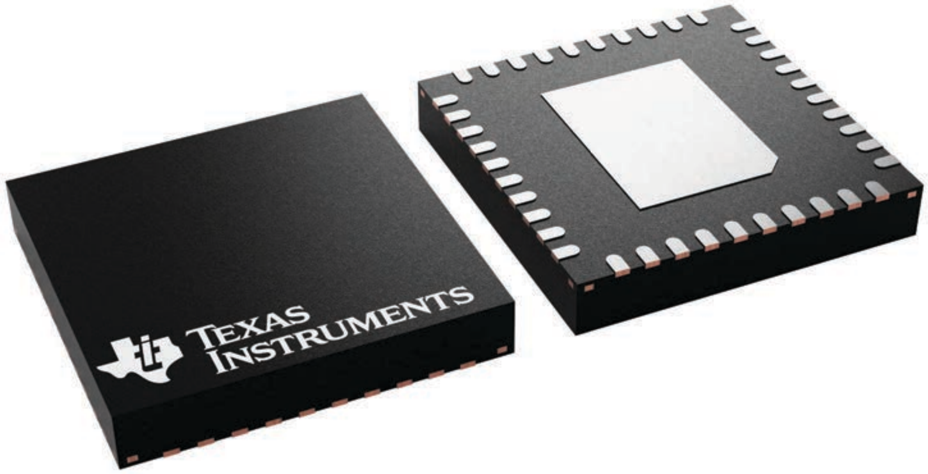
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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