TPS659128 PMU for Processor Power

1 Features

- Four step-down converters:
  - Input voltage (V_{IN}) range from 2.7 V to 5.5 V
  - Power save mode at light load current
  - Output voltage accuracy in PWM mode ±2%
  - Typical 26-µA quiescent current per converter
  - Dynamic voltage scaling
  - 100% duty cycle for lowest dropout
- Ten LDOs:
  - 8 general-purpose LDOs
  - Output voltage range from 0.8 V to 3.3 V
  - Typical 32-µA quiescent current per LDO
  - 2 low-noise RF-LDOs
  - Output voltage range from 1.6 V to 3.3 V
  - Preregulation support by separate power inputs
  - Eco-mode™ control scheme
  - V_{IN} range of LDOs respective to the following voltage ranges:
    - 1.8 V to 3.6 V
    - 3 V to 5.5 V
- Three LED drivers:
  - Internal dimming using I^2C
  - Up to 20 mA per current sink
- Thermal monitoring
  - High temperature warning
  - Thermal shutdown
- Bypass switch
  - Used with DCDC4 in applications powering a Radio Frequency Power Amplifier (RF-PA)
- Interface
  - I^2C interface
  - Power I^2C interface for Dynamic Voltage Scaling (DVS)
  - Serial Peripheral Interface (SPI)
- 32-kHz RC oscillator
- Undervoltage lockout, battery fault comparator, and long button-press detection
- 3.6-mm × 3.6-mm DSBGA package with 0.4-mm pitch

2 Applications

- Smart phones
- Wireless routers and switches
- Tablets
- Industrial applications
- LTE modem
- GPS

3 Description

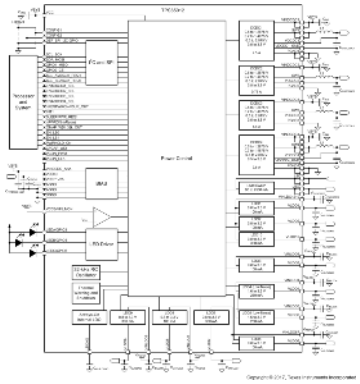
The TPS659128x device provides four configurable step-down converters with up to 2.5-A output current and ten LDO regulators for external use. These LDOs can be supplied from either a battery or a preregulated supply. Each specific part number has a different factory programmed power-up and power-down sequence.

The TPS659128x device integrates a 32-kHz RC oscillator to sequence all resources during power up or power down. All LDOs and DC-DC converters can be controlled by an I^2C or SPI interface or basic enable pins after boot. Additionally, a voltage-scaling interface allows for transitioning the DC-DC converters to a different voltage through I^2C or basic roof-floor control. Three LED drivers with an advanced dimming feature are integrated inside the device. General-purpose input-output (GPIO) functionality is multiplexed with various pins, including LED pins, ENx pins, and SPI pins when not used. Each GPIO can be configured as part of the power-up sequence to control external resources. One SLEEP pin enables switching between the active mode and preprogrammed sleep mode for power optimization. The TPS659128x device comes in a 9-pin × 9-pin DSBGA package (3.6 mm × 3.6 mm) with a 0.4-mm pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TPS6591286 TPS6591287	DSBGA (81)	3.60 mm × 3.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (June 2021)	Page
• Changed TPS6591287 from PREVIEW to ACTIVE	1

5 Pin Configuration and Functions

Figure 5-1 shows the 81-pin YFF Die-Size Ball-Grid Array pin assignments.

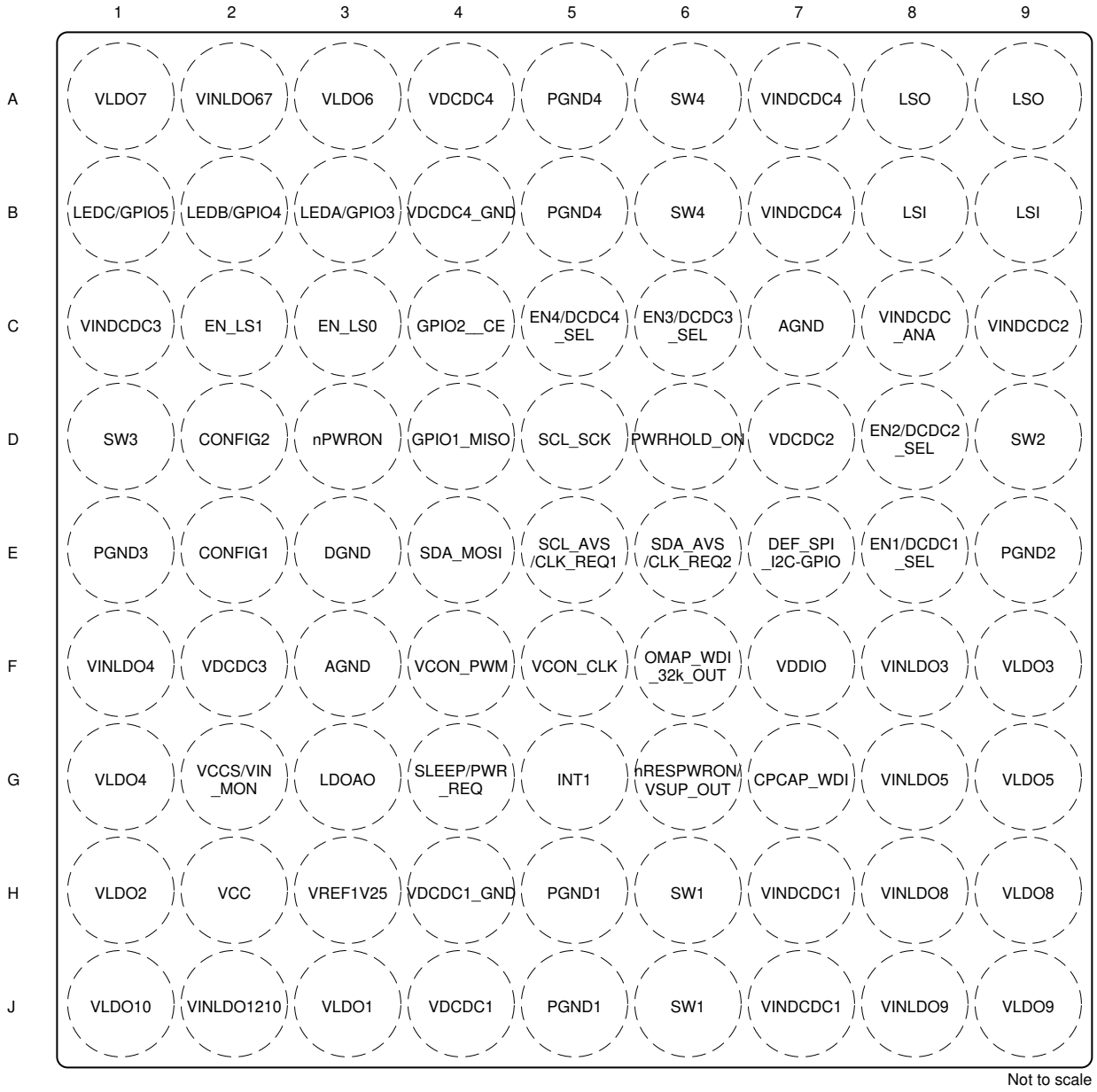


Figure 5-1. 81-Pin YFF DSBGA (Bottom View)

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	ALT NAME	NO.		
REFERENCE				
VREF1V25	—	H3	O	Internal reference voltage. Connect a 100-nF capacitor from this pin to AGND. Do not load this pin externally.
AGND	—	F3, C7	—	Analog-ground (AGND) connection. Connect this pin to the power-ground (PGND) plane on the printed circuit board (PCB).
DRIVERS AND LIGHTING				
LEDA/GPIO3	—	B3	I/O	General-purpose I/O or LED driver output

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ALT NAME	NO.		
LEDB/GPIO4	—	B2	I/O	General-purpose I/O or LED driver output
LEDC/GPIO5	—	B1	I/O	General-purpose I/O or LED driver output
STEP-DOWN CONVERTERS				
VINDCDC_ANA	—	C8	I	Analog supply input for the DC-DC converters. This pin must be connected to the VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC4 pins.
VINDCDC1	—	H7, J7	I	Power input to the DCDC1 converter. Connect this pin to the VINDCDC2, VINDCDC3, VINDCDC4, and VINDCDC_ANA pins.
VDCDC1	—	J4	I	Remote positive voltage sense (feedback) input for the DCDC1 converter
VDCDC1_GND	—	H4	I	Remote negative voltage sense (feedback) input for DCDC1. Tie this pin to the GND plane or to the AGND plane. Alternatively, tie this pin to the GND pad of the output capacitor.
SW1	—	H6, J6	O	Switch node of the DCDC1 converter. Connect this pin to the output inductor.
PGND1	—	H5, J5	—	Power GND connection for the DCDC1 converter
VCON_PWM	—	F4	I	Pulse-width modulation (PWM) period signal for dynamic voltage scaling on the DCDC1 converter if using VCON
VCON_CLK	—	F5	I	Clock signal for dynamic voltage scaling on the DCDC1 converter if using VCON
VINDCDC2	—	C9	I	Power input to the DCDC2 converter. Connect this pin to the VINDCDC1, VINDCDC3, VINDCDC4, and VINDCDC_ANA pins.
VDCDC2	—	D7	I	Remote voltage sense (feedback) input for the DCDC2 converter
SW2	—	D9	O	Switch node of the DCDC2 converter. Connect this pin to the output inductor.
PGND2	—	E9	—	Power GND connection for the DCDC2 converter
VINDCDC3	—	C1	I	Power input to the DCDC3 converter. Connect this pin to the VINDCDC1, VINDCDC2, VINDCDC4, and VINDCDC_ANA pins.
VDCDC3	—	F2	I	Remote voltage sense (feedback) input for the DCDC3 converter
SW3	—	D1	O	Switch node of the DCDC3 converter. Connect this pin to the output inductor.
PGND3	—	E1	—	Power GND connection for the DCDC3 converter
VINDCDC4	—	A7, B7	I	Power input to the DCDC4 converter. Connect this pin to the VINDCDC1, VINDCDC2, VINDCDC3, and VINDCDC_ANA pins.
VDCDC4	—	A4	I	Remote positive voltage sense (feedback) input for the DCDC4 converter
VDCDC4_GND	—	B4	I	Remote negative voltage sense (feedback) input the DCDC4 converter. Tie this pin to the GND plane or to the AGND plane. Alternatively, tie this pin to the GND-pad of the output capacitor.
SW4	—	A6, B6	O	Switch node of the DCDC4 converter. Connect this pin to the output inductor.
PGND4	—	A5, B5	—	Power GND connection for the DCDC4 converter
LOAD SWITCH				
LSI	—	B8, B9	I	Input of the load switch
LSO	—	A8, A9	O	Output of the load switch
EN_LS0	—	C3	I	Load switch enable pin. The status of this pin is copied to the ENABLE0 bit in the LOADSWITCH register in the CONFIG state.
EN_LS1	—	C2	I	Load switch enable pin. The status of this pin is copied to the ENABLE1 bit in the LOADSWITCH register in the CONFIG state.
LOW-DROPOUT REGULATORS				
VINLDO1210	—	J2	I	Power input for the LDO1, LDO2, and LDO10 regulators

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ALT NAME	NO.		
VINLDO3	—	F8	I	Power input for the LDO3 regulator
VINLDO4	—	F1	I	Power input for the LDO4 regulator
VINLDO5	—	G8	I	Power input for the LDO5 regulator
VINLDO67	—	A2	I	Power input for the LDO6 and LDO7 regulators
VINLDO8	—	H8	I	Power input for the LDO8 regulator
VINLDO9	—	J8	I	Power input for the LDO9 regulator
LDOAO	—	G3	O	*LDO always on* internal supply. Connect this pin to the buffer capacitor.
VLDO1	—	J3	O	LDO1 output
VLDO2	—	H1	O	LDO2 output
VLDO3	—	F9	O	LDO3 output
VLDO4	—	G1	O	LDO4 output
VLDO5	—	G9	O	LDO5 output
VLDO6	—	A3	O	LDO6 output
VLDO7	—	A1	O	LDO7 output
VLDO8	—	H9	O	LDO8 output
VLDO9	—	J9	O	LDO9 output
VLDO10	—	J1	O	LDO10 output
STANDARD INTERFACE				
DEF_SPI_I2C-GPIO	—	E7	I	Digital input that defines whether SPI is available or I^2C and GPIOs are available on the C4, D4, E4, D5 pins. Shorting this pin to GND selects SPI. Shorting this pin to LDOAO selects I^2C, and GPIO1 and GPIO2
SCL_SCK	SCK	D5	I	I^2C SCL or SPI SCK based on DEF_SPI_I2C-GPIO
SDA_MOSI	MOSI	E4	I/O	I^2C SDA or SPI master-out slave-in device (MOSI) based on DEF_SPI_I2C-GPIO
GPIO1_MISO	MISO	D4	I/O	GPIO1 or SPI master-out slave-in device (MISO) based on DEF_SPI_I2C-GPIO
GPIO2_ CE	CE	C4	I/O	GPIO2 or SPI chip enable (CE) active high based on DEF_SPI_I2C-GPIO
ENABLE AND VOLTAGE SCALING				
EN1/DCDC1_SEL(1)	DCDC1_SEL	E8	I	Enable pin for EN1_SETx assigned resources or voltage-scaling pin that changes the output of a converter or a group of converters between two predefined values
EN2/DCDC2_SEL(1)	DCDC2_SEL	D8	I	Enable pin for EN2_SETx assigned resources or voltage-scaling pin that changes the output of a converter or a group of converters between two predefined values
EN3/DCDC3_SEL(1)	DCDC3_SEL	C6	I	Enable pin for EN3_SETx assigned resources or voltage-scaling pin that changes the output of a converter or a group of converters between two predefined values
EN4/DCDC4_SEL(1)	DCDC4_SEL	C5	I	Enable pin for EN4_SETx assigned resources or voltage-scaling pin that changes the output of a converter or a group of converters between two predefined values
SCL_AVS/CLK_REQ1(2)	CLK_REQ1	E5	I	Clock pin of power I^2C for dynamic voltage scaling or clock request input signal 1 used to enable and disable power resources using EN2_SETx registers.
SDA_AVS/CLK_REQ2(2)	CLK_REQ2	E6	I/O	Data pin of power I^2C for dynamic voltage scaling or clock request input signal 2 used to enable and disable power resources using EN3_SETx registers.
SLEEP/PWR_REQ(2)	PWR_REQ	G4	I	SLEEP state request input or power request input signal used to enable and disable power resources using EN1_SETx registers.

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	ALT NAME	NO.		
nRESPWRON/VSUP_OUT	VSUP_OUT	G6	O	Active low reset output to disable processor until power-up sequence completes or the output of the input voltage monitor
VCCS/VIN_MON	VIN_MON	G2	I	Voltage sense for input voltage monitoring
PWRHOLD_ON	ON	D6	I	POWERHOLD or ON. This pin is an enable input.
INT1	—	G5	O	Interrupt output
nPWRON	nRESIN (OTP option)	D3	I	Active-low, debounced power-on input or power-request input to start the power-up sequencing. Alternatively, this pin is the active-low reset input to the PMIC that is debounced by 10 ms (OTP option). Tie this pin to the LDOAO pin for a logic high if not used.
OMAP_WDI_32k_OUT	32KCLKOUT	F6	O	Always used as 32KCLKOUT. Leave this pin floating if not using 32KCLKOUT.
CPCAP_WDI	—	G7	—	No connect, leave this pin floating.
CONFIG1	—	E2	I	Selects the predefined startup options and default voltages. Use this pin to choose from two internal OTP settings. Tie this pin to GND or the LDOAO pin.
CONFIG2	—	D2	I	Selects between two device modes. With the CONFIG2 tied to LDOAO, the primary functions of the pins (ENx, SCL_AVS, SDA_AVS, and SLEEP) and SLEEP state is usable. With the CONFIG2 tied to GND, the alternate functions of the pins are used (DCDCx_SEL, CLK_REQx, and PWR_REQ) and SLEEP state is not used.
VCC	—	H2	I	Digital supply input
VDDIO	—	F7	I	Supply voltage input for GPIOs and output stages that sets the high-level voltage (I/O voltage)
DGND	—	E3	–	Digital GND connection. Tie this pin to the AGND and PGNDx on the PCB.

(1) The DCDCx_SEL pin function is selected by pulling the CONFIG2 pin to GND which also selects the CLK_REQx and PWR_REQ pin functions as enable resources.
(2) The CLK_REQ1, CLK_REQ2, and PWR_REQ pin functions are selected by puling the CONFIG2 pin to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	All pins except AGND pins, PGND pins, and pins listed below with respect to AGND	–0.3	6	V
	VLDO1, VLDO2, VLDO3, VLDO4, VLDO5, VLDO6, VLDO7, VLDO8, VLDO9, VLDO10, VINLDO1210, VINLDO3, EN1/DCDC1_SEL, EN2/DCDC2_SEL, EN3/DCDC3_SEL, EN4/DCDC4_SEL, SLEEP/PWR_REQ, CLK_REQ1, CLK_REQ2, VDDIO, CONFIG1, CONFIG2, DEF_SPI_I2C-GPIO, EN_LS0, EN_LS1, OMAP_WDI, CPCAP_WDI, VCON_CLK with respect to AGND	–0.3	3.6	
	VDCDC1, VDCDC2, VDCDC3, VDCDC4 with respect to AGND	–0.3	3.8	
	SDA_SDI, SCL_CLK, GPIO1_MISO, GPIO1_CE, SDA_AVS, SCL_AVS, INT1, 32KCLKOUT, GPIO3 and GPIO4 and GPIO5 if defined as GPIOs with push-pull output (otherwise it is 6-V rated), nRESPWRON if nRESPWRON is push-pull output (otherwise it is 6-V rated) with respect to AGND	–0.3	VDDIO + 0.3	
	V_{CC}	VDDIO	6	
Current	All non-power pins		5	mA
	Power pins (per pin)		2	A
Operating free-air temperature, T_A		–40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* (Section 6.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	1000	V
		Charged device model (CDM), per JESD22-C101(2)	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DC-DC CONVERTERS					
VIN1, VIN2, VIN3, VIN4	Input voltage for step-down converter DCDC1, DCDC2, DCDC3, DCDC4	2.7		5.5	V
	Output voltage for step-down converter DCDC1, DCDC2, DCDC3, DCDC4(1)	0.5		3.8	V
	Inductance at L1, L2, L3, L4	0.5	1	1.3	µH
C_{IN1}, C_{IN4}	Input capacitance at VIN1 and VIN4 (on each pin)	10	22		µF
C_{IN2}, C_{IN3}	Input capacitance at VIN2 and VIN3 (on each pin)	4.7	10		µF
$C_{OUTDCDC1,2,3}$	Output capacitance at DCDC1, DCDC2 and DCDC3	4.7	10	22	µF
$C_{OUTDCDC4}$	Output capacitance at DCDC4	10	22	47	µF
LDOs					
VINLDO1210	Input voltage for LDO1, LDO2 and LDO10	1.7		3.6	V
VINLDO4	Input voltage for LDO4	1.9		5.5	V
VINLDO5	Input voltage for LDO5	1.9		5.5	V
V_{LDO1}, V_{LDO2}, V_{LDO3}, V_{LDO6} , V_{LDO7}, V_{LDO8} , V_{LDO9}, V_{LDO10}	Output voltage for general purpose (GP) LDOs(1)	0.8		3.3	V
V_{LDO4}, V_{LDO5},	Output voltage for RF-LDOs	1.6		3.3	V
$C_{INLDO1210}$, C_{INLDO3}, C_{INLDO4}, C_{INLDO5}, $C_{INLDO67}$, C_{INLDO8}, C_{INLDO8}	Input capacitance on LDO supply pins	0.5			µF
C_{OUTDO4}, $C_{OUTLDO5}$	Output capacitance on LDO4 and LDO5	2.2		10	µF
$C_{OUTLDO1}$, $C_{OUTLDO2}$, $C_{OUTLDO3}$, $C_{OUTLDO6}$, $C_{OUTLDO7}$, $C_{OUTLDO8}$	Output capacitance LDO1, LDO2, LDO3, LDO6, LDO7, LDO8 These LDOs are *capless*, the required capacitance can be placed at the load	0.5		10	µF
$C_{OUTLDO9}$, $C_{OUTLDO10}$	Output capacitance LDO9 and LDO10 These LDOs are *capless*, the required capacitance can be placed at the load	1		10	µF
$C_{OUTLDOAO}$	Output capacitance on LDOAO	0.5		10	µF
$C_{VINDCDC\_ANA}$	Input capacitance on VINDCDC_ANA	100			nF
C_{VCC}	Input capacitance on VCC	100			nF
C_{VDDIO}	Input capacitance on VDDIO	100			nF
C_{VREF}	Output capacitance on VREF1V25	100			nF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) The maximum output voltage of DCDC1 to DCDC4 and LDO1 to LDO4 can be reduced by an OTP setting to adopt the maximum voltage to the requirements (or maximum ratings) of the load powered. This setting helps protect the processor from exceeding the maximum ratings for the core voltage. The value is set in nonvolatile memory (OTP) by TI upon customer request with sufficient business case.

6.4 Thermal Characteristics

THERMAL METRIC(1)		TPS659128 YFF (DSBGA) 81 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – DCDC1, DCDC2, and DCDC3

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.3		5.5	V
V_{DCDC1} V_{DCDC2} V_{DCDC3}	DCDCx output voltage Range	Option1; in 12.5-mV steps; RANGE[1:0] = 00b	0.5		1.2875	V
		Option2; in 12.5-mV steps; RANGE[1:0] = 01b	0.7		1.4875	V
		Option3; in 25-mV steps; RANGE[1:0] = 10b	0.5		2.075	V
		Option4; in 50-mV steps; RANGE[1:0] = 11b	0.5		3.80	V
$I_{OUT(DCDCx)}$	Continuous output current	DCDC1 (VINDCDC1 ≥ 2.8 V)			2500	mA
		DCDC2 (VINDCDC2 ≥ 2.8 V)			750	
		DCDC3 (VINDCDC3 ≥ 2.8 V)			1200	
		DCDC3 for 2.8 V ≤ V_{IN} ≤ 4.5 V; VDCDC3(max) = 1.4875 V			1600	
I_Q	Quiescent current	I_{LOAD} = 0 mA, DCDCx_MODE = 0b, Device not switching, for DCDC1		26	55	µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 1b, Device switching, for DCDC1		8		mA
		I_{LOAD} < 1 mA, Device not switching, ECO = 1b *AND* DCDCx_MODE = 0b, for DCDC1		9		µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 0b, Device not switching, for DCDC2 or DCDC3		26	40	µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 1b, Device switching, for DCDC2 or DCDC3		8		mA
		I_{LOAD} < 1 mA, Device not switching; ECO = 1b *AND* DCDCx_MODE = 0b, for DCDC2 or DCDC3		3		µA

6.5 Electrical Characteristics – DCDC1, DCDC2, and DCDC3 (continued)

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{DCDC1/2/3}$	Accuracy	DCDCx_MODE = 1b, VINDCDCx = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C, ECO = 0	–2%			
		DCDCx_MODE = 1b, VINDCDCx = 3.6 V, I_{LOAD} = 0 mA, –40°C ≤ T_A ≤ 85°C, ECO = 0	–2.5%			
		DCDCx_MODE = 0b, VINDCDCx = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C, ECO = 0	–3%			
	ECO mode accuracy	VINDCDCx = 3.6 V, I_{LOAD} = 0 mA, –40°C ≤ T_A ≤ 85°C; ECO = 1b *AND* DCDCx_MODE = 0b	–5%		5%	
	Load regulation	DCDCx_MODE = 1b, VINDCDCx = 3.6 V, 120 mA ≤ I_{LOAD} ≤ 1080 mA, for DCDC1		0.01		%/A
		DCDCx_MODE = 1b, VINDCDCx = 3.6 V, 120 mA ≤ I_{LOAD} ≤ to 1080 mA, for DCDC3		0.01		
		DCDCx_MODE = 1b, VINDCDCx = 3.6 V, 50 mA ≤ I_{LOAD} ≤ 450 mA, for DCDC2		0.01		
	Line regulation	DCDCx_MODE = 1b, 2.5 V ≤ VINDCDCx ≤ 5.5 V, I_{LOAD} = 0 mA, for DCDC1		0.01		%/V
		DCDCx_MODE = 1b, 2.5 V ≤ VINDCDCx ≤ 5.5 V, I_{LOAD} = 0 mA, for DCDC2 or DCDC3		0.01		
f_{SW}	Switching frequency	DCDCx_MODE = 0b			3500	kHz
		DCDCx_MODE = 1b, VINDCDCx = 3.6 V, VDCDCx = 1.8 V		2800		kHz
$R_{DS(ON)}$	High-side FET on-resistance	for DCDC1 with VINDCDCx = 3.6 V, D = 100%		60	100	mΩ
		for DCDC2 and DCDC3 with VINDCDCx = 3.6 V, D = 100%		120	190	mΩ
$R_{DS(ON)}$	Low-side FET on-resistance	for DCDC1 with VINDCDCx = 3.6 V, D = 100%		60	100	mΩ
		for DCDC2 and DCDC3 with VINDCDCx = 3.6 V, D = 100%		100	160	mΩ
I_{LK_HS}	High-side FET leakage current	T_J = 85°C, DCDC1, VINDCDC1 = 4.2 V			20	µA
		T_J = 85°C, DCDC2 or DCDC3, VINDCDC2 = VINDCDC3 = 4.2 V			3	
I_{LK_LS}	Low-side FET leakage current	T_J = 85°C, DCDC1, VINDCDC1 = 4.2 V			20	µA
		T_J = 85°C, DCDC2 or DCDC3, VINDCDC2 = VINDCDC3 = 4.2 V			1	
I_{HS_LIMF}	High-side forward current limit	VINDCDC1 = 3.6 V, DCDC1	3200	4280	5300	mA
		VINDCDC2 = 3.6 V, DCDC2	1250	1667	2083	
		VINDCDC3 = 3.6 V, DCDC3	2100	2800	3500	
I_{LS_LIMF}	Low-side forward current limit	VINDCDC1 = 3.6 V, DCDC1	3200	4280	5300	mA
		VINDCDC2 = 3.6 V, DCDC2	1200	1600	2000	
		VINDCDC3 = 3.6 V, DCDC3	1875	2500	3125	
$t_{OFF(MIN)}$	Minimum high-side FET off time	VINDCDCx = 3.6 V		30		ns
V_{DCDCPG}	Power-good threshold	VDCDCx falling	86%	90%	94%	
		VDCDCx rising			98%	
t_{DCDCPG}	Power-good threshold deglitch time			1		ms
t_{Start}	Start-up time	Time to start switching, measured from end of I^2C command enabling converter	32	55	100	µs
t_{Ramp}	V_{OUT} ramp up time	Time to ramp from 5% to 95% of VDCDCx	100	160	250	µs
$R_{Discharge}$	Discharge resistor		250	400	500	Ω

6.5 Electrical Characteristics – DCDC1, DCDC2, and DCDC3 (continued)

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T_{pwm}	PWM clock period for VCON_CLK		30		300	ns
T_{su}	VCON setup time	VCON_PWM to rising edge of VCON_CLK			7	ns
T_{hd}	VCON hold time	VCON_PWM from rising edge of VCON_CLK			7	ns

6.6 Electrical Characteristics – DCDC4

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.3		5.5	V
V_{DCDC4}	DCDC4 output voltage range	Option1, in 12.5-mV steps, RANGE[1:0] = 00b	0.5		1.2875	V
		Option2, in 12.5-mV steps, RANGE[1:0] = 01b	0.7		1.4875	
		Option3, in 25-mV steps, RANGE[1:0] = 10b	0.5		2.075	
		Option4, in 50-mV steps, RANGE[1:0] = 11b	0.5		3.80	
$I_{OUT(DCDC4)}$	Continuous output current	DCDC4 (VINDCDC4 ≥ 2.8 V)			2500	mA
I_Q	Quiescent current	I_{LOAD} = 0 mA, DCDC4_MODE = 0b, Device not switching		26	55	µA
		I_{LOAD} = 0 mA, DCDC4_MODE = 1b, Device switching, EN_LS[1:0] = 00 or 01		8		mA
		I_{LOAD} < 1 mA, Device not switching, ECO = 1b *AND* DCDC4_MODE = 0b		9		µA
V_{DCDCx}	Accuracy	DCDC4_MODE = 1b, VINDCDC4 = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C, EN_LS[1:0] = 00b or 01b	–2%		2%	
		DCDC4_MODE = 1b, VINDCDC4 = 3.6 V, I_{LOAD} = 0 mA, –40°C ≤ T_A ≤ 85°C, EN_LS[1:0] = 00b or 01b	–2.5%		2.5%	
		DCDC4_MODE = 0b, VINDCDC4 = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C	–3%		3%	
		DCDC4_MODE = 0b, VINDCDC4 = 3.6 V, I_{LOAD} = 0 mA, –40°C ≤ T_A ≤ 85°C	–3%		3%	
	ECO mode accuracy	ECO = 1b *AND* DCDCx_MODE = 0b, VINDCDC4 = 3.6 V, I_{LOAD} = 0 mA, –40°C ≤ T_A ≤ 85°C	–5%		5%	
	Load regulation	DCDC4_MODE = 1b, VINDCDC4 = 3.6 V, EN_LS[1:0] = 00b or 01b, 250 mA ≤ I_{LOAD} ≤ 2250 mA		0.01		%/A
	Line regulation	DCDC4_MODE = 1b, 2.5 V ≤ VINDCDC4 ≤ 5.5 V, I_{LOAD} = 0 mA, EN_LS[1:0] = 00b or 01b		0.01		%/V
f_{SW}	Switching frequency	DCDC4_MODE = 0b			3500	kHz
		DCDC4_MODE = 1b, VINDCDC4 = 3.6 V, VDCDC4 = 1.8 V, EN_LS[1:0] = 00b or 01b		2800		kHz
$R_{DS(ON)}$	High-side MOSFET on-resistance	VINDCDC4 = 3.6 V, 100% duty cycle		60	100	mΩ
	Low-side MOSFET on-resistance	VINDCDC4 = 3.6 V, 0% duty cycle		60	100	mΩ
I_{LK_HS}	High-side leakage current	T_J = 85°C, VINDCDC4 = 4.2 V			20	µA
I_{LK_LS}	Low-side leakage current	T_J = 85°C, VINDCDC4 = 4.2 V			20	µA
I_{LIM}	High-side current limit	2.9 V ≤ VINDCDC4 ≤ 5.5 V	3000	4400	5000	mA
I_{LIM}	Low-side current limit	2.9 V ≤ VINDCDC4 ≤ 5.5 V	3000	3700	4300	mA
$t_{OFF(MIN)}$	Minimum high-side FET off time	VINDCDC4 = 3.6 V		30		ns
V_{DCDCPG}	Power good threshold	VDCDC4 falling	86%	90%	94%	
		VDCDC4 rising			98%	

6.6 Electrical Characteristics – DCDC4 (continued)

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DCDCPG}	Power good deglitch time			1		ms
t_{Start}	Start-up time	RAMP_TIME = 0b, Time to start switching, measured from end of I^2C command enabling converter	32	55	100	µs
		RAMP_TIME = 1b, Time to start switching, measured from end of I^2C command enabling converter	4	7	14	
t_{Ramp}	V_{OUT} ramp-up time	RAMP_TIME = 0b, Time to ramp from 5% to 95% of VDCDC4, VDCDC4 = 3.4 V	106	160	250	µs
		RAMP_TIME = 1b, Time to ramp from 5% to 95% of VDCDC4, VDCDC4 = 3.4 V	25	40	66	
$R_{Discharge}$	Discharge resistor		250	400	500	Ω
Vbyp-on	Bypass mode turnon duty cycle	For ENABLE[1:0] = 10b, turnon is based on the duty cycle of the PWM signal of DCDC4	90%	97.5%	99.5%	
Vbyp-off	Bypass mode turnoff output voltage threshold	For ENABLE[1:0] = 10b, turnoff is based on output voltage above the nominal value	8%	12%	15%	

6.7 Electrical Characteristics – LDOs

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	LDO1	1.7		3.6	V
		LDO2	1.7		3.6	
		LDO3	1.7		3.6	
		LDO4	1.9		5.5	
		LDO5	1.9		5.5	
		LDO6	1.8		5.5	
		LDO7	1.8		5.5	
		LDO8	1.8		5.5	
		LDO9	1.8		5.5	
		LDO10	1.7		3.6	
V_{LDOx}	LDO output voltage for general-purpose LDOs(1)		0.8		3.3	V
	LDO output voltage for RF_LDOs		1.6		3.3	V
	LDO voltage accuracy	ECO = 0b	–2%		2.5%	
		ECO = 1b	–5%		5%	
$I_{OUT(LDOx)}$	LDO continuous output current	LDO1	100			mA
		LDO2	100			
		LDO3	100			
		LDO4	250			
		LDO5	250			
		LDO6	100			
		LDO7	300			
		LDO8	100			
		LDO9	300			
		LDO10	300			

6.7 Electrical Characteristics – LDOs (continued)

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{SHORT(LDOx)}$	LDO current limit	LDO1, LDO2, LDO3, LDO6, LDO8	100		420	mA
		LDO4, LDO5	250		650	
		LDO7	300		750	
		LDO9, LDO10	300		750	
$V_{DO(LDOx)}$	Dropout voltage(2)	$I_{OUT(LDO1)}$ = 50 mA, VINLDO1 = 1.7 V			500	mV
		$I_{OUT(LDO2)}$ = 100 mA, VINLDO2 = 1.7 V			500	
		$I_{OUT(LDO3)}$ = 80 mA, VINLDO3 = 1.5 V			200	
		$I_{OUT(LDO4)}$ = 200 mA, VINLDO4 = 2.0 V			200	
		$I_{OUT(LDO5)}$ = 200 mA, VINLDO5 = 3.0 V			300	
		$I_{OUT(LDO6)}$ = 100 mA, VINLDO6 = 3.2 V			200	
		$I_{OUT(LDO7)}$ = 200 mA, VINLDO7 = 3.2 V			200	
		$I_{OUT(LDO8)}$ = 100 mA, VINLDO8 = 2.9 V			200	
		$I_{OUT(LDO9)}$ = 300 mA (LDO9), VINLDO9 = 3.1 V			200	
		$I_{OUT(LDO10)}$ = 300 mA (LDO10), VINLDO10 = 2 V			200	
	Line regulation	V_{IN} = V_{LDO} + 0.5 V and I_{LOAD} = 50 mA	–1%		1%	
	Load regulation;	LDO1, LDO2, LDO3, LDO6, LDO8: ECO = 0b, 1 mA ≤ I_{LOAD} ≤ 100 mA	–0.5%		0.5%	
		LDO5, LDO7: ECO = 0b, 1 mA ≤ I_{LOAD} ≤ 200 mA	–1%		1%	
		LDO4, LDO9, LDO10: ECO = 0b, 1 mA ≤ I_{LOAD} ≤ 300 mA	–1.5%		1.5%	
		LDO1 to LDO10: ECO = 1b, 0 mA ≤ I_{LOAD} ≤ 1 mA	–5%		5%	
	Line transient response	dV/dt = ±0.5 V/µs	–50		50	mV
	Load transient response	dI/dt = 100 mA/µs, 10% to 90% load step	–110		110	mV
PSRR	Power supply rejection ratio	LDO1 to LDO3 and LDO6 to LDO10: 10 Hz ≤ f ≤ 1 kHz, VINLDOx – VLDOx ≥ 0.5 V, 10 mA ≤ I_{LOAD} ≤ 0.75 × $I_{LOAD(MAX)}$	47			dB
		LDO4 and LDO5: 10 Hz ≤ f ≤ 1 kHz, VINLDOx – VLDOx ≥ 0.5 V, 10 mA ≤ I_{LOAD} ≤ 0.75 × $I_{LOAD(MAX)}$	63			
	Output voltage noise	LDO1 to LDO3 and LDO6 to LDO10: 10 Hz ≤ f ≤ 100 kHz, VINLDOx – VLDOx ≥ 0.5 V, I_{LOAD} ≥ 10 mA		150		µVrms
		LDO1 to LDO3 and LDO6 to LDO10: 10 Hz ≤ f ≤ 10 kHz, VINLDOx – VLDOx ≥ 0.5 V, I_{LOAD} ≥ 10 mA		50		
		LDO4 and LDO5: 10 Hz ≤ f ≤ 100 kHz, VINLDOx – VLDOx ≥ 0.5 V, I_{LOAD} ≥ 10 mA		30		
		LDO4 and LDO5: 10 Hz ≤ f ≤ 10 kHz, VINLDOx – VLDOx ≥ 0.5 V, I_{LOAD} ≥ 10 mA		15		
I_q	Quiescent current	ECO = 1b, I_{LOAD} ≤ 1 mA for LDO1, LDO2, LDO3, LDO6, LDO7, LDO8, LDO9, LDO10			8	µA
		ECO = 1b, I_{LOAD} ≤ 1 mA for LDO4, LDO5			16	
		ECO = 0b, I_{LOAD} ≤ 1 mA for LDO1, LDO2, LDO3, LDO6, LDO7, LDO8, LDO9, LDO10			32	
		ECO = 0b, I_{LOAD} ≤ 1 mA for LDO4, LDO5			40	
	ECO exit time	Minimum wait time before the full current can be drawn after ECO is set 0b			50	µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of VLDOx , I_{OUT} = 100 mA			170	µs
V_{LDOPG}	PG trigger	VLDOx ≤ V_{TARGET}, VLDOx falling	87%	90.6%	94.5%	
		V_{LDOx} rising			98%	
t_{LDOPG}	Power good deglitch time			1		ms

6.7 Electrical Characteristics – LDOs (continued)

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{Discharge}$	Discharge resistance at LDO output	LDO disabled	200	325	450	Ω

(1) LDO Output voltages are programmed separately
(2) $V_{DO} = V_{IN} – V_{OUT}$, where $V_{OUT} = V_{OUT(NOM)} – 2\%$

6.8 Electrical Characteristics – Digital Inputs, Digital Outputs

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Low-level input voltage		0	0.4	V
V_{IH}	High-level input voltage	All pins except digital interfaces and configuration pins listed below	1.1	V_{CC}	V
		For CONFIG1, CONFIG2, DEF_SPI_I2C-GPIO, EN_LS0, EN_LS1, EN1/DCDC1_SEL, EN2/DCDC2_SEL, EN3/DCDC3_SEL, EN4/DCDC4_SEL, SLEEP/PWR_REQ, CPCAP_WDI, VCON_CLK, CLK_REQ1, CLK_REQ2	1.1	3.3	
		For SDA, SCL, SDA_AVS, SCL_AVS	0.7 × VDDIO	VDDIO	
		For MOSI	1.1	VDDIO	
V_{OL}	Low-level output voltage	I_{OL}= 1 mA, except SDA, SCL, SDA_AVS, SCL_AVS	0	0.2	V
		I_{OL}= 3 mA, for SDA, SCL, SDA_AVS, SCL_AVS, for VDDIO = 1.8 V	0	0.2 × VDDIO	
		I_{OL}= 3 mA, for SDA, SCL, SDA_AVS, SCL_AVS, for 2 V < VDDIO ≤ 3.6 V	0	0.4	
V_{OH}	High-level output voltage	For pins configured as push-pull output to VDDIO, I_{OH} = 1 mA	VDDIO – 0.2	VDDIO	V
		For pins configured as open-drain output		V_{CC}	
I_{OL}	Low-level output current	Except SCL, SDA, AVS_SCL, AVS_SDA		1	mA
		For SCL, SDA, AVS_SCL, AVS_SDA		5	
I_{OH}	High-level output current			1	mA
I_{LKG}	Input-leakage current	Input pins tied to V_{IL} or V_{IH}		0.5	µA

6.9 Electrical Characteristics – VMON Voltage Monitor, VDDIO, Undervoltage Lockout (UVLO), and LDOAO

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMON	Voltage monitor threshold for VMON_SEL[1:0] = 00b, rising voltage	–2%	3.1	2%	V
	Voltage monitor threshold for VMON_SEL[1:0] = 01b, rising voltage	–2%	2.9	2%	V
	Voltage monitor threshold for VMON_SEL[1:0] = 10b, rising voltage	–2%	2.8	2%	V
	Voltage monitor threshold for VMON_SEL[1:0] = 11b, rising voltage	–2%	2.7	2%	V
VMON hysteresis	For falling voltage		250		mV
VDDIO voltage range	Voltage applied to VDDIO pin to set the high level voltage of push-pull output stages	1.63		3.6	V
VDDIO undervoltage lockout (UVLO) threshold		1.4		1.625	V
UVLO	Internal undervoltage lockout threshold (supply voltage rising)		2.5		V
	Internal UVLO threshold hysteresis		200		mV
VLDOAO	Output voltage for LDOAO (LDO always on)		2.5		V

6.10 Electrical Characteristics – Load Switch

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage between LSI and LSO				5.5	V
LSI input current limit	ILIM[1:0] = 00b, 2.7 V ≤ $V_{(LSI)}$ ≤ 5.5 V	75	90	115	mA
	ILIM[1:0] = 00b, 4.5 V ≤ $V_{(LSI)}$ ≤ 5.5 V, –10°C ≤ T_A ≤ 85°C	85	90	100	mA
	ILIM[1:0] = 01b, 2.7 V ≤ $V_{(LSI)}$ ≤ 5.5 V	450	485	520	mA
	ILIM[1:0] = 01b, V(LSI) = 4.5 V ≤ $V_{(LSI)}$ ≤ 5.5 V, –10°C ≤ T_A ≤ 85°C	460	485	500	mA
	ILIM[1:0] = 10b, 2.7 V ≤ $V_{(LSI)}$ ≤ 5.5 V	720	820	920	mA
	ILIM[1:0] = 10b, 2.7 V ≤ $V_{(LSI)}$ ≤ 5.5 V, –10°C ≤ T_A ≤ 85°C	750	820	900	mA
	ILIM[1:0] = 11b, 2.7 V ≤ $V_{(LSI)}$ ≤ 5.5 V, not tested in production	2000	2500	3000	mA
Current-limit response time			10		µs
Resistance from LSI to LSO	When switch closed and operated as load switch with ILIM[1:0] = 11b		20	40	mΩ
Resistance from LSI to LSO	When switch closed and operated as load switch with ILIM[1:0] = 00b or 01b or 10b			200	mΩ
Leakage current from LSI to LSO	When load switch is open			20	µA
Load switch over-voltage protection on the output (sensed at VDCDC4)	For EN_LS[1:0] = 10b or 11b, when load switch is used as BYPASS switch		4.18		V

6.11 Electrical Characteristics – LED Drivers

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SINK(LEDx)}$	LEDx output sink current	$V_{(LEDA)}$ = $V_{(LEDB)}$ = $V_{(LEDC)}$ = 0.25 V	2		20	mA
	Accuracy	Absolute accuracy	–8%		9.5%	
$V_{LO(LEDx)}$	Low-level output voltage	Output low voltage at LEDx pins, 20 mA			0.25	V
$I_{LKG(LEDx)}$	Output off leakage current	Output voltage = 5 V, driver set to OFF			1	µA

6.12 Electrical Characteristics – Thermal Monitoring and Shutdown

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hot-die temperature rising threshold	THERM_HDSEL[1:0] = 00b	113	117	136	°C
	THERM_HDSEL[1:0] = 01b	113	121		
	THERM_HDSEL[1:0] = 10b	113	125		
	THERM_HDSEL[1:0] = 11b	113	130	136	
Hot-die temperature hysteresis			10		°C
Thermal shutdown temperature rising threshold		136	148	160	°C
Thermal shutdown temperature hysteresis			10		°C
Ground current	Device in ACTIVE state, T_A = 27°C, V_{CCS} = 3.8 V		6		µA

6.13 Electrical Characteristics – 32-kHz RC Clock

–40°C ≤ T_A ≤ 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
32KCLKOUT rise and fall time	C_L = 35 pF			10	ns
Output-frequency low-level output voltage	32KCLKOUT output		32		kHz
Output-frequency accuracy	T_A = 25°C	–20%	0%	15%	
Output duty cycle		40%	50%	60%	
Settling time				150	µs

6.14 SPI Timing Requirements

For the SPI timing diagram, see Figure 7-3.

		MIN	MAX	UNIT
t_{cesu}	Chip select setup time	30		ns
t_{cehld}	Chip select hold time	30		ns
t_{ckper}	Clock cycle time	65		ns
t_{ckhigh}	Clock high typical pulse duration	20		ns
t_{cklow}	Clock low typical pulse duration	20		ns
t_{sisu}	Input data setup time, before clock active edge	5		ns
t_{sihld}	Input data hold time, after clock active edge	5		ns
t_{dr}	Data retention time		15	ns
t_{CE}	Time from CE going low to CE going high	65		ns
	Capacitive load on pin GPIO1_MISO		30	pF

6.15 I²C Interface Timing Requirements

Specified by design. Not tested in production. For the high-speed mode timing diagram, see Figure 7-2.

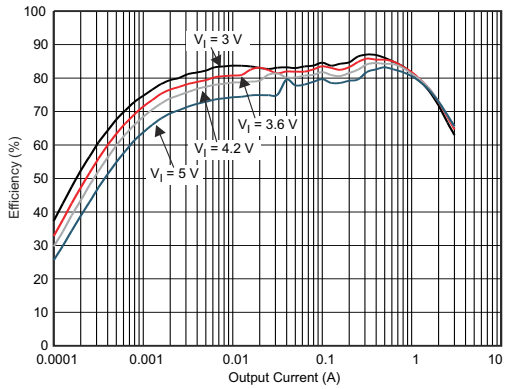
			MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B – 100 pF maximum		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF maximum		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF maximum		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF maximum		1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
t_{HD}, t_{STA}	Hold time (repeated) START condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B – 100 pF maximum	160		ns
		High-speed mode, C_B – 400 pF maximum	320		ns

6.15 I²C Interface Timing Requirements (continued)

Specified by design. Not tested in production. For the high-speed mode timing diagram, see Figure 7-2.

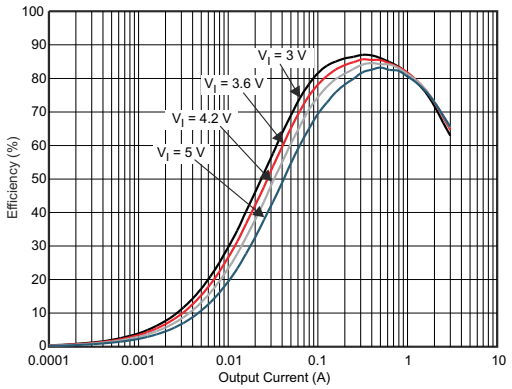
			MIN	MAX	UNIT
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF maximum	60		ns
		High-speed mode, C_B – 400 pF maximum	120		ns
t_{SU}, t_{STA}	Setup time for a repeated START condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data setup time	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data hold time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B – 100 pF maximum	0	70	ns
		High-speed mode, C_B – 400 pF maximum	0	150	ns
t_{RCL}	Rise time of SCL signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	40	ns
		High-speed mode, C_B – 400 pF maximum	20	80	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns
t_{FCL}	Fall time of SCL signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	40	ns
		High-speed mode, C_B – 400 pF maximum	20	80	ns
t_{RDA}	Rise time of SDA signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns
t_{FDA}	Fall time of SDA signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF maximum	10	80	ns
		High-speed mode, C_B – 400 pF maximum	20	160	ns
t_{SU}, t_{STO}	Setup time for STOP condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
C_B	Capacitive load for SDA and SCL			400	pF

6.16 Typical Characteristics



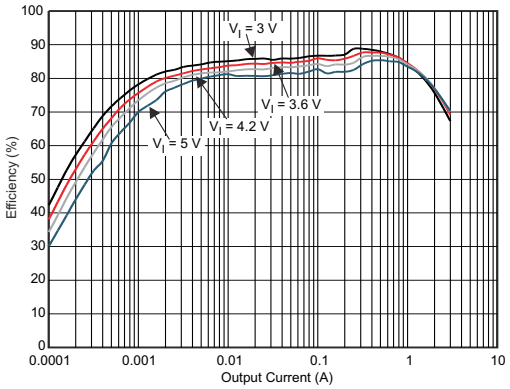
V_{OUT} = 0.9 V PFM Mode
DFE252012P-1R0 T_A = 25°C

Figure 6-1. DCDC1 Efficiency vs Output Current



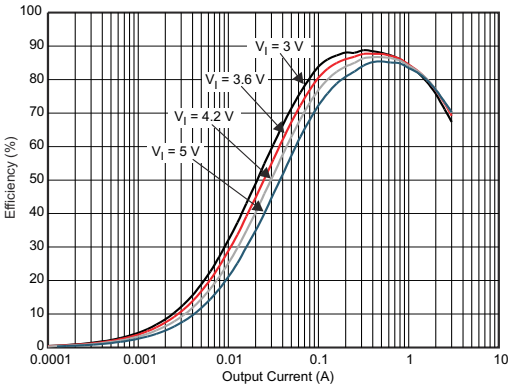
V_{OUT} = 0.9 V PWM Mode
DFE252012P-1R0 T_A = 25°C

Figure 6-2. DCDC1 Efficiency vs Output Current



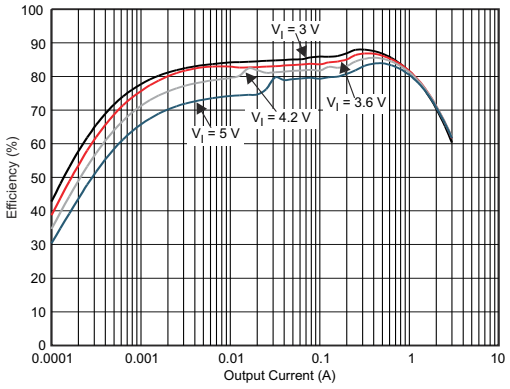
V_{OUT} = 1.1375 V PFM Mode
DFE252012P-1R0 T_A = 25°C

Figure 6-3. DCDC1 Efficiency vs Output Current



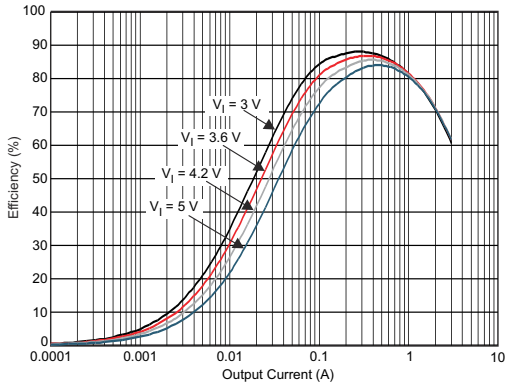
V_{OUT} = 1.1375 V PWM Mode
DFE252012P-1R0 T_A = 25°C

Figure 6-4. DCDC1 Efficiency vs Output Current



V_{OUT} = 1.2 V PFM Mode
LQM2MPN-1R0 T_A = 25°C

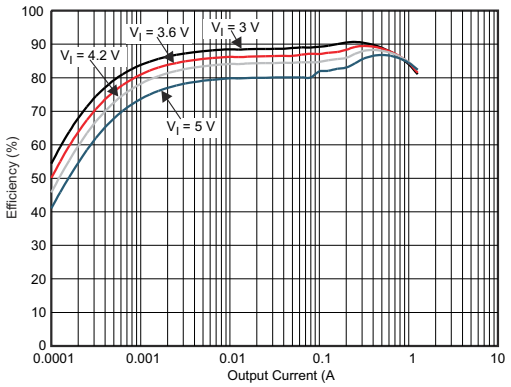
Figure 6-5. DCDC1 Efficiency vs Output Current



V_{OUT} = 1.2 V PWM Mode
LQM2MPN-1R0 T_A = 25°C

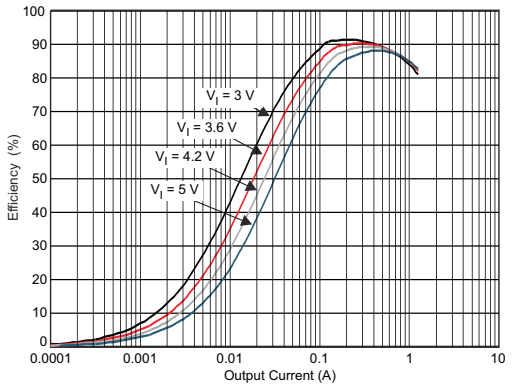
Figure 6-6. DCDC1 Efficiency vs Output Current

6.16 Typical Characteristics (continued)



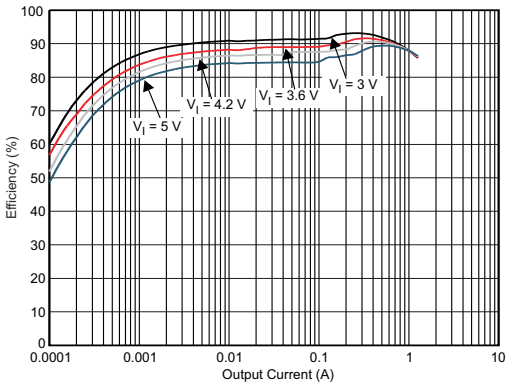
V_{OUT} = 1.8 V PFM Mode
LQM2MPN-1R0 T_A = 25°C

Figure 6-7. DCDC2 Efficiency vs Output Current



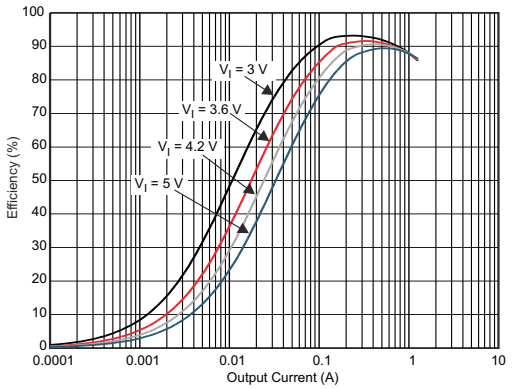
V_{OUT} = 1.8 V PWM Mode
LQM2MPN-1R0 T_A = 25°C

Figure 6-8. DCDC2 Efficiency vs Output Current



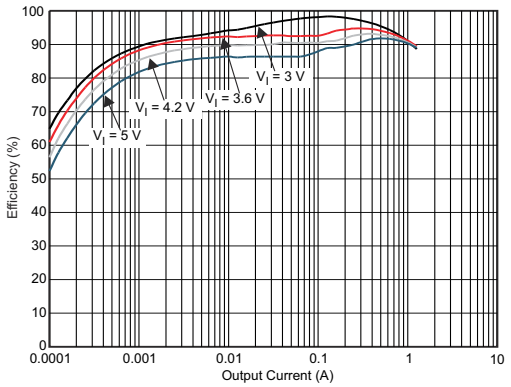
V_{OUT} = 2.25 V PFM Mode
VLS201612-1R0 T_A = 25°C

Figure 6-9. DCDC2 Efficiency vs Output Current



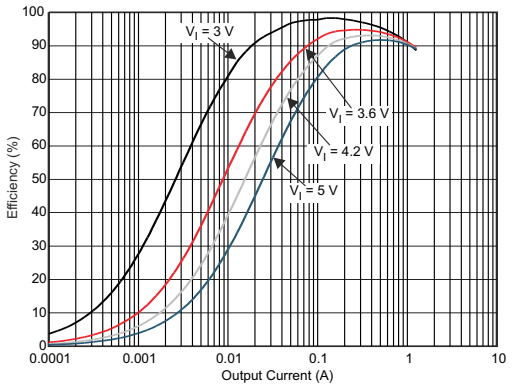
V_{OUT} = 2.25 V PWM Mode
VLS201612-1R0 T_A = 25°C

Figure 6-10. DCDC2 Efficiency vs Output Current



V_{OUT} = 2.95 V PFM Mode
VLS201612-1R0 T_A = 25°C

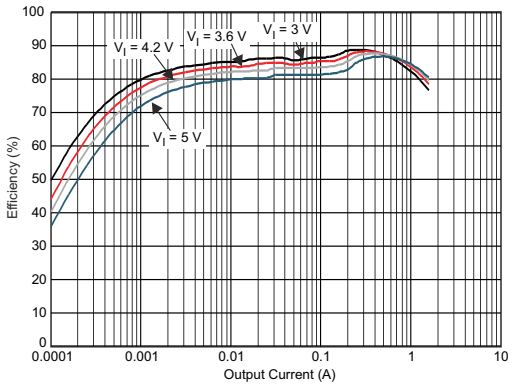
Figure 6-11. DCDC2 Efficiency vs Output Current



V_{OUT} = 2.95 V PWM Mode
VLS201612-1R0 T_A = 25°C

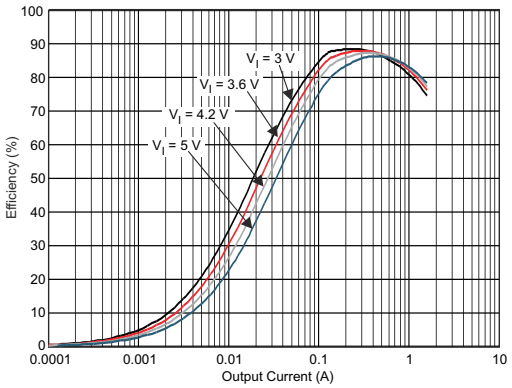
Figure 6-12. DCDC2 Efficiency vs Output Current

6.16 Typical Characteristics (continued)



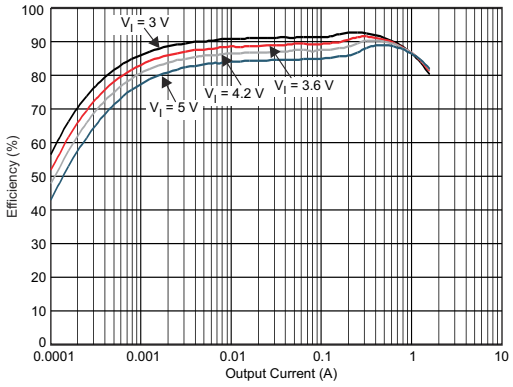
V_{OUT} = 1.1375 V PFM Mode
DFE252012-1R0 T_A = 25°C

Figure 6-13. DCDC3 Efficiency vs Output Current



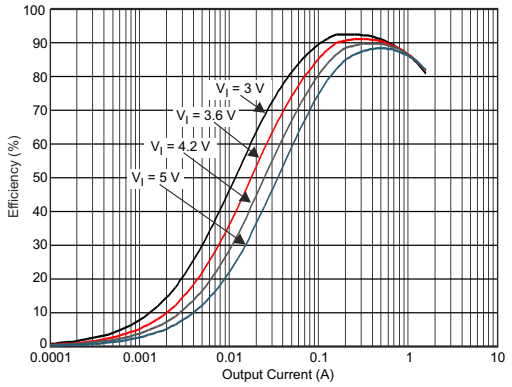
V_{OUT} = 1.1375 V PWM Mode
DFE252012-1R0 T_A = 25°C

Figure 6-14. DCDC3 Efficiency vs Output Current



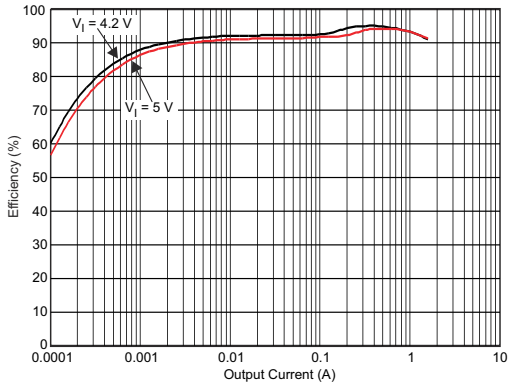
V_{OUT} = 2.1 V PFM Mode
LQM2MPN-1R0 T_A = 25°C

Figure 6-15. DCDC3 Efficiency vs Output Current



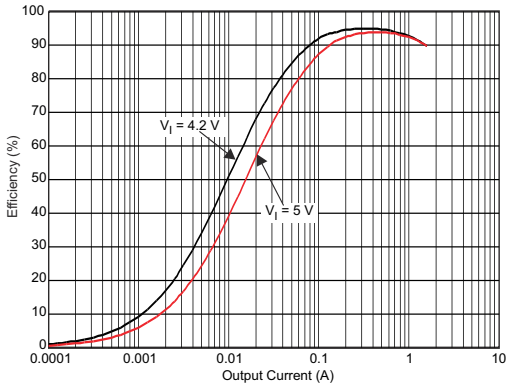
V_{OUT} = 2.1 V PWM Mode
LQM2MPN-1R0 T_A = 25°C

Figure 6-16. DCDC3 Efficiency vs Output Current



V_{OUT} = 3.2 V PFM Mode
DFE25012-1R0 T_A = 25°C

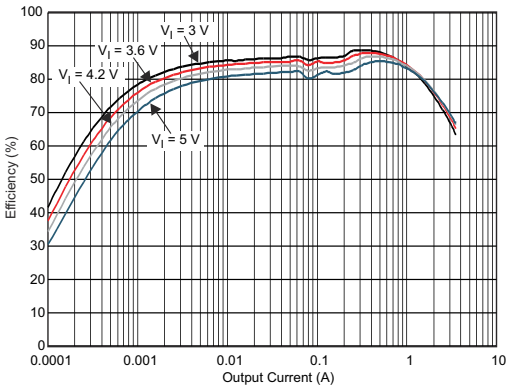
Figure 6-17. DCDC3 Efficiency vs Output Current



V_{OUT} = 3.2 V PWM Mode
DEF25012-1R0 T_A = 25°C

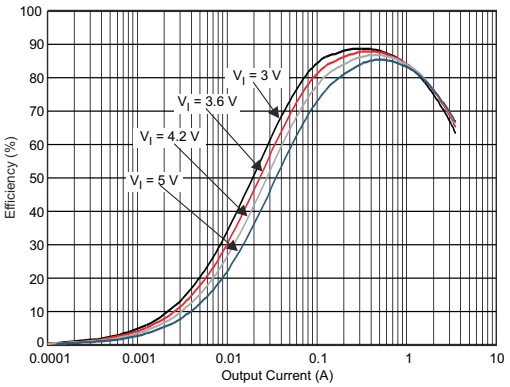
Figure 6-18. DCDC3 Efficiency vs Output Current

6.16 Typical Characteristics (continued)



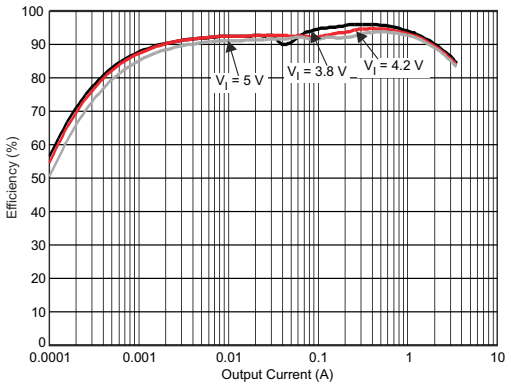
V_{OUT} = 1.1375 V PFM Mode
DEF25012-1R0 T_A = 25°C

Figure 6-19. DCDC4 Efficiency vs Output Current



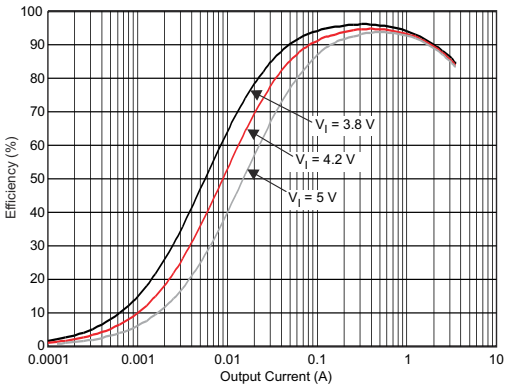
V_{OUT} = 1.1375 V PWM Mode
DEF322512-1R0 T_A = 25°C

Figure 6-20. DCDC4 Efficiency vs Output Current



V_{OUT} = 3.3 V PFM Mode
DEF322512-1R0 T_A = 25°C

Figure 6-21. DCDC4 Efficiency vs Output Current



V_{OUT} = 3.3 V PWM Mode
DEF322512-1R0 T_A = 25°C

Figure 6-22. DCDC4 Efficiency vs Output Current

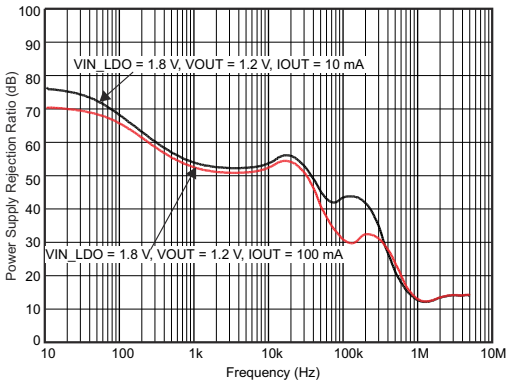
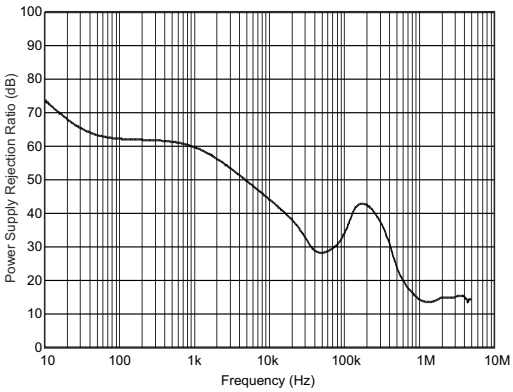


Figure 6-23. LDO1, LDO2, LDO3 PSRR vs Frequency



V_{IN} = 3.2 V V_{OUT} = 2.7 V
I_{OUT} = 225 mA

Figure 6-24. LDO4 and LDO5 PSRR vs Frequency

6.16 Typical Characteristics (continued)

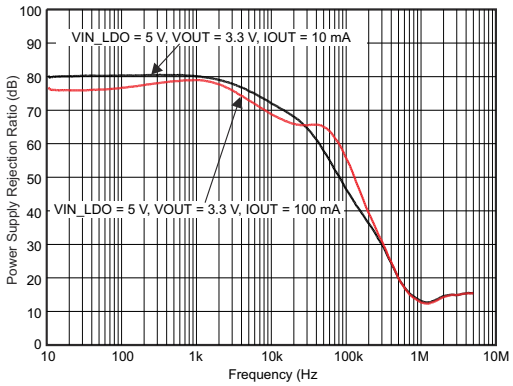


Figure 6-25. LDO4 PSRR vs Frequency

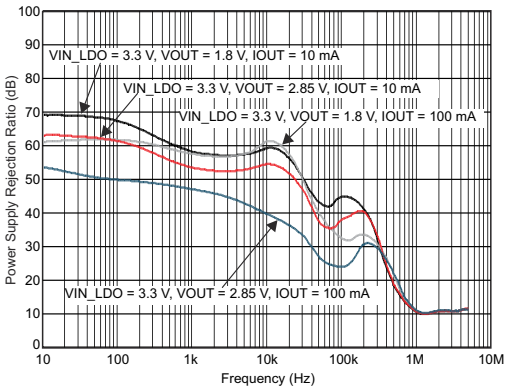


Figure 6-26. LDO6 and LDO8 PSRR vs Frequency

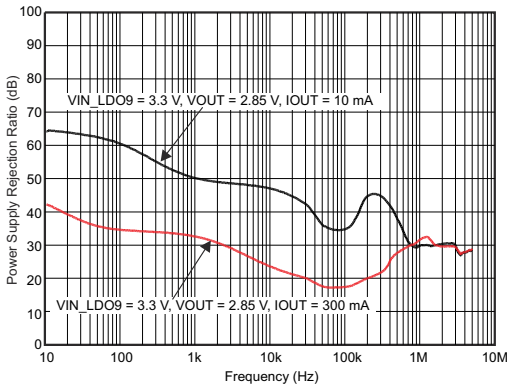


Figure 6-27. LDO9 PSRR vs Frequency

7 Parameter Measurement Information

7.1 I²C Timing Diagrams

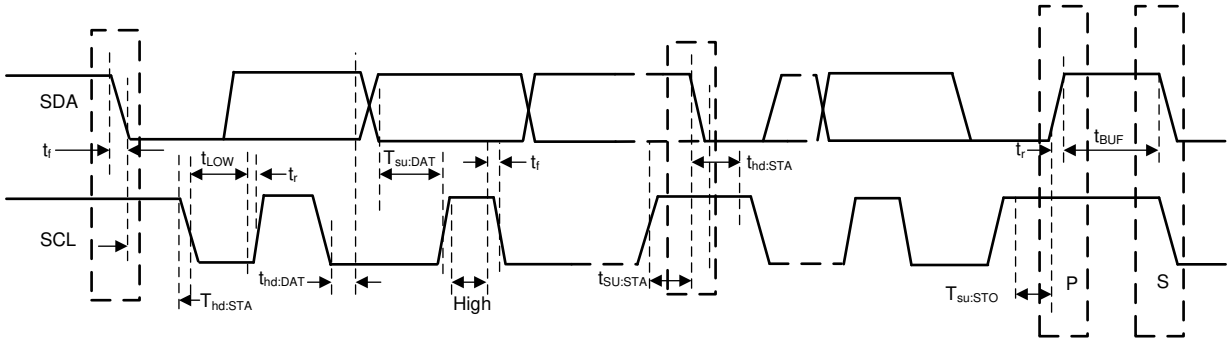
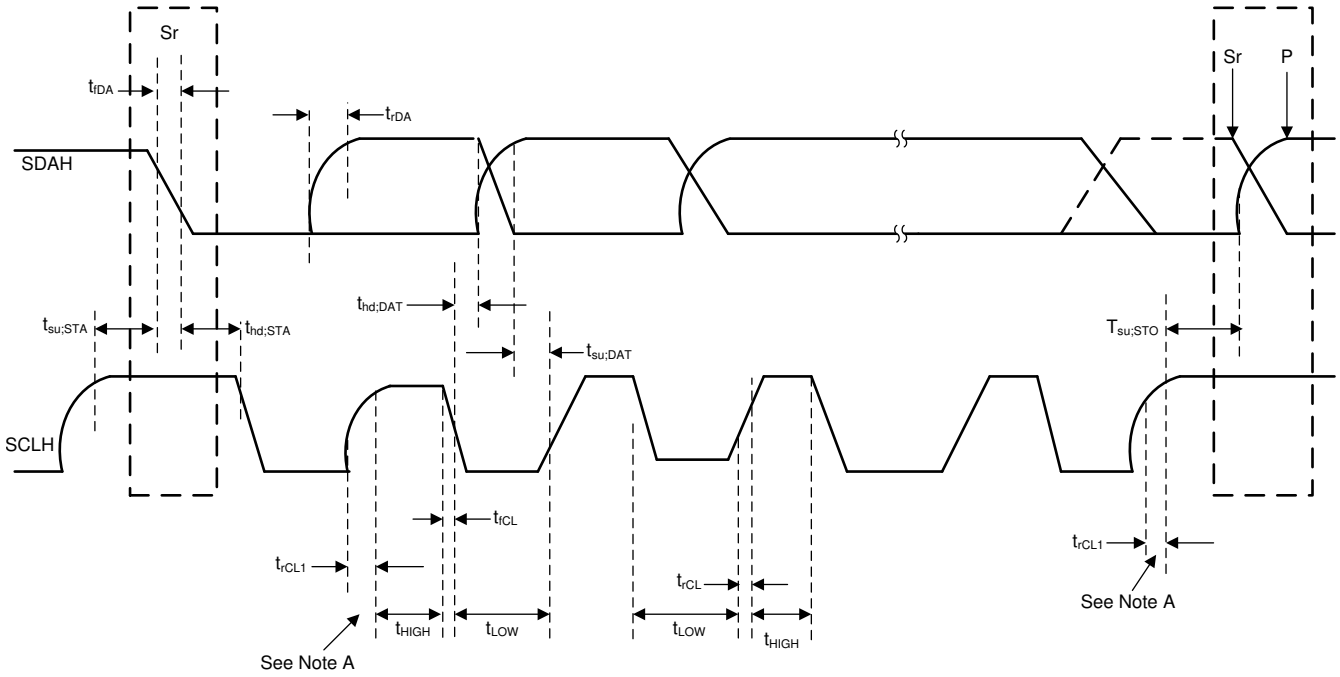


Figure 7-1. Serial Interface Timing Diagram for FS-Mode



A. First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 7-2. Serial Interface Timing Diagram for HS-Mode

7.2 SPI Timing Diagram

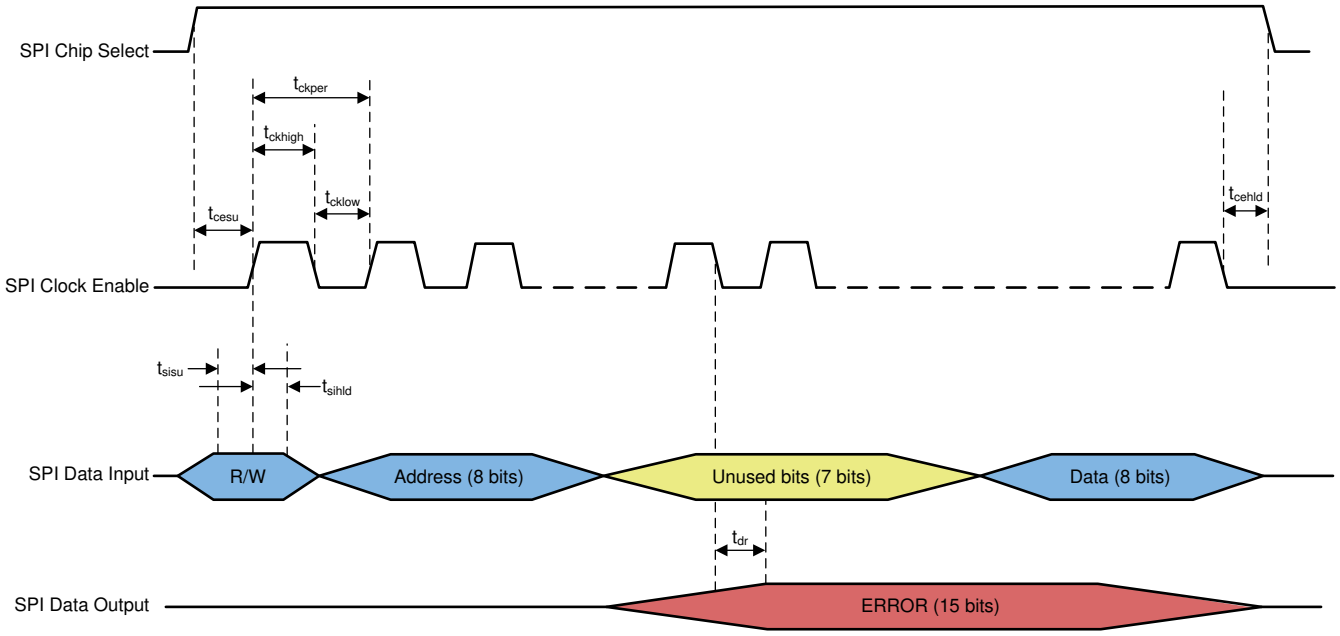


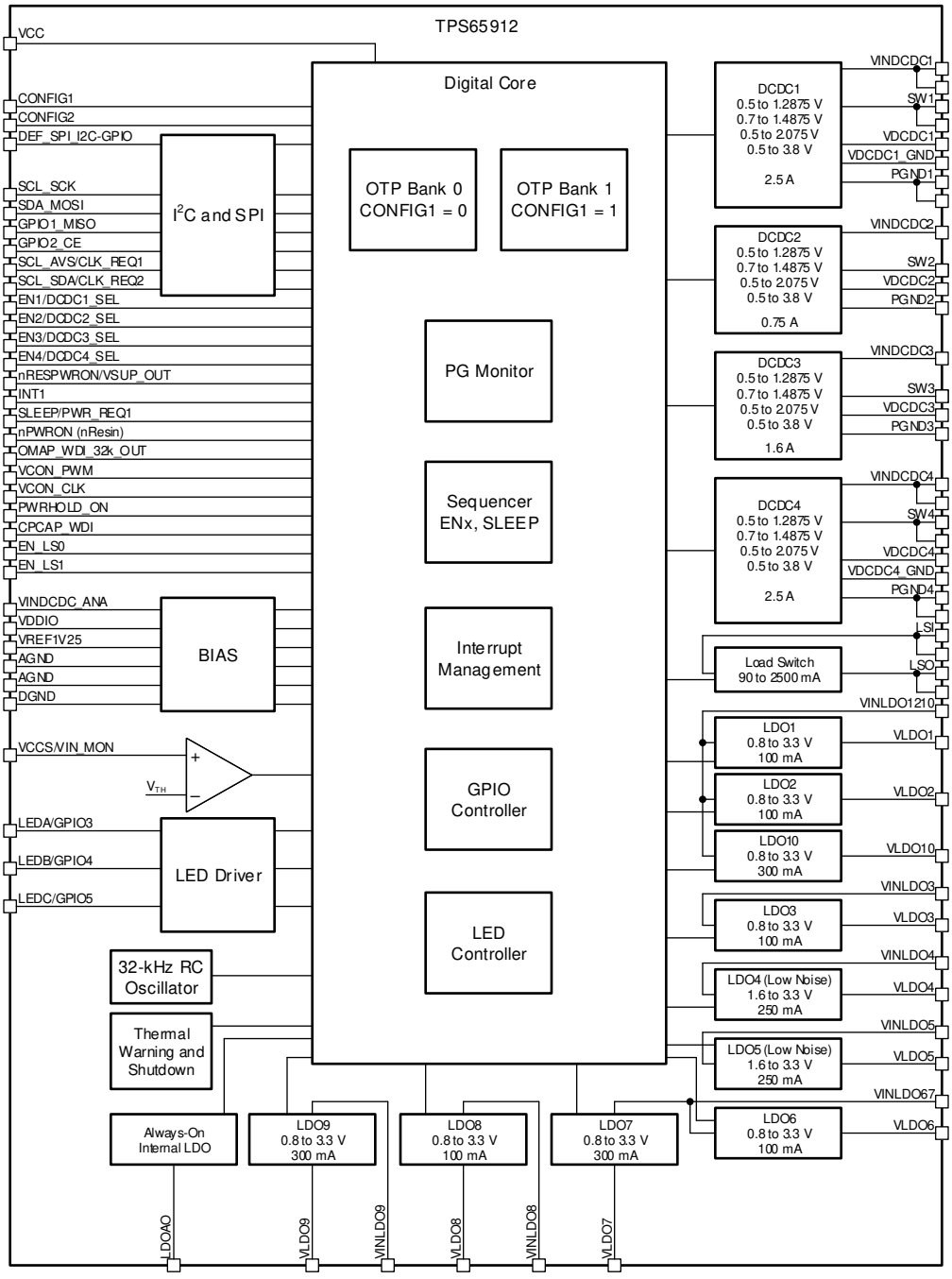
Figure 7-3. SPI Timing

8 Detailed Description

8.1 Overview

The TPS659128x device is an integrated power-management integrated circuit (PMIC), available in an 81-pin, 0.4-mm pitch, 3.6-mm × 3.6-mm DSBGA package. The device is designed for applications including data cards, smart phones, wireless routers and switchers, LTE modems, industrial applications, GPS, and tablets. The device provides four, configurable step-down converter rails with a power save mode for light loads. The TPS659128x device also provides ten external LDO rails. Eight are general purpose LDOs and two are low-noise RF-LDOs. The device also comes with two I^2C interface channels or one SPI channel, five GPIOs, a 32-kHz RC oscillator, and a programmable power sequencer and control for supporting different processors and applications. The four, step-down converter rails are consisting of four, high-frequency switch-mode converters with integrated FETs. The rails are capable of synchronizing to an external clock input and supports a switching frequency from 2.8 MHz to 3.5 MHz. The DCDC4 rail also includes a bypass switch that can be used to turn on and turn off high current loads. In addition, the DCDC rails support dynamic voltage scaling with a dedicated I^2C interface. The eight general LDOs support an output from 0.8 V to 3.3 V. The two low-noise LDOs support an output from 1.6 V to 3.3 V. All LDOs and step-down converters can be controlled by the SPI or I^2C interface. The power-up and power-down controller is configurable and programmable through one-time programmable (OTP) memory. The TPS659128x device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. Configurable GPIOs with a multiplexed feature are available on the TPS659128x device. The GPIOs can be configured and used as enable signals for external resources, which can be included in the power-up and power-down sequence. Lastly, the device includes a long button-press detection that allows startup of the device with the hold of a button.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Linear Regulators

The power-management core has 10 low-dropout (LDO) regulators with various output voltage and current capabilities. Each LDO output voltage can be set independently through the communication bus (see Table 8-85). The transition occurs immediately if the LDO regulator is enabled.

8.3.1.1 Low Quiescent Current Mode (Eco-mode™)

Each LDO regulator is equipped with a low quiescent-current mode that can be enabled or disabled separately. When the ECO bit is set to 1b, the LDOx Eco-mode control scheme is enabled if the proper conditions are met.

8.3.1.2 Output Discharge

Each LDO regulator is equipped with an output discharge bit located in the DISCHARGEx registers. When the LDOx_DISCHARGE bit is set to 1b, the output of the LDO is discharged to ground with the equivalent of a 300-Ω resistor. If the LDO regulator is enabled, the discharge bit is ignored.

8.3.1.3 Thermal Shutdown

Global thermal-shutdown protection is available for all step-down converters and LDO regulators. The thermal sensor generates an early warning depending on the setting of the THRM_REG register. This can generate an interrupt on the INT pin if the HOTDIE interrupt is not masked in the INT_MSK register. If the temperature rises above the thermal shutdown threshold, the device is powered down to the OFF state.

8.3.1.4 LDO Enable

The LDO enable and disable is part of the flexible power-up and power-down state machine. Each LDO regulator can be factory programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. More details on the startup sequencing is available in Section 8.4.3. The EN1, EN2, EN3, EN4, CLK_REQ1, CLK_REQ2, and PWR_REQ (SLEEP) pins can be mapped to any resource (LDO, DC-DC converter, 32-kHz clock output, or GPIO) to enable or disable the resource if the proper conditions are met.

8.3.1.5 LDO Voltage Range

The output voltage range for the standard LDO regulators is 0.8 V to 3.3 V. For the RF-LDO regulators, LDO4 and LDO5, the output voltage range is 1.6 V to 3.3 V. The most significant bit for the voltage settings (the SEL[5] bit) on LDO4 and LDO5 is ignored and is internally set to 1b.

8.3.1.6 LDO Power-Good Comparator

The output voltage of each LDO regulator is supervised by an internal power-good comparator. The output of the comparator is set and cleared by the power-good bits in the PGOOD and PGOOD2 registers. The power-good bits are not valid if the LDO regulator is enabled but the input voltage to the LDO is less than 1 V.

8.3.2 Step-Down Converters

The synchronous step-down converter used in the power-management core includes a unique, hysteric PWM-controller scheme which enables switch frequencies over 3 MHz, excellent transient and AC load regulation, and operation with tiny and cost-competitive external components.

The controller topology supports forced PWM mode as well as power save mode operation. Power save mode operation reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses.

A significant advantage of this architecture compared to other hysteretic PWM-controller topologies is its excellent DC and AC load regulation capability in combination with low output-voltage ripple over the entire load range which makes this device well suited for audio and RF applications.

When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated and the high-side switch is turned on. The switch remains turned on until a minimum on time expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the current limit of the high-side switch. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero.

8.3.2.1 PWM and PFM Mode

In forced PWM mode, the device avoids pulse skipping and allows easy filtering of the switch noise by external filter components. PWM mode is forced by setting the DCDCx_MODE bit to 1b. If this bit is not set, the DCDCx outputs are in auto mode, which can switch to a low-current PFM mode when a light load occurs and sufficient headroom is present between the DCDCx input and output rails.

8.3.2.2 Low Quiescent Current Mode

Each step-down converter can be individually controlled to enter a low quiescent-current mode. This mode can be entered when the ECO bit is set to 1b and the proper conditions are met. In Eco-mode, the quiescent current is reduced and the output voltage is supervised by a comparator while most parts of the control circuitry are disabled to save power. Eco-mode should only be enabled when a converter has less than 2 mA of load current. In addition, the Eco-mode should be disabled prior to a load transient step to allow the converter to respond in a timely manner to the excess current draw. Setting the step-down converter into PWM mode by setting the DCDCx_MODE bit to 1b disables Eco-mode independently from the setting of the ECO bit.

8.3.2.3 Output Voltage Monitoring

Internal power-good comparators monitor the switching regulator outputs and detect when the output voltage is less than 90% of the programmed value. This information is used by the power-management core to generate interrupts depending on specific I^2C register settings. For more information, see Section 8.4.8. An individual power-good comparator of the switching regulator is blanked when the regulator is disabled or when the voltage of the regulator is transitioning from one set point to another.

8.3.2.4 Output Discharge

Each switching regulator is equipped with an output discharge enable bit located in the DISCHARGE2 register. When the DCDCx_DISCHARGE bit is set to 1b, the output of the regulator is discharged to ground with the equivalent of a 400-Ω resistor. If the enable bit of the regulator is set, the discharge bit is ignored.

8.3.2.5 Thermal Shutdown

Global thermal-shutdown protection is available for all step-down converters and LDOs. The thermal sensor generates an early warning depending on the setting of the THRM_REG register. If the temperature rises above the thermal shutdown threshold, the device is powered down to the OFF state.

8.3.2.6 Step-Down Converter Enable

The step-down converter enable and disable is part of the flexible power-up and power-down state machine. Each converter can be factory programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. The EN1, EN2, EN3, EN4, CLK_REQ1,

CLK_REQ2, and PWR_REQ (SLEEP) pins can be mapped to any resource (LDO, DC-DC converter, 32 kHz clock output, or GPIO) to enable or disable the resource.

8.3.2.7 Step-Down Converter Soft Start

The step-down converters in the TPS659128x device have an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within a time defined in Section 6. This ramp time limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled after the start-up time, t_{Start}, has expired. The DCDC4 converter has an option to set two different values for the start-up and ramp time. For applications that require a fast response, set the DCDC4_CTRL:RAMP_TIME bit to 1b.

During soft start, the output voltage ramp up is controlled as shown in Figure 8-1.

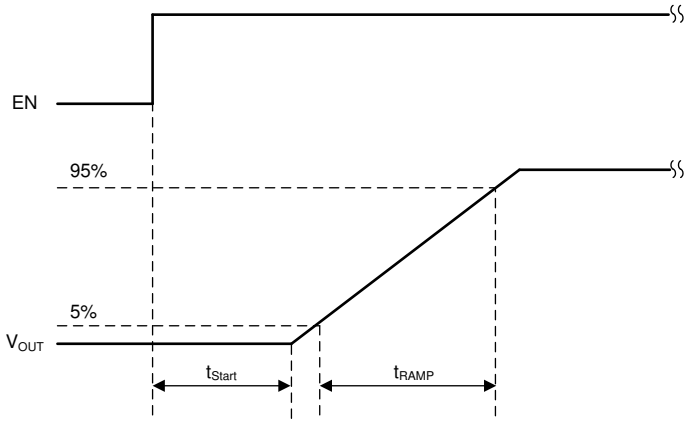


Figure 8-1. Soft Start

8.3.3 GPIOs

The TPS659128x device has five GPIOs. GPIO1 and GPIO2 are shared with the SPI and therefore they are not available if the SPI is used. GPIO3, GPIO4, and GPIO5 are for general-purpose use and are shared with the LED driver. The input and output stages of GPIO1 and GPIO2 are similar to GPIO3 however, they do not contain the LED current sink. If the output stage is programmed as a push-pull output, it pulls to the high-voltage set by the VDDIO pin. With the VDDIO supply voltage being less than the VDDIO UVLO threshold voltage, the high-side driver is disabled and the output is set to open drain.

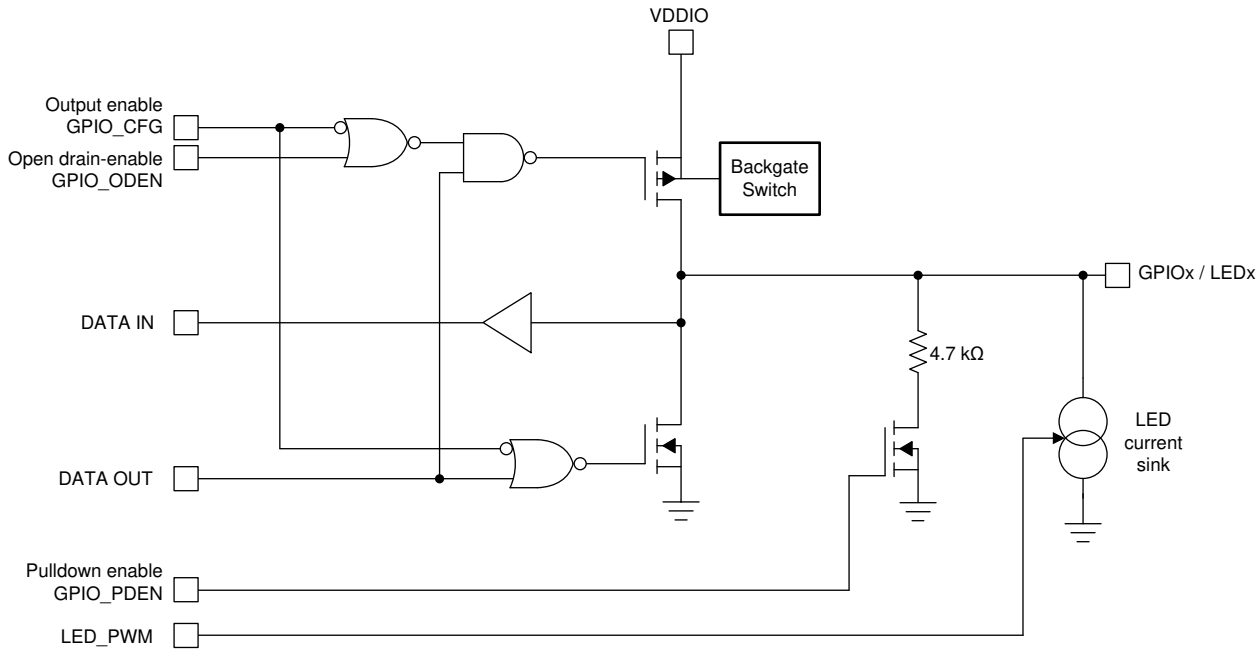


Figure 8-2. GPIO Block for GPIO3, GPIO4, and GPIO5

8.4 Device Functional Modes

8.4.1 Power State Machine

The embedded power controller (EPC) manages the state of the device and controls the power-up sequence.

The transitions for the state machine are shown in Figure 8-3 through Figure 8-8.

The EPC supports the following states:

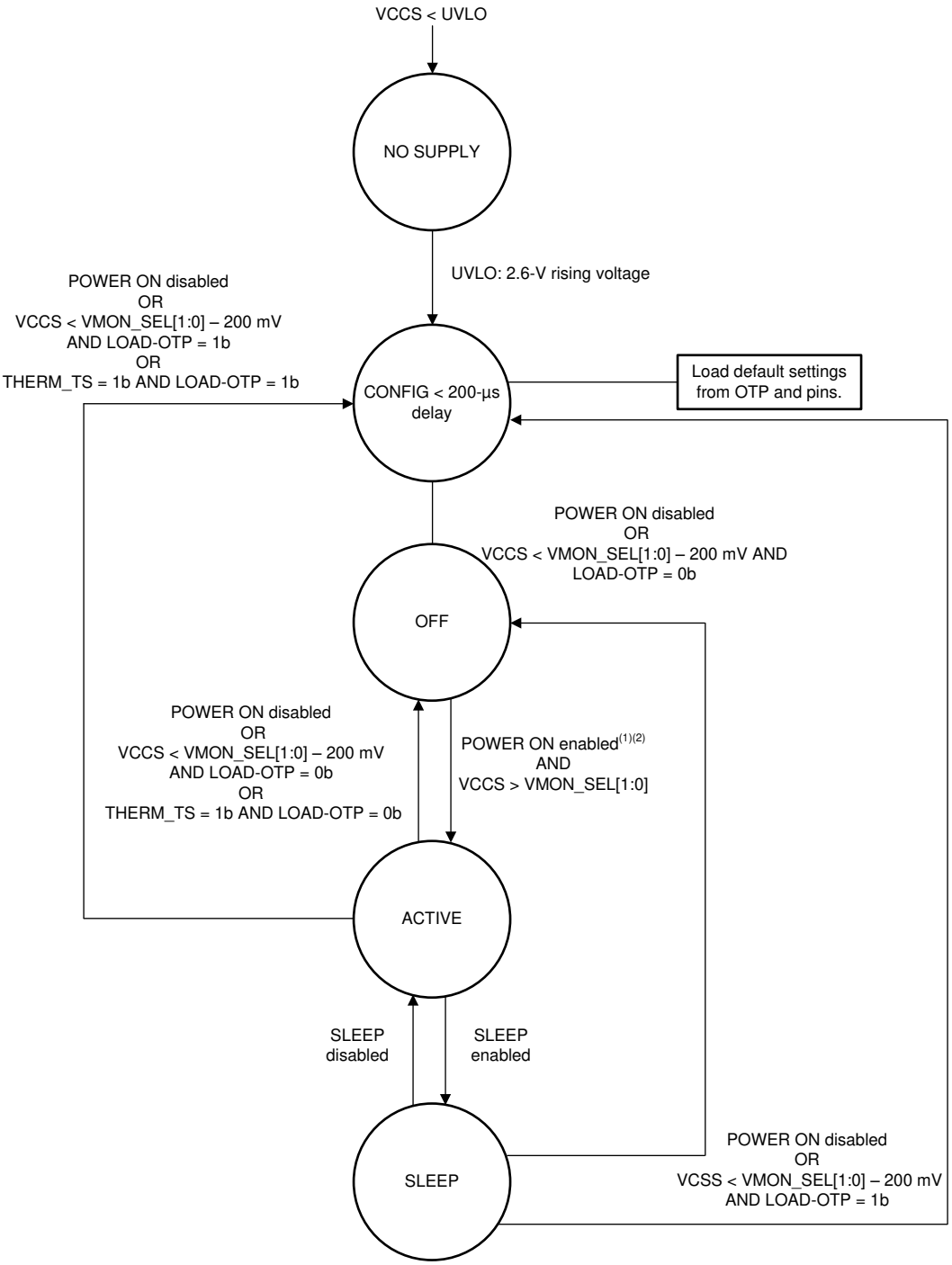
NO SUPPLY	The main battery-supply voltage is not high enough to power the LDOAO (LDO Always ON) regulator in this state. A global reset is asserted in this case. Everything on the device is off.
CONFIG	This state is entered either from the NO SUPPLY state automatically or from the ACTIVE or SLEEP state when the TPS659128x device is configured accordingly by the LOAD-OTP bit (bit 6) in the DEVCTRL register. When the CONFIG state is entered, all registers are set to their default value and the nRESPWRON pin is asserted.
OFF	The LDOAO regulator is on and internal logic is active in this state. All power supplies are off. The device can detect and execute a power-up sequence. The nRESPWRON pin is asserted.
ACTIVE	Device POWER-ON enable conditions are met and regulated power supplies are ON or can be enabled with full current capability in this state. A reset is released and the interfaces are active.
SLEEP	Device SLEEP enable conditions are met and selected regulated power supplies are in low-power or off mode in this state. Only used when CONFIG2 is shorted to GND.

8.4.2 Transition Conditions

The device transition conditions are:

- The device performs POWER ON transition when any of the following power on conditions are met:
  - nPWRON signal low level
  - PWRHOLD signal high level
  - PWRHLD bit in the DEVCTRL register set to 1b (OTP dependent default)
  - Interrupt flag active (default INT1 low) will generate a POWER ON enable condition for 5 seconds. During this time period, the processor or system is required to set PWRHOLD pin to high or set the PWRHLD bit in the DEVCTRL register to 1b to keep the device on. Interrupt sources generate POWER ON enable conditions only if they are not masked (OTP and register setting dependent).
- The device POWER ON transition will not occur if any of the following conditions are present:
  - nPWRON signal low level for more than the Long Press delay of 5 s. This can be disabled by setting the PWRON_LP_OFF and PWRON_LP_OFF_RST bits in the DEVCTRL2 register to 0b. The interrupt corresponding to this condition is the PWRON_LP_IT in INT_STS_REG register. The interrupt is generated after 4 s to allow processor to mask PWRON_LP_OFF if desired.
  - Die temperature has reached the thermal shutdown threshold (THERM_TS bit in THRM_REG register is 1b)
- Device performs POWER OFF transition from ACTIVE state if none of the POWER ON conditions are met, if long key press takes priority, the DEV_OFF bit is set to 1b, or die temperature reaches thermal shutdown threshold.
- Device performs ACTIVE to SLEEP transition when all of the following happen:
  - The interrupt flag is inactive, meaning there are no unmasked interrupts pending
  - The SLEEP_ENABLE bit in the DEVCTRL2 register is set to 1b
  - The SLEEP pin is active (polarity depending on SLEEP_POL bit in the DEVCTRL2 register)

  Alternatively, as long as no interrupts are pending, the DEV_SLP bit can also put the device into the SLEEP state with higher priority than the SLEEP pin. When the DEV_SLP bit is used, there must be an unmasked interrupt to cause SLEEP to ACTIVE transition, otherwise device will remain in SLEEP until set to OFF state and the DEV_SLP bit is cleared. It is not recommended to use the DEV_SLP bit when the CONFIG2 pin is shorted to LDOAO.
- The device has two different reset scenarios:
  - Full reset: all digital of device is reset
    - This reset is caused by a power-on reset (POR) when VCCS < UVLO.
  - General reset, where only OTP backed register bits are reloaded:
    - This reset is caused by a turnoff event while the LOAD-OTP bit is set to 1b.
    - A turnoff event happens when the PWRON_LP_OFF_RST bit is set to 1b.
    - The nPWRON pin can also be set in OTP to cause reset when pulled low longer than 100 ms.



A. Alternatively, the PWRHLD bit in the DEVCTRL register can be factory programmed to 1b in OTP, causing immediate power up. In this case, the bit must be set to 0b to allow normal device shutdown.

B. SLEEP state only applies when CONFIG2 is shorted to GND.

Figure 8-3. EPC State Machine

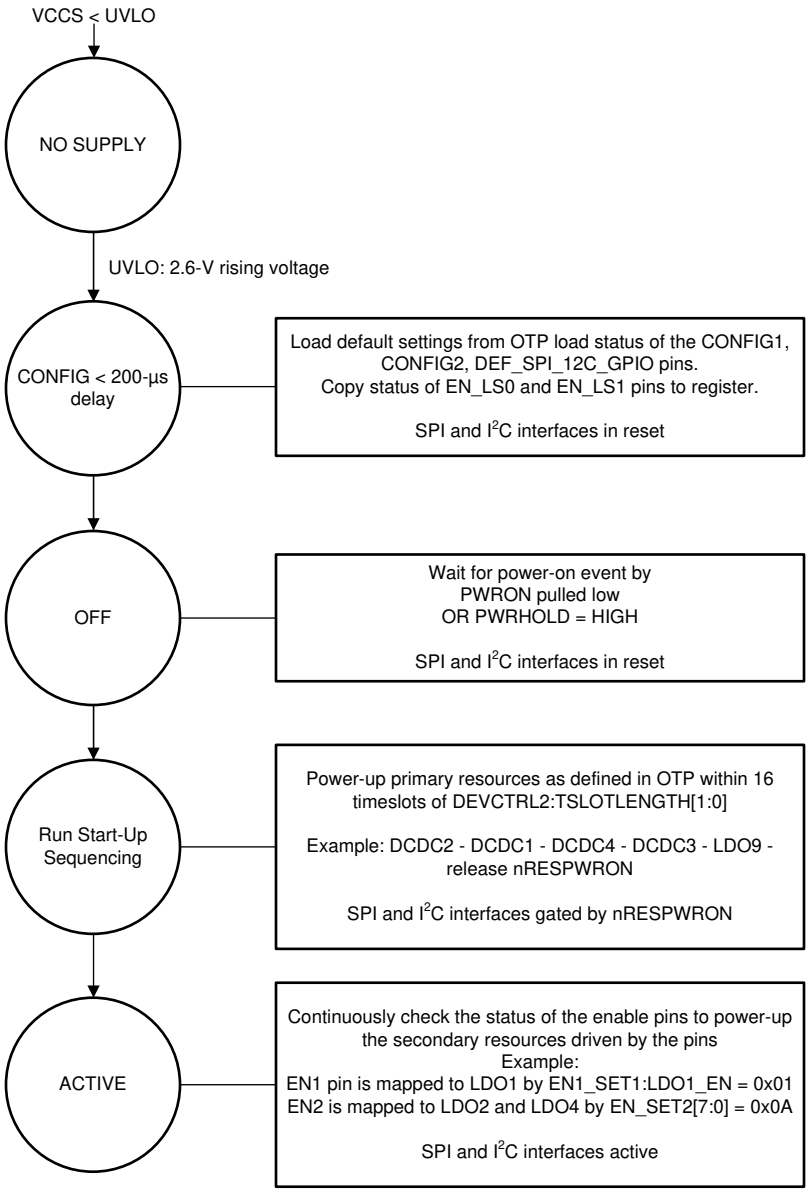


Figure 8-4. STARTUP Flow for CONFIG2 Pin Shorted to LDOAO

Figure 8-4 is valid when the CONFIG2 pin is shorted to LDOAO. The EN1, EN2, EN3, and EN4 pins are used as enable pins to enable one or several resources. The EN1_SET1 and EN1_SET2 registers define which converters or LDO regulators are controlled by the EN1 pin. The EN2, EN3, and EN4 are configured similarly.

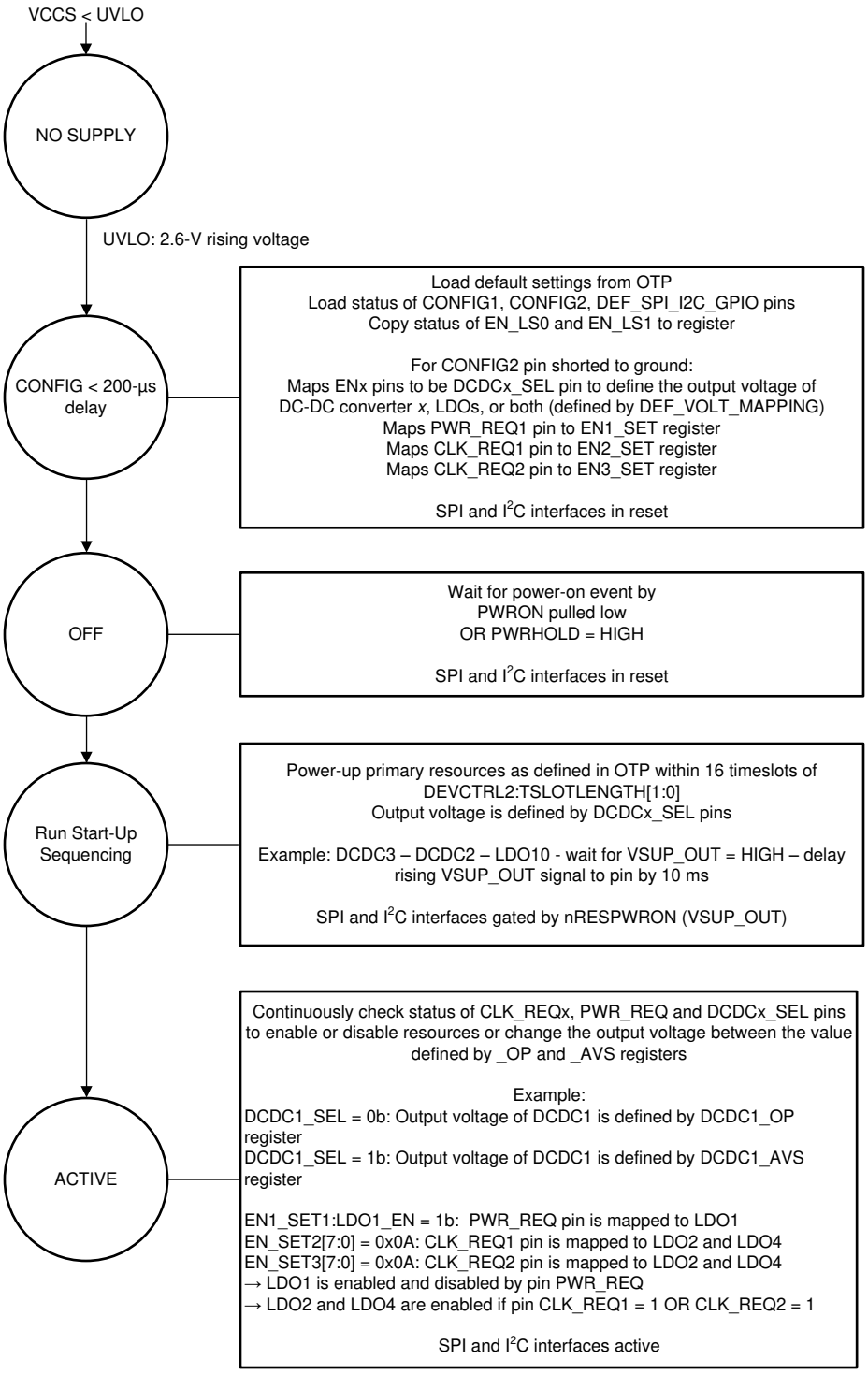


Figure 8-5. STARTUP Flow for CONFIG2 Pin Shorted to GND

Figure 8-5 is valid when the CONFIG2 pin is shorted to GND. The EN1, EN2, EN3, and EN4 pins are remapped as DCDCx_SEL pins, defining which register is used to set the output voltage on a specific DC-DC converter. For example, connecting the DCDC1_SEL pin to GND sets the output voltage of the DCDC1 converter to what is defined by the DCDC1_OP register. Connecting the DCDC1_SEL pin to a logic level high sets the output voltage to what is defined by the DCDC1_AVS register. The DCDC2 voltage is defined by the DCDC2_SEL pin and so forth.

The LDO1 to LDO4 regulators can be mapped to the DCDCx_SEL pins. The DEF_VOLT_MAPPING register defines which LDO regulator is controlled by which DCDCx_SEL pin.

Additionally, shorting the CONFIG2 pin to GND also remaps the SCL_AVS, SDA_AVS, and SLEEP pins as CLK_REQ1, CLK_REQ2, and PWR_REQ pins. The functionality is similar to the ENx pins.

The EN1_SET1 and EN1_SET2 registers define which resource is controlled by the PWR_REQ pins, the EN2_SETx register defines the resource controlled by the CLK_REQ1 pin, and the EN3_SETx register defines the resources controlled by the CLK_REQ2 pin.

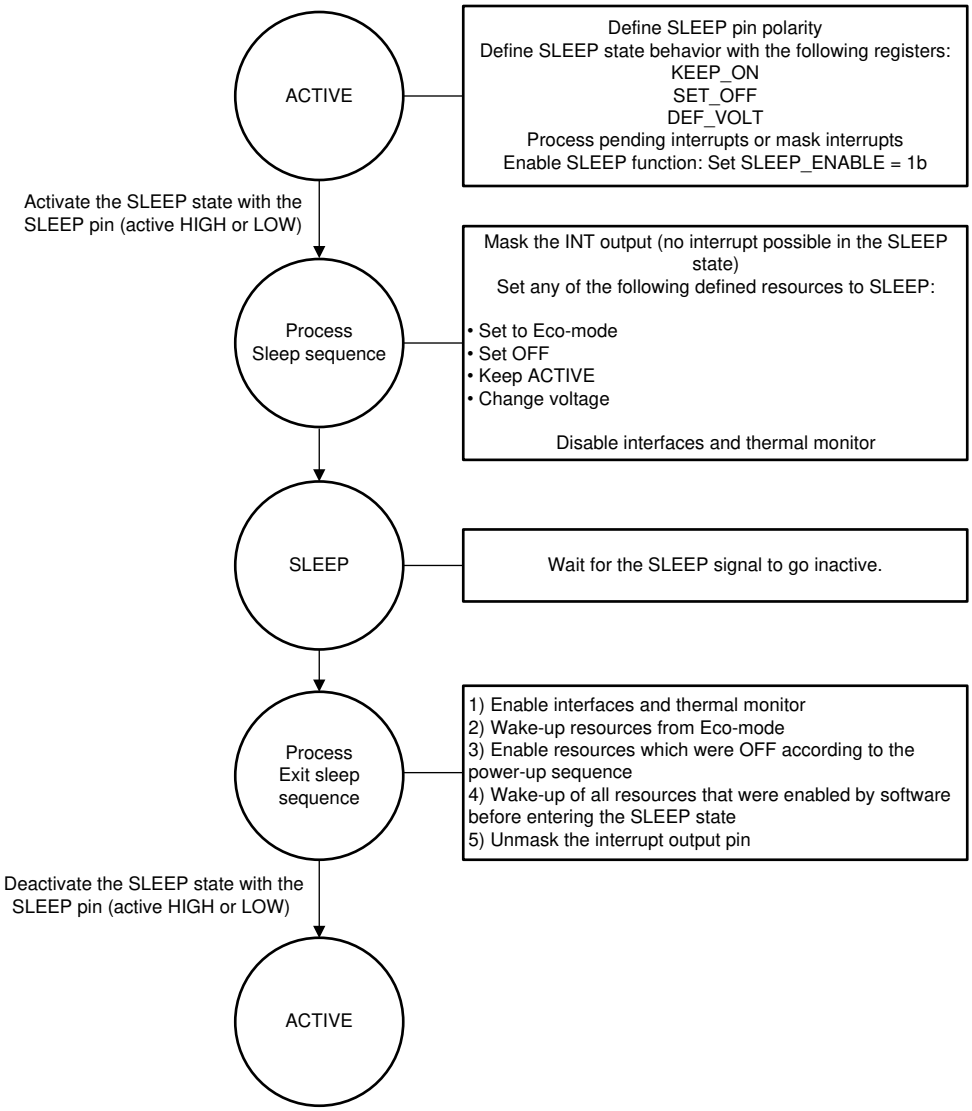


Figure 8-6. SLEEP Flow for CONFIG2 Pin Shorted LDOAO

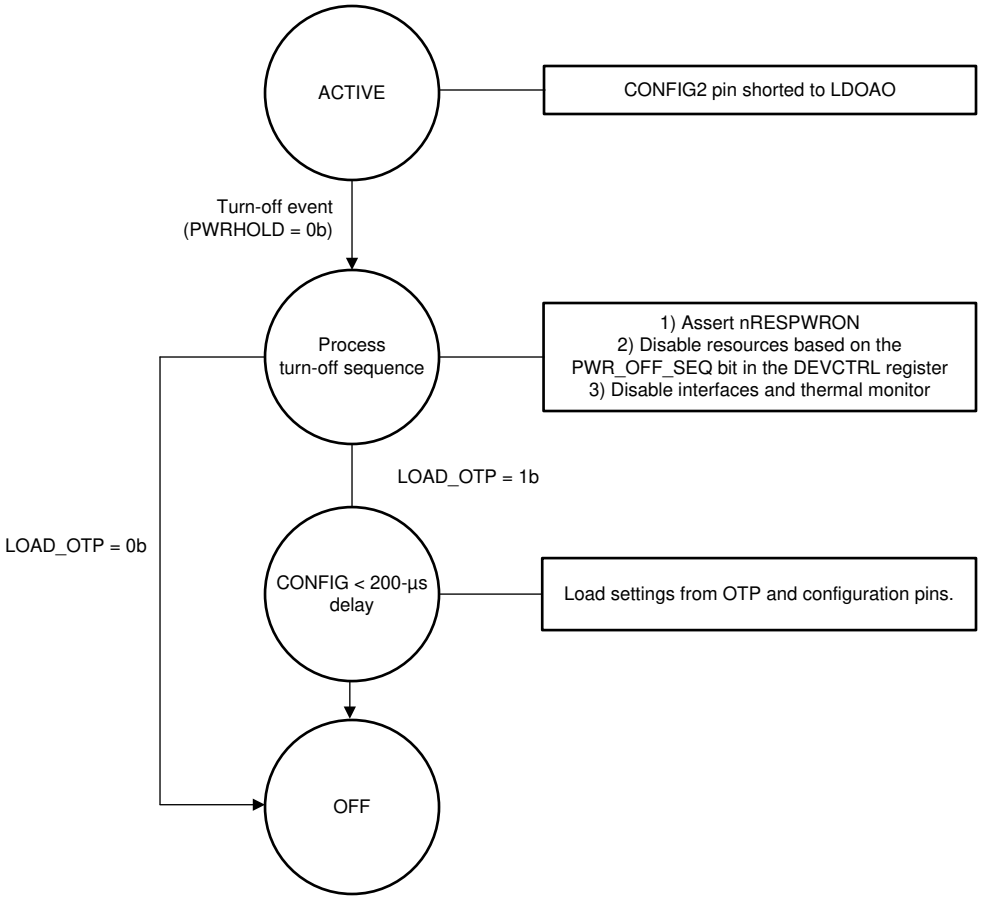


Figure 8-7. SHUTDOWN Flow for CONFIG2 Pin Shorted to LDOAO

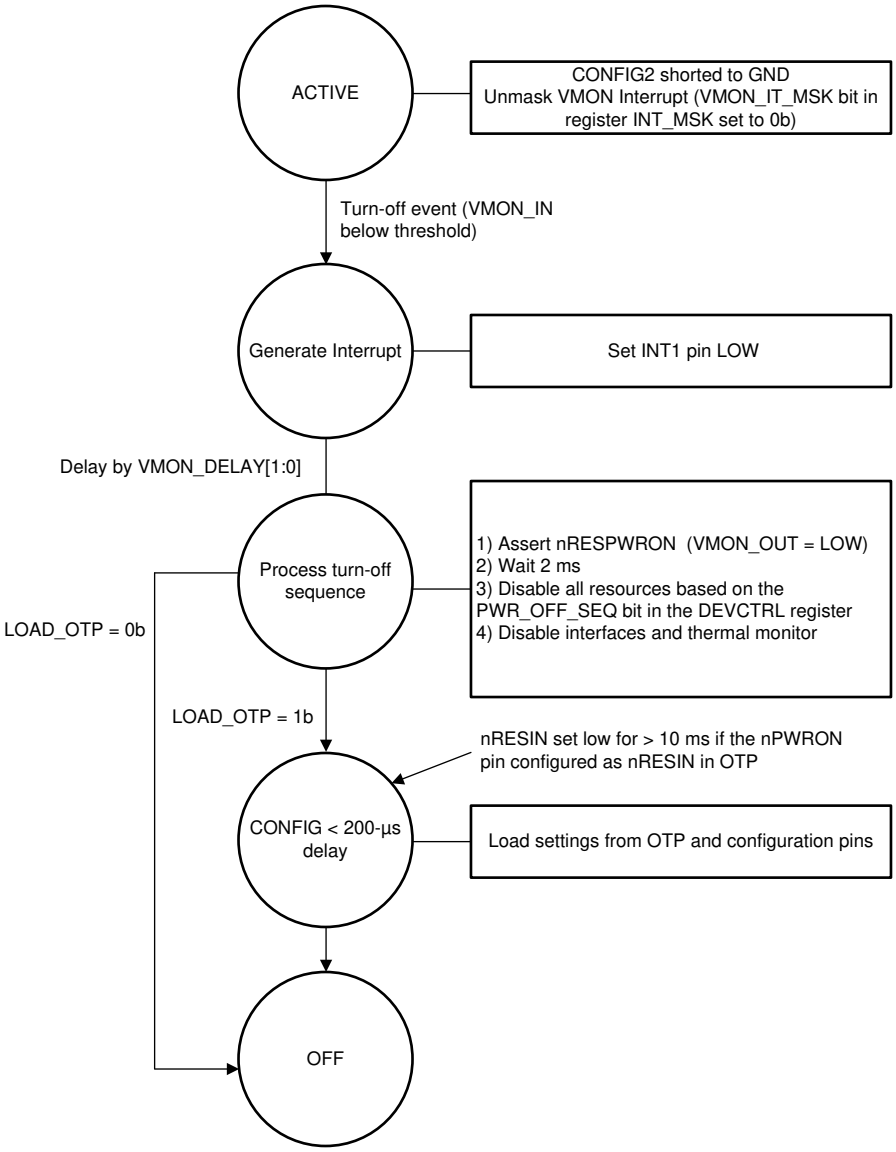


Figure 8-8. SHUTDOWN Flow for CONFIG2 Pin Shorted to GND

8.4.3 Implementation of Internal Power-Up and Power-Down Sequencing

The TPS659128x can internally enable resources during power up (going to the ON state) and power down (going to the OFF state), and for entering and exiting the SLEEP state. The internal power sequencing is defined in the factory programmed OTP memory. The sequencing can enable resources in 15 time slots during power up and power down. A resource can be associated to any of these 15 time slots that will be processed in the opposite direction during power down. Four settings are programmable for the delay and are effective for all 15 time slots:

Table 8-1. TSLOT_LENGTH Delay Options

Bits	Delay
00b	30 µs
01b	200 µs
10b	500 µs
11b	2 ms

Resources can include:

- Step-down converters
- LDO regulators
- 32-kHz clock output
- nRESPWRON output

Resources that are not part of the automatic sequencing can be configured such that they are enabled by external pins or by their enable bit in the register set once the device is in the ACTIVE or SLEEP states. Resources that are enabled automatically should not be assigned to an external enable pin. A *break point* can be defined which stops power-up sequencing and allows power-up sequencing to resume once voltage monitoring conditions are met. This break point prevents power up until the voltage of the voltage monitors exceeds a certain limit.

As shown in Figure 8-9, resources can be mapped to any of the time slots with none, one, or multiple resources for any time slot.

Note

Figure 8-9 is an example of the programmability of the sequencing and does not match the settings for a particular OTP of the device. For individual part-number settings, refer to the application report specific for each orderable part number.

For entry to the SLEEP state and exit from the SLEEP state, only three time slots are used with a 120-µs delay between time slots.

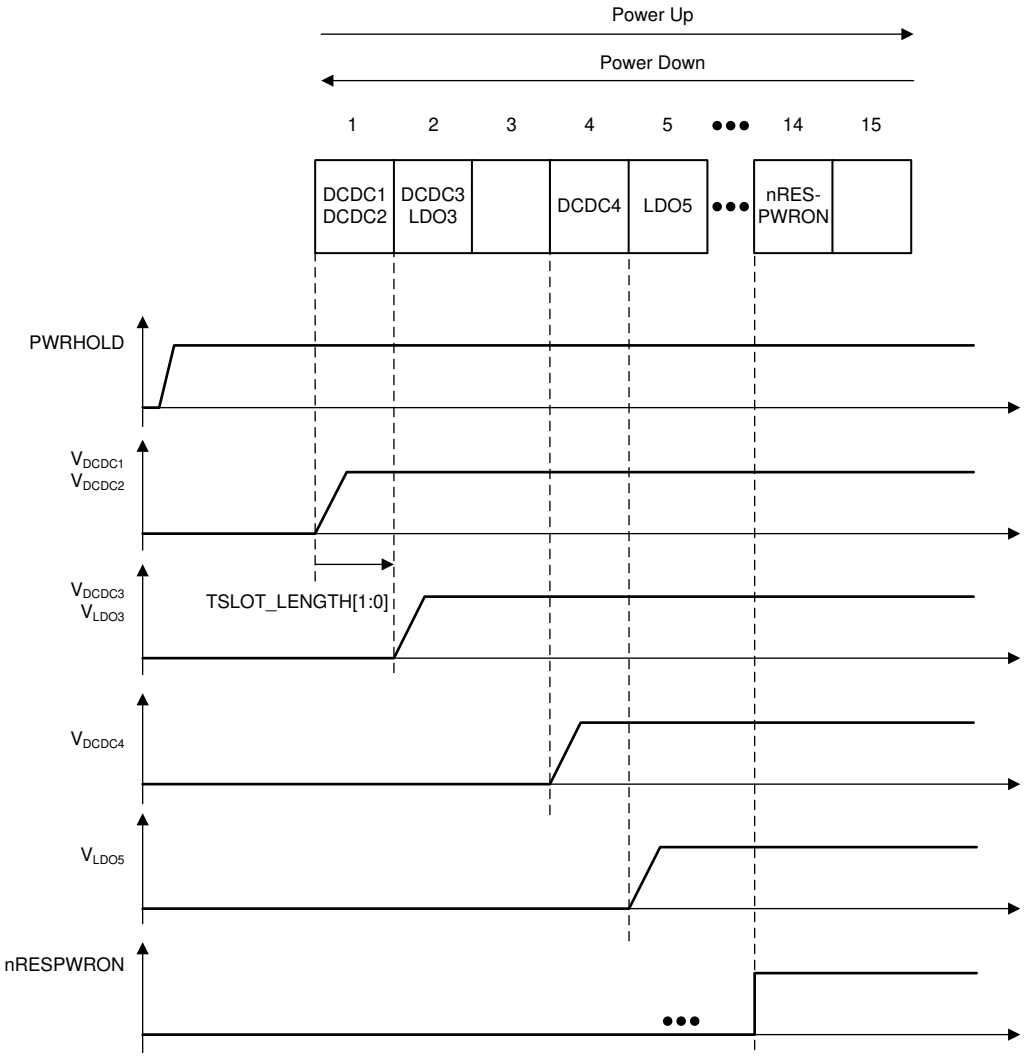


Figure 8-9. Internal Power-Up Example

8.4.4 Summary of CONFIG2, Device State, and Enable Pin Settings on Regulators

The behavior of the regulators is impacted by the state of various settings which can be modified by hardware, software, and part number specific settings. The LDOs are more simplistic and are shown first. The DCDCs are shown second and include an additional resource mode (force PWM). Both cases also indicate which voltage setting register (xxx_OP or xxx_AVS) is used. The following tables assume the LDOx_ENABLE bit or DCDCx ENABLE bit is set to 1b. Setting this bit to 0b will cause the resource to be off in all cases.

8.4.4.1 LDO Mode Summary

The LDO regulators can be off, on in normal-mode, or on in Eco-mode. Which mode the regulator is in depends on several variables which can be defined by the part-number specific settings, the host processor software, and the hardware configuration. The configurations are best broken into two categories. The first configuration applies when a regulator has been assigned to an external pin by the host processor or by OTP in any of the ENx_SETx registers. This configuration has few dependencies. The second configuration applies to all other cases. A summary of these two can be found in the following tables.

Table 8-2. LDO Mode Summary - Assigned LDO

Assigned Pin(s) State(1)	KEEP_ON Bit(2)	SET_OFF Bit(2)	Resource Mode
Low	0b	1b	Off

Table 8-2. LDO Mode Summary - Assigned LDO (continued)

Assigned Pin(s) State(1)	KEEP_ON Bit(2)	SET_OFF Bit(2)	Resource Mode
Low	0b	0b	Eco
Low	1b	x	Normal
High	x	x	Normal

(1) This is an OR of all assigned pins. If any of the assigned pins goes high, the pin state is considered high.
(2) There is a separate bit for each regulator.

Table 8-3. LDO Mode Summary - Unassigned LDO

CONFIG2	Device State	KEEP_ON Bit(1)	SET_OFF Bit(1)	ECO Bit(1)	Resource Mode
GND	—	x	x	0	Normal
GND	—	x	x	1	Eco
LDOAO	ACTIVE	x	x	0	Normal
LDOAO	ACTIVE	x	x	1	Eco
LDOAO	SLEEP	0	0	x	Eco
LDOAO	SLEEP	0	1	x	Off
LDOAO	SLEEP	1	x	0	Normal
LDOAO	SLEEP	1	x	1	Eco

(1) There is a separate bit for each regulator.

8.4.4.2 DCDC Mode Summary

The DCDC regulators are similar to the LDO regulators, but they have an additional on state option to choose between auto and force PWM modes.

Table 8-4. DCDC Mode Summary - Assigned DCDC

Assigned Pin(s) State(1)	DCDCx_MODE Bit(2)	KEEP_ON Bit(2)	SET_OFF Bit(2)	Resource Mode
Low	x	0	1	Off
Low	0	0	0	Eco
Low	0	1	x	Auto
Low	1	0	0	PWM
Low	1	1	x	PWM
High	0	x	x	Auto
High	1	x	x	PWM

(1) This is an OR of all assigned pins. If any of the assigned pins goes high, the pin state is considered high.
(2) There is a separate bit for each regulator.

Table 8-5. DCDC Mode Summary - Unassigned DCDC

CONFIG2	Device State	KEEP_ON Bit(1)	SET_OFF Bit(1)	DCDCx_MODE Bit(1)	ECO Bit(1)	Resource Mode
GND	—	x	x	0	0	Auto
GND	—	x	x	0	1	Eco
GND	—	x	x	1	x	PWM
LDOAO	ACTIVE	x	x	0	0	Auto
LDOAO	ACTIVE	x	x	0	1	Eco
LDOAO	ACTIVE	x	x	1	x	PWM
LDOAO	SLEEP	0	0	0	x	Eco
LDOAO	SLEEP	0	0	1	x	PWM
LDOAO	SLEEP	0	1	x	x	Off

Table 8-5. DCDC Mode Summary - Unassigned DCDC (continued)

CONFIG2	Device State	KEEP_ON Bit(1)	SET_OFF Bit(1)	DCDCx_MODE Bit(1)	ECO Bit(1)	Resource Mode
LDOAO	SLEEP	1	x	0	0	Auto
LDOAO	SLEEP	1	x	0	1	Eco
LDOAO	SLEEP	1	x	1	x	PWM

(1) There is a separate bit for each regulator.

8.4.4.3 Voltage Selection Summary

All four DCDC regulators have two voltage register options, one located in the DCDCx_OP register and one in the DCDCx_AVS register. The first four LDOs (LDO1, LDO2, LDO3, and LDO4) also have LDOx_OP and LDOx_AVS registers. The selection of which voltage is used can be summarized in the following table.

Table 8-6. Voltage Selection Summary

CONFIG2	Assigned Pin(s) State or Device State(1)	SELREG Bit(2)	DEF_VOLT Bit(2)	DCDCx_SEL Pin(3)	Voltage
GND	—	x	x	1	_AVS
GND	—	x	x	0	_OP
LDOAO	High or ACTIVE	1	x	—	_AVS
LDOAO	High or ACTIVE	0	x	—	_OP
LDOAO	0 or SLEEP	1	x	—	_AVS
LDOAO	0 or SLEEP	0	1	—	_AVS
LDOAO	0 or SLEEP	0	0	—	_OP

(1) For any regulators which are set in an ENx_SETx register, this is an OR of all assigned pins. If any of the assigned pins goes high, the pin state is considered high. For any regulators which are not set in an ENx_SETx register, the device state is used.
(2) There is a separate bit for each regulator.
(3) For LDO1, LDO2, LDO3, and LDO4, this is based on the DEF_VOLT_MAPPING register.

8.4.5 Details of CONFIG2, Device State, and Enable Pin Settings on Regulators

The full details of the behavior of the device based on the above signals and settings is outlined below.

8.4.5.1 EN1, EN2, EN3, and EN4 Resources Control

The ENx control signals can turn resources on and off as well as setting them into Eco-mode or changing the output voltage register from _AVS to _OP. Assigning several resources to one ENx control signal is possible. Assigning a resource to several ENx control signals is also possible. The inputs are connected to an OR gate, so if any assigned ENx pin is high, the assigned resource is considered enabled. Default configuration of the ENx control signals is done in OTP memory; however, changing the ENx settings after power up is possible through the ENx_SETx registers. The ENx control signals are effective only in the ACTIVE or SLEEP state. For more information on how the pin status on the ENx pin is interpreted, see Section 8.4.5.4.

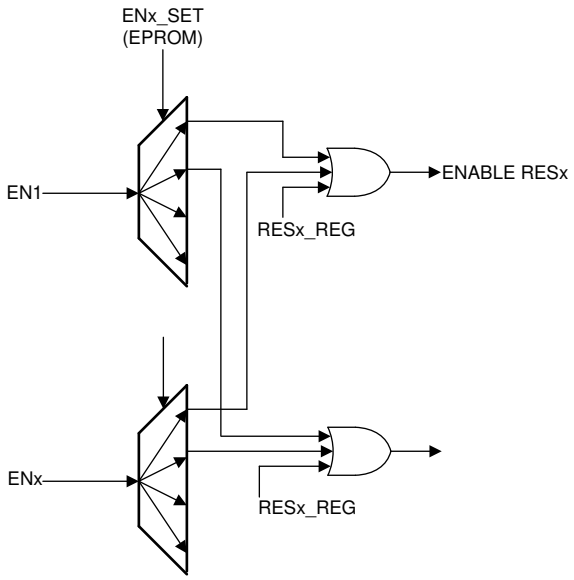


Figure 8-10. ENx Architecture

8.4.5.2 Device SLEEP State Control

The sleep control input on the SLEEP pin is used to move the device into the SLEEP state where the resources behavior (DC-DC converters, LDO regulators, 32-kHz clock output, and thermal monitor) are defined by the SET_OFF, KEEP_ON, and DEF_VOLT registers. The SLEEP pin is only active if the SLEEP_ENABLE bit in the DEVCTRL2 register is set to 1b and all unmasked interrupts are cleared. Otherwise, the state of the SLEEP pin is ignored. Additionally, the polarity of the SLEEP pin is controlled by the SLEEP_POL bit in the DEVCTRL2 register.

8.4.5.3 SET_OFF, KEEP_ON, and DEF_VOLT Registers Used in SLEEP State with CONFIG2 Pin Shorted to LDOAO

The DCDC1, DCDC2, DCDC3, and DCDC4 converters and LDO1, LDO2, LDO3, and LDO4 regulators allow changing the output voltage depending on the ACTIVE state versus SLEEP state. To program the SET_OFF, KEEP_ON, and DEF_VOLT registers:

- Keep the resource enabled in the SLEEP state by setting the KEEP_ON bit to 1b. The SET_OFF bit is ignored in this case. The DEF_VOLT bit will determine whether _OP (0b) or _AVS (1b) voltage is used in this case.
- Set the resource to Eco-mode in the SLEEP state by setting the SET_OFF bit to 0b and the KEEP_ON bit to 0b. The DEF_VOLT bit will determine whether _OP (0b) or _AVS (1b) voltage is used in this case.
- Turn the resource off in the SLEEP state by setting the SET_OFF bit to 1b and the KEEP_ON bit to 0b.

8.4.5.4 SET_OFF, KEEP_ON, and DEF_VOLT Registers Used for Resources Assigned to an External Enable Pin with CONFIG2 Pin Shorted to LDOAO

As described in Section 8.4.3, a resource can be assigned to an enable pin. In this case, the SLEEP state of the device has no effect on an assigned resource. Instead, the behavior of the resource is defined by the state of the enable pin. The SET_OFF, KEEP_ON, and DEF_VOLT registers are remapped and used to define how a resource functions when the enable pin is set low or is set high. When the resource's assigned ENx pin is high, the assigned resource behaves as if the device was in the ACTIVE state. When the resource's assigned ENx pin is low, the assigned resource behaves as if the device was in the SLEEP state. To control the resource:

- The resource is enabled when the ENx pin is set high. The SET_OFF and KEEP_OFF bits are ignored in this case.
- Enable the resource when the ENx pin is set low by setting the KEEP_ON bit to 1b. The SET_OFF bit is ignored in this case.

- Disable the resource when the ENx pin is set low by setting the SET_OFF bit to 1b and the KEEP_ON bit to 0b.
- Set the resource to Eco-mode when the ENx pin is set low by setting the SET_OFF bit to 0b and the KEEP_ON bit to 0b.
- Change the output voltage of a resource when the ENx pin is set low:
  - Set the DEF_VOLT bit to 0b and the voltage will be defined by the _OP register.
  - Set the DEF_VOLT bit to 1b and the voltage will be defined by the _AVS register.

8.4.5.5 SET_OFF, KEEP_ON, and DEF_VOLT Registers Used for Resources Assigned to Pins PWR_REQ, CLK_REQ1 and CLK_REQ2 with CONFIG2 pin shorted to GND

With the CONFIG2 pin tied to GND, the ENx pins are used as the voltage-select pins (DCDCx_SEL) for the DC-DC converters and LDO regulators assigned to these pins by the DEF_VOLT_MAPPING register. These pins are only used to switch the output voltage between two values as defined in the _OP (DCDCx_SEL pin set to 0) and _AVS (DCDCx_SEL pin set to 1) registers.

The basic function of enabling or disabling resources is remapped to the PWR_REQ, CLK_REQ1, and CLK_REQ2 pins. The pin function is managed by the ENx_SETx registers in the following list.

- PWR_REQ: EN1_SETx
- CLK_REQ1: EN2_SETx
- CLK_REQ2: EN3_SETx

The EN4_SETx register is not used and should be set 0h.

8.4.5.6 Configuration Pins CONFIG1, CONFIG2, and DEF_SPI_I2C-GPIO

The TPS659128x device contains two banks of OTP memory that define the programmed default settings. The CONFIG1 pin selects between these two banks of memory. The logic level at the CONFIG1 pin in the CONFIG state determines which of the OTP banks is used. The content of that OTP bank is then copied to the user registers to set all OTP configurable options, such as default voltages and power-up timing.

The CONFIG2 bit is used to remap functions to pins. When the CONFIG2 pin is shorted to LDOAO, the EN1, EN2, EN3, EN4, SCL_AVS, SDA_AVS, and SLEEP pins are active. When the CONFIG2 pin is shorted to GND, these pins are used as DCDCx_SEL, CLK_REQ1, CLK_REQ2, and PWR_REQ pins. Table 8-7 lists the default and alternative pin functions.

Table 8-7. Pin Configuration Based on CONFIG2 Pin

CONFIG2 PIN SHORTED TO LDOAO; DEFAULT PIN USAGE	DEFAULT FUNCTION	CONFIG2 PINSHORTED TO GND; ALTERNATE PIN USAGE	ALTERNATE FUNCTION
EN1	Enable pin for a set of DC-DC converters and LDOs defined by register EN1_SET1 and EN1_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN1=0	DCDC1_SEL	DCDC1_SEL = 1b: output voltage is defined by DCDC1_AVS register DCDC1_SEL = 0b: output voltage is defined by DCDC1_OP register
EN2	Enable pin for a set of DC-DC converters and LDOs defined by register EN2_SET1 and EN2_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN2=0	DCDC2_SEL	DCDC2_SEL = 1b: output voltage is defined by DCDC2_AVS register DCDC2_SEL = 0b: output voltage is defined by DCDC2_OP register
EN3	Enable pin for a set of DC-DC converters and LDOs defined by register EN3_SET1 and EN3_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN3=0	DCDC3_SEL	DCDC3_SEL = 1b: output voltage is defined by DCDC3_AVS register DCDC3_SEL = 0b: output voltage is defined by DCDC3_OP register
EN4	Enable pin for a set of DC-DC converters and LDOs defined by register EN4_SET1 and EN4_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN4=0	DCDC4_SEL	DCDC4_SEL = 1b: output voltage is defined by DCDC4_AVS register DCDC4_SEL = 0b: output voltage is defined by DCDC4_OP register
SLEEP	Used to transition the device between the ACTIVE and SLEEP states when there are no pending interrupts and the SLEEP_ENABLE bit is set to 1b. Polarity controlled by the SLEEP_POL bit.	PWR_REQ	Enable pin for a set of DC-DC converters and LDOs Defined by register EN1_SET1 and EN1_SET2

Table 8-7. Pin Configuration Based on CONFIG2 Pin (continued)

CONFIG2 PIN SHORTED TO LDOAO; DEFAULT PIN USAGE	DEFAULT FUNCTION	CONFIG2 PINSHORTED TO GND; ALTERNATE PIN USAGE	ALTERNATE FUNCTION
SCL_AVS	Clock input of the voltage scaling (AVS) I²C interface	CLK_REQ1	Enable pin for a set of DC-DC converters and LDOs Defined by register EN2_SET1 and EN2_SET2
SDA_AVS	Data input/output of the voltage scaling (AVS) I²C interface	CLK_REQ2	Enable pin for a set of DC-DC converters and LDOs Defined by register EN3_SET1 and EN3_SET2

The DEF_SPI_I2C-GPIO pin defines whether the SPI or the I²C interface is used as the standard communication interface. Setting the DEF_SPI_I2C-GPIO to 0 defines SPI as the standard interface associated to the SCL_SCK, SDA_MOSI, GPIO1_MISO, and GPIO2_CE pins. The CONFIG1, CONFIG2, and DEF_SPI_I2C-GPIO pins should be tied to GND for a low level and to the LDOAO pin for a logic high level.

The CONFIG1, CONFIG2, and DEF_SPI_I2C-GPIO pins should not be switched in operation but hardwired to a logic-low level (GND) or a logic-high level by connecting the pins to the LDOAO voltage.

8.4.6 Active Voltage Scaling Control

The output voltage of all the DCDC regulators, LDO1, LDO2, LDO3, and LDO4 can be changed during operation to match the system requirements. For example, this feature is useful for processors looking to minimize power loss or maximize performance. Alternatively, it can be used to select between different voltages based on the system configuration. For example, if different DDR options are available, then voltage can be selected to match the requirement of the DDR. The voltage can be changed in two different ways, outlined below.

8.4.6.1 Voltage-Scaling Interface Control Using _OP and _AVS Registers With SPI or I²C Interface

Typically, the standard SPI or I²C interface is used to communicate with the part. If there is a potential that the added voltage scaling bus traffic would interfere with other operations, a dedicated I²C interface is available for voltage scaling functionality. Resources are assigned to this interface by setting the DCDCx_AVS bits in the I2C_SPI_CFG register. The interface works in three different modes.

- With CONFIG2 shorted to LDOAO, the standard I²C or SPI voltage scaling interface can be used where output voltage is set in the resource's AVS and OP registers and the SELREG and DEF_VOLT bits are used to switch between the two voltage values.
- With CONFIG2 shorted to LDOAO, the power-I²C voltage scaling interface can be used instead. It operates the same as standard I²C but access to the DCDCx_OP and DCDCx_AVS registers of the assigned regulators use an alternate I²C address and cannot be accessed through the standard I²C bus. This is enabled with the DCDCx_AVS bits in the I2C_SPI_CFG register.
- With CONFIG2 shorted to GND, DCDCx_SEL pins can be used as roof or floor configuration where the DC-DC voltage switches between the value defined in the DCDCx_OP register and the DCDCx_AVS register.

The voltage slew rate of the DCDCx regulators reaching a new programmed value is programmable though the TSTEP bits located in the DCDCx_CTRL registers.

Both I²C interfaces are compliant with HS-I²C specification (100 kbits/s, 400 kbits/s, or 3.4 Mbits/s)

Shorting the CONFIG1 pin to GND selects OTP option A. Shorting the CONFIG1 pin to LDOAO selects the OTP option B. These values are loaded only during the device CONFIG state.

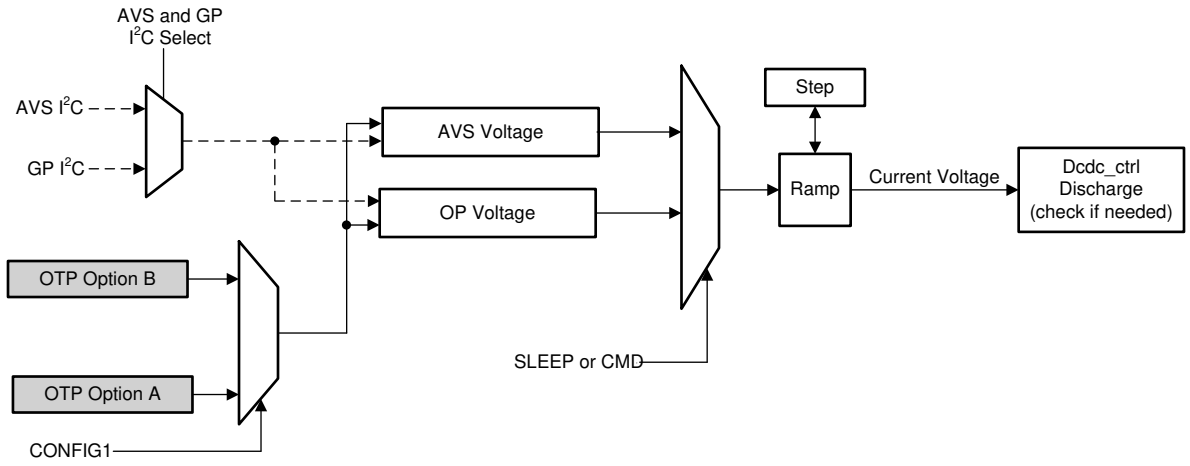


Figure 8-11. DC-DC Voltage Scaling Architecture

8.4.6.2 Voltage Scaling Using the VCON Decoder on VCON_PWM and VCON_CLK Pins

For specific processors, there is an option to set the voltage using analog signals, rather than I²C or SPI. For such processors, the output voltage control for the DCDC1 converter can be controlled by the VCON pins when the VCON_ENABLE bit in the DCDC1_CTRLregister is set to 1b.

When enabled, VCON sets the voltage based on the VCON_PWM signal duration during 32 cycles of the VCON_CLK signal. The VCON decoder validates that the generated output voltage does not exceed 1.1 V when a 25-mV step size is selected. For PWM ratios 0:32 to 7:32, the output voltage is fixed at 1.1 V. Four ranges can be selected by setting the VCON_RANGE[1:0] bits in the DCDC1_CTRL register.

The VCON_CLK and VCON_PWM signal must be active and one complete frame (32 clock cycles) must be received by the TPS659128x device before it is enabled with the VCON_ENABLE bit. When the VCON_ENABLE bit is set to 0b, the voltage setting is reverted back to the DCDC1_AVS or DCDC1_OP register depending on the pins summarized in Table 8-6 and the range bits also revert back to the value set in the DCDC1_LIMIT register. For VCON mode, the RANGE bits and MAX_SEL bits in the DCDC1_LIMIT register are ignored.

The function calculates the desired converter voltage based on the incoming PWM information. The maximum CLK frequency is 30 MHz. The period of the PWM signal is 1/32 of VCON_CLK. The decoding follows Equation 1.

$$V_{OUT} = V_{RANGE\_MAX} - \text{Count} \times \text{Step Size} \quad (1)$$

where

- V_{OUT} is the resulting converter voltage.
- V_{RANGE_MAX} is the maximum voltage from the voltage range selected in the VCON_RANGE bits.
- Count is the number of VCON_CLK cycles during which VCON_PWM is high within 32 clock cycles of VCON_CLK.
- Step Size is the step size from the voltage range selected in the VCON_RANGE bits

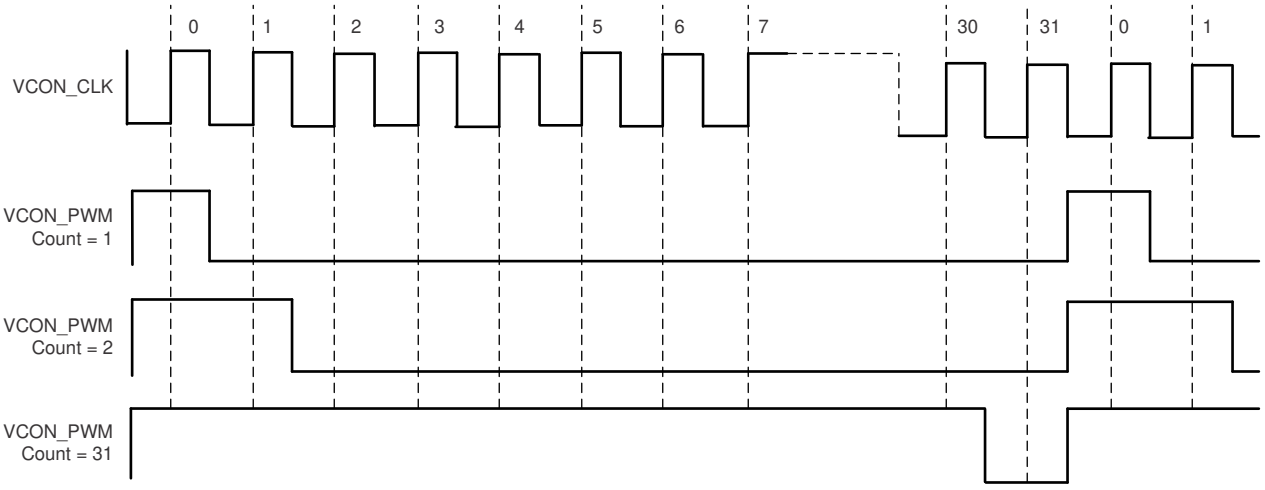


Figure 8-12. VCON Voltage Scaling Architecture

8.4.7 VDDIO Voltage for Push-Pull Output Stages

A number of outputs are available that are push-pull outputs or can be configured as push-pull outputs. Any pin with a push-pull output stage generates its output high level by the voltage applied to the VDDIO pin. The input voltage range on the VDDIO pin is 1.6 V to 3.3 V with an UVLO threshold below 1.6 V. With a VDDIO voltage below the UVLO threshold, the high-side driver of the push-pull output stages is disabled and the output default goes back to open drain. The affected pins include:

- nRESPWRON / VSUP_OUT push-pull or open drain defined by the nRESPWRON_OUTPUT bit in the DEVCTRL register
- INT1 push-pull or open drain defined by the INT_OUTPUT bit in the DEVCTRL2 register
- GPIO1, GPIO2: push-pull only
- GPIO3, GPIO4, GPIO5: push-pull or open drain managed by the GPIOx registers
- OMAP_WDI_32k_OUT

8.4.8 Digital Signal Summary

The digital signals are defined as:

SLEEP When all SLEEP conditions are met (the CONFIG2 pin is shorted to LDOAO, no pending interrupts, and SLEEP_ENABLE bit set to 1b), the SLEEP pin can be used to enter the SLEEP state which impacts LDO regulator and DC-DC converter behavior based on the settings defined in the SET_OFF, KEEP_ON, and DEF_VOLT registers. An interrupt or a change in the SLEEP pin level causes a transition back to the ACTIVE state. This input signal is level sensitive and no debouncing is applied. The SLEEP pin is configurable and is disabled by default, so at power up, its status is ignored. The SLEEP_ENABLE bit in the DEVCTRL2 register is used to make the SLEEP pin active and its active level is changed between active HIGH or active LOW using the SLEEP_POL bits. The SLEEP state can also be entered using the DEV_SLP bit in the DEVCTRL register as long as no interrupts are pending, however an interrupt must be unmasked to trigger a SLEEP-to-ACTIVE transition or else the device will stay in the SLEEP state until the device enters the OFF state.

PWRHOLD The PWRHOLD pin can be used as ON/OFF signal input when the nPWRON pin and interrupt are not used or in parallel with these power-on conditions. The PWRHOLD pin can also be used as an acknowledge (maintain power) of a power-up sequence triggered by an interrupt or the falling edge of the nPWRON pin. The PWRHOLD input signal is level sensitive and no debouncing is applied. The rising edge, falling edge, or both edges of the PWRHOLD pin are highlighted through an associated interrupt if the interrupt is unmasked.

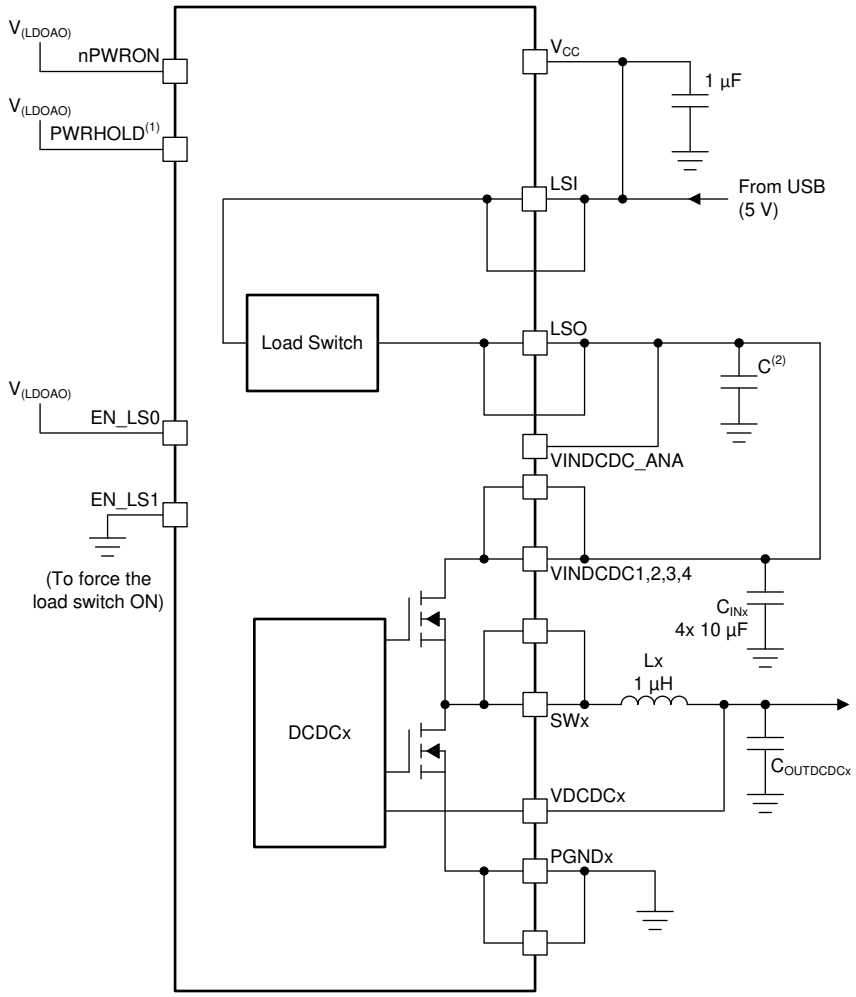
NRESPWRON/ VSUP_OUT	The NRESPWRON signal is used as the reset to the processor and is in the VDDIO domain. The signal is held low until the ACTIVE state is reached. For detailed timing, see the relevant application note for the part number specific settings. The VSUP_OUT signal is the output of the voltage monitor that can alternatively be used as a reset to a processor. It can be included in the power sequencing such that the power-up sequence is delayed until its output is HIGH or the device powers down when the output is LOW.
32KCLKOUT	This signal is the output of the 32-kHz RC oscillator, which can be enabled during the power-on sequence. This signal can be enabled and disabled by setting the CLK32KOUT_EN bit in the CLK32KOUT register when the device is in the ACTIVE state.
nPWRON	The nPWRON input is generally connected to an external button. A debounced falling edge on this signal causes a transition from the OFF state to the ACTIVE state. If the device is in the ACTIVE or SLEEP state, then a low level on this signal can generate an interrupt. If the nPWRON signal is low for more than 5 seconds, one of the PWRON_LP_OFF bits are set to 1b, and the corresponding PWRON_LP_IT interrupt is not acknowledged by the external processor in 1 second, then the device goes to the OFF state. An OTP option is available to have falling edge of nPWRON pin cause device reset. When used this way, it is described as nRESIN.
INT1	The INT1 signal (active low) warns the host processor of any event that occurred on the TPS659128x device. The host processor can then poll the interrupt from the interrupt status register through I^2C to identify the interrupt source. If the INT_POL bit is set to 0b, a low level indicates an active interrupt, highlighted in the INT_STSx registers. An active Interrupt flag generates a POWER ON enable condition pulse of 5 seconds only when the device is in the OFF state (when the NRESPWRON signal is low). The POWER ON enable condition pulse will occur only if the interrupt status bit is initially inactive (no previous interrupt pending in the status register). The interrupt status register must be cleared first to allow device to power off during the 5 second pulse duration. Any of the interrupt sources can be masked programming INT_MSKx registers. The default setting is masking all interrupts. When an interrupt is masked, its corresponding interrupt status bit is still updated, but the INT1 flag is not activated. Interrupt source masking can be used to mask a device switch-on event. The INT output can be programmed as push-pull or open drain output stage with either active LOW or active HIGH output defined by two OTP settings.
GPIO1, GPIO2, GPIO3, GPIO4, GPIO5	The GPIOx signals are muxed with the LED and SPI. The GPIOx signal can be used for event detection or control of external resources during power up.
VCCS/VIN_MON	This signal is the input for the internal UVLO monitor. The block provides a selectable low-battery warning as well as a undervoltage shutdown.
VCON_CLK, VCON_PWM	These signals are the clock and data inputs for voltage scaling of the DCDC1 converter using a custom PWM type voltage scaling. The feature is enabled by the VCON_ENABLE bit in the DCDC1_CTRL register. When enabled, voltage scaling through the DCDC1_OP and DCDC1_AVS registers is blocked.
CLK, MOSI, MISO, CE	These signals are the clock, chip enable (CE), master-in slave-out (MISO), and master-out slave-in (MOSI) pins for the SPI . The pins are shared with the standard I^2C interface SCL and SDA and GPIO1 and GPIO2.
DEF_SPI_I2C-GPIO	This signal defines whether multifunction pins are used for the SPI or for the I^2C interface and GPIOs. When the DEF_SPI_I2C-GPIO pin is set to low, the function is assigned to the SPI on the CLK, MOSI, MISO, and CE pins. When the DEF_SPI_I2C-GPIO pin is set to high, the function is assigned to the I^2C interface and GPIOs on the SCL, SDA, GPIO1, and GPIO2 pins.
SCL_AVS, SDA_AVS	These signals are used in the power I^2C interface, typically used for DVS on the step-down converters. Each step-down converter has a bit to switch the voltage scaling registers from

the standard I^2C interface or SPI to the power-I^2C interface. When switched to the power-I^2C, the register is blocked for access through the standard interface.

8.4.9 Load Switch

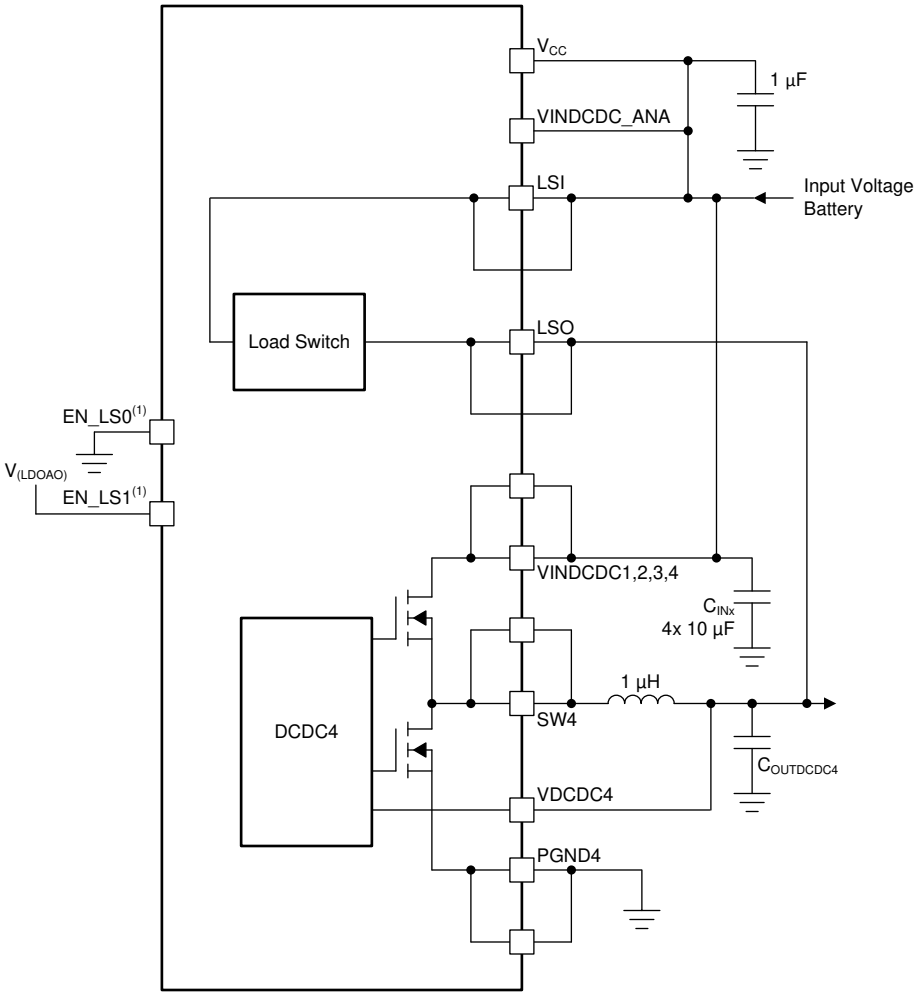
The load switch on the TPS659128x device can be used as the following:

- Bypass switch for the DCDC4 converter
- Current limited switch if the TPS659128x device is used in USB-powered applications
- A switch to turn on and off high current loads such as SD cards



A. Tie the PWRHOLD pin to LDOAO voltage to turn on automatically when 5 V is applied.
B. The capacitor size is dependent on buffer requirements.

Figure 8-13. Load Switch Connected as USB Input Current Limited Switch



A. The EN_LS1 pin must be high and the EN_LS0 pin must be low to auto-enable the load switch based on the comparator in DCDC4.

Figure 8-14. Load Switch Connected as BYPASS Switch for DCDC4

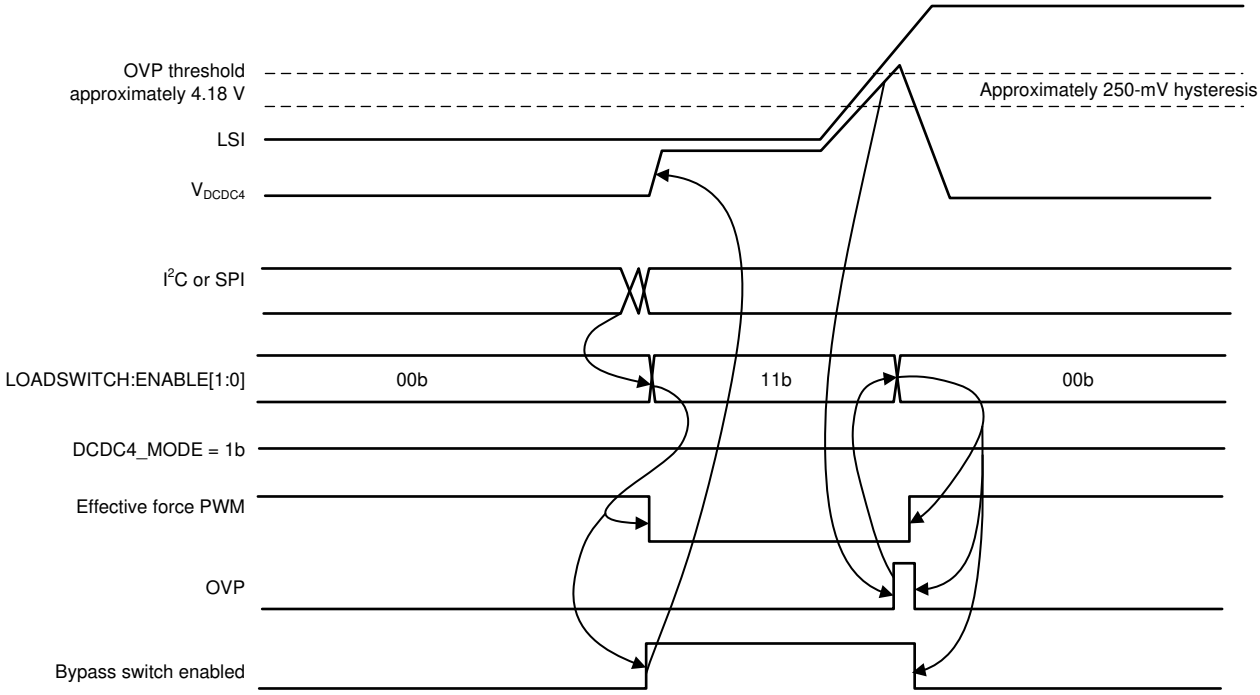
The LOADSWITCH register allows the load switch to be used as a bypass switch on the DCDC4 converter or as a current limited switch. Four programmable current limits are available from 90 mA (typical) to 2.5 A with the default current defined by an OTP setting. The enable bits are mapped to the external pins, EN_LS0 and EN_LS1. The status of the pins is copied to the register in the CONFIG state and therefore the usage of the load switch can be externally predefined. In the ACTIVE state (or SLEEP state) the functionality of the load switch is controlled by the ENABLE0 and ENABLE1 bits only to turn the load switch on, turn it off, or assign it to a comparator as a bypass switch for the DCDC4 converter. When the enable function is set to the comparator, it is auto-enabled based on the voltage differential of V_{IN} to V_{OUT} on the DCDC4 step-down converter.

Two additional features are available in case the load switch is used as a bypass switch for the DCDC4 converter. The following features are enabled with the LOADSWITCH:ENABLE[1:0] bit by setting it to either 10b or 11b:

- Forced PWM mode of the DCDC4 converter is blocked if the bypass switch is closed
- The bypass switch is opened automatically when a overvoltage condition happens. The LOADSWITCH:ENABLE[1:0] bit is automatically set 00b in an overvoltage event so the switch is opened.

In applications where the load switch is used as an USB-input current limited switch or as a load switch on the output of a DC-DC converter to LDO regulator, the previously listed features must be disabled. This case happens when the load switch is enabled by setting the LOADSWITCH:ENABLE[1:0] bit to 01b.

For more information, see the LOADSWITCH register in Register Descriptions.



A. OVP enable = LOADSWITCH:ENABLE[1:0] = 10b or 11b LOADSWITCH:ENABLE[1] = 0b → OVP enable = OVP = 0 If OVP hysteresis < V_{DCDC4} < OVP when LOADSWITCH:ENABLE[1] goes high, OVP indicates V_{DCDC4} < OVP

Figure 8-15. Load Switch Timing for LOADSWITCH:ENABLE[1:0] = 10b or 11b

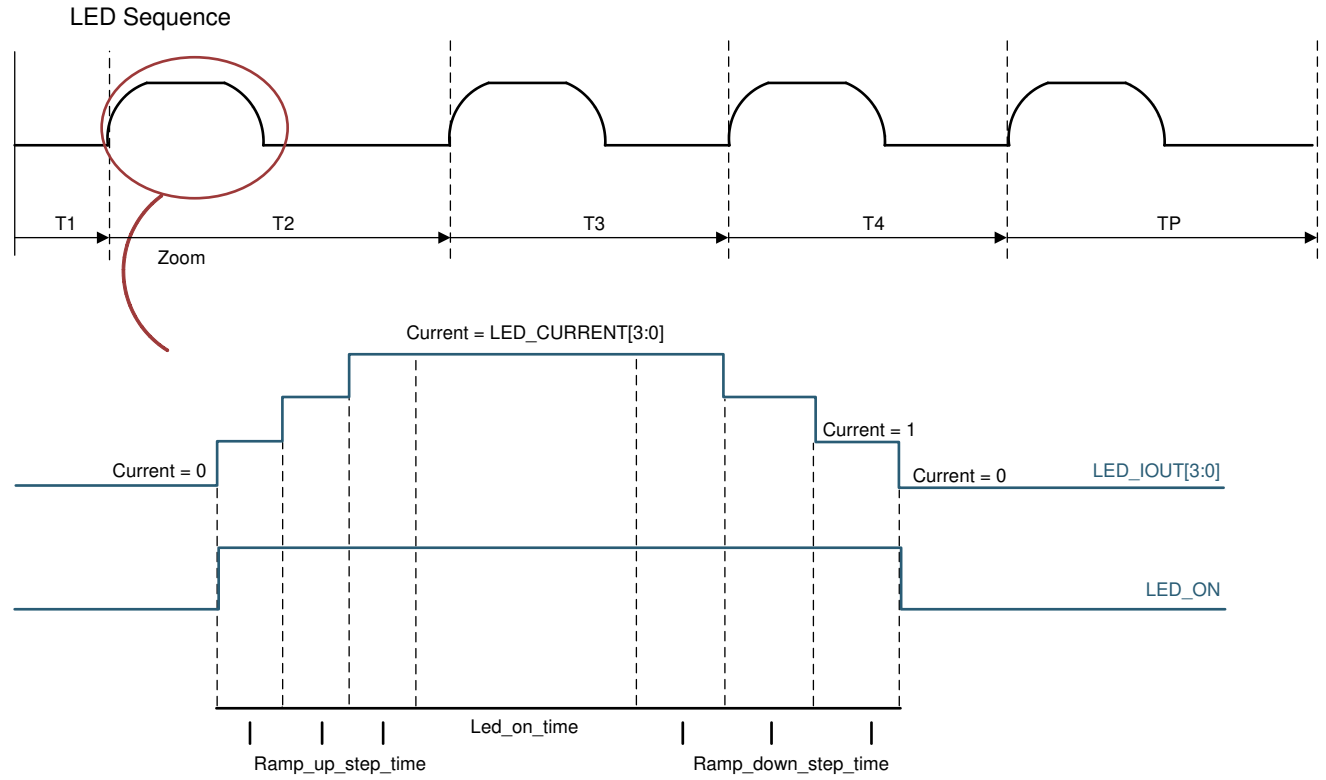
8.4.10 LED Driver

The GPIO3, GPIO4, and GPIO5 resources can alternatively be configured to drive the LEDs by setting the GPIO_SEL bit to 1b in the GPIOx register. This setting switches the output stage to a current sink controlled by the LED control registers (LEDx_CTRLx, LED_RAMP_UP_TIME, LED_RAMP_DOWN_TIME, and LED_SEQ_EN). The LEDs are enabled in the LED_SEQ_EN register. The LED current sink is pulse-width modulated with the duty cycle defined by the LEDx_PWM[4:0] bit in the LEDx_CTRL7 register. All three GPIOs should either be assigned as an LED driver or as a standard GPIO.

To turn on LEDA with a constant current of 10 mA:

- Set the GPIO as an LED current sink output by setting the GPIOA:GPIO_SEL bit to 1.
- Set the constant current to 10 mA by setting the LEDA_CTRL1:LEDA_CURRENT[3:0] bit to 0100b.
- Set the PWM duty cycle to 100% by setting the LEDA_CTRL7:LEDA_PWM[4:0] bit to 11111b.
- Enable the LEDA current sink by setting the LED_SEQ_EN:LEDA_EN bit to 1b.

In addition to turning on and turning off an LED, the LED driver allows the user to set LED sequence to perform a flash sequence in the hardware by enabling the flash sequencer. Setting the LEDx_SEQ_EN bit enables the flash sequencer for each of the three LEDs.



T1, T2, T3, T4 : 0, 1 ...127 × 64 ms → reg ledx_t1, ledx_t2 ….

Tp : 0, 1 …127 × 64 ms → reg ledx_tp

Ramp step time : 0, 1 … 31 × 8 ms → reg led_ramp_up_time, led_ramp_down_time

Figure 8-16. LED Sequencer

The LED driver allows the user to set a DC current from 2 mA to 20 mA for each LED. In addition to this ability, an LED flash sequence is programmable and defined by the time slots T1, T2, T3, T4, and TP. Within these time slots, the LED can be turned on as defined by the LEDx_ON_TIME bit with a defined ramp-up slope set by the LED_RAMP_UP register and a defined ramp-down slope set by the LED_RAMP_DOWN register. The slopes are set to the same value for all three LEDs but other parameters are programmable independently. Figure 8-16 shows an LED flash cycle. The ramp enable bits define whether the current immediately steps to its defined value (set by the LEDx_CURRENT[3:0] bit) or ramps with a certain slope. If the LEDx_RAMP_EN bit is set to 0b during a sequence, the current immediately goes to the value defined by the LEDx_I[3:0] bit. If the LEDx_RAMP_EN bit is set to 1b during a sequence, the current steps up and down to the value defined by the LEDx_I[3:0] bit with a certain slope.

In addition, the LED current is pulse-width modulated with a duty cycle defined in the LEDx_CTRL7 register.

For the LED driver to operate properly, the time for RAMP_UP + LED_ON + RAMP_DOWN must be smaller than the sequence T*n* (with n = 1, 2, 3, 4, P).

8.4.11 Thermal Monitoring and Shutdown

Two thermal-protection modules monitor the junction temperature of the device against the respective thresholds:

- Hot-die temperature threshold
- Thermal shutdown temperature thresholds

When the hot-die temperature threshold is reached, an interrupt is sent to the software (SW) to close the noncritical running tasks.

The output of both thermal protection modules is logically ORed. When the thermal shutdown temperature threshold is reached, the TPS659128x device is set under reset and a transition to the OFF state is initiated. Then the POWER ON enable conditions of the device are not taken into consideration until the die temperature has decreased below the hot-die threshold. A hysteresis is applied to the hot-die and shutdown threshold when detecting a falling edge of temperature, and both detections are debounced to avoid any parasitic detection. The TPS659128x device allows the user to program four hot-die temperature thresholds to increase the flexibility of the system.

By default, the thermal protection is enabled in the ACTIVE state, but it can be disabled through programming the THRM_REG register. The thermal protection is automatically enabled during a transition from the OFF state to the ACTIVE state and is kept enabled in the OFF state after a switch-off sequence caused by a thermal shutdown event. A transition to the OFF state sequence caused by a thermal shutdown event is highlighted in the INT_STS_REG status register. Recovery from this OFF state is initiated (switch-on sequence) when the die temperature falls below the hot-die temperature threshold.

The threshold detection state for the hot-die and thermal shutdown temperature can be monitored or masked by reading or programming the THRM_REG register. A hot-die interrupt can be masked by programming the INT_MSK_REG register.

8.4.12 Interfaces

The TPS659128x device has three available interfaces which are a high-speed I^2C interface that has access to all register, a SPI that can optionally be used to access all registers, and a high-speed power I^2C interface that can be used to dynamically change the output voltage of the DC-DC converters. The power I^2C interface only has access to the voltage scaling registers of the DC-DC converters. If it is activated by a selection bit, the registers it is using are blocked for the general-purpose I^2C or SPI. All interfaces are active only in the ACTIVE state. In all other states, the interfaces are held in a reset and cannot be used to access the device.

8.4.12.1 Serial Peripheral Interface

The serial peripheral interface (SPI) uses four signals: a chip enable (SPI_CE), the clock from the bus master (SPI_CLK), an input port (SPI_MOSI), and an output port (SPI_MISO). The read-write (R/W) bit is followed by an 8-bit register address followed by 7 bits of unused bits followed by the data bits. The MISO output is set to high impedance when the TPS659128x device is not addressed by setting the CE pin LOW which allows multiple slaves on the SPI bus.

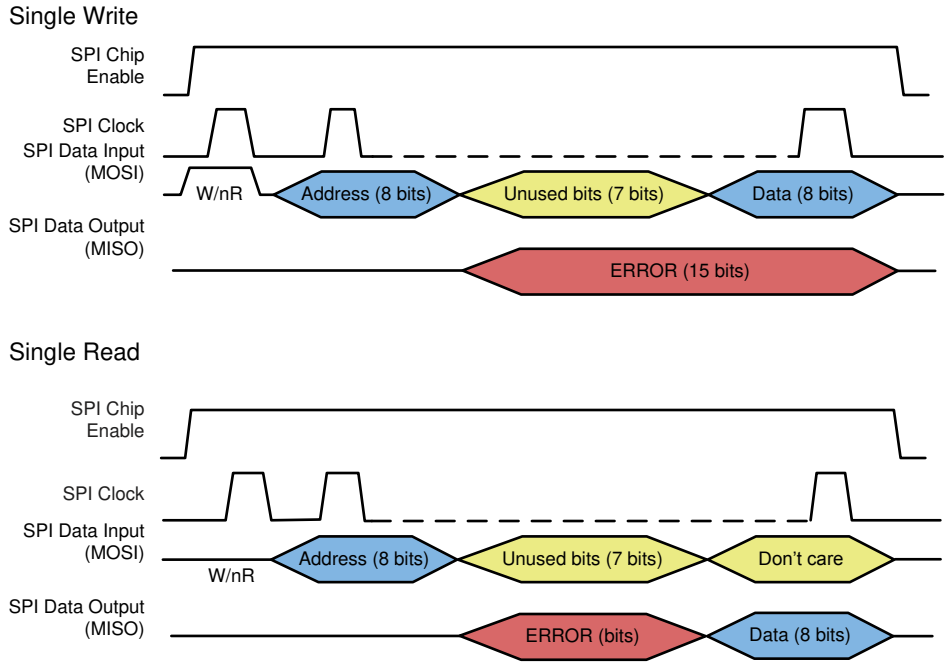


Figure 8-17. SPI READ and WRITE Protocol

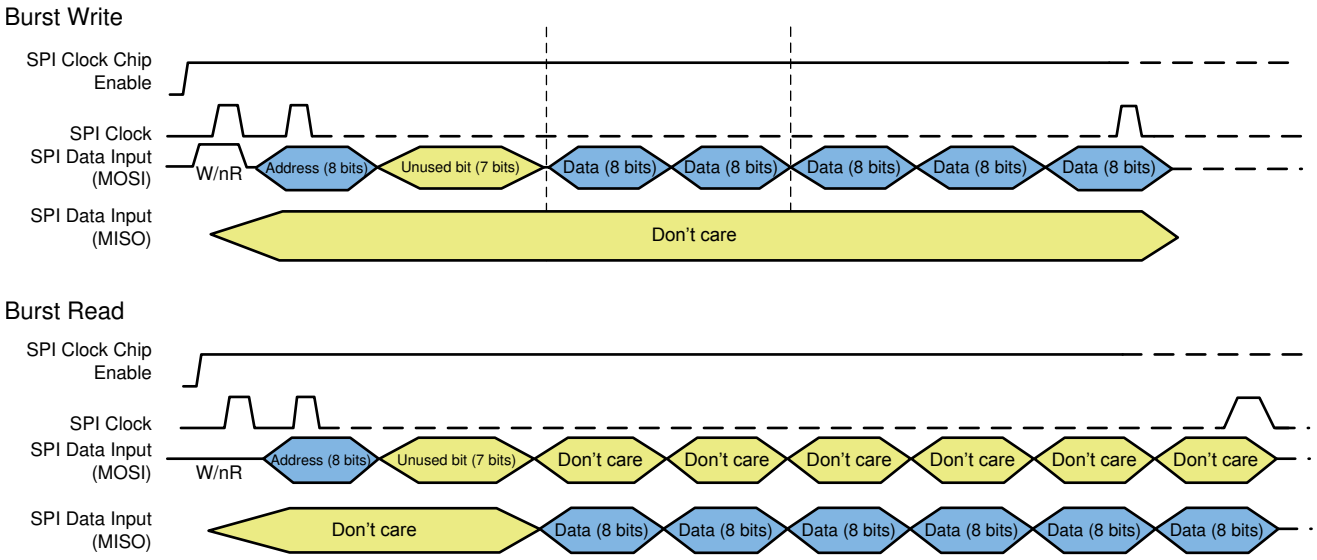


Figure 8-18. SPI BURST READ and BURST WRITE Protocol

8.4.12.2 I²C Interface

I²C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both the SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, the SDA pin, and the SCL pin. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives, transmits data, or does both on the bus under control of the master device.

The TPS659128x device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to the TPS659128x device that is higher than the UVLO level of 2.4 V. When the device is in the ACTIVE state and is turned off, the LOAD-OTP bit [bit 6 in the DEVCONTROL register] forces a reload of the registers when the LOAD-OTP bit is set to 1b (default). When the LOAD-OTP bit is set to 0b, register content is not changed unless the supply voltage drops below the UVLO threshold. The I²C interface runs off of an internal oscillator that is automatically enabled when an access to the interface happens.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S mode, and it is referred to as HS mode. The TPS659128x device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

8.4.12.2.1 I²C Implementation

Two I²C interfaces are available on the TPS659128x device. One interface is for general purpose use and is referred to as the general-purpose or standard I²C interface. The other interface is exclusively used for voltage scaling on the DC-DC converters and is referred to as AVS- or power-I²C interface.

The TPS659128x device has a 7-bit address with the LSB factory programmable.

The device address for the STANDARD-I²C interface is typically set to 0101101b.

The device address for the AVS-I²C interface is typically set to 0010011b.

Other default addresses can be factory programmed.

8.4.12.2.2 F/S-Mode Protocol

The master device initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while the SCL pin is high (see Figure 8-19). All I²C-compatible devices should recognize a start condition.

The master device then generates the SCL pulses, and transmits the 7-bit address followed by the read-write direction (R/W bit) on the SDA line. During all transmissions, the master device ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 8-20). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 8-21) by pulling the SDA line low during the entire high period of the ninth SCL cycle. This acknowledge confirms to the master that the communication link with the slave has been established.

The master device generates further SCL cycles to either transmit data to the slave device (R/W bit set to 0b) or receive data from the slave device (R/W bit set to 1b). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master device or by the slave device, depending on which one is the receiver. Valid 9-bit data sequences consisting of 8-bit data and 1-bit acknowledge can continue for as long as necessary.

To signal the end of the data transfer, the master device generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 8-19). This process releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition.

Upon the receipt of a stop condition, the bus is released, and all slave devices wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in Register Descriptions results in a readout of FFh.

8.4.12.2.3 H/S-Mode Protocol

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup devices.

The master device generates a start condition followed by a valid serial byte containing the HS master code 00001XXX. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master device then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS mode and switches all the internal settings of the slave devices to support the F/S mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in HS mode.

Attempting to read data from register addresses not listed in Register Descriptions results in a readout of FFh.

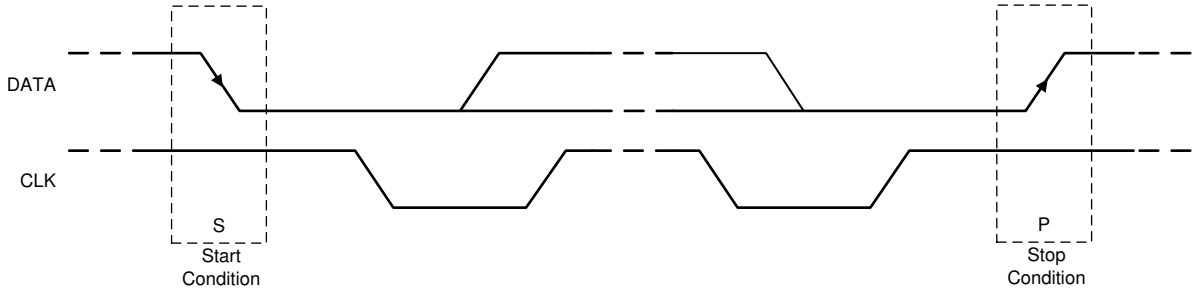


Figure 8-19. START and STOP Conditions

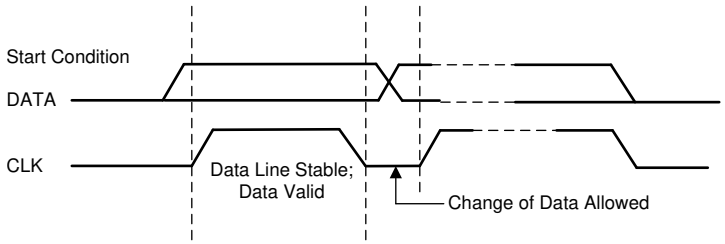


Figure 8-20. Bit Transfer on the Serial Interface

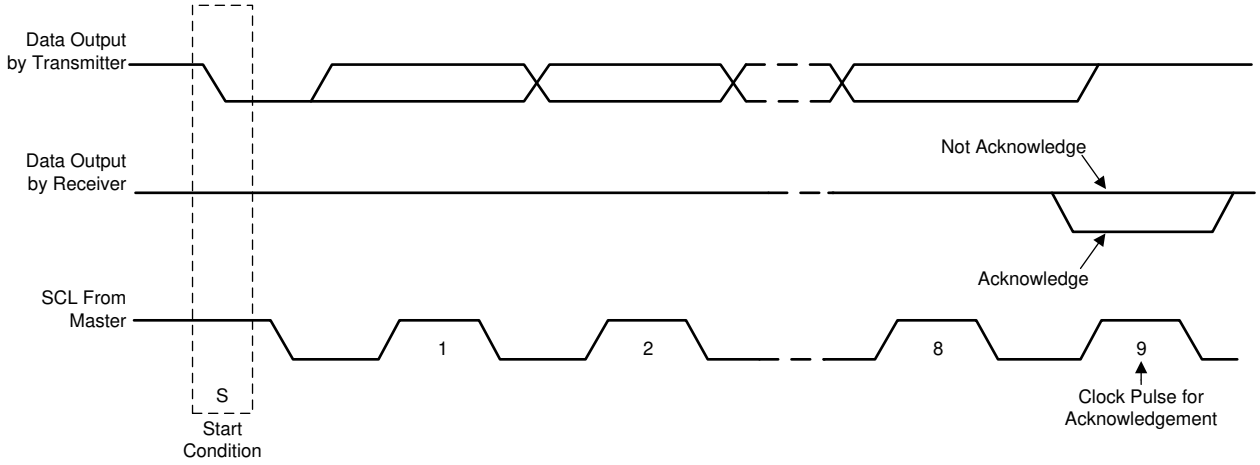


Figure 8-21. Acknowledge on the I²C Bus

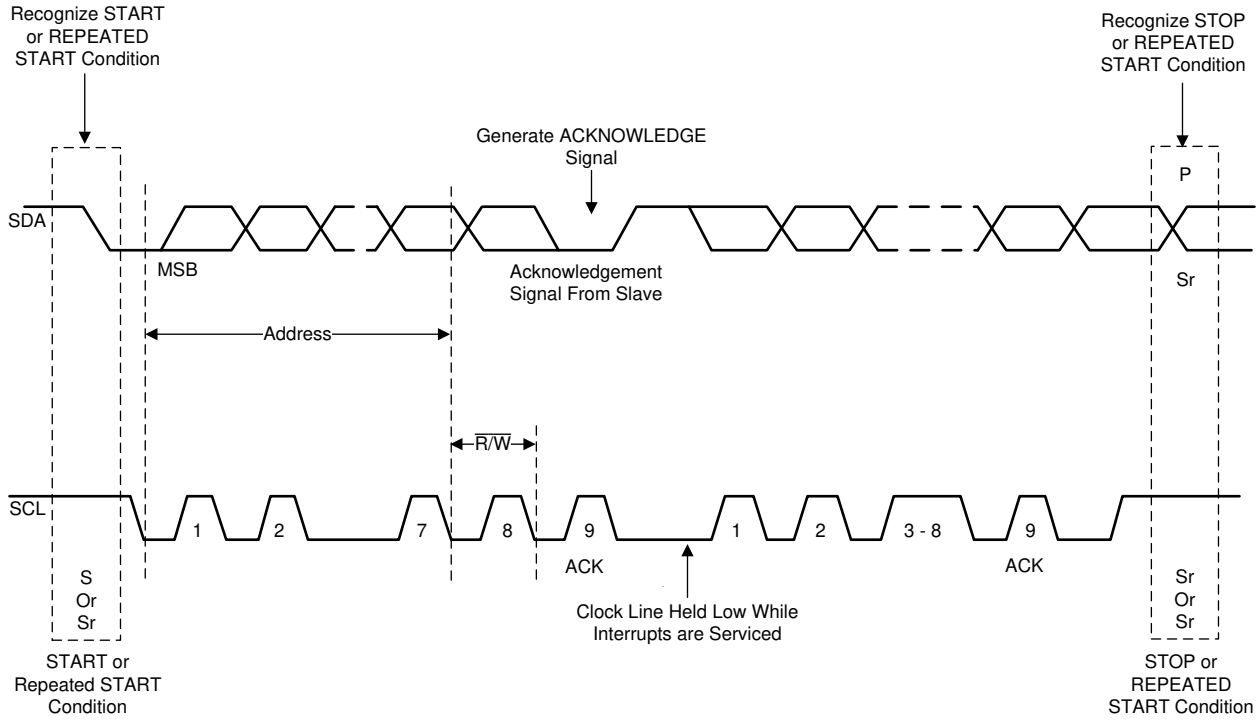
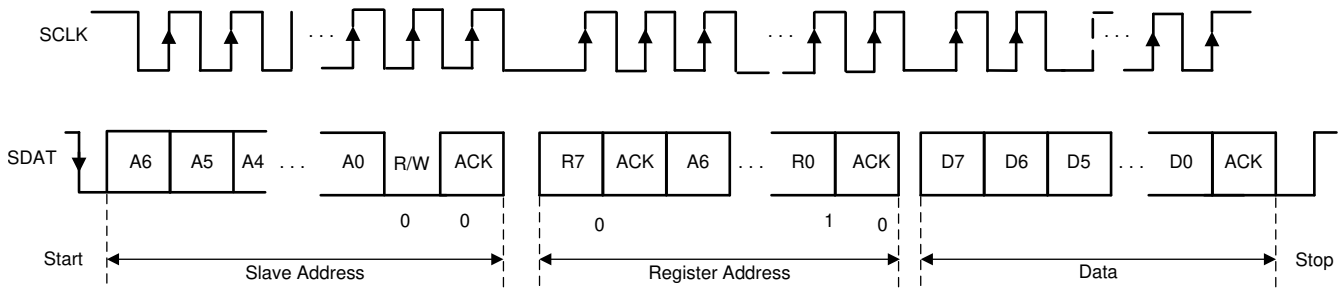
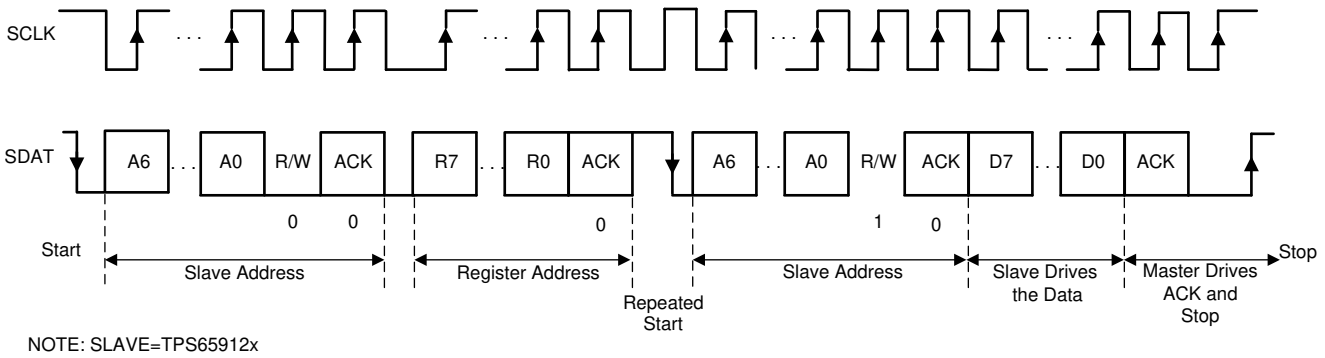


Figure 8-22. Bus Protocol



NOTE: SLAVE=TPS65912x

Figure 8-23. I²C Interface WRITE to TPS659128x; F/S Mode



NOTE: SLAVE=TPS65912x

Figure 8-24. I²C Interface READ from TPS659128x; F/S Mode

8.5 Register Maps

8.5.1 Register Descriptions

8.5.1.1 DCDC Registers (00h to 0Fh)

Table 8-8 lists the memory-mapped registers for the DCDC registers. All register offset addresses not listed in Table 8-8 should be considered as reserved locations and the register contents should not be modified.

Table 8-8. DCDC Registers

Offset	Acronym	Register Name	Section
00h	DCDC1_CTRL	DCDC1 Control Register	Section 8.5.1.1.1
01h	DCDC2_CTRL	DCDC2 Control Register	Section 8.5.1.1.2
02h	DCDC3_CTRL	DCDC3 Control Register	Section 8.5.1.1.3
03h	DCDC4_CTRL	DCDC4 Control Register	Section 8.5.1.1.4
04h	DCDC1_OP	DCDC1 OP Register	Section 8.5.1.1.5
05h	DCDC1_AVS	DCDC1 AVS Register	Section 8.5.1.1.6
06h	DCDC1_LIMIT	DCDC1 Limit Register	Section 8.5.1.1.7
07h	DCDC2_OP	DCDC2 OP Register	Section 8.5.1.1.8
08h	DCDC2_AVS	DCDC2 AVS Register	Section 8.5.1.1.9
09h	DCDC2_LIMIT	DCDC2 Limit Register	Section 8.5.1.1.10
0Ah	DCDC3_OP	DCDC3 OP Register	Section 8.5.1.1.11
0Bh	DCDC3_AVS	DCDC3 AVS Register	Section 8.5.1.1.12
0Ch	DCDC3_LIMIT	DCDC3 Limit Register	Section 8.5.1.1.13
0Dh	DCDC4_OP	DCDC4 OP Register	Section 8.5.1.1.14
0Eh	DCDC4_AVS	DCDC4 AVS Register	Section 8.5.1.1.15
0Fh	DCDC4_LIMIT	DCDC4 Limit Register	Section 8.5.1.1.16

Complex bit access types are encoded to fit into small table cells. Table 8-9 shows the codes that are used for access types in this section.

Table 8-9. DCDC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
-OTP		Bit reset value is defined in the OTP memory
-X		Bit determined by external connection

8.5.1.1.1 DCDC1_CTRL Register (Offset = 00h) [reset = OTP]

DCDC1_CTRL is shown in Table 8-10 and described in Table 8-11.

Return to Summary Table.

Register is reset on a POR event.

Table 8-10. DCDC1_CTRL Register

7	6	5	4	3	2	1	0
VCON_ENABLE	VCON_RANGE[1:0]		TSTEP[2]			DCDC1_MODE	RSVD
R/W-OTP	R/W-OTP		R/W-000b			R/W-OTP	R-0b

Table 8-11. DCDC1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCON_ENABLE	R/W	OTP	0b = Voltage scaling is done by the I^2C registers or DCDC1_SEL pin 1b = Voltage scaling is done by the VCON pins, VCON_PWM and VCON_CLK; the voltage table is automatically forced to RANGE[1:0] = 00b; register contents in voltage scaling registers are ignored
6-5	VCON_RANGE[1:0]	R/W	OTP	00b = Sets output voltage range for VCON operation: 500 mV to 1100 mV with 25 mV steps; 24 steps 01b = Sets output voltage range for VCON operation: 700 mV to 1100 mV with 12.5 mV steps; 32 steps 10b = Sets output voltage range for VCON operation: 600 mV to 1000 mV with 12.5 mV steps; 32 steps 11b = Sets output voltage range for VCON operation: 500 mV to 900 mV with 12.5 mV steps; 32 steps
4-2	TSTEP[2:0]	R/W	000b	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). Table 8-18 shows the equivalent programmable slew rate of the output voltage.
1	DCDC1_MODE	R/W	OTP	0b = Auto mode or Eco mode 1b = Force PWM mode
0	RSVD	R	0b	Unused bit, should be written to 0b.

8.5.1.1.2 DCDC2_CTRL (Offset = 01h) [reset = OTP]

DCDC2_CTRL is shown in Table 8-12 and described in Table 8-13.

Return to Summary Table.

Register is reset on a POR event.

Table 8-12. DCDC2_CTRL Register

7	6	5	4	3	2	1	0
RSVD			TSTEP[2:0]			DCDC2_MODE	RSVD
R-000b			R/W-000b			R/W-1b	R-0b

Table 8-13. DCDC2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit, should be written to 0b.
4-2	TSTEP[2:0]	R/W	000b	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). Table 8-18 shows the equivalent programmable slew rate of the output voltage.
1	DCDC2_MODE	R/W	OTP	0b = Auto mode or Eco mode 1b = Force PWM
0	RSVD	R	0b	Unused bit, should be written to 0b.

8.5.1.1.3 DCDC3_CTRL Register (Offset = 02h) [reset = OTP]

DCDC3_CTRL is shown in Table 8-14 and described in Table 8-15.

Return to Summary Table.

Register is reset on a POR event.

Table 8-14. DCDC3_CTRL Register

7	6	5	4	3	2	1	0
RSVD			TSTEP[2:0]			DCDC3_MODE	RSVD
R/W-000b			R/W-000b			R/W-OTP	R-0b

Table 8-15. DCDC3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R/W	000b	Unused bit, should be written to 0b.
4-2	TSTEP[2:0]	R/W	000b	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). Table 8-18 shows the equivalent programmable slew rate of the output voltage.
1	DCDC3_MODE	R/W	OTP	0b = Auto mode or Eco mode 1b = Force PWM
0	RSVD	R	0b	Unused bit, should be written to 0b.

8.5.1.1.4 DCDC4_CTRL Register (Offset = 03h) [reset = OTP]

DCDC4_CTRL is shown in Table 8-16 and described in Table 8-17.

Return to Summary Table.

Register is reset on a POR event.

Table 8-16. DCDC4_CTRL Register

7	6	5	4	3	2	1	0
RSVD			TSTEP[2:0]			DCDC4_MODE	RAMP_TIME
R-000b			R/W-000b			R/W-OTP	R/W-OTP

Table 8-17. DCDC4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit, should be written to 0b.
4-2	TSTEP[2:0]	R/W	000b	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). Table 8-18 shows the equivalent programmable slew rate of the output voltage.
1	DCDC4_MODE	R/W	OTP	0b = Auto mode or Eco mode 1b = Force PWM
0	RAMP_TIME	R/W	OTP	For additional options for DCDC4, see the SPARE register (address 63h). 0b = Ramp time for initial start up is 200-µs minimum 1b = Ramp time for initial start up is 60-µs maximum

Table 8-18. DCDCx TSTEP Settings

TSTEP[2:0]	Slew Rate (mV/µs)
000b	30
001b	12.5
010b	9.4
011b	7.5
100b	6.25
101b	4.7
110b	3.12
111b	2.5

8.5.1.1.5 DCDC1_OP Register (Offset = 04h) [reset = OTP]

DCDC1_OP is shown in Table 8-19 and described in Table 8-20.

Return to Summary Table.

Register is reset on a POR event.

Table 8-19. DCDC1_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-20. DCDC1_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b.
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	DCDC1 output voltage selection based on the RANGE[1:0] bit in the DCDC1 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.6 DCDC1_AVS Register (Offset = 05h) [reset = OTP]

DCDC1_AVS is shown in Table 8-21 and described in Table 8-22.

Return to Summary Table.

Register is reset on a POR event.

Table 8-21. DCDC1_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-22. DCDC1_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = DCDC1 disabled 1b = DCDC1 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.4.4.2
5-0	SEL[5:0]	R/W	OTP	DCDC1 output voltage selection based on the RANGE[1:0] bit in the DCDC1 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.7 DCDC1_LIMIT Register (Offset = 06h) [reset = OTP]

DCDC1_LIMIT is shown in Table 8-23 and described in Table 8-24.

Return to Summary Table.

Register is reset on a POR event.

Table 8-23. DCDC1_LIMIT Register

7	6	5	4	3	2	1	0
RANGE[1:0]		MAX_SEL[5:0]					
R/W-OTP		R/W-OTP					

Table 8-24. DCDC1_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE[1:0]	R/W	OTP	Selects the output range. For more information, see Table 8-43.
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the DCDC1_AVS or DCDC1_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.1.8 DCDC2_OP Register (Offset = 07h) [reset = OTP]

DCDC2_OP is shown in Table 8-25 and described in Table 8-26.

Return to Summary Table.

Register is reset on a POR event.

Table 8-25. DCDC2_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-26. DCDC2_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b.
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	DCDC2 output voltage selection based on the RANGE[1:0] bit in the DCDC2 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.9 DCDC2_AVS Register (Offset = 08h) [reset = OTP]

DCDC2_AVS is shown in Table 8-27 and described in Table 8-28.

Return to Summary Table.

Register is reset on a POR event.

Table 8-27. DCDC2_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-28. DCDC2_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = DCDC2 disabled 1b = DCDC2 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.4.4.2
5-0	SEL[5:0]	R/W	OTP	DCDC2 output voltage selection based on the RANGE[1:0] bit in the DCDC2 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.10 DCDC2_LIMIT Register (Offset = 09h) [reset = OTP]

DCDC2_LIMIT is shown in Table 8-29 and described in Table 8-30.

Return to Summary Table.

Register is reset on a POR event.

Table 8-29. DCDC2_LIMIT Register

7	6	5	4	3	2	1	0
RANGE[1:0]		MAX_SEL[5:0]					
R/W-OTP		R/W-OTP					

Table 8-30. DCDC2_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RANGE[1:0]	R/W	OTP	Selects the output range. For more information, see Table 8-43.
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the DCDC2_AVS or DCDC2_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.1.11 DCDC3_OP Register (Offset = 0Ah) [reset = OTP]

DCDC3_OP is shown in Table 8-31 and described in Table 8-32.

Return to Summary Table.

Register is reset on a POR event.

Table 8-31. DCDC3_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-32. DCDC3_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b.
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	DCDC3 output voltage selection based on the RANGE[1:0] bit in the DCDC3 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.12 DCDC3_AVS Register (Offset = 0Bh) [reset = OTP]

DCDC3_AVS is shown in Table 8-33 and described in Table 8-34.

Return to Summary Table.

Register is reset on a POR event.

Table 8-33. DCDC3_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-34. DCDC3_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = DCDC3 disabled 1b = DCDC3 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.4.4.2
5-0	SEL[5:0]	R/W	OTP	DCDC3 output voltage selection based on the RANGE[1:0] bit in the DCDC3 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.13 DCDC3_LIMIT Register (Offset = 0Ch) [reset = OTP]

DCDC3_LIMIT is shown in Table 8-35 and described in Table 8-36.

Return to Summary Table.

Register is reset on a POR event.

Table 8-35. DCDC3_LIMIT Register

7	6	5	4	3	2	1	0
RANGE[1:0]		MAX_SEL[5:0]					
R/W-OTP		R/W-OTP					

Table 8-36. DCDC3_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RANGE[1:0]	R/W	OTP	Selects the output range. For more information, see Table 8-43.
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the DCDC3_AVS or DCDC3_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.1.14 DCDC4_OP Register (Offset = 0Dh) [reset = OTP]

DCDC4_OP is shown in Table 8-37 and described in Table 8-38.

Return to Summary Table.

Register is reset on a POR event.

Table 8-37. DCDC4_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-38. DCDC4_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b.
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	This bit is for the DCDC4 output voltage selection based on the RANGE[1:0] bit in the DCDC4 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.15 DCDC4_AVS Register (Offset = 0Eh) [reset = OTP]

DCDC4_AVS is shown in Table 8-39 and described in Table 8-40.

Return to Summary Table.

Register is reset on a POR event.

Table 8-39. DCDC4_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-40. DCDC4_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = DCDC4 disabled 1b = DCDC4 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.4.4.2
5-0	SEL[5:0]	R/W	OTP	This bit is for the DCDC4 output voltage selection based on the RANGE[1:0] bit in the DCDC4 register selections shown in Table 8-44 through Table 8-47.

8.5.1.1.16 DCDC4_LIMIT Register (Offset = 0Fh) [reset = OTP]

DCDC4_LIMIT is shown in Table 8-41 and described in Table 8-42.

Return to Summary Table.

Register is reset on a POR event.

Table 8-41. DCDC4_LIMIT Register

7	6	5	4	3	2	1	0
RANGE[1:0]		MAX_SEL[5:0]					
R/W-OTP		R/W-OTP					

Table 8-42. DCDC4_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RANGE[1:0]	R/W	OTP	Selects the output range. For more information, see Table 8-43.
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the DCDC4_AVS or DCDC4_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.1.17 V_{DCDCx} Range Settings

Table 8-43. V_{DCDCx} Range Settings

RANGE[1:0]	Output Voltage Range
00b	0.5 V to 1.2875 V in 12.5 mV steps (See Table 8-44)
01b	0.7 V to 1.4875 V in 12.5 mV steps (See Table 8-45)
10b	0.5 V to 2.075 V in 25 mV steps (See Table 8-46)
11b	0.5 V to 3.8 V in 50 mV steps (See Table 8-47)

8.5.1.1.18 DCDCx Voltage Settings

Table 8-44. DCDCx Voltage Settings (RANGE[1:0] = 00b)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000b	0.5000	100000b	0.9000
000001b	0.5125	100001b	0.9125
000010b	0.5250	100010b	0.9250
000011b	0.5375	100011b	0.9375
000100b	0.5500	100100b	0.9500
000101b	0.5625	100101b	0.9625
000110bb	0.5750	100110b	0.9750
000111b	0.5875	100111b	0.9875
001000b	0.6000	101000b	1.0000
001001b	0.6125	101001b	1.0125
001010b	0.6250	101010b	1.025
001011b	0.6375	101011b	1.0375
001100b	0.6500	101100b	1.0500
001101b	0.6625	101101b	1.0625
001110b	0.6750	101110b	1.0750
001111b	0.6875	101111b	1.0875
010000b	0.7000	110000b	1.1000
010001b	0.7125	110001b	1.1125
010010b	0.725	110010b	1.1250
010011b	0.7375	110011b	1.1375
010100b	0.7500	110100b	1.1500
010101b	0.7625	110101b	1.1625
010110b	0.7750	110110b	1.1750
010111b	0.7875	110111b	1.1875
011000b	0.8000	111000b	1.2000
011001b	0.8125	111001b	1.2125
011010b	0.8250	111010b	1.2250
011011b	0.8375	111011b	1.2375
011100b	0.8500	111100b	1.2500
011101b	0.8625	111101b	1.2625
011110b	0.8750	111110b	1.2750
011111b	0.8875	111111b	1.2875

Table 8-45. DCDCx Voltage Settings (RANGE[1:0] = 01b)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000b	0.7000	100000b	1.1000
000001b	0.7125	100001b	1.1125
000010b	0.7250	100010b	1.1250
000011b	0.7375	100011b	1.1375
000100b	0.7500	100100b	1.1500
000101b	0.7625	100101b	1.1625
000110b	0.7750	100110b	1.1750
000111b	0.7875	100111b	1.1875
001000b	0.8000	101000b	1.2000
001001b	0.8125	101001b	1.2125
001010b	0.8250	101010b	1.225
001011b	0.8375	101011b	1.2375
001100b	0.8500	101100b	1.2500
001101b	0.8625	101101b	1.2625
001110b	0.8750	101110b	1.2750
001111b	0.8875	101111b	1.2875
010000b	0.9000	110000b	1.3000
010001b	0.9125	110001b	1.3125
010010b	0.925	110010b	1.3250
010011b	0.9375	110011b	1.3375
010100b	0.9500	110100b	1.3500
010101b	0.9625	110101b	1.3625
010110b	0.9750	110110b	1.3750
010111b	0.9875	110111b	1.3875
011000b	1.0000	111000b	1.4000
011001b	1.0125	111001b	1.4125
011010b	1.0250	111010b	1.4250
011011b	1.0375	111011b	1.4375
011100b	1.0500	111100b	1.4500
011101b	1.0625	111101b	1.4625
011110b	1.0750	111110b	1.4750
011111b	1.0875	111111b	1.4875

Table 8-46. DCDCx Voltage Settings (RANGE[1:0] = 10b)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000b	0.500	100000b	1.300
000001b	0.525	100001b	1.325
000010b	0.550	100010b	1.350
000011b	0.575	100011b	1.375
000100b	0.600	100100b	1.400
000101b	0.625	100101b	1.425
000110b	0.650	100110b	1.450
000111b	0.675	100111b	1.475
001000b	0.700	101000b	1.500
001001b	0.725	101001b	1.525
001010b	0.750	101010b	1.550
001011b	0.775	101011b	1.575
001100b	0.800	101100b	1.600
001101b	0.825	101101b	1.625
001110b	0.850	101110b	1.650
001111b	0.875	101111b	1.675
010000b	0.900	110000b	1.700
010001b	0.925	110001b	1.725
010010b	0.950	110010b	1.750
010011b	0.975	110011b	1.775
010100b	1.000	110100b	1.800
010101b	1.025	110101b	1.825
010110b	1.050	110110b	1.850
010111b	1.075	110111b	1.875
011000b	1.100	111000b	1.900
011001b	1.125	111001b	1.925
011010b	1.150	111010b	1.950
011011b	1.175	111011b	1.975
011100b	1.200	111100b	2.000
011101b	1.225	111101b	2.025
011110b	1.250	111110b	2.050
011111b	1.275	111111b	2.075

Table 8-47. DCDCx Voltage Settings (RANGE[1:0] = 11b)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000b	0.50	100000b	2.10
000001b	0.55	100001b	2.15
000010b	0.60	100010b	2.20
000011b	0.65	100011b	2.25
000100b	0.70	100100b	2.30
000101b	0.75	100101b	2.35
000110b	0.80	100110b	2.40
000111b	0.85	100111b	2.45
001000b	0.90	101000b	2.50
001001b	0.95	101001b	2.55
001010b	1.00	101010b	2.60
001011b	1.05	101011b	2.65
001100b	1.10	101100b	2.70
001101b	1.15	101101b	2.75
001110b	1.20	101110b	2.80
001111b	1.25	101111b	2.85
010000b	1.30	110000b	2.90
010001b	1.35	110001b	2.95
010010b	1.40	110010b	3.00
010011b	1.45	110011b	3.05
010100b	1.50	110100b	3.10
010101b	1.55	110101b	3.15
010110b	1.60	110110b	3.20
010111b	1.65	110111b	3.25
011000b	1.70	111000b	3.30
011001b	1.75	111001b	3.35
011010b	1.80	111010b	3.40
011011b	1.85	111011b	3.45
011100b	1.90	111100b	3.50
011101b	1.95	111101b	3.55
011110b	2.00	111110b	3.60
011111b	2.05	111111b	3.80

8.5.1.2 LDO Registers (10h to 21h)

Table 8-48 lists the memory-mapped registers for the LDO registers. All register offset addresses not listed in Table 8-48 should be considered as reserved locations and the register contents should not be modified.

Table 8-48. LDO Register Memory Map

Offset	Acronym	Register Name	Section
10h	LDO1_OP	LDO1 OP Register	Section 8.5.1.2.1
11h	LDO1_AVS	LDO1 AVS Register	Section 8.5.1.2.2
12h	LDO1_LIMIT	LDO1 Limit Register	Section 8.5.1.2.3
13h	LDO2_OP	LDO2 OP Register	Section 8.5.1.2.4
14h	LDO2_AVS	LDO2 AVS Register	Section 8.5.1.2.5
15h	LDO2_LIMIT	LDO2 Limit Register	Section 8.5.1.2.6
16h	LDO3_OP	LDO3 OP Register	Section 8.5.1.2.7
17h	LDO3_AVS	LDO3 AVS Register	Section 8.5.1.2.8
18h	LDO3_LIMIT	LDO3 Limit Register	Section 8.5.1.2.9
19h	LDO4_OP	LDO4 OP Register	Section 8.5.1.2.10
1Ah	LDO4_AVS	LDO4 AVS Register	Section 8.5.1.2.11
1Bh	LDO4_LIMIT	LDO4 Limit Register	Section 8.5.1.2.12
1Ch	LDO5	LDO5 Register	Section 8.5.1.2.13
1Dh	LDO6	LDO6 Register	Section 8.5.1.2.14
1Eh	LDO7	LDO7 Register	Section 8.5.1.2.15
1Fh	LDO8	LDO8 Register	Section 8.5.1.2.16
20h	LDO9	LDO9 Register	Section 8.5.1.2.17
21h	LDO10	LDO10 Register	Section 8.5.1.2.18

Complex bit access types are encoded to fit into small table cells. Table 8-49 shows the codes that are used for access types in this section.

Table 8-49. LDO Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
-OTP		Bit reset value is defined in the OTP memory
-X		Bit determined by external connection

8.5.1.2.1 LDO1_OP Register (Offset = 10h) [reset = OTP]

LDO1_OP is shown in Table 8-50 and described in Table 8-51.

Return to Summary Table.

Register is reset on a POR event.

Table 8-50. LDO1_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-51. LDO1_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage settings.

8.5.1.2.2 LDO1_AVS Register (Offset = 11h) [reset = OTP]

LDO1_AVS is shown in Table 8-52 and described in Table 8-53.

Return to Summary Table.

Register is reset on a POR event.

Table 8-52. LDO1_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-53. LDO1_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO1 disabled 1b = LDO1 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.3 LDO1_LIMIT Register (Offset = 12h) [reset = OTP]

LDO1_LIMIT is shown in Figure 8-25 and described in Table 8-54.

Return to Summary Table.

Register is reset on a POR event.

Figure 8-25. LDO1_LIMIT Register

7	6	5	4	3	2	1	0
RSVD		MAX_SEL[5:0]					
R-00b		R/W-OTP					

Table 8-54. LDO1_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit, should be written to 0b
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the LDO1_AVS or LDO1_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.2.4 LDO2_OP Register (Offset = 13h) [reset = OTP]

LDO2_OP is shown in Table 8-55 and described in Table 8-56.

Return to Summary Table.

Register is reset on a POR event.

Table 8-55. LDO2_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-56. LDO2_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.5 LDO2_AVS Register (Offset = 14h) [reset = OTP]

LDO2_AVS is shown in Table 8-57 and described in Table 8-58.

Return to Summary Table.

Register is reset on a POR event.

Table 8-57. LDO2_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-58. LDO2_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO2 disabled 1b = LDO2 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.6 LDO2_LIMIT Register (Offset = 15h) [reset = OTP]

LDO2_LIMIT is shown in Table 8-59 and described in Table 8-60.

Return to Summary Table.

Register is reset on a POR event.

Table 8-59. LDO2_LIMIT Register

7	6	5	4	3	2	1	0
RSVD		MAX_SEL[5:0]					
R-00b		R/W-OTP					

Table 8-60. LDO2_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit, should be written to 0b
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the LDO2_AVS or LDO2_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.2.7 LDO3_OP Register (Offset = 16h) [reset = OTP]

LDO3_OP is shown in Table 8-61 and described in Table 8-62.

Return to Summary Table.

Register is reset on a POR event.

Table 8-61. LDO3_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-62. LDO3_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.8 LDO3_AVS Register (Offset = 17h) [reset = OTP]

LDO3_AVS is shown in Table 8-63 and described in Table 8-64.

Return to Summary Table.

Register is reset on a POR event.

Table 8-63. LDO3_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-64. LDO3_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO3 disabled 1b = LDO3 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.9 LDO3_LIMIT Register (Offset = 18h) [reset = OTP]

LDO3_LIMIT is shown in Table 8-65 and described in Table 8-66.

Return to Summary Table.

Register is reset on a POR event.

Table 8-65. LDO3_LIMIT Register

7	6	5	4	3	2	1	0
RSVD		MAX_SEL[5:0]					
R-00b		R/W-OTP					

Table 8-66. LDO3_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit, should be written to 0b
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the LDO3_AVS or LDO3_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.2.10 LDO4_OP Register (Offset = 19h) [reset = OTP]

LDO4_OP is shown in Table 8-67 and described in Table 8-68.

Return to Summary Table.

Register is reset on a POR event.

Table 8-67. LDO4_OP Register

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5:0]					
R-0b	R/W-0b	R/W-OTP					

Table 8-68. LDO4_OP Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit, should be written to 0b
6	SELREG	R/W	0b	See Table 8-6
5-0	SEL[5:0]	R/W	OTP	Table 8-86 shows the supply-voltage setting. The SEL[5] bit is internally set to 1b on LDO4 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

8.5.1.2.11 LDO4_AVS Register (Offset = 1Ah) [reset = OTP]

LDO4_AVS is shown in Table 8-69 and described in Table 8-70.

Return to Summary Table.

Register is reset on a POR event.

Table 8-69. LDO4_AVS Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-70. LDO4_AVS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO4 disabled 1b = LDO4 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-86 shows the supply-voltage setting. The SEL[5] bit is internally set to 1b on LDO4 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

8.5.1.2.12 LDO4_LIMIT Register (Offset = 1Bh) [reset = OTP]

LDO4_LIMIT is shown in Table 8-71 and described in Table 8-72.

Return to Summary Table.

Register is reset on a POR event.

Table 8-71. LDO4_LIMIT Register

7	6	5	4	3	2	1	0
RSVD		MAX_SEL[5:0]					
R-00b		R/W-OTP					

Table 8-72. LDO4_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit, should be written to 0b
5-0	MAX_SEL[5:0]	R/W	OTP	This bit defines the maximum value the output voltage in the LDO4_AVS or LDO4_OP register can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If the MAX_SEL bit is set by I^2C or default OTP setting to any value other than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked until OTP is reloaded.

8.5.1.2.13 LDO5 Register (Offset = 1Ch) [reset = OTP]

LDO5 is shown in Table 8-73 and described in Table 8-74.

Return to Summary Table.

Register is reset on a POR event.

Table 8-73. LDO5 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-74. LDO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO5 disabled 1b = LDO5 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-86 shows the supply-voltage setting. The SEL[5] bit is internally set to 1b on LDO5 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

8.5.1.2.14 LDO6 Register (Offset = 1Dh) [reset = OTP]

LDO6 is shown in Table 8-75 and described in Table 8-76.

Return to Summary Table.

Register is reset on a POR event.

Table 8-75. LDO6 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-76. LDO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO6 disabled 1b = LDO6 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.15 LDO7 Register (Offset = 1Eh) [reset = OTP]

LDO7 is shown in Table 8-77 and described in Table 8-78.

Return to Summary Table.

Register is reset on a POR event.

Table 8-77. LDO7 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-78. LDO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO7 disabled 1b = LDO7 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.16 LDO8 Register (Offset = 1Fh) [reset = OTP]

LDO8 is shown in Table 8-79 and described in Table 8-80.

Return to Summary Table.

Register is reset on a POR event.

Table 8-79. LDO8 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-80. LDO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO8 disabled 1b = LDO8 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.17 LDO9 Register (Offset = 20h) [reset = OTP]

LDO9 is shown in Table 8-81 and described in Table 8-82.

Return to Summary Table.

Register is reset on a POR event.

Table 8-81. LDO9 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-82. LDO9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO9 disabled 1b = LDO9 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.18 LDO10 Register (Offset = 21h) [reset = OTP]

LDO10 is shown in Table 8-83 and described in Table 8-84.

Return to Summary Table.

Register is reset on a POR event.

Table 8-83. LDO10 Register

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5:0]					
R/W-OTP	R/W-0b	R/W-OTP					

Table 8-84. LDO10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	OTP	0b = LDO10 disabled 1b = LDO10 enabled unless it is being disabled by SET_OFF mode
6	ECO	R/W	0b	See Section 8.3.1.1
5-0	SEL[5:0]	R/W	OTP	Table 8-85 shows the supply-voltage setting.

8.5.1.2.19 LDO Voltage Settings

Table 8-85. LDO Voltage Settings; Except LDO4 and LDO5

SEL[5:0]	LDOx Output (V)	SEL[5:0]	LDOx Output (V)
000000b	0.800	100000b	1.600
000001b	0.825	100001b	1.650
000010b	0.850	100010b	1.700
000011b	0.875	100011b	1.750
000100b	0.900	100100b	1.800
000101b	0.925	100101b	1.850
000110b	0.950	100110b	1.900
000111b	0.975	100111b	1.950
001000b	1.000	101000b	2.000
001001b	1.025	101001b	2.050
001010b	1.050	101010b	2.100
001011b	1.075	101011b	2.150
001100b	1.100	101100b	2.200
001101b	1.125	101101b	2.250
001110b	1.150	101110b	2.300
001111b	1.175	101111b	2.350
010000b	1.200	110000b	2.400
010001b	1.225	110001b	2.450
010010b	1.250	110010b	2.500
010011b	1.275	110011b	2.550
010100b	1.300	110100b	2.600
010101b	1.325	110101b	2.650
010110b	1.350	110110b	2.700
010111b	1.375	110111b	2.750
011000b	1.400	111000b	2.800
011001b	1.425	111001b	2.850
011010b	1.450	111010b	2.900
011011b	1.475	111011b	2.950
011100b	1.500	111100b	3.000
011101b	1.525	111101b	3.100
011110b	1.550	111110b	3.200
011111b	1.575	111111b	3.300

Table 8-86. LDO Voltage Settings for LDO4 and LDO5

SEL[5:0]	LDOx Output (V)
100000b	1.600
100001b	1.650
100010b	1.700
100011b	1.750
100100b	1.800
100101b	1.850
100110b	1.900
100111b	1.950
101000b	2.000
101001b	2.050
101010b	2.100
101011b	2.150
101100b	2.200
101101b	2.250
101110b	2.300
101111b	2.350
110000b	2.400
110001b	2.450
110010b	2.500
110011b	2.550
110100b	2.600
110101b	2.650
110110b	2.700
110111b	2.750
111000b	2.800
111001b	2.850
111010b	2.900
111011b	2.950
111100b	3.000
111101b	3.100
111110b	3.200
111111b	3.300

8.5.1.3 DEVCTRL Registers (22h to 64h)

Table 8-87 lists the memory-mapped registers for the DEVCTRL registers. All register offset addresses not listed in Table 8-87 should be considered as reserved locations and the register contents should not be modified.

Table 8-87. DEVCTRL Register Memory Map

Offset	Acronym	Register Name	Section
22h	THRM_REG	Thermal Register	Section 8.5.1.3.1
23h	CLK32KOUT	32-kHz Clock Output Register	Section 8.5.1.3.2
24h	DEVCTRL	Device Control Register	Section 8.5.1.3.3
25h	DEVCTRL2	Device Control 2 Register	Section 8.5.1.3.4
26h	I2C_SPI_CFG	I²C-SPI Configuration Register	Section 8.5.1.3.5
27h	KEEP_ON1	LDO Keep-On Register	Section 8.5.1.3.6
28h	KEEP_ON2	DCDC Keep-On Register	Section 8.5.1.3.7
29h	SET_OFF1	LDO Set Off Register	Section 8.5.1.3.8
2Ah	SET_OFF2	DCDC Set Off Register	Section 8.5.1.3.9
(2Bh)	DEF_VOLT	Default Voltage Register	Section 8.5.1.3.10
2Ch	DEF_VOLT_MAPPING	Default Voltage Mapping Register	Section 8.5.1.3.12
2Dh	DISCHARGE1	LDO Discharge Register	Section 8.5.1.3.13
2Eh	DISCHARGE2	DCDC Discharge Register	Section 8.5.1.3.14
2Fh	EN1_SET1	LDO EN1 Pin Setting Register	Section 8.5.1.3.15
30h	EN1_SET2	DCDC EN1 Pin Setting Register	Section 8.5.1.3.16
31h	EN2_SET1	LDO EN2 Pin Setting Register	Section 8.5.1.3.17
32h	EN2_SET2	DCDC EN2 Pin Setting Register	Section 8.5.1.3.18
33h	EN3_SET1	LDO EN3 Pin Setting Register	Section 8.5.1.3.19
34h	EN3_SET2	DCDC EN3 Pin Setting Register	Section 8.5.1.3.20
35h	EN4_SET1	LDO EN4 Pin Setting Register	Section 8.5.1.3.21
36h	EN4_SET2	DCDC EN4 Pin Setting Register	Section 8.5.1.3.22
37h	PGOOD	Power Good Register	Section 8.5.1.3.23
38h	PGOOD2	Power Good 2 Register	Section 8.5.1.3.24
39h	INT_STS	Interrupt Mask Register	Section 8.5.1.3.25
3Ah	INT_MSK	Interrupt Status Register	Section 8.5.1.3.26
3Bh	INT_STS2	Interrupt Status 2 Register	Section 8.5.1.3.27
3Ch	INT_MSK2	Interrupt Mask 2 Register	Section 8.5.1.3.28
3Dh	INT_STS3	Interrupt Status 3 Register	Section 8.5.1.3.29
3Eh	INT_MSK3	Interrupt Mask 3 Register	Section 8.5.1.3.30
3Fh	INT_STS4	Interrupt Status 4 Register	Section 8.5.1.3.31
40h	INT_MSK4	Interrupt Mask 4 Register	Section 8.5.1.3.32
41h	GPIO1	GPIO1 Register	Section 8.5.1.3.33
42h	GPIO2	GPIO2 Register	Section 8.5.1.3.34
43h	GPIO3	GPIO3 Register	Section 8.5.1.3.35
44h	GPIO4	GPIO4 Register	Section 8.5.1.3.36
45h	GPIO5	GPIO5 Register	Section 8.5.1.3.37
46h	VMON	Voltage Monitor Register	Section 8.5.1.3.38
47h	LEDA_CTRL1	LEDA Control 1 Register	Section 8.5.1.3.39
48h	LEDA_CTRL2	LEDA Control 2 Register	Section 8.5.1.3.40
49h	LEDA_CTRL3	LEDA Control 3 Register	Section 8.5.1.3.41
4Ah	LEDA_CTRL4	LEDA Control 4 Register	Section 8.5.1.3.42
4Bh	LEDA_CTRL5	LEDA Control 5 Register	Section 8.5.1.3.43

Table 8-87. DEVCTRL Register Memory Map (continued)

Offset	Acronym	Register Name	Section
4Ch	LEDA_CTRL6	LEDA Control 6 Register	Section 8.5.1.3.44
4Dh	LEDA_CTRL7	LEDA Control 7 Register	Section 8.5.1.3.45
4Eh	LEDA_CTRL8	LEDA Control 8 Register	Section 8.5.1.3.46
4Fh	LEDB_CTRL1	LEDB Control 1 Register	Section 8.5.1.3.47
50h	LEDB_CTRL2	LEDB Control 2 Register	Section 8.5.1.3.48
51h	LEDB_CTRL3	LEDB Control 3 Register	Section 8.5.1.3.49
52h	LEDB_CTRL4	LEDB Control 4 Register	Section 8.5.1.3.50
53h	LEDB_CTRL5	LEDB Control 5 Register	Section 8.5.1.3.51
54h	LEDB_CTRL6	LEDB Control 6 Register	Section 8.5.1.3.52
55h	LEDB_CTRL7	LEDB Control 7 Register	Section 8.5.1.3.53
56h	LEDB_CTRL8	LEDB Control 8 Register	Section 8.5.1.3.54
57h	LEDC_CTRL1	LEDC Control 1 Register	Section 8.5.1.3.55
58h	LEDC_CTRL2	LEDC Control 2 Register	Section 8.5.1.3.56
59h	LEDC_CTRL3	LEDC Control 3 Register	Section 8.5.1.3.57
5Ah	LEDC_CTRL4	LEDC Control 4 Register	Section 8.5.1.3.58
5Bh	LEDC_CTRL5	LEDC Control 5 Register	Section 8.5.1.3.59
5Ch	LEDC_CTRL6	LEDC Control 6 Register	Section 8.5.1.3.60
5Dh	LEDC_CTRL7	LEDC Control 7 Register	Section 8.5.1.3.61
5Eh	LEDC_CTRL8	LEDC Control 8 Register	Section 8.5.1.3.62
5Fh	LED_RAMP_UP_TIME	LED Ramp-Up Time Register	Section 8.5.1.3.63
60h	LED_RAMP_DOWN_TIME	LED Ramp-Down Time Register	Section 8.5.1.3.64
61h	LED_SEQ_EN	LED Sequence Enable Register	Section 8.5.1.3.65
62h	LOADSWITCH	Load Switch Register	Section 8.5.1.3.67
63h	SPARE	Spare Register	Section 8.5.1.3.68
64h	VERNUM	Version Number Register	Section 8.5.1.3.69

Complex bit access types are encoded to fit into small table cells. Table 8-88 shows the codes that are used for access types in this section.

Table 8-88. DEVCTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
-OTP		Bit reset value is defined in the OTP memory
-X		Bit determined by external connection

8.5.1.3.1 THRM_REG Register (Offset = 22h) [reset = 0Dh]

THRM_REG is shown in Table 8-89 and described in Table 8-90.

Return to Summary Table.

Register is reset on a POR event.

Table 8-89. THRM_REG Register

7	6	5	4	3	2	1	0
RSVD		THERM_HD	THERM_TS	THERM_HDSEL[1:0]		RSVD	THERM_EN
R-00b		R-0b	R-0b	R/W-11b		R-0b	R/W-1b

Table 8-90. THRM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	THERM_HD	R	0b	0b = Hot die threshold is not reached 1b = Hot die threshold is reached
4	THERM_TS	R	0b	Thermal shutdown detector output 0b = Indicates thermal shutdown not reached (typically 150°C) 1b = Indicates thermal shutdown reached
3-2	THERM_HDSEL	R/W	11b	Temperature selection for hot die detector 00b = T = 117°C 01b = T = 121°C 10b = T = 125°C 11b = T = 130°C
1	RSVD	R	0b	Unused bit
0	THERM_EN	R/W	1b	Thermal shutdown module 0b = Disabled 1b = Enabled

8.5.1.3.2 CLK32KOUT Register (Offset = 23h) [reset = OTP]

CLK32KOUT is shown in Table 8-91 and described in Table 8-92.

Return to Summary Table.

Register is reset on a POR event.

Table 8-91. CLK32KOUT Register

7	6	5	4	3	2	1	0
RSVD							CLK32KOUT_EN
R-0000000b							R/W-OTP

Table 8-92. CLK32KOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RSVD	R	0000000b	Unused bit read returns 0b.
0	CLK32KOUT_EN	R/W	OTP	0b = 32KCLKOUT disabled 1b = 32KCLKOUT enabled

8.5.1.3.3 DEVCTRL Register (Offset = 24h) [reset = OTP]

DEVCTRL is shown in Table 8-93 and described in Table 8-94.

Return to Summary Table.

Register is reset on a POR event.

Table 8-93. DEVCTRL Register

7	6	5	4	3	2	1	0
PWR_OFF_SEQ	LOAD-OTP	LOCK_LDO9	RSVD	nRESPWRON_OUTPUT	PWRHLD	DEV_SLP	DEV_OFF
R/W-OTP	R/W-OTP	R-OTP	R-0b	R/W-OTP	R/W-OTP	R/W-0b	R/W-0b

Table 8-94. DEVCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWR_OFF_SEQ	R/W	OTP	0b = All resources disabled at the same time 1b = Power-off will be sequential, reverse of power-on sequence (first resource to power on will be the last to power off)
6	LOAD-OTP	R/W	OTP	0b = Register contents are kept in the OFF state 1b = Register default values are reloaded from OTP when in the OFF state
5	LOCK_LDO9	R	OTP	0b = LDO9 bits are allowed to be changed 1b = LDO9 bits are locked; LDO9 is enabled in the startup sequence and disabled in the OFF state; no further control allowed
4	RSVD	R	0b	Unused bit read returns 0b.
3	nRESPWRON_OUTPUT	R/W	OTP	0b = NRESPWRON output is open drain 1b = NRESPWRON output is push-pull to VDDIO
2	PWRHLD	R/W	OTP	0b = Cleared in the OFF state. 1b = Writing 1b will maintain the device on (ACTIVE or SLEEP device state) unless one of the power off events occur (DEV_OFF, long key press if not masked, or thermal shutdown).
1	DEV_SLP	R/W	0b	0b = This bit is cleared in the OFF state. 1b = Writing 1b will starts an ACTIVE-to-SLEEP transition as long as no unmasked interrupts are pending. If set to 1b, the device will require an unmasked interrupt to occur to perform SLEEP-to-ACTIVE transition or will need to transition to OFF to clear this bit.
0	DEV_OFF	R/W	0b	0b = This bit is cleared in the OFF state. 1b = Writing 1b will start an ACTIVE-to-OFF or SLEEP-to-OFF device state transition (switch-off event). This event has priority over PWRHLD bit and PWRHOLD pin. Device will restart if either is high once transition to OFF state is complete.

8.5.1.3.4 DEVCTRL2 Register (Offset = 25h) [reset = OTP]

DEVCTRL2 is shown in Table 8-95 and described in Table 8-96.

Return to Summary Table.

Register is reset on a POR event.

Table 8-95. DEVCTRL2 Register

7	6	5	4	3	2	1	0
SLEEP_ENABLE	INT_OUTPUT	TSLOT_LENGTH[1:0]		SLEEP_POL	PWRON_LP_OFF	PWRON_LP_OFF_RST	INT_POL
R/W-0b	R/W-OTP	R/W-OTP		R/W-0b	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-96. DEVCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_ENABLE	R/W	0b	0b = SLEEP signal is ignored; default for power-up and should remain this way for CONFIG2 shorted to GND. 1b = SLEEP signal is unmasked and the device can enter SLEEP state if there are no pending interrupts and the SLEEP pin (CONFIG2 tied to LDOAO) is active as defined by the SLEEP_POL bit
6	INT_OUTPUT	R/W	OTP	0b = Interrupt output is open drain 1b = Interrupt output is push-pull to VDDIO
5-4	TSLOT_LENGTH[1:0]	R/W	OTP	Time slot duration programming; selects length of the timeslots for startup or shutdown timing 00b = 30 µs 01b = 200 µs 10b = 500 µs 11b = 2 ms
3	SLEEP_POL	R/W	0b	0b = SLEEP signal active high 1b = SLEEP signal active low
2	PWRON_LP_OFF	R/W	OTP	0b = No effect 1b = Allows device turnoff after an nPWRON long press (signal low). After the nPWRON pin is low for 4 s, an interrupt is generated. After 1 additional second, the device performs the power-off sequence.
1	PWRON_LP_OFF_RST	R/W	OTP	0b = No effect 1b = Allows device turnoff after an nPWRON long press (signal low). After the nPWRON pin is low for 4 s, an interrupt is generated. After 1 additional second, the device performs the power-off sequence and registers are loaded with their default values, regardless of LOAD-OTP bit value. This bit has priority over the PWRON_LP_OFF bit and the LOAD-OTP bit.
0	INT_POL	R/W	OTP	0b = INT1 interrupt pad-polarity control signal is active low 1b = INT1 interrupt pad-polarity control signal is active high

8.5.1.3.5 I2C_SPI_CFG Register (Offset = 26h) [reset = OTP]

I2C_SPI_CFG is shown in Table 8-97 and described in Table 8-98.

Return to Summary Table.

Register is reset on a POR event.

Table 8-97. I2C_SPI_CFG Register

7	6	5	4	3	2	1	0
I2CAVS_ID_SEL[1:0]		I2CGP_ID_SEL[1:0]		DCDC4_AVS	DCDC3_AVS	DCDC2_AVS	DCDC1_AVS
R-OTP		R-OTP		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-98. I2C_SPI_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	I2CAVS_ID_SEL[1:0]	R	OTP	Device address for the AVS-I2C interface 00b = 12h 01b = 13h 10b = 14h 11b = 15h
5-4	I2CGP_ID_SEL1[1:0]	R	OTP	Device address for the standard-I2C interface 00b = 2Dh 01b = 2Eh 10b = 2Fh 11b = 30h
3	DCDC4_AVS	R/W	OTP	Interface assignment for the DCDC4_OP and DCDC4_AVS registers 0b = Standard interface 1b = AVS- interface
2	DCDC3_AVS	R/W	OTP	Interface assignment for the DCDC3_OP and DCDC3_AVS registers 0b = Standard interface 1b = AVS- interface
1	DCDC2_AVS	R/W	OTP	Interface assignment for the DCDC2_OP and DCDC2_AVS registers 0b = Standard interface 1b = AVS- interface
0	DCDC1_AVS	R/W	OTP	Interface assignment for the DCDC1_OP and DCDC1_AVS registers 0b = Standard interface 1b = AVS- interface

8.5.1.3.6 KEEP_ON1 Register (Offset = 27h) [reset = OTP]

KEEP_ON1 is shown in Table 8-99 and described in Table 8-100.

Return to Summary Table.

Register is reset on a POR event.
Settings shown in Table 8-109

Table 8-99. KEEP_ON1 Register

7	6	5	4	3	2	1	0
LDO8_KEEPON	LDO7_KEEPON	LDO6_KEEPON	LDO5_KEEPON	LDO4_KEEPON	LDO3_KEEPON	LDO2_KEEPON	LDO1_KEEPON
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-100. KEEP_ON1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
6	LDO7_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
5	LDO6_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
4	LDO5_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
3	LDO4_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
2	LDO3_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
1	LDO2_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
0	LDO1_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state

8.5.1.3.7 KEEP_ON2 Register (Offset = 28h) [reset = OTP]

KEEP_ON2 is shown in Table 8-101 and described in Table 8-102.

Return to Summary Table.

Register is reset on a POR event.
Settings shown in Table 8-109

Table 8-101. KEEP_ON2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_ KEEPON	DCDC3_ KEEPON	DCDC2_ KEEPON	DCDC1_ KEEPON	LDO10_ KEEPON	LDO9_ KEEPON
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-102. KEEP_ON2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bits
5	DCDC4_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state, unless DCDC4_MODE = 1b 1b = Keep active in the SLEEP state
4	DCDC3_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state, unless DCDC3_MODE = 1b 1b = Keep active in the SLEEP state
3	DCDC2_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state, unless DCDC2_MODE = 1b 1b = Keep active in the SLEEP state
2	DCDC1_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state, unless DCDC1_MODE = 1b 1b = Keep active in the SLEEP state
1	LDO10_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state
0	LDO9_KEEPON	R/W	OTP	0b = Set in Eco-mode in the SLEEP state 1b = Keep active in the SLEEP state

8.5.1.3.8 SET_OFF1 Register (Offset = 29h) [reset = OTP]

SET_OFF1 is shown in Table 8-103 and described in Table 8-104.

Return to Summary Table.

Register is reset on a POR event.
Settings shown in Table 8-109

Table 8-103. SET_OFF1 Register

7	6	5	4	3	2	1	0
LDO8_SET_OFF	LDO7_SET_OFF	LDO6_SET_OFF	LDO5_SET_OFF	LDO4_SET_OFF	LDO3_SET_OFF	LDO2_SET_OFF	LDO1_SET_OFF
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-104. SET_OFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
6	LDO7_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
5	LDO6_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
4	LDO5_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
3	LDO4_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
2	LDO3_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
1	LDO2_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
0	LDO1_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b

8.5.1.3.9 SET_OFF2 Register (Offset = 2Ah) [reset = OTP]

SET_OFF2 is shown in Table 8-105 and described in Table 8-106.

Return to Summary Table.

Register is reset on a POR event.
Settings shown in Section 8.5.1.3.11.

Table 8-105. SET_OFF2 Register

7	6	5	4	3	2	1	0
THERM_KEEP_ON	CLK32KOUT_KEEPON	DCDC4_SET_OFF	DCDC3_SET_OFF	DCDC2_SET_OFF	DCDC1_SET_OFF	LDO10_SET_OFF	LDO9_SET_OFF
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-106. SET_OFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THERM_KEEP_ON	R/W	OTP	0b = Enabled in the SLEEP state 1b = Set off in the SLEEP state
6	CLK32KOUT_KEEPON	R/W	OTP	0b = Enabled in the SLEEP state 1b = Set off in the SLEEP state
5	DCDC4_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
4	DCDC3_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
3	DCDC2_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
2	DCDC1_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
1	LDO10_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b
0	LDO9_SET_OFF	R/W	OTP	0b = Defined by the KEEP_ON register 1b = Set off in the SLEEP state if the KEEP_ON bit set to 0b

8.5.1.3.10 DEF_VOLT Register (Offset = 2Bh) [reset = OTP]

DEF_VOLT is shown in Table 8-107 and described in Table 8-108.

Return to Summary Table.

Register is reset on a POR event.
Settings shown in Table 8-109

Table 8-107. DEF_VOLT Register

7	6	5	4	3	2	1	0
LDO4_DEF_VOLT	LDO3_DEF_VOLT	LDO2_DEF_VOLT	LDO1_DEF_VOLT	DCDC4_DEF_VOLT	DCDC3_DEF_VOLT	DCDC2_DEF_VOLT	DCDC1_DEF_VOLT
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-108. DEF_VOLT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4_DEF_VOLT	R/W	OTP	See Table 8-6
6	LDO3_DEF_VOLT	R/W	OTP	See Table 8-6
5	LDO2_DEF_VOLT	R/W	OTP	See Table 8-6
4	LDO1_DEF_VOLT	R/W	OTP	See Table 8-6
3	DCDC4_DEF_VOLT	R/W	OTP	See Table 8-6
2	DCDC3_DEF_VOLT	R/W	OTP	See Table 8-6

Table 8-108. DEF_VOLT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DCDC2_DEF_VOLT	R/W	OTP	See Table 8-6
0	DCDC1_DEF_VOLT	R/W	OTP	See Table 8-6

8.5.1.3.11 LDO Sleep Mode Behavior

Table 8-109. LDO SLEEP MODE BEHAVIOR

CONFIG BITS	LDO IS SET TO Eco-mode	LDO STAYS ACTIVE	LDO IS SET TO OFF
DEF_VOLT	0b = Voltage defined by the _OP register	0b = Voltage defined by the _OP register	0b = Voltage defined by the _OP register
	1b = Voltage defined by the _AVS register	1b = Voltage defined by the _AVS register	1b = Voltage defined by the _AVS register
KEEP ON	0b	1b	0b
SET OFF	0b	x	1b

8.5.1.3.12 DEF_VOLT_MAPPING Register (Offset = 2Ch) [reset = OTP]

DEF_VOLT_MAPPING is shown in Table 8-110 and described in Table 8-111.

Return to Summary Table.

Register is reset on a POR event.

Table 8-110. DEF_VOLT_MAPPING Register

7	6	5	4	3	2	1	0
LDO4_VOLT_MAPPING[1:0]		LDO3_VOLT_MAPPING[1:0]		LDO2_VOLT_MAPPING[1:0]		LDO1_VOLT_MAPPING[1:0]	
R/W-OTP		R/W-OTP		R/W-OTP		R/W-OTP	

Table 8-111. DEF_VOLT_MAPPING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LDO4_VOLT_MAPPING[1:0]	R/W	OTP	Maps a DCDCx_SEL pin to the voltage scaling function to select either LDO4_OP or LDO4_AVS as the register defining the output voltage for LDO4 for when CONFIG2 is tied to GND. DEF_VOLT bit set and cleared by the status of the: 00b = DCDC1_SEL pin 01b = DCDC2_SEL pin 10b = DCDC3_SEL pin 11b = DCDC4_SEL pin
5-4	LDO3_VOLT_MAPPING[1:0]	R/W	OTP	Maps a DCDCx_SEL pin to the voltage scaling function to select either LDO3_OP or LDO3_AVS as the register defining the output voltage for LDO3. DEF_VOLT bit set and cleared by the status of the: 00b = DCDC1_SEL pin 01b = DCDC2_SEL pin 10b = DCDC3_SEL pin 11b = DCDC4_SEL pin
3-2	LDO2_VOLT_MAPPING[1:0]	R/W	OTP	Maps a DCDCx_SEL pin to the voltage scaling function to select either LDO2_OP or LDO2_AVS as the register defining the output voltage for LDO2. DEF_VOLT bit set and cleared by the status of the: 00b = DCDC1_SEL pin 01b = DCDC2_SEL pin 10b = DCDC3_SEL pin 11b = DCDC4_SEL pin

Table 8-111. DEF_VOLT_MAPPING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LDO1_VOLT_MAPPING[1:0]	R/W	OTP	Maps a DCDCx_SEL pin to the voltage scaling function to select either LDO1_OP or LDO1_AVS as the register defining the output voltage for LDO1. DEF_VOLT bit set and cleared by the status of the: 00b = DCDC1_SEL pin 01b = DCDC2_SEL pin 10b = DCDC3_SEL pin 11b = DCDC4_SEL pin

8.5.1.3.13 DISCHARGE1 Register (Offset = 2Dh) [reset = OTP]

DISCHARGE1 is shown in Table 8-112 and described in Table 8-113.

Return to Summary Table.

Register is reset on a POR event.

Table 8-112. DISCHARGE1 Register

7	6	5	4	3	2	1	0
LDO8_ DISCHARGE	LDO7_ DISCHARGE	LDO6_ DISCHARGE	LDO5_ DISCHARGE	LDO4_ DISCHARGE	LDO3_ DISCHARGE	LDO2_ DISCHARGE	LDO1_ DISCHARGE
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-113. DISCHARGE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_DISCHARGE	R/W	OTP	0b = LDO8 output is not discharged when disabled 1b = LDO8 output is discharged when disabled
6	LDO7_DISCHARGE	R/W	OTP	0b = LDO7 output is not discharged when disabled 1b = LDO7 output is discharged when disabled
5	LDO6_DISCHARGE	R/W	OTP	0b = LDO6 output is not discharged when disabled 1b = LDO6 output is discharged when disabled
4	LDO5_DISCHARGE	R/W	OTP	0b = LDO5 output is not discharged when disabled 1b = LDO5 output is discharged when disabled
3	LDO4_DISCHARGE	R/W	OTP	0b = LDO4 output is not discharged when disabled 1b = LDO4 output is discharged when disabled
2	LDO3_DISCHARGE	R/W	OTP	0b = LDO3 output is not discharged when disabled 1b = LDO3 output is discharged when disabled
1	LDO2_DISCHARGE	R/W	OTP	0b = LDO2 output is not discharged when disabled 1b = LDO2 output is discharged when disabled
0	LDO1_DISCHARGE	R/W	OTP	0b = LDO1 output is not discharged when disabled 1b = LDO1 output is discharged when disabled

8.5.1.3.14 DISCHARGE2 Register (Offset = 2Eh) [reset = OTP]

DISCHARGE2 is shown in Table 8-114 and described in Table 8-115.

Return to Summary Table.

Register is reset on a POR event.

Table 8-114. DISCHARGE2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_ DISCHARGE	DCDC3_ DISCHARGE	DCDC2_ DISCHARGE	DCDC1_ DISCHARGE	LDO10_ DISCHARGE	LDO9_ DISCHARGE
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-115. DISCHARGE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	DCDC4_DISCHARGE	R/W	OTP	0b = DCDC4 output is not discharged when disabled 1b = DCDC4 output is discharged when disabled
4	DCDC3_DISCHARGE	R/W	OTP	0b = DCDC3 output is not discharged when disabled 1b = DCDC3 output is discharged when disabled
3	DCDC2_DISCHARGE	R/W	OTP	0b = DCDC2 output is not discharged when disabled 1b = DCDC2 output is discharged when disabled
2	DCDC1_DISCHARGE	R/W	OTP	0b = DCDC1 output is not discharged when disabled 1b = DCDC1 output is discharged when disabled
1	LDO10_DISCHARGE	R/W	OTP	0b = LDO10 output is not discharged when disabled 1b = LDO10 output is discharged when disabled
0	LDO9_DISCHARGE	R/W	OTP	0b = LDO9 output is not discharged when disabled 1b = LDO9 output is discharged when disabled

8.5.1.3.15 EN1_SET1 Register (Offset = 2Fh) [reset = OTP]

EN1_SET1 is shown in Table 8-116 and described in Table 8-117.

Return to Summary Table.

Register is reset on a POR event.

Table 8-116. EN1_SET1 Register

7	6	5	4	3	2	1	0
LDO8_EN1	LDO7_EN1	LDO6_EN1	LDO5_EN1	LDO4_EN1	LDO3_EN1	LDO2_EN1	LDO1_EN1
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-117. EN1_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO8 enable 1b = EN1 pin is controlling LDO8
6	LDO7_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO7 enable 1b = EN1 pin is controlling LDO7
5	LDO6_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO6 enable 1b = EN1 pin is controlling LDO6
4	LDO5_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO5 enable 1b = EN1 pin is controlling LDO5
3	LDO4_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO4 enable 1b = EN1 pin is controlling LDO4
2	LDO3_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO3 enable 1b = EN1 pin is controlling LDO3
1	LDO2_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO2 enable 1b = EN1 pin is controlling LDO2
0	LDO1_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO1 enable 1b = EN1 pin is controlling LDO1

8.5.1.3.16 EN1_SET2 Register (Offset = 30h) [reset = OTP]

EN1_SET2 is shown in Table 8-118 and described in Table 8-119.

Return to Summary Table.

Register is reset on a POR event.

Table 8-118. EN1_SET2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_EN1	DCDC3_EN1	DCDC2_EN1	DCDC1_EN1	LDO10_EN1	LDO9_EN1
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-119. EN1_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	DCDC4_EN1	R/W	OTP	0b = EN1 pin has no effect on DCDC4 enable 1b = EN1 pin is controlling DCDC4
4	DCDC3_EN1	R/W	OTP	0b = EN1 pin has no effect on DCDC3 enable 1b = EN1 pin is controlling DCDC3

Table 8-119. EN1_SET2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCDC2_EN1	R/W	OTP	0b = EN1 pin has no effect on DCDC2 enable 1b = EN1 pin is controlling DCDC2
2	DCDC1_EN1	R/W	OTP	0b = EN1 pin has no effect on DCDC1 enable 1b = EN1 pin is controlling DCDC1
1	LDO10_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO10 enable 1b = EN1 pin is controlling LDO10
0	LDO9_EN1	R/W	OTP	0b = EN1 pin has no effect on LDO9 enable 1b = EN1 pin is controlling LDO9

8.5.1.3.17 EN2_SET1 Register (Offset = 31h) [reset = OTP]

EN2_SET1 is shown in Table 8-120 and described in Table 8-121.

Return to Summary Table.

Register is reset on a POR event.

Table 8-120. EN2_SET1 Register

7	6	5	4	3	2	1	0
LDO8_EN2	LDO7_EN2	LDO6_EN2	LDO5_EN2	LDO4_EN2	LDO3_EN2	LDO2_EN2	LDO1_EN2
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-121. EN2_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO8 enable 1b = EN2 pin is controlling LDO8
6	LDO7_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO7 enable 1b = EN2 pin is controlling LDO7
5	LDO6_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO6 enable 1b = EN2 pin is controlling LDO6
4	LDO5_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO5 enable 1b = EN2 pin is controlling LDO5
3	LDO4_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO4 enable 1b = EN2 pin is controlling LDO4
2	LDO3_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO3 enable 1b = EN2 pin is controlling LDO3
1	LDO2_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO2 enable 1b = EN2 pin is controlling LDO2
0	LDO1_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO1 enable 1b = EN2 pin is controlling LDO1

8.5.1.3.18 EN2_SET2 Register (Offset = 32h) [reset = OTP]

EN2_SET2 is shown in Table 8-122 and described in Table 8-123.

Return to Summary Table.

Register is reset on a POR event.

Table 8-122. EN2_SET2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_EN2	DCDC3_EN2	DCDC2_EN2	DCDC1_EN2	LDO10_EN2	LDO9_EN2
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-123. EN2_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	DCDC4_EN2	R/W	OTP	0b = EN2 pin has no effect on DCDC4 enable 1b = EN2 pin is controlling DCDC4
4	DCDC3_EN2	R/W	OTP	0b = EN2 pin has no effect on DCDC3 enable 1b = EN2 pin is controlling DCDC3

Table 8-123. EN2_SET2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCDC2_EN2	R/W	OTP	0b = EN2 pin has no effect on DCDC2 enable 1b = EN2 pin is controlling DCDC2
2	DCDC1_EN2	R/W	OTP	0b = EN2 pin has no effect on DCDC1 enable 1b = EN2 pin is controlling DCDC1
1	LDO10_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO10 enable 1b = EN2 pin is controlling LDO10
0	LDO9_EN2	R/W	OTP	0b = EN2 pin has no effect on LDO9 enable 1b = EN2 pin is controlling LDO9

8.5.1.3.19 EN3_SET1 Register (Offset = 33h) [reset = OTP]

EN3_SET1 is shown in Table 8-124 and described in Table 8-125.

Return to Summary Table.

Register is reset on a POR event.

Table 8-124. EN3_SET1 Register

7	6	5	4	3	2	1	0
LDO8_EN3	LDO7_EN3	LDO6_EN3	LDO5_EN3	LDO4_EN3	LDO3_EN3	LDO2_EN3	LDO1_EN3
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-125. EN3_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO8 enable 1b = EN3 pin is controlling LDO8
6	LDO7_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO7 enable 1b = EN3 pin is controlling LDO7
5	LDO6_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO6 enable 1b = EN3 pin is controlling LDO6
4	LDO5_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO5 enable 1b = EN3 pin is controlling LDO5
3	LDO4_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO4 enable 1b = EN3 pin is controlling LDO4
2	LDO3_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO3 enable 1b = EN3 pin is controlling LDO3
1	LDO2_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO2 enable 1b = EN3 pin is controlling LDO2
0	LDO1_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO1 enable 1b = EN3 pin is controlling LDO1

8.5.1.3.20 EN3_SET2 Register (Offset = 34h) [reset = OTP]

EN3_SET2 is shown in Table 8-126 and described in Table 8-127.

Return to Summary Table.

Register is reset on a POR event.

Table 8-126. EN3_SET2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_EN3	DCDC3_EN3	DCDC2_EN3	DCDC1_EN3	LDO10_EN3	LDO9_EN3
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-127. EN3_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	DCDC4_EN3	R/W	OTP	0b = EN3 pin has no effect on DCDC4 enable 1b = EN3 pin is controlling DCDC4
4	DCDC3_EN3	R/W	OTP	0b = EN3 pin has no effect on DCDC3 enable 1b = EN3 pin is controlling DCDC3

Table 8-127. EN3_SET2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCDC2_EN3	R/W	OTP	0b = EN3 pin has no effect on DCDC2 enable 1b = EN3 pin is controlling DCDC2
2	DCDC1_EN3	R/W	OTP	0b = EN3 pin has no effect on DCDC1 enable 1b = EN3 pin is controlling DCDC1
1	LDO10_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO10 enable 1b = EN3 pin is controlling LDO10
0	LDO9_EN3	R/W	OTP	0b = EN3 pin has no effect on LDO9 enable 1b = EN3 pin is controlling LDO9

8.5.1.3.21 EN4_SET1 Register (Offset = 35h) [reset = OTP]

EN4_SET1 is shown in Table 8-128 and described in Table 8-129.

Return to Summary Table.

Register is reset on a POR event.

Table 8-128. EN4_SET1 Register

7	6	5	4	3	2	1	0
LDO8_EN4	LDO7_EN4	LDO6_EN4	LDO5_EN4	LDO4_EN4	LDO3_EN4	LDO2_EN4	LDO1_EN4
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-129. EN4_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO8_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO8 enable 1b = EN4 pin is controlling LDO8
6	LDO7_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO7 enable 1b = EN4 pin is controlling LDO7
5	LDO6_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO6 enable 1b = EN4 pin is controlling LDO6
4	LDO5_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO5 enable 1b = EN4 pin is controlling LDO5
3	LDO4_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO4 enable 1b = EN4 pin is controlling LDO4
2	LDO3_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO3 enable 1b = EN4 pin is controlling LDO3
1	LDO2_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO2 enable 1b = EN4 pin is controlling LDO2
0	LDO1_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO1 enable 1b = EN4 pin is controlling LDO1

8.5.1.3.22 EN4_SET2 Register (Offset = 36h) [reset = OTP]

EN4_SET2 is shown in Table 8-130 and described in Table 8-131.

Return to Summary Table.

Register is reset on a POR event.

Table 8-130. EN4_SET2 Register

7	6	5	4	3	2	1	0
RSVD		DCDC4_EN4	DCDC3_EN4	DCDC2_EN4	DCDC1_EN4	LDO10_EN4	LDO9_EN4
R-00b		R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-131. EN4_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	DCDC4_EN4	R/W	OTP	0b = EN4 pin has no effect on DCDC4 enable 1b = EN4 pin is controlling DCDC4
4	DCDC3_EN4	R/W	OTP	0b = EN4 pin has no effect on DCDC3 enable 1b = EN4 pin is controlling DCDC3

Table 8-131. EN4_SET2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCDC2_EN4	R/W	OTP	0b = EN4 pin has no effect on DCDC2 enable 1b = EN4 pin is controlling DCDC2
2	DCDC1_EN4	R/W	OTP	0b = EN4 pin has no effect on DCDC1 enable 1b = EN4 pin is controlling DCDC1
1	LDO10_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO10 enable 1b = EN4 pin is controlling LDO10
0	LDO9_EN4	R/W	OTP	0b = EN4 pin has no effect on LDO9 enable 1b = EN4 pin is controlling LDO9

8.5.1.3.23 PGOOD Register (Offset = 37h) [reset = OTP]

PGOOD is shown in Table 8-132 and described in Table 8-133.

Return to Summary Table.

Register is reset on a POR event.

Table 8-132. PGOOD Register

7	6	5	4	3	2	1	0
PGOOD_LDO4	PGOOD_LDO3	PGOOD_LDO2	PGOOD_LDO1	PGOOD_DCDC4	PGOOD_DCDC3	PGOOD_DCDC2	PGOOD_DCDC1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-133. PGOOD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGOOD_LDO4	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block 0b = LDO4 output voltage is below its target regulation voltage or disabled 1b = LDO4 output voltage is in regulation
6	PGOOD_LDO3	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block 0b = LDO3 output voltage is below its target regulation voltage or disabled 1b = LDO3 output voltage is in regulation
5	PGOOD_LDO2	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block 0b = LDO2 output voltage is below its target regulation voltage or disabled 1b = LDO2 output voltage is in regulation
4	PGOOD_LDO1	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block 0b = LDO1 output voltage is below its target regulation voltage or disabled 1b = LDO1 output voltage is in regulation
3	PGOOD_DCDC4	R	0b	The bit is set or cleared by the power-good comparator in the DC-DC converter block The PGOOD_LDO4 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = DCDC4 output voltage is below its target regulation voltage or disabled 1b = DCDC4 output voltage is in regulation
2	PGOOD_DCDC3	R	0b	The bit is set or cleared by the power-good comparator in the DC-DC converter block The PGOOD_LDO3 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = DCDC3 output voltage is below its target regulation voltage or disabled 1b = DCDC3 output voltage is in regulation

Table 8-133. PGOOD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PGOOD_DCDC2	R	0b	The bit is set or cleared by the power-good comparator in the DC-DC converter block The PGOOD_LDO2 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = DCDC2 output voltage is below its target regulation voltage or disabled 1b = DCDC2 output voltage is in regulation
0	PGOOD_DCDC1	R	0b	The bit is set or cleared by the power-good comparator in the DC-DC converter block The PGOOD_LDO1 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = DCDC1 output voltage is below its target regulation voltage or disabled 1b = DCDC1 output voltage is in regulation

8.5.1.3.24 PGOOD2 Register (Offset = 38h) [reset = OTP]

PGOOD2 is shown in Table 8-134 and described in Table 8-135.

Return to Summary Table.

Register is reset on a POR event.

Table 8-134. PGOOD2 Register

7	6	5	4	3	2	1	0
RSVD		PGOOD_LDO10	PGOOD_LDO9	PGOOD_LDO8	PGOOD_LDO7	PGOOD_LDO6	PGOOD_LDO5
R-00b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-135. PGOOD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	PGOOD_LDO10	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO10 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO10 output voltage is below its target regulation voltage or disabled 1b = LDO10 output voltage is in regulation
4	PGOOD_LDO9	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO9 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO9 output voltage is below its target regulation voltage or disabled 1b = LDO9 output voltage is in regulation

Table 8-135. PGOOD2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PGOOD_LDO8	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO8 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO8 output voltage is below its target regulation voltage or disabled 1b = LDO8 output voltage is in regulation
2	PGOOD_LDO7	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO7 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO7 output voltage is below its target regulation voltage or disabled 1b = LDO7 output voltage is in regulation
1	PGOOD_LDO6	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO6 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO6 output voltage is below its target regulation voltage or disabled 1b = LDO6 output voltage is in regulation
0	PGOOD_LDO5	R	0b	The bit is set or cleared by the power-good comparator in the LDO converter block The PGOOD_LDO5 bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V. 0b = LDO5 output voltage is below its target regulation voltage or disabled 1b = LDO5 output voltage is in regulation

8.5.1.3.25 INT_STS Register (Offset = 39h) [reset = 00h]

INT_STS is shown in Table 8-136 and described in Table 8-137.

Return to Summary Table.

Register is reset on a POR event.

Table 8-136. INT_STS Register

7	6	5	4	3	2	1	0
GPIO1_F_IT	GPIO1_R_IT	HOTDIE_IT	PWRHOLD_R_IT	PWRON_LP_IT	PWRON_IT	VMON_IT	PWRHOLD_F_IT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-137. INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_F_IT	R/W	0b	0b = No falling edge occurred 1b = GPIO1 falling edge detection interrupt status; write 1b to clear the interrupt flag
6	GPIO1_R_IT	R/W	0b	0b = No rising edge occurred 1b = GPIO1 rising edge detection interrupt status; write 1b to clear the interrupt flag
5	HOTDIE_IT	R/W	0b	0b = No hot die event occurred 1b = Hot die event interrupt status; write 1b to clear the interrupt flag
4	PWRHOLD_R_IT	R/W	0b	0b = No rising edge on the PWRHOLD pin is detected 1b = Rising PWRHOLD event interrupt status; write 1b to clear the interrupt flag
3	PWRON_LP_IT	R/W	0b	0b = No nPWRON long press key detected 1b = nPWRON long press event interrupt status; write 1b to clear the interrupt flag
2	PWRON_IT	R/W	0b	0b = No nPWRON event detected 1b = nPWRON event interrupt status; write 1b to clear the interrupt flag
1	VMON_IT	R/W	0b	0b = No VMON event detected 1b = falling edge detection for VMON; voltage at VMON is below the VMON_SEL[1:0] threshold; no delay; write 1b to clear the interrupt flag
0	PWRHOLD_F_IT	R/W	0b	0b = No PWRHOLD event detected 1b = Falling PWRHOLD event interrupt status; write 1b to clear the interrupt flag

8.5.1.3.26 INT_MSK Register (Offset = 3Ah) [reset = FFh]

INT_MSK is shown in Table 8-138 and described in Table 8-139.

Return to Summary Table.

Register is reset on a POR event.

Table 8-138. INT_MSK Register

7	6	5	4	3	2	1	0
GPIO1_F_IT_MSK	GPIO1_R_IT_MSK	HOTDIE_IT_MSK	PWRHOLD_R_IT_MSK	PWRON_LP_IT_MSK	PWRON_IT_MSK	VMON_IT_MSK	PWRHOLD_F_IT_MSK
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-139. INT_MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_F_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = GPIO1 falling edge detection interrupt masked
6	GPIO1_R_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = GPIO1 rising edge detection interrupt masked
5	HOTDIE_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = Hot die event interrupt masked
4	PWRHOLD_R_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = Rising PWRHOLD event interrupt masked
3	PWRON_LP_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = nPWRON Long Press event interrupt masked
2	PWRON_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = nPWRON event interrupt masked
1	VMON_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = VMON event interrupt masked.
0	PWRHOLD_F_IT_MSK	R/W	OTP	0b = Interrupt not masked OTP = PWRHOLD falling edge event interrupt masked

8.5.1.3.27 INT_STS2 Register (Offset = 3Bh) [reset = 00h]

INT_STS2 is shown in Table 8-140 and described in Table 8-141.

Return to Summary Table.

Register is reset on a POR event.

Table 8-140. INT_STS2 Register

7	6	5	4	3	2	1	0
GPIO5_F_IT	GPIO5_R_IT	GPIO4_F_IT	GPIO4_R_IT	GPIO3_F_IT	GPIO3_R_IT	GPIO2_F_IT	GPIO2_R_IT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-141. INT_STS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO5_F_IT	R/W	0b	0b = No falling edge occurred 1b = GPIO5 falling edge detection interrupt status; write 1b to clear the interrupt flag
6	GPIO5_R_IT	R/W	0b	0b = No rising edge occurred 1b = GPIO5 rising edge detection interrupt status; write 1b to clear the interrupt flag
5	GPIO4_F_IT	R/W	0b	0b = No falling edge occurred 1b = GPIO4 falling edge detection interrupt status; write 1b to clear the interrupt flag
4	GPIO4_R_IT	R/W	0b	0b = No rising edge occurred 1b = GPIO4 rising edge detection interrupt status; write 1b to clear the interrupt flag
3	GPIO3_F_IT	R/W	0b	0b = No falling edge occurred 1b = GPIO3 falling edge detection interrupt status; write 1b to clear the interrupt flag
2	GPIO3_R_IT	R/W	0b	0b = No rising edge occurred 1b = GPIO3 rising edge detection interrupt status; write 1b to clear the interrupt flag
1	GPIO2_F_IT	R/W	0b	0b = No falling edge occurred 1b = GPIO2 falling edge detection interrupt status; write 1b to clear the interrupt flag
0	GPIO2_R_IT	R/W	0b	0b = No rising edge occurred 1b = GPIO2 rising edge detection interrupt status; write 1b to clear the interrupt flag

8.5.1.3.28 INT_MSK2 Register (Offset = 3Ch) [reset = OTP]

INT_MSK2 is shown in Table 8-142 and described in Table 8-143.

Return to Summary Table.

Register is reset on a POR event.

Table 8-142. INT_MSK2 Register

7	6	5	4	3	2	1	0
GPIO5_F_IT_MSK	GPIO5_R_IT_MSK	GPIO4_F_IT_MSK	GPIO4_R_IT_MSK	GPIO3_F_IT_MSK	GPIO3_R_IT_MSK	GPIO2_F_IT_MSK	GPIO2_R_IT_MSK
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-143. INT_MSK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO5_F_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO5 falling edge detection interrupt masked
6	GPIO5_R_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO5 rising edge detection interrupt masked
5	GPIO4_F_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO4 falling edge detection interrupt masked
4	GPIO4_R_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO4 rising edge detection interrupt masked
3	GPIO3_F_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO3 falling edge detection interrupt masked
2	GPIO3_R_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO3 rising edge detection interrupt masked
1	GPIO2_F_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO2 falling edge detection interrupt masked
0	GPIO2_R_IT_MSK	R/W	OTP	0b = Interrupt not masked 1b = GPIO2 rising edge detection interrupt masked

8.5.1.3.29 INT_STS3 Register (Offset = 3Dh) [reset = OTP]

INT_STS3 is shown in Table 8-144 and described in Table 8-145.

Return to Summary Table.

Register is reset on a POR event.

Table 8-144. INT_STS3 Register

7	6	5	4	3	2	1	0
PGOOD_LDO4_IT	PGOOD_LDO3_IT	PGOOD_LDO2_IT	PGOOD_LDO1_IT	PGOOD_DCDC4_IT	PGOOD_DCDC3_IT	PGOOD_DCDC2_IT	PGOOD_DCDC1_IT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-145. INT_STS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGOOD_LDO4_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO4 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled; write 1b to clear the interrupt flag
6	PGOOD_LDO3_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO3 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled; write 1b to clear the interrupt flag
5	PGOOD_LDO2_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO2 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled; write 1b to clear the interrupt flag
4	PGOOD_LDO1_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO1 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled; write 1b to clear the interrupt flag
3	PGOOD_DCDC4_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_DCDC4 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the converter is disabled; write 1b to clear the interrupt flag
2	PGOOD_DCDC3_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_DCDC3 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the converter is disabled; write 1b to clear the interrupt flag
1	PGOOD_DCDC2_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_DCDC2 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the converter is disabled; write 1b to clear the interrupt flag
0	PGOOD_DCDC1_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_DCDC1 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the converter is disabled; write 1b to clear the interrupt flag

8.5.1.3.30 INT_MSK3 Register (Offset = 3Eh) [reset = FFh]

INT_MSK3 is shown in Table 8-146 and described in Table 8-147.

Return to Summary Table.

Register is reset on a POR event.

Table 8-146. INT_MSK3 Register

7	6	5	4	3	2	1	0
PGOOD_LDO4_IT_MSK	PGOOD_LDO3_IT_MSK	PGOOD_LDO2_IT_MSK	PGOOD_LDO1_IT_MSK	PGOOD_DCDC4_IT_MSK	PGOOD_DCDC3_IT_MSK	PGOOD_DCDC2_IT_MSK	PGOOD_DCDC1_IT_MSK
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-147. INT_MSK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PGOOD_LDO4_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO4 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
6	PGOOD_LDO3_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO3 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
5	PGOOD_LDO2_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO2 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
4	PGOOD_LDO1_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO1 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
3	PGOOD_DCDC4_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_DCDC4 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
2	PGOOD_DCDC3_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_DCDC3 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
1	PGOOD_DCDC2_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_DCDC2 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled
0	PGOOD_DCDC1_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_DCDC1 falling edge detection interrupt status; masked by the ENABLE bit, therefore not triggered if the output voltage drops when the LDO is disabled

8.5.1.3.31 INT_STS4 Register (Offset = 3Fh) [reset = 00h]

INT_STS4 is shown in Table 8-148 and described in Table 8-149.

Return to Summary Table.

Register is reset on a POR event.

Table 8-148. INT_STS4 Register

7	6	5	4	3	2	1	0
RSVD		PGOOD_LDO10_IT	PGOOD_LDO9_IT	PGOOD_LDO8_IT	PGOOD_LDO7_IT	PGOOD_LDO6_IT	PGOOD_LDO5_IT
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-149. INT_STS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R/W	00b	Unused bit read returns 0b.
5	PGOOD_LDO10_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO10 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag
4	PGOOD_LDO9_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO9 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag
3	PGOOD_LDO8_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO8 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag
2	PGOOD_LDO7_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO7 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag
1	PGOOD_LDO6_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO6 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag
0	PGOOD_LDO5_IT	R/W	0b	0b = No status change occurred 1b = PGOOD_LDO5 falling or rising edge detection interrupt status; write 1b to clear the interrupt flag

8.5.1.3.32 INT_MSK4 Register (Offset = 40h) [reset = FFh]

INT_MSK4 is shown in Table 8-150 and described in Table 8-151.

Return to Summary Table.

Register is reset on a POR event.

Table 8-150. INT_MSK4 Register

7	6	5	4	3	2	1	0
RSVD		PGOOD_LDO10_IT_MSK	PGOOD_LDO9_IT_MSK	PGOOD_LDO8_IT_MSK	PGOOD_LDO7_IT_MSK	PGOOD_LDO6_IT_MSK	PGOOD_LDO5_IT_MSK
R/W-11b		R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-151. INT_MSK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R/W	11b	Unused bit read returns 0b.

Table 8-151. INT_MSK4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PGOOD_LDO10_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO10 falling or rising edge detection interrupt masked
4	PGOOD_LDO9_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO9 falling or rising edge detection interrupt masked
3	PGOOD_LDO8_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO8 falling or rising edge detection interrupt masked
2	PGOOD_LDO7_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO7 falling or rising edge detection interrupt masked
1	PGOOD_LDO6_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO6 falling or rising edge detection interrupt masked
0	PGOOD_LDO5_IT_MSK	R/W	1b	0b = Interrupt not masked 1b = PGOOD_LDO5 falling or rising edge detection interrupt masked

8.5.1.3.33 GPIO1 Register (Offset = 41h) [reset = OTP]

GPIO1 is shown in Table 8-152 and described in Table 8-153.

Return to Summary Table.

Register is reset on a POR event.

Table 8-152. GPIO1 Register

7	6	5	4	3	2	1	0
GPIO_SLEEP	RSVD		GPIO_DEB	RSVD	GPIO_CFG	GPIO_STS	GPIO_SET
R/W-OTP	R-00b		R/W-OTP	R-0b	R/W-OTP	R-x	R/W-OTP

Table 8-153. GPIO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SLEEP	R/W	OTP	0b = No impact, keep as in ACTIVE state 1b = When in the SLEEP state and GPIO in output mode, force output low
6-5	RSVD	R	00b	Unused bit read returns 0b.
4	GPIO_DEB	R/W	OTP	GPIO input debouncing time 0b = 94 µs 1b = 156 µs
3	RSVD	R	0b	Unused bit
2	GPIO_CFG	R/W	OTP	Configuration of the GPIO pad direction 0b = The GPIO pad is configured as an input 1b = The GPIO pad is configured as an output, GPIO assigned to power-up sequence
1	GPIO_STS	R	x	This bit has no reset value, it is generated based on GPIO pad voltage in real-time 0b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output 1b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output
0	GPIO_SET	R/W	OTP	0b = Value set to logic 0b on the GPIO output when configured in output mode 1b = Value set to logic 1b on the GPIO output when configured in output mode

8.5.1.3.34 GPIO2 Register (Offset = 42h) [reset = OTP]

GPIO2 is shown in Table 8-154 and described in Table 8-155.

Return to Summary Table.

Register is reset on a POR event.

Table 8-154. GPIO2 Register

7	6	5	4	3	2	1	0
GPIO_SLEEP	RSVD		GPIO_DEB	RSVD	GPIO_CFG	GPIO_STS	GPIO_SET
R/W-OTP	R-00b		R/W-OTP	R-0b	R/W-OTP	R-x	R/W-OTP

Table 8-155. GPIO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SLEEP	R/W	OTP	0b = No impact, keep as in ACTIVE state 1b = When in the SLEEP state and GPIO in output mode, force output low
6-5	RSVD	R	00b	Unused bit read returns 0b.
4	GPIO_DEB	R/W		GPIO input debouncing time 0b = 94 µs 1b = 156 µs
3	RSVD	R	0b	Unused bit
2	GPIO_CFG	R/W	OTP	Configuration of the GPIO pad direction 0b = The GPIO pad is configured as an input 1b = The GPIO pad is configured as an output, GPIO assigned to power-up sequence
1	GPIO_STS	R	x	This bit has no reset value, it is generated based on GPIO pad voltage in real-time 0b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output 1b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output
0	GPIO_SET	R/W	OTP	0b = Value set to logic 0b on the GPIO output when configured in output mode 1b = Value set to logic 1b on the GPIO output when configured in output mode

8.5.1.3.35 GPIO3 Register (Offset = 43h) [reset = OTP]

GPIO3 is shown in Table 8-156 and described in Table 8-157.

Return to Summary Table.

Register is reset on a POR event.

Table 8-156. GPIO3 Register

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R-x	R/W-OTP

Table 8-157. GPIO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SLEEP	R/W	OTP	0b = No impact, keep as in ACTIVE state 1b = When in the SLEEP state and GPIO in output mode, force output low
6	GPIO_SEL	R/W	OTP	0b = GPIO_SET to be available at the GPIO pin when configured as output 1b = LEDA out to be available at the GPIO pin when configured as output
5	GPIO_ODEN	R/W	OTP	0b = Push-pull output mode, GPIO assigned to power-up sequence 1b = Open drain output mode
4	GPIO_DEB	R/W	OTP	GPIO input debouncing time 0b = 94 µs 1b = 156 µs
3	GPIO_PDEN	R/W	OTP	GPIO pad pulldown control 0b = Pulldown is disabled 1b = Pulldown is enabled
2	GPIO_CFG	R/W	OTP	Configuration of the GPIO pad direction 0b = The GPIO pad is configured as an input 1b = The GPIO pad is configured as an output, GPIO assigned to power-up sequence
1	GPIO_STS	R	x	This bit has no reset value, it is generated based on GPIO pad voltage in real-time 0b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output 1b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output
0	GPIO_SET	R/W	OTP	0b = Value set to logic 0b on the GPIO output when configured in output mode 1b = Value set to logic 1b on the GPIO output when configured in output mode

8.5.1.3.36 GPIO4 Register (Offset = 44h) [reset = OTP]

GPIO4 is shown in Table 8-158 and described in Table 8-159.

Return to Summary Table.

Register is reset on a POR event.

Table 8-158. GPIO4 Register

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R-x	R/W-OTP

Table 8-159. GPIO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SLEEP	R/W	OTP	0b = No impact, keep as in ACTIVE state 1b = When in the SLEEP state and GPIO in output mode, force output low
6	GPIO_SEL	R/W	OTP	0b = GPIO_SET to be available at the GPIO pin when configured as output 1b = LEDB out to be available at the GPIO pin when configured as output
5	GPIO_ODEN	R/W	OTP	0b = Push-pull output mode, GPIO assigned to power-up sequence 1b = Open drain output mode
4	GPIO_DEB	R/W	OTP	GPIO input debouncing time 0b = 94 µs 1b = 156 µs
3	GPIO_PDEN	R/W	OTP	GPIO pad pulldown control 0b = Pulldown is disabled 1b = Pulldown is enabled
2	GPIO_CFG	R/W	OTP	Configuration of the GPIO pad direction 0b = The pad is configured as an input 1b = The GPIO pad is configured as an output, GPIO assigned to power-up sequence
1	GPIO_STS	R	x	This bit has no reset value, it is generated based on GPIO pad voltage in real-time 0b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output 1b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output
0	GPIO_SET	R/W	OTP	0b = Value set to logic 0b on the GPIO output when configured in output mode 1b = Value set to logic 1b on the GPIO output when configured in output mode

8.5.1.3.37 GPIO5 Register (Offset = 45h) [reset = OTP]

GPIO5 is shown in Table 8-160 and described in Table 8-161.

Return to Summary Table.

Register is reset on a POR event.

Table 8-160. GPIO5 Register

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP	R-x	R/W-OTP

Table 8-161. GPIO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SLEEP	R/W	OTP	0b = No impact, keep as in ACTIVE state 1b = When in the SLEEP state and GPIO in output mode, force output low
6	GPIO_SEL	R/W	OTP	0b = GPIO_SET to be available at the GPIO pin when configured as output 1b = LEDC out to be available at the GPIO pin when configured as output
5	GPIO_ODEN	R/W	OTP	0b = Push-pull output mode, GPIO assigned to power-up sequence 1b = Open drain output mode
4	GPIO_DEB	R/W	OTP	GPIO input debouncing time 0b = 94 µs 1b = 156 µs
3	GPIO_PDEN	R/W	OTP	GPIO pad pulldown control 0b = Pulldown is disabled 1b = Pulldown is enabled
2	GPIO_CFG	R/W	OTP	Configuration of the GPIO pad direction 0b = The pad is configured as an input 1b = The GPIO pad is configured as an output, GPIO assigned to power-up sequence
1	GPIO_STS	R	x	This bit has no reset value, it is generated based on GPIO pad voltage in real-time 0b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output 1b = Voltage on GPIO pad is greater than V_{IH} if configured as an input, V_{OH} if configured as an output
0	GPIO_SET	R/W	OTP	0b = Value set to logic 0b on the GPIO output when configured in output mode 1b = Value set to logic 1b on the GPIO output when configured in output mode

8.5.1.3.38 VMON Register (Offset = 46h) [reset = OTP]

VMON is shown in Table 8-162 and described in Table 8-163.

Return to Summary Table.

Register is reset on a POR event.

Table 8-162. VMON Register

7	6	5	4	3	2	1	0
RSVD	VMON_DELAY[1:0]		VSUP_MASK	RSVD	VSUP_OUT	VMON_SEL[1:0]	
R-0b	R/W-OTP		R/W-OTP	R-0b	R-x	R/W-OTP	

Table 8-163. VMON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6	VMON_DELAY[1:0]	R/W	OTP	Delays the output signal at the VSUP_OUT pin for a falling input voltage on the VMON_IN pin to allow an interrupt to be generated before the VSUP_OUT pin goes low 00b = No falling edge delay 01b = 50-µs falling edge delay 10b = 100-µs falling edge delay 11b = 250-µs falling edge delay
5	VSUP_MASK	R/W	OTP	0b = The output of the voltage monitor is not used as a switch-off event 1b = The output of the voltage monitor is used as a switch-off event
4	RSVD	R	0b	Unused bit
3	VSUP_OUT	R	x	This bit has no reset value, it is generated based on the status output of the voltage monitor: 0b = The voltage at the VCCS/VIN_MON pin is below the VMON threshold 1b = The voltage at the VCCS/VIN_MON pin is above the VMON threshold
2	VMON_SEL[1:0]	R/W	OTP	Battery voltage comparator threshold: 00b = VMON threshold is 3.1 V (rising voltage) 01b = VMON threshold is 2.9 V (rising voltage) 10b = VMON threshold is 2.8 V (rising voltage) 11b = VMON threshold is 2.7 V (rising voltage)

8.5.1.3.39 LEDA_CTRL1 Register (Offset = 47h) [reset = 00h]

LEDA_CTRL1 is shown in Table 8-164 and described in Table 8-165.

Return to Summary Table.

Register is reset on a POR event.

Table 8-164. LEDA_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD		LEDA_RAMP_ENABLE	RSVD	LEDA_CURRENT[3:0]			
R-00b		R/W-0b	R-0b	R/W-0000b			

Table 8-165. LEDA_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	LEDA_RAMP_ENABLE	R/W	0b	0b = No ramp 1b = Ramp enabled
4	RSVD	R	0b	Unused bit
3-0	LEDA_CURRENT[3:0]	R/W	0000b	LEDA DC current. See Table 8-218

8.5.1.3.40 LEDA_CTRL2 Register (Offset = 48h) [reset = 00h]

LEDA_CTRL2 is shown in Table 8-166 and described in Table 8-167.

Return to Summary Table.

Register is reset on a POR event.

Table 8-166. LEDA_CTRL2 Register

7	6	5	4	3	2	1	0
RSVD	LEDA_T1[6:0]						
R-0b	R/W-0000000b						

Table 8-167. LEDA_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDA_T1[6:0]	R/W	0000000b	LEDA T1 sequence length = LEDA_T1[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.41 LEDA_CTRL3 Register (Offset = 49h) [reset = 00h]

LEDA_CTRL3 is shown in Table 8-168 and described in Table 8-169.

Return to Summary Table.

Register is reset on a POR event.

Table 8-168. LEDA_CTRL3 Register

7	6	5	4	3	2	1	0
RSVD	LEDA_T2[6:0]						
R-0b	R/W-0000000b						

Table 8-169. LEDA_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDA_T2[6:0]	R/W	0000000b	LEDA T2 sequence length = LEDA_T2[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.42 LEDA_CTRL4 Register (Offset = 4Ah) [reset = 00h]

LEDA_CTRL4 is shown in Table 8-170 and described in Table 8-171.

Return to Summary Table.

Register is reset on a POR event.

Table 8-170. LEDA_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	LEDA_T3[6:0]						
R-0b	R/W-0000000b						

Table 8-171. LEDA_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDA_T3[6:0]	R/W	0000000b	LEDA T3 sequence length = LEDA_T3[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.43 LEDA_CTRL5 Register (Offset = 4Bh) [reset = 00h]

LEDA_CTRL5 is shown in Table 8-172 and described in Table 8-173.

Return to Summary Table.

Register is reset on a POR event.

Table 8-172. LEDA_CTRL5 Register

7	6	5	4	3	2	1	0
RSVD	LEDA_T4[6:0]						
R-0b	R/W-0000000b						

Table 8-173. LEDA_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDA_T4[6:0]	R/W	0000000b	LEDA T4 sequence length = LEDA_T4[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.44 LEDA_CTRL6 Register (Offset = 4Ch) [reset = 00h]

LEDA_CTRL6 is shown in Table 8-174 and described in Table 8-175.

Return to Summary Table.

Register is reset on a POR event.

Table 8-174. LEDA_CTRL6 Register

7	6	5	4	3	2	1	0
RSVD	LEDA_TP[6:0]						
R-0b	R/W-0000000b						

Table 8-175. LEDA_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDA_TP[6:0]	R/W	0000000b	LEDA TP sequence length = LEDA_TP[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.45 LEDA_CTRL7 Register (Offset = 4Dh) [reset = 00h]

LEDA_CTRL7 is shown in Table 8-176 and described in Table 8-177.

Return to Summary Table.

Register is reset on a POR event.

Table 8-176. LEDA_CTRL7 Register

7	6	5	4	3	2	1	0
RSVD			LEDA_PWM[4:0]				
R-000b			R/W-00000b				

Table 8-177. LEDA_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDA_PWM[4:0]	R/W	00000b	LEDA_ON duty-cycle: ([LEDA_PWM] +1) × 1 / 32 × 8-ms period 00000b = 1 / 2 × 8 ms (LEDA_ON is high for 250 µs, low for 7.75 ms) 11111b = 32 / 32 × 8 ms (LEDA_ON is always high)

8.5.1.3.46 LEDA_CTRL8 Register (Offset = 4Eh) [reset = 00h]

LEDA_CTRL8 is shown in Table 8-178 and described in Table 8-179.

Return to Summary Table.

Register is reset on a POR event.

Table 8-178. LEDA_CTRL8 Register

7	6	5	4	3	2	1	0
RSVD			LEDA_ON_TIME[4:0]				
R-000b			R/W-00000b				

Table 8-179. LEDA_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDA_ON_TIME[4:0]	R/W	00000b	LEDA ON-TIME: LEDA_ON_TME[4:0] × 64 ms 00000b = 0 × 64 ms 11111b = 31 × 64 ms

8.5.1.3.47 LEDB_CTRL1 Register (Offset = 4Fh) [reset = 00h]

LEDB_CTRL1 is shown in Table 8-180 and described in Table 8-181.

Return to Summary Table.

Register is reset on a POR event.

Table 8-180. LEDB_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD		LEDB_RAMP_ENABLE	RSVD	LEDB_CURRENT[3:0]			
R-00b		R/W-0b	R-0b	R/W-0000b			

Table 8-181. LEDB_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	LEDB_RAMP_ENABLE	R/W	0b	0b = No ramp 1b = Ramp enabled
4	RSVD	R	0b	Unused bit
3-0	LEDBA_CURRENT[3:0]	R/W	0000b	LEDB DC current. See Table 8-218

8.5.1.3.48 LEDB_CTRL2 Register (Offset = 50h) [reset = 00h]

LEDB_CTRL2 is shown in Table 8-182 and described in Table 8-183.

Return to Summary Table.

Register is reset on a POR event.

Table 8-182. LEDB_CTRL2 Register

7	6	5	4	3	2	1	0
RSVD	LEDB_T1[6:0]						
R-0b	R/W-0000000b						

Table 8-183. LEDB_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDB_T1[6:0]	R/W	0000000b	LEDB T1 sequence length = LEDB_T1[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.49 LEDB_CTRL3 Register (Offset = 51h) [reset = 00h]

LEDB_CTRL3 is shown in Table 8-184 and described in Table 8-185.

Return to Summary Table.

Register is reset on a POR event.

Table 8-184. LEDB_CTRL3 Register

7	6	5	4	3	2	1	0
RSVD	LEDB_T2[6:0]						
R-0b	R/W-0000000b						

Table 8-185. LEDB_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	000b	Unused bit read returns 0b.
6-0	LEDB_T2[6:0]	R/W	0000000b	LEDB T2 sequence length = LEDB_T2[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.50 LEDB_CTRL4 Register (Offset = 52h) [reset = 00h]

LEDB_CTRL4 is shown in Table 8-186 and described in Table 8-187.

Return to Summary Table.

Register is reset on a POR event.

Table 8-186. LEDB_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	LEDB_T3[6:0]						
R-0b	R/W-0000000b						

Table 8-187. LEDB_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDB_T3[6:0]	R/W	0000000b	LEDB T3 sequence length = LEDB_T3[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.51 LEDB_CTRL5 Register (Offset = 53h) [reset = 00h]

LEDB_CTRL5 is shown in Table 8-188 and described in Table 8-189.

Return to Summary Table.

Register is reset on a POR event.

Table 8-188. LEDB_CTRL5 Register

7	6	5	4	3	2	1	0
RSVD	LEDB_T4[6:0]						
R-0b	R/W-0000000b						

Table 8-189. LEDB_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	000b	Unused bit read returns 0b.
6-0	LEDB_T4[6:0]	R/W	0000000b	LEDB T4 sequence length = LEDB_T4[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.52 LEDB_CTRL6 Register (Offset = 54h) [reset = 00h]

LEDB_CTRL6 is shown in Table 8-190 and described in Table 8-191.

Return to Summary Table.

Register is reset on a POR event.

Table 8-190. LEDB_CTRL6 Register

7	6	5	4	3	2	1	0
RSVD	LEDB_TP[6:0]						
R-0b	R/W-0000000b						

Table 8-191. LEDB_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDB_TP[6:0]	R/W	0000000b	LEDB TP sequence length = LEDB_TP[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.53 LEDB_CTRL7 Register (Offset = 55h) [reset = 00h]

LEDB_CTRL7 is shown in Table 8-192 and described in Table 8-193.

Return to Summary Table.

Register is reset on a POR event.

Table 8-192. LEDB_CTRL7 Register

7	6	5	4	3	2	1	0
RSVD			LEDB_PWM[4:0]				
R-000b			R/W-00000b				

Table 8-193. LEDB_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDB_PWM[4:0]	R/W	00000b	LEDB_ON duty-cycle: ([LEDB_PWM] +1) × 1 / 32 × 8-ms period 00000b = 1 / 32 × 8 ms (LEDB_ON is high for 250 µs, low for 7.75 ms) 11111b = 32 / 32 × 8 ms (LEDB_ON is always high)

8.5.1.3.54 LEDB_CTRL8 Register (Offset = 56h) [reset = 00h]

LEDB_CTRL8 is shown in Table 8-194 and described in Table 8-195.

Return to Summary Table.

Register is reset on a POR event.

Table 8-194. LEDB_CTRL8 Register

7	6	5	4	3	2	1	0
RSVD			LEDB_ON_TIME[4:0]				
R-000b			R/W-00000b				

Table 8-195. LEDB_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDB_ON_TIME[4:0]	R/W	00000b	LEDB ON-TIME: LEDB_ON_TME[4:0] × 64 ms 00000b = 0 × 64 ms 11111b = 31 × 64 ms

8.5.1.3.55 LEDC_CTRL1 Register (Offset = 57h) [reset = 00h]

LEDC_CTRL1 is shown in Table 8-196 and described in Table 8-197.

Return to Summary Table.

Register is reset on a POR event.

Table 8-196. LEDC_CTRL1 Register

7	6	5	4	3	2	1	0
RSVD		LEDC_RAMP_ENABLE	RSVD	LEDC_CURRENT[3:0]			
R-00b		R/W-0b	R-0b	R/W-0000b			

Table 8-197. LEDC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Unused bit read returns 0b.
5	LEDC_RAMP_ENABLE	R/W	0b	0b = No ramp 1b = Ramp enabled
4	RSVD	R	0b	Unused bit
3-0	LEDCA_CURRENT[3:0]	R/W	0000b	LEDC DC current. See Table 8-218

8.5.1.3.56 LEDC_CTRL2 Register (Offset = 58h) [reset = 00h]

LEDC_CTRL2 is shown in Table 8-198 and described in Table 8-199.

Return to Summary Table.

Register is reset on a POR event.

Table 8-198. LEDC_CTRL2 Register

7	6	5	4	3	2	1	0
RSVD	LEDC_T1[6:0]						
R-0b	R/W-0000000b						

Table 8-199. LEDC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDC_T1[6:0]	R/W	0000000b	LEDC T1 sequence length = LEDC_T1[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.57 LEDC_CTRL3 Register (Offset = 59h) [reset = 00h]

LEDC_CTRL3 is shown in Table 8-200 and described in Table 8-201.

Return to Summary Table.

Register is reset on a POR event.

Table 8-200. LEDC_CTRL3 Register

7	6	5	4	3	2	1	0
RSVD	LEDC_T2[6:0]						
R-0b	R/W-0000000b						

Table 8-201. LEDC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDC_T2[6:0]	R/W	0000000b	LEDC T2 sequence length = LEDC_T2[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.58 LEDC_CTRL4 Register (Offset = 5Ah) [reset = 00h]

LEDC_CTRL4 is shown in Table 8-202 and described in Table 8-203.

Return to Summary Table.

Register is reset on a POR event.

Table 8-202. LEDC_CTRL4 Register

7	6	5	4	3	2	1	0
RSVD	LEDC_T3[6:0]						
R-0b	R/W-0000000b						

Table 8-203. LEDC_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDC_T3[6:0]	R/W	0000000b	LEDC T3 sequence length = LEDC_T3[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.59 LEDC_CTRL5 Register (Offset = 5Bh) [reset = 00h]

LEDC_CTRL5 is shown in Table 8-204 and described in Table 8-205.

Return to Summary Table.

Register is reset on a POR event.

Table 8-204. LEDC_CTRL5 Register

7	6	5	4	3	2	1	0
RSVD	LEDC_T4[6:0]						
R-0b	R/W-0000000b						

Table 8-205. LEDC_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDC_T4[6:0]	R/W	0000000b	LEDC T4 sequence length = LEDC_T4[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.60 LEDC_CTRL6 Register (Offset = 5Ch) [reset = 00h]

LEDC_CTRL6 is shown in Table 8-206 and described in Table 8-207.

Return to Summary Table.

Register is reset on a POR event.

Table 8-206. LEDC_CTRL6 Register

7	6	5	4	3	2	1	0
RSVD	LEDC_TP[6:0]						
R-0b	R/W-0000000b						

Table 8-207. LEDC_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6-0	LEDC_TP[6:0]	R/W	0000000b	LEDC TP sequence length = LEDC_TP[6:0] × 64 ms 0000000b = 0 × 64 ms 1111111b = 127 × 64 ms

8.5.1.3.61 LEDC_CTRL7 Register (Offset = 5Dh) [reset = 00h]

LEDC_CTRL7 is shown in Table 8-208 and described in Table 8-209.

Return to Summary Table.

Register is reset on a POR event.

Table 8-208. LEDC_CTRL7 Register

7	6	5	4	3	2	1	0
RSVD			LEDC_PWM[4:0]				
R-000b			R/W-00000b				

Table 8-209. LEDC_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDC_PWM[4:0]	R/W	00000b	LEDC_ON duty-cycle: ([LEDC_PWM] +1) × 1 / 32 × 8-ms period 00000b = 1 / 32 × 8 ms (LEDC_ON is high for 250 µs, low for 7.75 ms) 11111b = 32 / 32 × 8 ms (LEDC_ON is always high)

8.5.1.3.62 LEDC_CTRL8 Register (Offset = 5Eh) [reset = 00h]

LEDC_CTRL8 is shown in Table 8-210 and described in Table 8-211.

Return to Summary Table.

Register is reset on a POR event.

Table 8-210. LEDC_CTRL8 Register

7	6	5	4	3	2	1	0
RSVD			LEDC_ON_TIME[4:0]				
R-000b			R/W-00000b				

Table 8-211. LEDC_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LEDC_ON_TIME[4:0]	R/W	00000b	LEDC ON-TIME: LEDC_ON_TME[4:0] × 64 ms 00000b = 0 × 64 ms 11111b = 31 × 64 ms

8.5.1.3.63 LED_RAMP_UP_TIME Register (Offset = 5Fh) [reset = 00h]

LED_RAMP_UP_TIME is shown in Table 8-212 and described in Table 8-213.

Return to Summary Table.

Register is reset on a POR event.

Table 8-212. LED_RAMP_UP_TIME Register

7	6	5	4	3	2	1	0
RSVD			LED_RAMP_UP[4:0]				
R-000b			R/W-00000b				

Table 8-213. LED_RAMP_UP_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LED_RAMP_UP[4:0]	R/W	00000b	LED ramp up time for LEDA, LEDB and LEDC: LED_RAMP_UP[4:0] × 8 ms 00000b = 0 × 8 ms 11111b = 31 × 8 ms

8.5.1.3.64 LED_RAMP_DOWN_TIME Register (Offset = 60h) [reset = 00h]

LED_RAMP_DOWN_TIME is shown in Table 8-214 and described in Table 8-215.

Return to Summary Table.

Register is reset on a POR event.

Table 8-214. LED_RAMP_DOWN_TIME Register

7	6	5	4	3	2	1	0
RSVD			LED_RAMP_DOWN[4:0]				
R-000b			R/W-00000b				

Table 8-215. LED_RAMP_DOWN_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Unused bit read returns 0b.
4-0	LED_RAMP_DOWN[4:0]	R/W	00000b	LED ramp-down time for LEDA, LEDB and LEDC: LED_RAMP_DOWN[4:0] × 8 ms 00000b = 0 × 8 ms 11111b = 31 × 8 ms

8.5.1.3.65 LED_SEQ_EN Register (Offset = 61h) [reset = 00h]

LED_SEQ_EN is shown in Table 8-216 and described in Table 8-217.

Return to Summary Table.

Register is reset on a POR event.

Table 8-216. LED_SEQ_EN Register

7	6	5	4	3	2	1	0
RSVD	LEDA_EN	LEDB_EN	LEDC_EN	RSVD	LEDA_SEQ_EN	LEDB_SEQ_EN	LEDC_SEQ_EN
R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-217. LED_SEQ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Unused bit read returns 0b.
6	LEDA_EN	R/W	0b	0b = LEDA is disabled 1b = LEDA is enabled
5	LEDB_EN	R/W	0b	0b = LEDB is disabled 1b = LEDB is enabled
4	LEDC_EN	R/W	0b	0b = LEDC is disabled 1b = LEDC is enabled
3	RSVD	R	0b	Unused bit
2	LEDA_SEQ_EN	R/W	0b	0b = LEDA sequencer is disabled 1b = LEDA sequencer is enabled
1	LEDB_SEQ_EN	R/W	0b	0b = LEDB sequencer is disabled 1b = LEDB sequencer is enabled
0	LEDC_SEQ_EN	R/W	0b	0b = LEDC sequencer is disabled 1b = LEDC sequencer is enabled

8.5.1.3.66 LEDx DC current

Table 8-218. LEDx DC current

LEDx_CURRENT[3:0]	LED CURRENT (mA)
0000b	2
0001b	4
0010b	6
0011b	8
0100b	10
0101b	12
0110b	14
0111b	16
1000b	18
1001b	20
1010b to 1111b	20

8.5.1.3.67 LOADSWITCH (Offset = 62h) [reset = OTP]

LOADSWITCH is shown in Table 8-219 and described in Table 8-220.

Return to Summary Table.

Register is reset on a POR event.

Table 8-219. LOADSWITCH Register

7	6	5	4	3	2	1	0
RSVD				ILIM[1:0]		ENABLE[1:0]	
R-0000b				R/W-OTP		R/W-X	

Table 8-220. LOADSWITCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSVD	R	0000b	Unused bit read returns 0b.
3-2	ENABLE[1:0]	R/W	OTP	00b = Load switch is OFF 01b = Load switch is forced ON 10b = Load switch in bypass switch operation: It is automatically enabled by comparators in DCDC4; forced PWM mode of DCDC4 is blocked and the bypass switch is disabled (ENABLE[1:0] is set to 00b) if the voltage on the VDCDC4 pin exceeds typically 4.18 V 11b = Load switch in bypass switch operation: Switch is forced ON; forced PWM mode of DCDC4 is blocked and the bypass switch is disabled (ENABLE[1:0] is set to 00b) if the voltage on the VDCDC4 pin exceeds typically 4.18 V
1-0	ILIM[1:0]	R/W	X	ENABLE[1] reset value is set by the EN_LS1 pin. ENABLE[0] reset value is set by the EN_LS0 pin. 00b = Current limit is 100 mA maximum 01b = Current limit is 500 mA maximum 10b = Current limit is 750 mA ±10% 11b = Current limit is 2.5 A ±20%

8.5.1.3.68 SPARE Register (Offset = 63h) [reset = OTP]

SPARE is shown in Table 8-221 and described in Table 8-222.

Return to Summary Table.

Register is reset on a POR event.

Table 8-221. SPARE Register

7	6	5	4	3	2	1	0
SPARE[3:0]				9MHZ OSC OFF	DCDC4_ SEL DELAY	DCDC4_ IMMEDIATE	CLK32k_ OD_EN
R/W-OTP				R/W-OTP	R/W-OTP	R/W-OTP	R/W-OTP

Table 8-222. SPARE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SPARE[3:0]	R/W	OTP	Unused bit read returns 0b.
3	9 MHz OSC OFF	R/W	OTP	0b = 9-MHz oscillator enabled in ON state 1b = 9-MHz oscillator is disabled based on the PWR_REQ and CLK_REQ1 pins as listed below: PWR_REQ = 0b and CLK_REQ1 = 0b: oscillator OFF PWR_REQ = 0b and CLK_REQ1 = 1b: oscillator ON PWR_REQ = 1b and CLK_REQ1 = 0b: oscillator ON PWR_REQ = 1b and CLK_REQ1 = 1b: oscillator ON
2	DCDC4_SEL DELAY	R/W	OTP	0b = DELAY is (0.5 to 1.5) × (1 / 32 kHz) for a falling output voltage 1b = NO DELAY on the DCDC4_SELbit
1	DCDC4_IMMEDIATE	R/W	OTP	0b = A voltage change in registers DCDC4_OP or DCDC4_AVS is done with the slew rate defined in DCDC4_CTRL:TSTEP[2:0] 1b = A voltage change in registers DCDC4_OP or DCDC4_AVS is done immediately without limiting it by the slew rate control
0	CLK32K_OD_EN	R/W	OTP	0b = 32KCLKOUT is configured as a push-pull output to VDDIO 1b = 32KCLKOUT is configured as an open drain output

8.5.1.3.69 VERNUM (Offset = 64h) [reset = OTP]

VERNUM is shown in Table 8-223 and described in Table 8-224.

Return to Summary Table.

Register is reset on a POR event.

Table 8-223. VERNUM Register

7	6	5	4	3	2	1	0
OTP_VERSION[7:4]				VERNUM[3:0]			
R-OTP				R-OTP			

Table 8-224. VERNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OTP_VERSION[7:4]	R	OTP	Value varies based on OTP.

Table 8-224. VERNUM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	VERNUM[3:0]	R	OTP	Value depending on silicon revision 00000000b = Revision 1.0 00000001b = Revision 1.1 00000010b = Revision 1.2 00000011b = Revision 1.3 00000100b = Revision 1.4 00000101b = Revision 1.5

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS659128x device is an integrated power-management integrated circuit (PMIC) that comes in an 81-pin, 0.4-mm pitch, DSBGA package. This device was designed for personal electronics, industrial, and communication applications and is typically powered from a 5-V input supply. The device provides four step-down converters along with an interface to control ten external LDO regulators. The device can support a variety of different processors and applications. The step-down converters can also support dynamic voltage scaling (DVS) through a dedicated I^2C interface to provide optimum power savings. In addition to the power resources, the device contains an embedded power controller (EPC) to manage the power sequencing requirements of systems. The power sequencing is programmable through OTP memory. The device also contains five configurable GPIOs and three LED drivers. The following sections provide the typical application use-case with the recommended external components and layout guidelines.

9.2 Typical Application

The first item to evaluate is the use of the CONFIG1 and CONFIG2 pins. For more information on implementing a device in a given system, refer to the application report for a specific orderable part number.

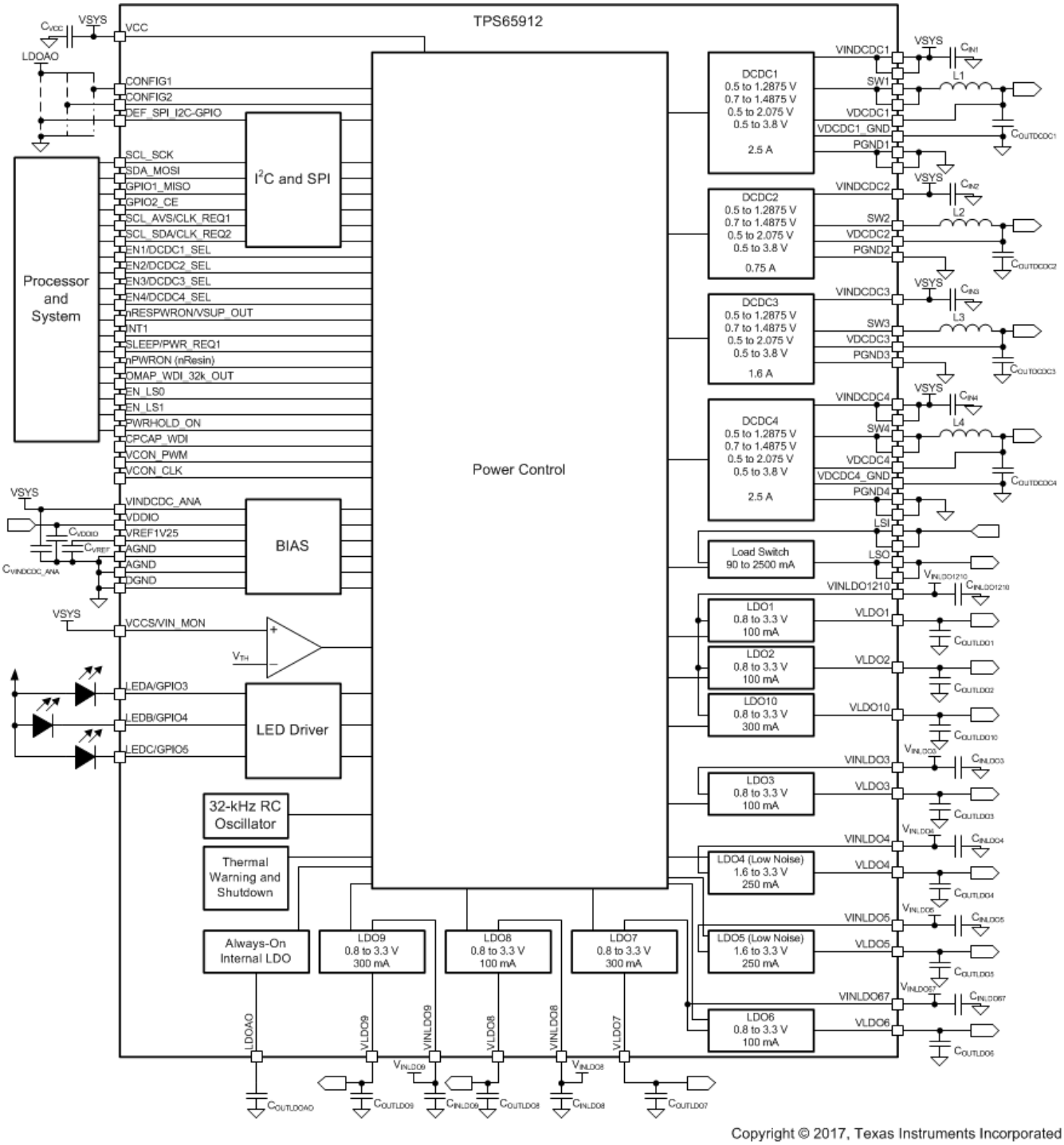


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

For a typical application shown in Figure 9-1, Table 9-1 lists sample key design parameters of the power resources. Voltages and currents will vary based on the application use case, the provided values are just an example.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	2.7 V to 5.5 V
Switching frequency	Up to 3.5 MHz
DCDC1 voltage	1.1 V
DCDC1 current	Up to 2.5 A
DCDC2 voltage	2.0 V
DCDC2 current	Up to 0.75 A
DCDC3 voltage	3.2 V
DCDC3 current	Up to 1.6 A
DCDC4 voltage	3.6 V
DCDC4 current	Up to 2.5 A
LDO1 voltage	850 mV or 900 mV
LDO1 current	Up to 100 mA
LDO2 voltage	850 mV or 900 mV
LDO2 current	Up to 100 mA
LDO3 voltage	1.2 V
LDO3 current	Up to 100 mA
LDO4 voltage	1.7 V or 1.8 V
LDO4 current	Up to 250 mA
LDO5 voltage	2.7 V
LDO5 current	Up to 250 mA
LDO6 voltage	1.8 V or 3.0 V
LDO6 current	Up to 100 mA
LDO7 voltage	3.0 V
LDO7 current	Up to 300 mA
LDO8 voltage	3.1 V
LDO8 current	Up to 100 mA
LDO9 voltage	3.0 V
LDO9 current	Up to 300 mA
LDO10 voltage	1.8 V
LDO10 current	Up to 300 mA

9.2.2 Detailed Design Procedure

Table 9-2 lists the recommended external components.

Table 9-2. Recommended External Components

REFERENCE COMPONENTS	COMPONENT(1)	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE(4)	SIZE (mm)	MASS PRODUCTION(2)
INPUT POWER SUPPLIES EXTERNAL COMPONENTS							
C_{VCC}, $C_{VINDCDC\_ANA}$	Power input capacitors	Murata	GRM188R71A225KE15	2.2 µF, 10 V	0603	1.6 × 0.8 × 0.8	Available(3)
C_{VDDIO}	I/O input capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available(3)
RGB LED EXTERNAL COMPONENTS							

Table 9-2. Recommended External Components (continued)

REFERENCE COMPONENTS	COMPONENT(1)	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE(4)	SIZE (mm)	MASS PRODUCTION(2)
LEDA	Yellow LED	Lite On	LTST-C190YKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (3)
LEDB	Green LED	Lite On	LTST-C190GKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (3)
LEDC	Red LED	Lite On	LTST-C190CKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (3)
DCDC EXTERNAL COMPONENTS							
C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4}	Input capacitor	Murata	GRM188R60J106ME47	10 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available (3)
$C_{OUTDCDC1}$, $C_{OUTDCDC4}$	Output capacitor	Murata	GCM32ER70J476KE19 (Two capacitors per rail)	10 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available (3)
$C_{OUTDCDC2}$, $C_{OUTDCDC3}$	Output capacitor	Murata	GRM188R60J106ME47	10 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available (3)
L1, L2, L3, L4	Inductor	Toko	1239AS-H-1R0N=P2	1 µH		2 × 2.5	Available(3)
LDO EXTERNAL COMPONENTS							
$C_{INLDO1210}$, C_{INLDO3}, $C_{INLDO67}$, C_{INLDO8}, C_{INLDO9}	Input capacitor	Murata	GRM188R71A225KE15	2.2 µF, 10 V	0603	1.6 × 0.8 × 0.8	Available(3)
C_{INLDO4}, C_{INLDO5}	Input capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available(3)
$C_{OUTLDO3}$, $C_{OUTLDO1}$, $C_{OUTLDO2}$, $C_{OUTLDO6}$, $C_{OUTLDO7}$, $C_{OUTLDO8}$, $C_{OUTLDO9}$, $C_{OUTLDO10}$, $C_{OUTLDOAO}$	Output capacitor	Murata	GRM188R71A225KE15	2.2 µF, 10 V	0603	1.6 × 0.8 × 0.8	Available(3)
$C_{OUTLDO4}$, $C_{OUTLDO5}$	Output capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3 V	0603	1.6 × 0.8 × 0.8	Available(3)
C_{VREF}	Output capacitor	Murata	GRM033R60J224ME15D	220 nF, 6.3 V	0201	0.6 × 0.3 × 0.33	Available

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.
(2) This column refers to the criteria.
(3) Component used on the validation boards.
(4) The PACK column describes the external component package type.

9.2.2.1 Output Filter Design (Inductor and Output Capacitor)

9.2.2.1.1 Inductor Selection

The step-down converters are designed to operate with small external components such as 1-µH output inductors. The values given in the *Recommended Operating Conditions* (see Section 6.3) include tolerances and saturation effects and must not be violated for stable operation. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductor will directly influence the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Use Equation 3 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This recommendation is because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (2)$$

where

- ΔI_L is the peak-to-peak inductor ripple current.
- L is the inductor value.
- f is the switching frequency.

$$I_{Lmax} = I_{OUTmax} \times \frac{\Delta I_L}{2} \quad (3)$$

where

- I_{Lmax} is the maximum inductor current.

The highest inductor current will occur at the maximum input voltage, V_{IN}.

Open-core inductors have a soft saturation characteristic and they can usually support higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor-current rating just for the maximum switch current of the corresponding converter. The core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies, and therefore the core material must be considered when selecting an inductor.

For possible inductors, refer to Table 9-3 and Table 9-2.

Table 9-3. Tested Inductors

INDUCTOR TYPE	NOMINAL INDUCTANCE	SUPPLIER
DFE252012	1 µH	Toko
DFE322510	1 µH	Toko
DFE322512	1 µH	Toko
VLS201612ET-1R0	1 µH	TDK
SPM3012T-1R0	1 µH	TDK

9.2.2.1.2 Output Capacitor Selection

The control scheme of the DC-DC converters allow the use of small ceramic capacitors with a typical value as given in the *Recommended Operating Conditions* (see Section 6.3), without having a large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values which result in the lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the RMS ripple-current rating of the capacitor ($I_{RMSCOUT}$) always meets the application requirements. Use Equation 4 to calculat the RMS ripple current.

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At the nominal load current, the inductive converters operate in PWM mode and the overall output-voltage ripple is the sum of the voltage spike caused by the ESR of the output capacitor plus the voltage ripple caused by charging and discharging the output capacitor. Use Equation 5 to calculate the output-voltage ripple (ΔV_{OUT}).

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (5)$$

The highest output voltage ripple occurs at the highest input voltage, V_{IN}.

At light load currents, the converters operate in power save mode and the output-voltage ripple is dependent on the value of the output capacitor. The output-voltage ripple is set by the internal comparator delay and the external capacitor. The typical output-voltage ripple is less than 1% of the nominal output voltage.

9.2.2.1.3 Input Capacitor Selection and Input Voltage

Because of the nature of the step-down converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. The converters require a ceramic input capacitor of 10 µF. The value of the input capacitor can be increased without any limit for better input voltage filtering. Ceramic capacitors suffer from the so-called *DC bias effect*. A DC voltage applied at a ceramic capacitor will change the effective capacitance to a value lower than the nominal value. Curves about that behavior are available from the capacitor manufacturers and must be considered when using the capacitors in applications where a DC voltage is applied and a minimum capacitance must be maintained for proper functionality of the circuit. The values given in the *Recommended Operating Conditions* for the TPS659128x device are for the capacitance; however, the actual capacitor used may have a larger nominal value that drops with the voltage applied to what is recommended. The capacitance drop depends on the voltage applied, therefore, higher voltages, such as the output voltage of a DC-DC converter or LDO, must be considered when choosing a proper capacitor.

The input voltage for the step-down converters must be connected to the VINDCDC1, VINDCDC2, VINDCDC3, and VINDCDC4 pins. These pins must be tied together with the VINDCDC_ANA pin to the power source. The VCC pin must be tied to the highest voltage in the system. If the load switch is used as a switch on the output, the VCC pin must be tied to the input voltage of the VINDCDCx and VINDCDC_ANA pins. If the load switch is used as a current limited switch on the input, the VCC pin must be connected to the LSI pin while the LSO pin is connected to the VINDCDCx and VINDCDC_ANA pins. The four step-down converters must not be supplied from different input voltages.

9.2.2.1.4 Output Capacitor Table

The DC-DC converters are designed for an output capacitance as given in the *Recommended Operating Conditions* (see Section 6.3). A ceramic capacitor, such as a X5R or X7R type, is required at the output. Table 9-4 lists capacitors used for the TPS659128x device.

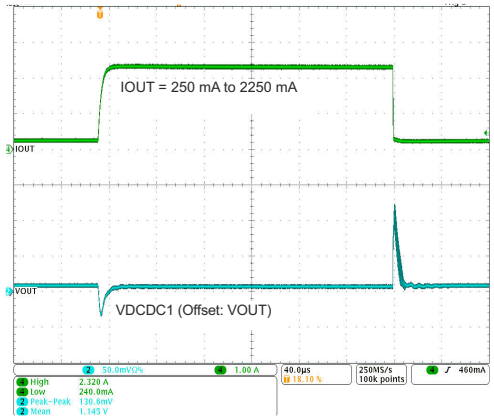
Table 9-4. Example Capacitors

VALUE	SIZE	SUPPLIER	MATERIAL AND RATING
47 µF / 6.3 V	0805	Murata GRM21BR60J476ME15	Ceramic X5R
22 µF / 6.3 V	0805	Murata GRM21BR60J226M	Ceramic X5R
10 µF / 10 V	0603	Murata GRM188R61A106ME69	Ceramic X5R
4.7 µF / 6.3 V	0603	Murata GRM188R60J475KE19	Ceramic X5R
4.7 µF / 6.3 V	0402	Murata GRM155R60J475ME87	Ceramic X5R

9.2.2.1.5 Voltage Change on DCDC1 to DCDC4

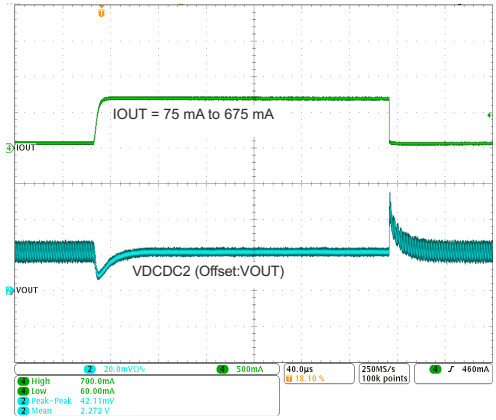
The output voltage of the DC-DC converters can be changed during operation by either the digital interfaces, by toggling the DCDCx_SEL pin, or by entering SLEEP state if the resources are configured to change voltage based on the device state.

9.2.3 Application Curves



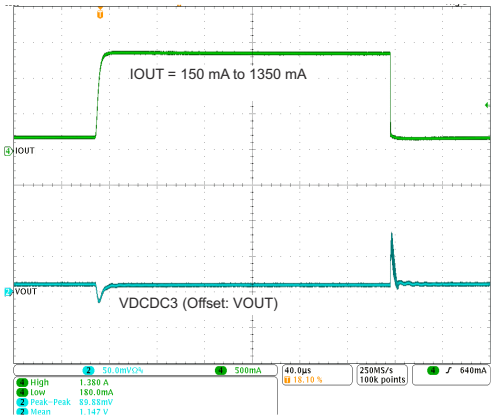
V_{IN} = 3.6 V V_O = 1.1375 V

Figure 9-2. DCDC1 Load Transient Response



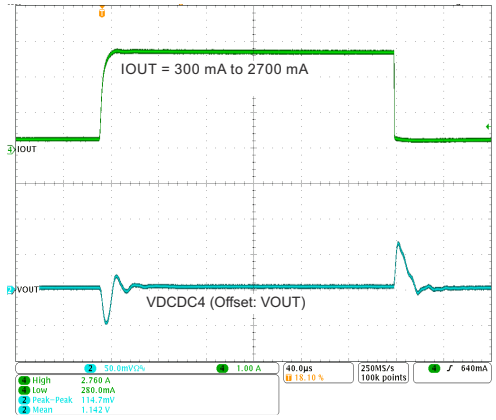
V_{IN} = 3.6 V V_O = 2.25 V

Figure 9-3. DCDC2 Load Transient Response



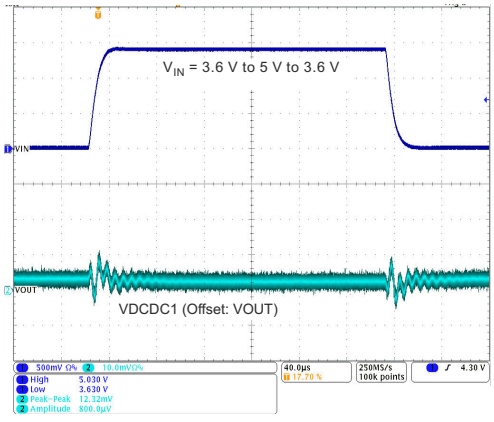
V_{IN} = 3.6 V V_O = 1.1375 V

Figure 9-4. DCDC3 Load Transient Response



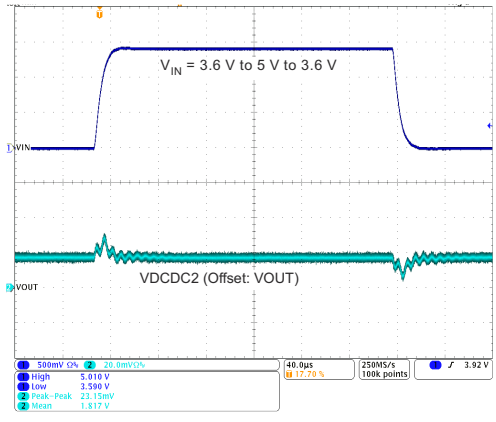
V_{IN} = 3.6 V V_O = 1.1375 V

Figure 9-5. DCDC4 Load Transient Response



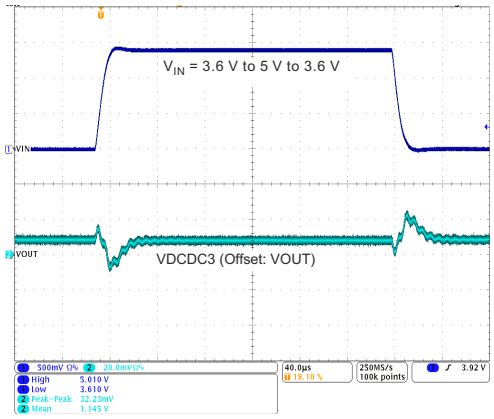
V_O = 1.1375 V I_O = 2500 mA

Figure 9-6. DCDC1 Line Transient Response



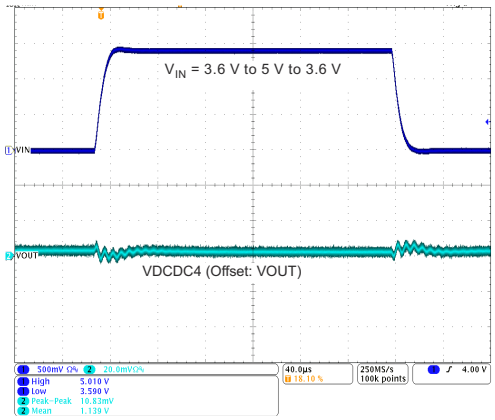
V_O = 1.8 V I_O = 750 mA

Figure 9-7. DCDC2 Line Transient Response



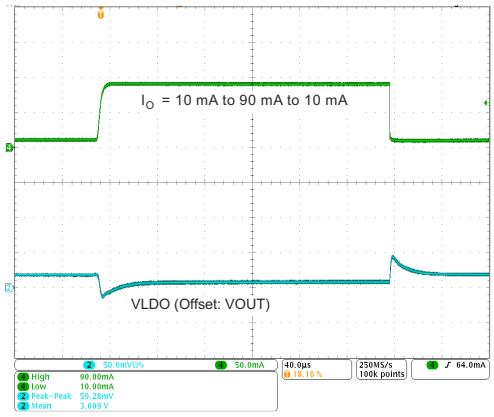
V_O = 1.1375 V I_O = 1500 mA

Figure 9-8. DCDC3 Line Transient Response



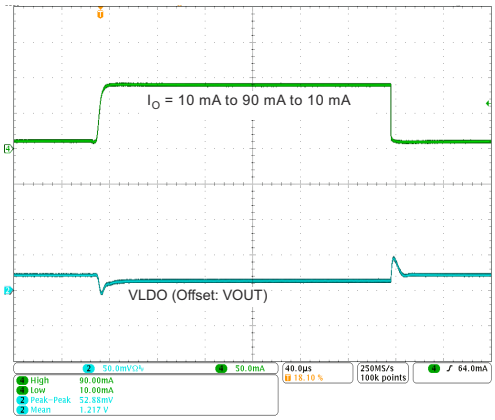
V_O = 1.1375 V I_O = 3000 mA

Figure 9-9. DCDC4 Line Transient Response



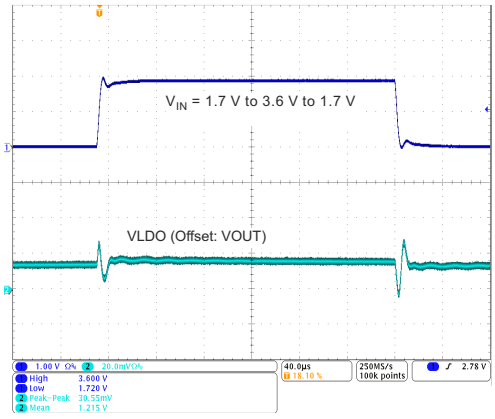
V_{IN} = 3.3 V V_O = 3 V

Figure 9-10. LDO1, LDO2, LDO3 Load Transient Response



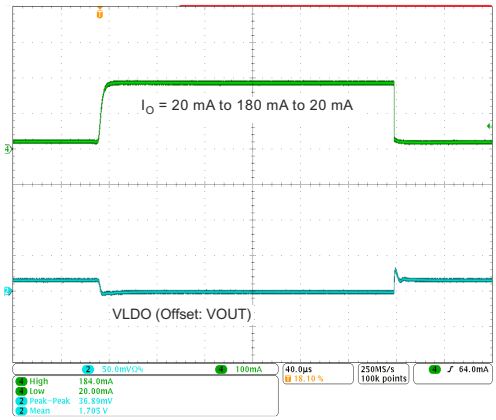
V_{IN} = 1.8 V V_O = 1.2 V

Figure 9-11. LDO1, LDO2, LDO3 Load Transient Response



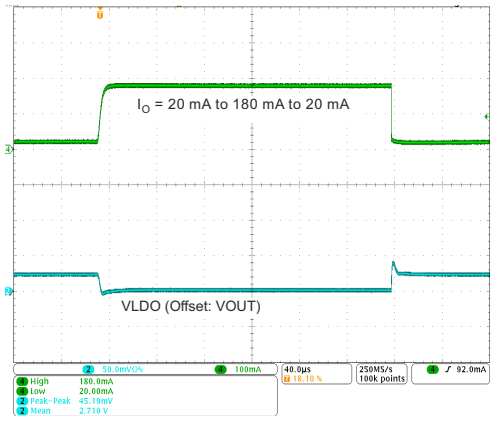
I_O = 100 mA V_O = 1.2 V

Figure 9-12. LDO1, LDO2, LDO3 Line Transient Response



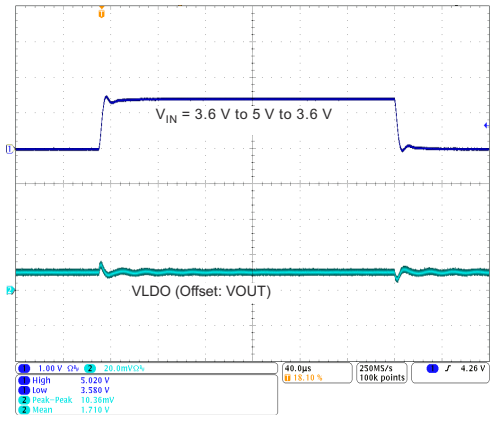
V_{IN} = 2 V V_O = 1.7 V

Figure 9-13. LDO4, LDO5 Load Transient Response



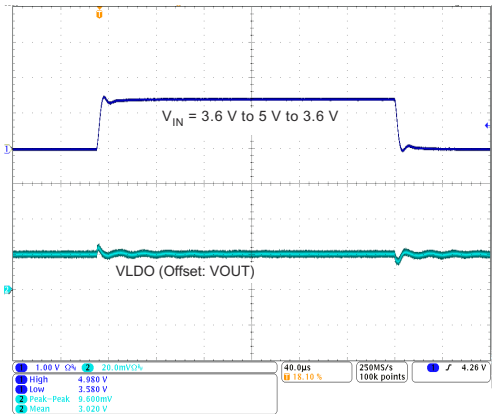
V_{IN} = 3.2 V V_O = 2.7 V

Figure 9-14. LDO4, LDO5 Load Transient Response



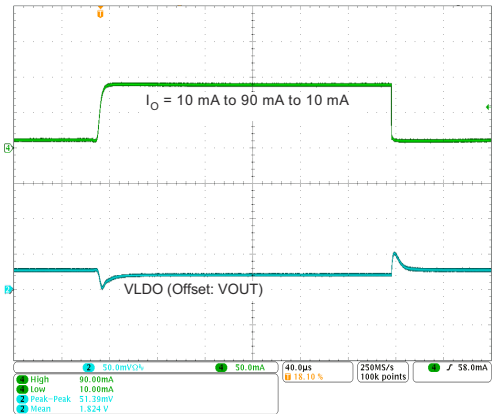
I_O = 100 mA V_O = 1.7 V

Figure 9-15. LDO4, LDO5 Line Transient Response



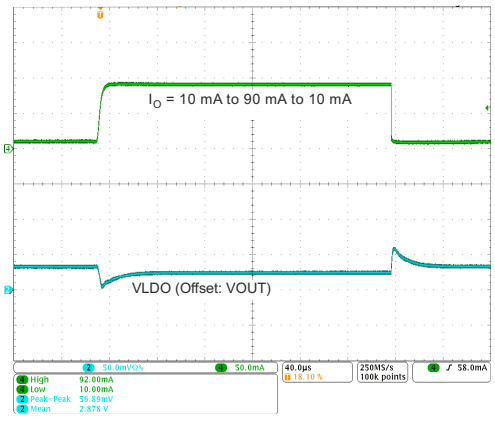
I_O = 100 mA V_O = 3 V

Figure 9-16. LDO4, LDO5 Line Transient Response



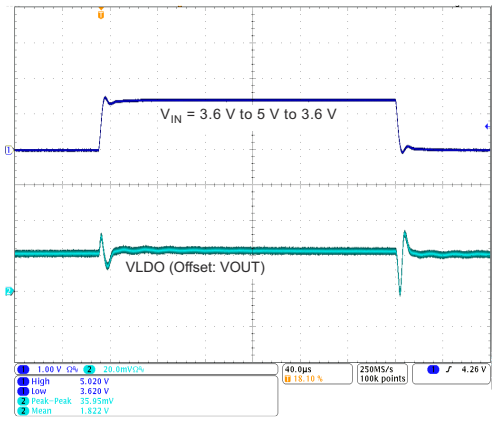
V_{IN} = 3.3 V V_O = 1.8 V

Figure 9-17. LDO6, LDO8 Load Transient Response



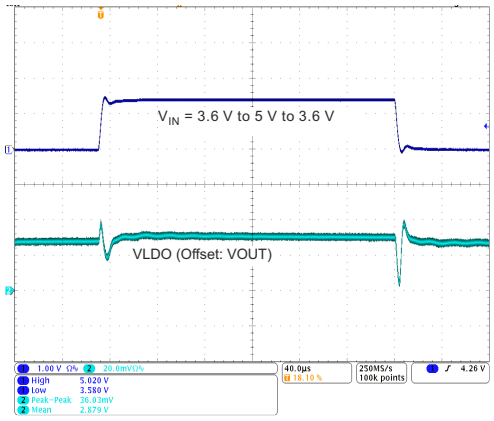
V_{IN} = 3.3 V V_O = 2.85 V

Figure 9-18. LDO6, LDO8 Load Transient Response



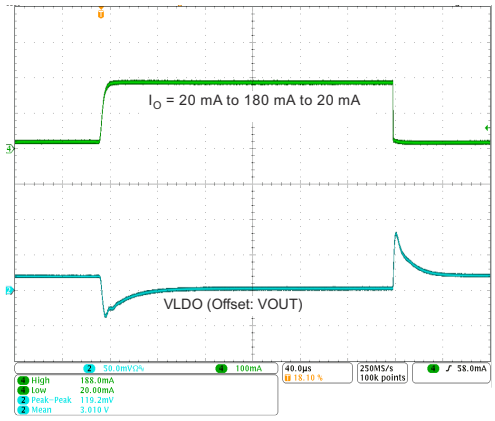
I_O = 100 mA V_O = 1.8 V

Figure 9-19. LDO6, LDO8 Line Transient Response



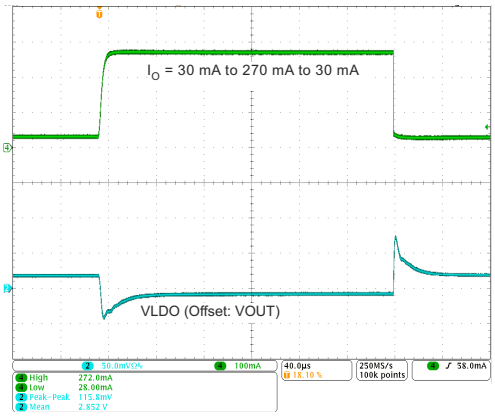
I_O = 100 mA V_O = 2.85 V

Figure 9-20. LDO6, LDO8 Line Transient Response



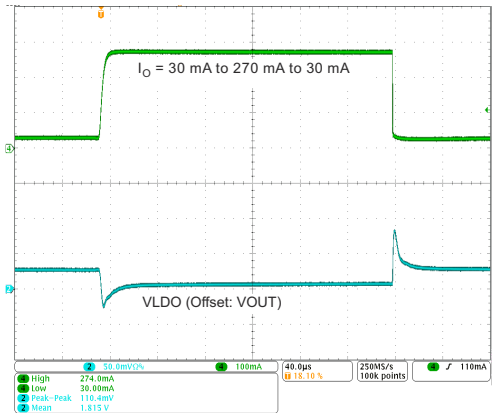
V_{IN} = 3.2 V V_O = 3 V

Figure 9-21. LDO7 Load Transient Response



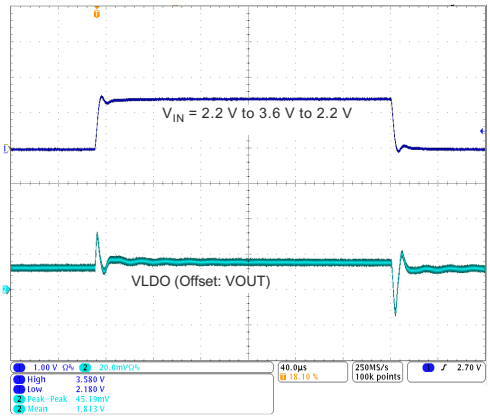
V_{IN} = 3.3 V V_O = 2.85 V

Figure 9-22. LDO9 Load Transient Response



V_{IN} = 3.3 V V_O = 1.8 V

Figure 9-23. LDO10 Load Transient Response



I_O = 300 mA V_O = 1.8 V

Figure 9-24. LDO10 Line Transient Response

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper functionality of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line regulation, load regulation, or both and stability issues, as well as EMI problems. Providing a low-impedance ground path is critical. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the device pins as well as the inductor and output capacitor.

Keep the common path to the GND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx trace should be connected directly to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, L3, and L4 traces).

The most critical connections are:

- PGNDx
- VDCDCx (positive output-voltage sense connection)
- VDCDCx_GND (ground-sense connection)
- AGND
- VINDCDCx, VINDCDC_ANA, VCC

The PGNDx pins are the ground connections of the power stages, so they will carry high DC-peak and AC-peak currents. A low impedance connection to the GND plane is required, which must be independent from other pins to not couple noise into other pins. Other pins must not be connected to PGNDx pins.

The VDCDCx pins are the positive-sense connections for the feedback loop. The connection must be made directly to the positive terminal pad of the output capacitor. Do not tie the pin to the pad of the output inductor or anywhere in between the inductor and capacitor. Shielding the connection by GND traces or a GND plane is a best practice.

The VDCDCx_GND pin is a sense connection for GND and is only available for the DCDC1 and DCDC4 convertors. The connection can be made either to the GND pad of the output capacitor (preferred) or to the GND plane directly if a solid connection of the GND-plane to the output capacitor exists. The pin must not be connected to the PGNDx pins as this will couple switching noise into the feedback loop.

The AGND (analog ground) pin is the main GND connection for internal analog circuitry. A proper connection must be made to a GND plane directly by a via. The AGND and DGND pins (located next to each other) can be connected and a via each be used to the GND plane.

The VINDCDCx, VINDCDC_ANA, and VCC pins are supply-voltage-input terminals and must be properly bypassed by their input capacitors. The required capacitance is given in the *Recommended Operating Conditions* (see Section 6.3). As ceramic capacitors will change their capacitance based on the voltage applied, temperature and age, the influence of these parameters must be considered when choosing the value of a capacitor. The input capacitors are ideally placed on the same layer as the device, so the connection can be made short and directly on the same layer with multiple vias used from the GND terminal to the GND-plane.

For more information about the layout for the TPS659128x device, refer to the *TPS65912xEVM-081 User's Guide*.

10.2 Layout Example

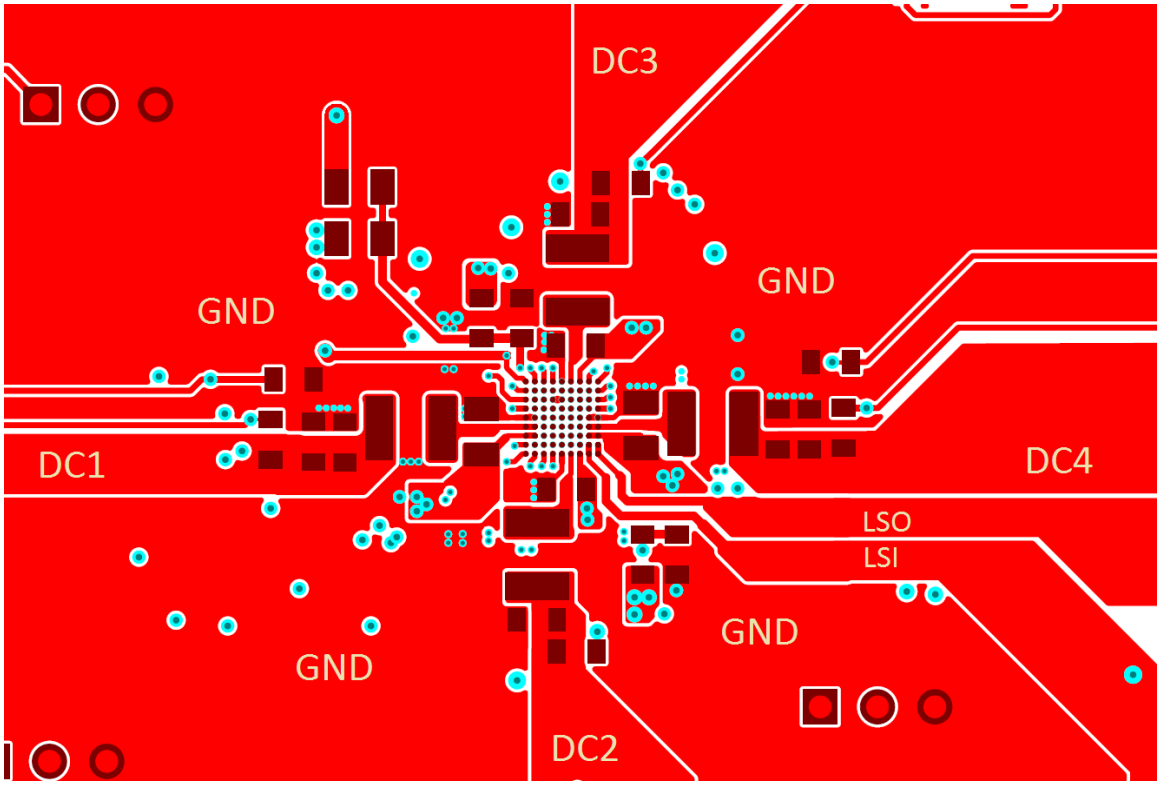


Figure 10-1. Layout Example

11 Power Supply Recommendations

The TPS659128x device is designed to work with an analog supply voltage range from 2.7 V to 5.5 V. The input supply should be well regulated and connected to the VCC pin, as well as the DCDC and LDO input pins. If the input supply is located more than a few inches from the device, additional capacitance may be required in addition to the recommended input capacitors at the VCC pin and the DCDC and LDO input pins.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the TPS659128x device applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any TPS659128x device application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TPS659128x platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage*
- Texas Instruments, *Empowering Designs With Power Management IC (PMIC) for Processor Applications* application report
- Texas Instruments, *TPS65912xEVM-081 User's Guide*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

Eco-mode™, Code Composer Studio™, DSP/BIOS™, and XDS™ are trademarks of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6591286YFFR	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	659128-6
TPS6591286YFFR.A	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	659128-6
TPS6591287YFFR	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	659128-7
TPS6591287YFFR.A	Active	Production	DSBGA (YFF) | 81	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	659128-7

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

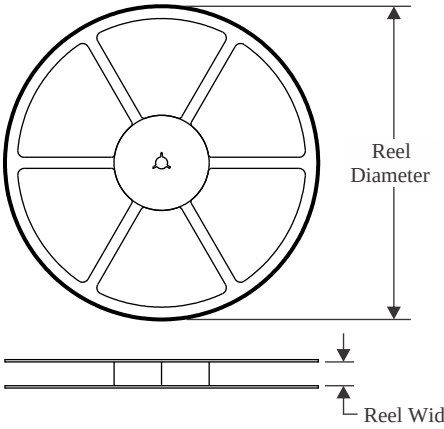
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

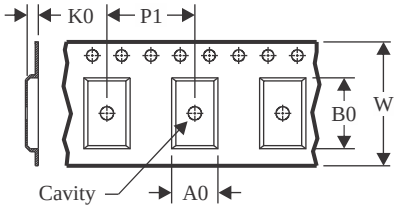
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

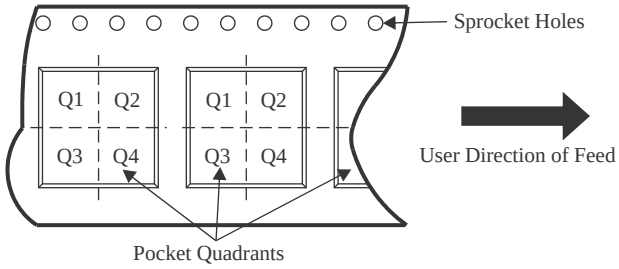


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

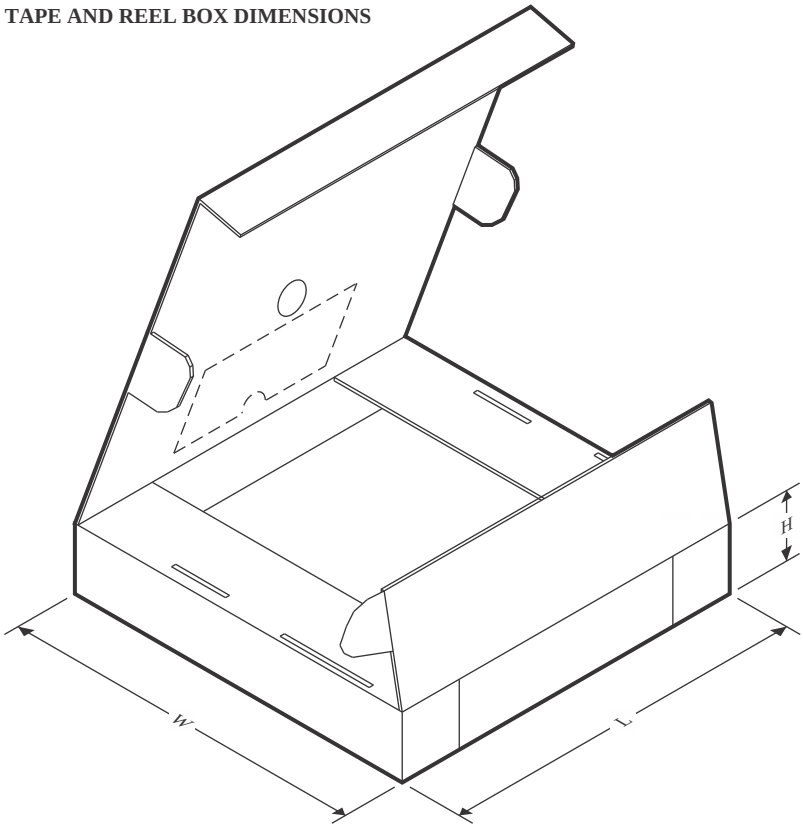
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6591286YFFR	DSBGA	YFF	81	3000	330.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS6591287YFFR	DSBGA	YFF	81	3000	330.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

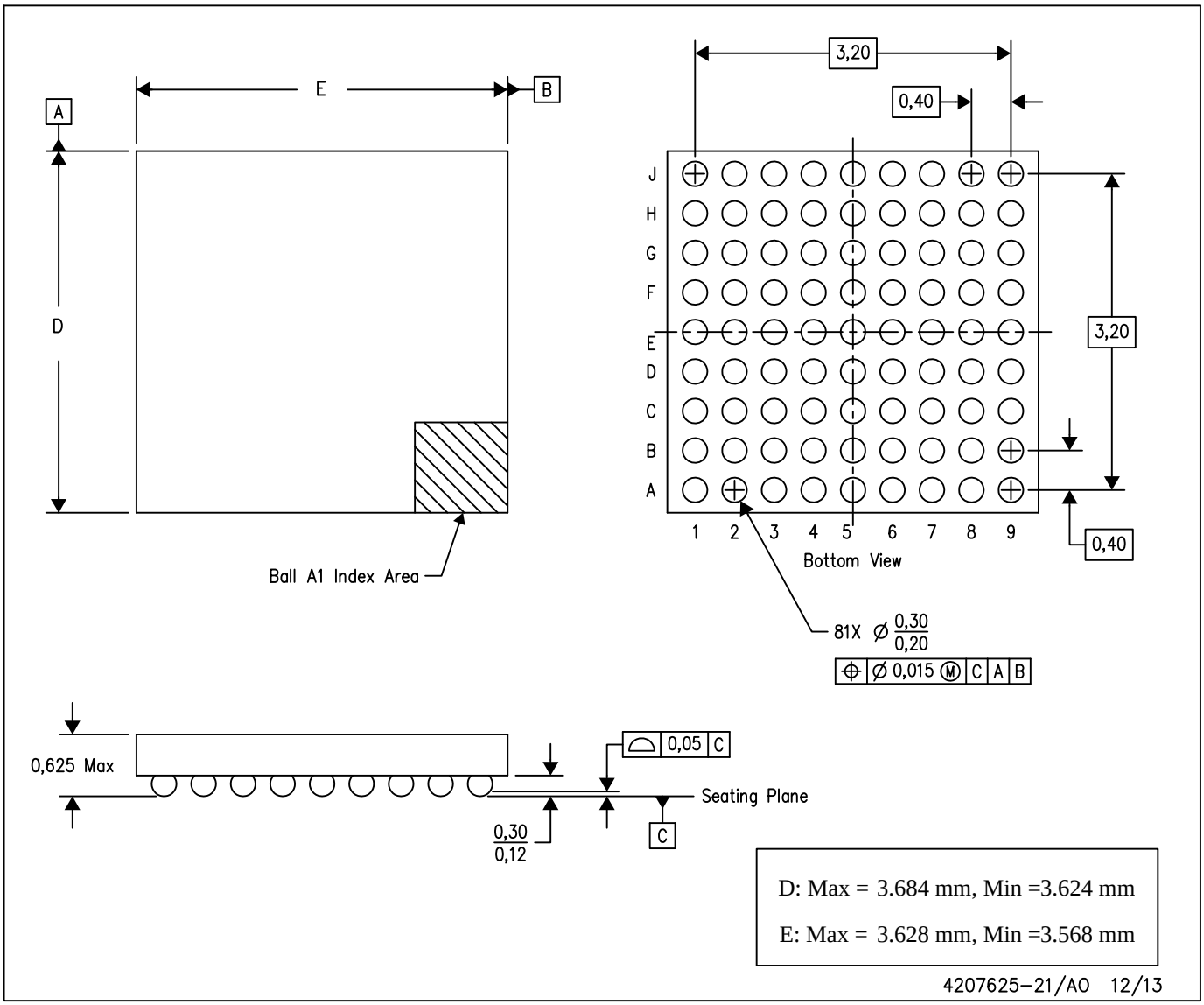
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6591286YFFR	DSBGA	YFF	81	3000	335.0	335.0	25.0
TPS6591287YFFR	DSBGA	YFF	81	3000	335.0	335.0	25.0

YFF (R–XBGA–N81) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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