12-V to 100-V Input, 0.2-A Output Switching Converter

Check for Samples: UCC25230

FEATURES

- **Highly Integrated Converter Operating as a Buck, or Isolated Forward-Flyback, Flybuck™**
- **Wide Operating Input Voltage Range from 12 V to 100 V, 105-V Surge.**
- **Up to 0.2-A Output Current**
- **9-V Always Available VDD Output with up to 2-mA Current Capability**
- **Thermally Enhanced 4-mm x 4-mm SON-8/S-PVSON-N8 (DRM) Package**
- **Internally Set Fixed 380-kHz Switching Frequency**
- **Internal 2-ms Duration Soft Start**
- **Voltage Mode Control with Input Feed Forward Allows Optimal Output Filter Design**
- **2% Accuracy Internal 2.5-V Reference**
- **V_{DD} UVLO**
- **Cycle-by-Cycle Current Limit with Frequency Fold Back for Initial Start up Under High Capacitive Loads**
- **Input UVLO and OVLO with Input Good Signal**
- **Integrated 110-V, High and Low-Side Switches**

APPLICATIONS

- **High Density Isolated Standby Bias Supplies**
- **DC-to-DC Converters**

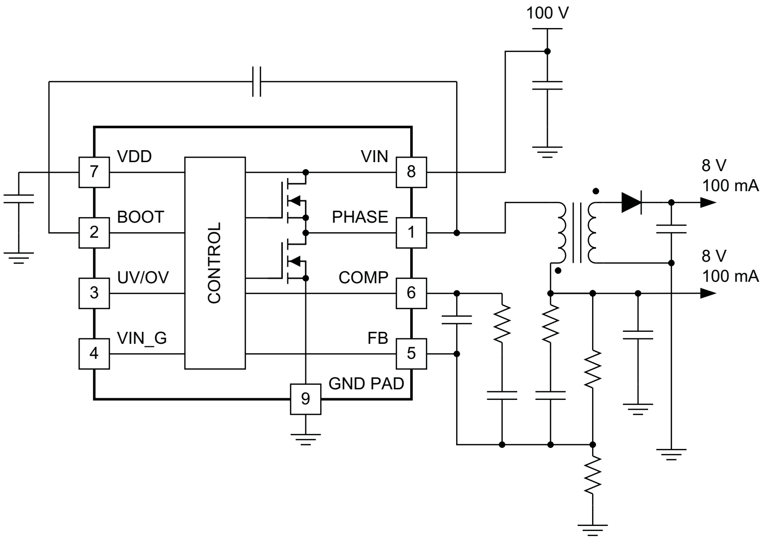
DESCRIPTION

The UCC25230 is a highly integrated PWM converter operating as an isolated forward flyback. It has high-side and low-side power switches integrated and the control circuit with all key converter functions included. The power stage requires only one- or multiple winding coupled inductor and output capacitors for the complete solution. Voltage-mode feed-forward control with external compensation allows optimal output filter selection over wide input voltage range. The UCC25230 has fixed frequency set internally at 380 kHz. It also includes input voltage UVLO and OVLO comparators with hysteresis and input-good, open-collector output signal which can be used to enable PWM controllers.

UCC25230 is available in a thermally enhanced 8-pin SON package with PowerPad™ serving as a ground pin.

Other features include internal soft start and cycle-by-cycle current protection. Measured efficiency of isolated converter over input voltage and output current ranges are shown in Figure 2.

Isolated Buck Converter



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad, Flybuck are trademarks of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

TEMPERATURE RANGE, $T_A = T_J$	PACKAGE	TAPE AND REEL QTY.	PART NUMBER
-40°C to +125°C	SON-8/S-PVSON-N8 (DRM)	250	UCC25230DRMT
		3000	UCC25230DRMR

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range, VIN	DC	-0.3	100	V
	Repetitive surge < 200 ms		105	
Output voltage on PHASE	DC	–0.3	VIN + 0.5	
	Repetitive pulse < 100 ns	-2	VIN + 1	
Voltage	BOOT with respect to PHASE	-0.3	10	
Voltage	VDD	-0.3	10	
Voltage	FB, UV/OV, COMP	-0.3	VDD	
Voltage	VIN_G	-0.3	5.5	
ESD rating	HBM		2	kV
	CDM		500	V
Sink current	PHASE (peak)		220 (internally limited)	mA
Source current	PHASE (peak)		-220 (internally limited)	
Operating virtual junction temperature range, T_J		-40	150	°C
Operating ambient temperature range, T_A		-40	125	
Storage temperature, T_{STG}		-65	150	
Lead temperature (soldering, 10 sec.)			300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

THERMAL INFORMATION

THERMAL METRIC(1)		UCC25230 DRM 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	33.2	
θ_{JB}	Junction-to-board thermal resistance(4)	11.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	11.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage range, VIN	12	48	75, (100 V for 1 ms)	V
Supply bypass capacitor, C_{VIN}		1.0		µF
Supply bypass capacitor, C_{VDD}	0.1	1.0	2.2	
Operating junction temperature range	-40		+125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 48 V, 1-µF capacitor from VIN to GND, 1-µF capacitor from VDD to GND, $T_A = T_J$ = -40°C to 125°C, (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Currents						
I_{VIN}	Quiescent current	V_{IN} = 5 V		0.5	2	mA
I_{VINO}	V_{IN} operating current	FB = COMP		4.5	10	
VDD Regulator						
V_{DD}	VDD, output voltage		8.46	9	9.54	V
	Line regulation	17 V < V_{IN} < 75 V		±5	±40	mV
	Load regulation	-2 mA < I_{VDD} < 0 mA		±5	±40	
	VDD current limit (when V_{DD} = 5.5 V)		-2	-6	-13	mA
Internal Undervoltage Lockout (V_{DD_UVLO})						
VDD_{rising}	VDD rising threshold		7.0	7.5	8	V
VDD_{hyst}	VDD threshold hysteresis		0.4	0.7	1.1	
$VDD_{falling}$	VDD falling threshold		6.3	6.8	7.3	
Undervoltage (external programmable)						
	Falling threshold		0.9	1.0	1.1	V
	Ihyst		7	11	18	µA
Overvoltage (external programmable)						
	OVLO Rising threshold		4.5	5	5.5	V
	Ihyst		-15	-22	-40	µA
VIN Power GOOD						
	PG output sink resistance	I_{PG} = 5 mA to 10 mA		50	100	Ω
Oscillator						
f	Oscillator frequency fixed		324	380	445	kHz
DC_{MIN}	Minimum duty cycle	FB = 3.0 V			0%	
DC_{MAX}	Maximum duty cycle	FB = 2.0 V	85%			
	Frequency variation	12 V < V_{IN} < 75 V	-15%		15%	

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 48 V, 1-µF capacitor from VIN to GND, 1-µF capacitor from VDD to GND, T_A = T_J = -40°C to 125°C, (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amplifier						
	REF voltage	FB = COMP, (T = 25°C)	2.42	2.50	2.58	V
		FB = COMP, (T = -40 to 125°C)	2.40	2.50	2.60	
Avol	Avol open loop voltage gain		40	80		dB
	Input leakage current, FB				±2	µA
$I_{COM(sink)}$	COMP sink current	V_{COMP} = 4.5 V	2	4.8	10	mA
$I_{COM(source)}$	COMP source current	V_{COMP} = 4.5 V	-2	-6.1	-12	
V_{OL}	COMP voltage range	I_{COMP} = 100 µA		.4	1.2	V
V_{OH}	COMP voltage range	I_{COMP} = -100 µA	VDD-1.2	VDD-0.7	VDD	
Soft Start						
	Time for COMP to ramp	FB = COMP	1.75	2.05	2.35	ms
Output						
	$R_{DS(on)}$ high	V_{IN} = 48 V		6	15	Ω
	$R_{DS(on)}$ low	V_{IN} = 48 V		5	10	
	Max average current			200		mA
ILIMIT (1)						
	ILIMIT phase high	V_{IN} = 30 V	-600	-400	-220	mA
	Propagation delay, blanking delay plus ILIMIT delay		60	100	140	ns
	ILIMIT phase low	V_{IN} = 30 V	220	400	600	mA
	Propagation delay, blanking delay plus ILIMIT delay (2)		60	100	140	ns

(1) Continued operation while in ILIM could exceed the maximum power dissipation for the device. For Non-Isolated applications additional external over current protection may be required.

(2) Specified by design, not production tested.

DEVICE INFORMATION

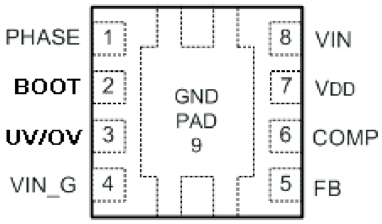


Figure 1.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PHASE	1	O	Phase output of high-side and low-side power FETs.
BOOT	2	I	0.1-µF capacitor connected between BOOT and PHASE pins along with the internal diode between BOOT and VDD provides supply voltage to the drive circuit of the upper power FET.
UV/OV	3	I	Input to internal comparators. Internal linear regulator remains functional. A bypass cap of at least 1000 pF is recommended.
VIN_G	4	O	VIN power good. Open drain output, state determined by UV/OV pin.
FB	5	I	Error amplifier inverting input. Connect to output voltage divider with compensation circuit to this pin.
COMP (1)	6	O	Output of error amplifier.
VDD	7	O	Output of internal linear regulator. Bypass VDD pin to GND pins close to device package with a high quality, low ESR 1-µF ceramic capacitor.
VIN	8	I	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to GND pins close to device package with a high quality, low ESR 1-µF ceramic capacitor.
GND PAD	9	-	Thermal ground pad and electrical ground for the device.

(1) Input feed forward control with RAMP magnitude V_{IN} x 6%.

Detailed Pin Description

PHASE (pin 1): Output of the internal high and low sides of the internal synchronous FETS. This output drives the external power inductor, or primary side of a coupled inductor for multiple outputs.

BOOT (pin 2): Connect a 0.1-µF capacitor between the BOOT pin and the PHASE pin. This provides the necessary level shift voltage to drive the internal upper FET gate.

UV/OV (pin 3): Input to the internal window comparator with a 1-V and 5-V reference. The input to the UV/OV pin determines the state of the open drain output of VIN_G. This does not determine the operating range of the UCC25230. A bypass cap at least 1000 pF is recommended for noise immunity.

VIN_G (pin 4): Open drain output of The UCC25230’s internal comparator. The output state is determined by the voltage on the UV/OV pin. The UCC25230 will continue to function regardless of the state of this pin. Used for controlling external circuitry. Maximum voltage to this pin is 5.5 V.

FB (pin 5): FB is the inverting input of the UCC25230’s internal error amplifier. Connect the output voltage sensing divider to this pin. Internal reference is 2.5 V on the non inverting input.

$$R2 = \left(\left(\frac{V_{OUT}}{2.5} \right) - 1 \right) \times R1 \tag{1}$$

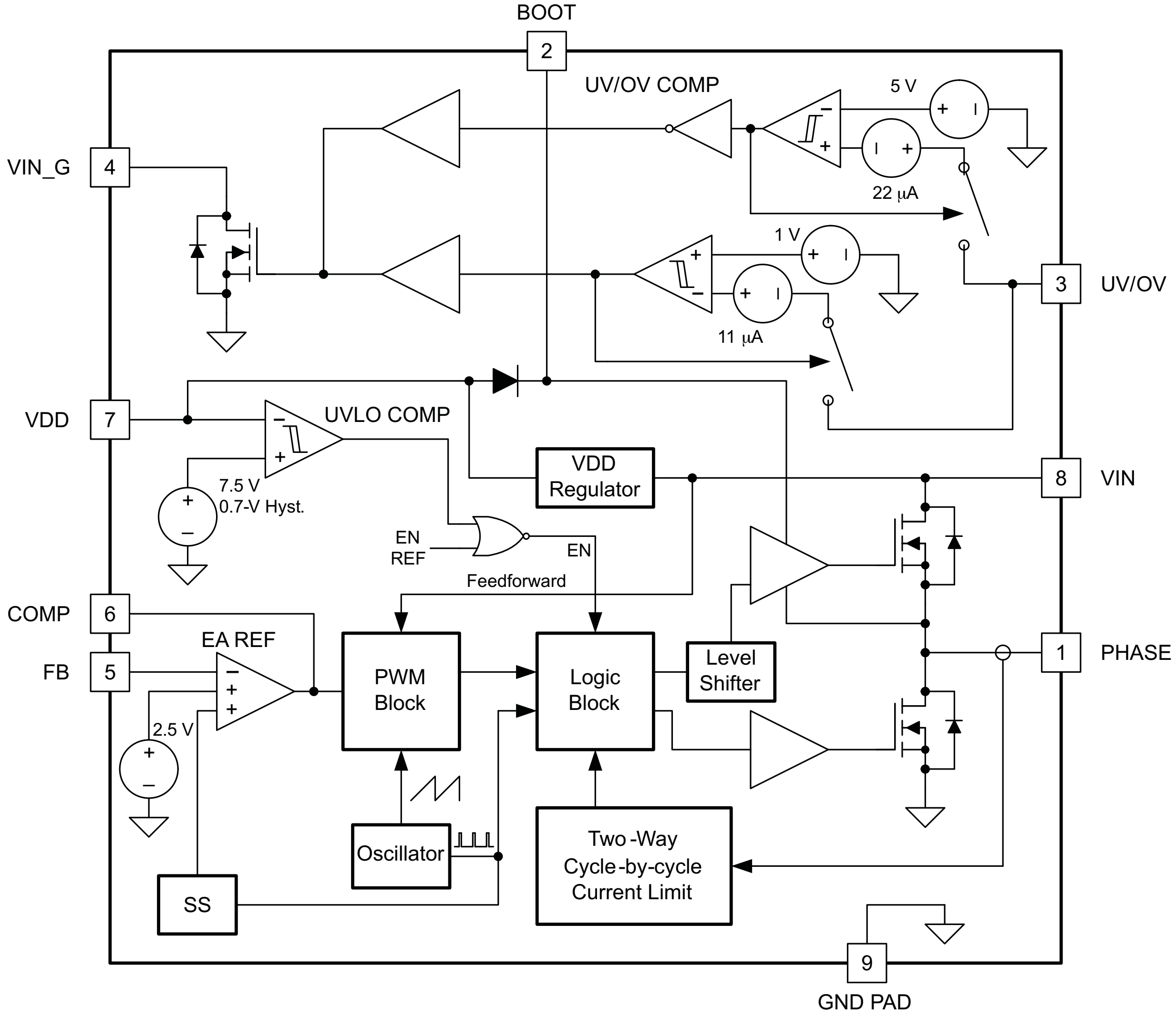
COMP (pin 6): The COMP pin is the internal error amplifier’s output. The voltage range of COMP is 0 V to 8.3 V. At steady state, a higher COMP pin voltage results in a larger duty cycle. Add compensation components between this pin and FB. The device has input feed forward control which makes PWM RAMP magnitude V_{IN} x 6%.

VDD (pin 7): This is the 9-V output of the UCC25230’s internal voltage regulator. This output may be used for powering additional circuitry, up to a current of 2 mA, depending on the voltage on the VIN pin. Care must be taken not to exceed the devices total power dissipation.

VIN (pin 8): This is the voltage input pin for the UCC25230. It supplies the internal voltage regulator and output switches. Bypass this pin with at least 1-µF low ESR capacitor.

GND PAD (pin 9): GND PAD is the ground reference for the whole device. Tie all signal returns to this point.

Functional Block Diagram



TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT POWER

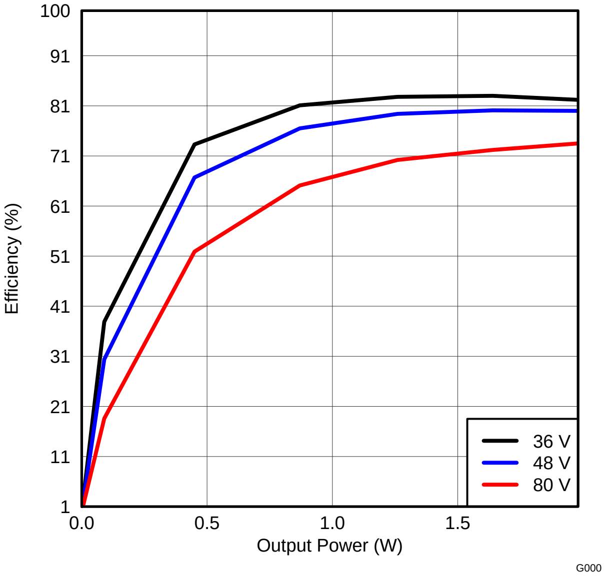


Figure 2.

OSCILLATOR CHANGE vs TEMPERATURE

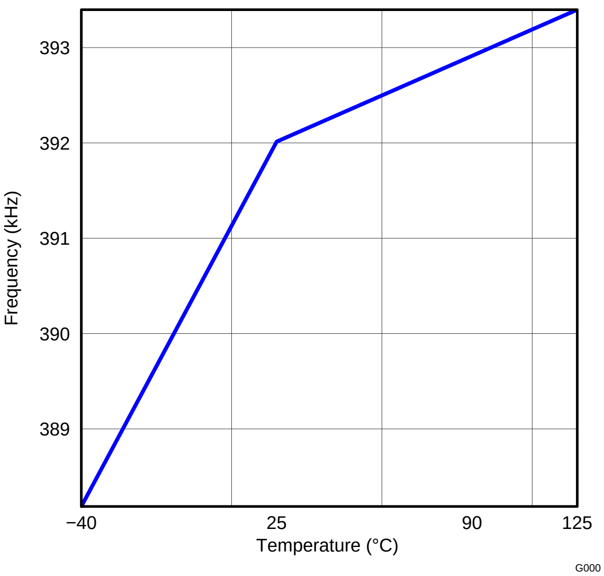


Figure 3.

OSCILLATOR CHANGE vs INPUT VOLTAGE

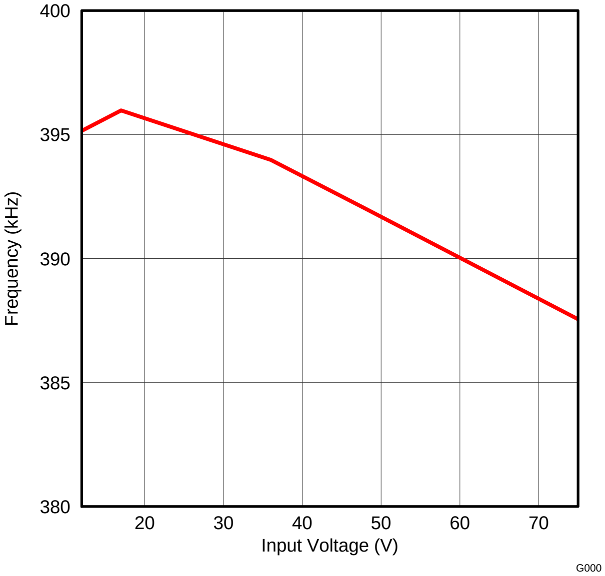


Figure 4.

SOFT-START TIME vs TEMPERATURE

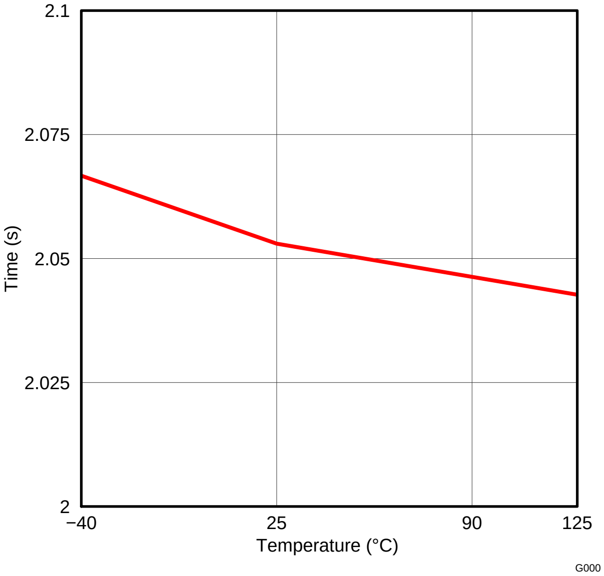


Figure 5.

TYPICAL CHARACTERISTICS (continued)

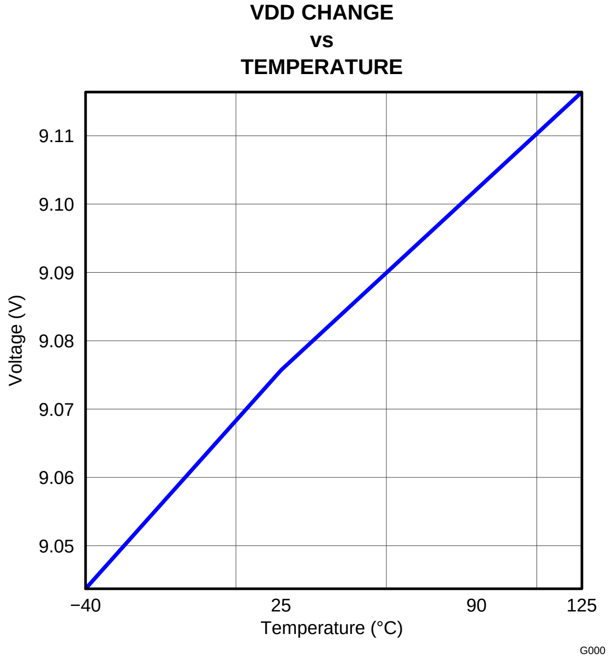


Figure 6.

APPLICATION INFORMATION

Detailed Description

The UCC25230 PWM converter integrates all necessary functions to operate as an isolated auxiliary bias supply. It is capable of operating from an input voltage range of 12 V to 100 V (up to 105-V surge), making it ideal for usage in 24-V or 48-V input telecom applications. High-side and low-side power switches are integrated and provide up to 200 mA of peak output current. The UCC25230 is an ideal, complementary solution to primary-side or secondary-side PWM control methodologies as it provides bias voltages necessary for PWM controllers and/or external peripheral circuitry. UCC25230 is capable of delivering a primary-side and/or secondary-side bias voltage for power supplies. As such, UCC25230 is optimized for Texas Instruments' family of UCD3k digital and analog PWM controllers as well as the C2000 family of microcontrollers.

UCC25230 operates using Texas Instruments' Flybuck™ Topology, which simplifies design versus a traditional flyback topology. FlybuckTM Topology allows a synchronous buck–like design methodology. It also enables a significant reduction in external parts count, and also allows usage of a small 2-winding transformer. The Flybuck™ Topology does not require a third transformer winding or opto-isolator for regulation. Circuits employing extra transformer windings compromise dynamic response, and add to the transformer's physical size and cost. The Flybuck™ is a portmanteau of flyback and buck since the transformer is connected as a flyback converter and the input to output voltage relationship is similar to a buck derived converter.

Typically, an auxiliary bias supply must be designed such that it is the first device in the system to power up, and be the very last device, in the system, to power down. It must be a robust supply, being able to ride through any fault conditions (OV, UV, OTP, etc) and it also must not prematurely shut down the entire power supply. The UCC25230 was designed with these goals in mind:

- A 2-ms soft start ensures a smooth, monotonic startup on both primary and secondary-side voltages.
- Voltage mode with input voltage feedforward allows optimal output filter design.
- Cycle-by-cycle current limit with frequency foldback permits startup under high-capacitive loading.
- Programmable UV/OV detection circuit.
- A VIN_G fault output provides a fast propagation open drain signal to indicate when an overvoltage or undervoltage condition has been detected. The UCC25230 is specifically designed to remain operational when a fault is detected in order to allow for fast external shutdown.

Operation of the Flybuck™ Converter

Figure 7 shows a simplified schematic and the two primary operational states of the Flybuck converter. The power supply is a variation of a Flyback converter and consists of a half bridge power stage S_{HS} and S_{LS}, transformer, primary side capacitor, diode and output capacitor. The output voltage is regulated indirectly by using the primary side capacitor voltage, V_{PRI}, as feedback. The Flybuck is a portmanteau of flyback and buck since the transformer is connected as a flyback converter and the input to output voltage relationship is similar to a buck derived converter, assuming the converter is operating in steady state and the transformer has negligible leakage inductance.

The C_{PRI} and L_{PRI} are charged by the input voltage source VIN during the time the high side switch S_{HS} is on. During this time, diode D1 is reversed biased and the load current is supplied by output capacitor C_O.

During the off time of S_{HS}, S_{LS} conducts and the voltage on C_{PRI} continues to increase during a portion of the S_{LS} conduction time. The voltage increase is due to the energy transfer from L_{PRI} to C_{PRI}. For the remaining portion of the S_{LS} conduction time, the C_{PRI} voltage decreases because of current in L_{PRI} reverses; see the IL_{PRI} and V_{PRI} waveforms in Figure 8. By neglecting the diode voltage drop, conduction dead time and leakage inductance, the input to output voltage conversion ratio can be derived as shown in Equation 2 from the flux balance in L_{PRI}. It can be seen in Equation 2 that the input to output relationship is the same as a buck-derived converter with transformer isolation. The dc voltage V_{PRI} on the primary side capacitor in Equation 3 has the same linear relationship to the input voltage as a buck converter.

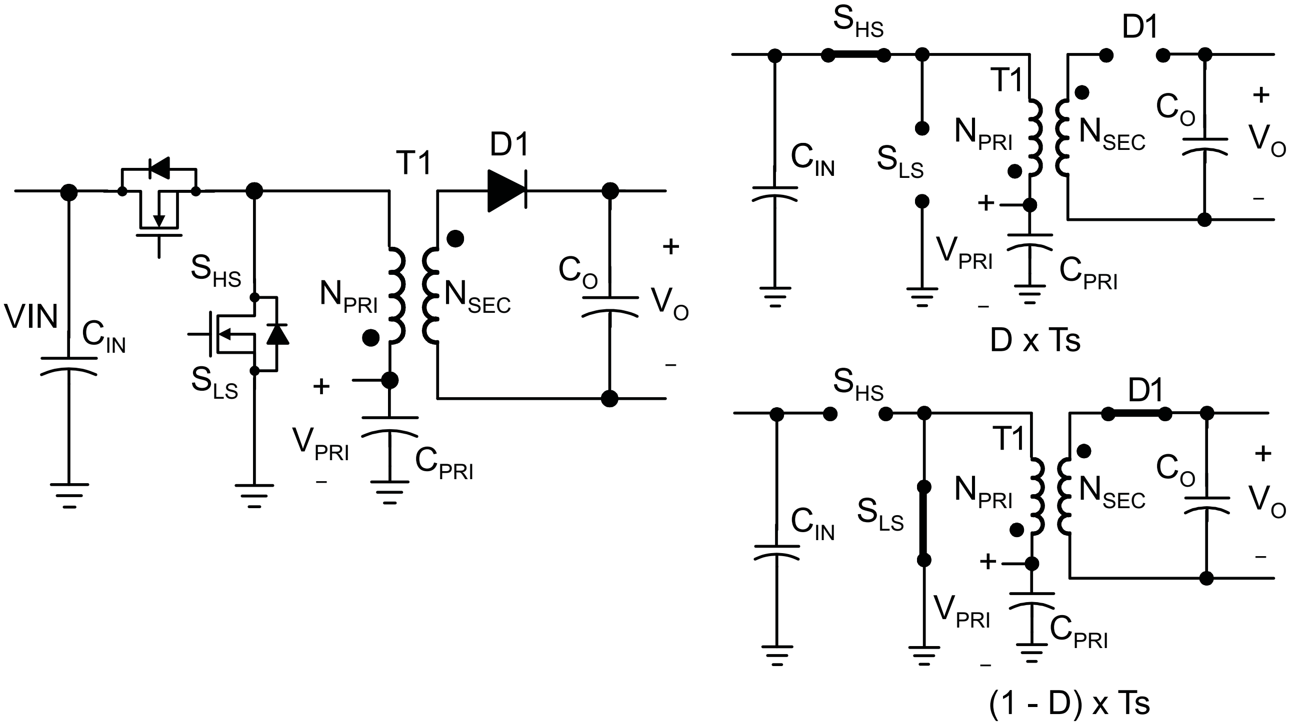


Figure 7. Simplified Schematic with Two Primary Operational States

The small signal model for the Flybuck is derived by changing the transformer to the inductor equivalent and reflecting the output filter to the primary side for the circuit shown in Figure 7. Assuming negligible leakage inductance and equivalent series resistance for the capacitors, the V_{PRI} transfer function is similar to the voltage mode control buck power stage transfer function with the exception that the C_O and load are in parallel with the C_{PRI} only for the 1-D time. The device has input feed forward control which makes PWM RAMP magnitude V_{IN} x 6%.

$$\frac{V_O}{V_{IN}} = \frac{N_{SEC}}{N_{PRI}} \times D \tag{2}$$

$$\frac{V_{PRI}}{V_{IN}} = D \tag{3}$$

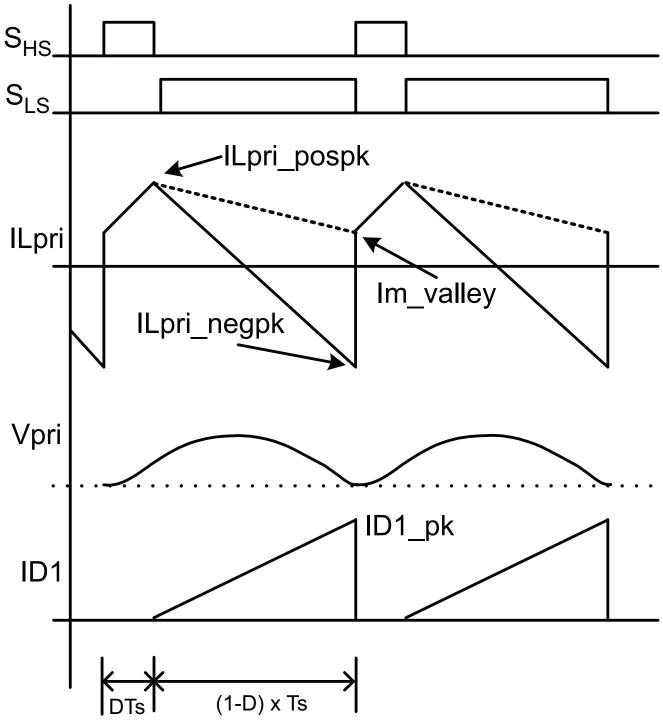


Figure 8. Simplified Voltage and Current Waveforms

Typical Application Diagram

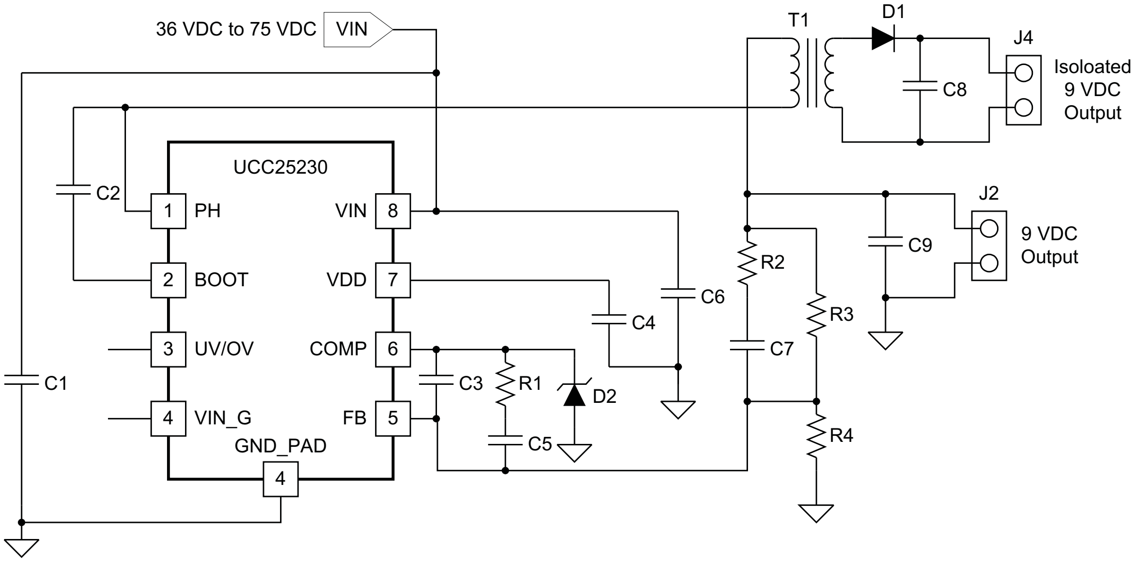


Figure 9. Typical Application Diagram

REVISION HISTORY

Changes from Revision A (November, 2011) to Revision B	**Page**
• Added Integrated 110-V High and Low-Side Switches feature bullet	1
• Added note, Input feed forward control with RAMP magnitude V_{IN} x 6%.	6
• Added COMP pin description, The device has input feed forward control which makes PWM RAMP magnitude V_{IN} x 6%.	7
• Deleted Averaging the secondary side components, an approximate transfer function is shown in and pole location in . R_O is the secondary side load resistance and the R_{LM} is the dc resistance of the primary. R_i is the inverse of the Comp to PH gm.	13
• Added The device has input feed forward control which makes PWM RAMP magnitude V_{IN} x 6%.	13

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC25230DRMR	Active	Production	VSON (DRM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	25230
UCC25230DRMR.A	Active	Production	VSON (DRM) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	25230
UCC25230DRMT	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	25230
UCC25230DRMT.A	Active	Production	VSON (DRM) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	25230

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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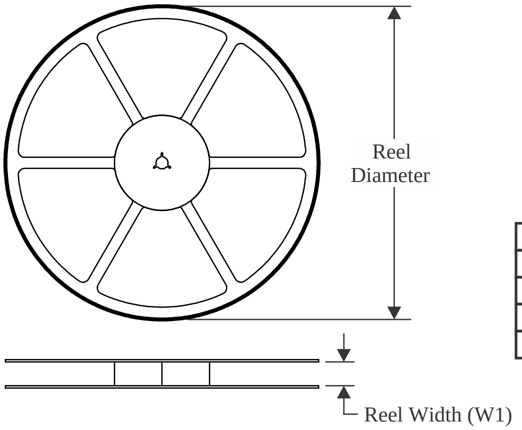
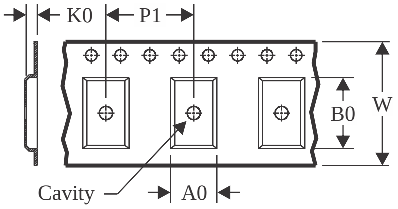
TAPE AND REEL INFORMATION

REEL DIMENSIONS

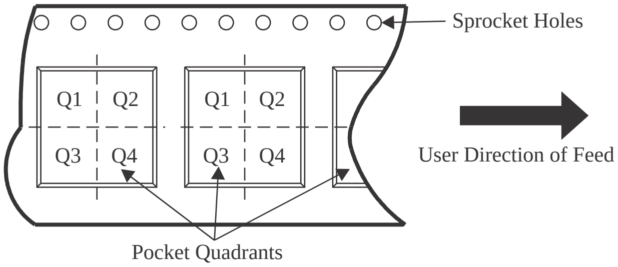


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

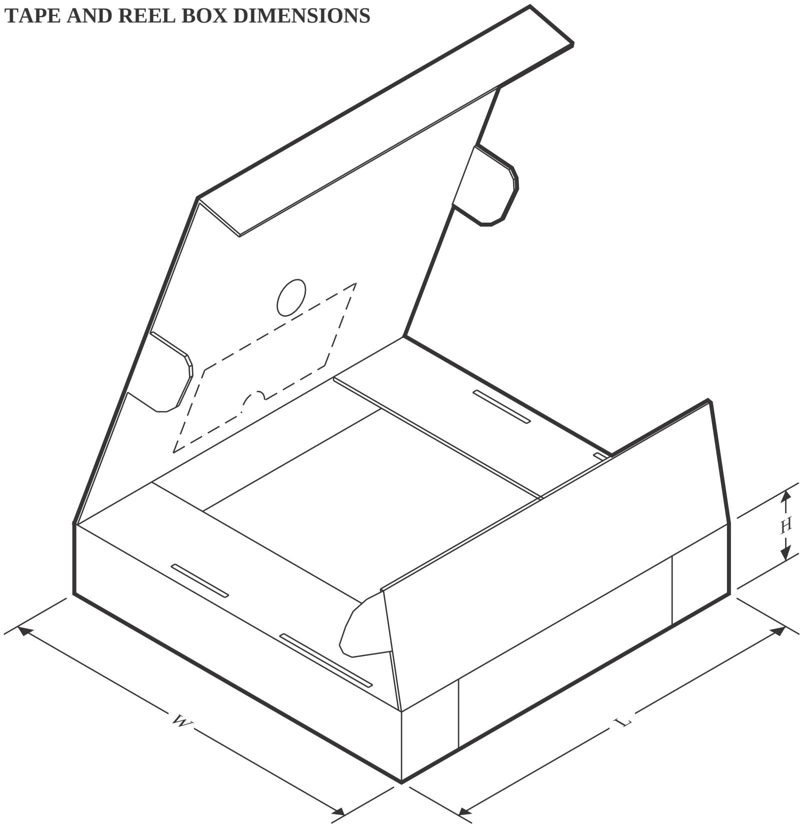
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

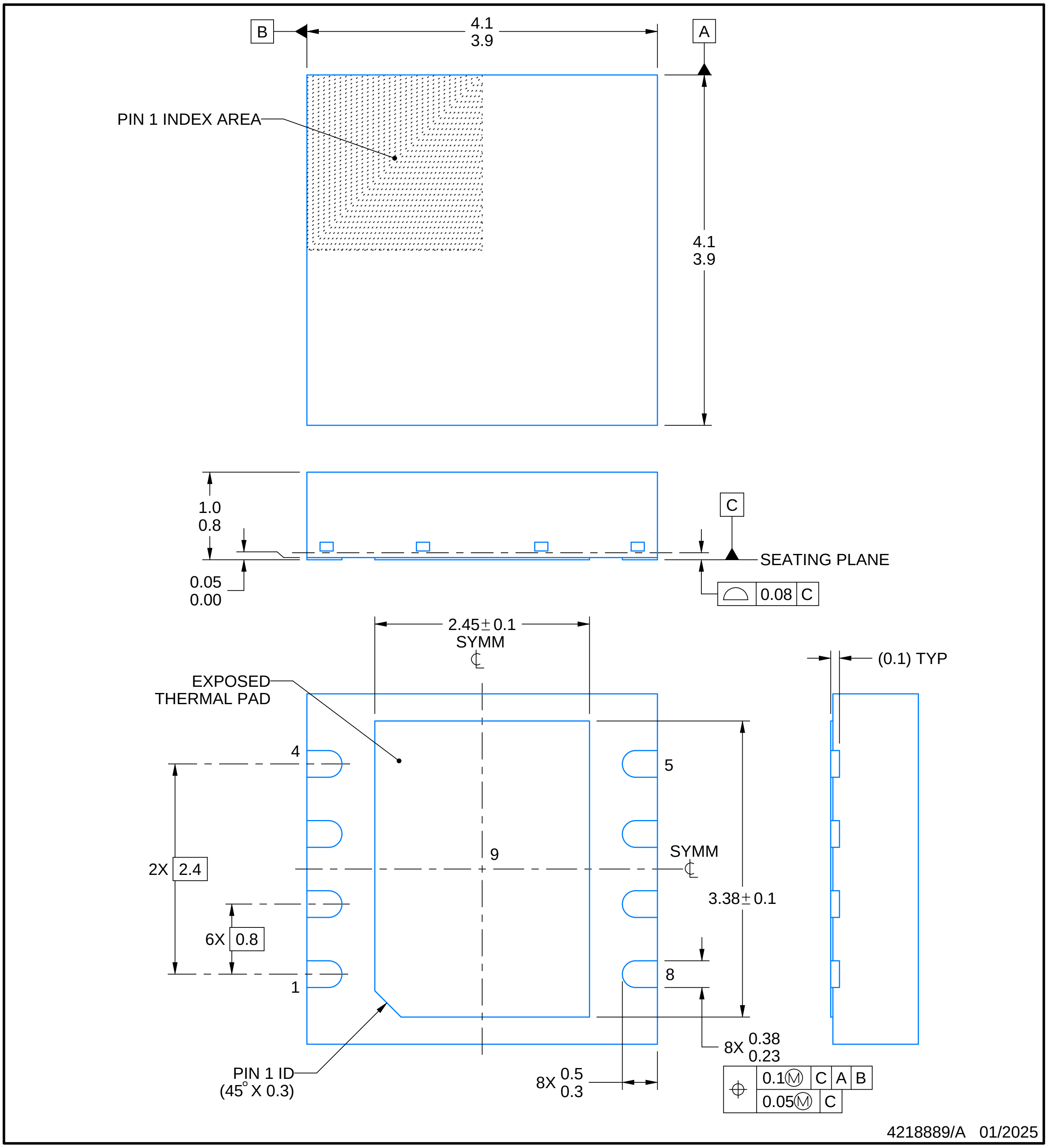
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25230DRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC25230DRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



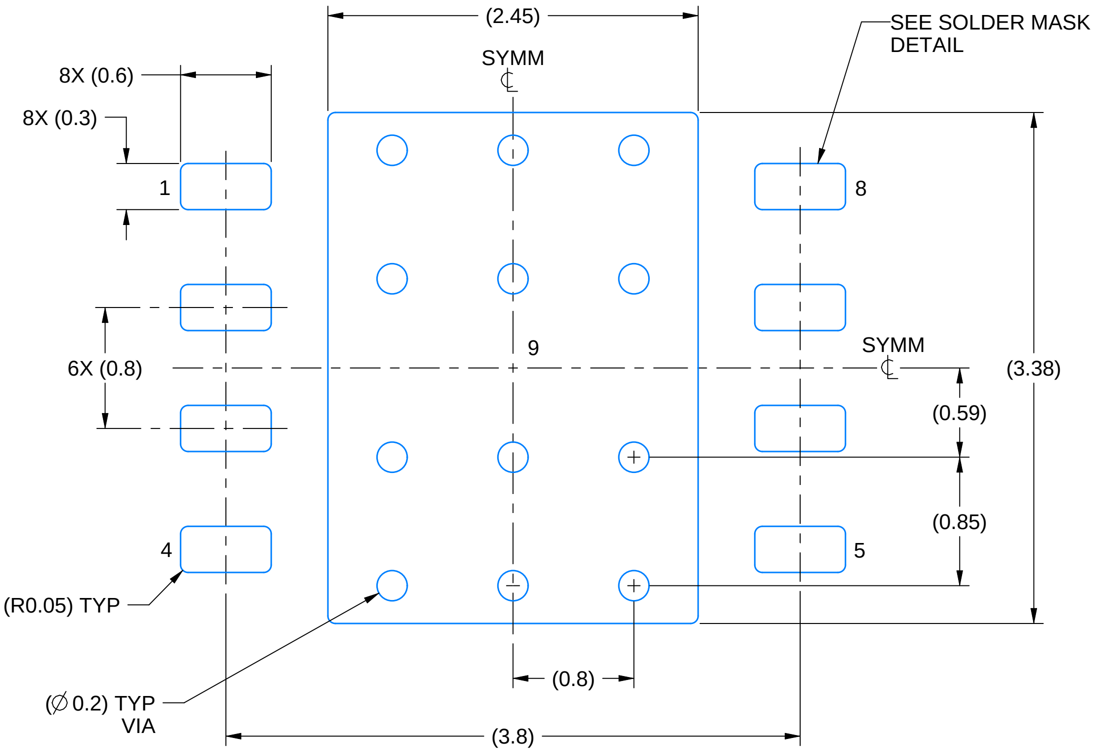
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25230DRMR	VSON	DRM	8	3000	353.0	353.0	32.0
UCC25230DRMT	VSON	DRM	8	250	213.0	191.0	35.0

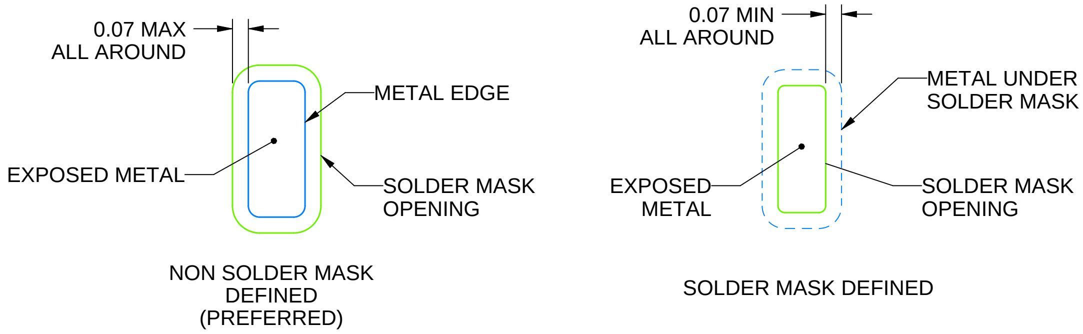


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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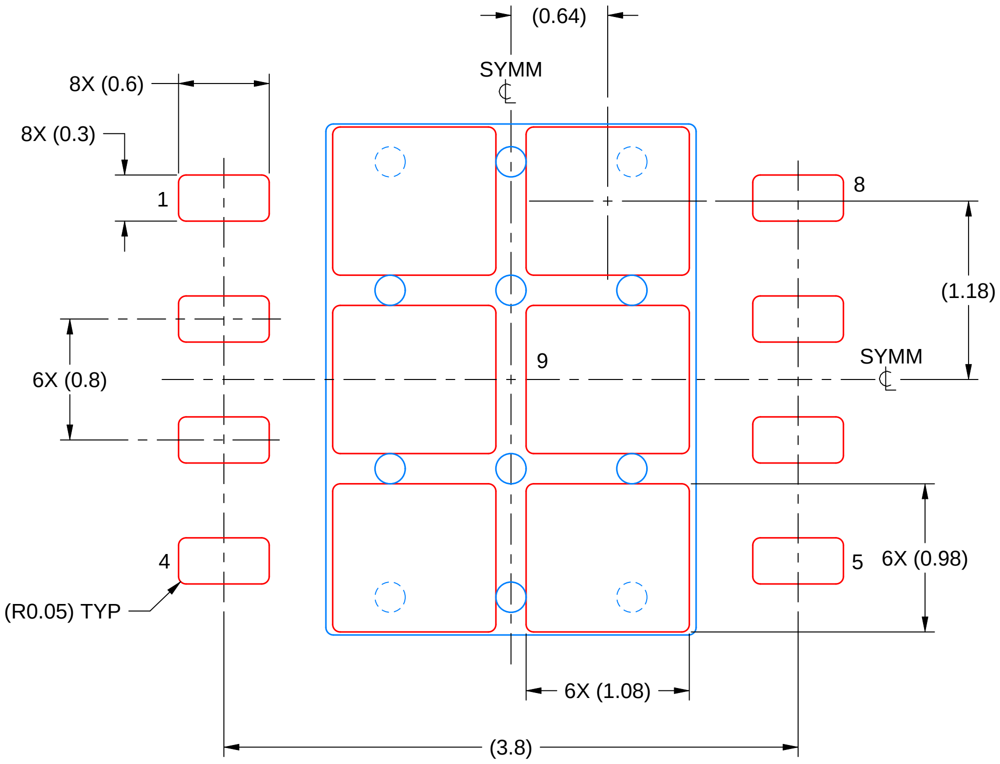
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 9
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025