

# UCC5350-Q1 10A Single-Channel Isolated Gate Driver for SiC/IGBT in Automotive Applications

## 1 Features

- 5kV<sub>RMS</sub> and 3kV<sub>RMS</sub> single-channel isolated gate driver
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1
- **Functional Safety-Quality Managed**
  - [Documentation available to aid functional safety system design](#)
- Feature options
  - Split outputs, 8V UVLO (UCC5350SB-Q1)
  - Miller clamp, 12V UVLO (UCC5350MC-Q1)
- ±5A minimum peak current drive strength
- ±10A typical peak current drive strength
- 3V to 15V input supply voltage
- Up to 33V driver supply voltage
  - 8V and 12V UVLO options
- 100V/ns minimum CMTI
- Negative 5V handling capability on input pins
- 100ns (maximum) propagation delay and <25ns part-to-part skew
- 8-pin DWV (8.5mm creepage) and D (4mm creepage) packages
- Isolation barrier life > 40 Years
- Safety-related certifications:
  - DIN EN IEC 60747-17(VDE 0884-17)
  - UL 1577 component recognition program
- CMOS inputs
- Operating junction temperature: –40°C to +150°C

## 2 Applications

- [On-board charger](#)
- [Traction inverter for EVs](#)
- [DC charging stations](#)
- [HVAC](#)
- [Heaters](#)

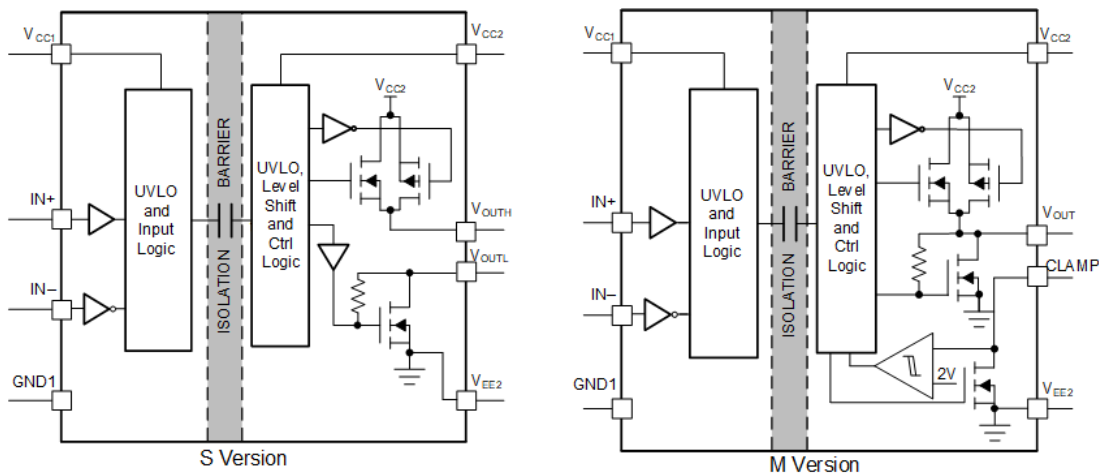
## 3 Description

The UCC5350-Q1 is a single-channel, isolated gate driver with 10A source and 10A sink typical peak current designed to drive MOSFETs, IGBTs, and SiC MOSFETs. The UCC5350-Q1 has the option for Miller clamp or Split Outputs. The CLAMP pin is used to connect the transistor gate to an internal FET beside the output to prevent false turn-on caused by Miller current injection. The split outputs option allows separate control of the rise and fall times of the gate voltage with OUTH and OUTL pins.

### Package Information

PART VERSION	FEATURES	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
UCC5350MC-Q1	Miller Clamp, 12V UVLO	DWV (SOIC, 8)	7.5mm × 5.85mm
		D (SOIC, 8)	3.91mm × 4.9mm
UCC5350SB-Q1	Split Outputs, 8V UVLO	D (SOIC, 8)	3.91mm × 4.9mm

(1) For all available packages, see [Section 13](#).



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**Functional Block Diagram (S and M Versions)**

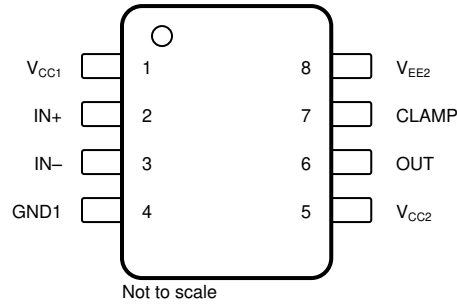
The UCC5350-Q1 is available in a 4mm SOIC-8 (D) or 8.5mm wide body SOIC-8 (DWV) package and can support isolation voltage up to  $3kV_{RMS}$  and  $5kV_{RMS}$ , respectively. The input side is isolated from the output side with  $SiO_2$  capacitive isolation technology with longer than 40 years isolation barrier lifetime. The UCC5350-Q1 is a good fit for driving IGBTs or MOSFETs in applications such as high-voltage traction inverters and on-board chargers.

Compared to an opto-isolated gate driver, the UCC5350-Q1 device has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI.

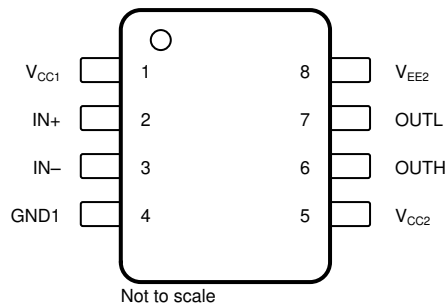
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## 4 Pin Configuration and Function



**Figure 4-1. UCC5350MC-Q1 8-Pin SOIC Top View**



**Figure 4-2. UCC5350SB-Q1 8-Pin SOIC Top View**

**Table 4-1. Pin Functions**

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	NO.	NO.		
	UCC5350MC-Q1	UCC5350SB-Q1		
CLAMP	7	—	I	Active Miller-clamp input used to prevent false turn-on of the power switches found on the 'M' version. Connect to gate directly with low inductance.
GND1	4	4	G	Input ground. All signals on the input side are referenced to this ground.
IN+	2	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open.
IN-	3	3	I	Inverting gate-drive voltage control input. The IN- pin has a CMOS input threshold. This pin is pulled high internally if left open.
OUT	6	—	O	Gate-drive output found on the 'M' version
OUTH	—	6	O	Gate-drive pullup output found on the 'S' version
OUTL	—	7	O	Gate-drive pulldown output found on the 'S' version
V <sub>CC1</sub>	1	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND1. Use a low-ESR or ESL capacitor located as close to the device as possible.
V <sub>CC2</sub>	5	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V <sub>EE2</sub> . Use a low-ESR or ESL capacitor located as close to the device as possible.
V <sub>EE2</sub>	8	8	G	Ground pin. Connect to MOSFET source or IGBT emitter. Connect a locally decoupled capacitor from V <sub>CC2</sub> to V <sub>EE2</sub> . Use a low-ESR or ESL capacitor located as close to the device as possible.

(1) P = Power, G = Ground, I = Input, O = Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input bias pin supply voltage	$V_{CC1} - GND1$	$GND1 - 0.3$	18	V
Driver bias supply	$V_{CC2} - V_{EE2}$	-0.3	35	V
Output signal voltage	$V_{OUTH} - V_{EE2}, V_{OUTL} - V_{EE2}, V_{OUT} - V_{EE2}, V_{CLAMP} - V_{EE2}$	$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
Input signal voltage	$V_{IN+} - GND1, V_{IN-} - GND1$	$GND1 - 5$	$V_{CC1} + 0.3$	V
Junction temperature, $T_J$ <sup>(2)</sup>		-40	150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) To maintain the recommended operating conditions for  $T_J$ , see the Thermal Information table.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	V
		Charged-device model (CDM), per AEC Q100-011	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC1}$	Supply voltage, input side	3		15	V
$V_{CC2}$	Positive supply voltage output side ( $V_{CC2} - V_{EE2}$ ), UCC5350MC	13.2		33	V
$V_{CC2}$	Positive supply voltage output side ( $V_{CC2} - V_{EE2}$ ), UCC5350SB	9.5		33	V
$T_J$	Junction Temperature	-40		150	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC5350-Q1		UNIT
		D	DWV	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.5	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.1	64.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	65.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	18.3	37.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	50.7	63.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).

## 5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>D Package (UCC5350MC-Q1)</b>						
$P_D$	Maximum power dissipation on input and output	$V_{CC1} = 15\text{ V}$ , $V_{CC2} = 15\text{ V}$ , $f = 2.1\text{-MHz}$ , 50% duty cycle, square wave, 2.2-nF load			1.14	W
$P_{D1}$	Maximum input power dissipation				0.05	W
$P_{D2}$	Maximum output power dissipation				1.09	W
<b>D Package (UCC5350SB-Q1)</b>						
$P_D$	Maximum power dissipation on input and output	$V_{CC1} = 15\text{ V}$ , $V_{CC2} = 15\text{ V}$ , $f = 1.8\text{-MHz}$ , 50% duty cycle, square wave, 2.2-nF load			0.99	W
$P_{D1}$	Maximum input power dissipation				0.05	W
$P_{D2}$	Maximum output power dissipation				0.94	W
<b>DWV Package (UCC5350MC-Q1)</b>						
$P_D$	Maximum power dissipation on input and output	$V_{CC1} = 15\text{ V}$ , $V_{CC2} = 15\text{ V}$ , $f = 1.9\text{-MHz}$ , 50% duty cycle, square wave, 2.2-nF load			1.04	W
$P_{D1}$	Maximum input power dissipation				0.05	W
$P_{D2}$	Maximum output power dissipation				0.99	W

## 5.6 Insulation Specifications for D Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			D	
CLR	External Clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	$\geq 4$	mm
CPG	External Creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	$\geq 4$	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	$> 21$	$\mu\text{m}$
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	$> 400$	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 150V_{RMS}$	I-IV	
		Rated mains voltage $\leq 300V_{RMS}$	I-III	
<b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b>				
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1200 <sup>(7)</sup>	$V_{PK}$
$V_{IOWM}$	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDb) test	850 <sup>(7) (8)</sup>	$V_{RMS}$
		DC Voltage	1200 <sup>(7)</sup>	$V_{DC}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , $t = 60\text{ s}$ (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ , $t = 1\text{ s}$ (100% production)	4242	$V_{PK}$
$V_{IMP}$	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1	5000	$V_{PK}$
$V_{IOSM}$	Maximum surge isolation voltage <sup>(4)</sup>	$V_{IOSM} \geq 1.3 \times V_{IMP}$ ; Tested in oil (qualification test), 1.2/50 $\mu\text{s}$ waveform per IEC 62368-1	6500	$V_{PK}$
$q_{pd}$	Apparent charge <sup>(5)</sup>	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60\text{ s}$ $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10\text{ s}$	$\leq 5$	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60\text{ s}$ ; $V_{pd(m)} = 1.3 \times V_{IORM}$ , $t_m = 10\text{ s}$	$\leq 5$	
		Method b: At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1\text{ s}$ ; $V_{pd(m)} = 1.5 \times V_{IORM}$ , $t_m = 1\text{ s}$ (method b1) or $V_{pd(m)} = V_{ini}$ , $t_m = t_{ini}$ (method b2)	$\leq 5$	

## 5.6 Insulation Specifications for D Package (continued)

PARAMETER	TEST CONDITIONS	VALUE	UNIT
		D	
$C_{IO}$	Barrier capacitance, input to output <sup>(6)</sup> $V_{IO} = 0.4 \times \sin(2\pi ft)$ , $f = 1 \text{ MHz}$	1.2	pF
$R_{IO}$	$V_{IO} = 500 \text{ V}$ , $T_A = 25^\circ\text{C}$	$> 10^{12}$	$\Omega$
	$V_{IO} = 500 \text{ V}$ , $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$> 10^{11}$	
	$V_{IO} = 500 \text{ V}$ at $T_S = 150^\circ\text{C}$	$> 10^9$	
Pollution degree		2	
Climatic category		40/125/21	
<b>UL 1577</b>			
$V_{ISO}$	Withstand isolation voltage $V_{TEST} = V_{ISO}$ , $t = 60 \text{ s}$ (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1 \text{ s}$ (100% production)	3000	$V_{RMS}$

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-pin device.
- (7) System isolation working voltages need to be verified according to application parameters.
- (8) UCC5350-Q1 is production tested for working voltage  $> 850V_{RMS}$  during IEC/VDE partial discharge test

### 5.7 Insulation Specifications for DWV Package

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DWV	
CLR	External Clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External Creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 600 <sub>V</sub> RMS	I-III	
		Rated mains voltage ≤ 1000 <sub>V</sub> RMS	I-II	
<b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDb) test	1500	V <sub>RMS</sub>
		DC Voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification) ; V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	7071	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum Impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	V <sub>ISOM</sub> ≥ 1.3 V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b: At routine test (100% production) V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.5 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s (method b1) or V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b2)	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz	1.2	pF
R <sub>IO</sub>	Isolation resistance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)	5000	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-pin device.

## 5.8 Safety-Related Certifications For D Package

VDE	UL
Certified according to DIN EN IEC 60747–17 (VDE 0884-17)	Recognized under UL 1577 Component Recognition Program
Certificate number: 40047657	File Number: E181974

## 5.9 Safety-Related Certifications For DWV Package

VDE	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Recognized under UL 1577 Component Recognition Program
Certificate number: 40040142	File Number: E181974

## 5.10 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>D PACKAGE (UCC5350MC-Q1)</b>					
I <sub>S</sub> Safety output supply current	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-2</a>			73	mA
	Output side				
I <sub>S</sub> Safety output supply current	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-2</a>			36	mA
	Output side				
P <sub>S</sub> Safety output supply power	R <sub>θJA</sub> = 109.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-4</a>	Input side		0.05	W
		Output side		1.09	
		Total		1.14	
T <sub>S</sub> Maximum safety temperature <sup>(1)</sup>				150	°C
<b>D PACKAGE (UCC5350SB-Q1)</b>					
I <sub>S</sub> Safety output supply current	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-2</a>			63	mA
	Output side				
I <sub>S</sub> Safety output supply current	R <sub>θJA</sub> = 109.5°C/W, V <sub>CC2</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-2</a>			31	mA
	Output side				
P <sub>S</sub> Safety output supply power	R <sub>θJA</sub> = 109.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-4</a>	Input side		0.05	W
		Output side		0.94	
		Total		0.99	
T <sub>S</sub> Maximum safety temperature <sup>(1)</sup>				150	°C
<b>DWV PACKAGE (UCC5350MC-Q1)</b>					
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 119.8°C/W, V <sub>I</sub> = 15 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-1</a>			66	mA
	Output side				
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 119.8°C/W, V <sub>I</sub> = 30 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-1</a>			33	mA
	Output side				
P <sub>S</sub> Safety input, output, or total power	R <sub>θJA</sub> = 119.8°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Figure 5-3</a>	Input side		0.05	W
		Output side		0.99	
		Total		1.04	
T <sub>S</sub> Maximum safety temperature <sup>(1)</sup>				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$$T_J = T_A + R_{\theta JA} \times P, \text{ where } P \text{ is the power dissipated in the device.}$$

$$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S, \text{ where } T_{J(max)} \text{ is the maximum allowed junction temperature.}$$

$$P_S = I_S \times V_I, \text{ where } V_I \text{ is the maximum input voltage.}$$

## 5.11 Electrical Characteristics

$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to  $\text{GND1}$ ,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_L = 100\text{-pF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (UCC5350MC-Q1),  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  (UCC5350SB-Q1), (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>						
$I_{VCC1}$	Input supply quiescent current			1.67	2.4	mA
$I_{VCC2}$	Output supply quiescent current			1.1	1.8	mA
<b>SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS</b>						
$V_{IT+}(UVLO1)$	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
$V_{IT-}(UVLO1)$	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
$V_{hys}(UVLO1)$	VCC1 UVLO threshold hysteresis			0.1		V
<b>OUTPUT SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (UCC5350MC-Q1)</b>						
$V_{IT+}(UVLO2)$	VCC2 Positive-going UVLO threshold voltage			12	13	V
$V_{IT-}(UVLO2)$	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
$V_{hys}(UVLO2)$	VCC2 UVLO threshold voltage hysteresis			1		V
<b>OUTPUT SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS (UCC5350SB-Q1)</b>						
$V_{IT+}(UVLO2)$	VCC2 Positive-going UVLO threshold voltage			8.7	9.4	V
$V_{IT-}(UVLO2)$	VCC2 Negative-going UVLO threshold voltage		7.3	8.0		V
$V_{hys}(UVLO2)$	VCC2 UVLO threshold voltage hysteresis			0.7		V
<b>LOGIC I/O</b>						
$V_{IT+}(IN)$	Positive-going input threshold voltage (IN+, IN-)			$0.55 \times V_{CC1}$	$0.7 \times V_{CC1}$	V
$V_{IT-}(IN)$	Negative-going input threshold voltage (IN+, IN-)		$0.3 \times V_{CC1}$	$0.45 \times V_{CC1}$		V
$V_{hys}(IN)$	Input hysteresis voltage (IN+, IN-)			$0.1 \times V_{CC1}$		V
$I_{IH}$	High-level input leakage at IN+	IN+ = $V_{CC1}$		40	240	$\mu\text{A}$
$I_{IL}$	Low-level input leakage at IN-	IN- = $\text{GND1}$	-240	-40		$\mu\text{A}$
		IN- = $\text{GND1} - 5\text{ V}$	-310	-80		
<b>GATE DRIVER STAGE</b>						
$V_{OH}$	High-level output voltage (VCC2 - OUT) and (VCC2 - OUTH)	$I_{OUT} = -20\text{ mA}$	100	240		mV
$V_{OL}$	Low level output voltage (OUT and OUTL)	IN+ = low, IN- = high; $I_{OUT} = 20\text{ mA}$	5	7		mV
$I_{OH}$	Peak source current	UCC5350MC, IN+ = high, IN- = low	5	10		A
		UCC5350SB, IN+ = high, IN- = low	5	8.5		A
$I_{OL}$	Peak sink current	IN+ = low, IN- = high	5	10		A
<b>Active Miller Clamp (UCC5350MC-Q1 only)</b>						
$V_{CLAMP}$	Low-level clamp voltage	$I_{CLAMP} = 20\text{ mA}$		7	10	mV
$I_{CLAMP}$	Clamp low-level current	$V_{CLAMP} = V_{EE2} + 15\text{ V}$	5	10		A

### 5.11 Electrical Characteristics (continued)

$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to GND1,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_L = 100\text{-pF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  (UCC5350MC-Q1),  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  (UCC5350SB-Q1), (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CLAMP(L)}$	Clamp low-level current for low output voltage $V_{CLAMP} = V_{EE2} + 2\text{ V}$	5	10		A
$V_{CLAMP-TH}$	Clamp threshold voltage		2.1	2.3	V
<b>SHORT CIRCUIT CLAMPING</b>					
$V_{CLP-OUT}$	Clamping voltage ( $V_{OUT} - V_{CC2}$ ) IN+ = high, IN- = low, $t_{CLAMP} = 10\text{ }\mu\text{s}$ , $I_{OUT} = 500\text{ mA}$		1	1.3	V
$V_{CLP-OUT}$	Clamping voltage ( $V_{EE2} - V_{OUT}$ ) IN+ = low, IN- = high, $t_{CLAMP} = 10\text{ }\mu\text{s}$ , $I_{OUT} = -500\text{ mA}$		1.5		V
		IN+ = low, IN- = high, $I_{OUT} = -20\text{ mA}$		0.9	
<b>ACTIVE PULLDOWN</b>					
$V_{OUTSD}$	Active pulldown voltage on OUT $I_{OUT} = 0.1 \times I_{OUT(typ)}$ , $V_{CC2} = \text{open}$		1.8	2.5	V

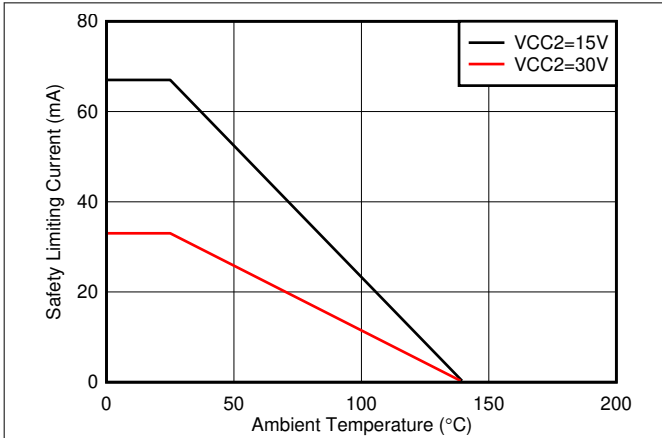
### 5.12 Switching Characteristics

$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to GND1,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)

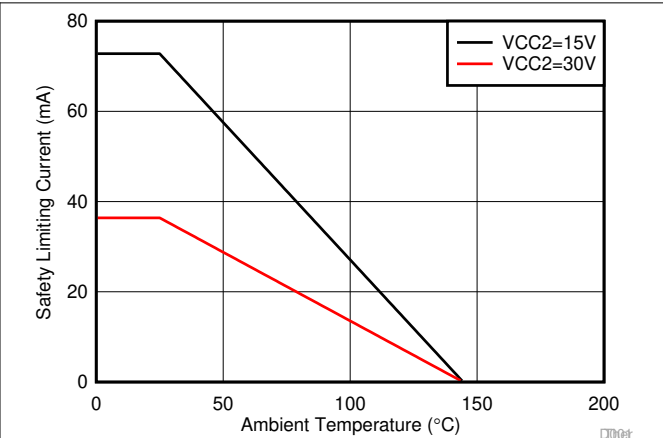
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output-signal rise time $C_{LOAD} = 1\text{ nF}$		10	26	ns
$t_f$	Output-signal fall time $C_{LOAD} = 1\text{ nF}$		10	22	ns
$t_{PLH}$	Propagation delay, high $C_{LOAD} = 100\text{ pF}$	40	55	70	ns
$t_{PHL}$	Propagation delay, low $C_{LOAD} = 100\text{ pF}$	40	55	70	ns
$t_{UVLO1\_rec}$	UVLO recovery delay of $V_{CC1}$ See Figure 7-7.		30		$\mu\text{s}$
$t_{UVLO2\_rec}$	UVLO recovery delay of $V_{CC2}$ See Figure 7-7.		50		$\mu\text{s}$
$t_{PWD}$	Pulse width distortion $ t_{PHL} - t_{PLH} $ $C_{LOAD} = 100\text{ pF}$		1	20	ns
$t_{sk(pp)}$	Part-to-part skew <sup>(1)</sup> $C_{LOAD} = 100\text{ pF}$		1	25	ns
$t_{PWmin1}$	No response at OUT where OUT $< 10\% \times V_{CC2}$ $C_{LOAD} = 100\text{ pF}$	8			ns
$t_{PWmin2}$	No response at OUT where OUT $\geq 90\% \times V_{CC2}$ $C_{LOAD} = 100\text{ pF}$			38	ns
CMT1	Common-mode transient immunity PWM is tied to GND or $V_{CC1}$ , $V_{CM} = 1200\text{ V}$	100	120		kV/ $\mu\text{s}$

- (1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

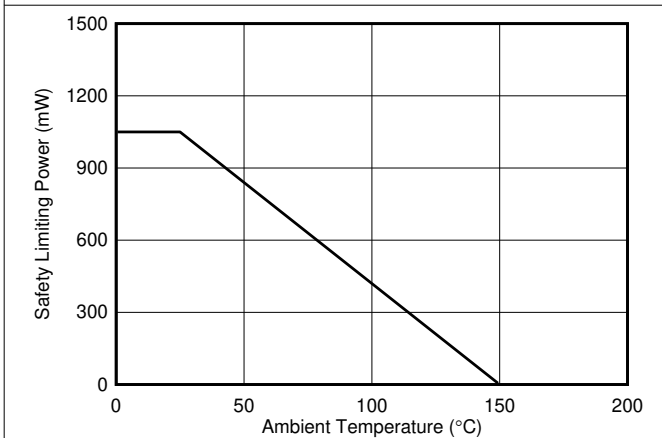
### 5.13 Insulation Characteristics Curves



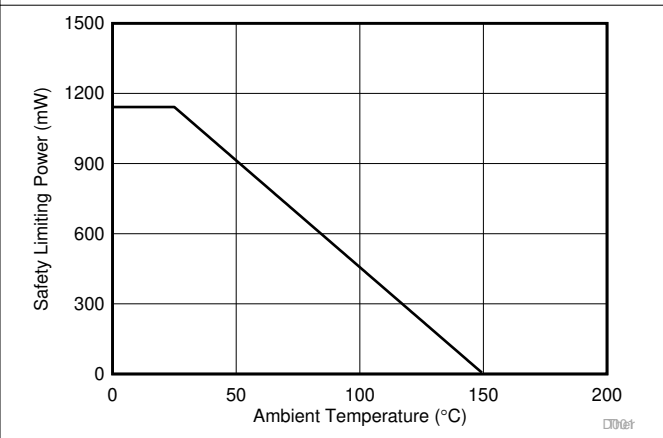
**Figure 5-1. Thermal Derating Curve for Limiting Current per VDE for DWV Package**



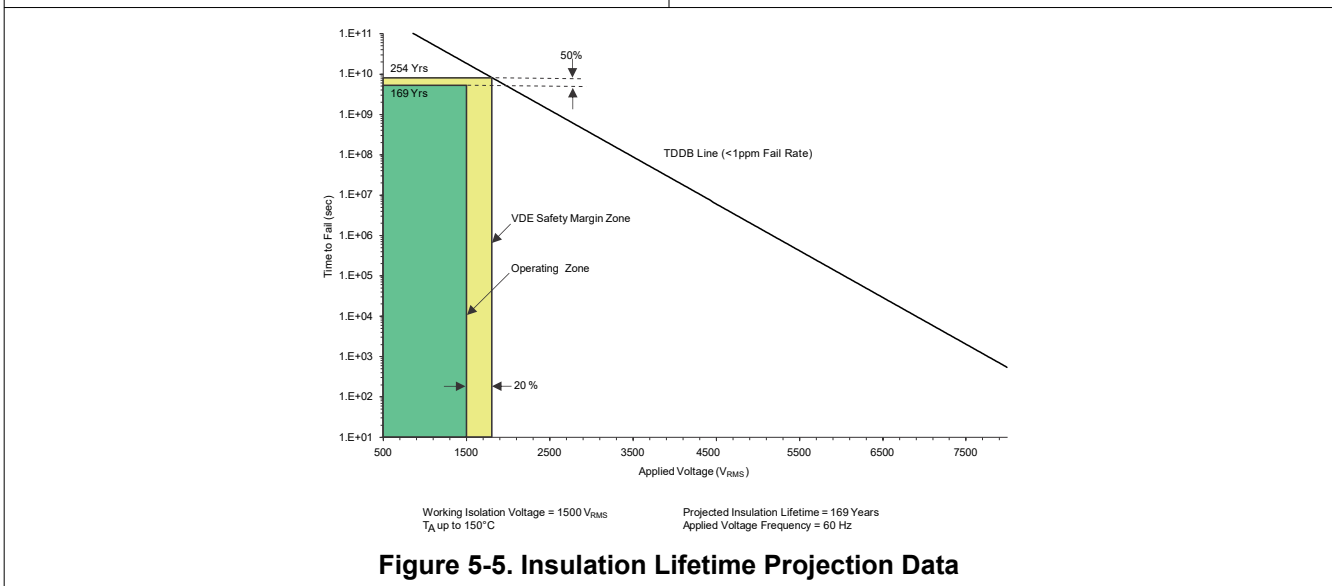
**Figure 5-2. Thermal Derating Curve for Limiting Current per VDE for D Package**



**Figure 5-3. Thermal Derating Curve for Limiting Power per VDE for DWV Package**



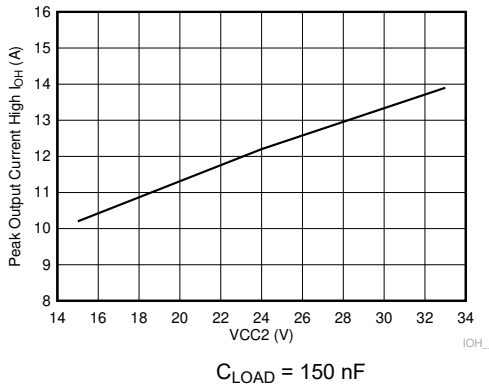
**Figure 5-4. Thermal Derating Curve for Limiting Power per VDE for D Package**



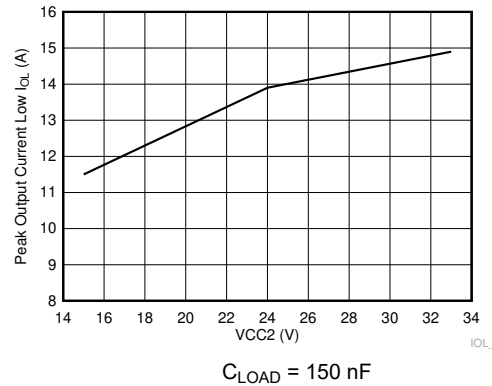
**Figure 5-5. Insulation Lifetime Projection Data**

### 5.14 Typical Characteristics

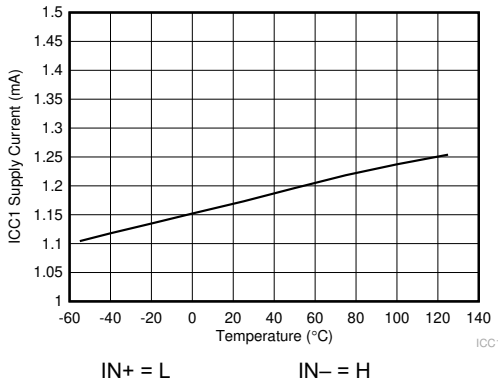
$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to  $\text{GND1}$ ,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)



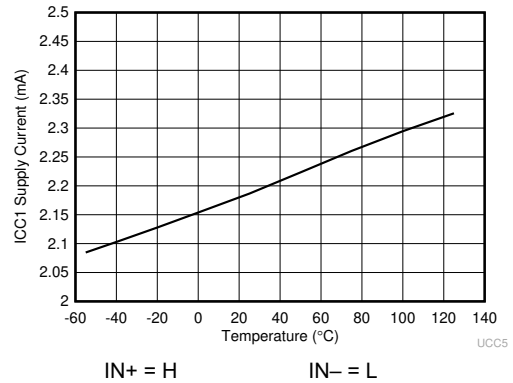
**Figure 5-6. Output-High Drive Current vs Output Voltage**



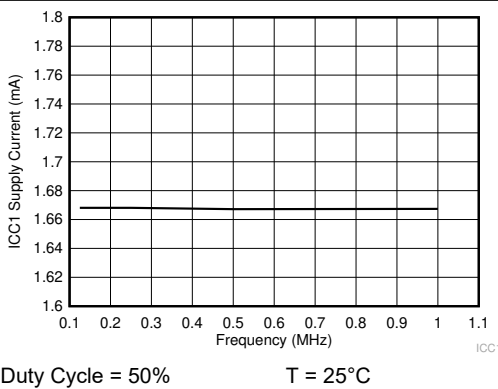
**Figure 5-7. Output-Low Drive Current vs Output Voltage**



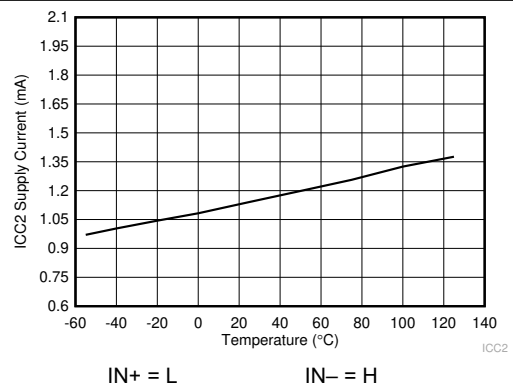
**Figure 5-8. I<sub>CC1</sub> Supply Current vs Temperature**



**Figure 5-9. I<sub>CC1</sub> Supply Current vs Temperature**



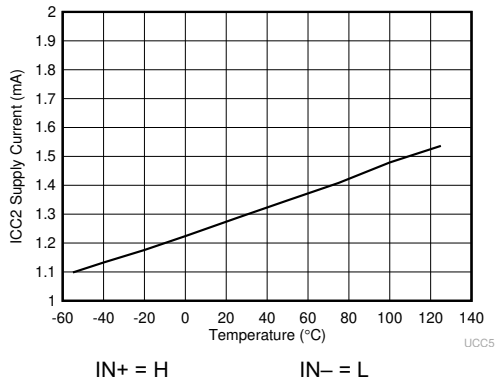
**Figure 5-10. I<sub>CC1</sub> Supply Current vs Input Frequency**



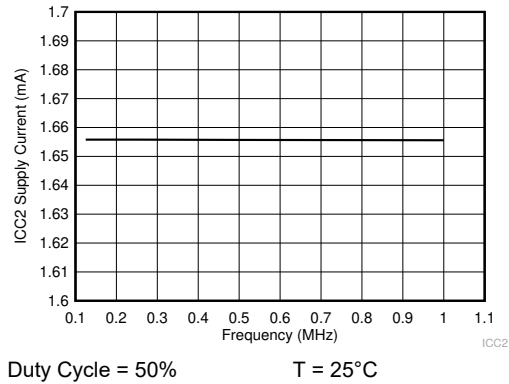
**Figure 5-11. I<sub>CC2</sub> Supply Current vs Temperature**

### 5.14 Typical Characteristics (continued)

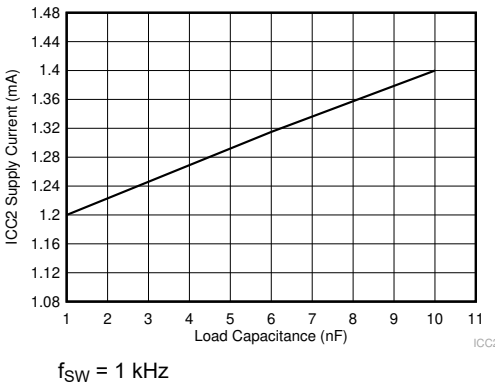
$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to  $\text{GND1}$ ,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)



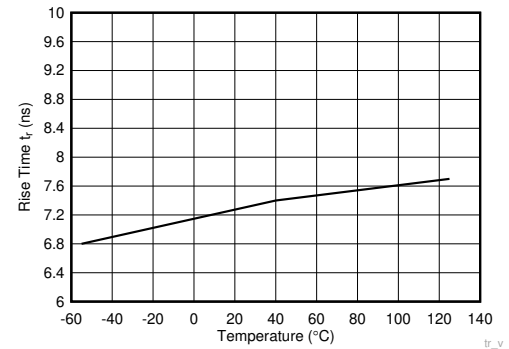
**Figure 5-12. ICC2 Supply Current vs Temperature**



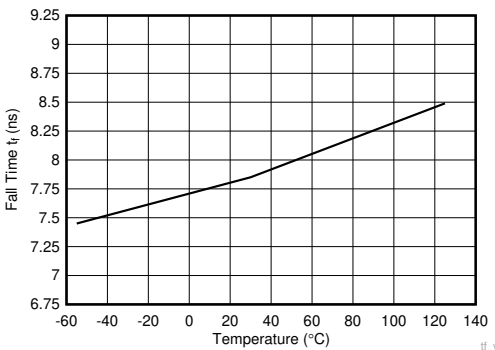
**Figure 5-13. ICC2 Supply Current vs Input Frequency**



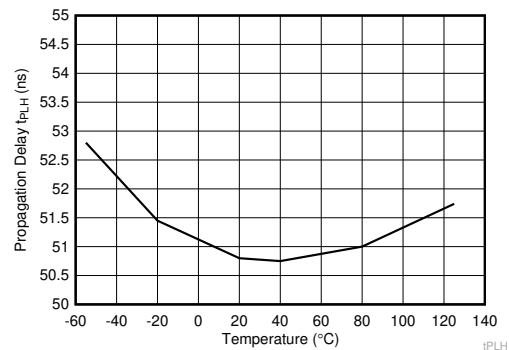
**Figure 5-14. ICC2 Supply Current vs Load Capacitance**



**Figure 5-15. Rise Time vs Temperature**



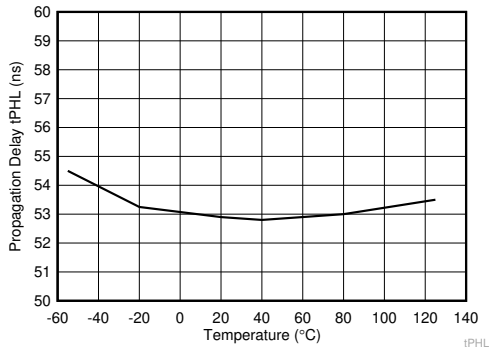
**Figure 5-16. Fall Time vs Temperature**



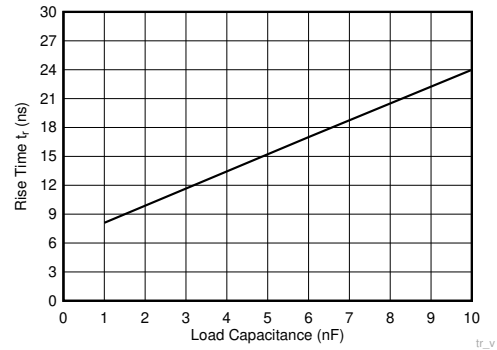
**Figure 5-17. Propagation Delay tPLH vs Temperature**

### 5.14 Typical Characteristics (continued)

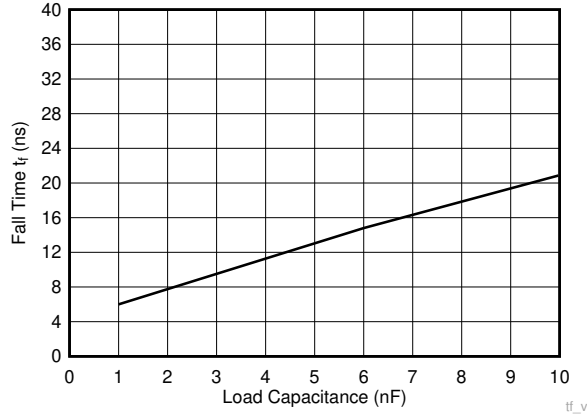
$V_{CC1} = 3.3\text{ V}$  or  $5\text{ V}$ ,  $0.1\text{-}\mu\text{F}$  capacitor from  $V_{CC1}$  to  $\text{GND1}$ ,  $V_{CC2} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{CC2}$  to  $V_{EE2}$ ,  $C_{LOAD} = 1\text{ nF}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , (unless otherwise noted)



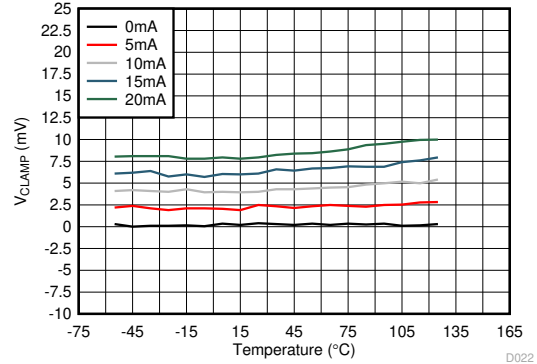
**Figure 5-18. Propagation Delay  $t_{PHL}$  vs Temperature**



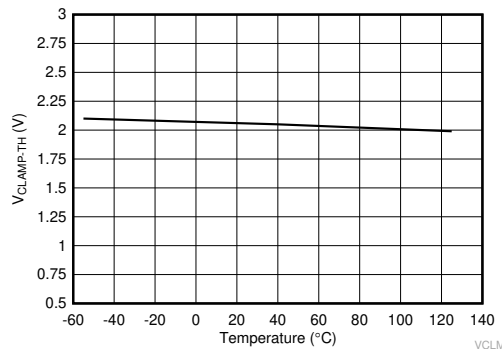
$f_{SW} = 1\text{ kHz}$        $R_{GH} = 0\ \Omega$        $R_{GL} = 0\ \Omega$   
**Figure 5-19. Rise Time vs Load Capacitance**



$f_{SW} = 1\text{ kHz}$        $R_{GH} = 0\ \Omega$        $R_{GL} = 0\ \Omega$   
**Figure 5-20. Fall Time vs Load Capacitance**



**Figure 5-21.  $V_{CLAMP}$  vs Temperature**



**Figure 5-22.  $V_{CLAMP-TH}$  vs Temperature**

## 6 Parameter Measurement Information

### 6.1 Propagation Delay, Inverting, and Noninverting Configuration

Figure 6-1 shows the propagation delay for noninverting configurations. Figure 6-2 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times.

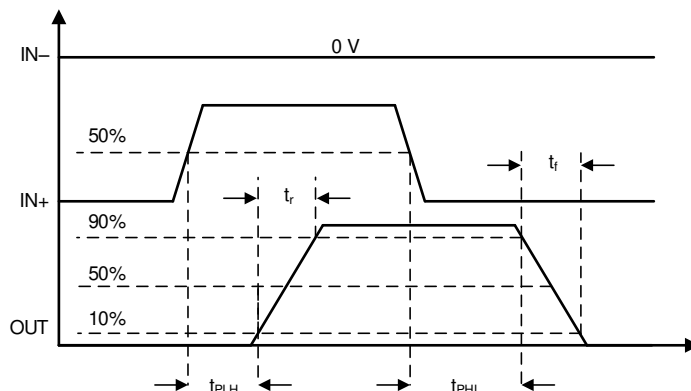


Figure 6-1. Propagation Delay, Noninverting Configuration

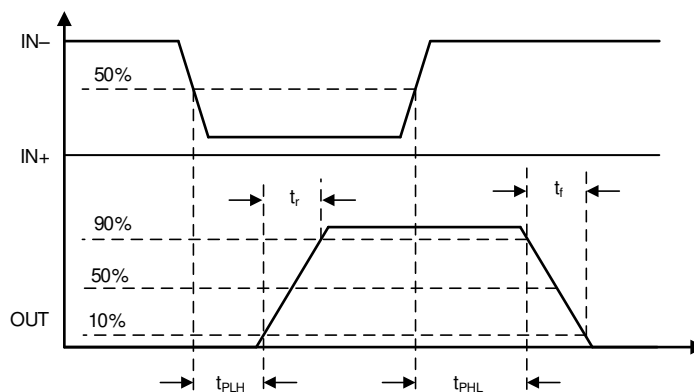
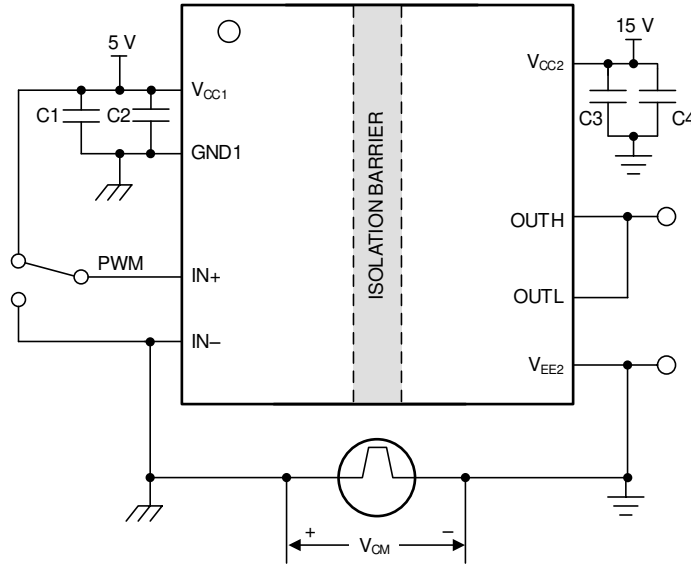


Figure 6-2. Propagation Delay, Inverting Configuration

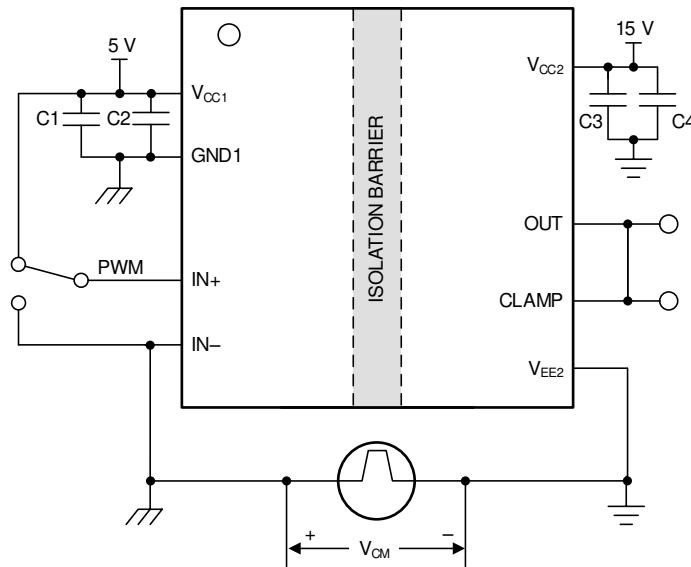
### 6.1.1 CMTI Testing

Figure 6-3 and Figure 6-4 are simplified diagrams of the CMTI testing configuration.



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**Figure 6-3. CMTI Test Circuit for Split Output (UCC5350SB)**



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**Figure 6-4. CMTI Test Circuit for Miller Clamp (UCC5350MC)**

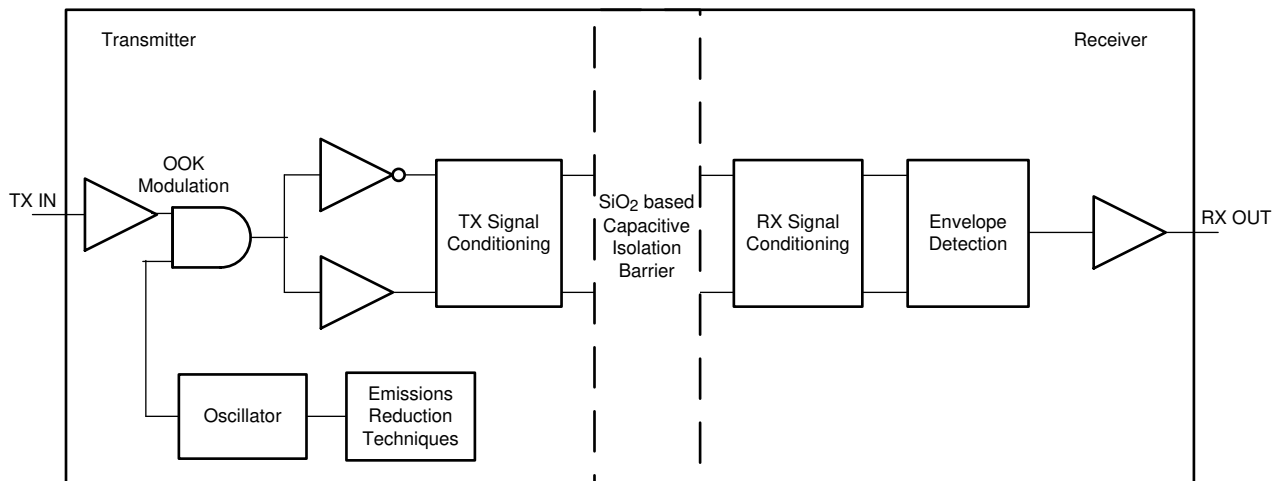
## 7 Detailed Description

### 7.1 Overview

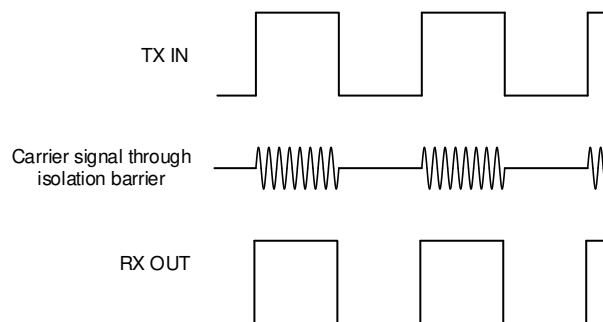
The UCC5350-Q1 family of isolated gate drivers has two variations: split output, and Miller clamp. The isolation inside the UCC5350-Q1 is implemented with high-voltage SiO<sub>2</sub>-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see [Figure 7-2](#)). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5350-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 7-1](#), shows a functional block diagram of a typical channel. [Figure 7-2](#) shows a conceptual detail of how the OOK scheme works.

[Figure 7-1](#) shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

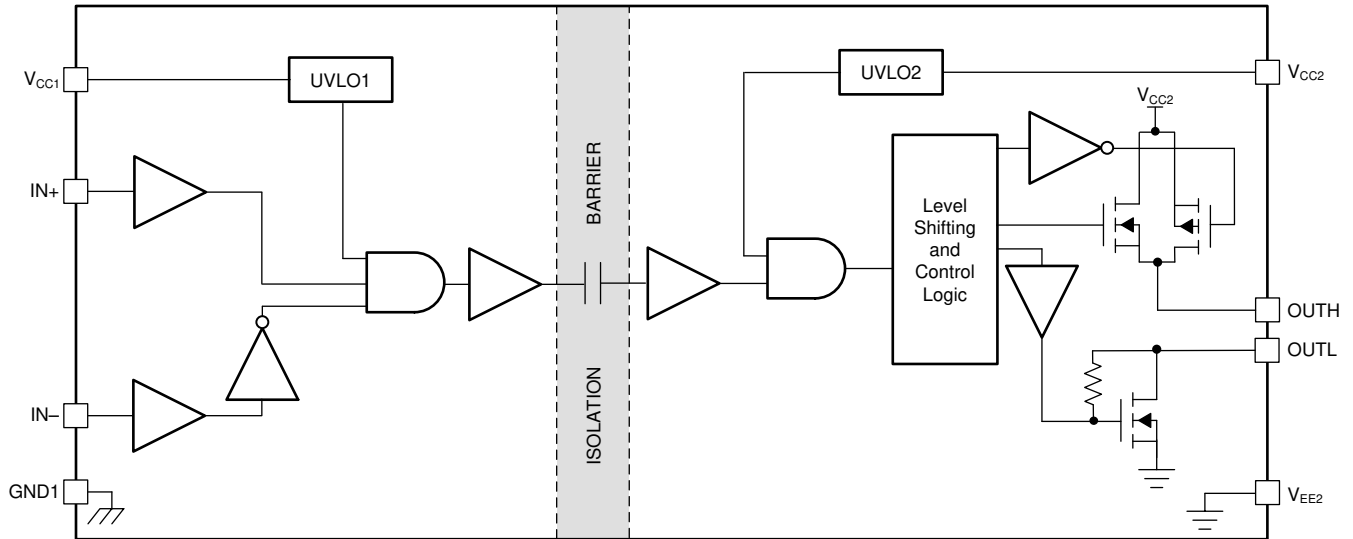
### 7.2 Functional Block Diagram



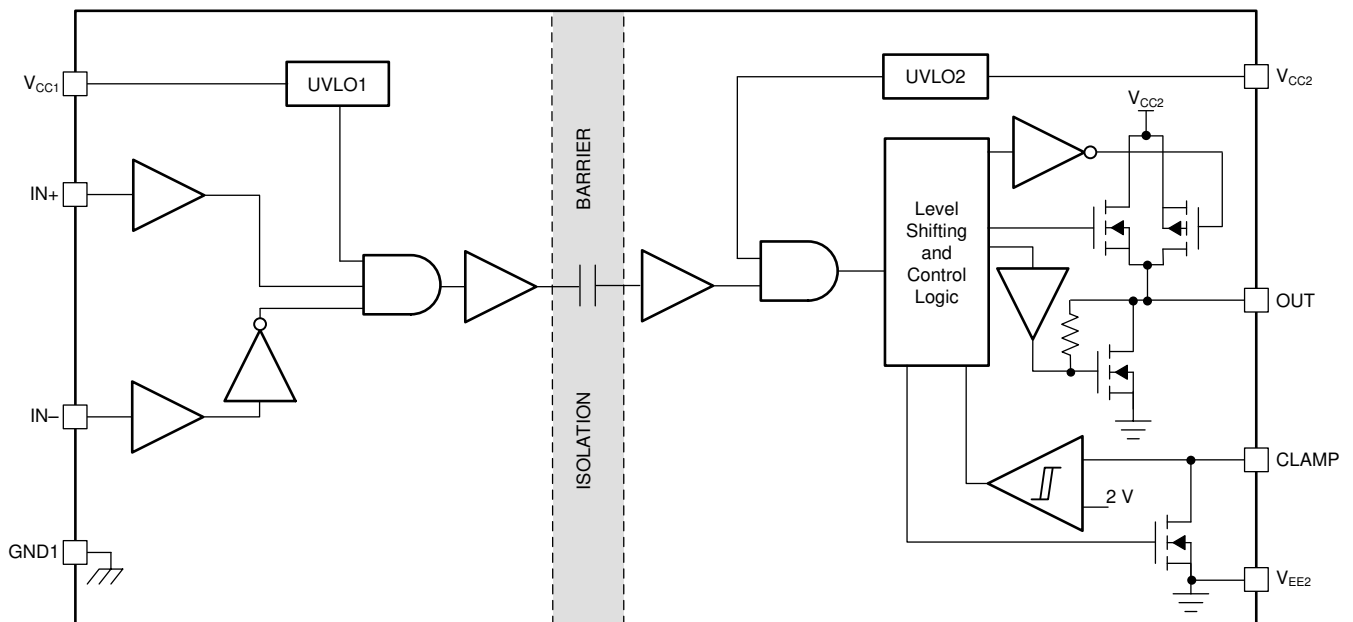
**Figure 7-1. Conceptual Block Diagram of a Capacitive Data Channel**



**Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme**



**Figure 7-3. Functional Block Diagram — Split Output**



**Figure 7-4. Functional Block Diagram — Miller Clamp**

## 7.3 Feature Description

### 7.3.1 Power Supply

The  $V_{CC1}$  input power supply supports a wide voltage range from 3 V to 15 V and the  $V_{CC2}$  output supply supports a voltage range from 13.2 V to 33 V (UCC5350MC) or 9.5 V to 33 V (UCC5350SB).

For operation with unipolar supply, the  $V_{CC2}$  supply is connected to 15 V with respect to  $V_{EE2}$  for IGBTs, and 20 V for SiC MOSFETs. The  $V_{EE2}$  supply is connected to 0 V. In this use case, the Miller clamp helps to prevent a false turn-on of the power switch without a negative voltage rail. The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the  $V_{EE2}$  supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate.

### 7.3.2 Input Stage

The input pins (IN+ and IN–) of the UCC5350-Q1 are based on CMOS-compatible input-threshold logic that is completely isolated from the  $V_{CC2}$  supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC5350-Q1 has a typical high threshold ( $V_{IT+(IN)}$ ) of  $0.55 \times V_{CC1}$  and a typical low threshold of  $0.45 \times V_{CC1}$ . A wide hysteresis ( $V_{hys(IN)}$ ) of  $0.1 \times V_{CC1}$  makes for good noise immunity and stable operation. If either of the inputs are left open, 128 k $\Omega$  of internal pull-down resistance forces the IN+ pin low and 128 k $\Omega$  of internal resistance pulls IN– high. However, TI still recommends grounding an input or tying to VCC1 if it is not being used for improved noise immunity.

Because the input side of the UCC5350-Q1 is isolated from the output driver, the input signal amplitude can be larger or smaller than  $V_{CC2}$  provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient  $V_{CC2}$  for any gate. However, the amplitude of any signal applied to IN+ or IN– must never be at a voltage higher than  $V_{CC1}$ .

### 7.3.3 Output Stage

The output stage of the UCC5350-Q1 features a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences  $dV/dt$ ). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. [Table 7-1](#) lists the typical internal resistance values of the pull-up and pull-down structure.

**Table 7-1. UCC5350-Q1 On-Resistance**

DEVICE OPTION	$R_{NMOS}$	$R_{OH}$	$R_{OL}$	$R_{CLAMP}$	UNIT
UCC5350MC-Q1	1.54	12	0.26	0.26	$\Omega$
UCC5350SB-Q1	1.54	12	0.26	Not applicable	$\Omega$

The  $R_{OH}$  parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pull-up N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC5350-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the  $R_{OH}$  parameter, which yields a faster turn-on. The turn-on-phase output resistance is the parallel combination  $R_{OH} \parallel R_{NMOS}$ .

The pull-down structure in the UCC5350-Q1 is simply composed of an N-channel MOSFET. The output of the UCC5350-Q1 is capable of delivering, or sinking, 5-A peak current pulses. The output voltage swing between  $V_{CC2}$  and  $V_{EE2}$  provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

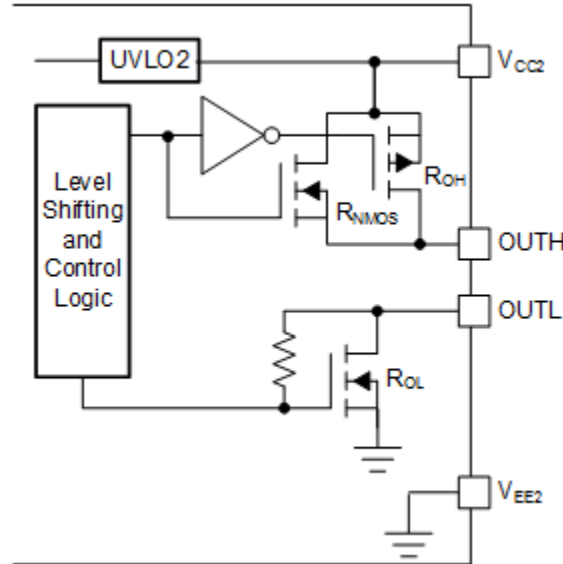


Figure 7-5. Output Stage—S Version

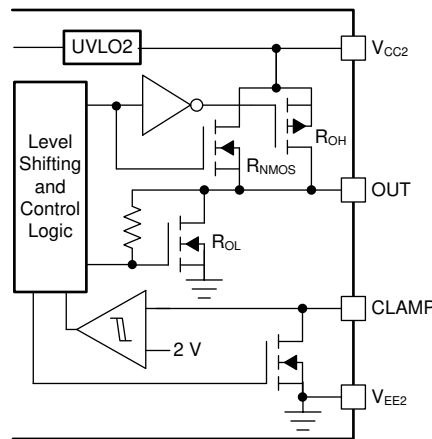


Figure 7-6. Output Stage—M Version

### 7.3.4 Protection Features

#### 7.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the  $V_{CC1}$  and  $V_{CC2}$  supplies between the  $V_{CC1}$  and  $GND1$ , and  $V_{CC2}$  and  $V_{EE2}$  pins to prevent an underdriven condition on IGBTs and MOSFETs. When  $V_{CC}$  is lower than  $V_{IT+}$  (UVLO) at device start-up or lower than  $V_{IT-}$  (UVLO) after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins ( $IN+$  and  $IN-$ ) as shown in Table 7-2. The  $V_{CC}$  UVLO protection has a hysteresis feature ( $V_{hys}(UVLO)$ ). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. Figure 7-7 shows the UVLO functions.

Table 7-2. UCC5350-Q1  $V_{CC1}$  UVLO Logic

CONDITION	INPUTS		OUTPUT
	IN+	IN-	OUT
$V_{CC1} - GND1 < V_{IT+}(UVLO1)$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

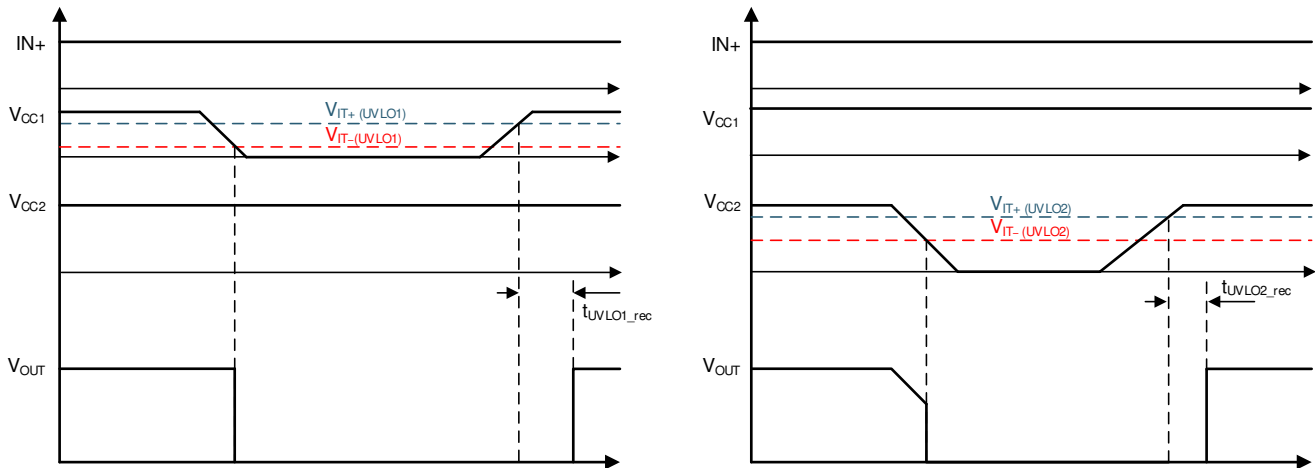
**Table 7-2. UCC5350-Q1 V<sub>CC1</sub> UVLO Logic (continued)**

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
$V_{CC1} - GND1 < V_{IT-(UVLO1)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

**Table 7-3. UCC5350-Q1 V<sub>CC2</sub> UVLO Logic**

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
$V_{CC2} - V_{EE2} < V_{IT+(UVLO2)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
$V_{CC2} - V_{EE2} < V_{IT-(UVLO2)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

When  $V_{CC1}$  or  $V_{CC2}$  drops below the UVLO1 or UVLO2 threshold, a delay,  $t_{UVLO1\_rec}$  or  $t_{UVLO2\_rec}$ , occurs on the output when the supply voltage rises above  $V_{IT+(UVLO)}$  or  $V_{IT-(UVLO2)}$  again. [Figure 7-7](#) shows this delay.



**Figure 7-7. UVLO Functions**

**7.3.4.2 Active Pulldown**

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the  $V_{CC2}$  supply. This feature prevents false IGBT and MOSFET turn-on on the OUT and CLAMP pins by clamping the output to approximately 2 V.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pull-up resistor while the lower NMOS gate is tied to the driver output through a 500-kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

### 7.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the  $V_{CC2}$  voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the  $V_{CC2}$  pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10  $\mu$ s and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

### 7.3.4.4 Active Miller Clamp

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground ( $V_{EE2}$ ) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. [Figure 8-2](#) shows a typical application circuit of this function.

## 7.4 Device Functional Modes

[Table 7-5](#) lists the functional modes for the UCC5350-Q1 assuming  $V_{CC1}$  and  $V_{CC2}$  are in the recommended range.

**Table 7-4. Function Table for UCC5350SB-Q1**

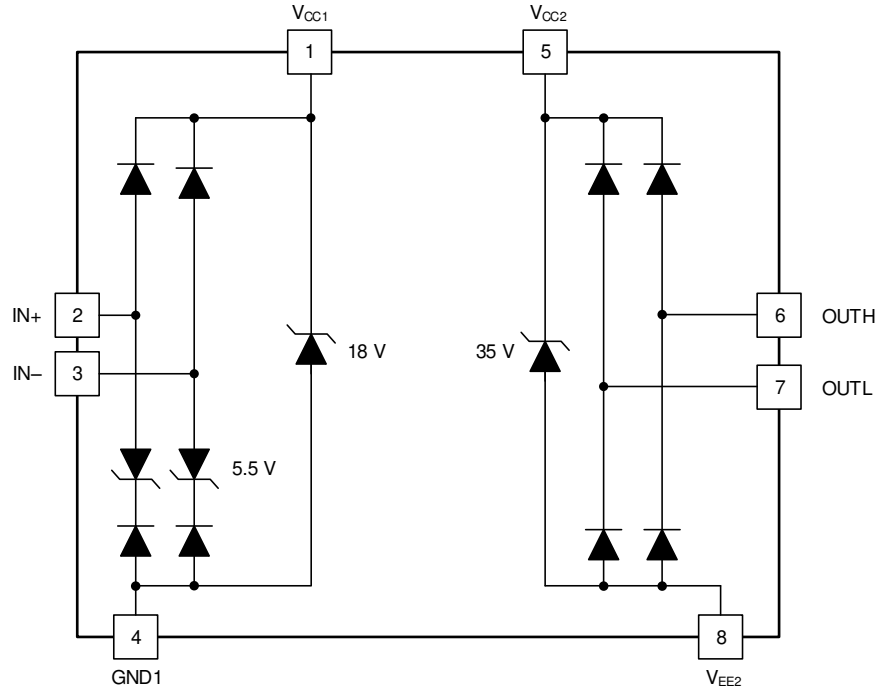
IN+	IN–	OUTH	OUTL
Low	X	Hi-Z	Low
X	High	Hi-Z	Low
High	Low	High	High-Z

**Table 7-5. Function Table for UCC5350MC-Q1**

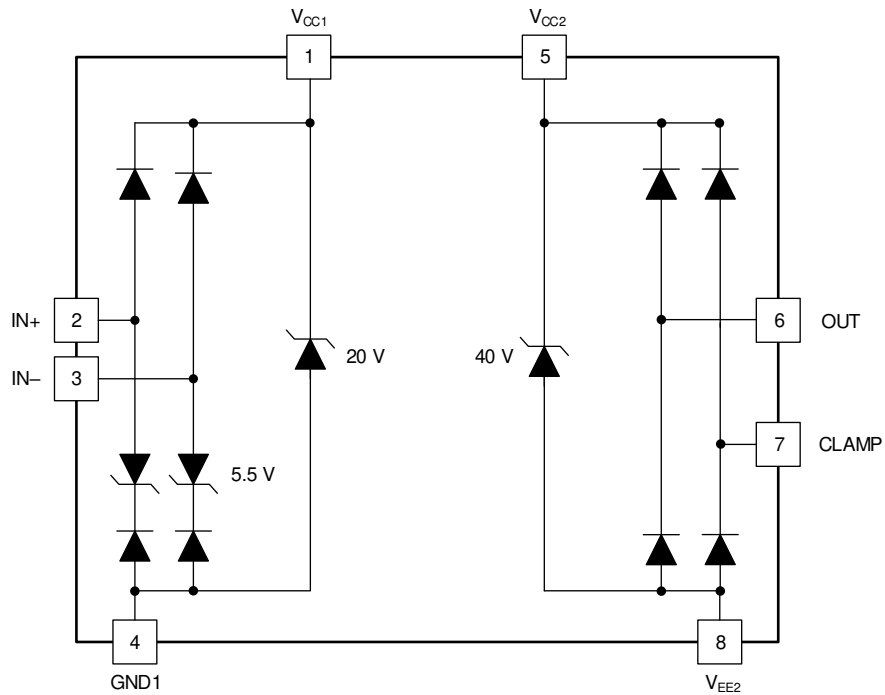
IN+	IN–	OUT
Low	X	Low
X	High	Low
High	Low	High

### 7.4.1 ESD Structure

[Figure 7-9](#) shows the multiple diodes involved in the ESD protection components of the UCC5350-Q1 device. This provides pictorial representation of the absolute maximum rating for the device.



**Figure 7-8. ESD Structure 'S' version**



**Figure 7-9. ESD Structure 'M' Version**

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

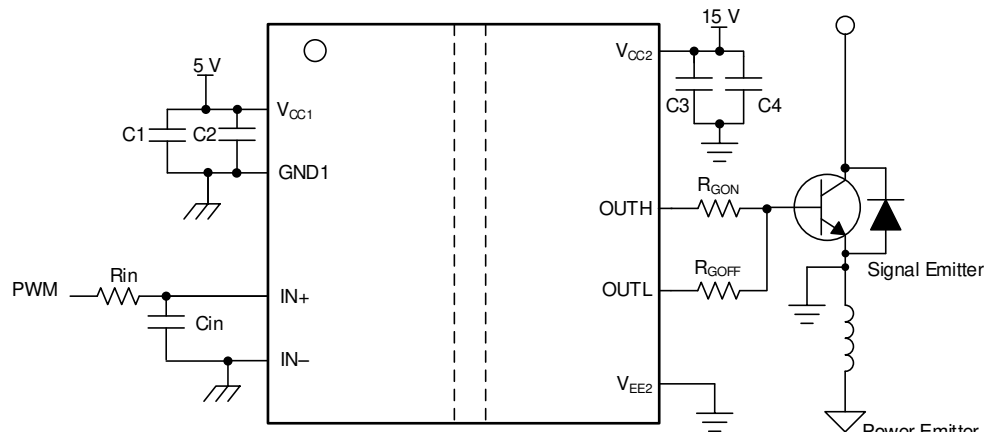
The UCC5350-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

The UCC5350-Q1 has two pinout configurations, featuring split outputs and Miller clamp. The split outputs, OUTH and OUTL, are used to separately decouple the power transistor turn on and turn off commutations.

The M version features active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The device comes in an 8-pin D and 8-pin DWV package and has creepage, or clearance, of 4 mm and 8.5 mm, respectively, which is suitable for applications where basic or reinforced isolation is required. The UCC5350-Q1 offers a 5-A minimum drive current.

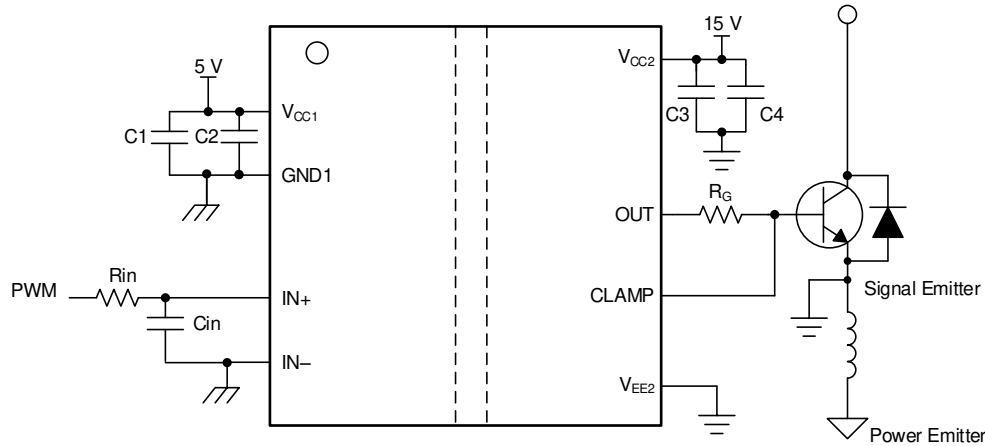
### 8.2 Typical Application

The circuits in [Figure 8-1](#) and [Figure 8-2](#) show a typical application for driving IGBTs.



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**Figure 8-1. Typical Application Circuit for UCC5350SB-Q1 to Drive IGBT**



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**Figure 8-2. Typical Application Circuit for UCC5350MC-Q1 to Drive IGBT**

### 8.2.1 Design Requirements

**Table 8-1. UCC5350-Q1 Design Requirements**

PARAMETER	VALUE	UNIT
V <sub>CC1</sub>	3.3	V
V <sub>CC2</sub> – V <sub>EE2</sub>	18	V
IN+	3.3	V
IN–	GND1	-
Switching frequency	150	kHz
Gate Charge of Power Device	126	nC

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter, R<sub>IN</sub>-C<sub>IN</sub>, can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R<sub>IN</sub> resistor with a value from 0 Ω to 100 Ω and a C<sub>IN</sub> capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for R<sub>IN</sub> is 51 Ω and C<sub>IN</sub> is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

#### 8.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors, R<sub>G(ON)</sub> and R<sub>G(OFF)</sub> are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pull-up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined typical peak source current is 10 A for UCC5350-Q1. Use Equation 1 to estimate the peak source current.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} || (R_{OH} + R_{GON} + R_{GFET\_Int})} \quad (1)$$

where

- $R_{ON}$  is the external turn-on resistance, which is  $2.2\ \Omega$  in this example.
- $R_{GFET\_Int}$  is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume  $1.8\ \Omega$  for our example.
- $I_{OH}$  is the typical peak source current which is the minimum value between 10 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak source current is approximately 3.36 A as calculated in [Equation 2](#).

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS} || R_{OH} + R_{GON} + R_{GFET\_Int}} = \frac{18\text{ V}}{1.54\ \Omega || 12\ \Omega + 2.2\ \Omega + 1.8\ \Omega} \approx 3.36\text{ A} \quad (2)$$

Similarly, use [Equation 3](#) to calculate the peak sink current.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} \quad (3)$$

where

- $R_{OFF}$  is the external turn-off resistance, which is  $2.2\ \Omega$  in this example.
- $I_{OL}$  is the typical peak sink current which is the minimum value between 10 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum value between [Equation 4](#) and 10 A.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} = \frac{18\text{ V}}{0.26\ \Omega + 2.2\ \Omega + 1.8\ \Omega} \approx 4.23\text{ A} \quad (4)$$

---

#### Note

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

---

#### 8.2.2.3 Estimate Gate-Driver Power Loss

The total loss,  $P_G$ , in the gate-driver subsystem includes the power losses ( $P_{GD}$ ) of the UCC5350-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The  $P_{GD}$  value is the key power loss which determines the thermal safety-related limits of the UCC5350-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss,  $P_{GDQ}$ , which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The  $P_{GDQ}$  parameter is measured on the bench with no load connected to the OUT pins at a given  $V_{CC1}$ ,  $V_{CC2}$ , switching frequency, and ambient temperature. In this example,  $V_{CC1}$  is 3.3V and  $V_{CC2}$  is 18 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 150 kHz, is measured to be  $I_{CC1} = 1.67\text{ mA}$  and  $I_{CC2} = 1.11\text{ mA}$ . Therefore, use [Equation 5](#) to calculate  $P_{GDQ}$ .

$$P_{GDQ} = V_{CC1} \times I_{VCC1} + (V_{CC2} - V_{EE2}) \times I_{CC2} \approx 23.31\text{ mW} \quad (5)$$

The second component is the switching operation loss,  $P_{GDO}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use [Equation 6](#) to calculate the total dynamic loss from load switching,  $P_{GSW}$ .

$$P_{GSW} = (V_{CC2} - V_{EE2}) \times Q_G \times f_{SW} \quad (6)$$

where

- $Q_G$  is the gate charge of the power transistor at  $V_{CC2}$ .

So, for this example application the total dynamic loss from load switching is approximately 340 mW as calculated in [Equation 7](#).

$$P_{GSW} = 18 \text{ V} \times 126 \text{ nC} \times 150 \text{ kHz} = 340 \text{ mW} \quad (7)$$

$Q_G$  represents the total gate charge of the power transistor and is subject to change with different testing conditions. The UCC5350-Q1 gate-driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  is equal to  $P_{GSW}$  if the external gate-driver resistance and power-transistor internal resistance are  $0 \Omega$ , and all the gate driver-loss will be dissipated inside the UCC5350-Q1. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 10 A, however, it will be non-linear if the source/sink current is saturated. The gate driver loss will be estimated in the case in which it is not saturated as given in [Equation 8](#).

$$P_{GDO} = \frac{P_{GSW}}{2} \left( \frac{R_{OH} \parallel R_{NMOS}}{R_{OH} \parallel R_{NMOS} + R_{GON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} \right) \quad (8)$$

In this design example, all the predicted source and sink currents are less than 10 A, therefore, use [Equation 9](#) to estimate the gate-driver loss.

$$P_{GDO} = \frac{340 \text{ mW}}{2} \left( \frac{12 \Omega \parallel 1.54 \Omega}{12 \Omega \parallel 1.54 \Omega + 2.2 \Omega + 1.8 \Omega} + \frac{0.26 \Omega}{0.26 \Omega + 2.2 \Omega + 1.8 \Omega} \right) \approx 53.66 \text{ mW} \quad (9)$$

where

- $V_{OUTH/L(t)}$  is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (10 A at turnon and turnoff) charging or discharging a load capacitor. Then, the  $V_{OUTH/L(t)}$  waveform will be linear and the  $T_{R\_Sys}$  and  $T_{F\_Sys}$  can be easily predicted.

Use [Equation 10](#) to calculate the total gate-driver loss dissipated in the UCC5350-Q1 gate driver,  $P_{GD}$ .

$$P_{GD} = P_{GDQ} + P_{GDO} = 25.31 \text{ mW} + 53.66 \text{ mW} = 78.97 \text{ mW} \quad (10)$$

#### 8.2.2.4 Estimating Junction Temperature

Use the equation below to estimate the junction temperature ( $T_J$ ) of the UCC5350-Q1 family.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (11)$$

where

- $T_C$  is the UCC5350-Q1 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$  is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance ( $R_{\theta JC}$ ) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The  $R_{\theta JC}$  resistance can only be used effectively when most of the thermal energy is released through the case,

such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of  $R_{\theta JC}$  will inaccurately estimate the true junction temperature. The  $\Psi_{JT}$  parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

### 8.2.2.5 Selecting $V_{CC1}$ and $V_{CC2}$ Capacitors

Bypass capacitors for the  $V_{CC1}$  and  $V_{CC2}$  supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

#### Note

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1- $\mu$ F X7R capacitor is measured to be only 500 nF when a DC bias of 15- $V_{DC}$  is applied.

#### 8.2.2.5.1 Selecting a $V_{CC1}$ Capacitor

A bypass capacitor connected to the  $V_{CC1}$  pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the  $V_{CC1}$  pin, a tantalum or electrolytic capacitor with a value greater than 1  $\mu$ F should be placed in parallel with the MLCC.

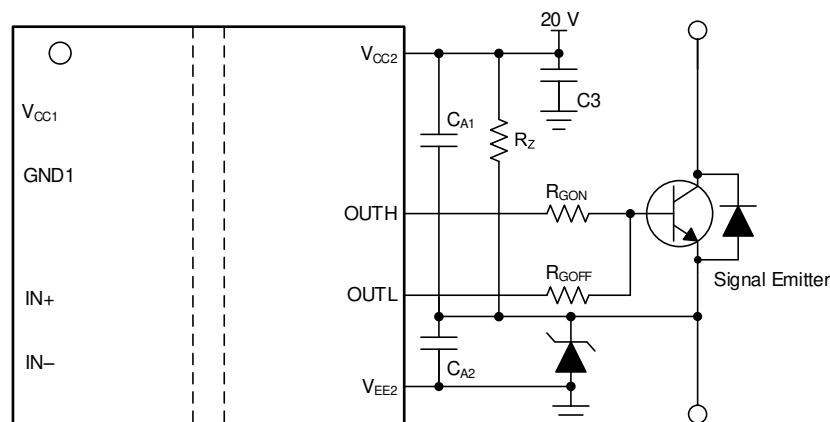
#### 8.2.2.5.2 Selecting a $V_{CC2}$ Capacitor

A 50-V, 10- $\mu$ F MLCC and a 50-V, 0.22- $\mu$ F MLCC are selected for the  $C_{VCC2}$  capacitor. If the bias power supply output is located a relatively long distance from the  $V_{CC2}$  pin, a tantalum or electrolytic capacitor with a value greater than 10  $\mu$ F should be used in parallel with  $C_{VCC2}$ .

#### 8.2.2.5.3 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turn-on and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

Figure 8-3 shows the first example with negative bias turn-off on the output using a Zener diode on the isolated power-supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply is equal to 20 V, the turn-off voltage is  $-5.1$  V and the turn-on voltage is  $20$  V  $-$   $5.1$  V  $\approx$  15 V.



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Figure 8-3. Negative Bias With Zener Diode on Iso-Bias Power-Supply Output

Figure 8-4 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across  $V_{CC2}$  and the emitter determines the positive drive output voltage and the power supply across  $V_{EE2}$  and the emitter determines the negative turn-off voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

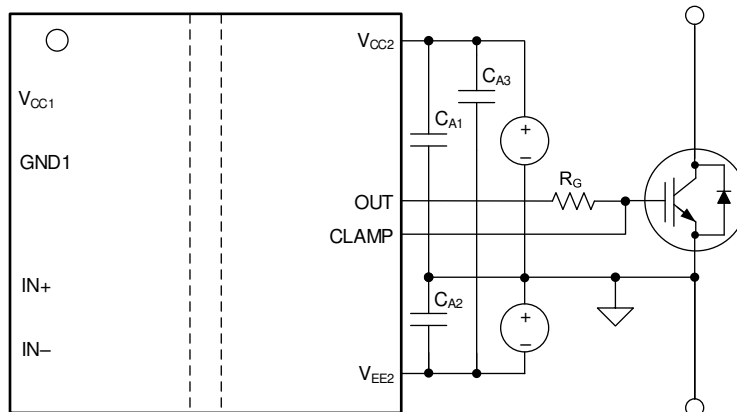
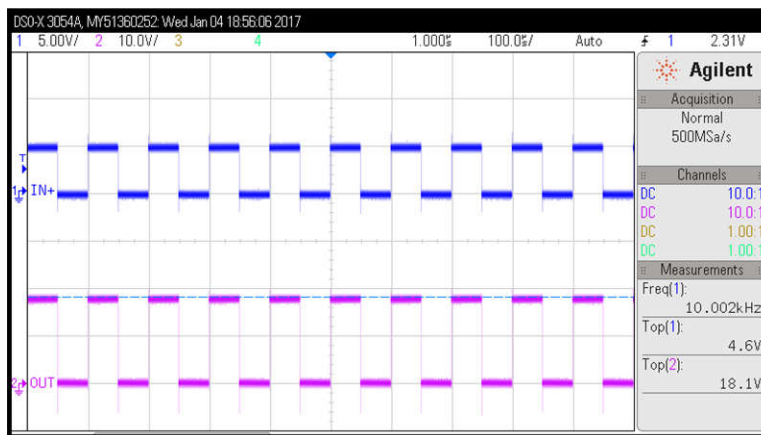


Figure 8-4. Negative Bias With Two Iso-Bias Power Supplies

### 8.2.3 Application Curve



$V_{CC2} = 20\text{ V}$        $V_{EE2} = \text{GND}$        $f_{\text{SW}} = 10\text{ kHz}$

Figure 8-5. PWM Input and Gate Voltage Waveform

## 9 Power Supply Recommendations

The recommended input supply voltage ( $V_{CC1}$ ) for the UCC5350-Q1 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage ( $V_{CC2}$ ) is determined by the internal UVLO protection feature of the device. The  $V_{CC1}$  and  $V_{CC2}$  voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50  $\mu\text{s}$  by the UVLO protection feature. For more information on UVLO, see Section 7.3.4.1. The higher limit of the  $V_{CC2}$  range depends on the maximum gate voltage of the power device that is driven by the UCC5350-Q1 device, and should not exceed the recommended maximum  $V_{CC2}$  of 33 V. A local bypass capacitor should be placed between the  $V_{CC2}$  and  $V_{EE2}$  pins, with a value of 220-nF to 10- $\mu\text{F}$  for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the  $V_{CC1}$  and GND1 pins. Given the small amount

of current drawn by the logic circuitry within the input side of the UCC5350-Q1 device, this bypass capacitor has a minimum recommended value of 100 nF.

## 10 Layout

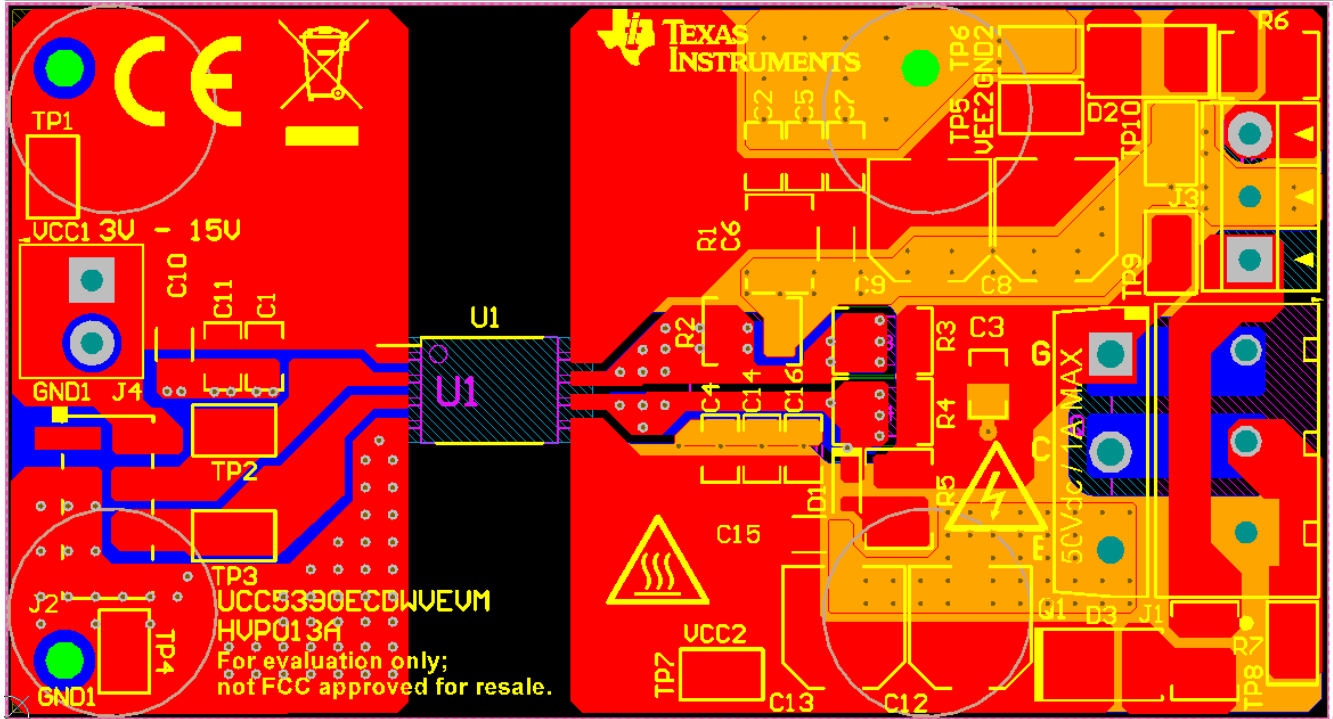
### 10.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC5350-Q1. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the  $V_{CC1}$  and GND1 pins and between the  $V_{CC2}$  and  $V_{EE2}$  pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the  $V_{EE2}$  pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC5350-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (for more information, see [Section 8.2.2.3](#)). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ( $\theta_{JB}$ ).
  - Increasing the PCB copper connecting to the  $V_{CC2}$  and  $V_{EE2}$  pins is recommended, with priority on maximizing the connection to  $V_{EE2}$ . However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the  $V_{CC2}$  and  $V_{EE2}$  pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

### 10.2 Layout Example

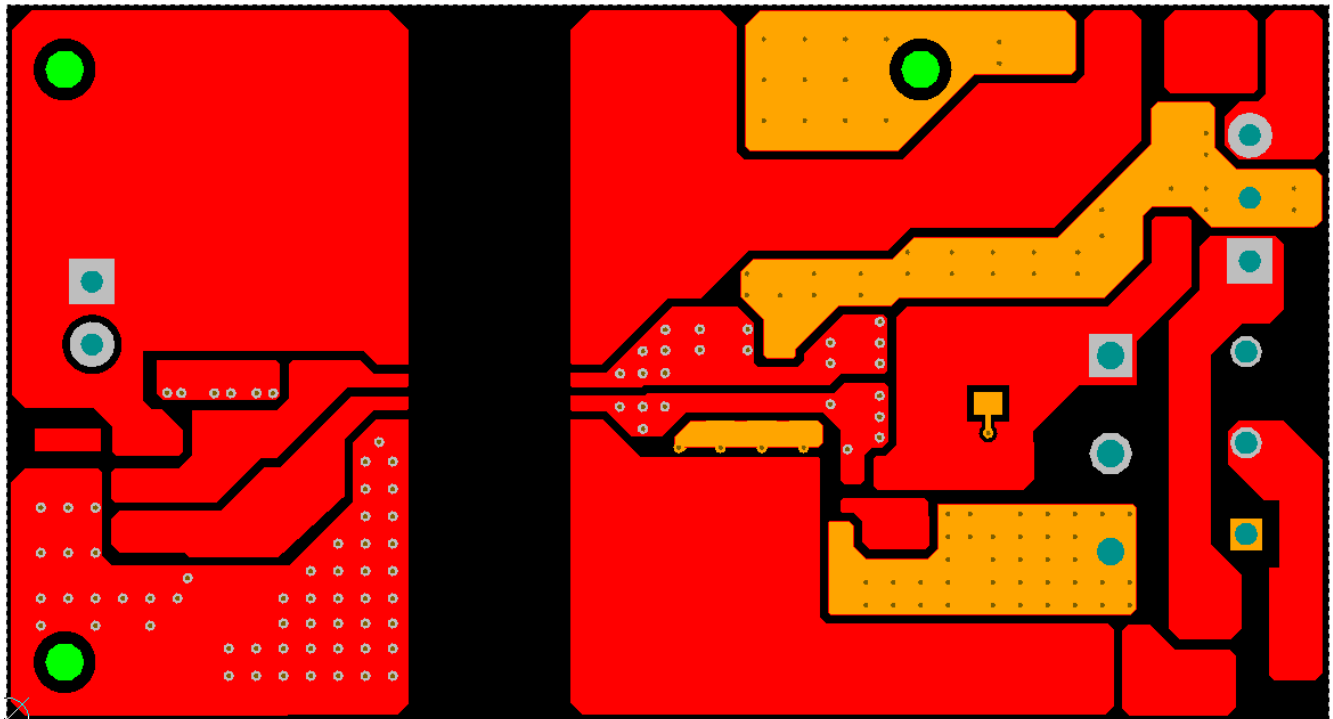
[Figure 10-1](#) shows a PCB layout example with the signals and key components labeled. The UCC5390ECDWV evaluation module (EVM) is given as an example, available in the same DWV package as the UCC5350-Q1. The UCC5390EC has a split emitter versus Miller clamp so although the layout is not exactly the same, general guidelines and practices still apply. The evaluation board can be configured for the Miller clamp version, as well, as described in the [UCC5390ECDWV Isolated Gate Driver Evaluation Module User's Guide](#).



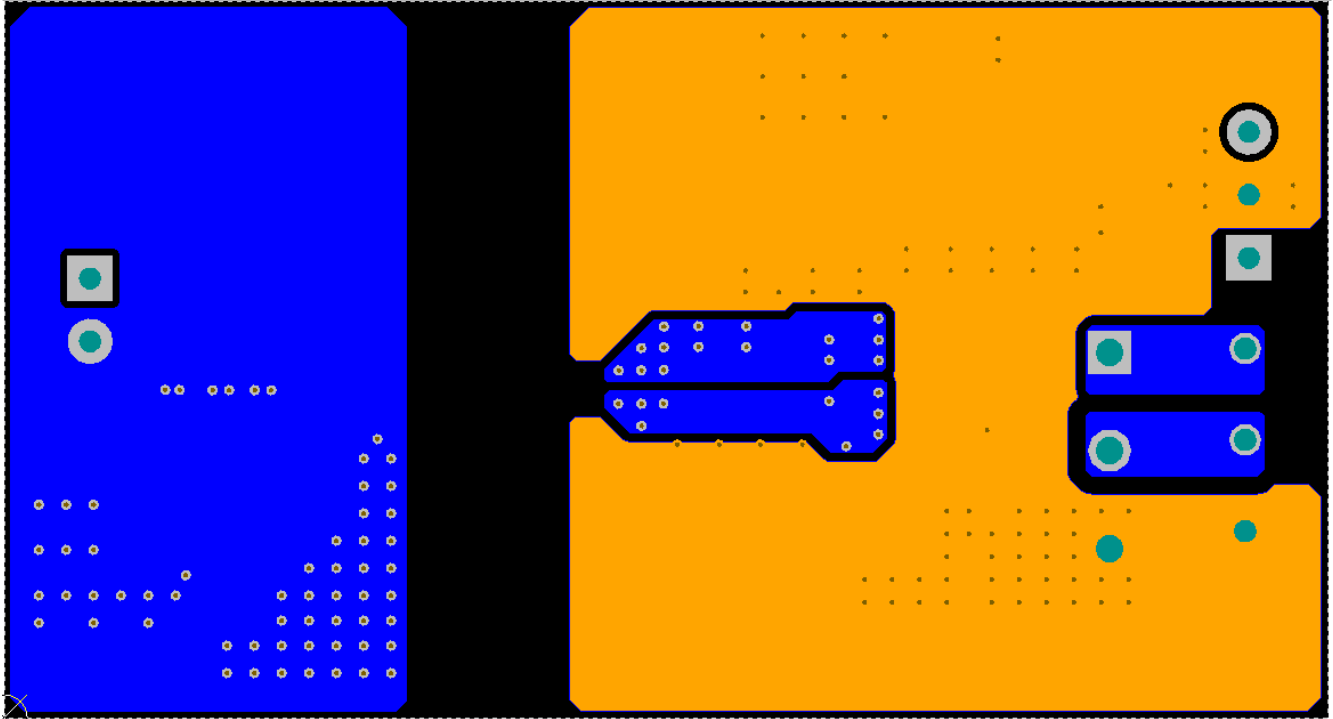
A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

**Figure 10-1. Layout Example**

Figure 10-2 and Figure 10-3 show the top and bottom layer traces and copper.

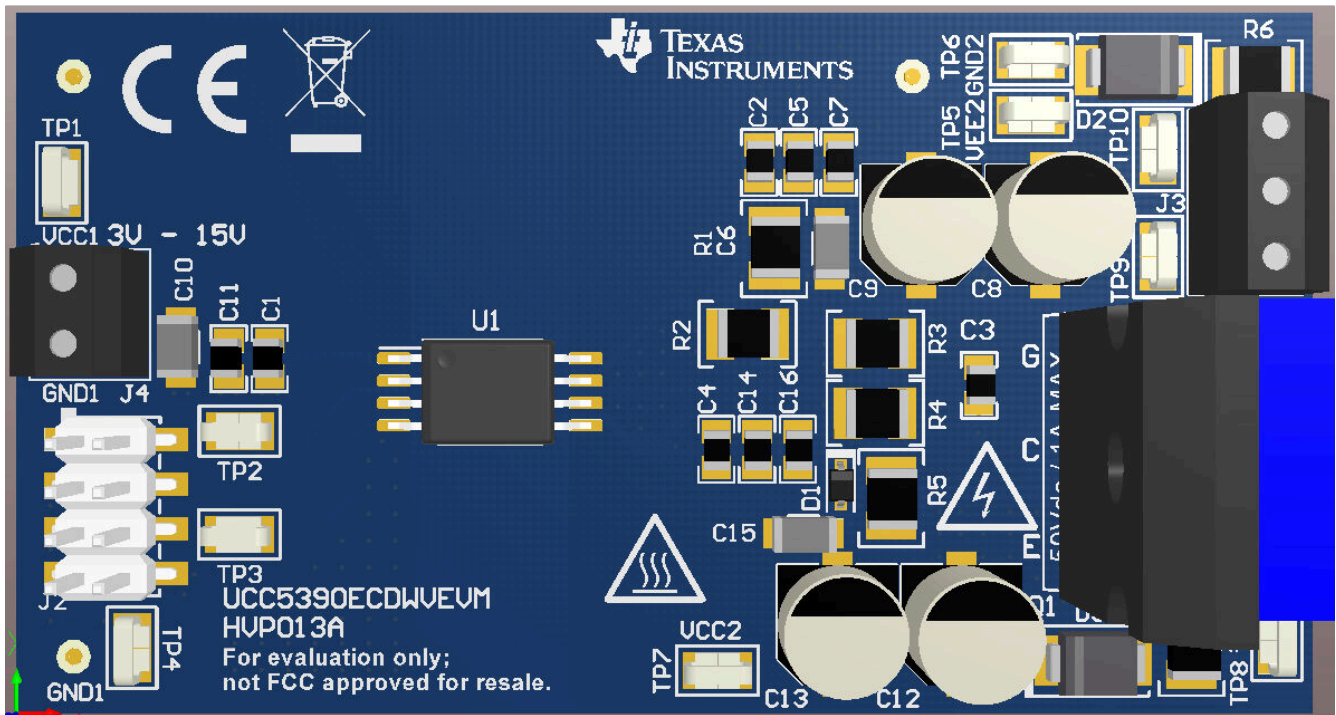


**Figure 10-2. Top-Layer Traces and Copper**



**Figure 10-3. Bottom-Layer Traces and Copper (Flipped)**

Figure 10-4 shows the 3D layout of the top view of the PCB.



**Figure 10-4. 3-D PCB View**

### 10.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

Figure 10-5 shows the recommended layer stack.

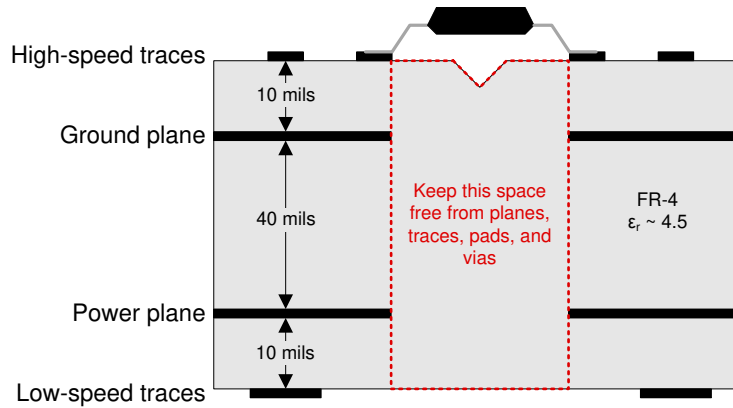


Figure 10-5. Recommended Layer Stack

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

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### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#)
- Texas Instruments, [UCC5390ECDWV Isolated Gate Driver Evaluation Module user's guide](#)
- Texas Instruments, [UCC53x0xD Evaluation Module user's guide](#)

### 11.3 Certifications

UL Online Certifications Directory, ["FPPT2.E181974 Nonoptical Isolating Devices - Component" Certificate Number: 20170718-E181974](#),

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.5 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 11.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision F (July 2024) to Revision G (January 2025)</b>	<b>Page</b>
• Updated Safety-related certifications in Features.....	1
• Changed $V_{IORM}$ from 990 to 1200V <sub>PK</sub> , to reflect $V_{IOWM}$ update.....	6
• Changed $V_{IOWM}$ (AC voltage) from 700 to 850V <sub>RMS</sub> , since UCC5350 is production tested with 850V <sub>RMS</sub> × 1.5 in an IEC partial discharge test. Previously, TI decided to spec the $V_{IOWM}$ more conservatively .....	6
• Changed $V_{IOWM}$ (DC voltage) from 990 to 1200V <sub>DC</sub> , to reflect $V_{IOWM}$ update.....	6
• Added $V_{IMP}$ according to IEC 60747-17 test definition in air (D package).....	6
• Changed $V_{IOSM}$ (DC voltage) from 4242 to 6500V <sub>DC</sub> , replacing VDE 0884-11 surge test voltage definition to IEC 60747-17 test definition in oil (D package).....	6
• Added $V_{IMP}$ according to IEC 60747-17 test definition in air (DWV package).....	8
• Changed $V_{IOSM}$ (DC voltage) from 8000 to 10400V <sub>DC</sub> , replacing VDE 0884-11 surge test voltage definition to IEC 60747-17 test definition in oil (DWV package).....	8
• Updated Safety-Related Certifications For D Package.....	9
• Changed VDE V 0884–11:2017–01 to IEC 60747-17 (VDE 0884-17) in Safety-Related Certifications for the DWV package.....	9
• Corrected propagation delay tolerance.....	11
• Added Insulation Lifetime Projection Data graph in Insulation Characteristics Curves.....	12

<b>Changes from Revision E (February 2024) to Revision F (July 2024)</b>	<b>Page</b>
• Deleted HBM and CDM ESD classifications from Features.....	1
• Added Functional Safety bullets to Features.....	1
• Added ±10A typical peak current drive strength to Features.....	1
• Updated Safety-Related Certifications For DWV Package.....	9
• Added the VDE information for the DWV package.....	9

<b>Changes from Revision D (August 2022) to Revision E (February 2024)</b>	<b>Page</b>
• Changed current from 5A min to 10A typ.....	1
• Changed CTI and Material Group values in insulation specifications and added table note.....	6

<b>Changes from Revision C (June 2022) to Revision D (August 2022)</b>	<b>Page</b>
• Changed UCC5350SB-Q1 from Advance Information to Production Data.....	1
• Added the "Connect to gate directly with low inductance" to CLAMP <a href="#">Section 4</a> Removed "Use Table 8.4 to understand the input and output logic of these devices" from IN+ and IN- <a href="#">Section 4</a> .....	4

<b>Changes from Revision B (June 2020) to Revision C (June 2022)</b>	<b>Page</b>
• Added the Advance Information for the UCC5350SBQDRQ1 device.....	1
• Added the UCC5350SB device to <a href="#">Section 4</a> .....	4
• Added SB-Q1 D package power ratings.....	6
• Added SB-Q1 insulation specs.....	6
• Added the UL certificate number for the D package.....	9
• Added the UL certificate number for the DWV package.....	9
• Added SB-Q1 D package safety limiting values.....	9
• Added SB-Q1 parameters.....	10
• Added minimum pulse width specs.....	11
• Added <a href="#">Table 7-4</a> .....	23
• Added SB-Q1 ESD figure .....	23

- 
- Added typical application circuit for SB-Q1..... [25](#)
- 

### **13 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC5350MCQDWVQ1	Obsolete	Preproduction	SOIC (DWV)   8	-	-	Call TI	Call TI	-40 to 125	
<a href="#">UCC5350MCQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	Call TI   Nipdau	Level-2-260C-1 YEAR	-40 to 125	5350Q
UCC5350MCQDRQ1.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350Q
<a href="#">UCC5350MCQDWVRQ1</a>	Active	Production	SOIC (DWV)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ
UCC5350MCQDWVRQ1.A	Active	Production	SOIC (DWV)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350MCQ
<a href="#">UCC5350SBQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	Call TI   Nipdau	Level-3-260C-168 HR	-40 to 125	5350Q
UCC5350SBQDRQ1.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	5350Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF UCC5350-Q1 :**

- Catalog : [UCC5350](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5350MCQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5350MCQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
UCC5350SBQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5350MCQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
UCC5350MCQDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0
UCC5350SBQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

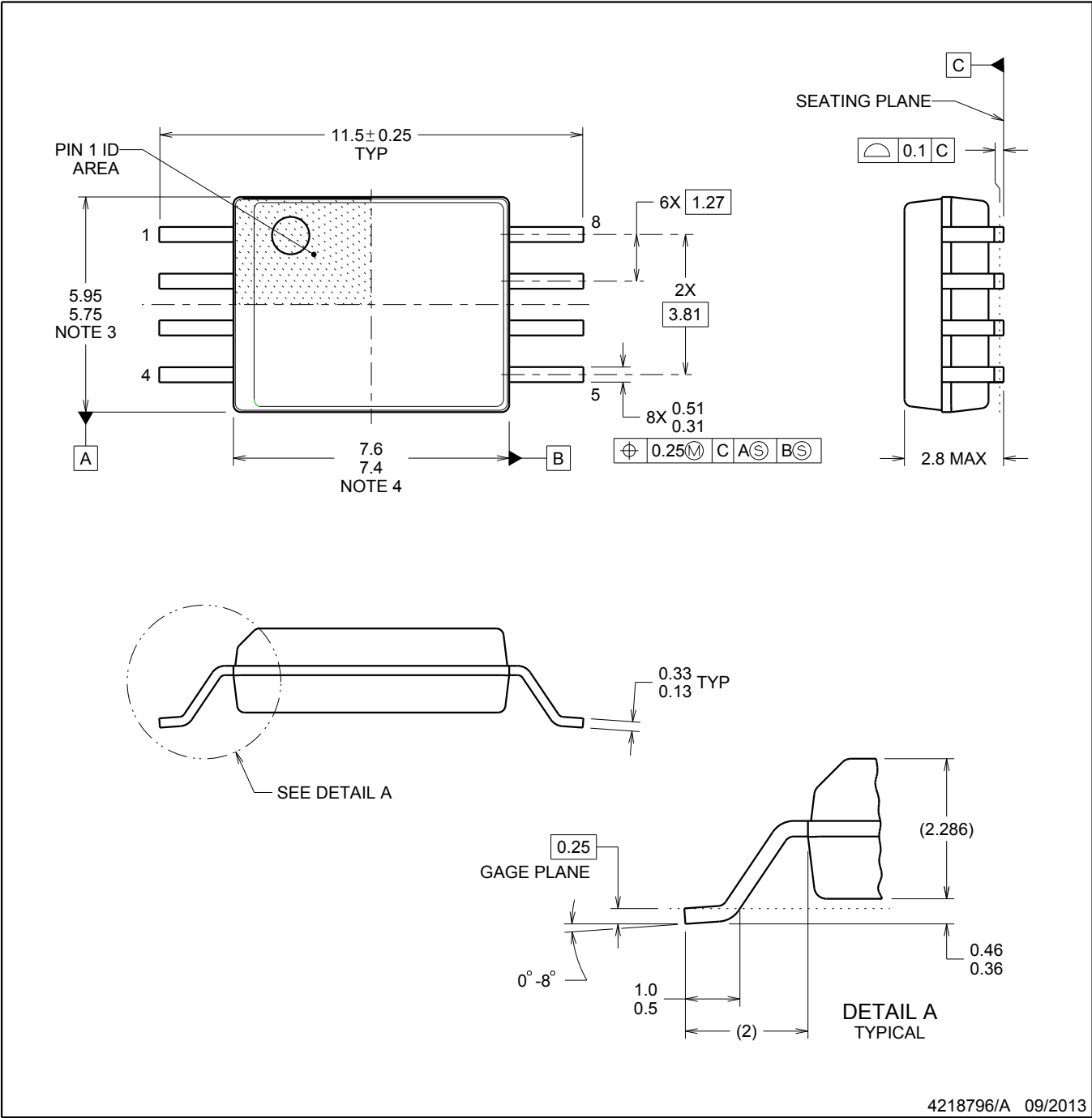
# PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

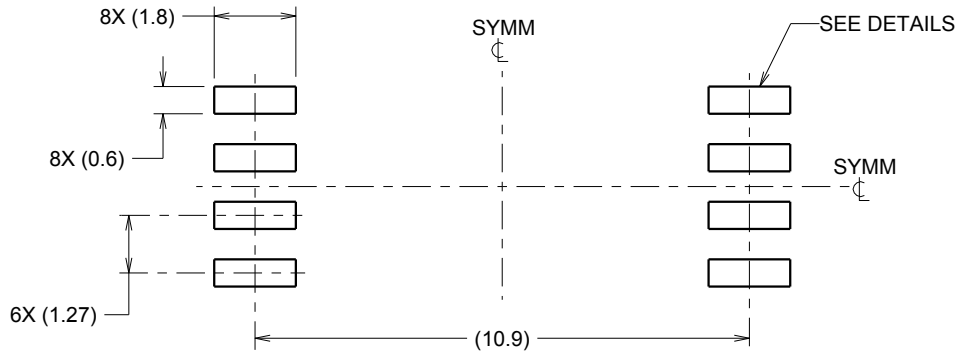
SOIC



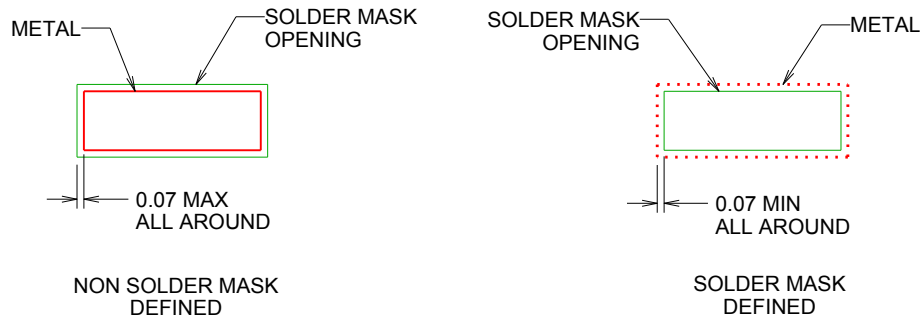
4218796/A 09/2013

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE:6X

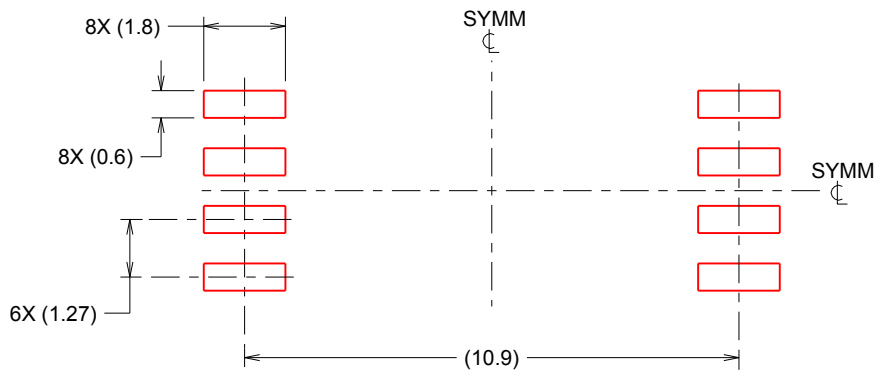


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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