Design Summary for 3- and 5-Pin KTT Packages

(Complies to JEDEC TO-263 AA and BA)

Introduction

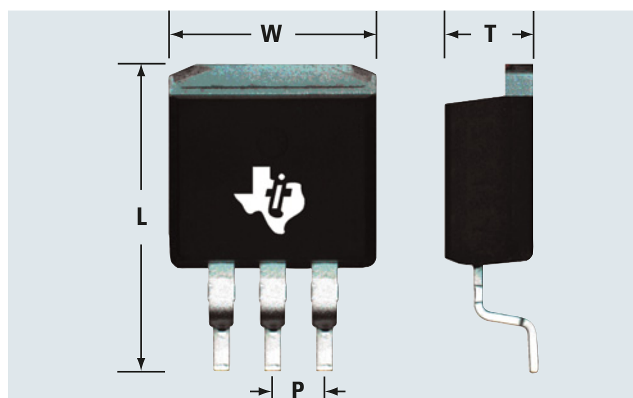
Texas Instruments (TI) introduces the KTT packages, registered in JEDEC Standard TO-263 as variation AA for the 3-pin version and variation BA for the 5-pin version. The KTT packages meet or exceed the requirements set forth in the European Union's RoHS legislation; the packages are suitable for high-temperature, Pb-Free soldering processes. They have an exposed pad that enhances thermal performance, enabling high-power applications such as low-dropout (LDO) regulators. The KTT plastic encapsulated packages use conventional copper-lead-frame technology for a cost-effective solution. They ship in tape-and-reel format.

Package Details

	3-Pin KTT	5-Pin KTT
Length, L (mm)*	15,24	15,24
Width, W (mm)*	10,16	10,16
Thickness, T (mm)**	4,83 Max	4,83 Max
Pitch, P (mm)*	2,54	1,70
Lead Finish	Matte Sn	Matte Sn
RoHS-Compliant	Yes	Yes
Moisture Sensitivity Level (JEDEC)	Level 3/245°C	Level 3/245°C

* Nominal dimensions shown.
** The package seating height will depend on the solder paste volume and land pad design.

3-Pin KTT Package



Electrical Characteristics

The electrical package parasitic was achieved through electrical modeling and is based on a 2D model. Actual electrical data may differ slightly from simulated results.

Description	R (Ω)	L (nH)	C (pF)
3-Pin KTT Package Parasitics	0.054	5.427	0.770
5-Pin KTT Package Parasitics	0.043	4.612	0.649

Thermal Characteristics

The results in the table are modeled. These modeled test boards utilized 5% top-layer Cu coverage in addition to an 8.4 × 4.8-mm land pad and 1 W of power.

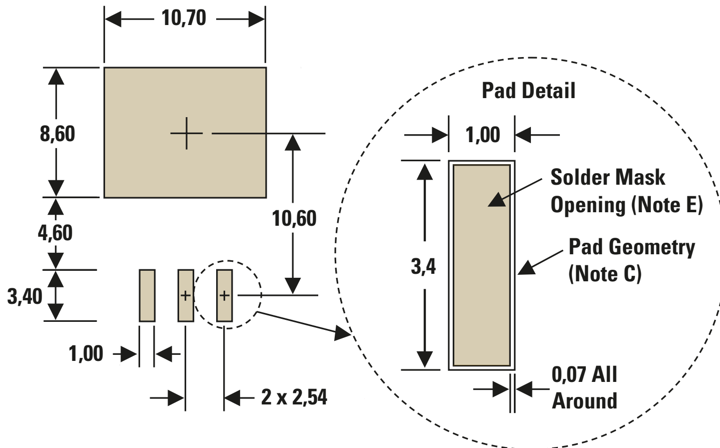
KTT Thermal Impedance with Die Size 4 x 4 mm

Thermal Impedance (°C/W)	3-Pin KTT	5-Pin KTT	Description
$R_{\theta JA}$	26.9	26.5	High K with Vias 51-5 Using JEDEC 2S2P Test Board and 5 × 8 Thermal Via
$R_{\theta JC}$	32.27	31.8	Low K with 51-3 Using JEDEC 1S1P Test Board and Upper Cold Block
$R_{\theta JP}$	0.39	0.38	Lower Cold Plate

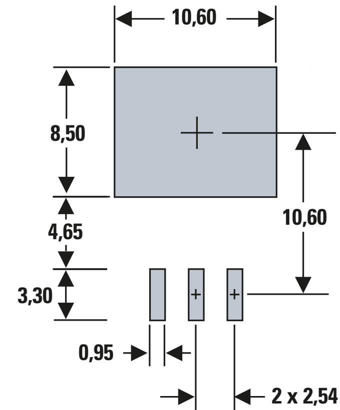
PCB Design Guidelines

Although TI recommends nonsolder-mask-defined (NSMD) pads over solder-mask-defined (SMD) pads for surface mounting KTT packages, both can be utilized. NSMD allows tighter tolerance on copper etching and, due to the exposed edges free from solder mask, provides a larger solderable area that improves solder-joint reliability.

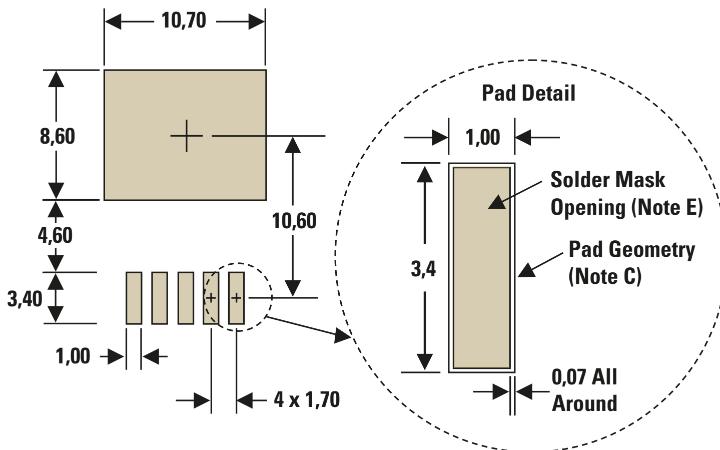
3-Pin KTT Recommended PCB Land Pad Design



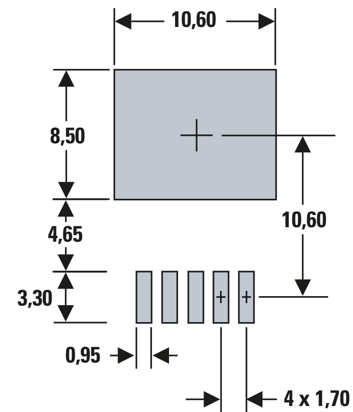
3-Pin KTT Recommended Stencil Design (See Note E)



5-Pin KTT Recommended PCB Land Pad Design



5-Pin KTT Recommended Stencil Design (See Note E)



NOTES:
- A. All dimensions are in millimeters.
- B. These drawings are subject to change without notice.
- C. Publication IPC-7351 is an alternate information source for PCB land pattern designs.
- D. Laser-cutting apertures with trapezoidal walls and rounded corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PCB Design Guidelines (Continued)

Solder Paste Recommendations

TI recommends the use of type 3 or finer solder paste for mounting the KTT packages. Using paste offers the following advantages:

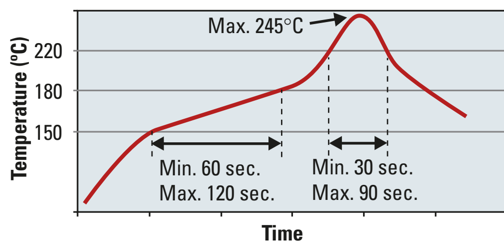
- The paste contains flux to aid solder wetting to the PCB land.
- The adhesive properties of the paste will hold the component in place during manufacture.
- Paste by volume typically contains around 50% metal load and can be varied by print volume for calculating the amount of paste necessary to form a given solder joint. KTT packages are typically manufactured with printed pad volumes of ~90% to 100% by area but can be reduced if necessary. Customers should contact their SMT manufacturing site for recommendations.
- Paste contributes to the final volume of solder in the joint, allowing it to vary for an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty of cleaning under the mounted components.

IR Reflow Profiles

The KTT’s matte Sn lead finish is compatible with both lead and lead-free solder pastes.

TI recommends following the solder paste supplier’s recommendations to optimize flux activity and to achieve proper alloy melting temperatures within J-STD-20 guidelines. The figure below shows a range of temperatures that TI packages can withstand without risking reliability; however, TI prefers parts to be processed with the lowest peak temperature possible below the component’s peak temperature rating as listed on the MSL label. The exact profile depends on that rating, the solder paste manufacturer’s recommendation, complexity of the PWB and the capability of the reflow equipment to be confirmed by the SMT assembly operation.

Recommended Temperature Profile for SnAgCu Pb-Free Solder Paste



Reflow Parameters

	Pb-Free
Ramp Rate	3°C/sec. Max.*
Preheat	150 to 180°C
	60 to 120 sec.
Time Above Liquidus	220°C
	30 to 90 sec.
Peak Temp.	245°C (+0/–5°C)
Time Within 5°C Peak Temp.	10 to 20 sec.
Ramp Down Rate	6°C/sec. Max.

*No testing with a forced cooldown of 6°C/sec. has been conducted.

Test Sockets

This socket is given as an example; others may be available for use.

Package Designator	Package Type	Orderable Part Number	Vendor
3-Pin KTT	TO-263/AA	410-006-11	CTI
5-Pin KTT	TO-263/BA	02937-052-X2X5	Loranger

Package Repair Guidelines

KTT Repair Procedure

A hot-gas repair/rework station (i.e., Air-Vac Engineering, Metcal or Denon) is strongly recommended for this process.

Package replacement procedure:

- Bake PWB and package at 125°C for 48 hours prior to rework. See IPC/JEDEC J-STD-033 Bake Conditions for further information.
- Preheat board (bake is recommended).
- Reflow component solder.
- Vacuum to remove component.
- Clean and prepare PWB lands.
- Screen solder paste either onto the part or onto the board.
- Place and reflow new component.
- Inspect solder joints.
- Place and reflow new component.
- Inspect solder joints.

Repair procedure notes:

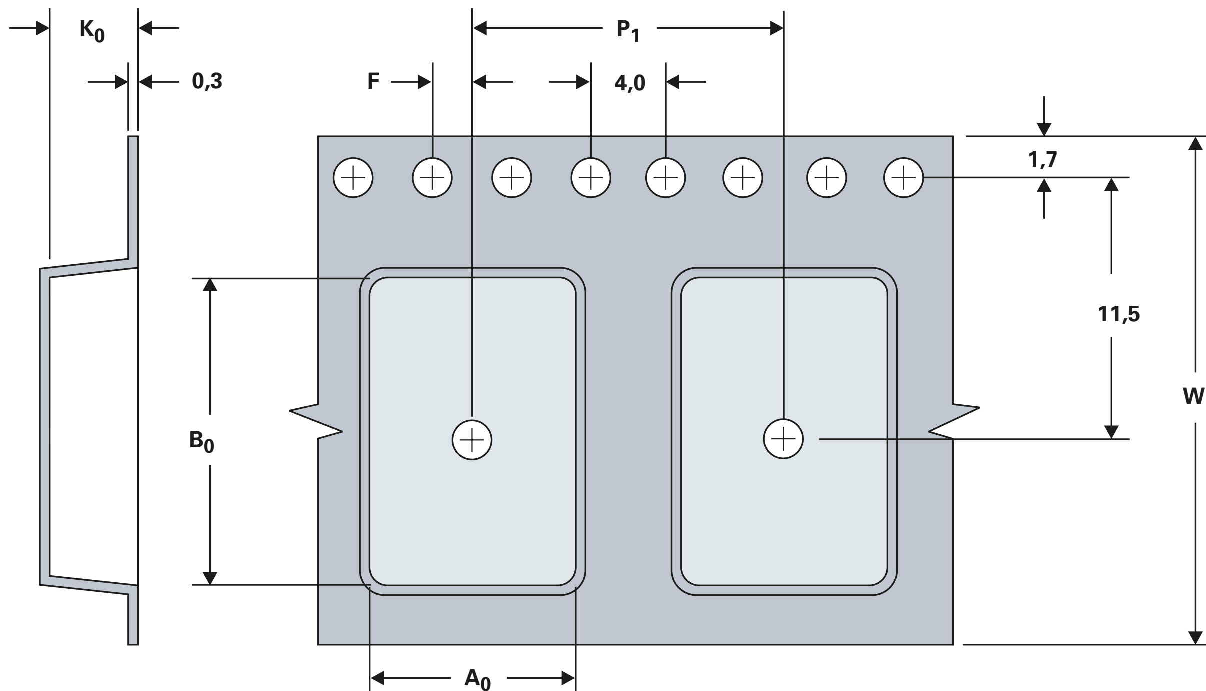
- Reuse of a removed package is not recommended.
- Utilize a new package for the repair process. The new package should be kept dry and should not exceed the stated floor life after the dry pack has been opened.
- If the package has exceeded the floor life, rebake it for 48 hours at 125°C.
- Rebake a package only a maximum of three times.

Packaging Tape and Reel

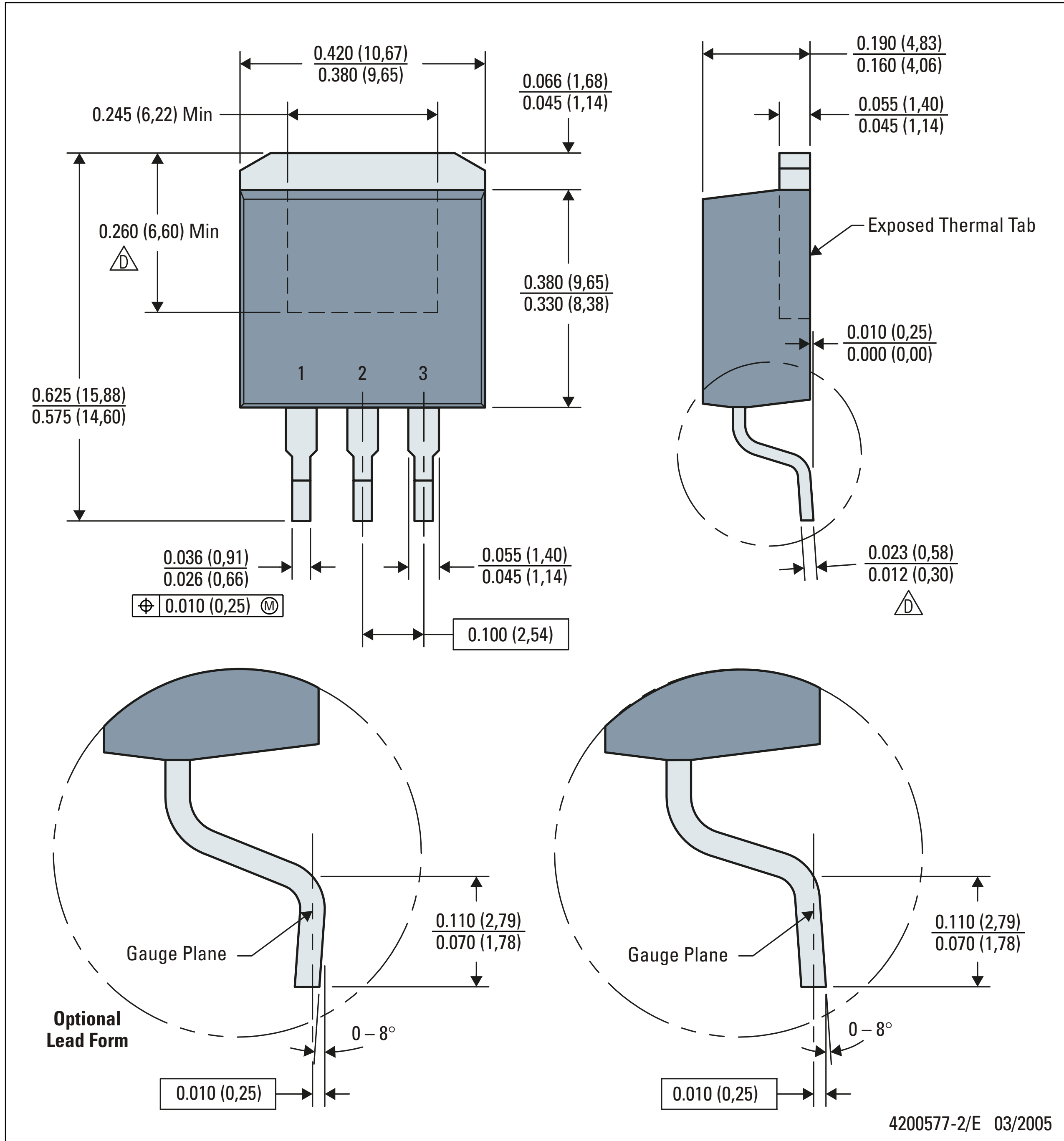
Carrier Tape Dimensions (Millimeters)

	Carrier Tape Width (W)	Pocket Pitch (P_1)	Pocket Width (A_0)	Pocket Length (B_0)	Pocket Depth (K_0)	Hole to Pocket CL (F)	Reel	
							Dia.	SPQ/MOQ*
KTT	24	16	10,60	15,80	4,90	2,0	330	1000

*SPQ = standard pack quantity; MOQ = minimum order quantity.



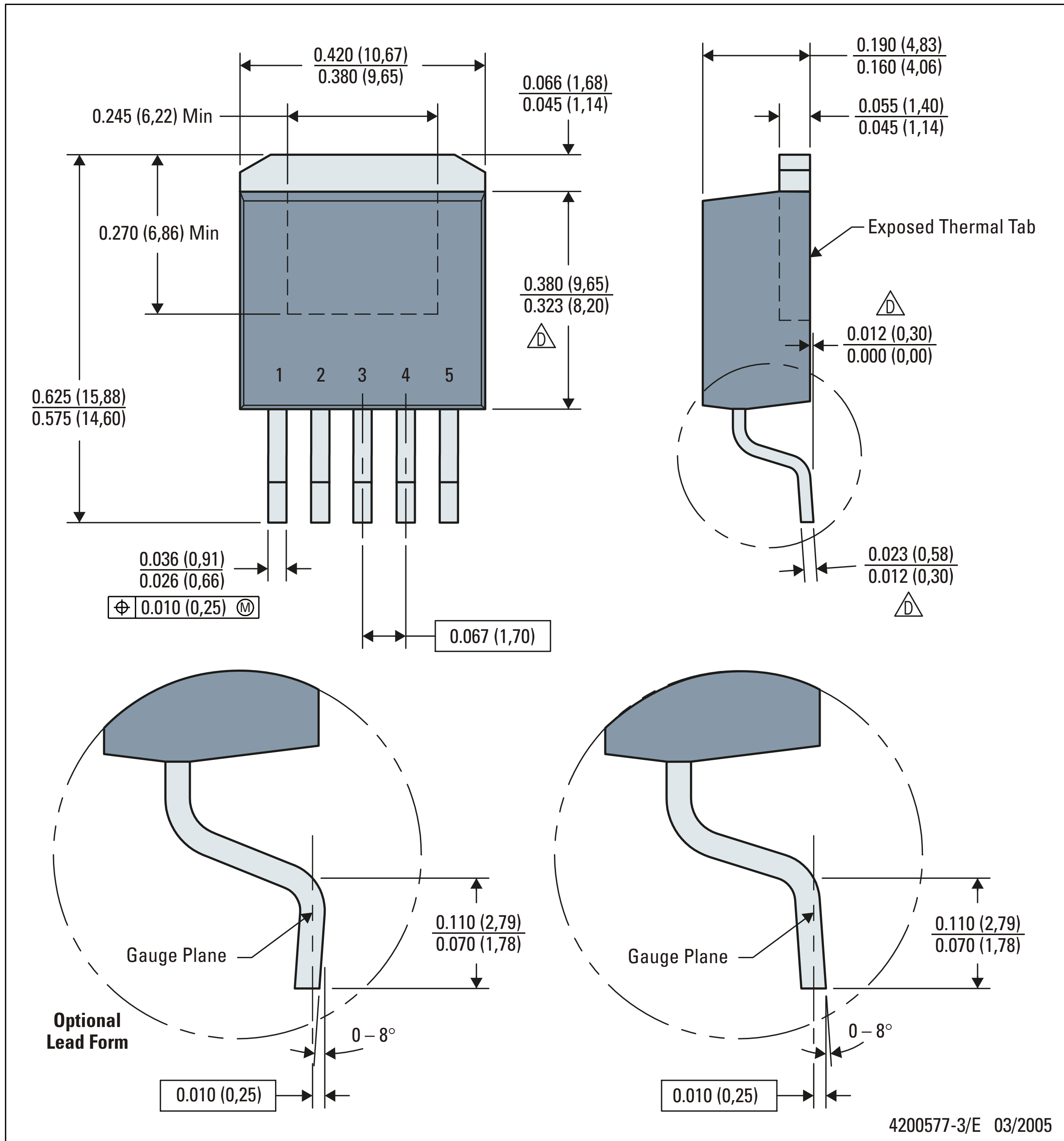
3-PIN KTT (R–PSFM–G3) PLASTIC FLANGE-MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.005 (0,13) per side.
D Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minum exposed pad length.

Please visit www.ti.com/packaging for more information.

5-PIN KTT (R–PSFM–G5) PLASTIC FLANGE-MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height and minimum body length.

Please visit www.ti.com/packaging for more information.

Q. Is package rework possible? Are tools available?

A. Yes, rework is possible, and there are several semi-automatic SMT rework machines and profiles available. However, TI does not guarantee the reliability of reused packages. It is best to discard and replace any package that fails test.

Q. What alignment accuracy is possible?

A. Alignment accuracy for the KTT packages is dependent on board-level pad tolerance, placement accuracy and lead position tolerance. Nominal lead position tolerances are specified at ±50 microns. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy. To maximize the self-alignment effect of the KTT packages, it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded. A good guide is to subject the PCB to a temperature ramp not exceeding 4°C/sec.

Q. What size land pad should I design on my board for these packages?

A. Pad size is the key to board-level reliability, and TI strongly recommends following the design rules included in this design summary.

Q. Can the solder joints be inspected after reflow?

A. Many customers are achieving satisfactory results during process setup with lamographic X-ray techniques.

Q. What factors can increase KTT assembly yields?

A. TI recommends the following solder paste quality:

- PCB-quality, uniform viscosity and texture. Free from foreign material. Protect paste from drying out on the solder stencil.
- PCB-quality, clean, flat, plated or coated solder land area. Attachment surface must be clean and free of solder-mask residue.
- KTT packages self-center accurately as long as a major portion (more than 50%) of the lead finger is in contact with the solder-paste-covered land area on the board.
- A solder reflow profile should be developed for each PCB type with various packages.
- Solder volume is important to ensure optimum contact of all intended solder connections.
- TI recommends using a recommended stencil design to minimize the amount of solder paste on the bottom side of the board during assembly.

Q. Is TI developing a RoHS version of KTT?

A. Yes, TI has developed the KTT packages to comply with all RoHS/lead-free environmental policies. Check with your local TI field sales representative for sample availability.

Q. Are there any EMI concerns for traces under the package? How can I design my board to minimize EMI?

A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:

- Solid ground and power planes can be used in the design. Partitioned ground and power planes must be avoided, as they may create complex current loops that increase radiation.
- Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance, causing signal degradation.
- Minimize power-supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced with this method.

Q. What are the time requirements for floor life on these packages?

A. Moisture absorption is a significant factor in popcorn-type defects during reflow. Since these packages are classified as moisture level 3, the first and second reflow have to be completed within 168 hours after the moisture barrier bag is opened. If this time frame cannot be met, it is highly recommended to bake the packages at 125°C for 48 hours prior to reuse.

Q. Can I mount KTT packages on the bottom side of the PCB board?

A. Yes. The ideal second-reflow profile is the same as the first (the IR profile is recommended in this design summary).

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