Circuit Design and Power Loss Analysis of a Synchronous Switching Charger with Integrated MOSFETs for Li-Ion Batteries

Jinrong Qian and Lingyin Zhao, Texas Instruments

ABSTRACT

Driven by integrated functionality and shrinking form-factors, the demand for portable devices such as cellular phones, PDAs and portable DVD players has grown significantly during the last few years. The power source has quickly become a bottleneck for advancing technology, and improvement of battery-power density cannot keep-up with demand. The lithium-ion (Li-Ion) battery is widely-adopted because of its high energy density on both a gravimetric and volumetric basis. To achieve longer system run-time and smaller size, more and more system designers are finding that improving a system's power conversion efficiency with advanced circuit topologies is no longer sufficient. Battery charging has become another area to focus on for maximizing battery capacity and extending its service cycle-life. The linear charger is suitable for the low-capacity battery charge applications with its reasonable cost and small-size advantages. With the increasing power demand from portable devices, the linear battery charger no longer adequately meets charge requirements due to its high-power dissipation. This paper presents a MHz synchronous switching battery charger to efficiently charge the battery and extend its cycle-life. The design considerations and detail power loss analysis are provided to estimate the IC junction temperature

I. HOW TO CHARGE A LI-ION BATTERY

Fig. 1 shows a popular charge profile recommended for a Li-Ion battery. Most dedicated Li-Ion-charge integrated circuits (ICs) are designed to charge the battery in this manner. The charging of a Li-Ion battery consists of three charging phases: pre-charge; fast-charge constant current (CC); and fast-charge constant voltage (CV). In the pre-charge phase, the battery is charged at a low-rate (typical of 1/10 the fast charge rate) when the battery cell voltage is below 3.0 V. This provides recovery of the passivating layer which might be dissolved after prolonged storage in deep discharge state. It also prevents overheating at 1C charge when partial copper decomposition appears on anode-shorted cells on over-discharge. When the battery cell voltage reaches 3.0 V, the charger enters to the CC phase.

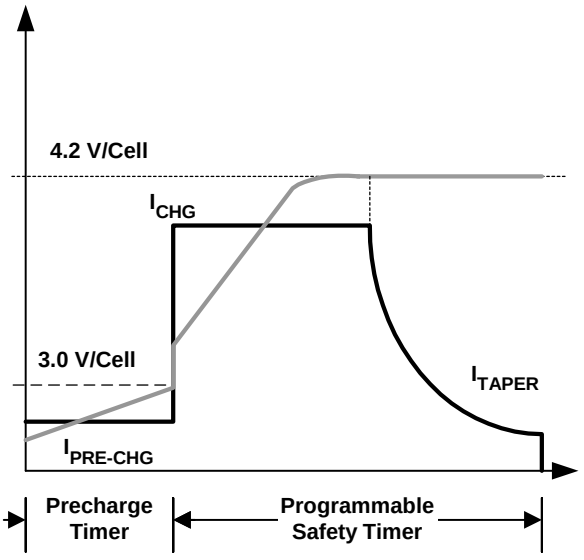

Fig. 1. Li-Ion battery charge profile.

Fast-charge current should be limited to 1-C rate (0.7-C rate typical) to prevent overheating and resulting accelerated degradation. However, cells designed for high power capability can allow higher charge rates. Rates should be selected so that the battery temperature does not exceed 50°C during fast charge. The battery is charged at the fast-charge rate until the battery reaches a voltage regulation limit (typical of 4.2 V/cell, but 4.1 V for coke-based anode Li-Ion battery). The charger starts to regulate the battery voltage and enters CV phase while the charge current exponentially drops to a defined termination level. However, the output voltage regulation accuracy is critical to maximizing battery capacity and improving its service life. Less battery voltage regulation accuracy means to undercharge the battery, which results in a large decrease in battery capacity. The battery loses about eight percent capacity if it is undercharged by one percent voltage. On the other hand, less battery voltage regulation accuracy also means the battery is overcharged, which reduces the battery service life-cycle. To safely charge the Li-Ion battery, it only allows initiating to charge the battery when the battery temperature is between 0°C to 45°C. Charging the battery at lower temperatures promotes formation of metallic Lithium, which increases the battery impedance and causes cell degradation.

On the other hand, charging the battery at higher temperatures causes accelerated degradation because of promoting Li-electrolyte reaction. This presents a market need for more accurate, efficient and safe battery charge for portable devices.

II. Low Cost Standalone Linear Battery Charger

Many IC manufacturers are responding to the market need for more accurate and safer battery charge by developing low-cost linear battery chargers for low-power portable equipment. Fig. 2 shows a low cost standalone linear battery charger circuit that uses few external components. The charger simply drops the adapter's DC voltage down to the battery voltage. The power dissipation across the pass element equals adapter voltage minus the battery voltage times the charge current, which is given by Equation (1).

$$P_{Loss} = (V_{IN} - V_{BAT}) \bullet I_{CHG} \quad (1)$$

If a 5-V adapter is used to charge a 1200-mAh or 2200-mAh single cell Li-Ion battery, Fig. 3 shows its power dissipation with 0.7 C rate fast-charge current. It has maximum power dissipation of 1.68 W and 3.0 W when the battery transitions from pre-charge to fast-charge phase, respectively. Power dissipation at 3.0 W results in 141°C temperature rise for a 3 mm × 3 mm QFN package with 47°C/W thermal impedance. This definitely exceeds maximum 125°C silicon junction operating temperature at 25°C ambient temperature.

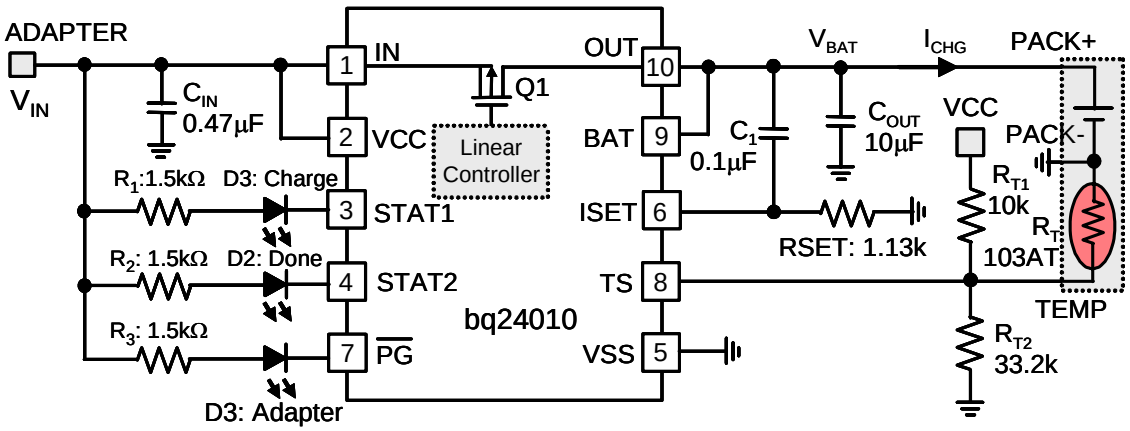

Fig. 2. Low cost standalone linear battery charger diagram.

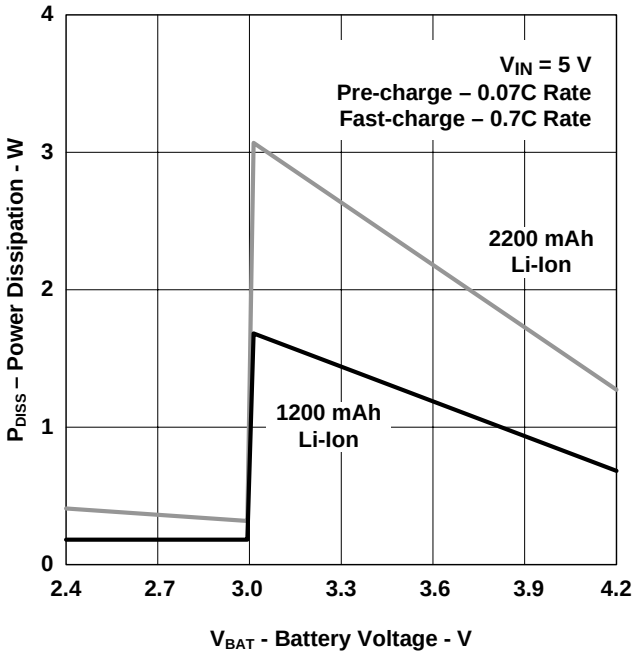

Fig. 3. Power dissipation for linear battery charger.

The tolerance on the fast- charge current regulation and the AC adapter voltage is also very important in a linear charger. If the regulation tolerance is loose, the pass transistor and package will need to be oversized, adding to size and cost. The fundamental issue for the linear charger is its high power dissipation.

A trade-off must be made between the charge current, size, cost and thermal requirements of the charging system. Therefore, the linear charger is usually suitable for the low capacity (less than 1300 mAh) Li-Ion battery applications because of their superior size, cost considerations and thermal issue. How to solve the thermal issue for high capacity battery packs or high input-to-output voltage difference applications? The answer is the high-efficiency synchronous switching battery charger.

III. High Efficiency MHz Synchronous Switching Battery Charger with Integrated Power MOSFETs

Synchronous switching mode charging solutions are generally used in the applications that have high input-to-output voltage difference or for high capacity battery packs. For a 2200 mAh Li-Ion battery pack, it is extremely difficult to use a linear charger to charge a single cell battery from a car adapter (12 V) at a fast charge rate of 0.5 C to 1 C. A linear charger with thermal regulation could be used, but the charge cycle time at the reduced charge rate will be extremely long.

Fig. 4 shows a standalone high efficiency synchronous switching buck battery charger with charge current up to 2 A for portable devices such as DVD players and smart phones.

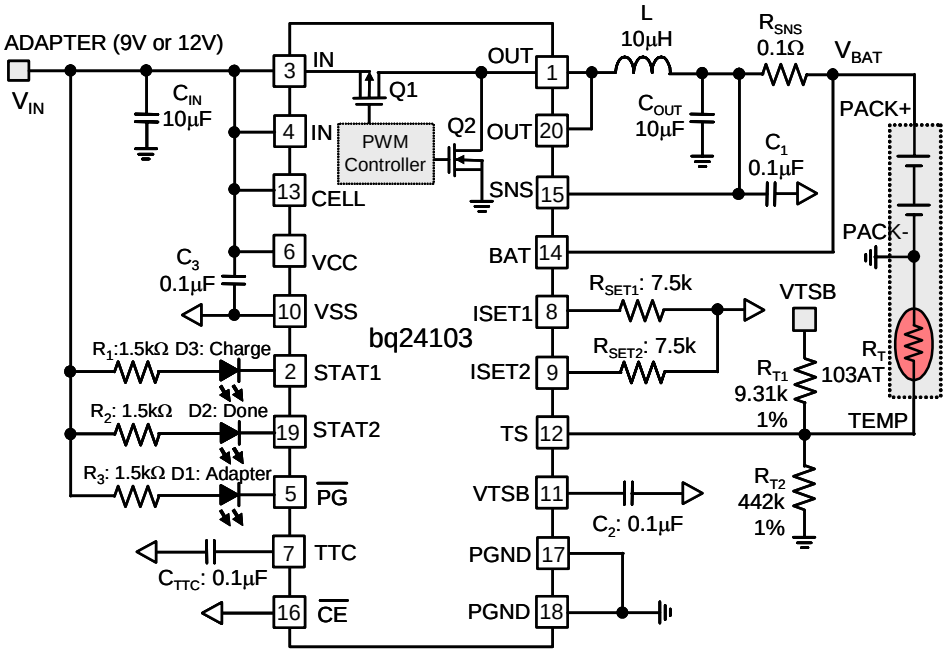

Fig. 4. 1.1-MHz standalone synchronous switching battery charger.

The battery charger uses a 1.1-MHz switching frequency voltage mode control architecture with internal Type III loop compensator to minimize the external components. To further minimize the battery charger size, it has integrated two power MOSFETs into the PWM controller in a small 4.5 mm × 3.5 mm package. The power MOSFETs Q1 and Q2 are complementarily turned on and off with optimized dead time to optimize the efficiency at high switching frequency. Q1 is used as P-channel MOSFET to eliminate an external boost strap capacitor and a diode when used for high side N-MOSFET gate driver and it is also easy to achieve 100 % duty cycle when the input voltage is very close to the battery voltage by completely turning on Q1. The turn-on and turn-off time are controlled to regulate the battery charge current (CC phase) or battery voltage (CV phase) depending on the feedback control loops. The charger has highly integrated functions to safely and healthily charge the Li-Ion battery. It is able to program the pre-charge current, fast charge current, charge voltage, charge timer, battery temperature monitoring, automatic recharging, short circuit and over temperature protection.

IV. CIRCUIT DESIGN

The circuit parameters are designed for the following specifications in the following design example.

- Adapter DC voltage: 12 V
- Two-cell Li-Ion battery pack: 4.2 V/cell, 1900 mAh/Cell
- Pre-charge current: $I_{PRE\text{-}CHG}$=133 mA
- Fast charge current: I_{CHG}=1.33 A
- Charge time limit: t_{CHG} = 5-hour
- Temperature range for initiating charge: T= 0°C-45°C

Since the size of the battery charger is very critical for portable devices, the output inductor is required to be as small as possible. For a given inductor ripple current, the required inductance is given by Equation (2).

$$L = \frac{(V_{IN} - V_{BAT})V_{BAT}}{V_{IN}\,\Delta I_L} \bullet \frac{1}{f_s} \qquad (2)$$

where

- f_s is the switching frequency
- ΔI_L is the inductor ripple current

Substituting V_{IN}=12 V, V_{BAT}=6.0 V (3.0 V/ cell), $\Delta I_{rRIPPLE,L}$=30 % I_{CHG}, I_{CHG}=1.33 A and f_S=1.1 MHz into the above equation yields L=7.5 μH. Selecting a 10-μH shielded inductor. Note that the shielded inductor has better capability to restrain the magnetic flux within the inductor and minimize the radiated electromagnetic interference (EMI). It is shown that the required inductance is inversely proportional to the switching frequency. The inductance can be 10 times smaller and it has a smaller size at 1 MHz than at 100 kHz. On the other hand, the higher the switching frequency, the higher the switching loss across Q1 and Q2 and the higher the core loss in the inductor as well. A detailed power loss analysis is discussed in the next section. After selecting the inductance and given the switching frequency, the inductor ripple current is give by Equation (3).

$$\Delta I_L = \frac{(V_{IN} - V_{BAT})V_{BAT}}{V_{IN}\,L} \bullet \frac{1}{f_s} \qquad (3)$$

Selecting inductor current rating is also critical for achieving desired efficiency. The peak inductor current I_{Peak} is calculated by Equation (4).

$$I_{Peak} = I_{CHG} + \frac{(V_{IN} - V_{BAT})V_{BAT}}{2\,V_{IN}\,L} \bullet \frac{1}{f_s} \qquad (4)$$

$$= 1.48A$$

The inductor has maximum ripple current when the battery voltage is half of the input voltage. Therefore, the inductor saturation current rating should be always higher than the maximum peak inductor current at all operating conditions.

To reduce the number of external components, it is the common practice to use internal loop compensation. The resonant frequency of the output inductor and capacitor should be around 16 kHz in order to achieve the optimum loop stability. Therefore, the output capacitance is calculated from Equation (5).

$$C = \frac{1}{(2 \bullet \pi \bullet f_o)^2 L} = 12\mu F \qquad (5)$$

Select 10μF/25V X5R or X7R ceramic capacitor. It is important to select a small ESR ceramic output capacitor with good temperature characteristics such as the X7R or X5R ceramic capacitor. The ripple current flowing into the battery is given by

$$I_{ripple,BAT} = \frac{ESR}{ESR + R_{SNS} + R_{BAT}} \Delta I_{ripple,L} \quad (6)$$

where

- ESR is the equivalent series resistance of the output capacitor
- R_{SNS} is the current-sensing resistor
- R_{BAT} is the battery internal impedance including the $R_{DS(on)}$ of the protection MOSFETs in the battery pack

The smaller the ESR of the output capacitor, the smaller the ripple current going to the battery. The ripple current to the battery should be designed less than one-tenth of the inductor ripple current and a 10 μF/10 mΩ ESR ceramic capacitor is usually enough to meet this requirement.

A. Select the Current Sensing Resistor R_{SNS}

Choose R_{SNS} based on the regulation threshold V_{IREG} across the sensing resistor. Let V_{IREG}=133 mV for achieving standard sensing resistor value. Solve for R_{SNS}.

$$R_{SNS} = \frac{V_{IREG}}{I_{CHG}} = \frac{133mV}{1.33A} = 0.1\Omega \quad (7)$$

The power dissipation across the sensing resistor is $I_{CHG}^2 \bullet R_{SNS} = 0.18W$. Select 1206 size rated at 0.5 W.

Select fast charge current set resistor R_{SET1}.

R_{SET1} is used to set the fast charge current, R_{SET1} is given by Equation (8).

$$R_{SET1} = \frac{1000}{V_{IREG}} = \frac{1000}{133mV} = 7.5k\Omega \quad (8)$$

Select pre-charge current set resistor R_{SET2}.

R_{SET2} is used to set the pre-charge current and is determined by Equation (9).

$$R_{SET2} = \frac{100}{R_{SNS} I_{PRE-CHG}} = \frac{100}{13.3mV} = 7.5k\Omega \quad (9)$$

Select the maximum charge time set capacitor C_{TTC}.

The charge timer detects the *bad* battery pack if the battery has not been fully-charged when the charge timer is expired. C_{TTC} is used to program the charge timer and it provides 2.6minute per nF.

$$C_{TTC} = \frac{t_{CHG}}{K_{TTC}} = \frac{5 \bullet 60}{2.6} = 115nF \quad (10)$$

Choose a 0.1 μF ceramic capacitor.

Select minimum and maximum battery charge temperature set resistors R_{T1} and R_{T2}

R_{T1} and R_{T2} are used to program the battery charge temperature range between 0^0 C and 45^0 C for initiating the battery charger. For a commonly used 103AT-2 thermistor in the battery pack, $R_T(0°C)=R_{TL}$=27.28 kΩ, $R_T(45°C)=R_{TH}$=4.911 kΩ, the R_{T1} and R_{T2} are determined by Equation (11).

$$R_{T1} = \frac{1.546 R_{TL} \bullet R_{TH}}{R_{TL} - R_{TH}} \qquad R_{T2} = \frac{4.289 R_{TL} \bullet R_{TH}}{R_{TL} - 5.289 R_{TH}} \quad (11)$$

Substituting R_{TL} and R_{TH} into the above equations yields R_{T1}=9.31 kΩ and R_{T2}=442 kΩ.

V. POWER LOSS ANALYSIS

Power loss is critical for highly integrated power MOSFETs since the power MOSFETs dissipate much more power than any other devices. It is not only an issue of efficiency, but also of thermal management and reliability. Having an idea of the losses in each component helps the system designer to layout the PCB properly and correctly, i.e. selecting PCBs with the right copper thickness and number of layers, determining the size of the circuit, determining the placement of the components as well.

Power dissipation in the MOSFETs is highly dependent on their on-resistances, gate charge factors and current and voltage rise and fall times, as well as the switching frequency and operating temperature. Losses in the MOSFETs consist of conduction loss, switching loss, body diode conduction loss and gate drive loss. The waveforms associated with the MOSFETs are shown in Fig. 5.

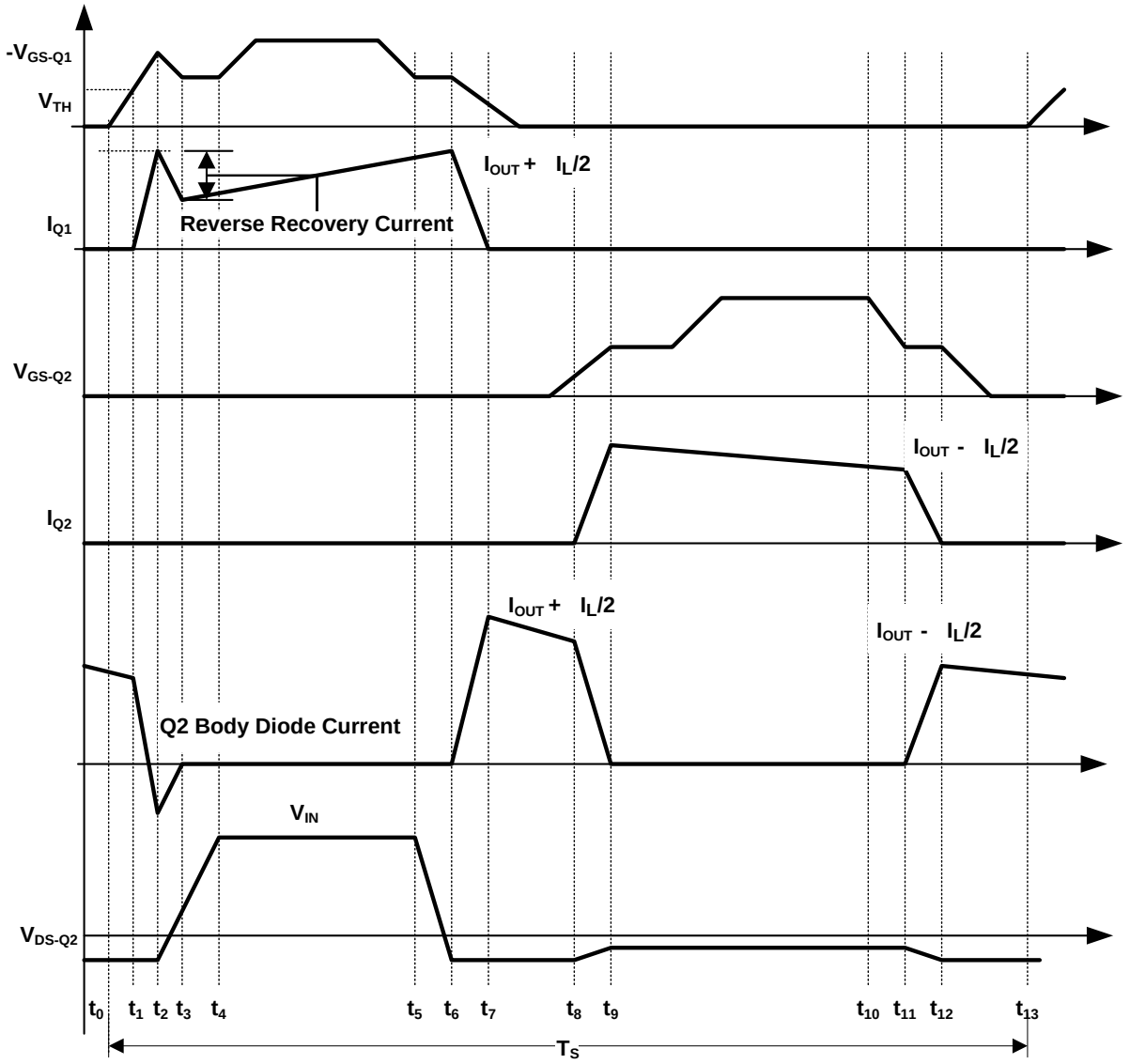

Fig. 5. Switching waveforms of a synchronous buck converter.

A. *Conduction Loss*

Based on the switching waveform in Fig. 5, to simplify the conduction loss calculation, assume that the switching time is negligible compared with the switching period. The current through Q1 and Q2 is trapezoidal. The RMS current of the upper switch Q1 can be estimated by

$$I_{RMS\_Q1} = \sqrt{\frac{1}{T_S}\int_0^{D\cdot T_S}\left[(I_{OUT} - \frac{\Delta I_L}{2}) + \frac{\Delta I_L}{D \bullet T_S} \bullet t\right]^2 dt} = \sqrt{D\left(I_{OUT}^2 + \frac{1}{12}\Delta I_L^2\right)} \quad (12)$$

where

- ΔI_L is the inductor ripple current
- T_S is the switching period

The conduction loss of the upper MOSFET Q_1 is given by Equation (13).

$$P_{COND\_Q1} = I_{RMS\_Q1}^2 \bullet R_{DS(on)\_Q1} \quad (13)$$

The RMS current of the lower MOSFET Q2 can be estimated by Equation (14).

$$I_{RMS\_Q2} = \sqrt{\frac{1}{T_S}\int_0^{(1-D)\cdot T_S}\left[(I_{OUT} + \frac{\Delta I_L}{2}) - \frac{\Delta I_L}{D \cdot T_S} \bullet t\right]^2 dt} = \sqrt{(1-D)\left(I_{OUT}^2 + \frac{1}{12}\Delta I_L^2\right)} \quad (14)$$

Conduction loss of the lower switch Q2 is:

$$P_{COND\_Q2} = \left(I_{RMS\_Q2}\right)^2 \bullet R_{DS(on)\_Q2} \quad (15)$$

The on-resistance of a MOSFET is temperature-dependent. The higher the temperature, the higher the on-resistance. It normally can be estimated as:

$$R_{DS(on)}(T) = R_{DS(on)\_25C} \bullet (1 + K \bullet \Delta T) \quad (16)$$

where

- K is the temperature coefficient ($K \approx 0.0039/°C$)
- $R_{DS(on)\_25C}$ the on-resistance under ambient temperature of 25°C.

In order to reduce the conduction loss, on-resistance of both MOSFETs Q1 and Q2 must be minimized, which requires more silicon resulting in cost increase. So, there is a trade-off between the conduction loss and silicon cost.

Switching Loss

Switching Loss - Upper Switch Q1

Fig. 5 shows in detail the switching waveforms of a synchronous buck converter. There is a voltage and current overlap across the upper switch Q1. This causes the switching loss from the time intervals from t1 to t4 and from t5 to t7. During turn-on period from t1 to t4, Q1 conducts a high peak current associated with the reverse recovery of the body diode of Q2 while its drain voltage starts to rise. The switching loss occurs when the switch is turned on and off. From Fig. 5, the turn-on loss of Q1 during t_1 through t_4:

$$P_{swon\_Q1} = 0.5 \bullet V_{IN} \cdot (I_{OUT} - \frac{\Delta I_L}{2}) \bullet t_{ON} \bullet f_S \quad (17)$$

where

- $t_{ON} = t_4 - t_1$

The turn-off loss of Q_1 during t_5~t_7: is described in Equation (18).

$$P_{swoff\_Q1} = 0.5 \bullet V_{IN} \bullet (I_{OUT} + \frac{\Delta I_L}{2}) \bullet t_{OFF} \bullet f_S \quad (18)$$

where

- $t_{OFF} = t_7 - t_5$

The total switching loss across Q1 is given by Equation (19).

$$P_{sw\_Q1} = P_{swon\_Q1} + P_{swoff\_Q1} \quad (19)$$

From the above switching loss calculation, it is shown that the switching loss is proportional to the switching frequency, turn-on and off switching times. To minimize the switching loss, we have to reduce the switching frequency resulting in increasing the inductance and size for a given inductor ripple current as discussed in last section. Besides turning on and off the MOSFETs fast is another way to minimize the switching loss.

Too fast switching may generate high electromagnetic interference (EMI), especially radiated EMI and the system may not pass the EMI regulation. In EMI sensitive applications, it may be necessary to slow down the switching speed by increasing the gate resistance to meet the EMI specifications. Therefore, there is a compromise between the switching speed and EMI compliance.

Switching Loss - Lower Switch Q2

From Fig 5, the body diode of Q2 is conducting just before MOSFET Q2 is turned on or off. Therefore, the voltage drop across Q2 during switching period is only the forward conduction voltage of the body diode. This is the so-called zero-voltage switching (ZVS), thus the switching losses can be neglected.

Lower MOSFET Body Diode Reverse Recovery Loss

As the lower MOSFET Q2 turns off, conduction of output current takes place through the body diode. To turn off the diode, a reverse bias voltage is applied across it. The charge stored in the body diode has to be evacuated from the junction. This adds to the switching loss of Q_1. The loss can be estimated as:

$$P_{QRR} = Q_{RR} \bullet V_{IN} \bullet f_S \quad (20)$$

where

- Q_{RR} is the reverse recovery charge of the lower MOSFET body diode

To eliminate the body diode reverse recovery loss, the best way is to avoid body diode conduction by turning on the lower MOSFET immediately when the higher MOSFET turns off. This requires adaptive control and it is very difficult to achieve since even a very small simultaneous conduction of Q1 and Q2 results in shoot-through current and increase the loss.

Body Diode Conduction Loss

To avoid shoot through between upper and lower MOSFETs, a dead time is required to prevent from simultaneous conduction. From Fig. 5, before Q_2 turns on and after Q_2 turns off, the body diode of Q_2 conducts for a period of a dead-time t_{DT}. This leads to body diode conduction loss shown in Equation (21).

$$P_{BD\_Q2} = 2 \bullet V_{BD} \bullet I_{OUT} \bullet t_{DT} \bullet f_S \quad (21)$$

where

- V_{BD} is the body diode forward voltage drop
- t_{DT} is dead time

Gate Drive Loss

The gate capacitor of Q_1 is charged every cycle to an energy level of $\frac{1}{2} C_{gs} \bullet V_{DRV\_Q1}^2$. The same amount of energy is dissipated internally in the MOSFET gate resistance to provide this charge. The same energy must be discharged once during each cycle.

The gate drive power dissipated by Q1 can therefore be given by Equation (22).

$$P_{DRV\_Q1} = Q_{g\_Q1} \bullet V_{DRV} \bullet f_S \quad (22)$$

where

- $Q_{g\_Q1} = Q_{gs\_Q1} + Q_{gd\_Q1}$
- V_{DRV} is the gate drive power supply voltage

The gate drive power dissipated by Q_2 can therefore be given by

$$P_{DRV\_Q2} = Q_{g\_Q2} \bullet V_{DRV} \bullet f_S \quad (23)$$

where

- $Q_{g\_Q2} = Q_{gs\_Q2}$ ($Q_{gd\_Q2} = 0$ since Q_2 operates in zero-voltage switching and Q_{gd_Q2} is recovered)

The gate drive power supply voltage is clamped to 6 V generated by a LDO when the input voltage is higher than 7 V. If the input voltage is below 7 V, then the gate drive voltage is 1-V below the input voltage. There is another power loss associated with the LDO generating a gate supply voltage, which is given by Equation (24).

$$P_{LDO} = \left(Q_{g\_Q1} + Q_{g2\_Q2}\right) \bullet f_S \bullet \left(V_{in} - V_{DRV}\right) \qquad (24)$$

Thermal Calculation

The junction temperature is crucial for IC with integrated power MOSFETs. During normal battery charge operation, the integrated MOSFETs dissipate a certain amount of power and generate the heat. This increases the die temperature resulting in on-resistance increase of the MOSFETs. The increase on-resistance in turn increases the conduction loss again. Therefore, it should have a thermal balance point ultimately. The junction temperature rise is equal to the total power dissipation across the IC times thermal impedance from the junction to the ambient, which is given by Equation (25).

where

- $P_{MOS\_fixed} = P_{sw\_Q1} + P_{QRR} + P_{BD\_Q2} + P_{DRV\_Q1} + P_{DRV\_Q2} + P_{LDO}$
- θ_{jA} is the thermal impedance

Solving the above equation yields Equation (26).

Inductor Loss

The inductor loss consists of winding loss and core loss. The total winding loss is a function of frequency and temperature. The core loss depends upon the core material and is function of switching frequency, maximum flux density as well as the volume.

For a synchronous buck converter topology, the inductor ripple current is relatively small compared with its DC current. The core loss due to core flux change $\Delta\varnothing$ is negligible. The calculation based on DC resistance (DCR) is fairly good for general purpose estimation.

$$I_{RMS\_L} == \sqrt{I_{OUT}^2 + \frac{1}{12}\Delta I_L^2} \qquad (27)$$

The winding loss can be estimated as

$$P_{L\_winding} \approx I_{L\_RMS}^2 R_{L\_DCR} \qquad (28)$$

The DCR of an inductor is also temperature-dependent. It normally can be estimated as:

$$R_{L\_DCR}(T) = R_{L\_DCR25C} \bullet (1 + K \bullet \Delta T) \qquad (29)$$

where

- K is the temperature coefficient (K=0.0039/°C for copper)
- Loss Across the Sense Resistor

The power dissipation across the current sensing resistor is

$$P_{RSNS} = I_{OUT}^2 R_{SNS} \qquad (30)$$

- Capacitor ESR Loss

The input capacitor has an internal ESR and it dissipates power when a ripple current flows through the capacitor. The RMS current flowing through the input capacitor is given by Equation (31).

$$\Delta T = \left[I_{RMS\_Q1}^2 \bullet R_{DS(on)\_Q1\_25C} \bullet (1 + K \bullet \Delta T) + I_{RMS\_Q2}^2 \bullet R_{DSON\_Q2\_25C} \bullet (1 + K \bullet \Delta T) + P_{MOS\_fixed}\right] \bullet \theta_{jA} \qquad (25)$$

$$\Delta T = \frac{I_{RMS\_Q1}^2 \bullet R_{DSON\_Q1\_25} + I_{RMS\_Q2}^2 \bullet R_{DSON\_Q2\_25} + P_{MOS\_fixed}}{\frac{1}{\theta_{jA}} - K \bullet (I_{RMS\_Q1}^2 \cdot R_{DSON\_Q1\_am} + I_{RMS\_Q2}^2 \bullet R_{DSON\_Q2\_am})} \qquad (26)$$

$$I_{RMS\_CIN} = \sqrt{\frac{1}{T_S}\left\{\int_0^{D \cdot T_S} \left[I_{OUT}(1-D)\right]^2 dt + \int_0^{(1-D) \cdot T_S} \left[I_{OUT} \bullet D\right]^2 dt\right\}} = I_{OUT} \bullet \sqrt{D \bullet (1-D)} \qquad (31)$$

The current flowing through the output capacitor can be approximated by the AC component of the inductor current. The RMS current of the output capacitor is given by Equation (32).

The loss of the input capacitor due to its ESR:

$$P_{CIN\_ESR} = I_{RMS\_CIN}^2 \, R_{ESR,CIN} \quad (33)$$

The loss of the output capacitor due to its ESR:

$$P_{COUT\_ESR} = I_{RMS\_COUT}^2 R_{ESR,COUT} \quad (34)$$

VI. Calculation Results

The circuit parameters for the bqSWITCHER™ (TPS24103) are:

For the primary switcher (Q1)

- $R_{DS(on)\_Q1}$ (5 V) =305 mΩ at 25°C
- $R_{DS(on)\_Q1}$ (12 V)=250 mΩ at 25°C
- $V_{DRV\_Q1}=V_{IN}$
- Qg_Q1=6.722 nC,
- Δt_{ISW_ON1} = 2.042 ns
- Δt_{VISW_ON1} = 7.49 ns
- $\Delta t_{ISW\_OFF1} = \Delta t_{ISW\_ON1}$
- $\Delta t_{VSW\_OFF1} = \Delta t_{VSW\_ON1}$

For the secondary switcher (Q2)

- $R_{DS(on)\_Q2}$ (5 V)=80 mΩ at 25°C
- $R_{DS(on)\_Q2}$ (12V)=69 mΩ at 25°C
- $V_{DRV\_Q1}=2 \cdot V_{IN}$
- $V_{DRV\_Q2}=V_{IN}$
- Qg_Q2=6.979 nC
- QRR=0.02 nC,
- VBD=0.7 V,
- t_{DT}=25 ns

For the inductor (L)

- R_{L_DCR}=49 mΩ

For the input capacitor (C_{IN})

- $R_{ESR,CIN}$=8 mΩ

For the output capacitor (C_{OUT}):

- $R_{ESR,COUT}$=8 mΩ.

Table 1 shows the calculated breakdown.

- The conduction loss is dominant over switching loss although it operates at 1.1 MHz.
- The lower the ambient temperature, the lower the conduction loss due to the on-resistance increase with the temperature rise.
- A lower input voltage normally leads to lower loss.
- The junction temperature for single cell applications is lower than that of two-cell applications. For a 55°C ambient temperature, the IC junction temperature could reach as high as 90°C for two Li-Ion cell applications.

$$I_{RMS\_COUT} = \sqrt{\frac{1}{T_S}\left\{\int_0^{D\cdot T_S}\left[-\frac{\Delta I_L}{2}+\frac{\Delta I_L}{D\bullet T_S}\bullet t\right]^2 dt + \int_0^{(1-D)\cdot T_S}\left[\frac{\Delta I_L}{2}-\frac{\Delta I_L}{(1-D)\cdot T_S}\bullet t\right]^2 dt\right\}} = \frac{\Delta I_L}{2\sqrt{3}} \quad (32)$$

TABLE 1:
CALCULATED LOSS BREAKDOWN UNDER DIFFERENT OPERATING CONDITIONS

V_{IN}=12 V, I_{CHG}=1.2 A		2S Li-Ion Battery V_{BAT}=8.4 V, V_{IN}=12 V		Single Cell Li-Ion V_{BAT}=4.2 V, V_{IN}=5 V	
Item	**Symbol (Unit)**	T_{AM}=25°C	T_{AM}=55°C	T_{AM}=25°C	T_{AM}=55°C
MOSFETs Q1 and Q2	P_{COND} (W)	0.315	0.353	0.430	0.484
	P_{sw_Q1} (W)	0.151	0.151	0.063	0.063
	P_{QRR} (mW)	0.264	0.264	0.11	0.11
	P_{BD_Q2} (W)	0.046	0.046	0.046	0.046
	P_{DRV} (W)	0.09	0.09	0.075	0.075
	P_{LDO} (W)	0.09	0.09		
	P_{FETs} (W)	0.692	0.730	0.614	0.668
Inductor	$P_{L\_winding}$ (W)	0.071	0.071	0.071	0.071
Sense Resistor	P_{RSNS} (mW	0.144	0.144	0.144	0.144
Capacitors	P_{C_ESR} (mW)	2.45	2.45	1.551	1.551
Total Losses	P_{TOTAL} (W)	0.90	0.948	0.829	0.883
Efficiency	η (%)	91.7	91.35	85.8	85.1
IC Temperature Rise	ΔT (°C)	32.7	34.5	28.7	31.2
IC Junction Temperature	T_J (°C)	57.7	89.5	53.7	86.2

The calculation results and the measurement results of the charger efficiency vs output current when V_{IN}=12 V are shown in Fig. 6 and Fig. 7, respectively. The calculation results correlate with the measurement results well.

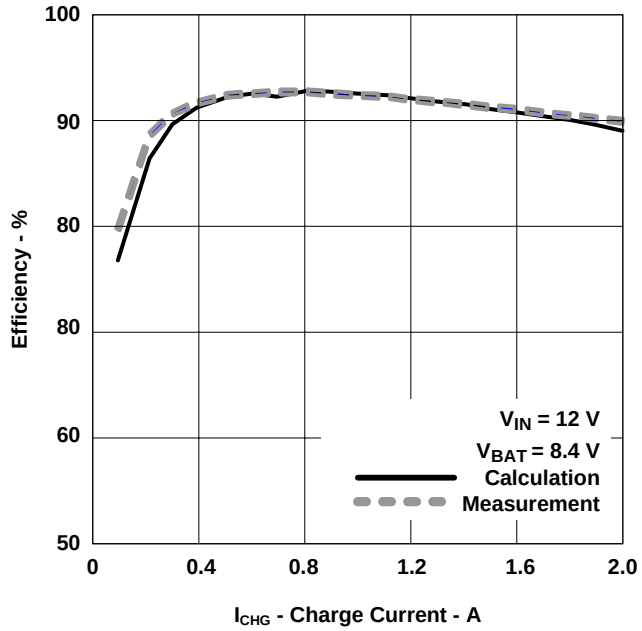

Fig. 6. Measured and calculated efficiency at different charge current.

Fig. 7 shows the efficiency curves with various input voltages. It has over 90 percent efficiency even at 16-V input voltage.

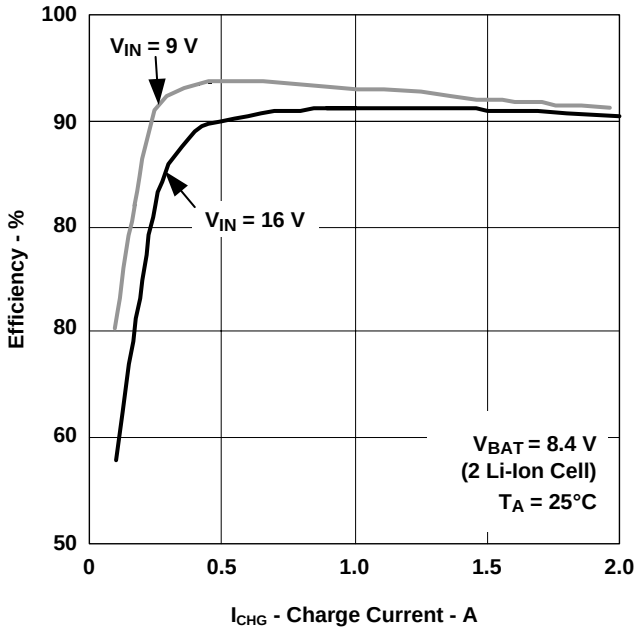

Fig. 7. 1.1MHz synchronous switching charger efficiency with different input voltages.

Compared with the linear charger, the power dissipation is much smaller and it is possible to design the synchronous-switching charger in the battery pack's side to minimize the use of mother board since the inductor size is small due to MHz frequency operation. One important thing to remember is that the battery's service life is strongly dependent on its temperature. Charging the Li-Ion battery with synchronous switching charger basically generates less heat. As a result, it has longer service cycle-life compared with the linear charger.

VII. CONCLUSION

The linear charger is suitable for the low-capacity battery charge applications with low cost and small size advantages. Continuing power demand increase from portable devices such as portable DVD players and smart phones makes the linear battery charger no longer efficiently adequate to charge the Li-Ion battery due to its inherent high power dissipation limitation. A high-efficiency synchronous switching battery charger with integrated MOSFETs provides an efficient charging solution for those advanced portable devices with less heat and longer battery service life.