Evaluation and Performance Optimization of Fully Integrated DC/DC Converters

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ABSTRACT

This topic explains the evaluation and optimization of a fully integrated DC/DC converter. The focus is given to the converter loop stability analysis and load transient response. Mainly due to space constraints in portable equipments the DC/DC converter is internally compensated. When the converter needs to be optimized for specific application conditions the inductor, output capacitor and the feedback divider are the only components that can be changed. This paper discusses how these components influence the performance of the converter. The paper also details converter evaluation and test to assure stable operation during its production and life time.

I. BASIC DC/DC ANALYSIS SIGNALS

Regardless of the converter topology (step down, boost, or buck-boost, etc.) the three basic waveforms that need to be measured are shown in Fig. 1. using a step down converter as the example.

Fig. 1 shows the basic topology of a step down converter with its most important waveforms. V_L is measured with the oscilloscope at the switch pin and should show a stable square wave signal. The inductor current is measured with a current probe. The best way to measure the inductor current is to use a small wire for the current probe in series to the inductor.

The wire does not change the circuit parameter since it adds only a small parasitic inductance in series to the normal inductor.

The output voltage is measured directly across the output capacitor of the device. To further minimize noise coupling into the probe, the ground clip must be removed and replaced with a short and direct ground connection across the output capacitor. Special probe connectors are usually the most convenient way to measure the output voltage ripple if they are populated on the PCB. The signals are measured using the TPS62044 a fully integrated 1.2-A step-down converter in a 3 mm×3 mm QFN package, optimized for portable applications, and shown in Fig. 2.

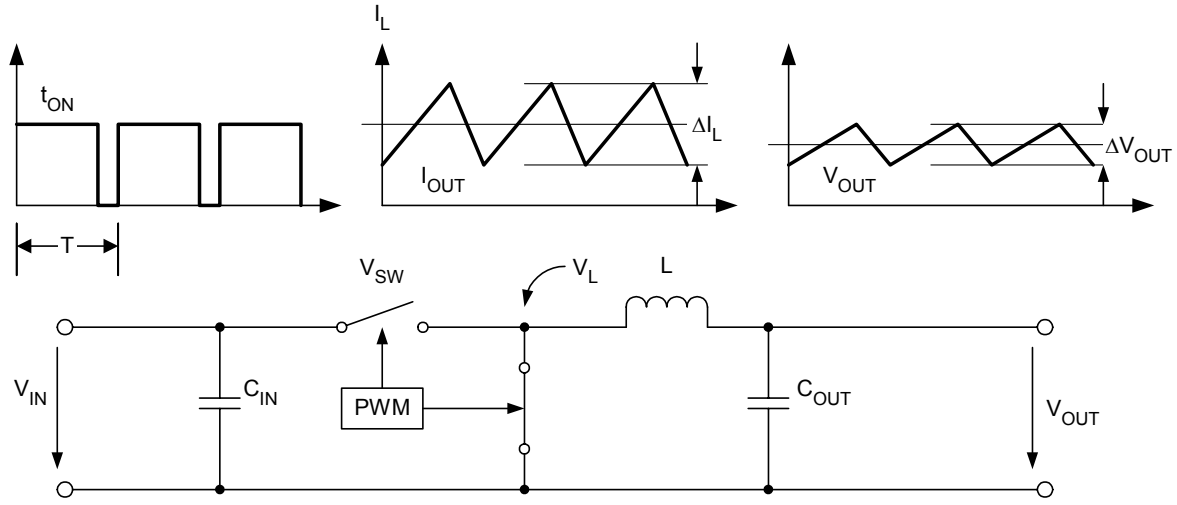

Fig 1. Basic signal waveforms.

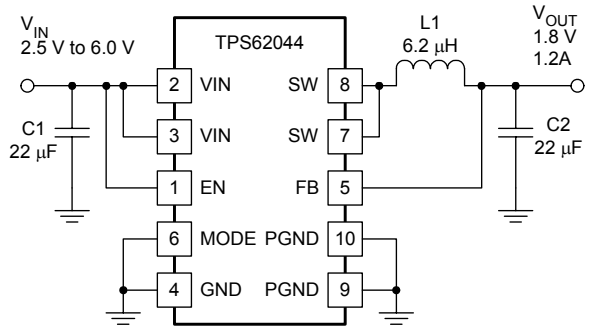

Fig 2. A fully integrated step-down converter.

Fig. 3 shows the square wave switching signal, output ripple voltage and inductor current.

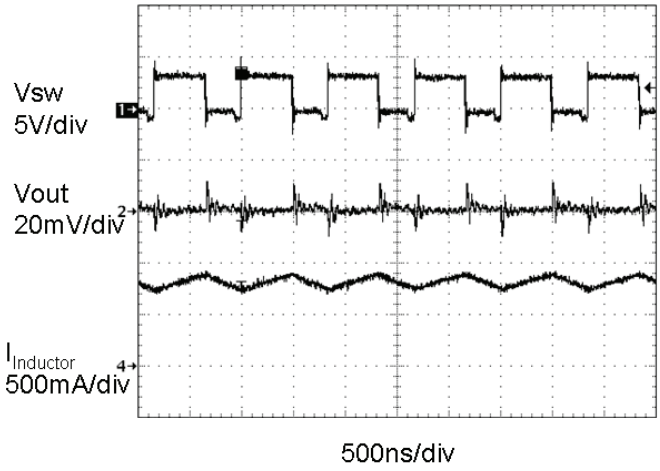

Fig 3. Basic oscilloscope signals used to evaluate a switching DC/DC converter.

When the switching waveform at the switch pin SW shows large duty cycle jitter or the output voltage or inductor current shows oscillations then the regulation loop is most likely unstable. In some cases the instability can also be related to layout problems and noise issues. When the converter shows a stable square wave signal on the switch pin and a stable inductor current over the entire input voltage range then the design is already fairly stable. As a next step it needs to be quantified "how stable" the converter is and if there are no other large signal circuit limitations caused by maximum switch current limitations, inductor saturation, etc. This is done with an evaluation like the one in Fig. 4, showing a load transient response from 150 mA to 1.15 A with only a 100-mV output voltage drop.

The best way to apply load transients to a DC/DC converter is to use a load resistor in series with a MOSFET switch. The MOSFET can be controlled directly from a square waveform generator or a MOSFET driver circuit. It is important to achieve fast MOSFET turn-on and turn-off time so as to excite the circuit with the entire frequency range that could possibly cause circuit oscillation. During the load transient the output voltage overshoot and undershoot needs to be observed. Based on the amount of overshoot and undershoot occurring during the load transient, the converter loop phase margin and crossover frequency can be determined.

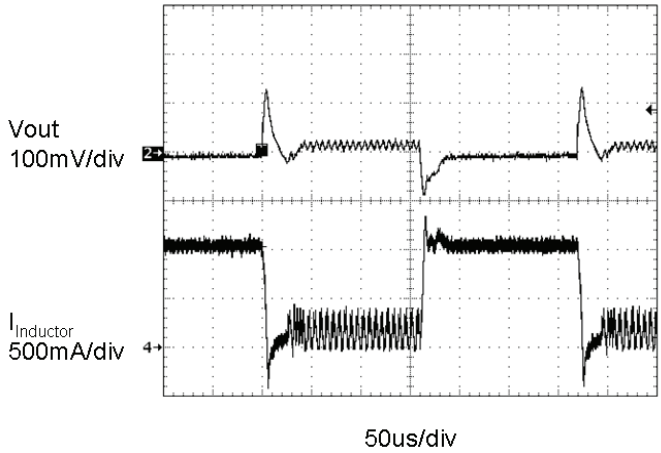

Fig 4. Load transient response.

To determine these parameters, the converter step response is plotted in Fig. 5 for different converter loop phase margins.

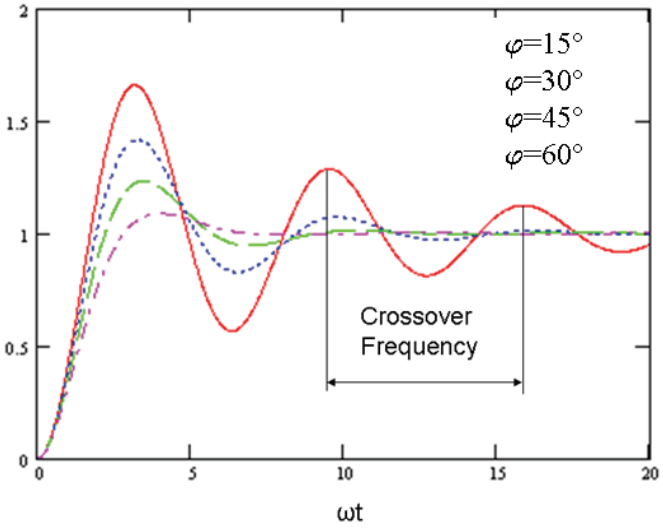

Fig. 5. Step response vs loop phase margin

The theoretical results shown in Fig. 5 can be compared with the step response measurement in the actual application to determine the phase margin and crossover frequency of the converter loop. Usually a phase margin of φ=45° is sufficient. It is important to perform the load transient test over the entire input voltage range to make sure the converter operates in its stable region over the entire operation range. If external filter component values with a parameter variation up to ±20% are used, the test has to be performed with component values at least half the specified nominal values. The converter step response gives fairly exact information about the converter loop, but only in the vicinity of the crossover frequency. To get an exact picture of the entire converter loop, the loop gain has to be measured.

II. Loop Gain Measurements Analyze The Entire Regulation System

The loop gain measurement can be done with a network analyzer or a specific loop gain measurement instrument as available from Venable or AP.

The frequency of the injected AC signal (distortion signal) is swept and the magnitude and phase of the injected and returned signals are measured. Then the gain and phase between the two signals is then plotted against the frequency. For the DC/DC converter shown in Fig. 2 the loop gain is measured and plotted in Fig. 7.

The bottom trace shows the loop gain and the top curve shows the phase. The phase margin is measured at the point where the gain is 0dB (i.e. unity). The response plotted in Fig. 7. is unconditionally stable and has sufficient "design-margin" to cover all practical parameter and component variations. With the successful completion of the AC analysis by measuring the loop gain the circuit evaluation is completed and a robust design in terms of converter stability has been achieved.

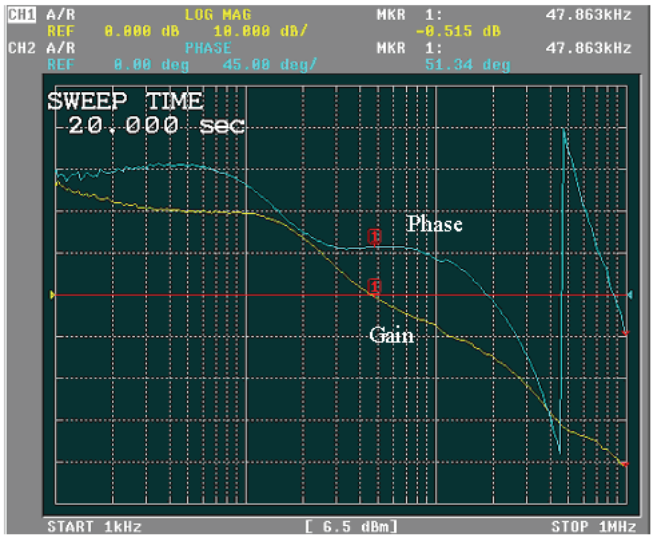

Fig 7. DC/DC converter closed loop gain plot.

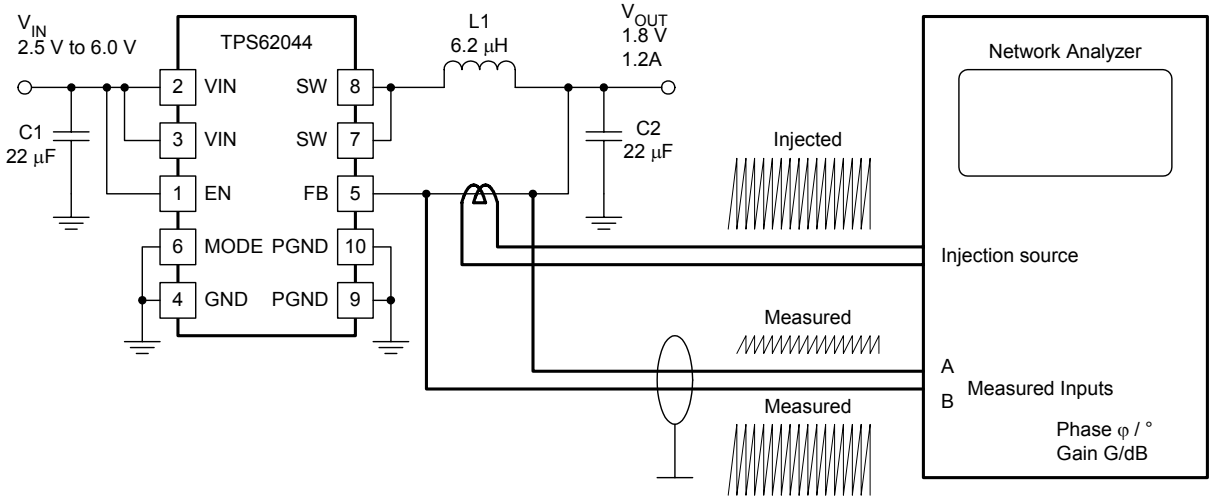

Fig. 6. Close loop gain measurement set up for a DC/DC converter.

III. Application Example - Boost Converter Compensation

This section demonstrates how to improve the phase margin of the boost converter by adding a feedforward capacitor across the feedback divider. The measurements were obtained, using the TPS65160, an LCD bias power management device for large size TV panels.

For simplicity the circuit of Fig. 8 shows only the boost converter section of the TPS65160. As a common practice the TPS65160 uses a feedforward capacitor (C4) across the top feedback resistor (R1) to insert a zero in the control loop. A mathematical explanation is included at the end of the paper. To verify the stability of the boost converter, the load transient test is done as shown in Fig. 9, with a load current step from 100 mA to 1.3 A.

The top trace shows the output voltage and the bottom trace the load current applied to the output. From these waveforms the crossover-frequency can be determined to be around 20 kHz. The phase margin is estimated to be greater than 30° which is slightly marginal.

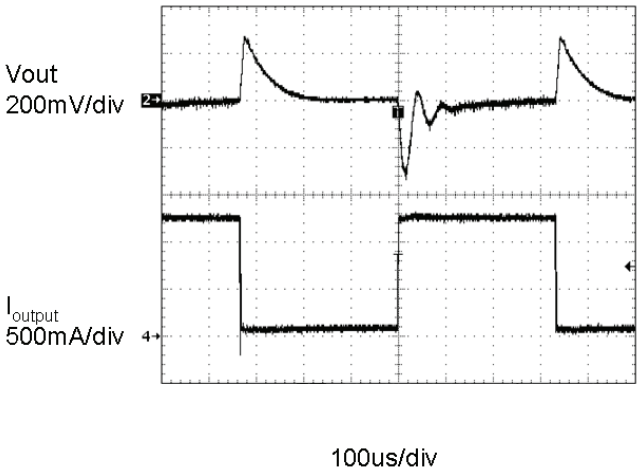

Fig 9. Load transient step 100 mA to 1.3 A, C4=10 pF.

Unfortunately the load transient response does give not much insight regarding the root cause of the insufficient phase margin. With the limited information, available from the load transient response, only a very experienced designer would be able to solve the problem without spending a lot of time in the lab. A much better picture of the situation is given by the loop gain measurement of Fig 10, enabling the problem to be solved much faster.

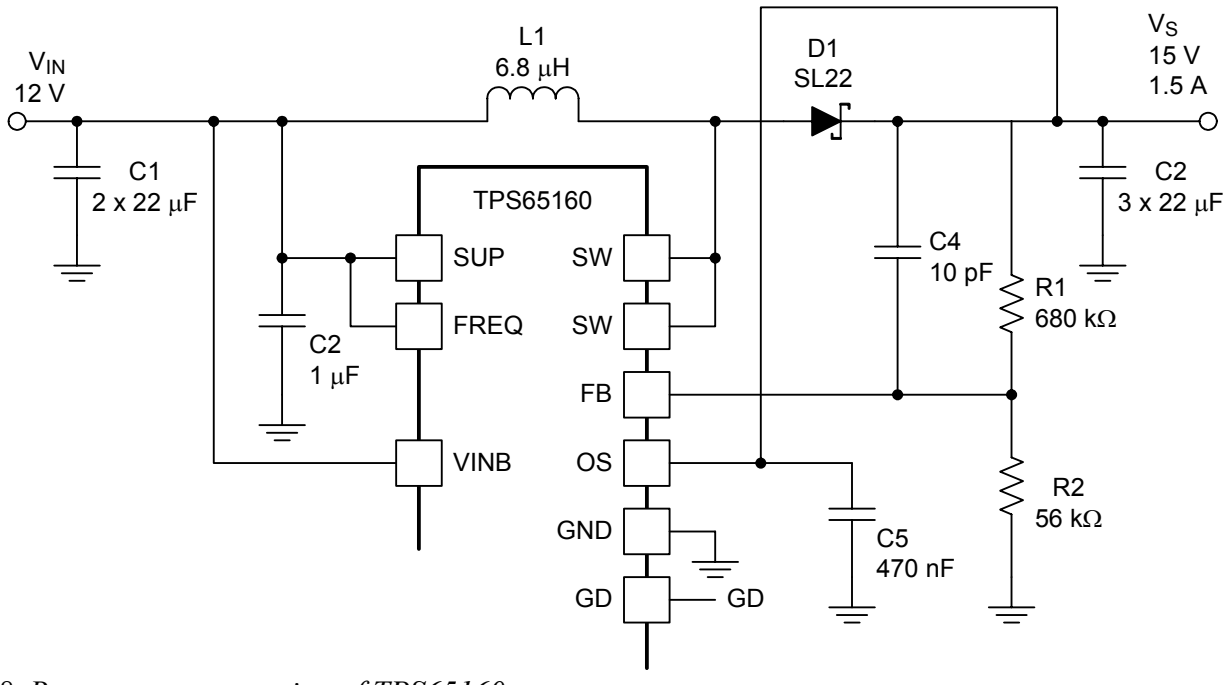

Fig 8. Boost converter section of TPS65160.

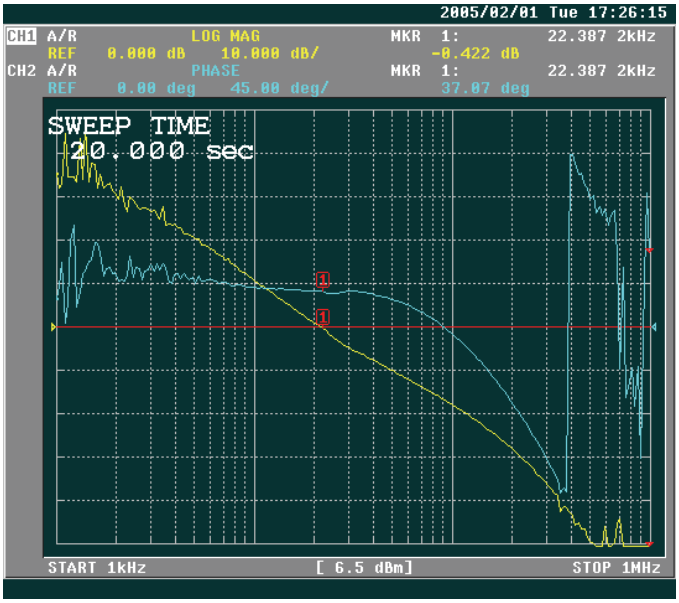

Fig 10. Boost converter loop gain.

Fig. 10 also shows an increasing phase beyond the crossover frequency (unity gain) but insufficient phase around the crossover frequency. In this case the zero introduced by the external feedforward capacitor (C4) partially prevents the phase from rolling off but only at higher frequencies. Moving the zero to a lower frequency should increase the phase margin at the unity gain and further raise the crossover frequency. Therefore the feedforward capacitor is increased from 10 pF to 22 pF. The new load transient response is shown in Fig. 11.

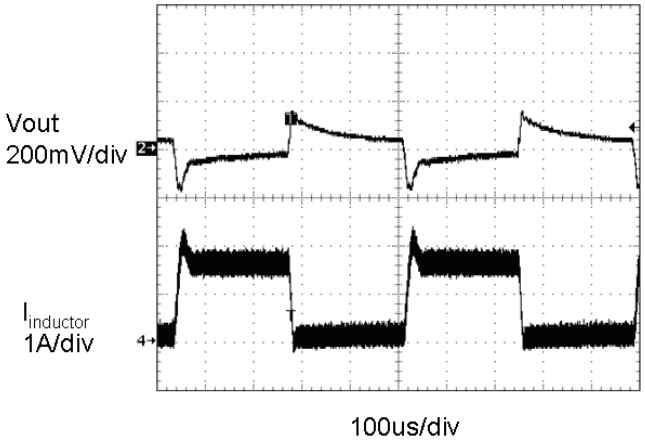

Fig 11. Load transient with increased feed-forward capacitor (C4 = 22 pF).

As a consequence of the higher crossover-frequency the overall load transient voltage drop is reduced from around 300 mV down to 180 mV. This change reduced the total output voltage drop to impressive 1.2% for the 15-V output. The load transient response shows minimum overshoot and based on the output voltage response the phase margin is estimated to be larger than 40º. To confirm this result the loop gain is measured and shown in Fig. 12.

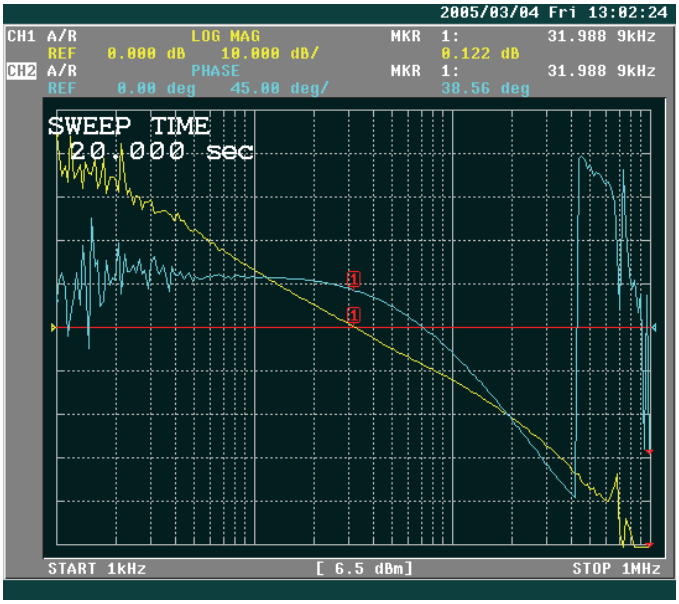

Fig 12. Loop gain with 22 pF feedforward capacitor.

The loop gain shows a crossover frequency of 31 kHz vs 22 kHz before. The phase margin is 39º. The converter loop is un-conditionally stable and has sufficient margin to cover temperature and process variations. If the phase margin needs to be further increased the next step would be to increase the output capacitor value. Increasing the feedforward capacitor value does not increase the phase margin any further.

IV. Transfer Function of Various Feedback Voltage Dividers

Since a fully integrated DC/DC converter has internal compensation the feedback divider can be used to optimize the design. This section describes different combinations and their effect on the converter's transfer loop. The feedback divider allows compensation and optimization of the regulation loop. Most of the DC/DC converters on the market have at least a feedforward capacitor across the upper feedback divider resistor. Different combinations of R-C networks around the feedback divider allow shaping the transfer loop of the feedback divider. The most common examples and their transfer functions are shown. The software tool Mathcad facilitates graphing of complex transfer functions.

A. Standard feedback divider with R1, R2.

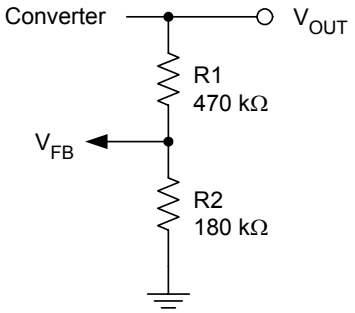

Fig 13. Standard Feedback Divider with R1, R2

The transfer function G(s) is defined as:

$$G(s) = \frac{Vo}{Vin} \tag{1}$$

For the standard feedback divider the transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{R2}{R1 + R2} \tag{2}$$

$$\begin{aligned} Gdc &= 20 \bullet \log\left(\frac{V_{FB}}{Vo}\right) \\ &= 20 \bullet \log\left(\frac{180k\Omega}{470k\Omega + 180k\Omega}\right) \\ &= -11dB \end{aligned} \tag{3}$$

The transfer function is plotted as:

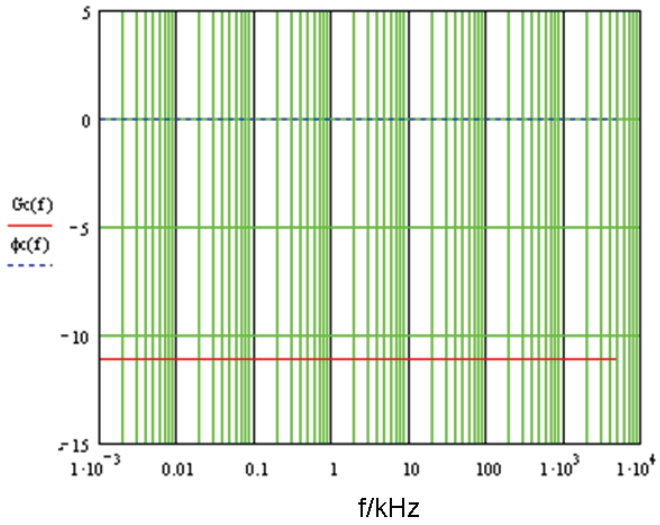

Fig. 14. Standard feedback divider transfer function.

B. Feedback Divider with Feedforward Capacitor

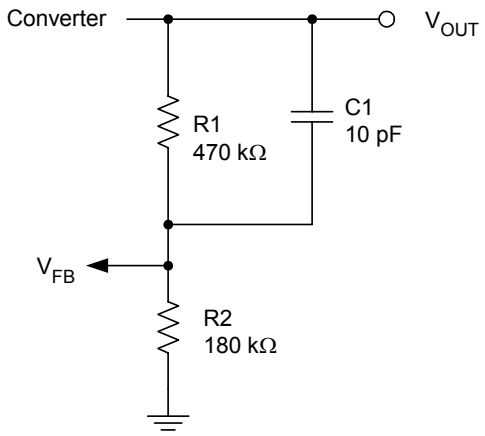

Fig. 15. Feedback divider with feedforward capacitor.

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \tag{4}$$

with

$$G(s) = \frac{1 + sC1R1}{1 + \frac{R1}{R2} + sC1R1} \tag{5}$$

This transfer functions has a zero and a high frequency pole. The configuration is used to increase the phase margin and crossover-frequency of the converter transfer function.

R1 and C1 place a zero in the transfer loop at:

$$fz = \frac{1}{2\pi \bullet R1 \cdot C1} = \frac{1}{2\pi \bullet 470k\Omega \bullet 10pF} = 33.86kHz \tag{6}$$

The high frequency pole is calculated:

$$fp = \frac{1}{2\pi \bullet R1 // R2 \bullet C1} = \frac{1}{2\pi \bullet C1 \bullet \frac{R1R2}{R1+R2}} = 122.28kHz \tag{7}$$

The transfer function is plotted as:

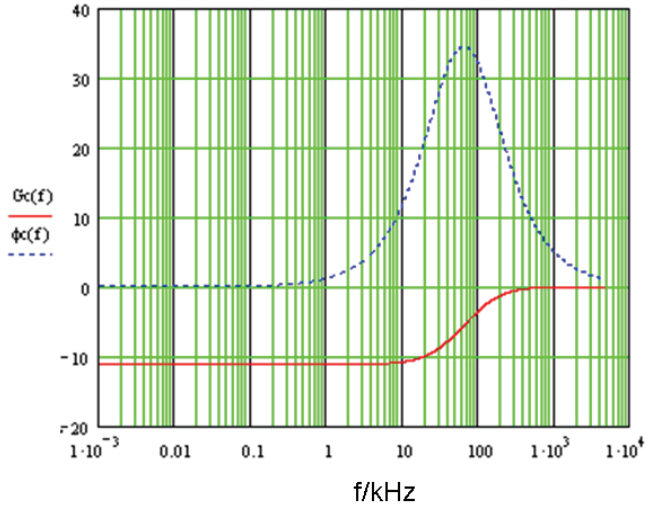

Fig 16. Feedback divider with feedforward capacitor transfer function.

C. *Feedback Divider with Feedforward Capacitor and Resistor*

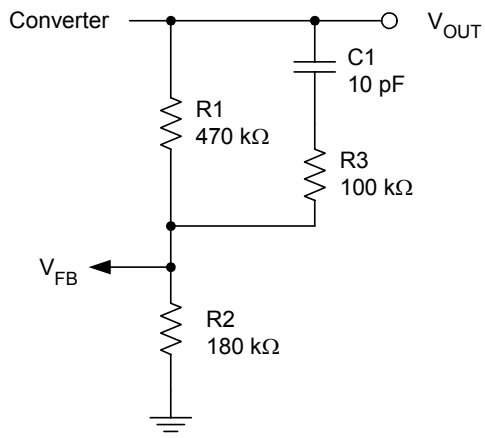

Fig 17. Feedback divider with feedforward capacitor and restistor.

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \tag{8}$$

with

$$G(s) = \frac{1 + sC1(R1 + R3)}{1 + \frac{R1}{R2} + sC1\left(R1 + R3 + \frac{R1R3}{R2}\right)} \tag{9}$$

This transfer functions has a zero and a high frequency pole similar to the previous configuration but with reduced high frequency gain. The configuration is used to increase the phase margin of the converter transfer function. R1, R3 and C1 place a zero in the transfer loop at:

$$fz = \frac{1}{2\pi \bullet C1 \bullet (R1 + R3)} = 33.79kHz \tag{10}$$

Followed by the high frequency pole at:

$$fp = \frac{1}{2\pi \bullet C1 \bullet \frac{R1R2 + R3R2 + R1R3}{R1 + R2}} = 121.35kHz \tag{11}$$

At high frequencies R3 is in parallel to R1 increasing the high frequency gain. The high frequency gain is calculated:

$$Rtop = \frac{R1 \bullet R3}{R1 + R3} = \frac{470k\Omega \bullet 100k\Omega}{470k\Omega + 100k\Omega} = 82.4k\Omega \quad (12)$$

$$Gdc_{HF} = 20 \bullet \log\left(\frac{R2}{Rtop + R2}\right) = 20 \bullet \log\left(\frac{180k\Omega}{82.4k\Omega + 180k\Omega}\right) = -3.27dB \quad (13)$$

The transfer function is plotted as:

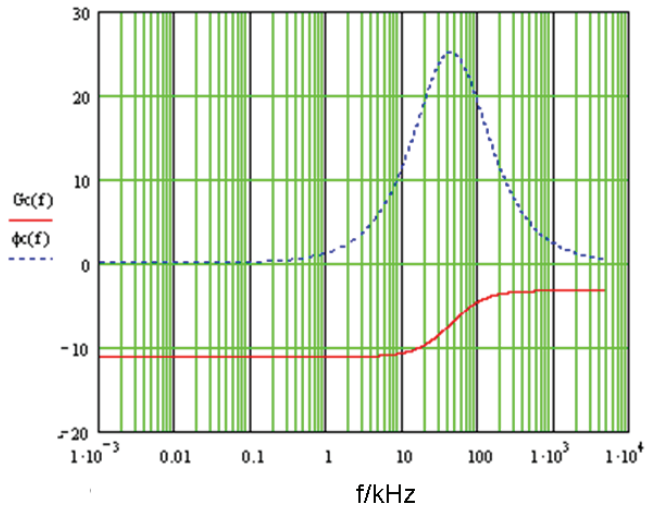

Fig 18. Feedback divider with feedforward capacitor and resistor.

D. Feedback Divider with Capacitor Across the Bottom Feedback Divider

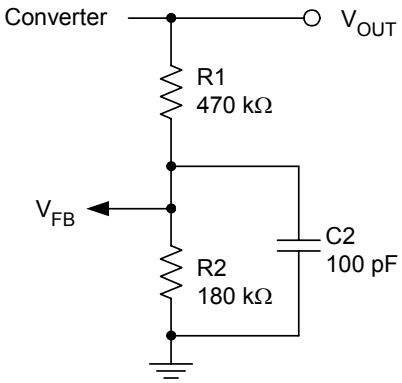

Fig 19. Feedback divider with capacitor across the bottom feedback divider.

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \quad (14)$$

with

$$G(s) = \frac{1}{1 + \frac{R1}{R2} + sC2R1} \quad (15)$$

The configuration is used to reduce the converter gain at higher frequencies improving phase margin and reducing noise at the feedback pin of the DC/DC converter.

The pole is placed in the transfer loop at:

$$fp = \frac{1}{2\pi \cdot C2 \cdot \frac{R1R2}{R1 + R2}} = 12.2kHz \quad (16)$$

The transfer function is plotted as:

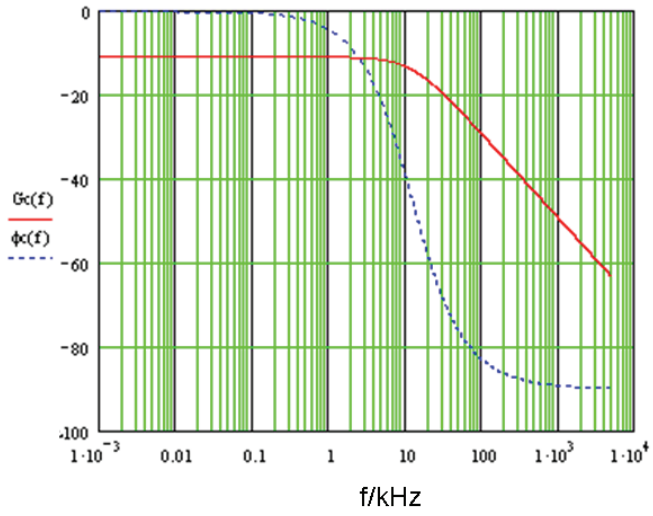

Fig. 20. Feedback divider with capacitor across the bottom feedback divider transfer function.

E. *Feedback Divider with Capacitor and Resistor Across The Bottom Feedback Divider*

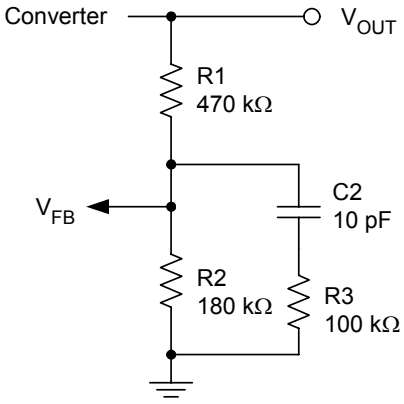

Fig. 21. Feedback divider with capacitor and resistor across the bottom feedback divider.

The configuration is used to reduce the overall converter gain with the additional zero. Placing the pole at lower frequencies gives a reduced overall converter gain without losing phase margin at the crossover frequency.

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \tag{17}$$

with

$$G(s) = \frac{1 + sC2 \bullet R3}{1 + \frac{R1}{R2} + sC2 \bullet \left(R1 + R3 + \frac{R1R3}{R2} \right)} \tag{18}$$

The transfer function has a pole at:

$$fp = \frac{1}{2\pi \bullet C2 \bullet \frac{R2R3 + R1R2 + R1R3}{R1 + R2}} \tag{19}$$

$$= 69.1 kHz$$

A high frequency zero after the pole at:

$$fz = \frac{1}{2\pi \bullet R3 \bullet C2} = \frac{1}{2\pi \bullet 100 k\Omega \bullet 10 pF} \tag{20}$$

$$= 159.15 kHz$$

At high frequencies R3 is in parallel to R2 and limiting the high frequency gain. The high frequency gain is calculated:

$$Rbottom = \frac{R2 \bullet R3}{R2 + R3} = \frac{180 k\Omega \bullet 100 k\Omega}{180 k\Omega + 100 k\Omega} \tag{21}$$

$$= 64.28 k\Omega$$

$$Gdc_{HF} = 20 \bullet \log\left(\frac{Rbottom}{Rbottom + R1} \right)$$

$$= 20 \bullet \log\left(\frac{64.28 k\Omega}{64.28 k\Omega + 470 k\Omega} \right) = -18.39 dB \tag{22}$$

The transfer function is plotted as:

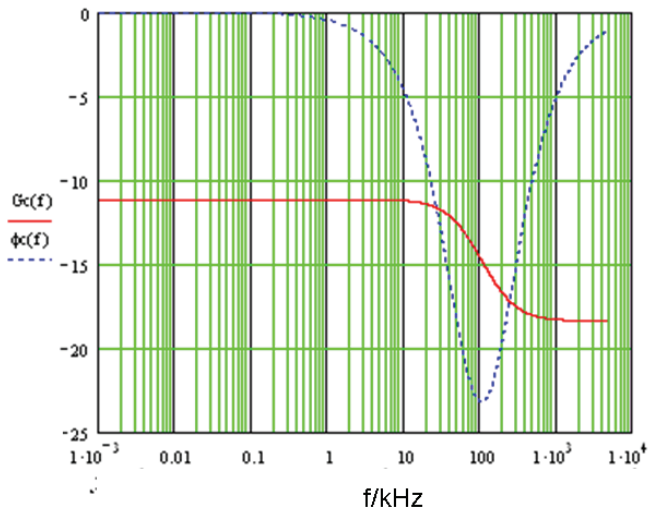

Fig. 22. Feedback divider with capacitor and resistor across the bottom feedback divider transfer function.

F. *Feedback Divider Forming an "All Pass"*

The capacitors across the feedback resistor form an "all-pass" filtering any possible noise present at the feedback to ground without changing the overall converter gain or phase. The capacitors have to be selected inversely proportional to the resistor divider.

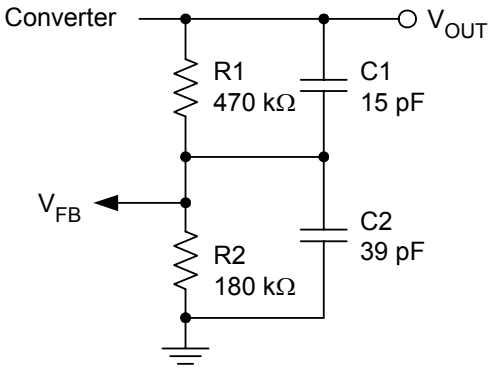

Fig.23. Feedback divider forming an "all pass".

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \tag{23}$$

with

$$G(s) = \frac{1 + sC1R1}{1 + \frac{R1}{R2} + sR1(C1 + C2)} \tag{24}$$

C2 is selected inversely proportional to the resistor divider:

$$C2 = \frac{R1}{R2} \bullet C1 \tag{25}$$

The transfer function is plotted as:

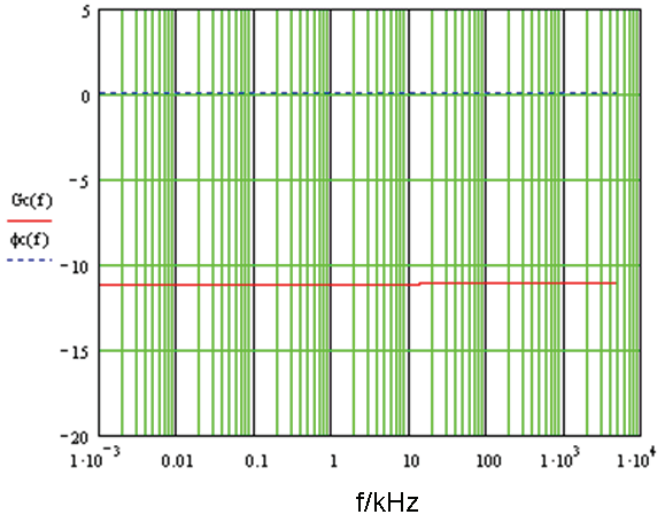

Fig 24. Feedback divider forming an "all pass" transfer function.

G. *Feedback Divider Placing a Pole and Zero with Dominant Pole*

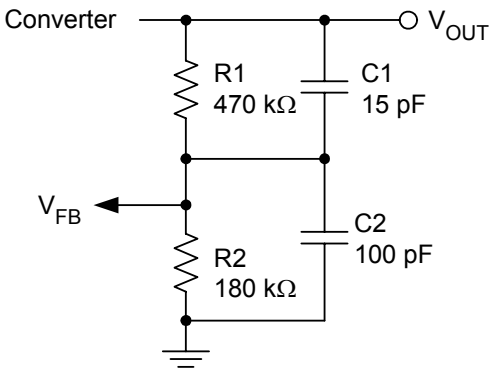

Fig. 25. Feedback divider placing a pole and zero with dominant pole.

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \tag{26}$$

with

$$G(s) = \frac{1 + sC1R1}{1 + \frac{R1}{R2} + sR1(C1 + C2)} \tag{27}$$

The configuration reduces the overall converter gain. If the pole is placed at low frequencies then the phase margin at the crossover frequency of the converter remains the same. R1 and C1 place a zero in the transfer function at:

$$fz = \frac{1}{2\pi \bullet R1 \bullet C1} = \frac{1}{2\pi \bullet 470k\Omega \bullet 15pF} = 22.5kHz \quad (28)$$

A pole is placed at:

$$fp = \frac{1}{2\pi \bullet (C1 + C2) \bullet \frac{R1 \bullet R2}{R1 + R2}} = 10.63kHz \quad (29)$$

Placing the pole before the zero gives a "dominant" pole. The intention of this compensation is to reduce the gain at high frequencies without losing phase margin.

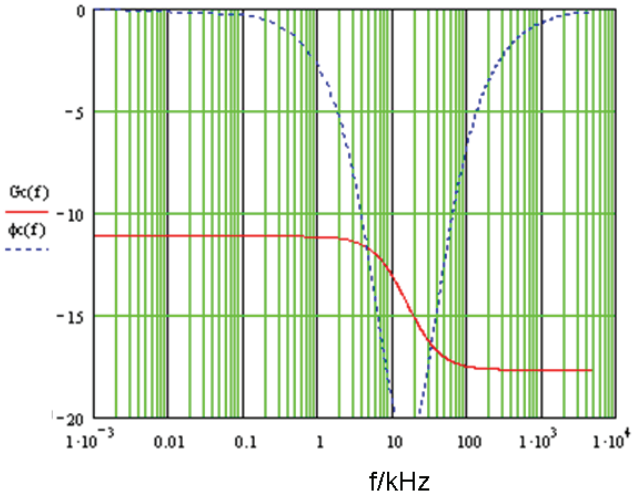

Fig 25. Transfer function of feedback divider placing a pole and zero with dominant pole.

H. Feedback Divider Placing a Pole and Zero with Dominant Zero

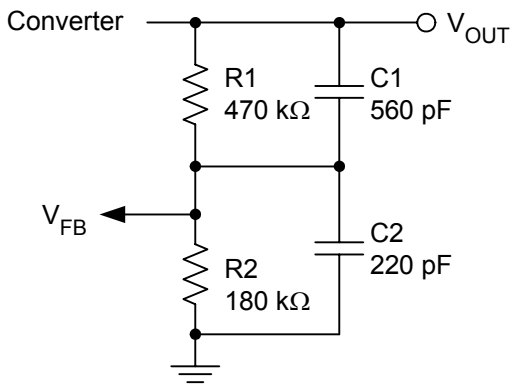

Fig 26. Feedback divider placing a pole and zero with dominant zero.

The feedback divider transfer function becomes:

$$G(s) = \frac{V_{FB}}{Vo} = \frac{Z2(s)}{Z1(s) + Z2(s)} \quad (30)$$

with

$$G(s) = \frac{1 + sC1R1}{1 + \frac{R1}{R2} + sR1(C1 + C2)} \quad (31)$$

The configuration is used to increase the high frequency gain. If the zero is placed at low frequencies then the phase margin at the crossover frequency of the converter remains the same. R1 and C1 place a zero in the transfer function at:

$$fz = \frac{1}{2\pi \bullet R1 \bullet C1} = \frac{1}{2\pi \bullet 470k\Omega \bullet 15\,pF} = 604\,Hz \quad (32)$$

A pole is placed at:

$$fp = \frac{1}{2\pi \bullet (C1 + C2) \bullet \frac{R1 \bullet R2}{R1 + R2}} = 1.56kHz \quad (33)$$

Placing the pole after the zero gives a "dominant" zero. The intention of this compensation is to increase the high frequency gain and when placed just before the crossover frequency of the converter it improves the phase margin as well. Then the compensation improves the load transient response as well.

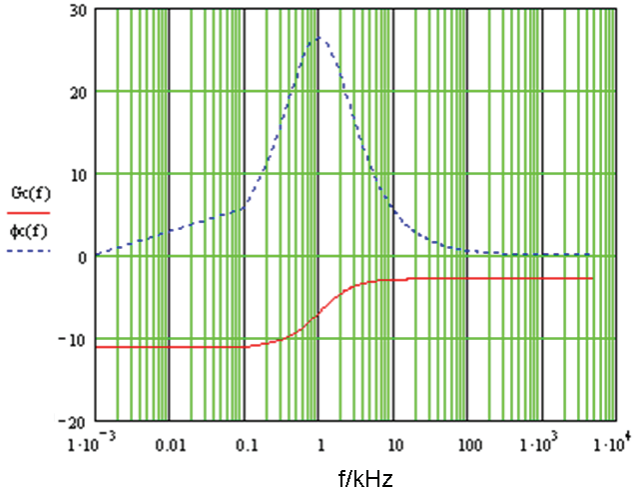

Fig. 27. Transfer function of feedback divider placing a pole and zero with dominant zero.

V. Conclusion

The paper demonstrates the evaluation and test of a DC/DC converter. The converter loop gain and crossover frequency can be measured using standard equipment. A simple load transient test allows the determination of the phase margin and crossover frequency of the converter loop. Using a Network analyzer or a dedicated phase/gain analyzer gives a more detailed and complete picture of the converter loop over the entire frequency range. The external feedback divider is an effective and simple tool to optimize and compensate the converter loop and load transient response.

VI. Acknowledgements

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