

Under the Hood of a DC/DC Boost Converter

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ABSTRACT

Despite having the same number of significant power components as the well-understood buck converter, the boost converter has the reputation of being low-performance and complicated to design. This topic discusses continuous-conduction-mode (CCM) and discontinuous-conduction-mode (DCM) operation of the boost converter in practical terms and presents a mathematical model for analysis of voltage-mode and current-mode feedback control.

I. INTRODUCTION

Necessitated by the proliferation of devices requiring unique voltage rails, the single-voltage, intermediate-bus architecture has gained in popularity over using a centralized, multivoltage source. Localized point-of-load converters optimized for specific loads remove from the system the overhead of multiple-voltage distribution. While stepping the intermediate-bus voltage down to a lower voltage with buck converters is the most common requirement, there is the occasional need for a boost converter to step the bus voltage up.

This topic discusses a few basics of the boost topology, going into some detailed discussion regarding modes of operation, and then discusses design trade-offs in the control options and their effect on overall converter performance. Mathematical models aid in the analysis.

Examples presented in this text discuss a number of fixed-frequency boost converters designed with a TPS40210 controller operating at a nominal 700 kHz (Fig. 1). For all of the converters, the input voltage is 12 V and the output voltage is 24 V, with a sourcing-current capability of 1 A. The individual implementations of each converter will highlight differences in various modes of operation.

II. TRANSFER OF ENERGY

To help facilitate this discussion of the boost power stage, we begin with three underlying assumptions.

1. In steady-state operation, the volt seconds ($V \cdot s$) across the inductor, $L1$, during the ON time of the switch, $Q1$, must be equal to the $V \cdot s$ across the inductor during the switch OFF time. In other words, the average $V \cdot s$ over a single switching period is zero. This assumption ensures steady-state operation from one switching cycle to the next.
2. Charge balance in output capacitor. In steady-state operation, the ampere-seconds ($A \cdot s$) charging the output capacitor during the ON time of the switch must be equal to the $A \cdot s$ discharging of the capacitor during the switch OFF time. This means

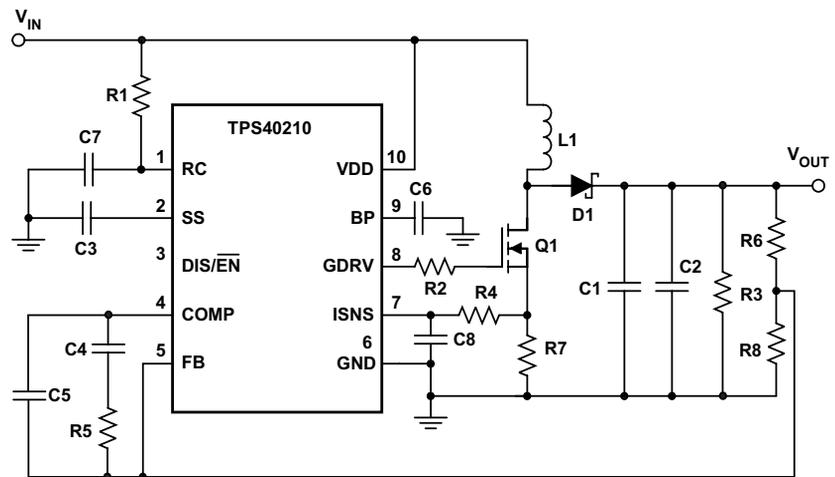


Fig. 1. Generalized circuit schematic of a TPS40210-based boost converter.

that the average $A \cdot s$ over a single switch period is zero. This assumption ensures steady-state operation from one switching cycle to the next.

3. The ripple voltage across the output capacitor is small compared to the DC voltage generated by the converter. This assumption simplifies the analysis somewhat when we look at the $V \cdot s$ balance across the inductor.

The nonsynchronous boost topology is one of the few topologies where, even if the converter is off, there is an output voltage. Unfortunately, the voltage is unregulated and is subject to every change of the input. Under this steady-state condition, load current—if there is any—flows continuously through the inductor and diode and into the load. With the exception of the drop across the inductor due to the DC resistance, there is no voltage across the inductor.

To generate a regulated output voltage, the switch must begin switching. When switch Q1 turns ON, the voltage across the inductor increases to approximately the input voltage, and energy is stored in the inductor. The amount of energy stored is a function of the input voltage, the inductance, and the duration of the ON pulse. The diode rectifier, D1, is reverse-biased during this time interval. When the switch turns OFF, the stored energy releases to the output through the rectifier. The output capacitor filters the pulsating current, allowing DC current to flow into the load.

There are two fundamentally different operating modes for the converter. The first, continuous-conduction mode (CCM), is where energy in the inductor flows continuously during the operation of the converter. The increase of stored energy in the inductor during the ON time of the switch is equal to the energy discharged into the output during the OFF time of the switch, ensuring steady-state operation. At the end of the discharge interval, residual energy remains in the inductor. During the next ON interval of the switch, energy builds from that residual level to that required by the load for the next switching cycle.

In the other mode, discontinuous-conduction mode (DCM), the energy stored in the inductor during the ON interval of the switch is equal only to the energy required by the load for one switching

cycle, plus an amount for converter losses. The energy in the inductor depletes to zero before the end of each switching cycle, resulting in a period of no energy flow, or discontinuous operation.

These two operating modes have significant influence on the performance of the converter. One of the first decisions to make in designing a boost converter is to select in which of these two modes the converter is to operate.

Unlike a buck-derived topology, energy flows to the load during the OFF time of the control switch. The effect of any control action during the ON time of the switch is delayed until the switch is turned OFF. For example, during a load-step increase, the output voltage drops due to insufficient stored energy in the inductor. The lower output voltage in turn creates a demand for a longer pulse width in order to store additional energy in the inductor. In a fixed-frequency converter, a longer ON-time pulse means a shorter OFF-time pulse, which means the output will droop even further. It is not until the release of the energy in the inductor from the longer ON-time pulse that the output voltage will reverse towards regulation. From the standpoint of small-signal feedback control, the phenomenon of the output response initially going in the opposite direction of the desired correction creates a right-half-plane (RHP) zero, so named because of the placement of the zeros in the right-half plane of a complex s -plane. The frequency-response curve in Fig. 2 shows that with a left-half-plane (LHP) zero (as from the ESR of a capacitor), the phase *increases* with increasing gain; and with an RHP zero, the phase *decreases* with increasing gain. This condition makes compensating the control loop a difficult task if a feedback loop is to have adequate phase margin. This discussion later shows that design decisions regarding mode of operation and the choice of control method largely alleviate the RHP-zero effect.

A. Continuous-Conduction Mode (CCM)

In CCM, power transfer is a two-step process. When the switch is ON, stored energy builds in the inductor. When the switch is OFF, energy transfers to the output through the diode. The switch current is a stepped sawtooth with a fixed steady-state ON time with some amount of ripple

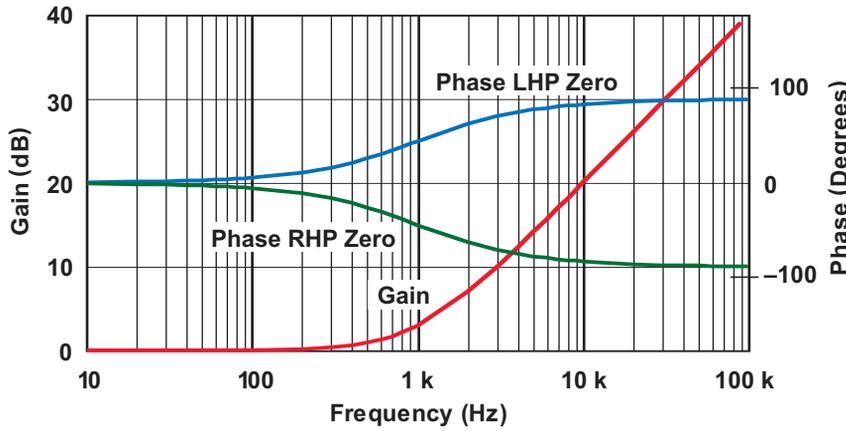


Fig. 2. Examples of frequency response RHP and LHP zeros.

current superimposed. During the ON time of the switch, if we assume zero losses for the moment, the voltage across the inductor is approximately the input voltage; and the voltage across the rectifier is the capacitor, or output voltage. When the switch turns OFF, the energy stored in the inductor releases into the output through the rectifier. The voltage across the inductor is approximately the input-to-output voltage difference, and the voltage across the switch becomes approximately the output voltage (see Fig. 3).

Important to any model is the understanding of the current in each of the relevant components in the power path. The mathematical construction of these currents helps to determine the magnitude and shapes of these currents.

With zero losses assumed, the inductor current's ON-time slope is

$$m_{I_{L(ON)}} = \frac{V_{IN}}{L}. \quad (1)$$

During the OFF time, the current will have a slope of

$$m_{I_{L(OFF)}} = \frac{V_{IN} - V_{OUT}}{L}. \quad (2)$$

If the V•s during the ON time of the switch is equated with the V•s during the OFF time of the switch,

$$\frac{V_{IN}}{L} \times D \times T_s = \frac{V_{IN} - V_{OUT}}{L} \times (1 - D) \times T_s. \quad (3)$$

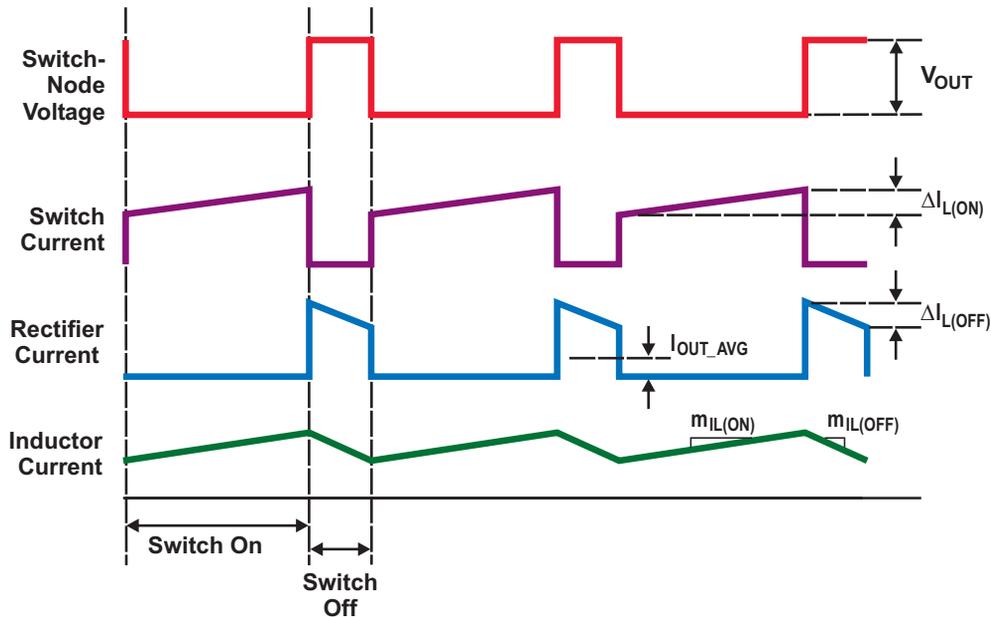


Fig. 3. Representative CCM waveforms.

*See Appendix C for a glossary of variables.

Solving for the switch duty cycle, D , results in

$$D_{CCM(ideal)} = 1 - \frac{V_{IN}}{V_{OUT}} \quad (4)$$

Power-stage input and output losses that impact the duty cycle are shown in Fig. 4. The input losses include the inductor winding resistance (R_L), the switch MOSFET $R_{DS(ON)}$, and (in the case of a current-mode-controlled converter) a current-sense resistor (R_{ISENSE}). The output losses are represented by the output diode rectifier, D1.

If the loss elements of the power-stage components are included, the equation for the duty cycle in CCM is shown by Equation (5) below. Equation (5) holds true for CCM when the ripple current in the inductor is small relative to the average DC current. The equation is “close” when there is a high percentage of ripple current. Reassuringly, if the losses in Equation (5) reduce to zero, the equation simplifies to the ideal case.

B. Discontinuous-Conduction Mode (DCM)

In DCM, a switching cycle is composed of three intervals. The first two are the same as in CCM, where energy is stored in the inductor during the ON time of the switch, and transferred to the load during the OFF time of the switch. In DCM, however, all of the energy in the inductor transfers to the load during this second interval. The third interval begins when the energy in the inductor is depleted, and terminates at the end of the switching period the next time

the switch turns on. During this third interval (the idle period in Fig. 5), the voltage across the inductor decays to zero, the voltage across the switch decays to the input voltage, and the input-to-output voltage differential is across the rectifier. There is essentially no current flowing in the power stage during this interval.

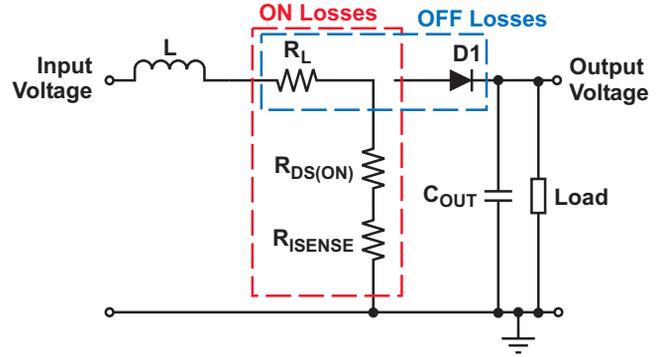


Fig. 4. Boost model with loss elements.

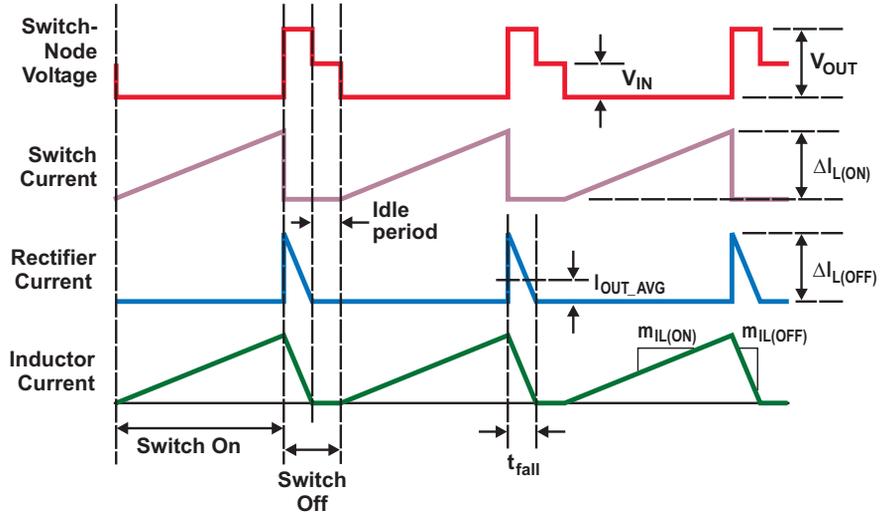


Fig. 5. Representative DCM waveforms.

$$D_{CCM} = 1 - \frac{\left\{ \frac{V_{IN} + I \times (R_{DS(ON)} + R_{ISENSE})}{\sqrt{[V_{IN} + I_{OUT} \times (R_{DS(ON)} + R_{ISENSE})]^2 - 4I_{OUT} \times (R_{DS(ON)} + R_{ISENSE}) \times (V_{OUT} + V_d)}} \right\}}{2(V_{OUT} + V_d)} \quad (5)$$

Observe that since all of the energy in the inductor discharges in each switching cycle during an interval shorter than the $(1 - D)$ conduction time, the peak current in the diode must be higher in DCM than in CCM. If the peak current is higher in the diode in DCM, then the peak current will be higher in the inductor and in the switch as well. With higher peaks and the same or a shorter conduction time, as a rule of thumb, we can assume that for the same components, the RMS losses will be greater in a DCM converter than in an equivalent CCM converter.

The operating duty cycle of the converter in DCM is dependent not only on the input and output voltages but on the inductor value and load current as well. In addition, in DCM operation, the current fall time (to zero) is usually different than $(1 - D) \times T_s$. To find the duty cycle in DCM, we can first find the fall time that is required to discharge the inductor by taking the peak current during the ON time and dividing it by the current's rate of decay during the OFF time:

$$t_{\text{fall}} = \frac{m_{I_{L(\text{ON})}}}{-m_{I_{L(\text{OFF})}}} \times D \times T_s \quad (6)$$

The negative sign in the denominator of t_{fall} is due to the OFF-time slope being a negative value. If t_{fall} is less than $(1 - D) \times T_s$, the converter is operating in DCM. That is, if the time to discharge the energy in the inductor to zero is less than the OFF time of the switch, the converter is operating in DCM. Under this condition, the fall-time duty cycle, D_{disch} , is

$$D_{\text{disch}} = \frac{t_{\text{fall}}}{T_s} = \frac{V_{\text{IN}}}{V_{\text{OUT}} - V_{\text{IN}}} \times D_{\text{DCM}} \quad (7)$$

In steady-state operation, the average output current is equal to the average diode current. This average output current is equal to the peak current, averaged over the switching period:

$$\begin{aligned} I_{\text{OUT}} &= \frac{V_{\text{IN}} \times T_s}{2L} \times D_{\text{DCM}} \times D_{\text{disch}} \\ &= \frac{V_{\text{IN}} \times T_s}{2L} \times \frac{V_{\text{IN}}}{V_{\text{OUT}} - V_{\text{IN}}} \times D_{\text{DCM}}^2 \end{aligned} \quad (8)$$

Solving for the DCM duty cycle results in

$$D_{\text{DCM}} = \frac{1}{V_{\text{IN}}} \sqrt{\frac{2L \times (V_{\text{OUT}} - V_{\text{IN}})}{T_s}} \times I_{\text{OUT}} \quad (9)$$

If losses are included, the following is a slightly better approximation[†]:

$$\begin{aligned} D_{\text{DCM}} &= \frac{1}{V_{\text{IN}} - \frac{(V_{\text{OUT}} + V_d) \times I_{\text{OUT}}}{V_{\text{IN}}} \times R_{\text{tot}}} \\ &\times \sqrt{\frac{2L \times (V_{\text{OUT}} + V_d - V_{\text{IN}})}{T_s}} \times I_{\text{OUT}} \end{aligned} \quad (10)$$

III. DESIGNING FOR CCM OR DCM OPERATION

The two design parameters whose selection a designer can control when determining the operating mode of the converter at a given load current are the switching frequency and the value of the inductance. If the converter size and overall switching loss determine the switching frequency, the inductor value remains as the only design parameter available to determine whether the converter will operate in CCM or DCM. To find the value of inductance required to guarantee operation in the selected mode, we can set the CCM and DCM duty cycles to be equal, and solve for L:

$$L = \frac{V_{\text{IN}} \times T_s}{2I_{\text{OUT_DCM}}} \times D_{\text{CCM}} \times (1 - D_{\text{CCM}}) \quad (11)$$

Note that the requirement for inductance is at a maximum at the 50% duty cycle and decreases at the duty-cycle extremes. This highlights the need to check all aspects of operation when component values are being determined.

[†]This approximation assumes that voltage drops are due to the *average* current, whereas the actual drops are due to the *peak* current. The approximation loses accuracy if the voltage drops due to the loss elements are a significant percentage of the input voltage.

For simplicity, further equations will omit the loss terms. Fig. 6 compares waveforms obtained from a CCM and a DCM boost converter (both designed from the schematic in Fig. 1 and simulated in SIMPLIS™). Arbitrarily selecting CCM operation at down to a 100-mA load results in $L = 22 \mu\text{H}$. From Equation (11), $L = 1.0 \mu\text{H}$ is selected to allow DCM operation of the other converter over a wide duty-cycle range.

The RMS and average values of the currents may be calculated and compared with the technique outlined in Appendix A. A waveform calculator has inserted values from the simulation in the figure.

In all three paths, the peak and RMS currents are larger in the DCM converter. This implies that for equivalent resistive components, power losses will be higher and turn-off switching and recovery losses will be higher. For the diode, the average current is the same in both modes; therefore the conduction losses will be the same.

In Sections III.A through III.C, we develop a small-signal model to analyze the feedback

loop in four configurations: CCM and DCM operation with voltage-mode control (VMC), and CCM and DCM operation with peak-current-mode control (peak-CMC).

A. VMC in CCM Small-Signal Analysis

Fig. 7 depicts how the error-amplifier output, V_C , controls the converter's output voltage, V_{OUT} . Understanding this VMC transfer is necessary to ensure that the network is capable of controlling the output voltage over the entire range of operation.

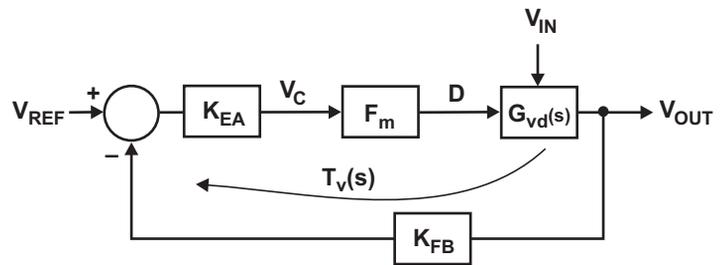


Fig. 7. Simplified transfer-function diagram of VMC.

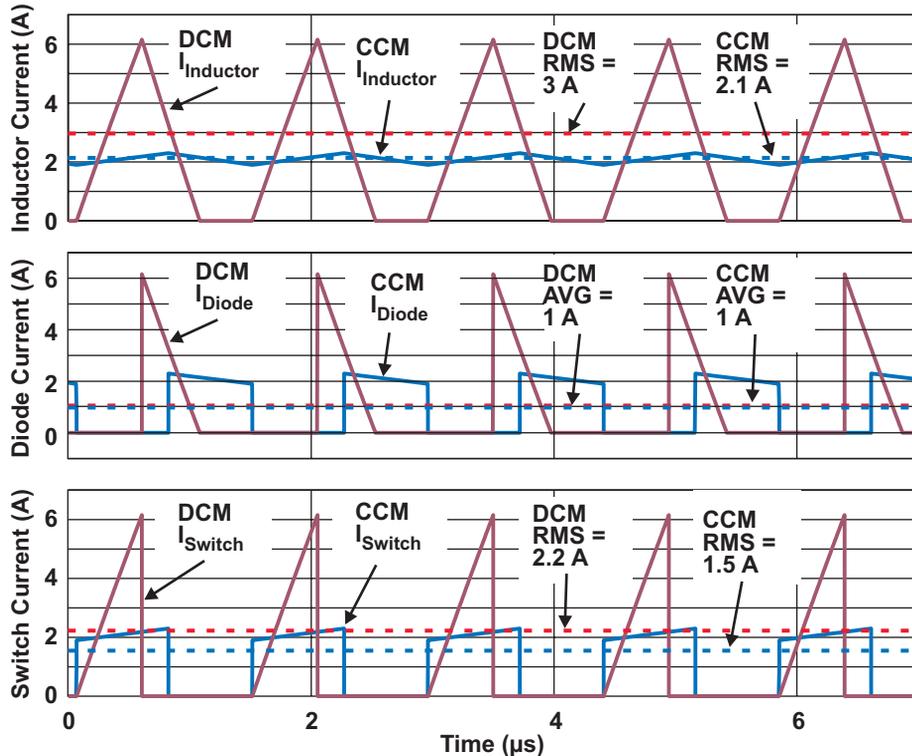


Fig. 6. Comparison of waveforms from CCM and DCM converters.

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The modulator gain, F_m , is the transfer function that generates the duty cycle based on the V_C control voltage. That is, for a given change in V_C , the duty cycle will change by an amount proportional to the modulator gain. For VMC, F_m is simply

$$F_m = \frac{1}{m_a \times T_s}, \quad (12)$$

where m_a is the slope of a sawtooth ramp waveform (Fig. 8). The controller’s internal clock oscillator usually generates this sawtooth waveform. As a side note, the TPS40210 is configurable so that m_a is fixed or is a function of the input voltage. This provides an option for including voltage feedforward to the transfer function. The impact of increasing the slope, m_a , is a decreasing F_m , the result of which is described later in this section.

The small-signal duty-cycle-to-output-voltage transfer function, $G_{vd_CCM}(s)$, is determined from the boost circuit’s impedances (Fig. 9). Z_{ON} is the impedance of the inductor as a function of frequency, plus the $R_{DS(ON)}$ of the MOSFET switch and any other series impedances:

$$Z_{ON} = Z_L + R_{DS(ON)} + R_{ISENSE} \quad (13)$$

Z_{OFF} is the parallel combination of the output capacitors and the load resistance:

$$Z_{OFF} = \frac{Z_C \times R_{load}}{Z_C + R_{load}} \quad (14)$$

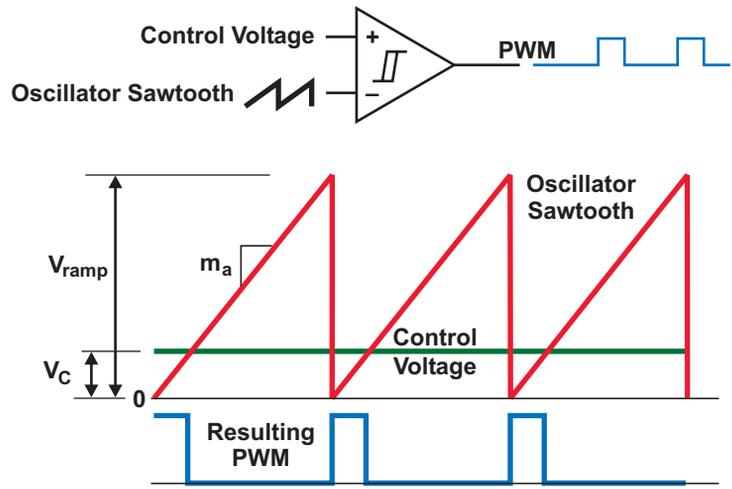


Fig. 8. Pulse-width modulation (PWM).

Note that if the output capacitors are of mixed types (i.e., aluminum electrolytic and ceramic), their impedances may be included in this parallel combination, allowing characterization of converters with a variety of mixed component types.

The derivation of $G_{vd_CCM}(s)$ is developed in detail in Reference [1]. Without re-creating that work here, it is sufficient to give that function for CCM in terms of circuit impedances as

$$G_{vd_CCM}(s) = V_{IN} \times M_{CCM}^2 \times \frac{1 - \frac{Z_{ON} \times M_{CCM}^2}{R_{load}}}{1 + \frac{Z_{ON} \times M_{CCM}^2}{Z_{OFF}}} \quad (15)$$

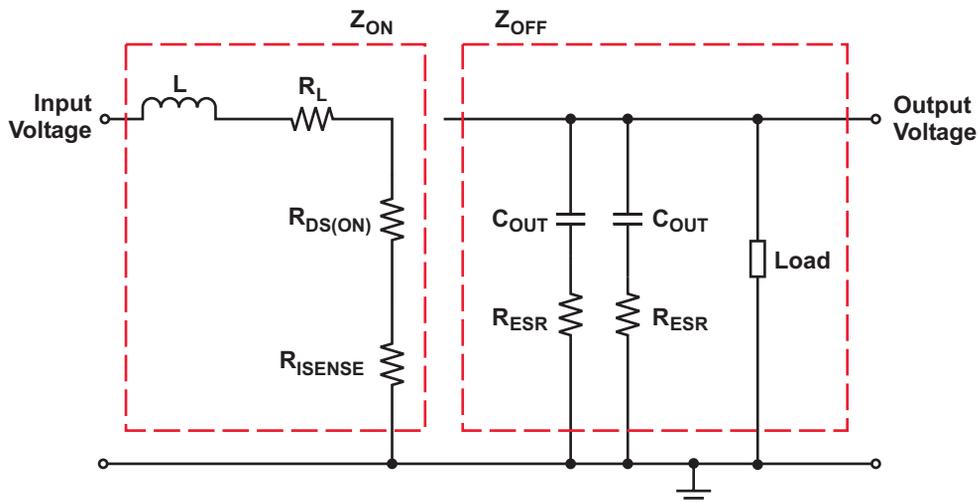


Fig. 9. Circuit highlighting ON- and OFF-time impedances.

where M_{CCM} is the conversion ratio in CCM,

$$M_{CCM} = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}. \quad (16)$$

It is in $G_{vd}(s)$ that the RHP zero comes into play. As the numerator of Equation (15) indicates, the zero is a function of the converter's ON impedance (determined from the inductor value, the frequency, and parasitic impedances) load, and duty cycle. In Fig. 10, the span of movement of the RHP zero is from about 23 kHz to 96 kHz over the input-voltage range. At lighter load (Fig. 11), the RHP zero moves to a much higher frequency, likely beyond any frequency of interest. Note again that the ESR-zero frequency of the output capacitor is just over 11 kHz. The interaction of the two zeros (the RHP zero from the converter and the LHP zero from the capacitor's ESR) tends to flatten the phase response while providing a double-zero correction to the L-C filter double pole.

Notice also that the lower gain occurs at higher input voltages (smaller M_{CCM} , Equation (16)). This is in contrast to a buck-derived converter where the gain increases with increasing input voltage. In this example, adding input-voltage feedforward increases the gain spread for the 9- to 18-V input-voltage change from -5.5 dB (see Figs. 10 and 11) to -11.5 dB. This further decrease in gain with increasing input voltage is due to the decrease in F_m with input voltage (see Equation (12)).

Putting the blocks together yields the control-to-output transfer function of the converter:

$$G_{vc}(s) = F_m \times G_{vd}(s) \quad (17)$$

The dominant pole in CCM is generated from the ratio of the network impedance when the switch is on (basically, the inductor impedance) to the output-network impedance when the switch is off (when the output capacitance is in parallel with

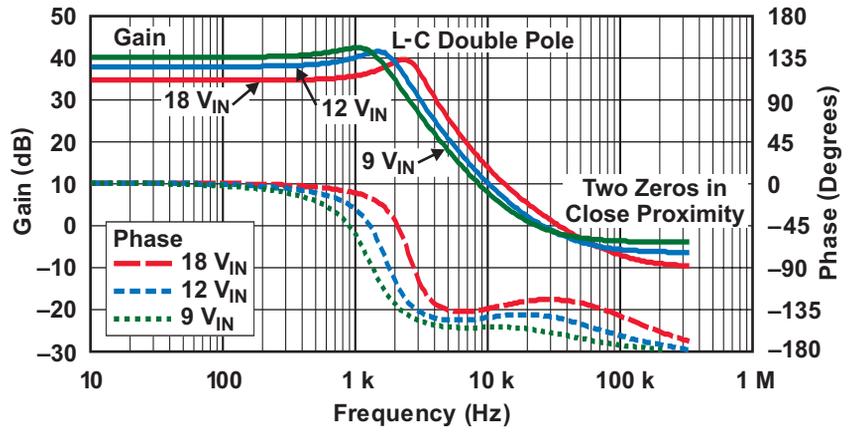


Fig. 10. Control-to-output Bode plot for VMC CCM operation at 1-A load.

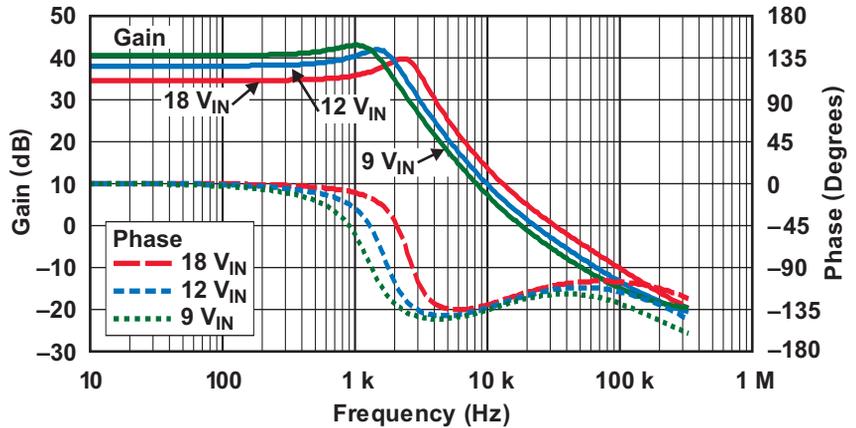


Fig. 11. Control-to-output Bode plot for VMC CCM operation at 150-mA load.

the load resistance), scaled by the CCM duty cycle.

With VMC used in CCM, the three dominant characteristics of the curves are observable (see Fig. 10):

- A relatively low-frequency double pole due to the inductor and output capacitor
- An RHP zero due to the inductor, the load, and the duty cycle
- An LHP zero due to the output capacitor and ESR

The complexities in compensating this path are numerous (Figs. 10 and 11): The RHP zero shifts in frequency with varying duty cycle and load, and the gain changes inversely with input voltage. The zero occurs with a control-to-output gain above 0 dB, and the phase shifts dramatically

in the 1- to 5-kHz range. The output capacitor's ESR provides an additional phase boost (at 11 kHz in these plots), lessening the available margin. To compensate this control loop, a feedback network must be designed so that the closed-loop response has a crossover frequency in the low 100s of hertz, perhaps an octave below the minimum worst-case L-C pole frequency and the dramatic phase shift.

B. VMC in DCM Small-Signal Analysis

In DCM, the energy stored in the inductor in each switching cycle is equal to the output energy and is a function of the input voltage, the inductance, and the output power. Equating the energy over a switching cycle gives us the conversion ratio:

$$M_{DCM} = \frac{1 + \sqrt{1 + 2 \times \frac{(V_{OUT} + V_d) \times D^2 \times T_s}{I_{OUT} \times L}}}{2} \quad (18)$$

The control-to-output transfer characteristic in DCM is

$$G_{vd_DCM}(s) = \frac{2V_{OUT}}{D} \times \frac{M_{DCM} - 1}{2M_{DCM} - 1} \times \frac{1 - \frac{s \times D}{2F_s}}{1 + \frac{(M_{DCM} - 1) \times R_{load}}{(2M_{DCM} - 1) \times Z_C}} \quad (19)$$

In DCM, and because of the relatively smaller inductor, the RHP-zero frequency extends to beyond the switching frequency with negligible impact at typical loop crossover frequencies [2]. See Figs. 12 and 13.

The low-frequency pole is a function of the output capacitance and load resistance, and is lower in frequency than in the CCM example.

The gain change over an input voltage range is +4.7 dB. This is because $G_{vd}(s)$ now increases

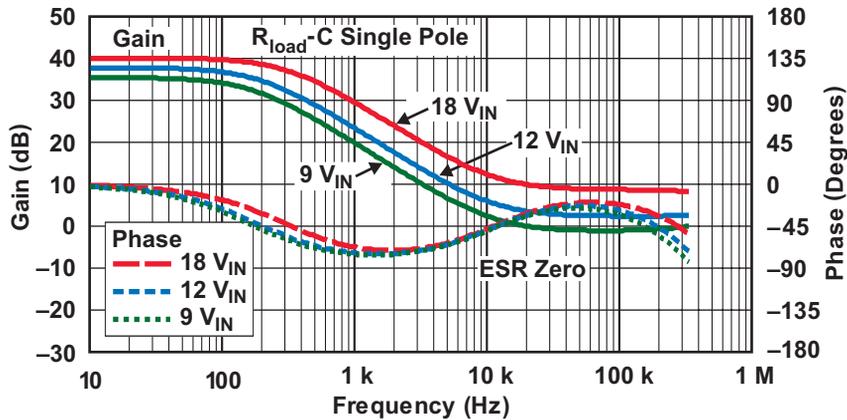


Fig. 12. Control-to-output Bode plot for VMC DCM operation at 1-A load.

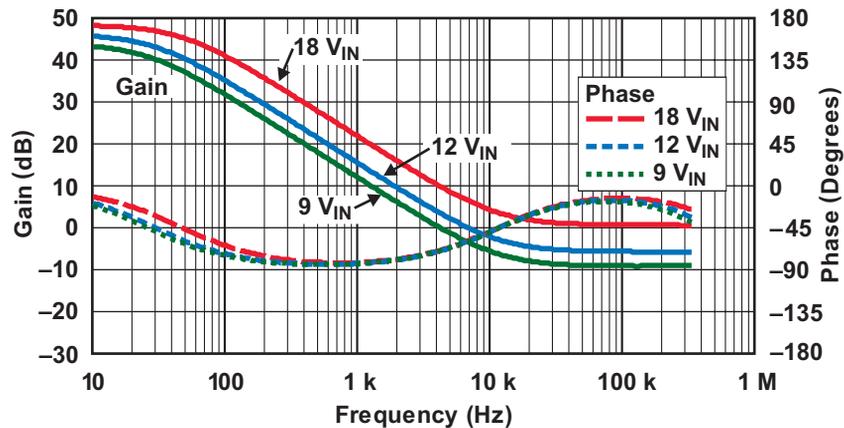


Fig. 13. Control-to-output Bode plot for VMC DCM operation at 150-mA load.

with increasing V_{IN} . Adding voltage feedforward reduces F_m with increasing input voltage and reduces the gain variation to -1.3 dB.

To compensate this converter, a network with a zero at a few hundred hertz and a pole at about 10 kHz will yield a stable system with a crossover frequency in the low 10s of kilohertz.

C. Peak-Current-Mode Control

Incorporating peak-CMC is a matter of monitoring the switch current during the ON time of the switch and summing a current signal into the modulator (see Fig. 14). The modulator gain then becomes

$$F_m = \frac{1}{m_n \times T_s}, \quad (20)$$

where m_n is a slope proportional to the inductor's current slope during the ON time of the switch,

$$m_n = m_{IL(ON)} \times R_{ISENSE} \times A_{CS}, \quad (21)$$

and A_{CS} is the gain of the current-sense amplifier. Notice that the current slope is a function of the input voltage (Equation (1)), and that a shift in gain will occur from that changing slope. The effect is similar to that of voltage feedforward in the VMC converter.

The current feedback path has a transfer function in CCM, but not in DCM. This is because

there is no output information in the current signal in DCM.

$$G_{id_CCM}(s) = 2I_{OUT} \times M_{CCM}^2 \times \frac{1 + \frac{R_{load}}{2Z_C}}{1 + \frac{Z_{ON} \times M_{CCM}^2}{Z_{OFF}}}, \quad (22)$$

where M_{CCM} is defined by Equation (16).

As shown in Fig. 15, the inner current loop is

$$T_I(s) = F_m \times A_{CS} \times R_{ISENSE} \times G_{id}(s) \times H_e(s), \quad (23)$$

where $H_e(s)$ is the sampling gain[‡][3]. The sense resistor, R_{ISENSE} , used in this example is 50 mΩ, and the current-sense gain (A_{CS}) of the TPS40210 is about 6.

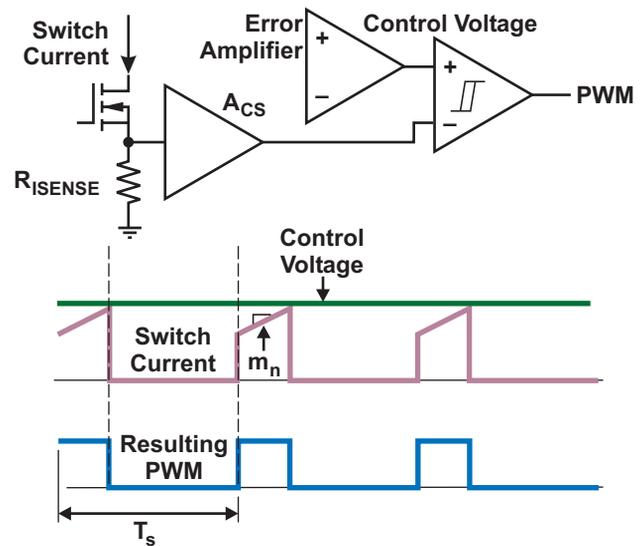


Fig. 14 Current Mode PWM.

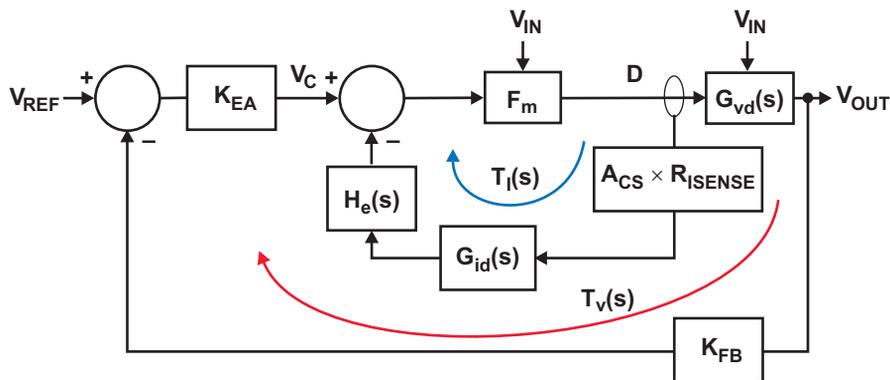


Fig. 15. Simplified block diagram of CMC converter.

[‡]The sampling gain is a modeling tool that allows the zero-order sample-and-hold effects of peak-CMC to be included in this simple frequency-domain model.

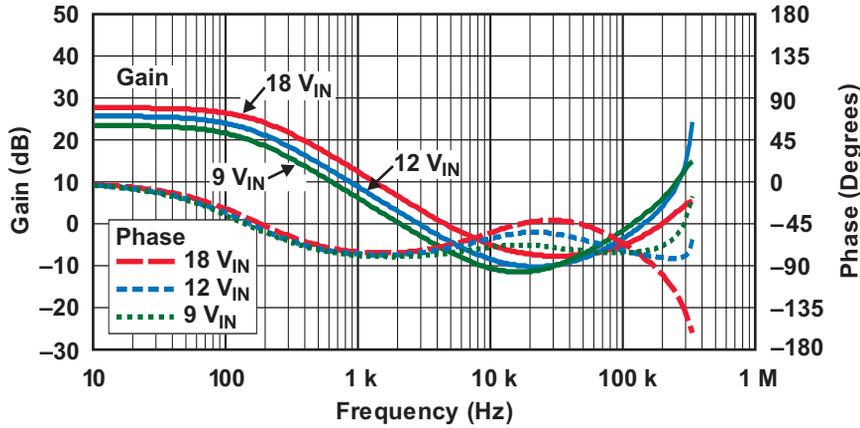


Fig. 16. Control-to-output Bode plot for CMC CCM operation at 1-A load.

The control-to-output transfer function, including the inner current loop, is

$$G_{vc}(s) = \frac{F_m \times G_{vd}(s)}{1 + T_I(s)} \times e^{-s \times t_d}, \quad (24)$$

where $e^{-s \times t_d}$ is the delay time from the PWM comparator input to the transition of the converter switch node. This delay introduces a phase lag at higher frequencies.

The inner current loop tends to reduce the overall gain of the system, in this example by about 13 dB. The voltage feedforward of the current feedback reduces the gain variation over the input-voltage range to 4.2 dB. The slope above resonance is reduced to -20 dB/decade, allowing a simple type II compensation to yield a closed-loop crossover frequency in the middle kilohertz range. A crossover frequency any higher could cause gain-margin instability because of the higher-frequency zero.

Notice in Fig. 16 that the 12-V response curve has high peaking at high frequencies. This peaking occurs at near 50% duty cycle at half the switching frequency. This peaking is due to the sample-and-hold effect of the peak-CMC and the inherent tendency towards subharmonic oscillation.

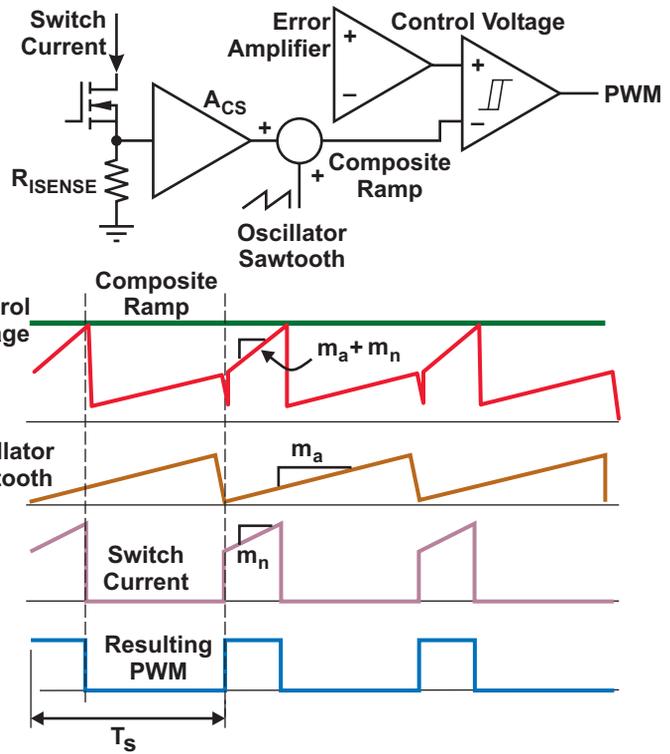


Fig. 17 Current-mode PWM with slope compensation.

Slope Compensation

The addition of an external ramp to the current-feedback signal reduces the effect of subharmonic oscillation (see Fig. 17). An artificial ramp, m_a , is summed with the signal proportional to the current-feedback signal, m_n , creating a composite signal that is used to determine the modulator gain:

$$F_m = \frac{1}{(m_a + m_n) \times T_s} \quad (25)$$

Adding slope compensation helps control the high-frequency peak at the expense of lower overall control-to-output gain. In Fig. 18, a slight amount of slope compensation is included, resulting in reduced peaking at the duty cycle extremes; however, there is insufficient slope compensation to remove the peaking at wide (low input voltage) duty cycle.

In Fig. 19, the load is reduced to 150 mA, resulting in a minor shift in the low-frequency pole and a dramatic shift in the RHP zero to higher frequency. A pole at about 11 kHz is necessary to compensate the ESR zero. The crossover frequency should be limited to less than 10 kHz to prevent the peaking at high frequency from affecting overall stability.

Current-Mode DCM Operation

In DCM, changes in control-to-output gain depends on changes in the modulator gain, F_m . There is no AC contribution ($G_{id}(s)$) in DCM because the energy builds from zero in each switching cycle; i.e., there is no contribution from the output to the feedback signal within the current signal. In Figs. 20 and 21, the current-sense resistor is reduced from 50 mΩ to 17 mΩ to limit the peak voltage at the sense pin and to keep power dissipation low.

With essentially only a gain shift, the curves follow the poles and zeros of the VMC converters operating in DCM. The inclusion of slope compensation, with or without voltage feed-forward, has only a minor effect on this signal path

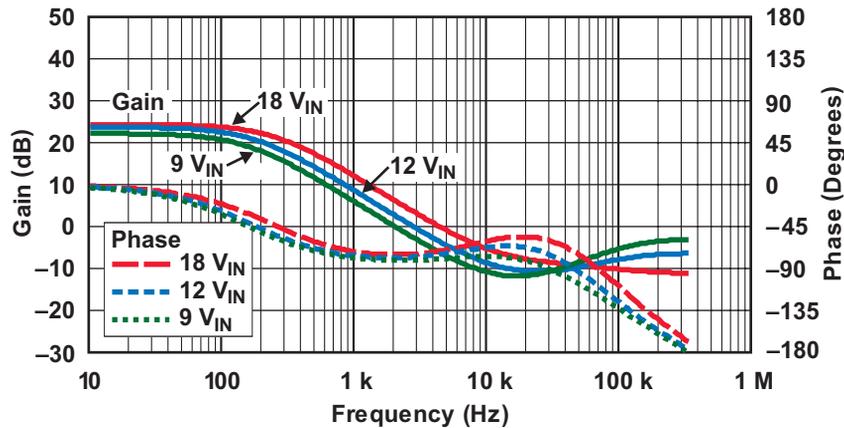


Fig. 18. Control-to-output Bode plot for CMC CCM operation at 1-A load, including slope compensation.

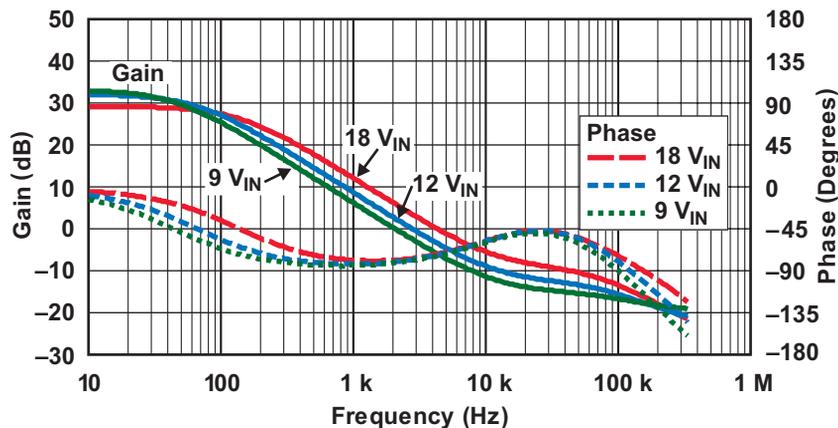


Fig. 19. Control-to-output Bode plot for CMC CCM operation at 150-mA load, including slope compensation.

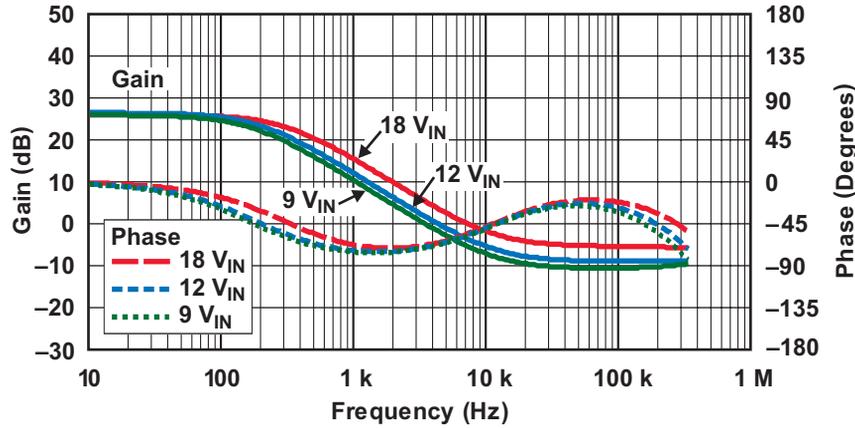


Fig. 20. Control-to-output Bode plot for CMC DCM operation at 1-A load.

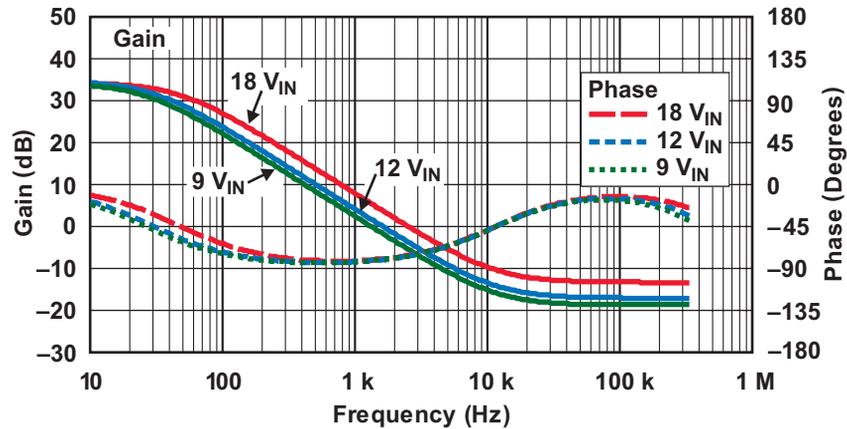


Fig. 21. Control-to-output Bode plot for CMC DCM operation at 150-mA load.

because of the relatively large current signal. The ESR zero dominates the curves in the areas of interest for loop crossover.

D. Component Selection and Design Considerations

Inductor Selection

The inductance required by a converter operating in DCM at heavy load will be much lower than the inductance of a converter operating in CCM under the same load condition. This means the inductor in a DCM converter will likely have lower winding resistance than the inductor in a CCM converter. Although the RMS current is higher in a DCM converter, the winding losses in the inductor may be equivalent to or less than those of the CCM counterpart.

The peak-current rating of the inductor selected should be well above the expected peak current of

the converter, including transients. The winding resistance should be low enough to limit power dissipation and avoid overheating. The structure of the inductor should yield low interwinding capacitance to limit ringing and EMI. A closed-field magnetic structure also reduces radiated EMI.

In a DCM design, high ripple current can create high core losses. High losses increase temperature, which in turn can lead to a loss of inductance. Therefore a core material with low permeability and low core losses at the switching frequency, such as gapped ferrite, powdered iron, or MPP should be chosen. The vendor can help calculate the core losses for a particular design.

The conduction losses in the inductor are

$$P_{d_{L_cond}} = I_{L_RMS}^2 \times R_L \quad (26)$$

MOSFET Selection

MOSFET selection focuses primarily on breakdown voltage and power dissipation. A MOSFET with a breakdown voltage of about 1.5 times the output voltage is preferable. Once the converter is running, the designer should ensure that all drain voltage spikes are well below this value.

Power dissipation in the switch is composed of three elements—conduction loss, switching loss, and gate loss. The conduction losses in the MOSFET are approximated as

$$P_{d_{SW_cond}} = I_{SW_RMS}^2 \times R_{DS(ON)}. \quad (27)$$

The switching losses are approximated as shown by Equation (28) below are comprised of the losses incurred in driving the node capacitance (MOSFET C_{oss} and the rectifier capacitance or Q_{rr}) and the device itself. The gate losses are approximated as

$$P_{d_{SW_gate}} = Q_{GATE} \times V_{GATE} \times F_s. \quad (29)$$

An $R_{DS(ON)}$ should be selected for the MOSFET so that the conduction power dissipation is limited to 1% or so of the total output power. With this selection, the maximum allowable drain current of the MOSFET will be much greater than what will occur in the application. A MOSFET with low capacitance will minimize switching losses. A good rule of thumb is to select a MOSFET with switching losses equal to conduction losses with the converter operating at maximum load. Obviously, selecting a MOSFET to meet these criteria is a somewhat iterative endeavor.

Diode Rectifier Selection

The rectifier must be capable of handling the capacitor's peak input current and of dissipating the rectifier's average power—the rectifier voltage drop times the load current. The voltage breakdown of the device must be greater than the output voltage plus some margin. The typical choice for a rectifier in applications with low output voltage is a low-capacitance Schottky diode. If the output

voltage is high, a fast-recovery diode is an alternate possibility. For converters operating in CCM, a diode with a “soft” recovery characteristic will minimize EMI and the need for a snubber. This characteristic is not necessary in a DCM application because there is no current flowing in the diode when the switch is turned on.

A simple approximation of conduction losses in the diode is

$$P_{d_{RECT_cond}} = I_{OUT} \times V_d. \quad (30)$$

Switching losses associated with a Schottky rectifier are dissipated by the switch. In this case, the results of Equation (31) are added to those of Equation (28).

$$P_{d_{SW_SCH}} = \frac{1}{2} \times C_{RECT} \times \frac{(V_{OUT} + V_d)^2}{2T_s}, \quad (31)$$

and for a fast-recovery device, as shown by

$$P_{d_{RECT_Qrr}} = \frac{V_{OUT} \times t_{rr} \times I_{OFFSET}}{2T_s}. \quad (32)$$

Synchronous Rectification

If the $R_{DS(ON)}$ is low and the output current is high, a MOSFET may replace the diode. The benefits of the increased efficiency must be weighed against the additional complexity of driving the MOSFET. Using a MOSFET allows a “discontinuous” design to be run in CCM. If the gate-driver timing allows the synchronous rectifier's MOSFET to be on for the full $(1 - D)$ interval, then when the inductor current decays to zero during the OFF period, it then reverses and conducts energy back into the input. However, during such CCM operation, power dissipation increases significantly due to the recirculation of energy.

Selection of an Output Capacitor

To provide relatively smooth DC voltage to the load, the output capacitor in a boost converter must absorb pulsating ripple current. For this to occur, the impedance of the capacitor at the

$$P_{d_{SW_switch}} = \frac{1}{2T_s} \times \left[C_{OSS} \times (V_{OUT} + V_d)^2 + (V_{OUT} + V_d) \times \frac{I_{OUT}}{1-D} \times \frac{Q_{GD} \times R_{GATE}}{V_{GATE} - V_{th}} \right] \quad (28)$$

switching frequency and the ESR of the capacitor must be low enough to keep the ripple voltage across the capacitor very small as compared to the average output voltage (see Fig. 22).

The output capacitor should be chosen for its holdup (if necessary) and filtering performance and, more important, its RMS ripple-current rating. The power dissipation in the capacitor can be significant if the ESR is high in a high-ripple-current DCM converter. To find the power dissipated in the capacitor, first find the ripple current into the capacitor and the capacitor's ESR. Assuming a steady-state load current, the voltage drop created by the capacitance is

$$V_{\text{RIPPLE_CAP}} = \frac{I_{\text{OUT}} \times D \times T_s}{C_{\text{OUT}}} \quad (33)$$

The peak-to-peak voltage drop created by the ESR is

$$V_{\text{RIPPLE_ESR(PP)}} = R_{\text{ESR}} \times (I_{\text{OFFSET}} + \Delta I_L) \quad (34)$$

The capacitor ripple current is shown by Equation (35) below and the power dissipation in the capacitor is then

$$P_{\text{dCAP}} = I_{\text{CAP_RMS}}^2 \times R_{\text{ESR}} \quad (36)$$

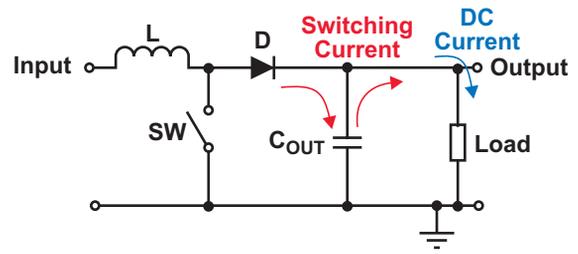


Fig. 22. Capacitor current flow.

Current Limiting and Inrush Current

An inspection of the schematic for a simple boost converter makes it clear that upon instantaneous start-up there will be a large surge current charging the output capacitor. The peak of the current is dependent on the rate of rise of the input voltage, the inductance, the capacitance, and the circuit resistance. In practice, inductor saturation is not generally a problem when the sourcing converter has a soft start of some sort, limiting the rate of rise of the voltage. For those applications where a switch is in series with the input of the boost converter, an inrush-limiting circuit such as an NTC thermistor or a resistor shunted by a switch is in series with the inductor. Alternatively, a rugged diode placed in parallel with the series connection of the inductor and diode shunts most of the inrush current from the inductor.

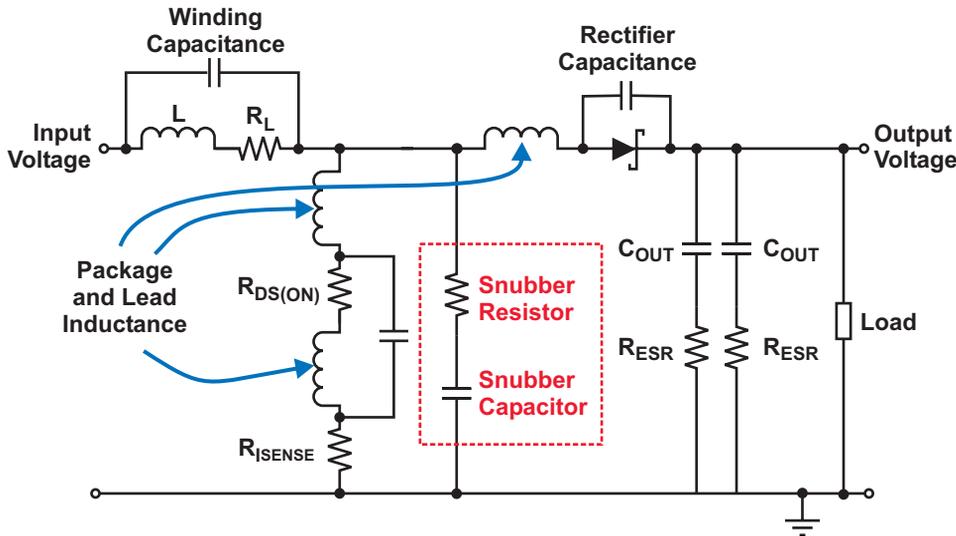


Fig. 23. Boost power stage with parasitic elements.

Controlling Switch-Node Ringing

Parasitic components, such as inductor shunt capacitance and lead-wire inductance in the MOSFET and diode (see Fig. 23), can cause ringing at the switch node in excess of 100 MHz. Damage to the MOSFET may occur if the voltage spikes created by this ringing exceed the MOSFET's voltage rating.

$$I_{\text{CAP_RMS}} = \sqrt{I_{\text{OUT}}^2 \times D + \frac{t_{\text{fall}}}{T_s} \times (I_{\text{OFFSET}} - I_{\text{OUT}})^2 + (I_{\text{OFFSET}} - I_{\text{OUT}}) \times |\Delta I_{\text{L(OFF)}}| \times t_{\text{fall}} + \frac{(\Delta I_{\text{L(OFF)}} \times t_{\text{fall}})^2}{3}} \quad (35)$$

In addition to more power loss, conducted and radiated EMI are by-products of this ringing.

Good PCB layout practices minimize some of this ringing. The physical trace loop areas of the switch node must be as small as possible to minimize stray inductance. Tying the source of the MOSFET at the return path of the output capacitor can help, or a high-frequency capacitor can be connected from the cathode of the diode directly to the source of the MOSFET.

An additional technique is to place a small (2- to 10- Ω) resistor in series with the gate of the MOSFET. This will serve to slow the turn-on and turn-off of the MOSFET and will further reduce the ringing. However, a resistor that is too large will increase switching times and power dissipation.

Another technique is to add a series R-C snubber across the MOSFET to dampen the

parasitic energy. The snubber capacitor controls the maximum peak voltage at the switch node:

$$C = \frac{I_{C(PK)} \times t_r}{V_{\max}} \quad (37)$$

The snubber resistor ensures that the capacitor is discharged when the switch is turned on.

$$R = \frac{t_{ON_min}}{3C} \quad (38)$$

The power dissipation in the resistor will be approximately

$$P_d = \frac{1}{2} C \times V^2 \times F_s. \quad (39)$$

Reference [4] contains a technique for finding the R and C values based on bench measurements of the ringing.

IV. DESIGN EXAMPLES

Two CMC application circuits utilizing the TPS40210 demonstrate a few of the principles outlined in this topic. One converter operates in CCM with a 22- μH inductor (see Fig. 24). The other operates in DCM and has a 1.0- μH inductor. Components other than those in the feedback loop are the same and were selected by using the guidelines in the previous section. See Table 1 for a comparison of the test results for both converters. A detailed design example for the CCM converter can be found in Appendix B.

With a 12-V input, 24-V output, and 1-A load, the power dissipation of the significant components highlights the difference in power loss between CCM and DCM. The losses in the MOSFET and inductor comprise most of the additional loss in the DCM converter, with a small amount of increased switching loss in the rectifier. The increased losses bring the full load efficiency down from 93% for the CCM converter to 88% for the DCM converter.

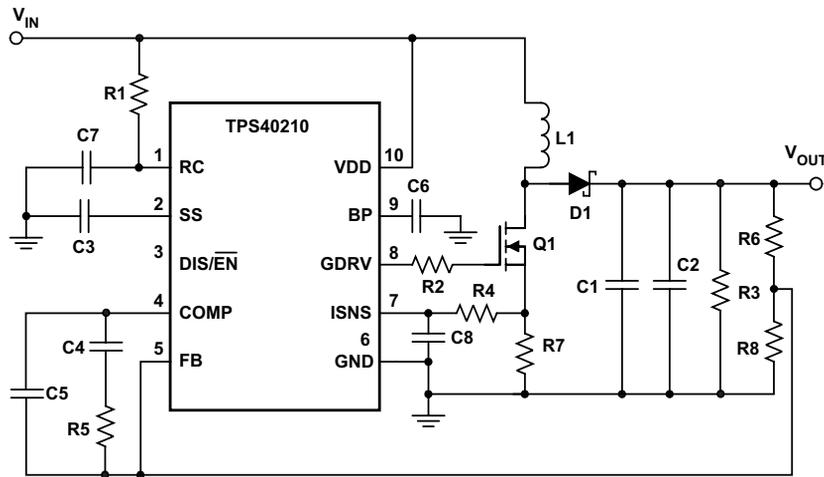


Fig. 24. Schematic of example CCM boost converter.

TABLE 1. COMPARISON OF CCM AND DCM POWER LOSSES

Device	Type	I_{PK} (A)	I_{RMS} (A)	I_{AVG} (A)	Conduction Loss (W)	AC Loss (W)	Total Loss (W)
CCM							
MOSFET Switch	0.07 Ω	2.3	1.5		0.16	0.60	1.90
Sense Resistor	0.05 Ω		1.5		0.11		
Inductor	22 μH , 79 m Ω		2.1		0.35	0.02	
Rectifier	$V_f = 0.5 \text{ V}$, $C = 100 \text{ pF}$	2.3		1	0.50	0.01	
Output Capacitor	ESR = 140 m Ω		1			0.15	
DCM							
MOSFET Switch	0.07 Ω	6	2.2		0.34	0.96	3.15
Sense Resistor	0.017 Ω		2.2		0.08		
Inductor	1 μH , 6 m Ω		3		0.06	0.80	
Rectifier	$V_f = 0.5 \text{ V}$, $C = 100 \text{ pF}$	6		1	0.50	0.01	
Output Capacitor	ESR = 140 m Ω		1.7			0.40	

Fig. 25 shows the control-to-output gain and phase plot for the CCM converter to compensate the feedback loop, a pole was selected at about 200 Hz, and a zero at about 11 kHz. The error-amplifier compensation network has a zero at about 200 Hz and a pole at about 10 kHz, resulting in a response of a straight line. The crossover frequency is about 6 kHz, with a phase margin of 75° .

Compensation of the DCM version of this converter is achieved in a similar fashion (see Fig. 26). The poles and zeros are selected at the same location as for the CCM converter, but this time the gain is increased by about 10 dB to compensate for the lower control-to-output gain. The result is a closed-loop plot similar to that of the CCM converter but without the phase lag at higher frequency. Clearly, this loop may be optimized further.

Step 11 in Appendix B details how to find the values of R5, C4 and C5. With $R5 = 150 \text{ k}\Omega$, $C4 = 5600 \text{ pF}$, and $C5 = 180 \text{ pF}$, the closed-loop crossover frequency is again about 6 kHz, with a phase margin of 75° . In this case, the gain may be pushed out further since there is little risk of running out of phase margin at higher frequency.

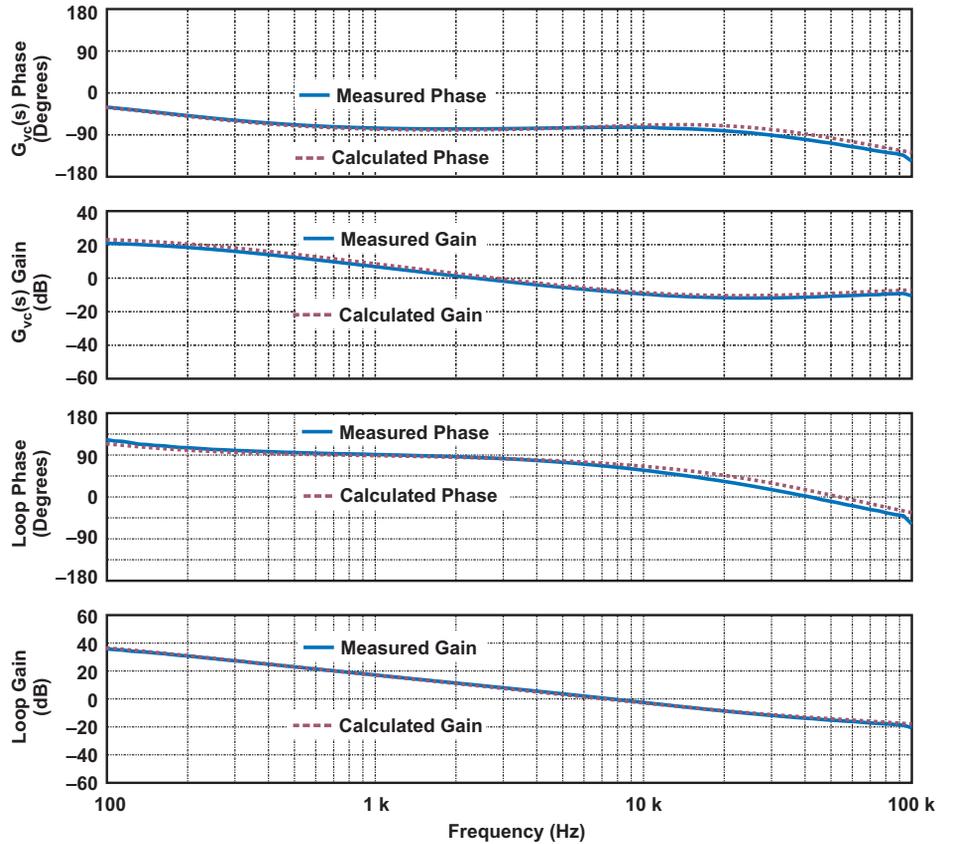


Fig. 25. CCM loop plots.

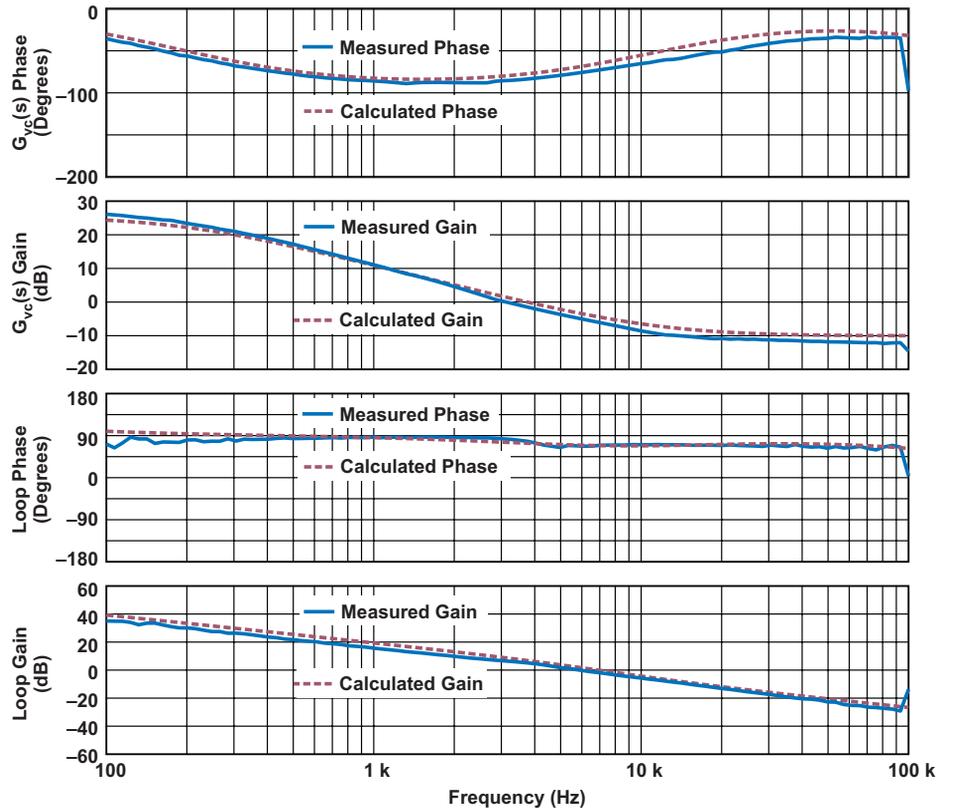


Fig. 26. DCM loop plots.

V. CONCLUSION

There are a variety of ways to design a boost converter and a variety of control techniques to stabilize it. The choice of operating in CCM or DCM has a direct impact on power-stage efficiency and loop crossover frequency. Operating in DCM generally will result in a higher loop bandwidth at the expense of lower efficiency. The DCM converter will likely be smaller due to the smaller inductor, but the demands on the output capacitor's ability to handle ripple current are higher.

Employing peak-CMC allows some correction of the double-pole rolloff found in VMC. Further, including slope compensation minimizes the possibility for subharmonic oscillation during CCM operation. Operating a DCM converter with CMC has the same effect as operating it with VMC—increased loop bandwidth with better phase margin at the expense of higher power dissipation.

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**APPENDIX A. CALCULATION OF RMS AND AVERAGE VALUES
FOR COMMON SWITCHING WAVEFORMS**

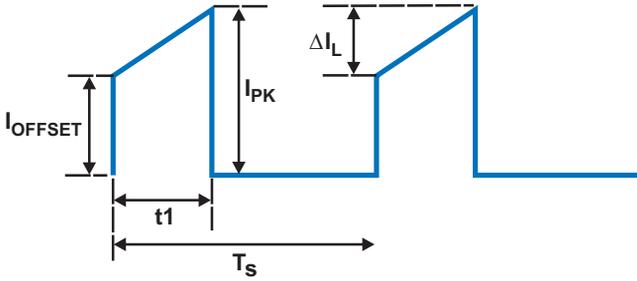


Fig. 27. Switch current in boost converter.

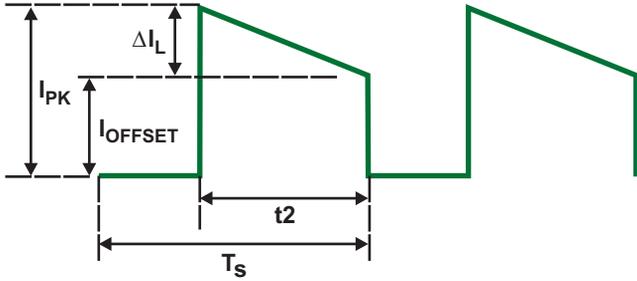


Fig. 28. Rectifier switch current.

One of the most common waveforms in a switching power supply is the stepped sawtooth. Fig. 27 shows the switch current in the boost converter.

Pedestal I_{OFFSET} is the level from which the current begins to rise at the start of a switching cycle. The level corresponds to the average input current, less one-half the peak current value:

$$I_{\text{OFFSET}} = \frac{I_{\text{out}}}{1-D} - \frac{|\Delta I_L|}{2}$$

The RMS switch current is

$$I_{\text{RMS}} = \sqrt{\left(I_{\text{OFFSET}}^2 + I_{\text{OFFSET}} \times \Delta I_L + \frac{\Delta I_L^2}{3} \right)} \times \frac{t1}{T_s}$$

The average value is

$$I_{\text{AVG}} = \left(I_{\text{OFFSET}} + \frac{\Delta I_L}{2} \right) \times \frac{t1}{T_s}$$

In the case of DCM operation, I_{OFFSET} goes to zero, and the calculations simplify to

$$I_{\text{RMS}} = I_{\text{PK}} \times \sqrt{\frac{t1/T_s}{3}}$$

and

$$I_{\text{AVG}} = I_{\text{PK}} \times \frac{t1/T_s}{2}$$

In the rectifier, similar calculations hold true (see Fig. 28).

In CCM,

$$I_{\text{RMS}} = \sqrt{\left(I_{\text{OFFSET}}^2 + I_{\text{OFFSET}} \times \Delta I_L + \frac{\Delta I_L^2}{3} \right)} \times \frac{t2}{T_s}$$

and

$$I_{\text{AVG}} = \left(I_{\text{OFFSET}} + \frac{\Delta I_L}{2} \right) \times \frac{t2}{T_s}$$

In DCM,

$$I_{\text{RMS}} = I_{\text{PK}} \times \sqrt{\frac{t2/T_s}{3}}$$

and

$$I_{\text{AVG}} = I_{\text{PK}} \times \frac{t2/T_s}{2}$$

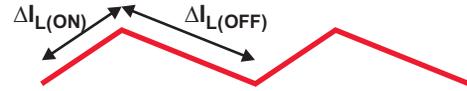


Fig. 29. Inductor current.

The average and RMS values of the inductor current are calculated from the switch and rectifier currents.

$$I_{L_AVG} = \left(\frac{\Delta I_L(\text{ON})}{2} + I_{\text{OFFSET}} \right) + I_{\text{RECT_AVG}}$$

$$I_{L_RMS} = \sqrt{I_{\text{SW_RMS}}^2 + I_{\text{RECT_RMS}}^2}$$

For CCM cases, an alternative is

$$I_{L_AVG} = \frac{I_{\text{OUT}}}{1-D}$$

APPENDIX B. DETAILED DESIGN EXAMPLE OF CCM CONVERTER

For this example, the boost converter has a 9- to 18-V input and 24-V output and is operating in CCM with CMC (see Fig. 30). The output current is 1 A, and the controller is a TPS40210 operating at about 700 kHz. With the operating mode and control technique established, the remaining design tasks are straightforward.

1. The value of L is calculated to achieve CCM operation over the operating range of the input and load. The ideal duty cycle from Equation (4), is

$$D_{\text{CCM(ideal)}} = 1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}} = 1 - \frac{12}{24} = 0.5.$$

Desiring CCM operation with at least a 10% load, we can calculate the value of L using Equation (11):

$$L = \frac{V_{\text{IN}} \times T_s}{2I_{\text{OUT_DCM}}} \times D_{\text{CCM}} \times (1 - D_{\text{CCM}})$$

$$= \frac{12 \times 1.43 \mu\text{s}}{2 \times 0.1} \times 0.5 \times (1 - 0.5) \approx 22 \mu\text{H}$$

2. Next we select components for the switch, rectifier, inductor, sense resistor and the output capacitor. Given the input and output parameters, we can then determine approximate current in each component.

The peak-to-peak ripple current (ΔI_L in Appendix A) is found from Equation (1) times the ON time of the switch:

$$\Delta I_{L(\text{ON})} = \frac{V_{\text{IN}}}{L} \times D \times T_s$$

$$= \frac{12}{22 \mu\text{H}} \times 0.5 \times 1.43 \mu\text{s} \approx 0.39 \text{ A.}$$

The pedestal of the current is approximated by

$$I_{\text{OFFSET}} = \frac{I_{\text{out}}}{1 - D} - \frac{\Delta I_L}{2}$$

$$= \frac{1}{1 - 0.5} - \frac{0.39}{2} \approx 1.8 \text{ A.}$$

The peak-to-peak current is

$$I_{\text{SW(PK)}} = I_{\text{OFFSET}} + \frac{\Delta I_{L(\text{ON})}}{2} \approx 2.2 \text{ A,}$$

and the RMS current is

$$I_{\text{RMS}} = \sqrt{\left(I_{\text{OFFSET}}^2 + I_{\text{OFFSET}} \times \Delta I_L + \frac{\Delta I_L^2}{3} \right) \times \frac{t_1}{T_s}}$$

$$= \sqrt{\left(3.61 + 1.9 \times 0.39 + \frac{0.152}{3} \right) \times 0.5} \approx 1.5 \text{ A.}$$

For conduction losses to be (arbitrarily) 1% of the total losses, a

$$R_{\text{DS(ON)}} = \frac{P_{\text{out}} \times 0.01}{I_{\text{RMS}}^2} = \frac{24 \times 0.01}{2.25} \approx 100 \text{ m}\Omega.$$

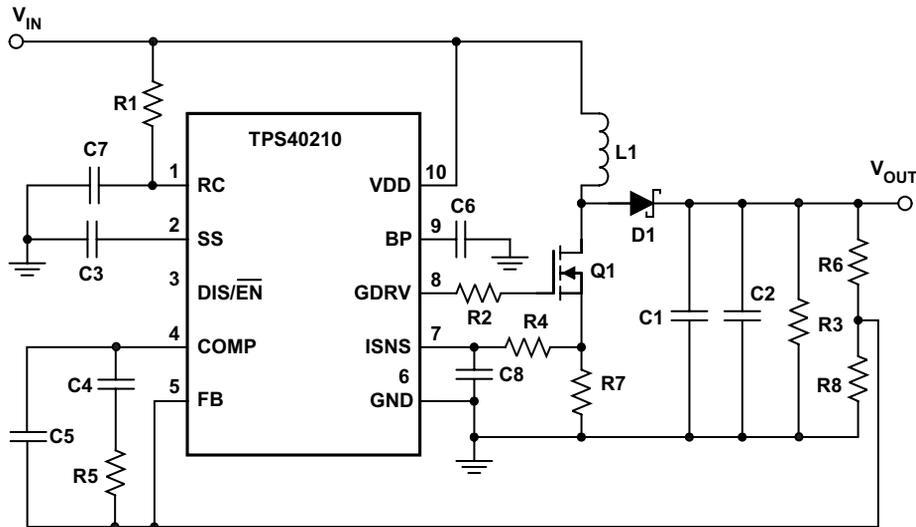


Fig. 30. Schematic for CCM converter.

The MOSFET should have a maximum voltage rating of at least 24 V. For this converter, an Si4446DY has a maximum $R_{DS(ON)}$ of 72 m Ω with a typical value of 43 m Ω , and a breakdown voltage rating of 40 V.

For the rectifier, the average rectifier current will be the same as the load current: 1 A. An MBR340 has 3-A capability and a breakdown voltage of 40 V.

The inductor is a Pulse P1169.273NL. This device has a 20- μ H inductance at 2.4 A and 27- μ H inductance at 0 A.

To suppress the tendency towards subharmonic oscillation, the current-sense resistor is selected so that the slope of the current signal (at the input of the PWM) is half that of the compensating ramp. Refer to the TSP40210 datasheet [4] for further detail.

The slope of the compensating ramp is the peak-to-peak value of the sawtooth waveform divided by the period of oscillation:

$$m_a = \frac{0.6}{1.43 \mu\text{s}} \approx 420 \text{ V/ms}$$

The sense-resistor value is

$$\begin{aligned} R_{ISENSE} &= \frac{m_a}{\Delta I_{L(OFF)} \times A_{CS} \times 2} \\ &= \frac{420 \times 1 \text{ k}}{545 \times 1 \text{ k} \times 6 \times 2} \approx 64 \text{ m}\Omega. \end{aligned}$$

A 50-m Ω resistor is used.

The remaining component in the power stage is the output capacitor. From earlier, the peak-to-peak ripple current was determined to be 2.2 A.

For a 2% peak-to-peak ripple voltage, a capacitor with an ESR of less than 218 m Ω should be used. In this example, a Panasonic 100- μ F FK series capacitor is used. The ESR for this capacitor is measured to be about 140 m Ω .

Using Equation (35), the RMS ripple current in the capacitor is about 1 A. The rating of the capacitor is just under 400 mA at 105°C. Although dissipation is low, about 140 mW, a more robust solution should be found for a production converter.

3. With the major components selected, calculate the CCM duty cycle, D_{CCM} , from Equation (5) as shown at bottom of this page, this time including losses.

Note: If the converter was operating in DCM, this is where the DCM duty cycle would be calculated using Equation (10) for use in subsequent calculations.

4. For CCM, peak CMC operation, we calculate the slope of the current in the switch during the ON interval. Equation (1) is modified to include the voltage drop across the loss elements of the MOSFET and the current-sense resistor:

$$\begin{aligned} m_{I_{L(ON)}} &= \frac{V_{IN} - \frac{I_{OUT}}{1-D} \times (R_{ISENSE} + R_{DS(ON)})}{L} \\ &= \frac{12 - \frac{1}{1-0.52} \times (0.05 + 0.07)}{22 \mu\text{H}} \approx 529 \text{ A/ms} \end{aligned}$$

$$D_{CCM} = 1 - \frac{\left\{ \frac{V_{IN} + I_{OUT} \times (R_{DS(ON)} + R_{ISENSE})}{+\sqrt{[V_{IN} + I_{OUT} \times (R_{DS(ON)} + R_{ISENSE})]^2 - 4I_{OUT} \times (R_{DS(ON)} + R_{ISENSE}) \times (V_{OUT} + V_d)}} \right\}}{2(V_{OUT} + V_d)}$$

$$D_{CCM} = 1 - \frac{\left\{ \frac{12 + 1 \times (0.07 + 0.05)}{+\sqrt{[12 + 1 \times (0.07 + 0.05)]^2 - 4 \times 1 \times (0.07 + 0.05) \times (24 + 0.5)}} \right\}}{2 \times (24 + 0.5)} \approx 52\%$$

5. From Equation (25), calculate the modulator gain, F_m :

$$F_m = \frac{1}{(m_a + m_n) \times T_s} = \frac{1}{(417000 + 529000 \times 6 \times 0.05) \times 1.43 \mu s} = 1.2$$

Notice that m_n from Equation (21) is the inductor-current ON slope times the sense resistor amplified by the current-sense amplifier gain, A_{CS} , of 6.

6. The conversion ratio from Equation (16) is

$$M_{CCM} = \frac{1}{1-D} = \frac{1}{1-0.52} \approx 2.1.$$

7. To find $G_{vd}(s)$, the duty-cycle to output-voltage transfer function, the frequency dependent parameters, Z_{ON} and Z_{OFF} must first be calculated.[§] Solving Equation (15):

$$G_{vd_CCM}(s) = V_{IN} \times M_{CCM}^2 \times \frac{1 - \frac{Z_{ON} \times M_{CCM}^2}{R_{load}}}{1 + \frac{Z_{ON} \times M_{CCM}^2}{Z_{OFF}}} = 12 \times 4.34 \times \frac{1 - \frac{Z_{ON} \times 4.34}{24}}{1 + \frac{Z_{ON} \times 4.34}{Z_{OFF}}}$$

8. The inner current-loop transfer function, $T_I(s)$, is determined from Equation (23) as shown at the bottom of this page:

9. We can use Equation (24) to plot the control-to-output transfer function, $G_{vc}(s)$ (see Fig. 31):

$$G_{vc}(s) = \frac{F_m \times G_{vd}(s)}{1 + T_I(s)} \times e^{-s \times t_d}$$

The plots in Fig. 31 indicate the calculated and measured control-to-output gain and phase of the control-to-output transfer function of the evaluation circuit as a function of frequency.

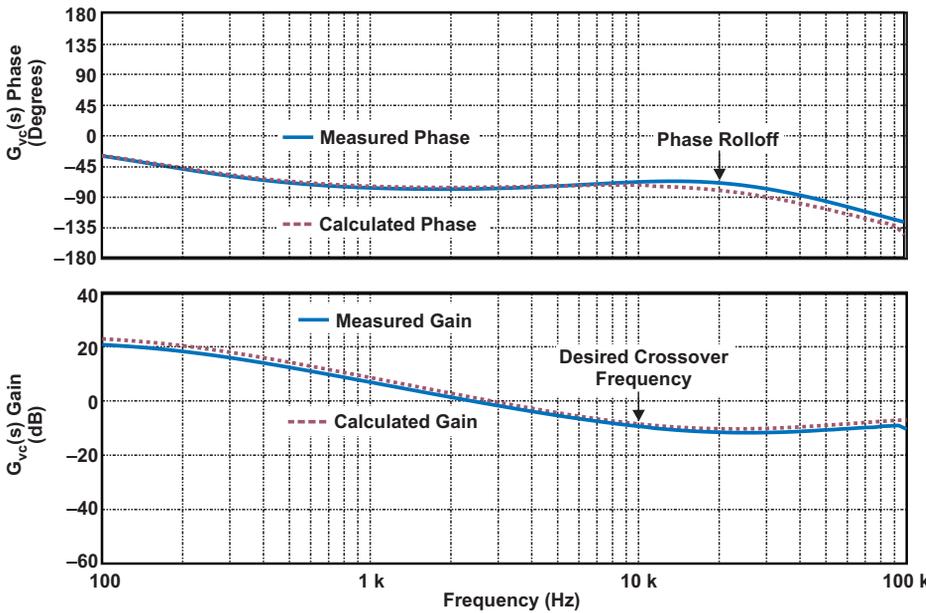


Fig. 31 Control-to-output frequency-response curves of CCM converter.

$$T_I(s) = F_m \times 2I_{OUT} \times M_{CCM}^2 \times \frac{1 + \frac{R_{load}}{2Z_C}}{1 + \frac{Z_{ON} \times M_{CCM}^2}{Z_{OFF}}} \times R_{ISENSE} \times A_{CS} \times H_e(s)$$

$$= 1.2 \times 2 \times 1 \times 4.34 \times \frac{1 + \frac{24}{2Z_C}}{1 + \frac{Z_{ON} \times 4.34}{Z_{OFF}}} \times 0.05 \times 6 \times \frac{2\pi f \times 1.43 \mu}{e^{2\pi f \times 1.43 \mu} - 1}$$

[§]It is left to the reader to calculate the impedances Z_{ON} and Z_{OFF} as a function of frequency. Refer to Fig. 9 and Equations (13) and (14).

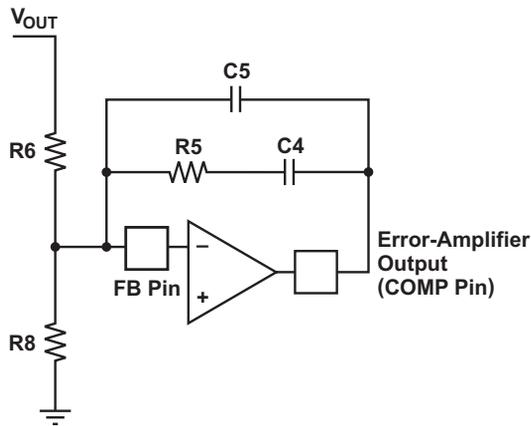


Fig. 32. Error amplifier with type II compensation.

10. Find the poles and zeros of the circuit. There is a pole at about 200 Hz, and a zero at about 11 kHz. The error-amplifier compensation network should then have a zero at about 200 Hz and a pole at about 11 kHz. The resulting desired response will be a straight line with a -20 -dB/decade slope.

11. Referring to the Bode plot, the phase begins to roll off at about 20 kHz. The loop crossover frequency should then be below 10 kHz to give some margin of safety. The error-amplifier gain therefore needs to be about $+9$ dB to bring the gain curve to 0 dB in the region of 10 kHz at the nominal 12-V input.

The voltage divider, R6 and R8 in this example, determines the output voltage. Arbitrarily setting R8 to 1.5 k Ω , the remaining components to find

are R6, R5, C4, and C5 (see Fig. 32).

$$R6 = \frac{V_{OUT}}{V_{REF}} \times R8 = \frac{24}{0.7} \times 1500 \approx 49.9 \text{ k}\Omega,$$

$$R5 = R6 \times 10^{\frac{A_{V_CA}}{20}} = 49.9 \text{ k}\Omega \times 10^{\frac{9}{20}} \approx 138 \text{ k}\Omega,$$

where A_{V_CA} is the desired gain (9 dB) of the compensated amplifier at the crossover frequency. To set the zero at about 200 Hz,

$$C4 = \frac{1}{2\pi f_{z_EA} \times R5} = \frac{1}{2\pi \times 200 \times 138 \text{ k}\Omega} \approx 5.8 \text{ nF},$$

and to set the pole at about 11 kHz,

$$C5 = \frac{1}{2\pi f_{p_CA} \times \left(R5 + \frac{1}{2\pi f_{p_CA} \times C4} \right)} = \frac{1}{2\pi \times 11000 \times \left(138 \text{ k}\Omega + \frac{1}{2\pi \times 11000 \times 5.8 \text{ nF}} \right)} \approx 100 \text{ pF}.$$

The calculation for R5 assumes that the C4 impedance at the desired crossover frequency is small compared to R5. If not, then the overall gain is greater than originally desired. Also, if the impedance of C5 at the crossover frequency is near the value of R5, the compensated amplifier gain will be lower than calculated. After some iteration of values, Fig. 33 shows a gain/phase plot with R5 = 138 k Ω , C4 = 5800 pF, and C5 = 100 pF.

The crossover frequency, which is about 6 kHz with a phase margin of 75° , is lower than originally desired. As mentioned, the gain is also lower than originally desired due to the process of selecting R5, C4, and C5.

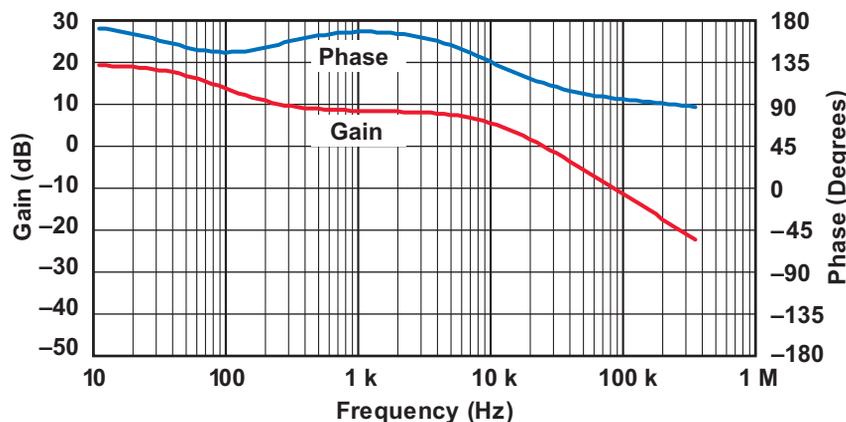


Fig. 33. Error-amplifier gain/phase plot.

The measured and predicted results compare fairly well (see Fig. 25). The low-frequency differences are accounted for by the omission of losses in the M_{CCM} conversion-ratio calculation on page 3-23. The high-frequency differences likely result from the parasitic elements of the output capacitor being different than those assumed.

APPENDIX C. GLOSSARY OF TERMS

A_{CS}	Gain of the current sense signal path	$G_{vd_DCM}(s)$	Voltage-loop duty-cycle to output-voltage transfer function in DCM
A_{V_CA}	Voltage gain of a compensated error amplifier at the desired crossover frequency	$G_{id}(s)$	Current-loop duty-cycle to current transfer function
C_{OSS}	MOSFET capacitance	$G_{id_CCM}(s)$	Current-loop duty-cycle to output-voltage transfer function in CCM
C_{OUT}	Output capacitance		
C_{RECT}	Capacitance of Schottky rectifier	$H_e(s)$	Sampling gain
D	Converter duty cycle (generic). Equal to the ON time of the switch divided by the total period.	I_{AVG}	Average current
D_{CCM}	Duty cycle of the converter in CCM	I_{CAP_RMS}	RMS capacitor ripple current
D_{DCM}	Duty cycle of the converter in DCM	$I_{C(PK)}$	Capacitor peak current
D_{disch}	Percentage of switching period required to discharge inductor energy in DCM	$I_{L(AVG)}$	Inductor average current
$D_{CCM(ideal)}$	Ideal duty cycle	$I_{L(RMS)}$	RMS inductor current
$e^{-s \times t_d}$	Time delay in the switching path of the converter	I_{OFFSET}	The pedestal level from which the current begins to rise at the start of a switching cycle.
f_{z_CA}	Desired zero frequency of the compensation error amplifier	I_{OUT}	Output load current
f_{p_CA}	Desired pole frequency of the compensation error amplifier	$I_{OUT(AVG)}$	Average output current
F_m	Modulator gain	I_{OUT_DCM}	Level of average output current at boundary between CCM and DCM operation
F_s	Converter switching frequency	I_{PK}	Peak current
$G_{vc}(s)$	Control-to-output transfer function	$I_{RECT(RMS)}$	Rectifier RMS current
$G_{vd}(s)$	Voltage-loop duty-cycle to output-voltage transfer function	I_{RMS}	RMS current
$G_{vd_CCM}(s)$	Voltage-loop duty-cycle to output-voltage transfer function in CCM	$I_{SW(RMS)}$	RMS switch current
		L	Inductor value
		m_a	Slope of artificial ramp
		m_n	Slope of the current-feedback signal during the ON time of the switch
		M_{CCM}	Converter conversion ratio in CCM
		M_{DCM}	Converter conversion ratio in DCM

APPENDIX C. GLOSSARY OF TERMS (CONTINUED)

$m_{I_L(ON)}$	Slope of the inductor current during ON time of the switch	t_{DISCHG}	Discharge time of sawtooth
$m_{I_L(OFF)}$	Slope of the inductor current during OFF time of the switch	t_{OFF}	Turn-OFF time
P_d	Power dissipated	t_{ON_min}	Switch ON time under minimum duty-cycle conditions
$P_{d_{CAP}}$	Power dissipated by output capacitor	$T_I(s)$	Inner current-loop transfer function
$P_{d_{L_cond}}$	Inductor winding power loss	t_r	Desired SW-node rise time
$P_{d_{RECT_cond}}$	Rectifier conduction power loss	T_s	Converter switching period
$P_{d_{RECT_FR}}$	Rectifier switching power loss	t_{fall}	Time for the inductor current to decay to zero in DCM operation
$P_{d_{RECT_Qrr}}$	Schottky rectifier switching loss	V_d	Rectifier diode forward voltage
$P_{d_{SW_cond}}$	MOSFET conduction power loss	V_f	Rectifier forward voltage
$P_{d_{SW_switch}}$	MOSFET switching power loss	V_{GATE}	MOSFET gate-drive voltage
$P_{d_{SW_gate}}$	MOSFET gate power loss	V_{IN}	Converter input voltage
P_{out}	Converter output power	V_{max}	Maximum voltage across the snubber capacitor
Q_{GD}	MOSFET gate-drain charge	V_{OUT}	Converter output voltage
Q_{GATE}	MOSFET total gate charge	V_{ramp}	Sawtooth waveform peak-to-peak voltage
$R_{DS(ON)}$	Switch ON resistance	V_{RIPPLE_CAP}	Voltage ripple across the output capacitor
R_{ESR}	Capacitor ESR	$V_{RIPPLE_ESR(PP)}$	Peak-to-peak voltage ripple across the output capacitor's ESR
R_{GATE}	MOSFET gate resistance	V_{th}	MOSFET gate-threshold voltage
R_L	Inductor winding resistance	Z_C	Parallel impedances of output capacitors
R_{load}	Converter load resistance	Z_{ON}	Total impedance of the network when the switch is on
R_{ISENSE}	Current-sense resistor	Z_{OFF}	Total impedance of the network when the switch is off
R_{tot}	Sum of DC loss elements when the switch is on		
s	Frequency in radians/s		