High-Voltage Energy Storage: The Key to Efficient Holdup

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ABSTRACT

This topic provides a tutorial on how to design a high-voltage-energy storage (HVES) system to minimize the storage capacitor bank size. The first part of the topic demonstrates the basics of energy and the benefits/limitations of HVES; it also provides volumetric analysis graphs illustrating volume reduction and energy density. The second part provides an overview of the critical aspects of an HVES design. It compares the possible topologies and control techniques, identifies the pitfalls and design challenges of the recharge and holdup modes, and discusses the impact of design decisions on power losses. Design guidelines applicable to a preselected power topology and control strategy are also provided, including a design example for a 48-V application.

I. Fundamentals of High-Voltage Energy Storage

A. Basic Principles

Many high-reliability systems have a requirement for modules to ride through short input-power interruptions. Some systems require a graceful shutdown mechanism while others need a local bank of energy to supply power during occasional and brief high-load-current demand. There are also other applications that require short-term backup power when the main power fails—for example, a security system that needs to record information for a limited time following a power interruption.

Input-power interruptions can come from a short-circuited module or from the switchover from a primary to a redundant bus when a power-bus failure occurs. Fig. 1 shows a basic energy-storage system that could maintain V_{bus} during a holdup event such as a momentary input-power interruption. Fig. 2 shows typical V_{bus} levels with and without an energy-storage system. For example, in telecommunications applications, the PICMG® AdvancedTCA® specification requires continuous operation in the presence of a 5-ms, 0-V input-voltage transient (the total duration is 9.2 ms when rise and fall times are included). The 5 ms is the time in which a fuse can blow when there is a short circuit on a module or a short-circuited module is plugged into the system. Many other similar examples can be enumerated, both for DC and AC bus voltages.

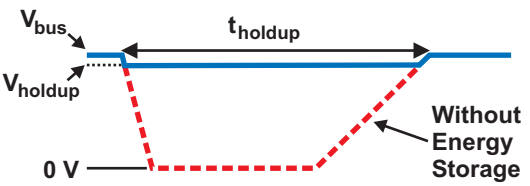

Fig. 2. Bus voltage during holdup event.

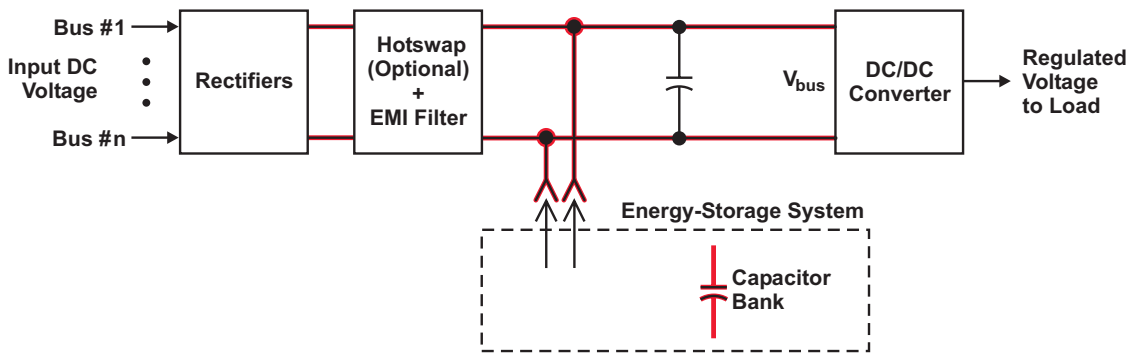

Fig. 1. Bulk-capacitors solution for energy storage.

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One way to ride through the fault is to use storage capacitors. The energy available is defined as

$$E = \frac{1}{2} C \times (V_1^2 - V_2^2), \quad (1)$$

where E is the energy in joules (J), C is the capacitance in farads (F), V_1 is the starting capacitor voltage before discharge, and V_2 is the final capacitor voltage after discharge. The greater the voltage decrease, the smaller is the capacitance required to hold up the circuit.

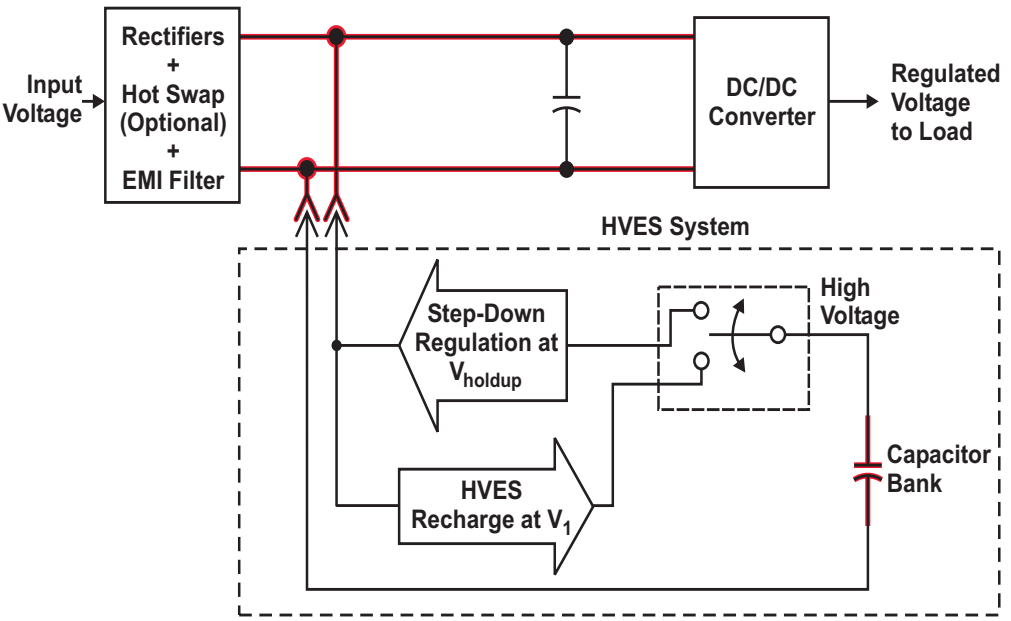


Fig. 3. HVES Solution.

In a bulk-capacitors solution (Fig. 1), energy is stored in capacitors on the power bus. This requires a large capacitance value because the allowed voltage decrease is usually a small percentage of the bus voltage.

An alternative solution, high-voltage-energy storage (HVES) stores the energy on a capacitor at a higher voltage and then transfers that energy to the power bus during the dropout (see Fig. 3). This allows a smaller capacitor to be used because a large percentage of the energy stored is used for holdup. HVES is a particularly good choice when the bus voltage has a wide range of variation (for example, a 48-V bus with 72 V maximum), already requiring high-voltage bulk capacitors; or the minimum normal bus voltage is not much higher than the minimum needed by the loads to stay in operation (for example, 44 V versus 39 V).

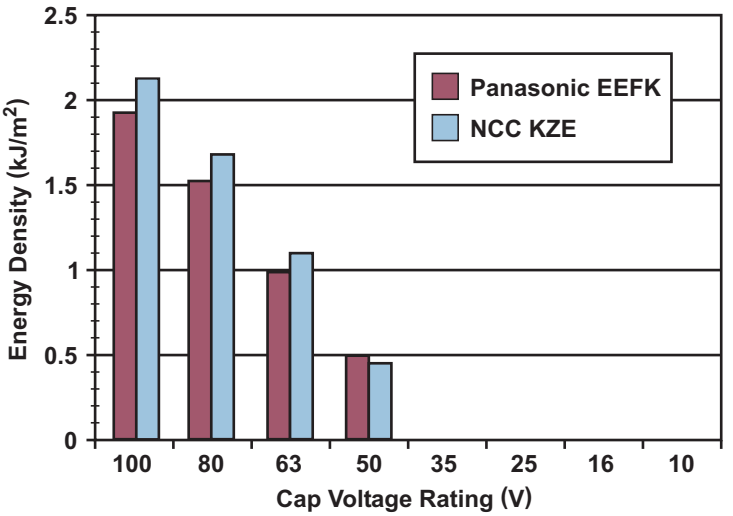


Fig. 4. PCB energy density with V_2 = 39 V and HVES solution with V_1 = 88% of capacitor rating.

B. Volumetric Design Examples

In Fig. 3 and Equation (1), the capacitor bank has initially been recharged and its voltage is V_1. V_2 represents the capacitor bank's minimum voltage required to maintain V_{holdup}, which is the regulated bus voltage during a holdup event.

If, for example, 2 J are required over a 10-ms time period, V_2 is 39 V, and V_1 is only 44 volts, then 9639 µF is required. If V_1 is increased to 88 V and the power-conversion efficiency is 91%, the required capacitance decreases to less than 706 µF, which means a reduction factor of close to 14. In both cases, some derating must be applied to the required capacitance. This includes the initial tolerance, the temperature variation, and the lifetime variation.

Figs. 4 and 5 illustrate how increasing the storage voltage reduces the PCB area, assuming

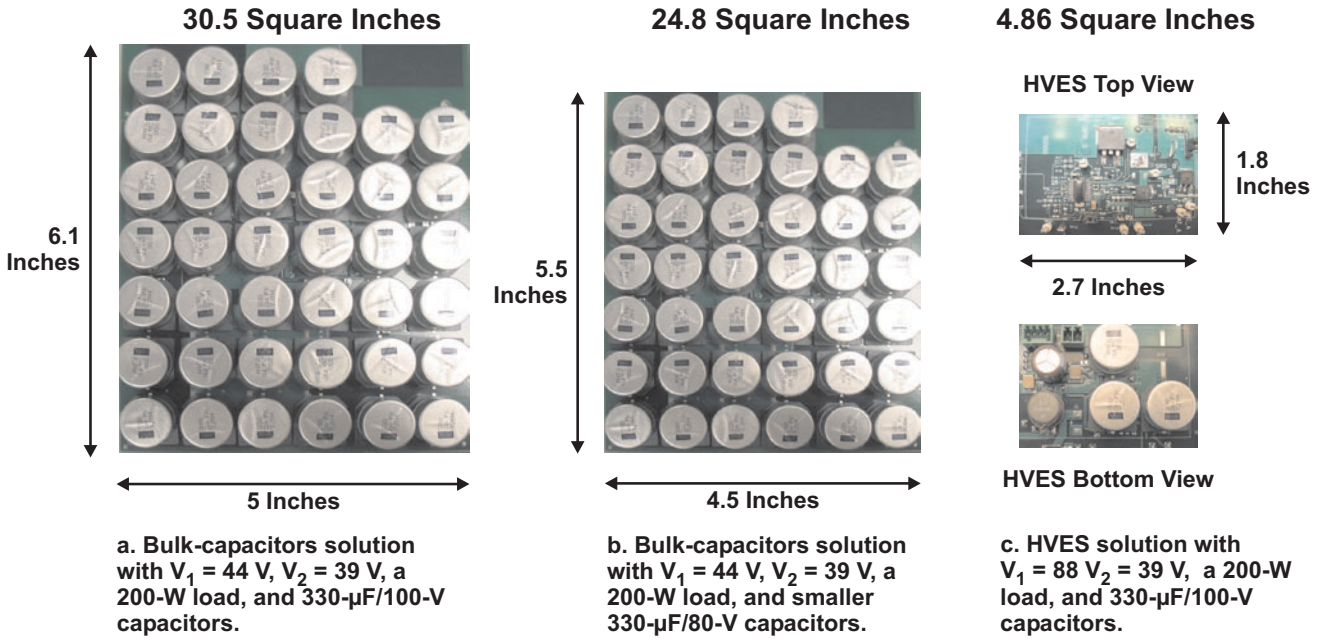


Fig. 5. PCB area with HVES solution versus bulk-capacitors solution.

that the capacitor's height is no more than 21 mm and the capacitor's final voltage (V_2) is 39 V. Capacitor types considered are the Panasonic surface-mount EEFK and the Nippon Chemi-Con (NCC) leaded through-hole KZE. The storage voltage has been arbitrarily set to 88% of the maximum capacitor voltage rating, the capacitance derating factor has been set to 74%, and the conversion efficiency has been set to 91%.

Fig. 6 illustrates the energy density achievable with a bulk-capacitors solution that uses the same final voltage and capacitor types. The starting capacitor voltage has been set to 44 V, and the capacitor voltage rating varies depending on the maximum expected bus voltage during system operation.

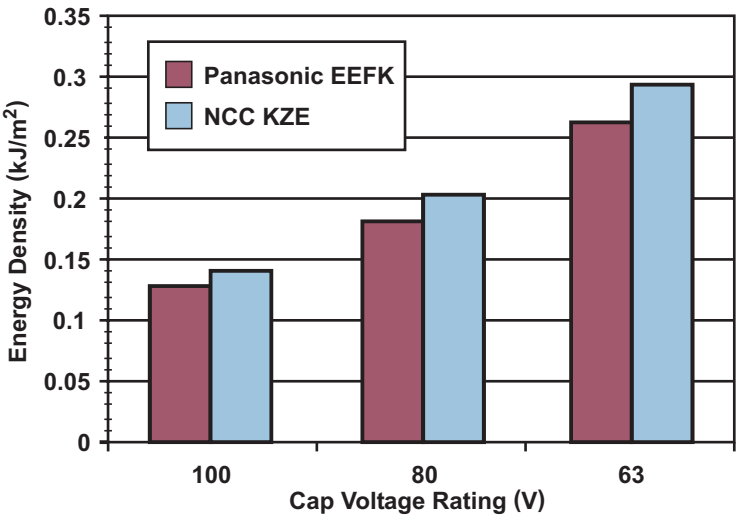


Fig. 6. PCB energy density with V_2 = 39 V and bulk-capacitors solution.

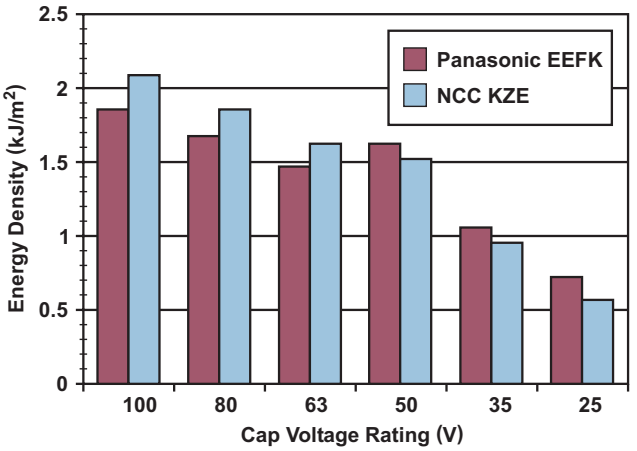


Fig. 7. PCB energy density for 12-V system and HVES solution with V_1 = 90% of capacitor rating and 70% conversion efficiency.

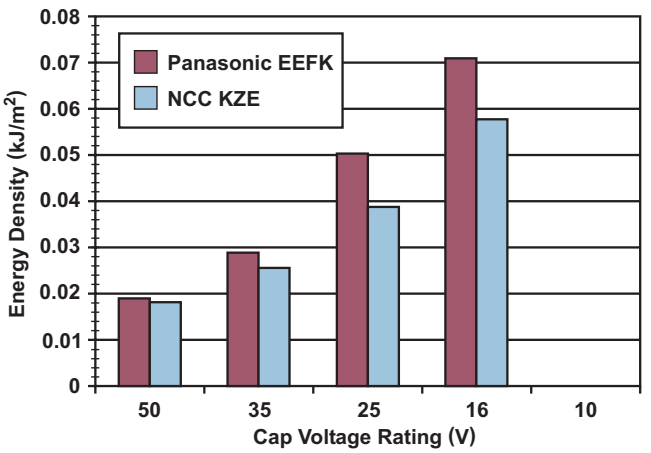


Fig. 8. PCB energy density with V_1 = 11 V, V_2 = 10 V, and bulk-capacitors solution.

Analysis results for a 12-V system having a conversion efficiency of 70% are shown in Figs. 7 and 8. It is clear that storing energy at 50 V is enough to provide a high size-reduction ratio.

II. Critical Aspects of HVES Implementation

A. General System Requirements

Basically, an HVES system must be able to:

- use the bus voltage to charge and maintain the storage capacitors to a nominal voltage,
- use the energy available in the storage capacitors to quickly maintain and regulate the internal input bus voltage during a short input-power interruption,
- automatically discharge the storage capacitors on unit removal for safety, and
- minimize the size of the storage capacitor bank.

Secondary needs include inrush-current control during initial recharge, short-circuit protection during recharge and very low power consumption when the capacitors become completely charged for minimum impact on the system. It is also highly preferable to make use of a single inductor for all modes of operation for a compact system solution. EMI requirements, thermal aspects, and total cost must also be considered.

B. Optimum Power-Bridge Configuration and Control Strategy for Bidirectional Converter

A simplified system diagram is shown in Fig. 9, which presents the HVES like a virtual capacitor. While the key to minimizing the size of the HVES unit is high-voltage storage, conversion efficiency also has some impact.

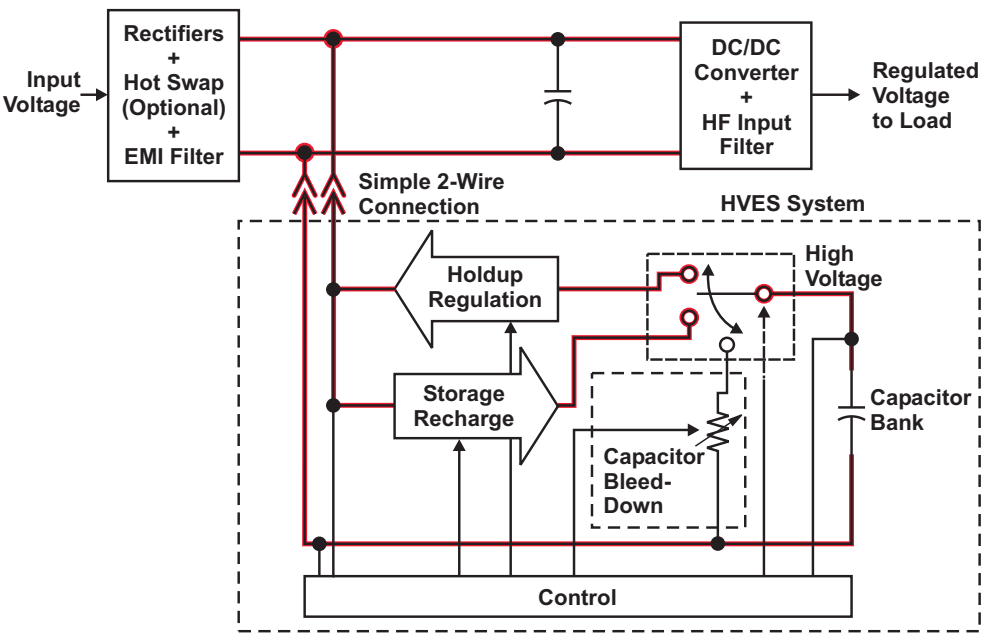


Fig. 9. Simpified HVES functional diagram.

The storage capacitor bank is connected only to the HVES power-bridge circuit. It is also normally physically located very close to this circuit, with enclosure(s) or other types of barriers that bar user access to satisfy safety concerns. These conditions remove any need for an isolation transformer during energy transfer.

The power bridge configurations considered are (1) the boost/buck, (2) the flyback/buck, and (3) the multimode buck/boost.

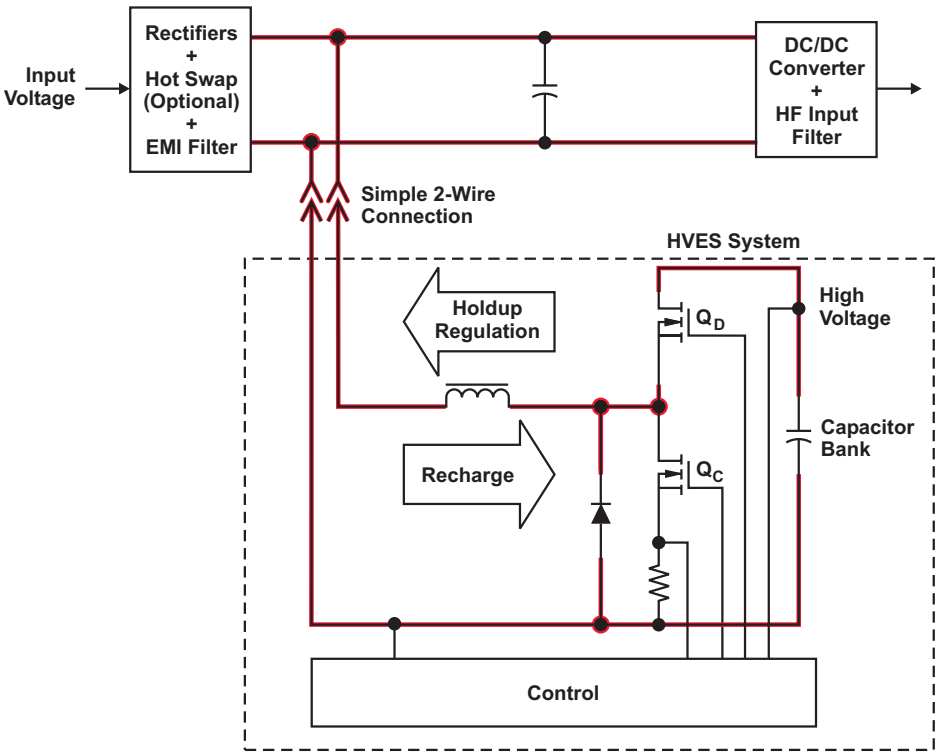
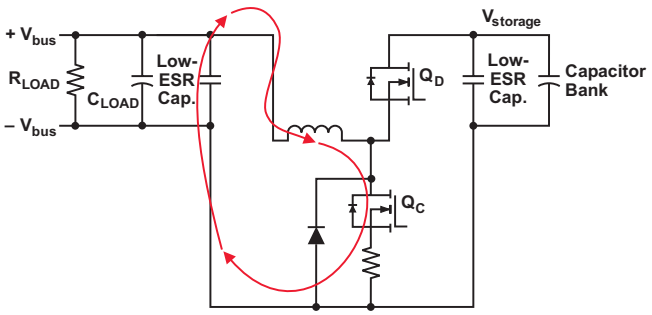


Fig. 10. Bridge configuration 1: Boost in recharge, buck in holdup.

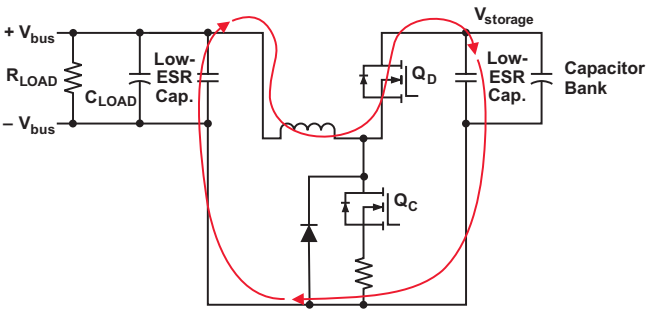
Bridge Configuration 1: Boost/Buck

This power-bridge configuration is simple, requiring only two MOSFETs and a diode with one high-side gate driver (see Fig. 10). It uses a boost topology operating in peak-current control to recharge the capacitors (see Fig. 11). The current sensing is simply done with a low-side resistor. The boost topology does not provide any inrush limiting or any protection against a short-circuit in the storage capacitor bank. This requires additional circuitry, for example a hot-swap device located upstream. Note that a hot-swap device in the main power path introduces power loss during normal operation, so that using it makes more sense if the system already needs it for bus-capacitor inrush control or load short-circuit protection. A hot-swap device operates its MOSFET in linear mode during inrush, during which it must keep the MOSFET within its safe operating area (SOA) in worst-case temperature conditions. Because of additional energy storage in the HVES capacitors, the SOA limitations result in a largely oversized hot-swap MOSFET, a very long recharge time, or even both. For these reasons, the boost/buck solution is not the preferred one.

Note that a hot-swap device could instead be inserted directly within the HVES charge/discharge path and out of the main load power



a. Q_C is on and Q_D is off.



b. Q_C and Q_D are off.

Fig. 11. Current flow in boost recharge mode.

path. The limitations, however, would remain similar; and additional complexity would be introduced, including a current-sensing element and a power parallel diode.

During holdup, a boost/buck solution uses a nonsynchronous buck topology similar to that used in a flyback/buck topology discussed next.

Bridge Configuration 2: Flyback/Buck

This configuration uses a flyback (also known as buck-boost) topology with peak-current-mode control to recharge the capacitors. Many current-sensing strategies are possible. Fig. 12 shows a low-side resistor acting as a current sensor similar to the boost/buck topology. One advantage of the flyback topology over the boost is that it provides complete inrush-current control while the storage capacitors are being recharged from 0 V (Fig. 13). This control also provides protection against capacitor short-circuits. The Q_A MOSFET is operated only in switch mode, resulting in a smaller MOSFET than would be required for a circuit that linearly limits inrush.

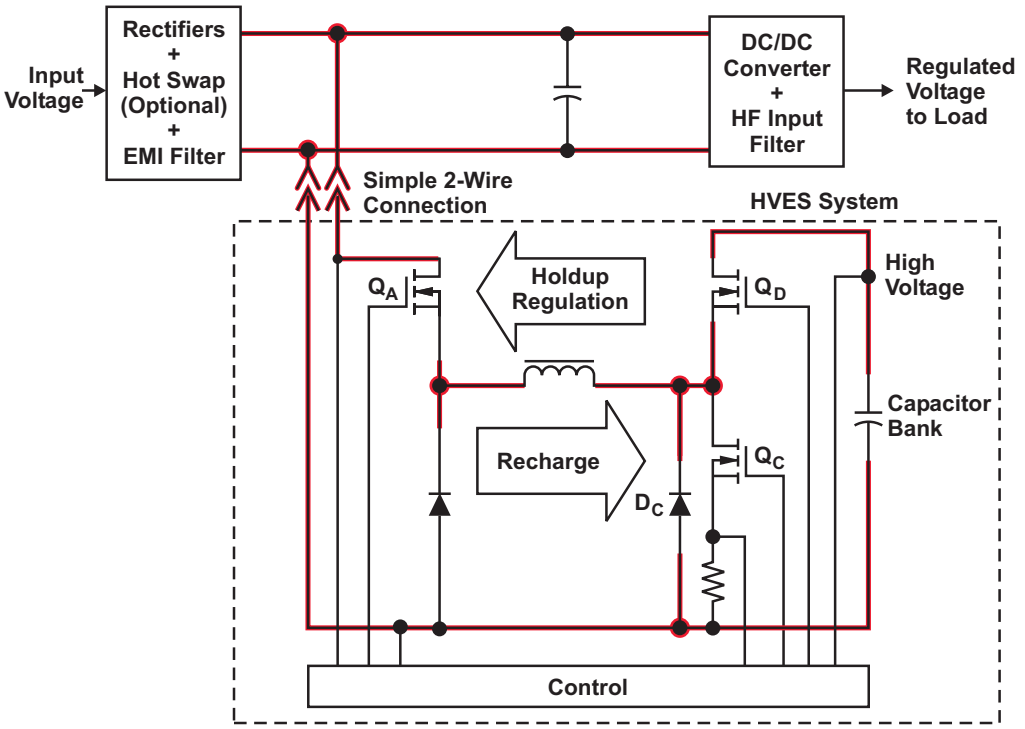
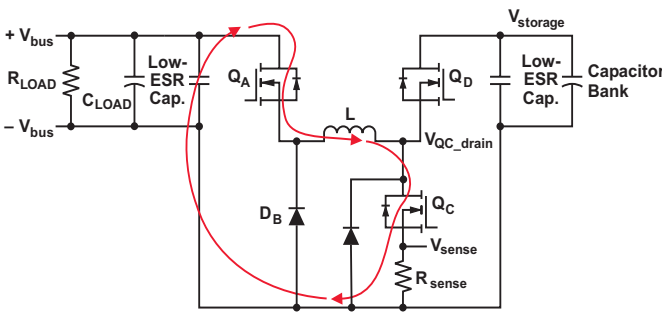
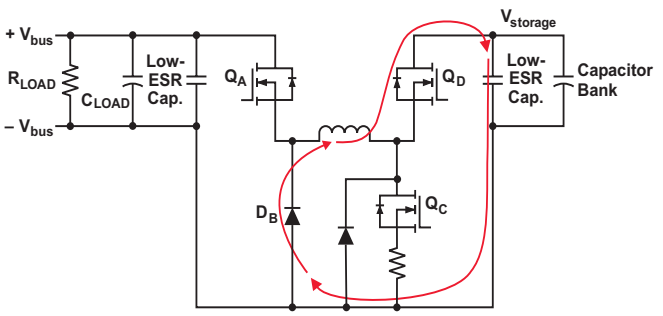


Fig. 12. Bridge configuration 2: flyback/buck.

During holdup, a buck topology with voltage-mode control is used. Voltage-mode control does not use current sensing and therefore does not need slope compensation, which would be required for current-mode control at higher duty cycles. This is particularly important in the actual application, where the storage-capacitor voltage drops down to V_{bus} during holdup, resulting in the duty cycle approaching 100%.

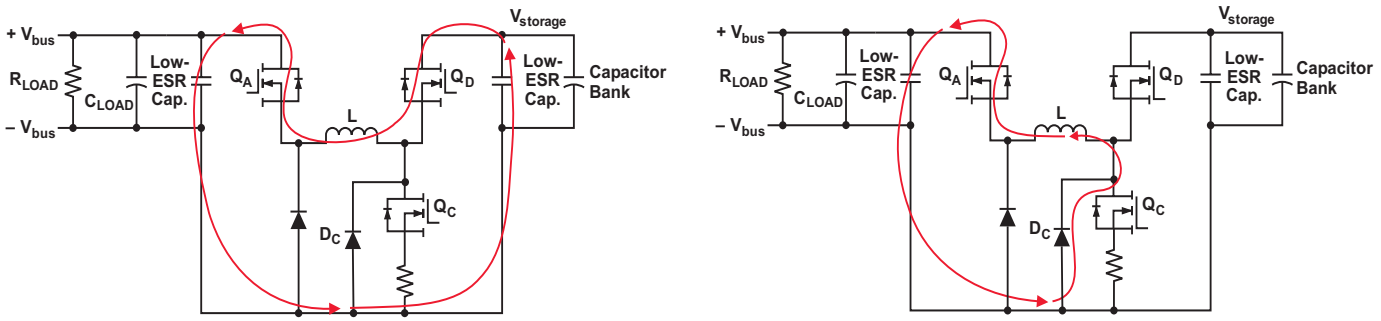


a. Q_A and Q_C are on and Q_D is off.



b. Q_A, Q_C, and Q_D are off.

Fig. 13. Current flow in flyback recharge mode.



a. Q_D is on and Q_A and Q_C are off.

b. Q_A, Q_C, and Q_D are off.

Fig. 14. Current flow in buck holdup mode.

Note that in Fig. 14, the ultrafast diode, D_C, shunts the holdup current around R_{sense} so that the recharge current can be optimized without penalizing the buck efficiency. Also note that the R_{sense} value is normally high enough to ensure that D_C is the preferred path over Q_C's body diode during holdup, providing a much lower and more predictable reverse-recovery loss.

The main drawback in using a buck topology is that if operation needs to be maintained when the storage voltage is becoming equal to the bus voltage, operation at virtual 100% duty cycle is needed, which adds some complexity to the control circuitry and the high-side gate driver of Q_D MOSFET.

Bridge Configuration 3: Multimode Buck/Boost

The third power-bridge configuration is by far the most complex. It uses a flyback topology to recharge the capacitor, but during holdup it transitions from a buck to a flyback topology and to a boost topology as the storage voltage goes down (see Figs. 15 and 16).

With this configuration during holdup mode, the converter can be run as a buck when $V_{storage}$ is greater than V_{bus} (bus voltage) and as a boost when $V_{storage}$ is less than V_{bus}. It is also run as a flyback when $V_{storage}$ is close to V_{bus}.

Analyses indicate that in many cases there is little benefit in trying to use this multimode configuration in holdup, as it results in an oversized

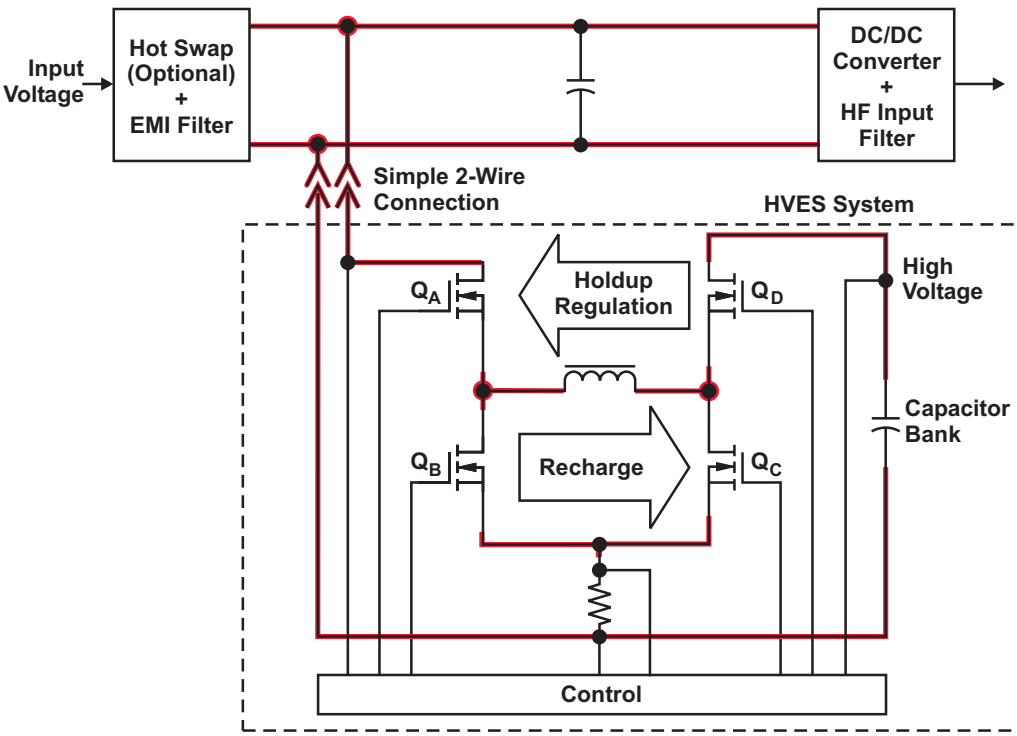
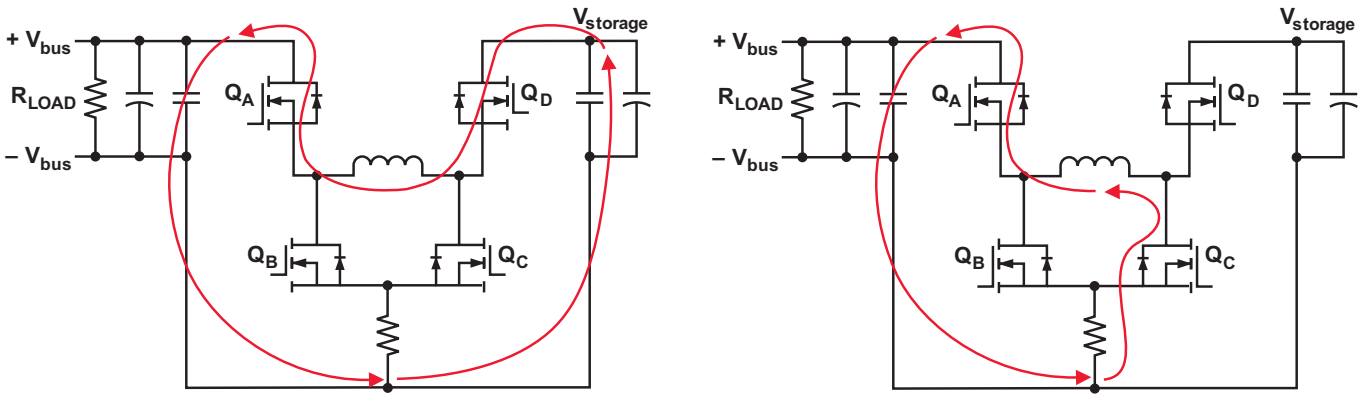
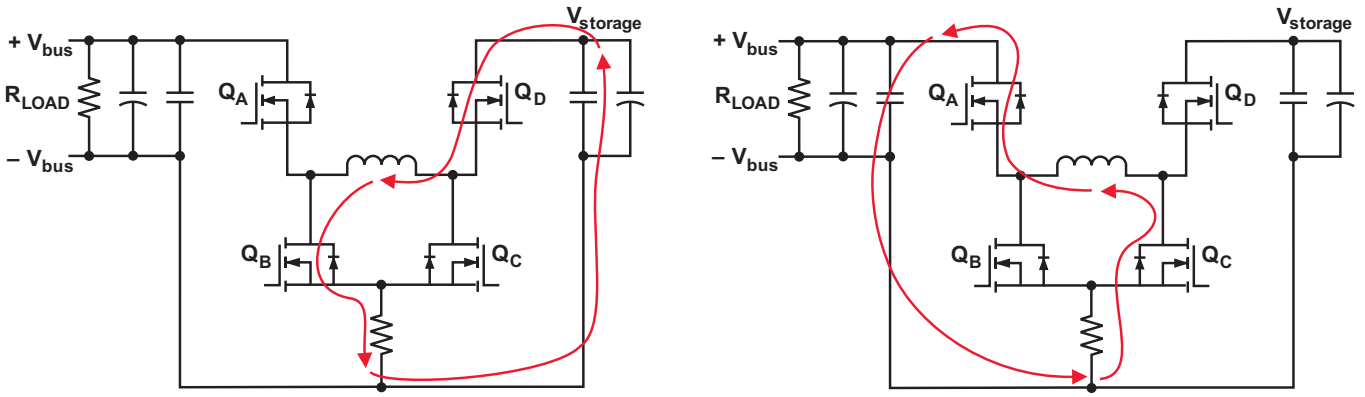


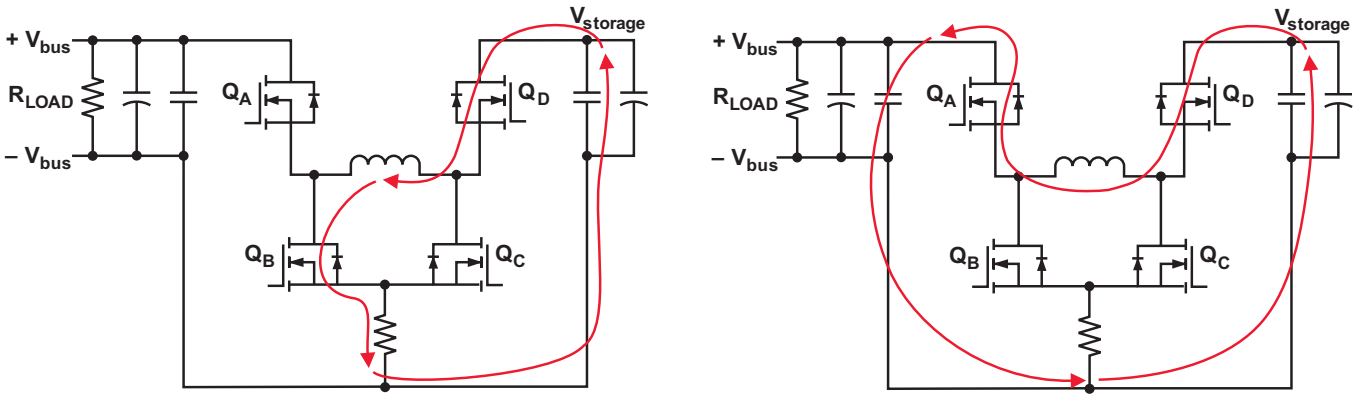
Fig. 15. Bridge configuration 3: Multimode buck/boost.



a. Buck ($V_{storage} > V_{bus}$).



b. Flyback ($V_{storage} \approx V_{bus}$).



c. Boost ($V_{storage} < V_{bus}$).

Fig. 16. Current flow in holdup with bridge configuration 3.

and much more complex power circuitry. Four power MOSFETs with gate drivers are needed, which is two more than configuration 1 and one more than configuration 2. There are additional concerns with potential body-diode reverse-recovery problems in each operating mode, for example, when MOSFET Q_B is turned on while there is already a current circulating in Q_A's body diode. Trade-off solutions exist but add losses, complexity, and/or costs. For all these reasons, switching and gate losses become higher in holdup with bridge configuration 3.

Also, the rms ripple current circulating in the output capacitor is much higher with a boost converter than with a buck converter. See Figs. 17 and 18. Consequently, a bus capacitor's equivalent series resistance (ESR) may become an issue mainly because of bus voltage ripple during

holdup, particularly if an electrolytic capacitor is used. Of secondary importance is the impact on efficiency during holdup.

The required inductance value is higher for a buck topology while the required current capability is higher with a boost topology.

An inductor designed for both modes would therefore be larger than one optimized for either mode by itself. Similar considerations apply to the MOSFETs, for example Q_D, for which the voltage rating is dictated by the buck topology while the conduction loss, being proportional to $R_{DS(on)}$, is at its worst in the boost topology. The consequence is either lower system efficiency, larger component size, higher cost, or a combination of these.

Also, the energy in a capacitor is proportional to V^2, which reduces the benefits of boosting at low voltage. For example, the energy left in a capacitor between 40 V and 20 V is quite low (<18%) versus that left between 90 V and 40 V.

Finally, the control strategy is much more complex when this multimode configuration is used during holdup. For example, a right-half-plane zero will be present during operation in boost and buck/boost modes, and slope compensation is required for each mode when the source voltage is going down.

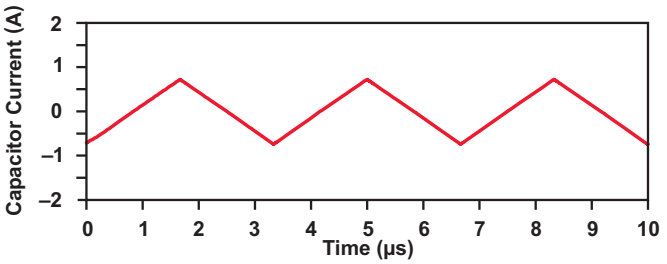


Fig. 17. Output-capacitor current with buck topology, 250-W load, 80-V input, and 40-V output.

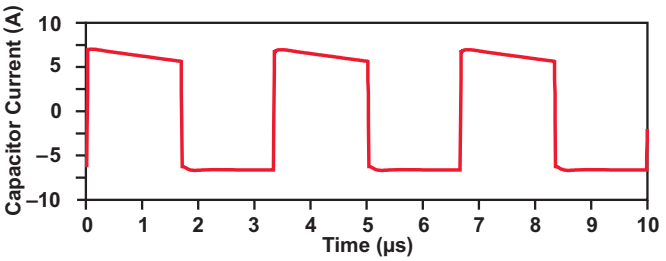


Fig. 18. Output-capacitor current with boost topology and same buck inductance value, 250-W load, 20-V input, and 40-V output.

Power-Bridge Trade-offs Summary

A comparison of the three power-bridge configurations is shown in Table 1. Note that all of these configurations use N-channel MOSFETs, which provide better performance and efficiency at lower cost than PMOS devices. Storing energy

TABLE 1. HVES CONFIGURATIONS COMPARISON

Configurations, Topologies, and Control		Mode	Benefits	Drawbacks	Cost	HVES Size
1	Recharge: Boost, peak-current-mode control	Recharge	• Low HVES parts count	• Needs upstream hot swap in main path to handle inrush • Oversized hot-swap MOSFET • Long recharge time	Low	Low
	Holdup: Buck, voltage-mode control	Holdup	• Low power-bridge complexity • No current sensing • Simple control strategy	• 100% duty cycle may be needed		
2	Recharge: Flyback, peak-current-mode control	Recharge	• Inrush control • short-circuit protection	• High-side gate driver for Q_A	Low	Low
	Holdup: buck, voltage-mode control	Holdup	• Low power bridge complexity • No current sensing • Simple control strategy	• Less efficient with Q_A MOSFET • 100% duty-cycle may be needed		
3	Recharge: Flyback, peak current mode control	Recharge	• Inrush control • Short-circuit protection	• High-side gate driver for Q_A	Medium	Medium
	Holdup: Buck, flyback and boost, current-mode control	Holdup	• Operates even if $V_{storage} < V_{bus}$	• High complexity • Larger inductor • Bus capacitors ripple current • Four large power MOSFETs and drivers		

at high voltage is the main factor that reduces the size of HVES systems, while conversion efficiency also has some impact, but to a lesser degree.

Since bridge configuration 2 (flyback/buck) appears to be the best choice, it will be the focus of the rest of this topic. This topology provides a good trade-off between addressing the basic system needs (HVES functionality with small size) and keeping the complexity and costs to an acceptable level.

During recharge mode, peak-current mode provides good current control and adjustability of the total recharge time.

Using the voltage-mode buck topology during holdup mode results in straightforward control, good transient response, low output-ripple current, and small size. Also, no synchronous rectification is used and the Q_C/Q_A packages can be small.

During recharge mode, the converter operates in discontinuous mode most of the time, with the exception of the initial recharge from 0 V. In order to achieve quasi-zero current consumption under such conditions, Q_D's body diode is used. This is explained in more detail in the next section.

C. Recharge Mode

Charging the Bank on Power Up: Bus Protection and Recharge Time

The HVES capacitor bank can be very large, which poses several challenges during the recharge cycle. It is important to minimize the impact of the HVES on the system, particularly at the start of recharge when the capacitor voltage is near 0 VDC, which can result in very high input current. Short-circuit protection is also needed, and the total recharge time must be considered.

One issue is related to the inductor's volt-second balance when the voltage across the storage capacitors is close to 0 V for a long time. In peak-current-mode control, the use of leading-edge blanking and/or filtering on current sensing introduces a minimum time (t_{LEB_filt}) during which the power switch is on. This means that during the ON time, neglecting the voltage drop in the series elements, the minimum increase of inductor current is

$$\Delta I_R = \frac{V_{IN} \times t_{LEB\_filt}}{L}. \quad (2)$$

Based on the current path shown in Fig. 13b, the change in current during OFF time can be expressed as

$$\Delta I_F = \frac{(V_{storage} + V_{dB} + V_{dD}) \times t_{OFF}}{L}, \quad (3)$$

where V_{dB} and V_{dD} correspond respectively to diode D_B and Q_D's body diode (supposing Q_D is maintained off), and t_{OFF} is the OFF time. Note that V_{dB} and V_{dD} go down as the junction temperature of D_B and Q_D increases. While $V_{storage}$ is close to 0 V, volt-second imbalance will occur if t_{OFF} is not long enough. This imbalance will cause the inductor current to rise very high even though there is still peak-current detection.

A second issue during recharge is the risk of not reaching the peak-current threshold during the ON time while $V_{storage}$ is close to 0 V. Based on Fig. 13a, when Q_C is turned on, the drain voltage is

$$V_{QC\_drain} = I_{QC} \times (R_{sense} + R_{on\_QC}). \quad (4)$$

Before using Equation (4), the following equation must be satisfied or some of the inductor current will flow through Q_D's body diode and the current-sensing circuit will detect only part of the inductor current.

$$V_{QC\_drain} < V_{storage} + V_{dD} \quad (5)$$

Also, given that the voltage across the sense resistor is

$$V_{sense} = \frac{V_{QC\_drain} \times R_{sense}}{R_{sense} + R_{on\_QC}}, \quad (6)$$

the selection of R_{sense} and R_{on_QC} must ensure that the V_{sense} threshold can always be reached while $V_{storage} \approx 0$ V. Otherwise, Q_A will stay on even at very high current.

A third issue is that the total recharge time must be low enough to support application performance requirements. In some applications, however, a recharge time of many seconds may be acceptable to minimize the impact of the HVES capacitor recharge on the input bus.

Charge Maintenance and Recharge: Low Noise and Minimal Loss

When the HVES capacitors are in a fully recharged state, the HVES power consumption on the bus must be less than the leakage loss of an equivalent bulk-capacitors solution. To achieve low current consumption during charge maintenance, synchronous rectifiers should not be used. This allows the converter to operate in discontinuous conduction, resulting in maximum efficiency.

There are many techniques that can be used in order to minimize power consumption of a power supply at light load. One popular technique is pulse-frequency modulation (PFM), which activates the power bridge only when the capacitor's voltage is below a predefined threshold. As a result, the total consumption becomes proportional to the storage capacitor's leakage current and the idle consumption of the control circuitry, including the voltage-feedback network(s). Note that using this hysteretic-control technique means that an output-voltage ripple is regulated at a very low frequency. The leakage characteristic of the capacitors (including temperature effects), in addition to the allowed voltage-ripple amplitude, has a strong impact on this modulation frequency. See Fig. 45 in Section III.B.

The HVES system must be designed so that there are minimal conducted and radiated emissions, particularly when the capacitors are in a fully recharged state. The use of PFM with a low recharge current may help to achieve that goal.

Stability

The HVES capacitance required can change considerably depending on specific system requirements. Energy storage at high voltage normally requires the use of electrolytic capacitors for which the ESR varies considerably, particularly over temperature. These variables need to be considered during the design to result in a stable control loop.

D. Holdup Mode

Speed, Accuracy, and Load Protection

The transient response at the beginning of a holdup event is critical. This includes the detection of the bus-voltage drop and the transition from recharge mode to holdup mode.

Many issues related to holdup mode need to be considered during the HVES design.

- The holdup error-amplifier reaction time is important since the holdup-voltage regulation loop is open prior to the holdup event. Depending on the dynamics of the compensation design for the holdup error amplifier, the transient response of the system may be unacceptable. Note that an advantage of voltage-mode control versus current-mode control is that the error amplifier's output directly defines the operating dutycycle, which could result in enhanced transient response.
- It is important to consider the bus-capacitance ESR and the effect on the bus voltage when the system voltage drops out. The bus capacitance is expected to be lower as a benefit of using HVES. The bus capacitors' ESR introduces a negative voltage step during the transition to holdup mode. Also, some capacitor types exhibit strong ESR variation over temperature.
- Some applications require high regulation and detection accuracy during a holdup event. V_{holdup}, the regulated voltage during holdup, must be higher than V_{load_min} but lower than V_{bus_min} (see Fig. 19). The closer V_{bus_min} and V_{load_min} are, the more precise the detection and regulation need to be.

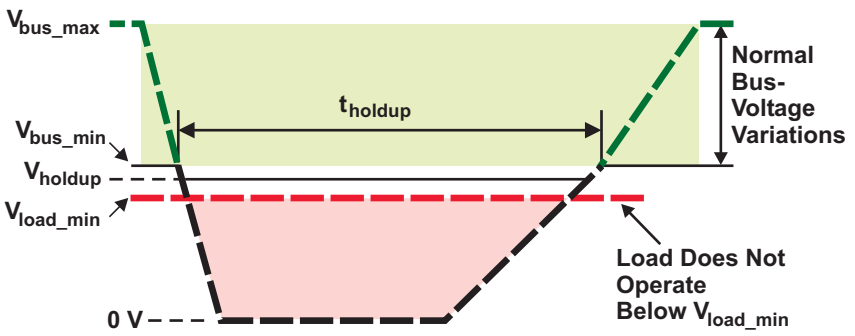


Fig. 19. Critical voltage levels for holdup circuit.

- To be able to handle a series of short dropout events, the HVES system needs to draw from the capacitors only the energy required by the load for the dropout event and must automatically detect the return of the input bus.
- The holdup mechanism must provide load protection and preferably maintain the internal bus voltage within maximum limits (V_{bus_max}) during some types of failures. A dedicated overvoltage-detection feedback network might be required to provide protection against loss of feedback in the main HVES voltage loop.
- Finally, the possibility of a complete short-circuit on the internal bus needs to be considered—for example, a capacitor or semiconductor failure in the input stage of a load unit. One mitigating factor is that the amount of energy available is limited to the amount of HVES capacity.

Efficiency and Energy

The following component selection has been assumed for the efficiency and dissipation graphs of this topic: Vishay SUD15N15-95 for Q_D, Fairchild FDD2512 for Q_C, NXP PHT4NQ10T for Q_A, Vishay ES3C for D_C, Renco RL-1256-1-47 for inductor L, and Panasonic EEVFK2A331M for the HVES capacitors (unless otherwise noted).

As mentioned before, the conversion efficiency during holdup has some impact on the size of the HVES unit. The losses can be categorized as follows:

- Conduction losses in MOSFETs, diodes, PCB traces, and capacitors' ESR
- MOSFET switching and gate losses
- Reverse-recovery losses
- Inductor losses—winding losses and core losses

Figs. 20 and 21 show an example of the efficiency and major losses for an HVES system configured as in Fig. 12. In this example, only Q_D is switched while Q_C and Q_A are maintained off, using D_C and Q_A's body diode.

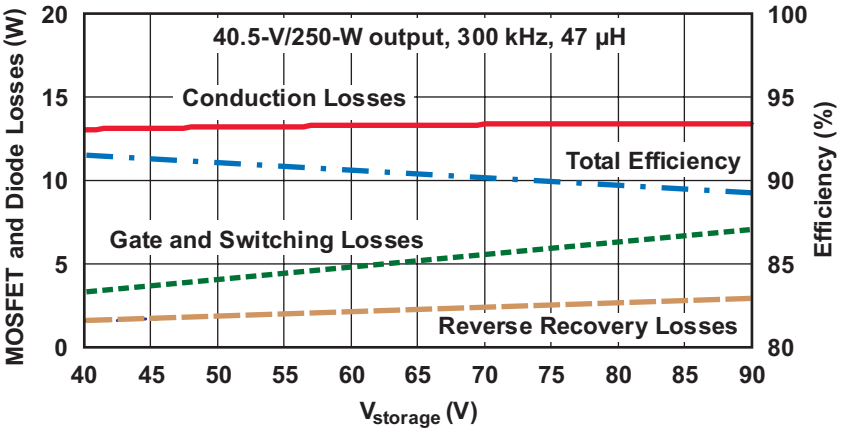


Fig. 20. Total MOSFET and power-diode losses with overall efficiency versus storage capacitor's voltage for HVES buck at high temperature ($T_J \approx 100°C$).

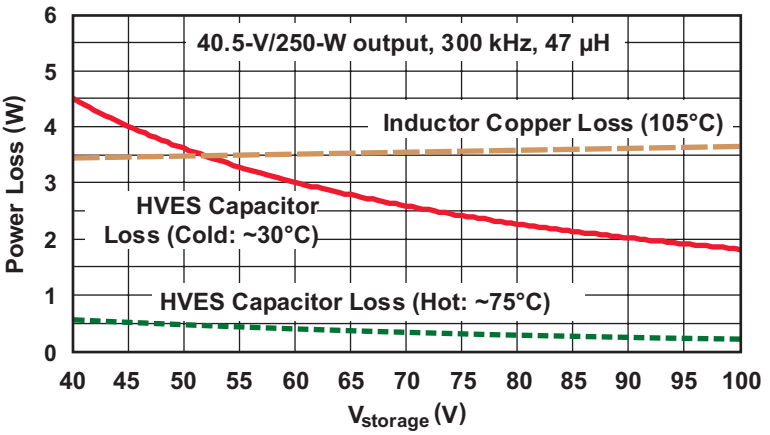


Fig. 21. Capacitor losses (at high and low temperature) and inductor losses versus storage voltage.

Note that the dissipation in the HVES capacitors increases at cold temperature because of the increase in ESR. Dissipation also increases as the voltage goes down, since the duty cycle then goes up.

Lower efficiency results in the need for higher storage capacitance, although the change in volume may vary on a case-by-case basis.

In the example in Section I.B where the Panasonic EEFK 100-V capacitor series is used and V_1 equals 88 V, if the average efficiency goes down to 80%, the minimum required storage capacitance becomes approximately 803 µF, which is a 14% increase. After a capacitance derating factor of 74% is applied for worst-case variations, the capacitor bank's PCB area increases by close to 30% because a fourth 330-µF capacitor becomes necessary.

EMI and Self-Compatibility

Holdup is the highest-power mode and therefore a potential source of EMI; but because holdup events are infrequent and short in duration, the EMI conducted and radiated to the outside world during such events may not be an issue. However, requirements for self-compatibility between the elements of a system using HVES must still be met, and this is applicable to any operating mode, including a holdup event.

E. Safety and Bank Discharge

People whose safety needs must be considered are the users of the equipment and service personnel [1].

Users must be protected against inadvertent contact with hazardous voltages. In an HVES system, this is achieved with physical spacing and grounded enclosures that isolate the user from the charged capacitor bank.

Service personnel, who normally have access to all parts of a system, must also be protected from inadvertent contact with a hazardous surface and from unknowingly bridging a tool between parts with high energy levels while servicing another part. The main concern with an HVES system is that the storage capacitor's voltage and energy must be reduced to a safe level in a reasonable time after the unit has been unplugged. This requires a mechanism that automatically discharges these storage capacitors upon unit removal.

F. State-Machine Considerations

Fig. 22 shows an example of a simplified HVES state machine and timing diagram using a PFM recharge mode. In this state machine, "V_{st} = Low" stands for "low storage voltage" and

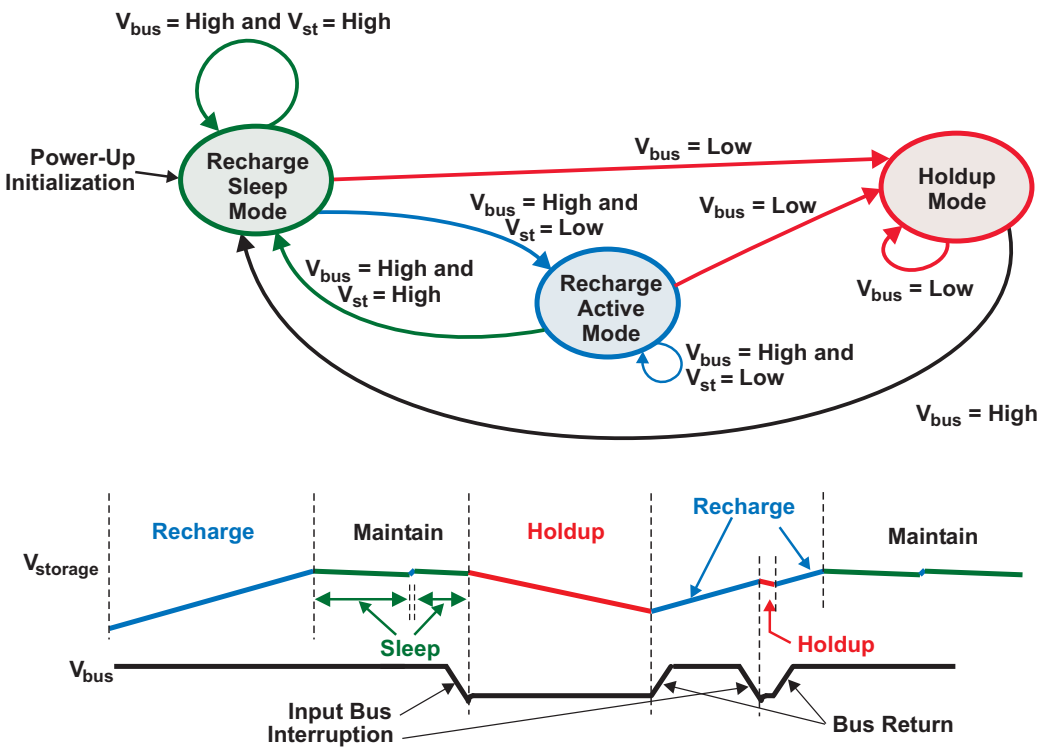


Fig. 22. Simplified HVES state machine.

indicates when the capacitor's voltage is below a threshold. "V_{bus} = Low" means that the input power goes down, and "V_{bus} = High" means there is no input-power interruption or the system returns to the beginning state.

The following describes a typical operating sequence based on this state machine.

- After input-power-bus power up, the HVES capacitors are recharged (Recharge Active Mode) and maintained at an elevated voltage. Once the capacitors are fully charged (V_{st} = High), the PFM technique is used.
  - With the PFM technique, the HVES system operates in Recharge Active Mode only when the capacitors' voltage is below a threshold (V_{st} = Low). Otherwise, it operates in Recharge Sleep Mode for minimum power consumption. See Fig. 45.
- The input-power bus is momentarily interrupted. The bus voltage goes below the holdup trigger threshold (V_{bus} = Low). The HVES operates in holdup mode and maintains the bus voltage at the holdup regulation voltage, discharging the storage capacitors partly or completely.
- At the end of input-power-bus interruption (V_{bus} = High), the HVES returns to recharge mode.

Other aspects not shown in Fig. 22 also need to be considered, for example the automatic discharge of storage capacitors upon unit removal, whatever the current operating mode.

G. Thermal Aspects

When the thermal performance of an HVES system is analyzed, the following aspects need to be considered.

- The recharge mode uses the PFM technique, which implies sleep intervals. The duration of initial recharge varies with the storage capacitance and the nominal recharge voltage. HVES MOSFETs are operated in switch mode only; there is no linear inrush limiting.
- The holdup mode duration is limited, so dynamic thermal behavior needs to be considered. This concerns the MOSFETs, the diodes, and the PCB when used as a heatsink. Allowed dynamic stresses can be significantly higher than static stresses, depending on component types, packages, and power-pulse duration. See Fig. 23 for an example.
- The mechanism that automatically discharges the storage capacitors upon unit removal needs to be able to dissipate all of the stored energy as heat without exceeding critical temperatures.
- There are three basic methods to move heat away from the source: conduction, convection, and radiation.
- With the use of small component packages, conduction is particularly important because it spreads out the heat to the surface area needed to dissipate the heat by means of convection and radiation. PCB copper planes are commonly used for that purpose.

Graph data courtesy of Vishay Intertechnology.

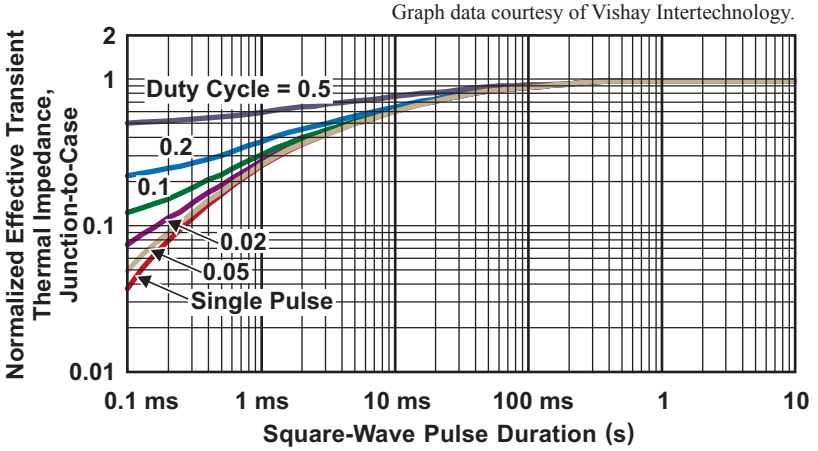
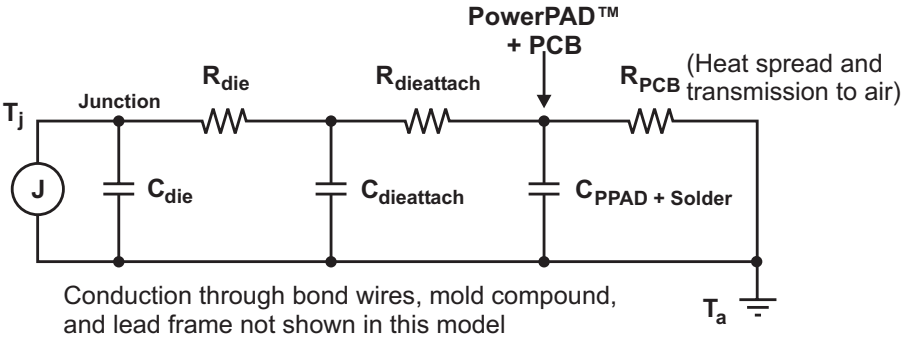
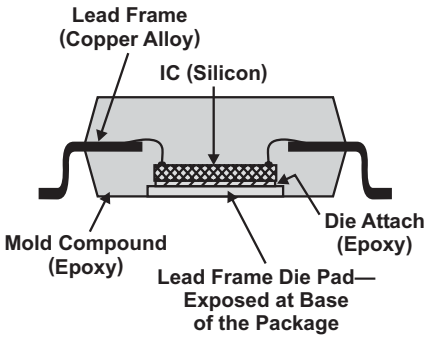


Fig. 23. Example of MOSFET effective transient thermal impedance (with Vishay SUD15N15-95).



a. Circuit model.



b. Package components.

Fig. 24. Example of simplified thermal model for integrated circuit with PowerPAD™.

The wattage that can be safely dissipated within the part depends on how well heat is removed from the package. Fig. 24 shows an example of a simplified thermal model where heat is transferred to the air from the die mainly through the die attach material, the PowerPAD™ [2], and the PCB. Each capacitor in fact represents an element's thermal capacitance determined by its specific heat and mass.

III. Bidirectional Converter HVES System Design

The following design guidelines are based on bridge configuration 2 shown in Fig. 12, which uses a nonisolated flyback topology in recharge and a voltage-mode buck topology (Q_C and Q_A being maintained off) in holdup mode. The PFM technique with constant OFF time is also used during recharge. Note that during holdup operation, the voltage source becomes the storage capacitor bank while the load is on the bus side of the power bridge.

A. Power-Stage Considerations

Although the HVES system has two main operating modes, the holdup mode needs to be considered first during the selection or design of power components. The recharge mode, which is a low-power mode, needs to be flexible enough to accommodate itself to these selections.

Inductor Design or Selection

The design or selection of the inductor should be made based on the following criteria.

Inductance Value—For a buck topology, the inductor is directly in series with the output load. Consequently, it carries the load current added to the ripple current circulating into the output capacitors. Typically, a buck inductor is designed to have a ripple factor of around 20% when operated with continuous current at full load (the ripple factor being the ratio of the peak-to-peak ripple current to the average maximum current value).

In an HVES application, the capacitor bank constitutes the input of the buck power supply, and its voltage goes down as the capacitors' energy is delivered. This means that the ripple factor also goes down, as shown in Figs. 25 and 26.

The peak maximum inductor current and the peak-to-peak ripple inductor current can be estimated respectively as

$$I_{L\_pk(max)} = \frac{P_o}{V_{bus}} + \frac{1}{2} \times \frac{(V_{bus} + V_{fA} + V_{fC}) \times (1 - D)}{L \times f_s}, \quad (7a)$$

and

$$I_{rip\_pkpk} = \frac{(V_{bus} + V_{fA} + V_{fC}) \times (1 - D)}{L \times f_s}, \quad (7b)$$

and where P_o is the load power; V_{bus} is the buck output; V_{fA} and V_{fC} are the forward voltage drop of, respectively, Q_A's body diode and Q_C's parallel diode series elements; D is the duty cycle; f_s is the switching frequency; and L is the inductance. The duty cycle can be predicted as

$$D = \frac{V_{bus} + V_{fA} + V_{fC}}{V_{storage} + V_{fC} - V_{QD}}, \quad (8)$$

where $V_{storage}$ is the input of the buck and V_{QD} is Q_D's $R_{DS(on)}$ voltage drop. Note that the impact of the series loss elements is to increase the duty cycle. Note also that, as shown in the previous equation and Figs. 25 and 26, the ripple current isn't a function of load in a continuous-mode buck.

The inductor is calculated as

$$L = \frac{D \times (V_{storage} - V_{bus} - V_{fA} - V_{QD})}{f_s \times I_{rip\_pkpk}}, \quad (9)$$

where I_{rip_pkpk} is the peak-to-peak inductor current as already defined. Note that since the storage capacitors' voltage is not constant, the calculated inductance value changes according to what level of $V_{storage}$ the 20% rule is applied (see Fig. 26). Also, the required inductance value will decrease as the switching frequency increases.

The inductance value has a strong impact on transient response. A low inductance value results in a higher di/dt with theoretically faster speed. However, with a higher inductance, the buck power supply stays in continuous mode at a lower load level. This in turn improves the transient response to a strong load step simply because, in discontinuous mode, the error-amplifier output goes down with the load current and would take longer to rise to the level needed for the load step.

Selecting a higher inductance value also reduces the ripple current, which then reduces the output voltage ripple which depends on the ESR of the output-bus capacitors.

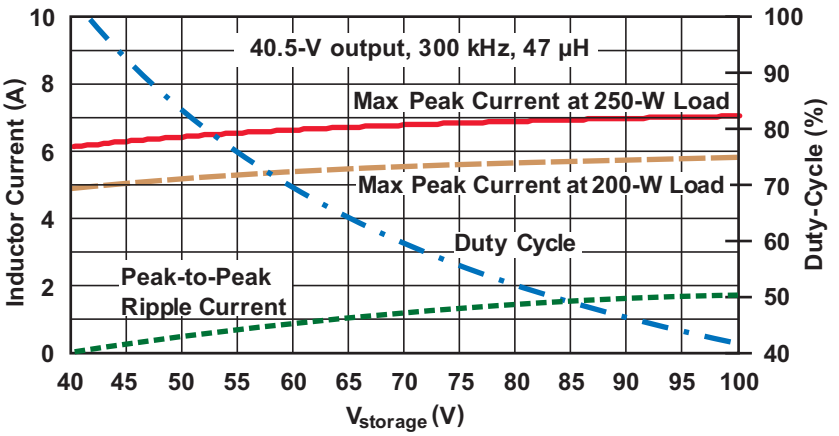


Fig. 25. Buck inductor current and duty cycle versus $V_{storage}$.

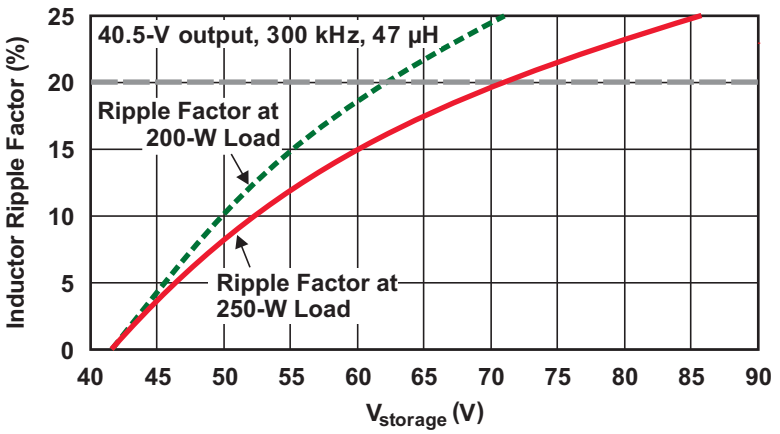


Fig. 26. Buck inductor ripple factor versus $V_{storage}$.

Low enough DC and AC winding resistance for good efficiency—DC resistance is dictated by wire size and the number of winding turns. AC resistance, which is related to skin effect but is largely due to proximity effect [3], is also influenced by wire type (single-strand or Litz) and the number of winding layers. AC resistance can be estimated, but a measurement with adequate instrumentation (i.e., with the inductor's magnetic core not installed to exclude core loss) is necessary for better accuracy. See Fig. 27.

The simplified equation for total winding loss is

$$P_W = (R_{DC} \times I_{DC}^2) + (R_{AC} \times I_{AC}^2) \quad (10)$$

with

$$I_{AC}^2 = I_{RMS}^2 - I_{DC}^2, \quad (11)$$

where R_{DC} is the D_C resistance of the inductor; R_{AC} is its resistance measured at the switching frequency; and I_{DC} and I_{AC} are, respectively, the DC and AC current circulating through the inductor.

R_{AC} is in the form

$$R_{AC} = R_{DC} \times (1 + K_{PSE}), \quad (12)$$

where K_{PSE} is the resistance-increase factor related to the proximity and skin effects. Analysis can demonstrate that for a buck operating in CCM, the DC losses in the inductor dominate in most applications, even when single-strand wire is used. The AC losses become more important with high ripple current where higher harmonics are no longer negligible or at high switching frequencies.

Core Shape and Material—This has a direct impact on core loss and inductor-radiated emissions. Gapped ferrite cores provide lower core loss at high frequency and have large flux swings, but they have a sharp saturation characteristic and low-saturation flux density. A torroidal core with distributed gap material, for example powdered iron or Permalloy powder, provides a softer saturation characteristic and lower radiated EMI (torroid shape) but has much more core loss at high frequency.

Graph data courtesy of Renco Electronics. www.Rencousa.com

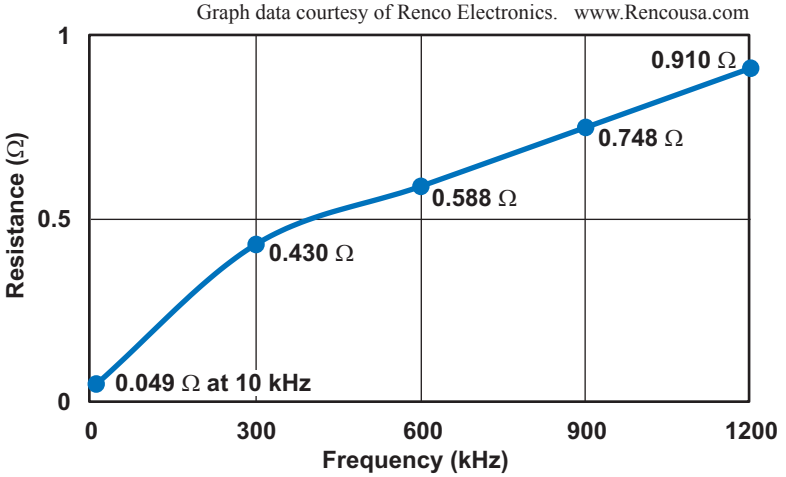


Fig. 27. Inductor AC resistance versus frequency (with Renco RL-1256-1-47).

The unshielded open-core inductor using ferrite provides a good cost and size alternative, although it has its limitations. Due to its inherent open flux path, it couples noise to circuits nearby and radiates EMI to the outside world. It is worth noting that the very close proximity of a metallic surface having magnetic properties can change the inductance by an amount that is difficult to predict. For example, steel material, because of its high-absorption-loss properties, can reduce the inductance value [4]. In addition, currents induced in a surface having conduction properties can introduce additional power losses.

For example, with the Coilcraft DO-5040H inductor, the core loss per unit of core volume can be calculated as

$$P = K_{loss} \times f^X \times B^Y, \quad (13)$$

where P is in mW/cm^3, K_{loss} is 0.041, f is the frequency in kHz, B is the peak value of flux density in kilogauss, x = 1.63, and y = 2.51.

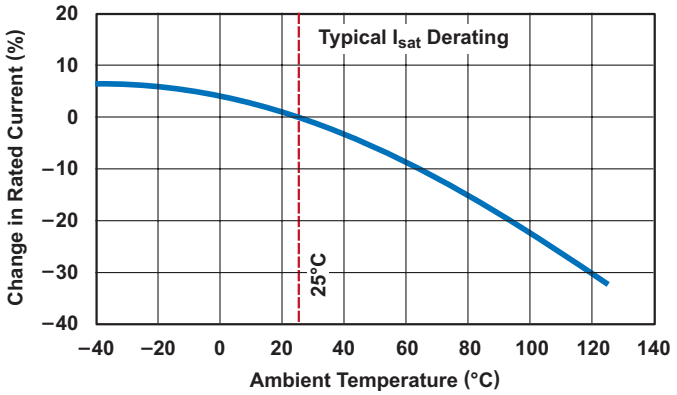
B can be calculated in gauss as

$$B = \frac{D \times (V_{storage} - V_{bus} - V_{fA} - V_{QD}) \times 10^5}{2f_s \times N_{turns} \times A_{core}}, \quad (14)$$

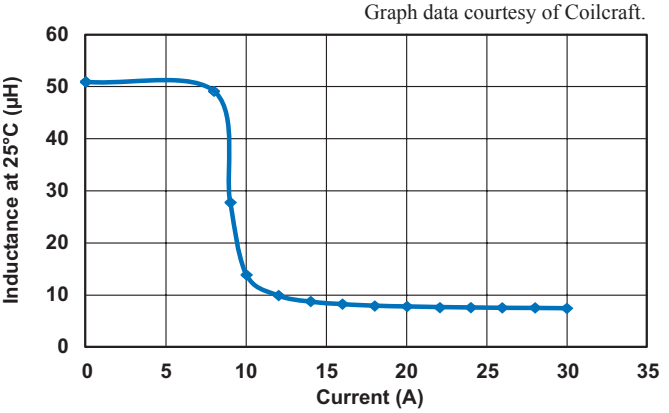
where all voltages are in volts, N_{turns} is the number of turns, A_{core} is the inductor's core cross-section in cm^2, and f_s is in kHz. The parameter values mentioned are normally not available in data catalogs and need to be provided by the inductor manufacturer. Other manufacturers instead provide a simple equation calculating the core loss*, starting from the frequency and the ripple current.

*See Equation (43) on page 5-29.

Graph data courtesy of Coilcraft.



a. Saturation current versus temperature.



b. Inductance versus current.

Fig. 28. Inductor saturation characteristic (with Coilcraft DO-5040H-473 inductor).

High DC Saturation Current—The peak current at full load should be considered. The worst case is at minimum switching frequency and maximum $V_{storage}$ where the ripple current is maximum (see Figs. 25 and 26), and at high temperature where typical inductors show a decrease in saturation current level (see Fig. 28). There should also be some margin for overloads of short duration as well as for inductors' manufacturing tolerance variations.

Small Physical Size—Since the inductor dissipates high power only during a short holdup event, its physical size and PCB footprint depends mainly on its peak saturation current and to a much lesser extent on its winding resistance.

Selecting Switches and Diodes

The selection of power semiconductors is a trade-off between size, efficiency, and cost. As shown in Fig. 12, during holdup mode only Q_D is activated and the release of the inductor energy to the bus is done through diodes. Using an ultrafast diode in parallel with Q_C and a sense resistor constitutes a good trade-off, providing acceptable conduction loss with low reverse-recovery loss and no Q_C-gate switching loss in holdup mode. For higher efficiency, a Schottky diode can be used in parallel with Q_A, particularly at lower bus voltages.

Because the average and peak currents involved during recharge mode are very low, the Q_C and Q_A packages can be small and low-cost, for example D-PAK or even SOT-223 and SOIC. Since a holdup event is a relatively short event, physically smaller diodes can be used.

The selection of Q_D is critical to holdup performance and efficiency. While $V_{storage}$ varies from its initial to its final value, Q_D should provide a good balance between conduction loss, which is proportional to $R_{DS(on)}$; reverse-recovery loss; and gate-drive and switching losses. Also, a low Q_{rr} of the body diode of Q_D and low drain-to-source capacitance will provide a more efficient and faster recharge mode.

Fig. 29 shows an example in which 40.5 V is regulated with a 250-W load, with the Vishay SUD15N15-95 MOSFET. Not surprisingly, the

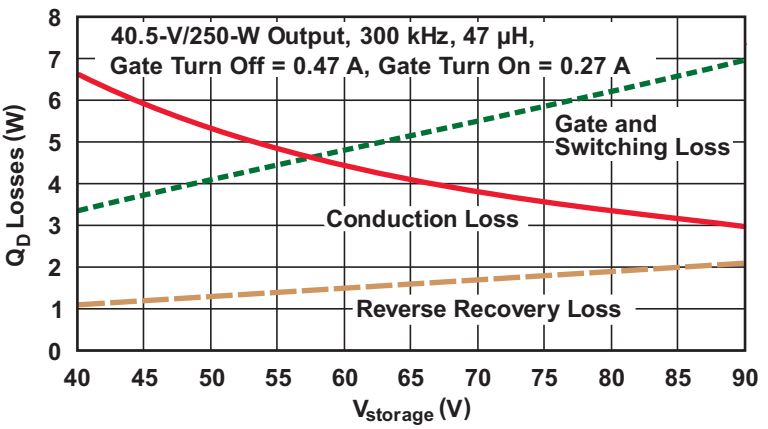


Fig. 29. Q_D's power losses versus $V_{storage}$ at T_j = 110°C using Vishay SUD15N15-95 MOSFET and ES3C diode.

conduction loss is dominant at low $V_{storage}$ while the gate-drive, switching, and reverse-recovery losses become more important at a high voltage. The switching frequency used, f_s = 300 kHz, has a strong impact on the results as reflected in several equations below.

The loss types for Q_D during holdup are conduction, switching, reverse recovery, and gate drive. Q_D's conduction loss can be calculated as

$$P_{QD\_cond} = R_{on\_QD} \times I^2_{QD\_RMS}, \quad (15)$$

where

$$I_{QD\_RMS} = \sqrt{D \times \left[\left(\frac{P_o}{V_{bus}} \right)^2 + \frac{I_{rip\_pkpk}^{\ 2}}{12} \right]} \quad (15a)$$

and

$$I_{rip\_pkpk} = \frac{(V_{bus} + V_{fA} + V_{fC}) \times (1 - D)}{L \times f_s}. \quad (16)$$

Q_D's switching loss can be calculated as shown below in Equation (17) where Q_{gdD} and Q_{gs2D} are the gate-drain and gate-source charges as shown in Fig. 30; I_{G_off} and I_{G_on} are the average gate-drive currents during Q_D turnoff and turn-on, respectively; and C_{dsD} is the drain-to-source parasitic capacitance with V_{ds_QD} equal to $V_{storage}$. Note that Q_{gdD} and Q_{gs2D} vary depending on $V_{storage}$ (shown in Fig. 31) and the load current.

For the selected configuration, only Q_D is activated. This limits the gate switching losses, which can be calculated as

$$P_{gdrv} = f_s \times \left(V_g \times Q_{gTD} + \frac{1}{2} Q_{gdD} \times V_{storage} \right), \quad (18)$$

where Q_{gTD} is Q_D's total gate charge as shown in Fig. 30 (Q_{g_tot}), and V_g is the supply voltage needed by the gate driver. However, if V_g is derived from V_{bus} with linear regulation, V_{bus} should be used in the equation instead of V_g.

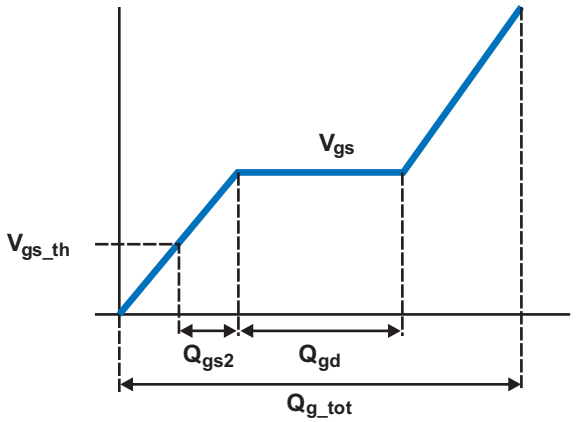


Fig. 30. General plot of a gate-charge waveform.

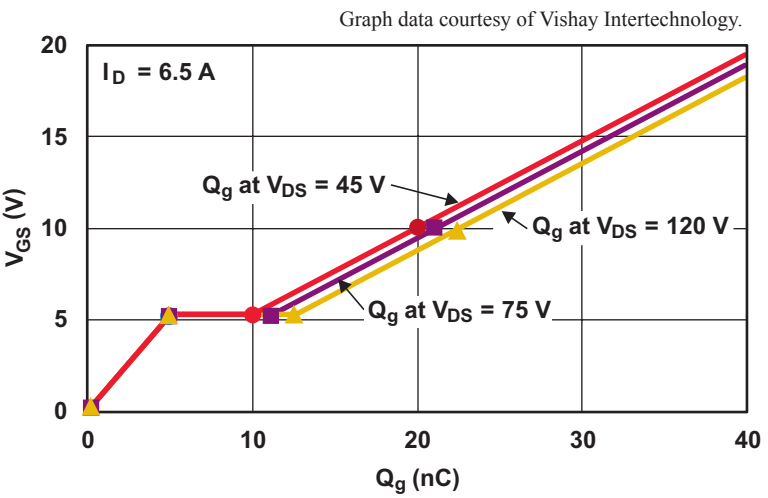


Fig.31. Gate-charge waveform for Vishay SUD15N15-95.

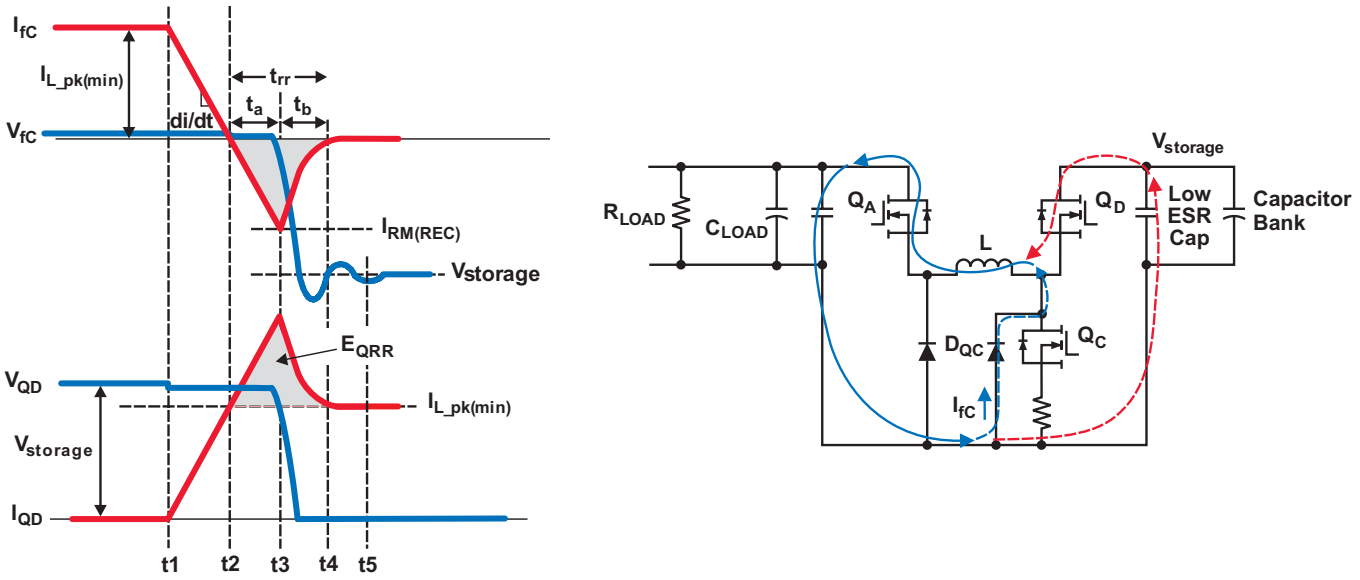
It is worth noting that

$$P_{QOSS\_D} = \frac{f_s}{2} \times \left(C_{dsD} \times V^2_{storage} + Q_{gdD} \times V_{storage} \right). \quad (19)$$

The first element is part of P_{QD_SW} since it is dissipated in Q_D (at turn-on), while the second element is part of P_{gdrv} because it is dissipated in the gate driver.

If, at the time Q_D is turned on there is a forward current through the diode placed in parallel with

$$P_{QD\_SW} = \frac{f_s \times V_{storage}}{2} \times \left\{ \left[\left(\frac{I_{L\_pk\,max}}{I_{G\_off}} + \frac{I_{L\_pk\,min}}{I_{G\_on}} \right) \times \left(Q_{gdD} + Q_{gs2D} \right) \right] + C_{dsD} \times V_{storage} \right\}, \quad (17)$$



a. Timing waveforms. *b. Current paths.*

Fig. 32. Example of reverse-recovery effect with fast Q_D turn-on.

Q_C (D_{QC}), there will be a reverse-recovery effect as shown in Fig. 32. This effect could occur, for example, when the power circuit is operated with a continuous current. The following simplified equation provides an estimate of the extra loss related to the reverse-recovery effect:

$$P_{rr\_tot} \approx f_s \times V_{storage} \times Q_{rrC}, \quad (20)$$

where Q_{rrC} is the reverse-recovery charge of D_{QC}. Note that P_{rr_tot} is distributed between the diode and Q_D. This power distribution can be influenced by many factors including diode characteristics, speed of MOSFET turn-on, and circuit parasitics. In most cases, the reverse-recovery losses are higher in the MOSFET (a ratio of 2 is common) than in the diode when an ultrafast diode is used.

Q_{rrC} can be estimated as

$$Q_{rrC} = I_{fC} \times t_T \times e^{-\sqrt{\frac{I_{fC}}{t_T \times di/dt}}}, \quad (21)$$

where I_{fC} is D_{QC}'s current prior to Q_D turn-on, t_T is the diode transit time (estimated using Q_{rrC}'s equation and diode reverse-recovery data with test conditions), and di/dt is the slew rate of the current as shown in Fig. 32. To mitigate reverse-recovery losses, D_{QC} should be selected for ultrafast reverse-recovery performance.

During holdup there is also conduction loss for D_{QC} which can be calculated as

$$P_{DQC\_cond} = \frac{P_o}{V_{bus}} \times V_{fC} \times (1-D). \quad (22)$$

The only type of loss for Q_A's body diode is conduction, which can be calculated as

$$P_{QA\_cond} = \frac{P_o}{V_{bus}} \times V_{fA}. \quad (23)$$

Unless negative bias is used to keep the MOSFETs turned off, it is better to select MOSFETs that have a relatively high V_{gs} threshold (for example, 2 to 4 V at 25°C), particularly for Q_C and Q_D, which are part of a half-bridge circuit. Note that V_{gs_th} typically goes down as the temperature increases.

Fig. 33 shows plots of typical losses using PHT4NQ10T and Vishay SUD15N15-95 MOSFETs and ES3C diode.

Selecting Capacitors

The primary concerns when selecting capacitors are size, voltage ripple, power dissipation, leakage current, circuit noise, and the impact on the control loops. Although there is a wide variety of capacitors on the market, very few can provide high capacitance per volume and

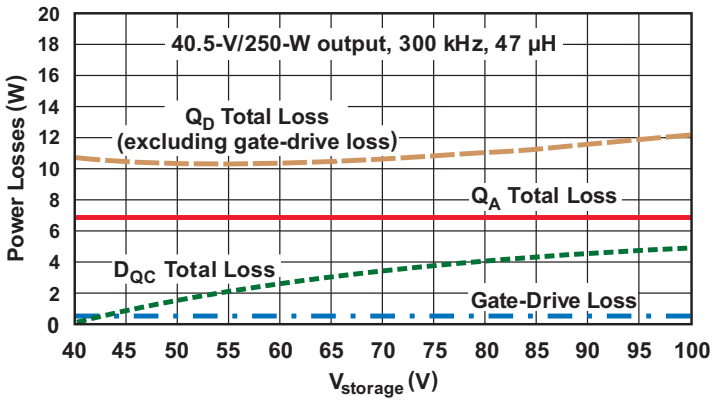


Fig. 33. Power losses with PHT4NQ10T (Q_A), SUD15N15-95 (Q_D) and ES3C.

Graph data courtesy of TDK Corporation of America.

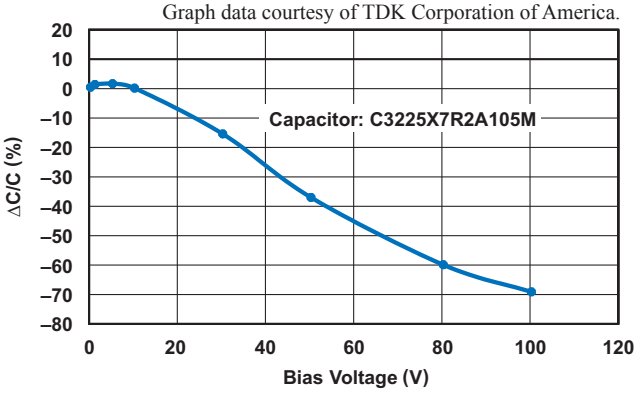


Fig. 34. Example of capacitance change versus voltage for a 100-V-rated TDK X7R ceramic capacitor.

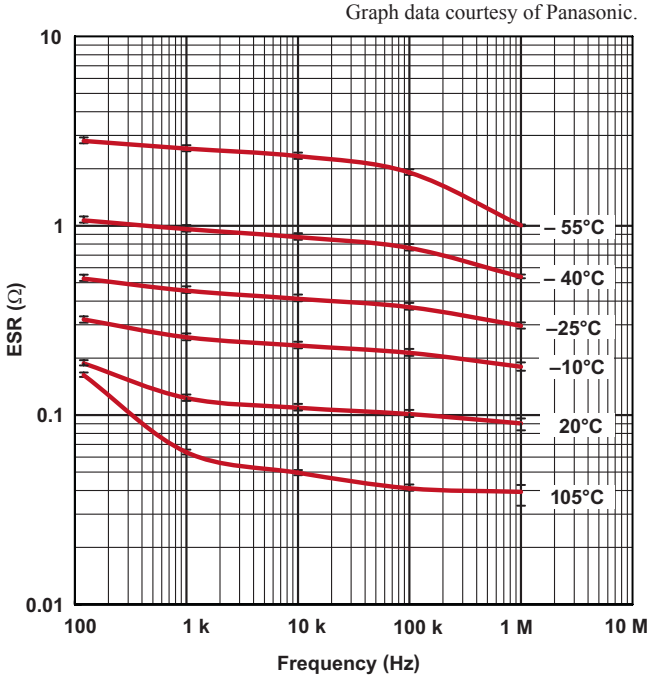
operate at 50 V or higher. This leaves the aluminium electrolytic capacitor as the first choice for energy storage, based on volume and cost. On the bus side, depending on the operating voltage, additional selection includes tantalum, polymer aluminium, and OS-CON capacitors, for example. Ceramic low-impedance capacitors are also required, on both the bus and the storage-bank sides, for the high-frequency switching current and noise filtering. Note that ceramic capacitors are strongly dependent on DC bias voltage, with capacitance going down substantially at higher voltage. See Fig. 34.

Capacitors for Energy Storage—Since the current is pulsating similarly to Q_D during holdup, the ESR is of prime importance. Electrolytic capacitors typically exhibit a very strong ESR variation, initially and over temperature (with the maximum ESR value at low temperature), as shown in Fig. 35. This variation has a direct impact on the capacitors' power loss which can be calculated as

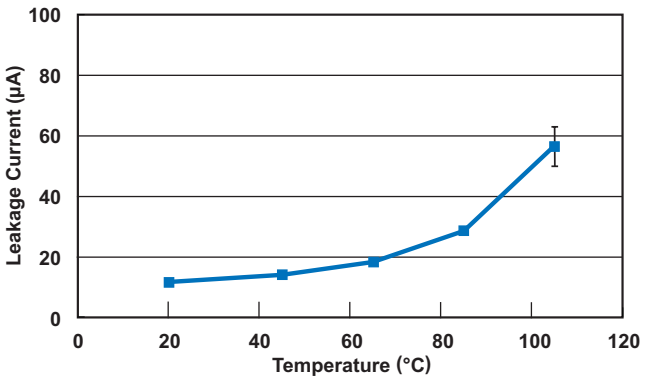
$$P_{cap\_st} = \frac{ESR_{c\_st}}{n_{c\_st}} \times I^2_{QD\_RMS}, \qquad (24)$$

where ESR_{c_st} is the ESR per capacitor, n_{c_st} is the number of storage capacitors in parallel, and all ESRs are assumed to be equal. The temperature dependency of capacitor power loss is shown in Fig. 21.

Graph data courtesy of Panasonic.



a. ESR variation.



b. Leakage current.

Fig. 35. Typical ESR and leakage current at 100 V over temperature for Panasonic EEVFK2A331M, 330-µF/100-V electrolytic capacitor.

Topic 5

The presence of a strong equivalent series inductance (ESL) in series with these capacitors can introduce undesirable resonance during recharge mode. Surface-mount or radial capacitors mounted vertically (with no right-angle mount) are recommended for storage, and they should be installed on the same PCB as the power bridge.

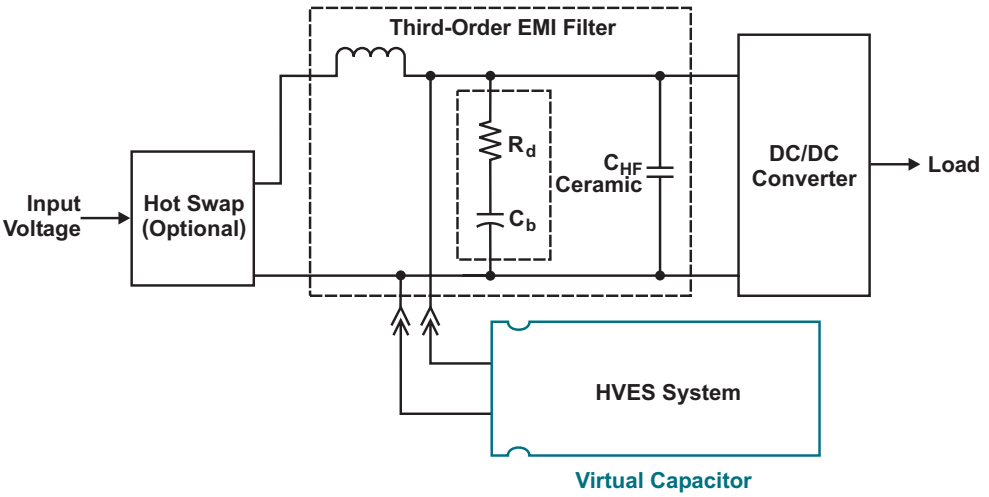
The leakage current of storage capacitors is also important as it influences the sleep-mode duration when the power bridge is off in recharge mode. The lower the leakage current, the lower the average current consumption of the HVES system while in sleep mode. The leakage normally increases with temperature (see Fig. 35).

Capacitors on Internal Bus—On the bus side, the capacitors are typically part of an existing EMI filter as shown in Fig. 36. C_b represents the internal-bus main capacitor(s). The DC/DC converter provides a constant power load and represents a negative incremental impedance to the EMI filter [5] and the HVES system. The EMI filter typically requires a damping resistance, R_d, as in Fig. 36 to avoid introducing instability into the system DC/DC converter(s). R_d includes the capacitor's ESR.

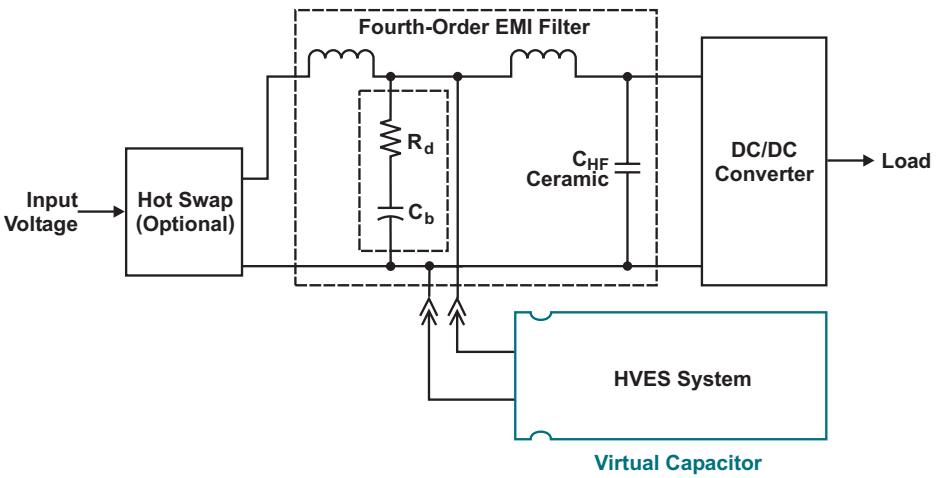
C_b and C_{HF} play the role of output capacitors when the HVES system operates in holdup mode. They minimize switching-noise voltage and help regulate voltage during load transients. Variations in peak output voltage can be estimated [6] with

$$V_{pk\,var\_bus} \approx Z_{out\_pk} \times I_{step}, \qquad (25)$$

where Z_{out_pk} is the peak output impedance (Z_{out}) of the HVES buck power supply including bus capacitance, and I_{step} is the load-step current. The initial spike is handled by capacitors and their parasitics. The overshoot duration during a load drop may be longer than expected since no synchronous rectifier is used.



a. With third-order differential-mode EMI filter.



b. With fourth-order differential-mode EMI filter.

Fig. 36. HVES systems with EMI filters.

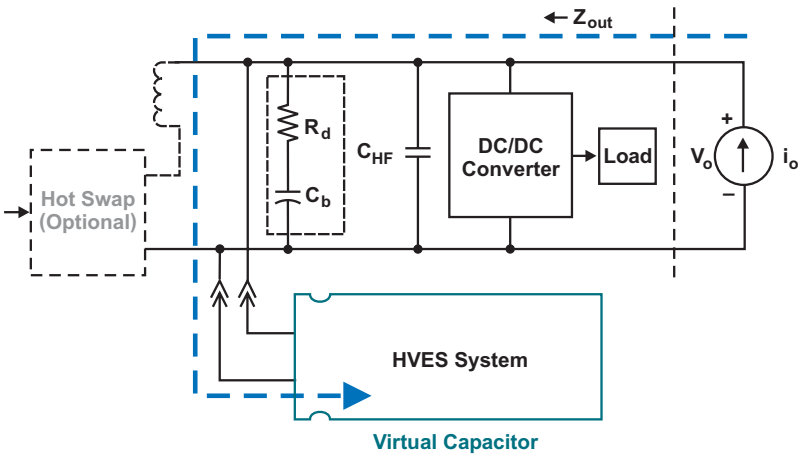


Fig. 37. In holdup mode, the load is powered by the HVES systems and the bus capacitance (parasitics not shown) is part of the system's output impedance.

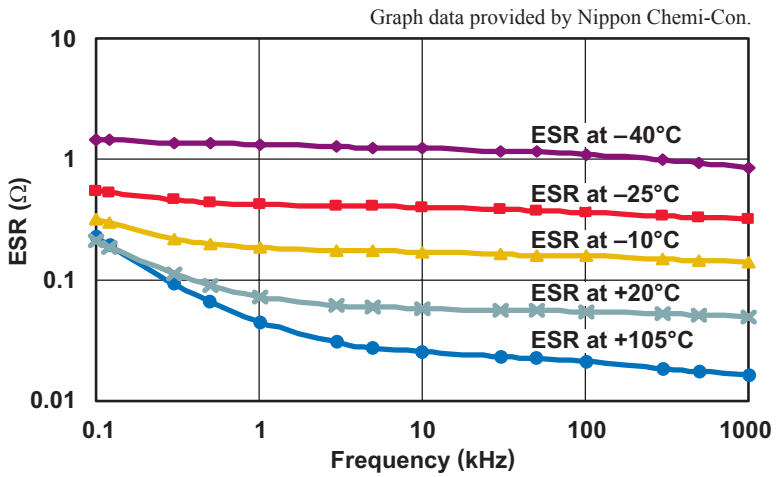


Fig. 38. Typical variation of ESR over frequency and temperature for Nippon Chemi-Con EKZE101E__101MJ16S, 100-µF/100-V electrolytic capacitor.

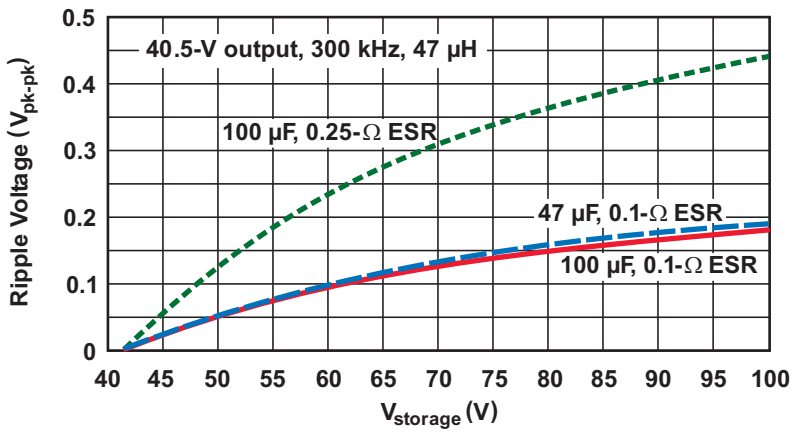


Fig. 39. Output-bus ripple voltage versus $V_{storage}$ with various ESRs and capacitances.

As shown in Fig. 37, the output impedance, Z_{out}, of a power supply can be determined over a frequency range by driving the supply output with a current source, i_o, then measuring the output voltage v_o.

C_b and C_{HF} also help maintain the bus voltage during the transition from recharge to holdup mode. The capacitors' series impedances (ESR, ESL) affect performance during that time. If, for example, C_b is electrolytic, the worst-case maximum ESR is at cold temperature as shown in Fig. 38. If the buck error amplifier is in open loop during recharge mode, significant additional bus-voltage drop may be introduced at the beginning of the holdup mode.

The bus ripple voltage (see Fig. 39) caused by the HVES system switching during holdup can be conservatively estimated as

$$V_{rip\_bus} \approx \frac{I_{rip\_pkpk}}{8f_s \times C_b} + I_{rip\_pkpk} \times R_d. \qquad (26)$$

The C_b ESL-related spike is not shown in the equation because with the addition of ceramic capacitors, which can also reduce V_{rip_bus}, the ESL is not contributing significantly to the noise.

For more accurate simulations, parasitic impedances of capacitor and PCB traces should be modeled. See the capacitor model in Fig. 40.

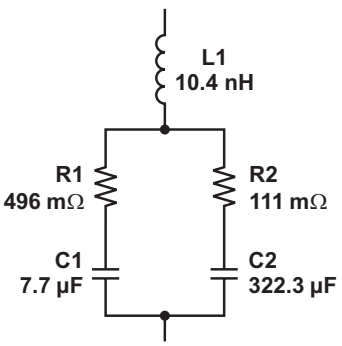


Fig. 40. PSpice® model for Panasonic EEVFK2A331M electrolytic capacitor at 100 kHz and 20°C.

The dissipation in the bus capacitors and damping resistor related to HVES operation can be estimated with the equation

$$P_{cap\_bus} = \frac{I_{rip\_pkpk}^2}{12} \times R_d. \quad (27)$$

Capacitor ESR also has a strong influence on the buck-voltage control loop, introducing a zero at the frequency $1/(2\pi R_d C_b)$ and providing damping against the negative impedance of the constant power load.

Gate Drivers

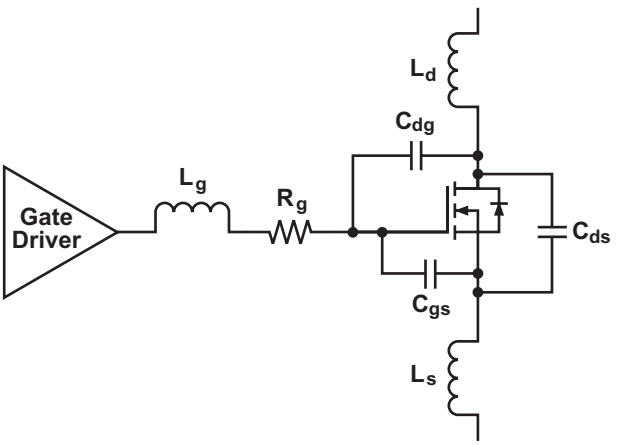
When gate-drive circuits are defined, the following needs should be considered:

- Optimal gate-drive voltage amplitude for full enhancement of MOSFETs and minimal gate-drive losses.
- Very low pull-down impedance for low turnoff switching loss and minimal risk of parasitic turn-on.
- Slower Q_D and Q_C turn-on to get the following:
  - Lower I_{RM} and voltage transients and stress related to reverse recovery (higher P_{QD_SW} but lower P_{rr_tot})
  - Lower risk of parasitic turn-on of the "other" MOSFET of the half bridge through its C_{dg} (see Fig. 41).
  - Limited dV/dt applied to the "other" MOSFET of the half bridge, reducing the risk of destructive turn-on [7, 8] of a parasitic bipolar junction transistor (BJT) if the body diode is conducting (see Fig. 41).
- Immunity of high-side Q_A and Q_D gate drivers to common-mode noise.
- Stable floating supply voltage for Q_A and Q_D under all conditions, for example by using a bootstrap technique. This can be done by monitoring the floating supply voltage and forcing a refresh of the bootstrap capacitor. The technique is particularly useful for the buck operation which requires the duty cycle to virtually reach 100%.
- Adequate power-dissipation capability of gate drivers.
- Adequate dead time between Q_D and Q_C if used in the same operating mode.

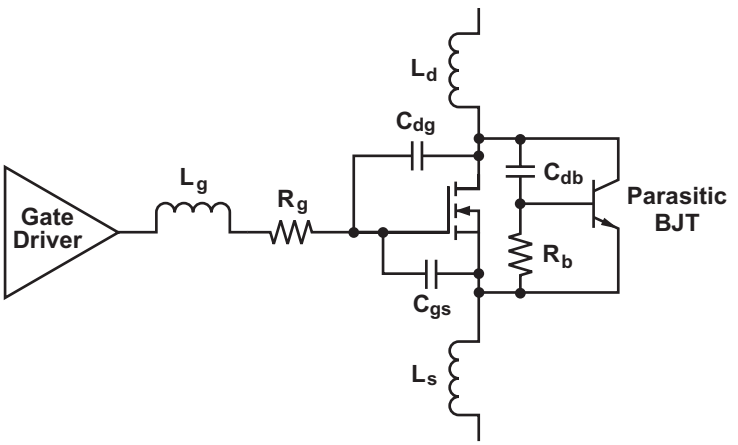
B. Control-Circuit Design Considerations

Recharge-Mode Control-Loop Design Considerations

The recharge-control circuit operates in a constant-off-time using peak-current-mode control (CMC) with a hysteretic error amplifier. See Figs. 42 and 43. Typical voltage-loop compensation is normally highly dependent on output capacitance and parasitics. One benefit of hysteretic control is that no compensation is required. Another is that there is no stability concern with a right-half-plane zero and a double pole at half the switching frequency. Peak CMC inherently provides current



a. Simplified view.



b. With parasitic BJT.

Fig. 41. MOSFET with parasitic components.

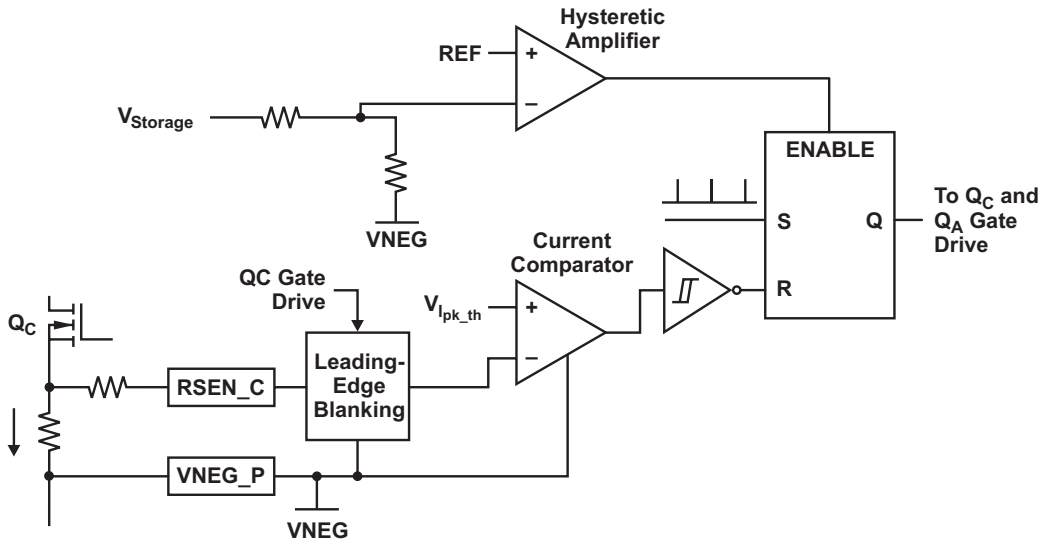


Fig. 42. Peak-current mode during recharge.

limiting. Note that turnoff time delays (t_{del_OFF}) and leading-edge blanking result in a higher peak current (I_{pk}) than the programmed threshold (I_{pk_th}), as shown in Fig. 43. With the constant-OFF-time technique, any current disturbance dies out in one cycle and the current loop is inherently stable. When the capacitors are fully recharged, the converter operates in the discontinuous-conduction mode (DCM).

In continuous-conduction mode (CCM), for example at the beginning of recharge, I_{pk_th} and t_{off_CONT} always define I_{pk_min} as shown in Fig. 44.

The PFM technique provides high efficiency as shown in Fig. 45. The duration of the sleep interval depends mainly on leakage currents.

Hysteretic control means that an output-voltage ripple is regulated. This is acceptable since only a capacitor bank is at the output. The amount of ripple should be high enough to prevent any erratic behavior related to the capacitors' ESR.

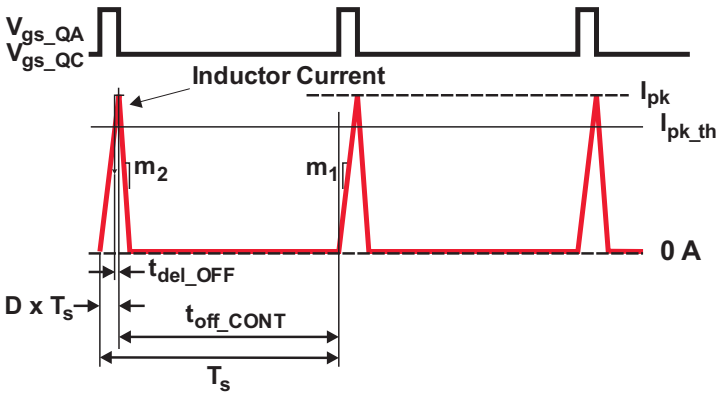


Fig. 43. Discontinuous peak-current operation in recharge mode.

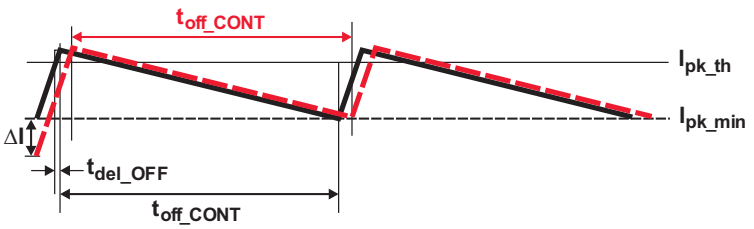


Fig. 44. Peak-current mode with current perturbation.

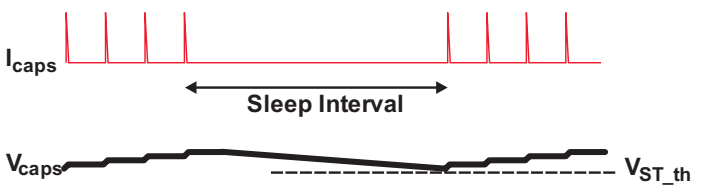


Fig. 45. PFM operation in recharge mode.

The total recharge time can be estimated with the equation

$$t_{rech\_tot} \approx \frac{E_{C\_final}}{E_L} \times \left(\frac{I_{pk\_th} \times L}{V_{bus}} + t_{off\_CONT} + t_{del\_OFF} \right), \quad (28)$$

where

$$E_{C\_final} = \frac{1}{2} C_{storage} \times V^2_{storageF} \quad (29)$$

is the final storage energy, $V_{storageF}$ is the final $V_{storage}$, and the minimum energy transferred per cycle is

$$E_L = \frac{1}{2} L \times I^2_{pk\_th}. \quad (30)$$

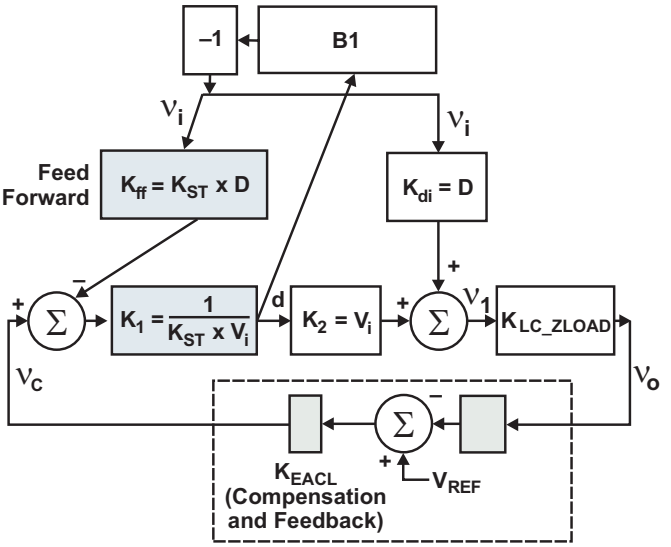
The leakage currents and the conversion efficiency are neglected but should be in the equation if significant. I_{pk_th} is used instead of I_{pk} since t_{del_OFF} is hard to predict. In reality, E_L is higher, which reduces the recharge time. Also, at the beginning of the recharge, the converter operates in CCM so that the recharge is faster. It operates in DCM as soon as

$$\frac{L \times I_{pk}}{V_{storage}} < t_{off\_CONT}. \quad (31)$$

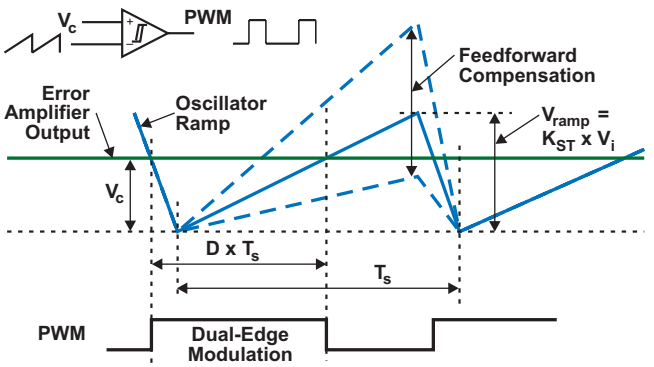
Holdup-Mode Control-Loop Design Considerations

The buck power supply is a pulse-width-modulation (PWM) fixed-frequency, voltage-mode-control type. A small-signal representation of the control model in CCM is shown in Fig. 46. In this model, V_i and D are the buck input DC voltage and the steady-state duty cycle; ν_i, d, ν_o, and ν_1 are small-signal variations; and K_{LC_ZLOAD} represents the output LC filter with load impedance. B1 represents the impact of the duty-cycle variation, d, on the input voltage, v_i, of the buck power supply. Note that B1 is greatly influenced by the input-network impedance, which in this case, includes the storage-bank capacitance.

The output voltage of a voltage-mode-control buck is $V_o = D \times V_i$ and its small-signal variation is proportional to $(d \times V_i) + (D \times \nu_i)$. Blocks K_2 and K_{di} show this relationship and how the small-signal behaviour is affected by V_i and ν_i. The feed-forward effect shown with block K_{ff} (which



a. Buck voltage-mode-control model in CCM.



b. Oscillator ramp and PWM signals.

Fig. 46. Small-signal control model in CCM.

cancels K_{di}), and block K_1 (which cancels K_2), ensures that the loop gain stays independent of the input voltage. This is particularly important since the storage capacitors' voltage changes considerably during a holdup event.

In order to compensate for the double poles inherent in voltage-mode control, a type III compensation network (Fig. 47), which provides two zeros, is required. The double-pole frequency is

$$f_{dp} = \frac{1}{2\pi\sqrt{L \times C_b}}. \quad (32)$$

It is also important to pay attention to the zero introduced by the ESR of the bus capacitor (mostly R_d as shown in Fig. 37). Its frequency is

$$f_{Z\_cap} = \frac{1}{2\pi \times R_d \times C_b}. \quad (33)$$

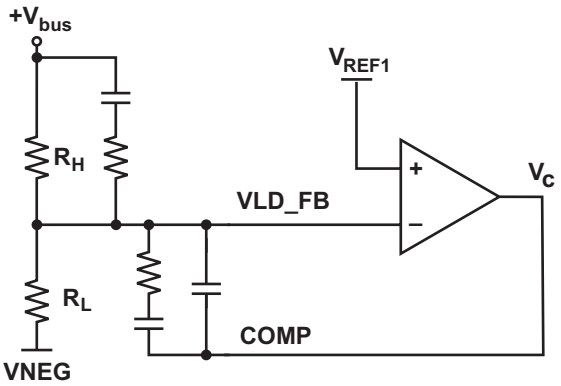


Fig. 47. With type III compensation.

If the effect of V_{fA} and V_{fC} is neglected, the overall open-loop gain is shown by Equation (34) below, where K_{ST} is the feedforward factor defining the ramp amplitude from $V_{storage}$, and $K_{EACL}(s)$ is the compensator gain. The output impedance is

$$Z_{out}(s) = \frac{1}{\frac{K_{EACL}(s)}{K_{ST} \times L \times s} + \frac{1}{Z_{load}(s)} + \frac{1}{L \times s}}, \quad (35)$$

where $Z_{load}(s)$ is the total impedance seen by the inductance, mainly the bus capacitance in parallel with the load, and $s = j\omega$, which is based on the Laplace Transform function.

The previous equations (in Section III.B) are applicable to CCM. If DCM is used and the effect of V_{fA} and V_{fC} is neglected, the duty-cycle equations then become as follows.

- MOSFET conduction:

$$D_{MOSFET\_DM} = \sqrt{\frac{2 \times L \times P_{load} \times f_s}{\left(V_{storage} - V_{bus}\right) \times V_{storage}}}, \quad (36)$$

where P_{load} is the load power.

- Diode conduction: (See Equation (37) below.)
- Off period:

$$D_{3\_DM} = 1 - D_{MOSFET\_DM} - D_{DIODE\_DM} \quad (38)$$

The critical load power below which the converter operates in DCM is

$$P_{crit} = \frac{V_{bus}^2 \times \left(V_{storage} - V_{bus}\right)}{2 \times L \times V_{storage} \times f_s}. \quad (39)$$

IV. Design Example: –48-V HVES Application for ATCA Using the TPS2355

A. Basic Design Overview

To illustrate the design of an HVES system (see Fig. 48), a –48-V bus application has been selected. The design requirements are (see Fig. 19):

- Power output = 250 W maximum constant-power load
- t_{holdup} = 9.3 ms
- V_{bus_min} = 44 V, V_{bus_max} = 72 V
- V_{load_min} = 38 V
- V_{holdup} = 40.5 V ± 1.5 V
- Storage voltage = 87.8 V ± 4%
- Bus capacitance (C7) = 100 µF with 0.1 to 0.25-Ω ESR (including R20)
- f_s = 300 kHz ±15%

If a 25% ripple factor (K_{rip}) at 87.8 V is assumed, the inductance calculation becomes

$$L = \frac{47.8\% \times \left(87.8\,V - 40.5\,V - 1.3\,V\right)}{300\,kHz \times 1.543\,A} \approx 47\,\mu H \quad (40)$$

where the peak-to-peak ripple is defined as

$$I_{rip\_pkpk} = K_{rip} \times \frac{P_o}{V_{bus}} = 25\% \times \frac{250\,W}{40.5\,V} = 1.543\,A \quad (41)$$

$$G_{VOL}(s) = K_{EACL}(s) \times \frac{K_{LC}(s) \times K_1 \times \left(K_2 - K_{di} \times B_1(s)\right)}{1 - K_1 \times K_{ff} \times B_1(s)} = K_{EACL}(s) \times \frac{K_{LC}(s)}{K_{ST}} \quad (34)$$

$$D_{DIODE\_DM} = \frac{-D_{MOSFET\_DM} + \sqrt{D_{MOSFET\_DM}^2 + \frac{8 \times L \times P_{load} \times f_s}{V_{bus}^2}}}{2} \quad (37)$$

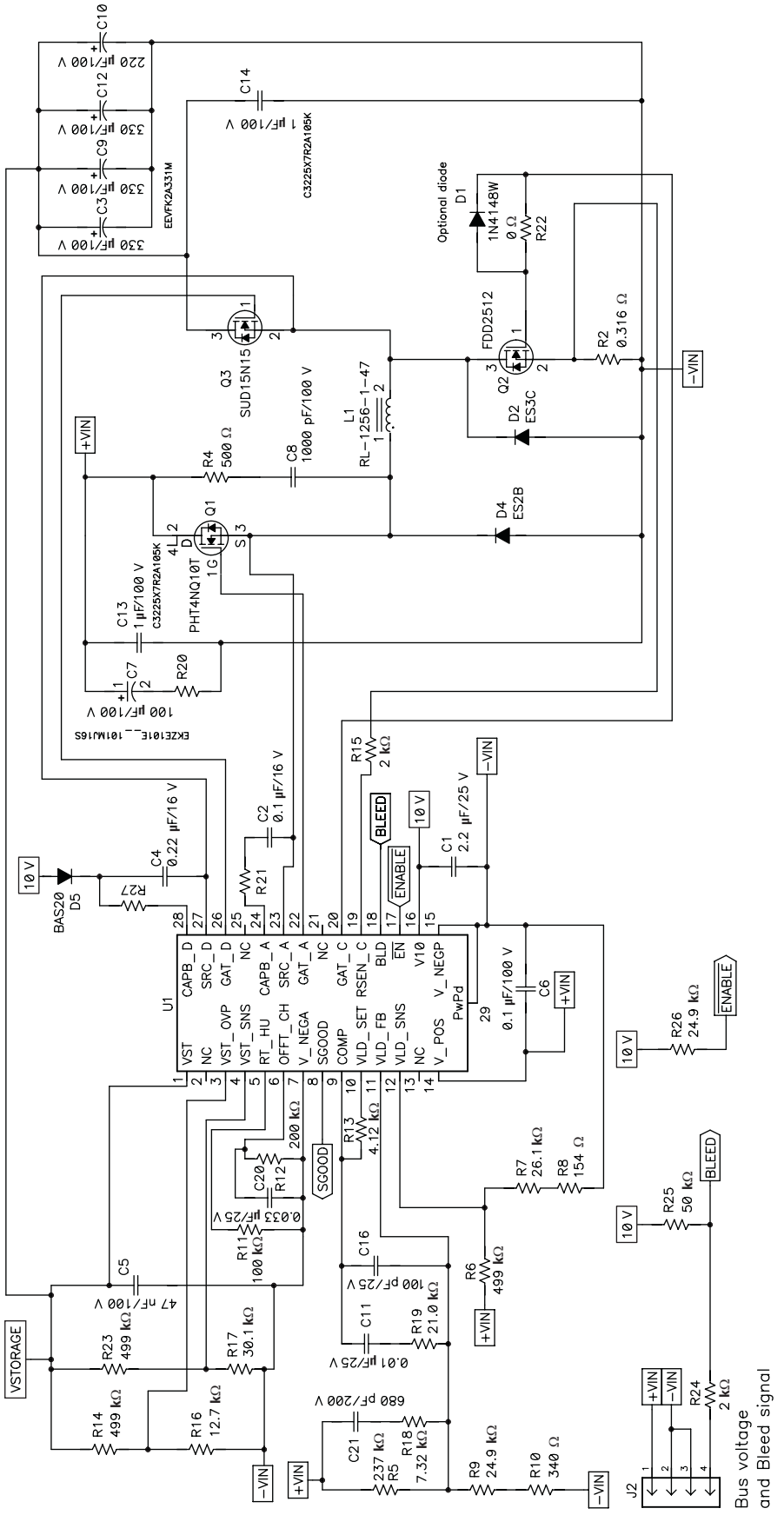
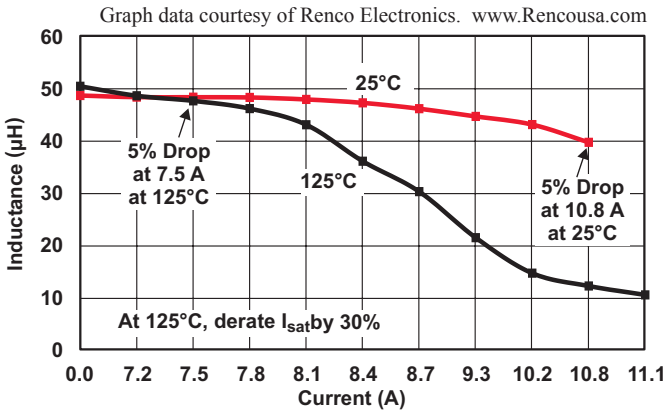
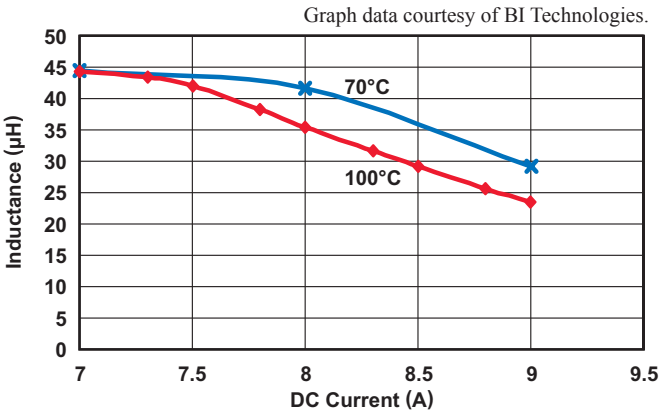


Fig. 48. Example of HVES system for a –48-V/250-W bus application.



a. Renco RL-1256-1-47



b. BI Technologies HM00-A7802LFTR

Fig. 49. Inductor saturation characteristics.

For 250 W, the Renco RL-1256-1-47 is selected to provide a margin against saturation at high temperature and high $V_{storage}$.

$$I_{L\_pk(max\_1)} \approx \frac{250\,W}{40.5\,V} + \frac{1}{2} \times \frac{(40.5\,V + 1.6\,V) \times (1 - 45.4\%)}{47\,\mu H \times 255\,kHz} = 7.13\,A \quad (42)$$

The BI Technologies HM00-A7802LFTR is another alternative. See Fig. 49.

Note that if a standard 200-W ATCA is needed, the small surface-mount Coilcraft DO-5040H-473 is a possibility, depending on the maximum temperature (see Figs. 25, 26, and 28) and the storage voltage. However, for a 250-W output, the power losses are as shown in Figs. 20, 21, 29, and 33. Equation (43) shows the typical core loss for the Renco RL-1256-1-47 from 100 kHz to 500 kHz. If the maximum gate charge, a high temperature, 80 V, and 0.47-A and 0.27-A gate-drive currents are assumed, Equations (44) through (46) apply.

$$P_{core} = 0.1436 \times \left(f_s^{1.63}\right) \times \left(0.1262456 \times I_{rip\_pkpk}\right)^{2.62} = 26\,mW \text{ at } 300\,kHz, \quad (43)$$

where P_{core} is in mW, f_s is in kHz, and I_{rip_pkpk} is in A.

$$P_{QD\_SW} \approx \frac{300\,kHz \times 80\,V}{2} \times \left\{\left[\left(\frac{6.895\,A}{0.47\,A} + \frac{5.45\,A}{0.27\,A}\right) \times (8.75\,nC + 5\,nC)\right] + 45\,pF \times 80\,V\right\} = 5.794\,W \quad (44)$$

$$P_{gdrv} = 300\,kHz \times \left(40.5\,V \times 25\,nC + \frac{1}{2} \times 8.75\,nC \times 80\,V\right) = 0.409\,W, \quad (45)$$

$$P_{rr\_tot} = f_s \times V_{storage} \times I_{fC} \times t_{T\_ES3C} \times e^{-\sqrt{\frac{Q_{gs2D}}{t_{T\_ES3C} \times I_{G\_on}}}} \quad (46)$$

$$\approx 300\,kHz \times 80\,V \times 5.45\,A \times 39.9\,ns \times e^{-\sqrt{\frac{5\,nC}{39.9\,ns \times 0.27\,A}}} = 2.64\,W.$$

B. Simulation Results

Following is a summary of the buck feedback loop design. Graphs of predicted performance (operation in CCM) are shown in Figs. 50–52.

The double-pole nominal frequency of the LC filter is

$$f_{dp\_nom} = \frac{1}{2\pi\sqrt{L \times C_b}} = \frac{1}{2\pi\sqrt{47\,\mu H \times 100\,\mu F}} = 2.32\,kHz. \quad (47)$$

The bus capacitor's zero frequency changes with its series resistor:

$$f_{Z\_cap(100\,m\Omega\ ESR)} = \frac{1}{2\pi \times R_d \times C_b} = \frac{1}{2\pi \times 0.1\Omega \times 100\,\mu F} = 15.91\,kHz \quad (48)$$

$$f_{Z\_cap(250\,m\Omega\ ESR)} = \frac{1}{2\pi \times 0.25\Omega \times 100\,\mu F} = 6.36\,kHz \quad (49)$$

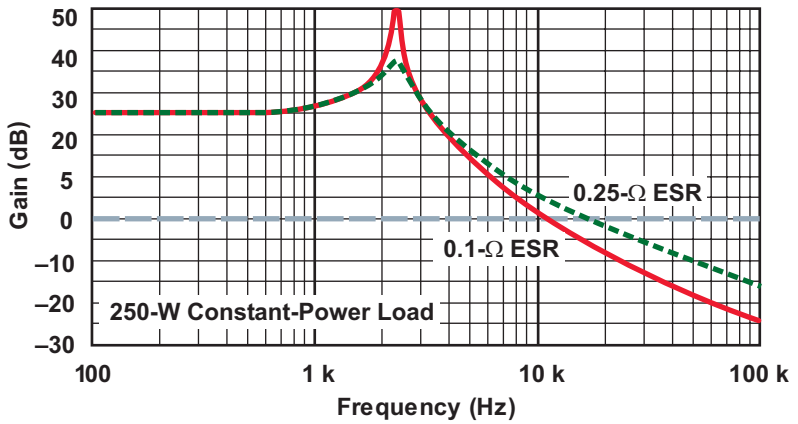
The compensation poles and zeros are as follows:

$$f_z = \frac{1}{2\pi \times R19 \times C11} = 758\,Hz \quad (50a)$$

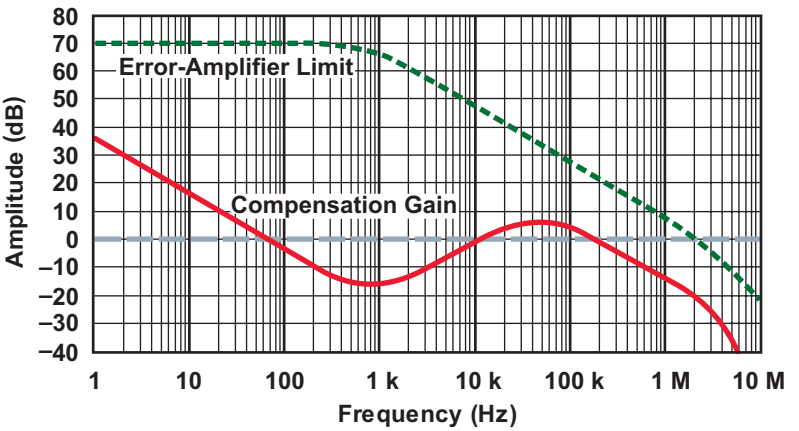
$$f_p = \frac{C11 + C16}{2\pi \times R19 \times C11 \times C16} = 76.55\,kHz \quad (50b)$$

$$f_{zi} = \frac{1}{2\pi \times (R5 + R18) \times C21} = 958\,Hz \quad (51a)$$

$$f_{pi} = \frac{1}{2\pi \times R18 \times C21} = 31.974\,kHz \quad (51b)$$

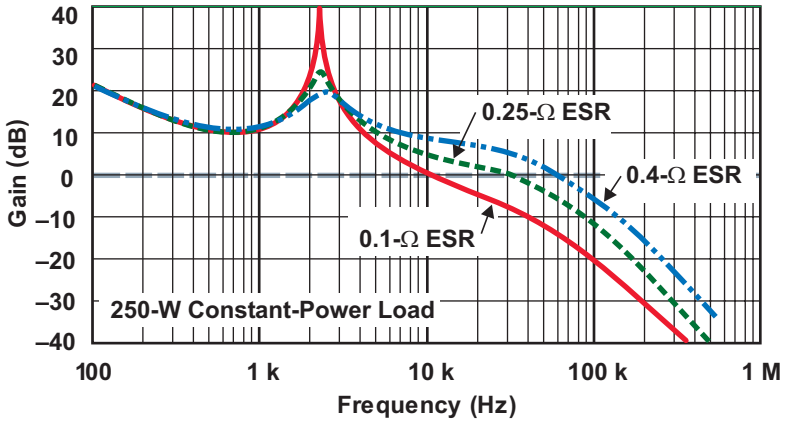


a. Power stage and PWM gain.

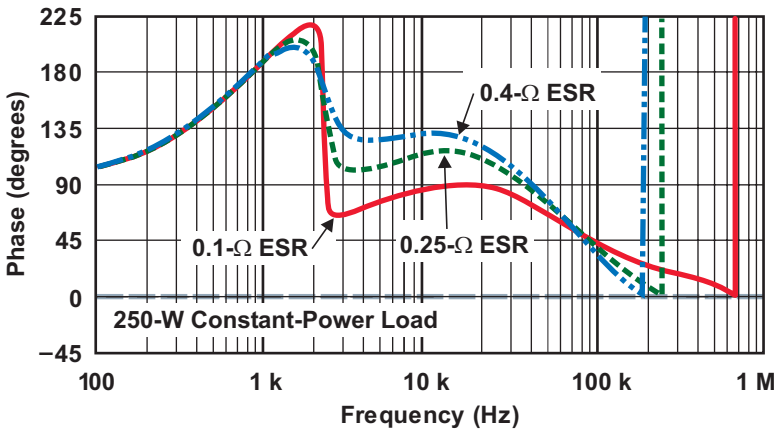


b. Compensation-amplifier gain.

Fig. 50. Bode plots of system frequency response.



a. System loop gain.



b. System loop phase margin.

Fig. 51. Typical system open-loop gain and phase shows effects of capacitor's high ESR of up to 0.4 Ω.

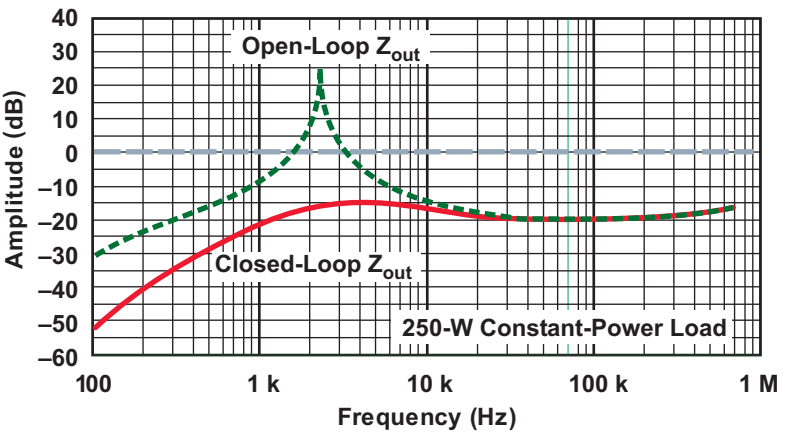


Fig. 52. Typical output impedance with 0.1-Ω C_b ESR and 250-W constant-power load.

Simulations have been performed on a large-signal average model operating in both CCM and DCM. An examples of HVES-system behavior during holdup is shown in Fig. 53.

C. Test Results

The HVES system discussed has been built and tested. Fig. 54 shows the transient response during a holdup event. The response matches well with the predictions in Fig. 53. The duty-cycle preset provides a quick response at the beginning of holdup. See Appendix A for more details.

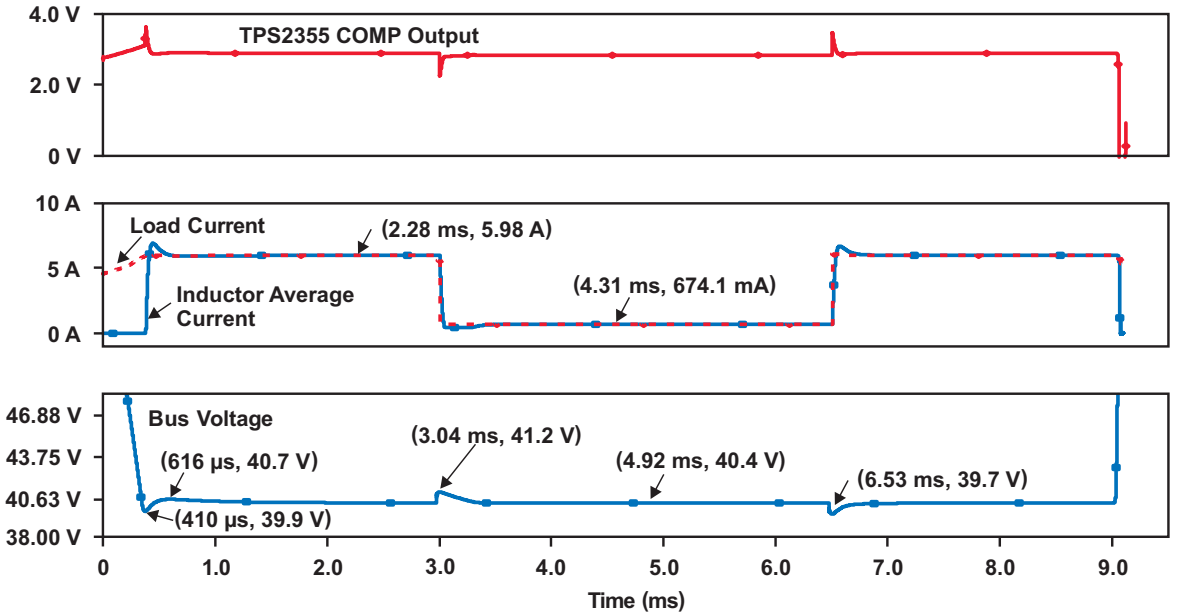


Fig. 53. HVES-system simulation results: buck response with load pulsed between 241 and 27.5 W.

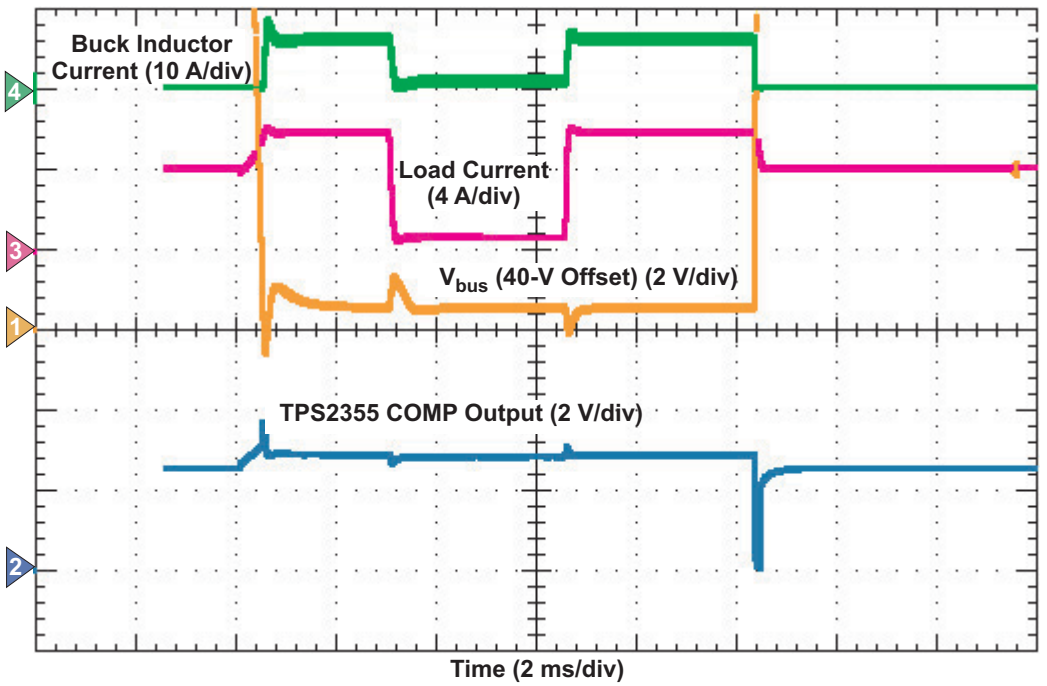


Fig. 54. Transient response of HVES system during holdup. Test used the TI TPS2355, and power load pulsed between 241 and 27.5 W.

Fig. 55 shows the recharge cycle of the storage-capacitor bank when starting from 0 V. Adaptive soft start is used for adequate inrush current control and the capacitor's short-circuit protection. As shown in the expanded-time insets, when $V_{storage}$ is very low, the peak-current threshold (I_{pk_th}) is substantially reduced and the off time (t_{off_CONT}) has increased.

V. Conclusion

The design of an HVES system is complex and requires a broad knowledge of power supplies. This topic has presented the basics. More details are provided in Appendix A.

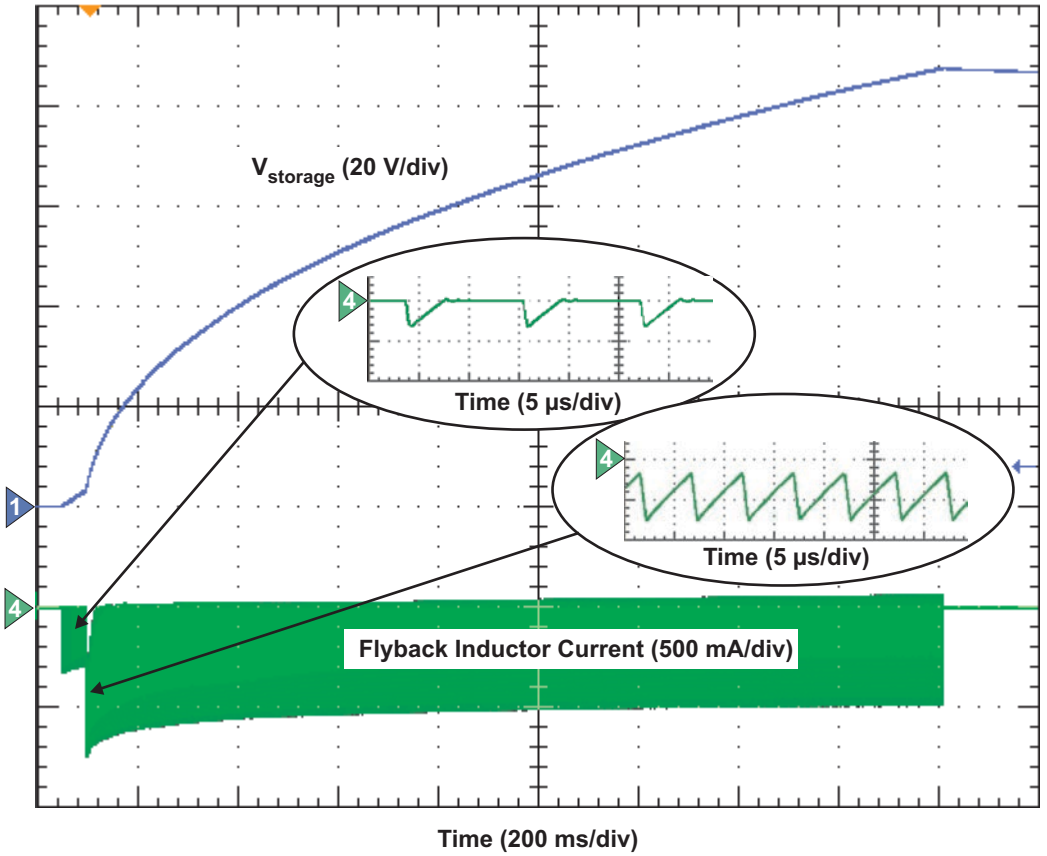


Fig. 55. HVES system capacitor recharge cycle with adaptive soft start. Test used the TPS2355 with V_{IN} = 44 V.

VI. References

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I. Description of the Problem

During recharge mode, the holdup error amplifier system loop is not closed, which means the normal speed of its reaction to a holdup event will be inadequate. Fig. 56 shows what happens in such circumstances—the bus voltage goes down to 27 V before slowly rising up to 40.5 V.

II. The Duty-Cycle Preset Solution

The transient response at the beginning of holdup is critical. One characteristic of a buck topology operating with voltage-mode control and feedforward is that the output of the voltage-loop error amplifier directly defines the operating duty cycle. This can be used to achieve immediate response to a holdup event by presetting the error-amplifier output while in the recharge mode. Fig. 57 shows a possible implementation of this function.

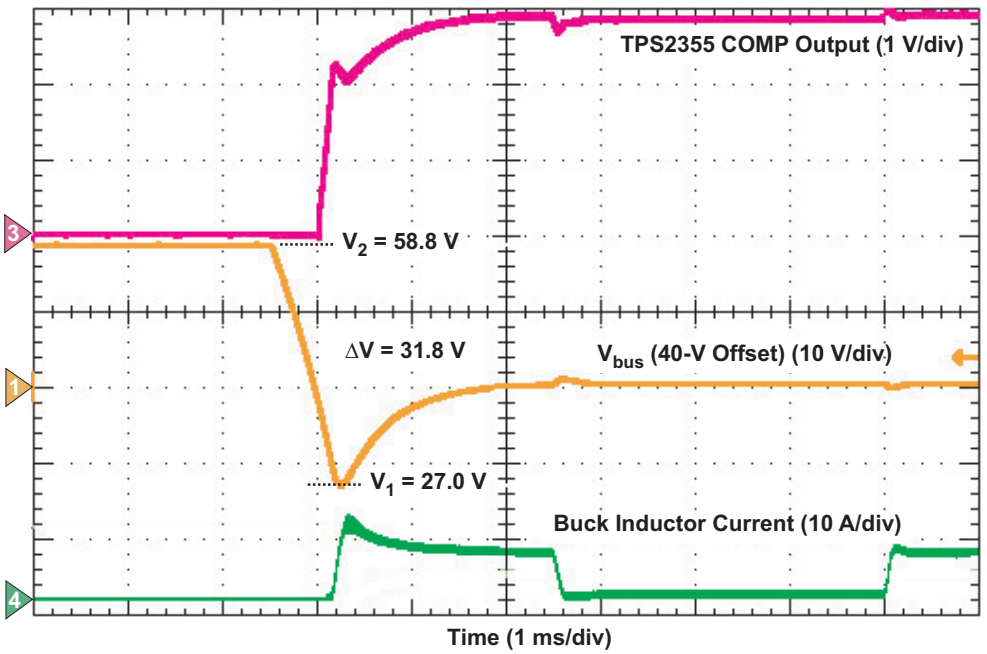


Fig. 56. Reaction of HVES system if there is no duty-cycle preset function. Test used the TI TPS2355 with R13 uninstalled, $V_{storage}$ = 60 V, and power load pulsed between 241 and 27.5 W.

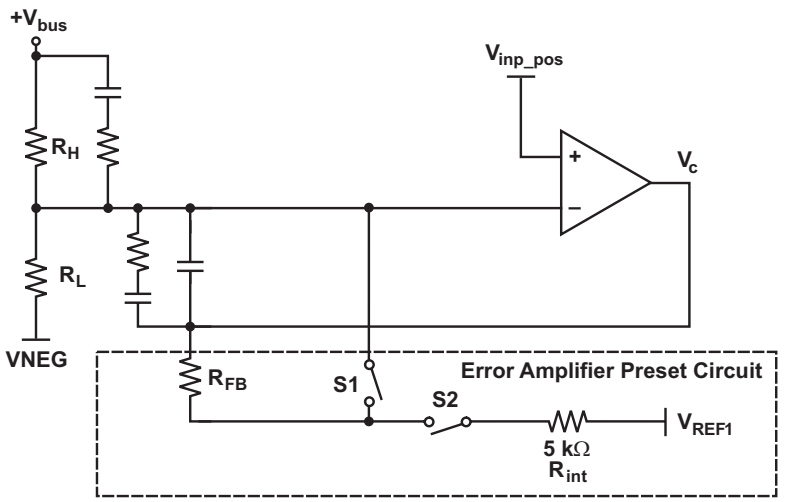


Fig. 57. Duty-cycle preset circuit.

During recharge mode, switches S1 and S2 are closed, so that the amplifier behaves like an inverter with a gain defined by R_{int} and R_{FB}. During that time, the compensation capacitors are precharged for a fast holdup response. This DC feedback is disconnected as soon as the holdup mode begins.

The equation defining the offset injected by the duty-cycle preset circuit (see Fig. 57) is Equation (52) below.

The preset voltage provided by the error amplifier is defined independently from the storage voltage, but it follows the state of the bus voltage. For example, if $V_{bus_}$preset = 40.5 V, R_{int} = 5 kΩ, R_H = 237 kΩ, R_L = 25.24 kΩ, V_{REF1} = 5 V, R_{FB} = 4.53 kΩ and V_{inp_pos} = 3.9 V, then V_c = 2.904 V. If V_{bus_preset} = 42 V and R_{FB} = 4.12 kΩ, then V_c = 2.968 V.

On the other hand, because of the feedforward, the required voltage at V_c is constant whatever $V_{storage}$ may be. This is useful when multiple successive holdup events occur, in which case the storage voltage does not have time to reach its final recharge value before the next holdup event. For example, if $V_{storage}$ nominal is 88 V,

$$D = \frac{V_{bus\_preset} + V_{fA} + V_{fC}}{V_{storage} + V_{fC} - V_{QD}} \approx \frac{42\,V + 1.6\,V}{88\,V + 0.3\,V} = 49.37\%. \quad (53)$$

The ramp peak-to-peak voltage is 5 V, and V_{c_req} = (49.37% × 5 V) + 0.5 V = 2.968 V, where 0.5 V is the ramp offset. If $V_{storage}$ has decreased and is still at 55 V when the next holdup happens,

$$D \approx \frac{42\,V + 1.6\,V}{55\,V + 0.3\,V} = 78.84\%. \quad (54)$$

The ramp peak-to-peak voltage is 5 V × 55/88 = 3.125 V, and V_{c_req} = (78.84% × 3.125 V) + 0.5 V = 2.964 V.

In the duty-cycle equation, V_{bus_preset} represents the target bus voltage for which the error amplifier gets preset during recharge mode. V_{bus_preset} does not have to be exactly equal to V_{bus}, and it may be slightly higher. This helps to mitigate the first V_{bus} undershoot (at the beginning of holdup), which is influenced by circuit parameters that can vary with device manufacturing tolerances, temperature, and age. However, the V_{bus_preset} voltage selection represents a trade-off because a higher voltage can increase the first overshoot. In the duty-cycle calculation, 42 V was selected, although a different value could be used.

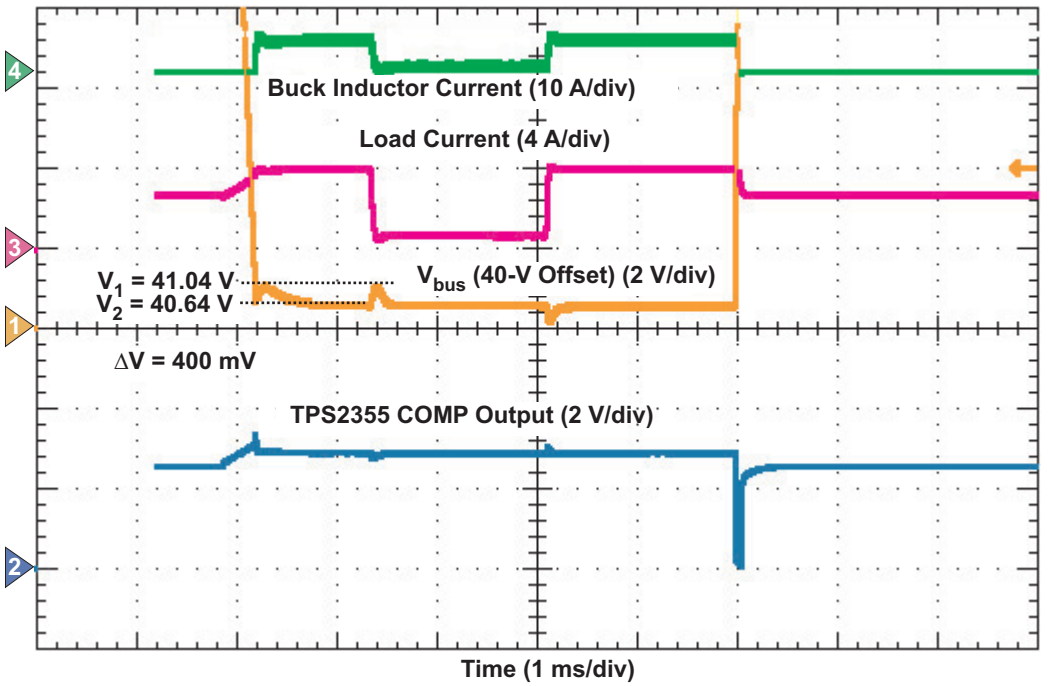
Equation (55) below defines R_{FB}. Note that R_{FB} corresponds to R13 in the schematic of Fig. 48.

III. Test Results

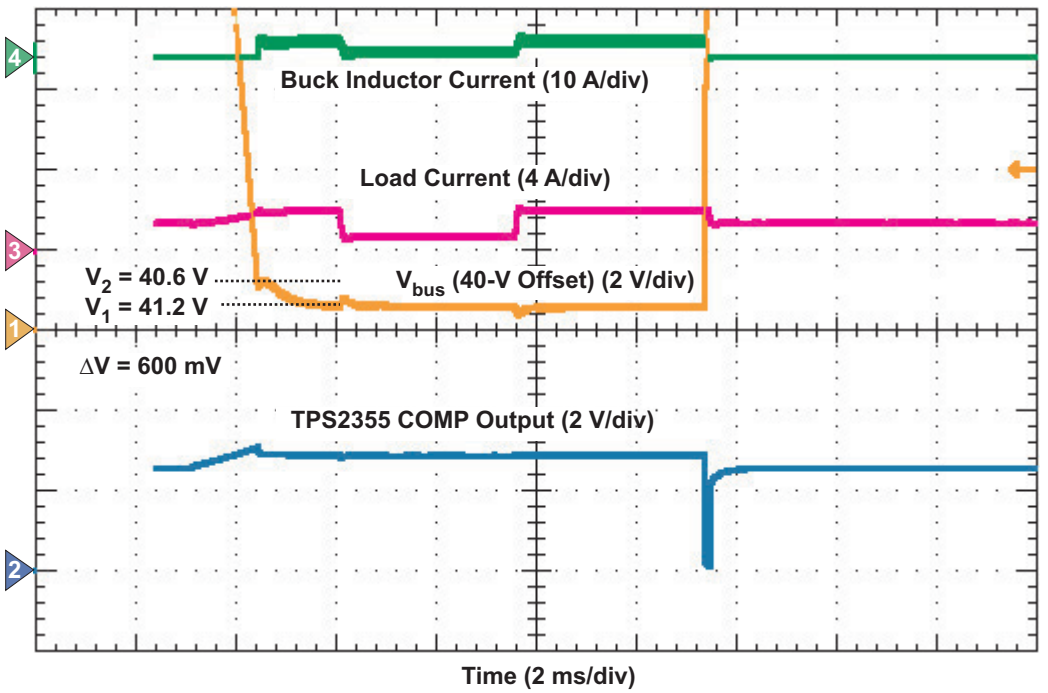
A comparison between Figs. 55 and 56 shows the effect of using the duty-cycle preset function. Figs. 58 and 59 show the performance of the duty-cycle preset function with different R13 (R_{FB}) values.

$$V_c = R_{FB} \times \left[V_{inp\_pos} \times \left(\frac{1}{R_H} + \frac{1}{R_L} + \frac{1}{R_{int}} + \frac{1}{R_{FB}} \right) - \frac{V_{bus\_preset}}{R_H} - \frac{V_{REF1}}{R_{int}} \right]. \quad (52)$$

$$R_{FB} = \frac{V_{c\_req} - V_{inp\_pos}}{V_{inp\_pos} \times \left(\frac{1}{R_H} + \frac{1}{R_L} + \frac{1}{R_{int}} \right) - \frac{V_{bus\_preset}}{R_H} - \frac{V_{REF1}}{R_{int}}} \quad (55)$$

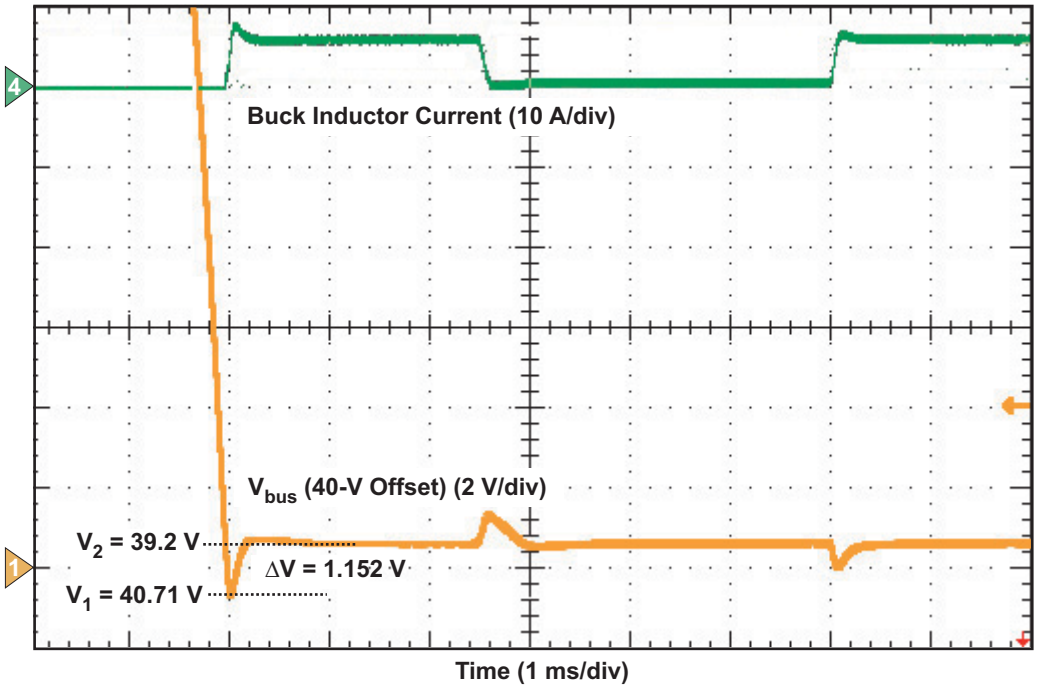


a. Power load pulsed between 161 and 27.5 W.

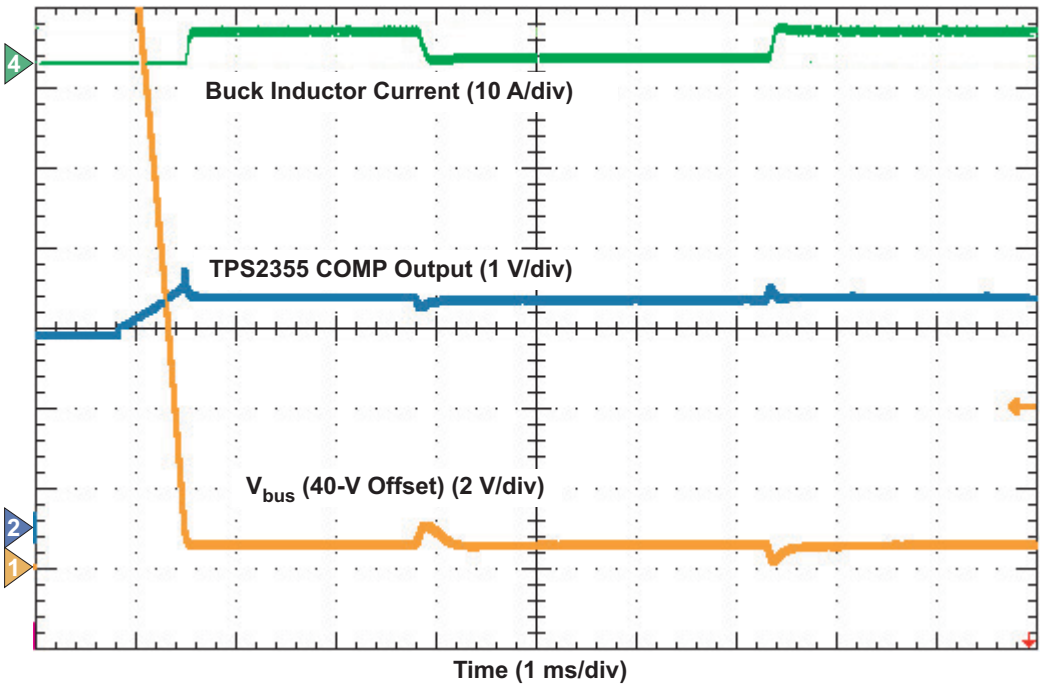


b. Power load pulsed between 81 and 27.5 W.

Fig. 58. Reaction of HVES system with duty-cycle preset function when test used the TI TPS2355 with R13 = 4.12 kΩ.



a. Power load pulsed between 241 and 27.5 W.



b. Power load pulsed between 161 and 27.5 W.

Fig. 59. Reaction of HVES system with duty-cycle preset function when test used the TI TPS2355 with R13 = 4.5 kΩ.