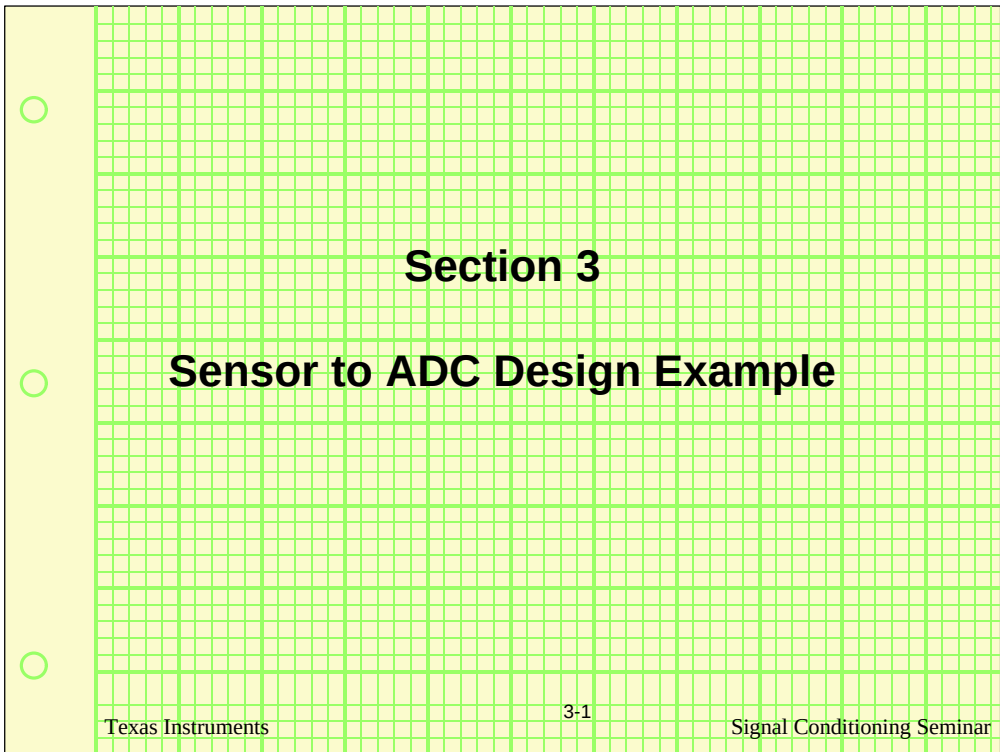
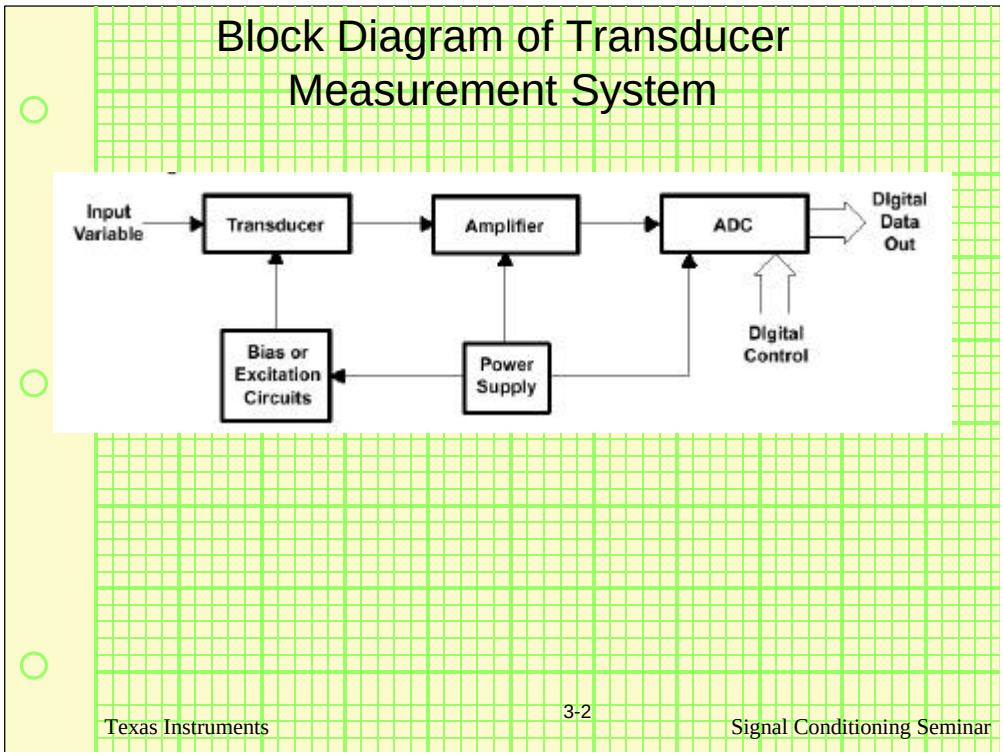
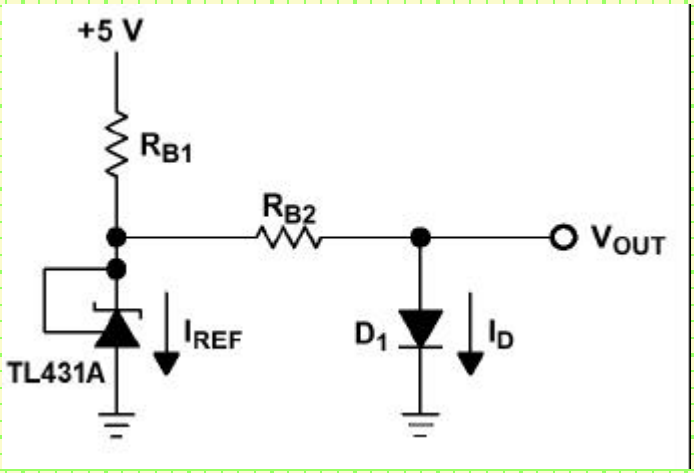


This section describes the design of a sensor to ADC system. The sensor measures temperature, and the measurement is interfaced into an ADC selected by the systems engineering department.



The temperature sensor (transducer) must be excited with a bias to perform per the specification. As is often the case, the bias comes from a reference circuit which supplies reference voltages for the system. The ADC is selected prior to this design, and because we can not modify the selection, we just work with it. The amplifier is designed last because it is the interface between the sensor and ADC.

Transducer Considerations
Reference and Bias Circuit



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A shunt diode was chosen as the reference because it can do the job at the least cost. More accurate references exist, and we would like to sell them to you because they cost more, but they are not justified but the accuracy requirements of this design. R_{B1} is selected to supply the reference and temperature sensing diode current. R_{B2} is selected to limit the diode current to the specification value, and worst case calculations show that the diode current is always within specification. The reference output voltage also acts as a bias voltage for the op amp, but this current is negligible so it isn't considered here.

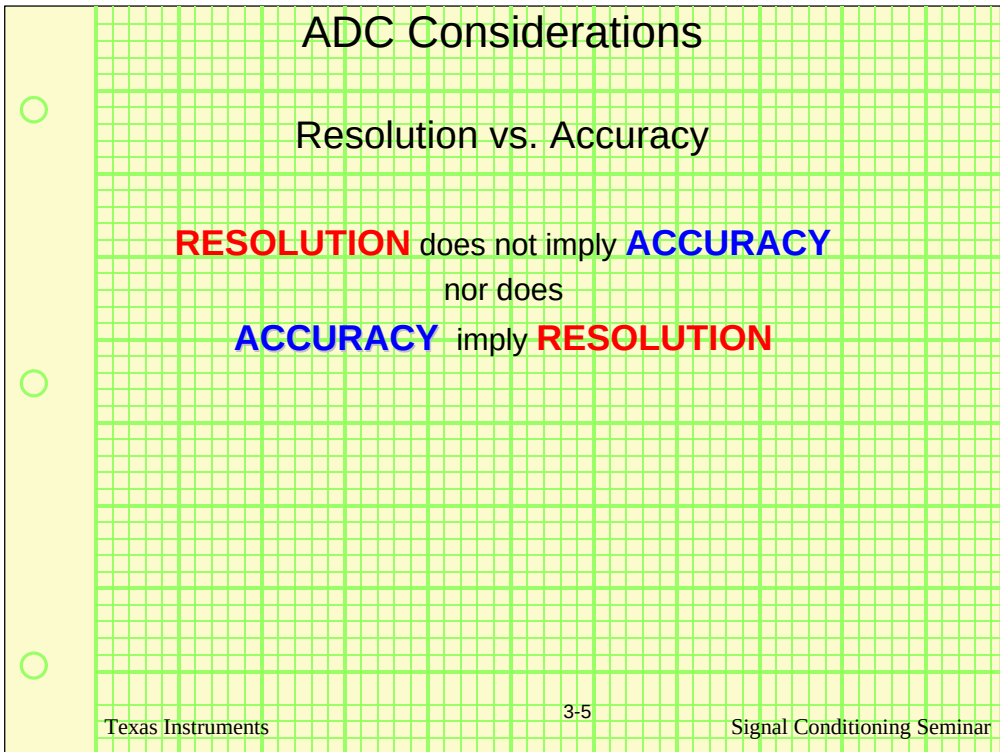
Transducer Output Voltage

- Transducer specifications
- Transducer bias

$$R_D = \frac{26}{I\,(ma)} = \frac{26}{2} = 13\ \Omega$$

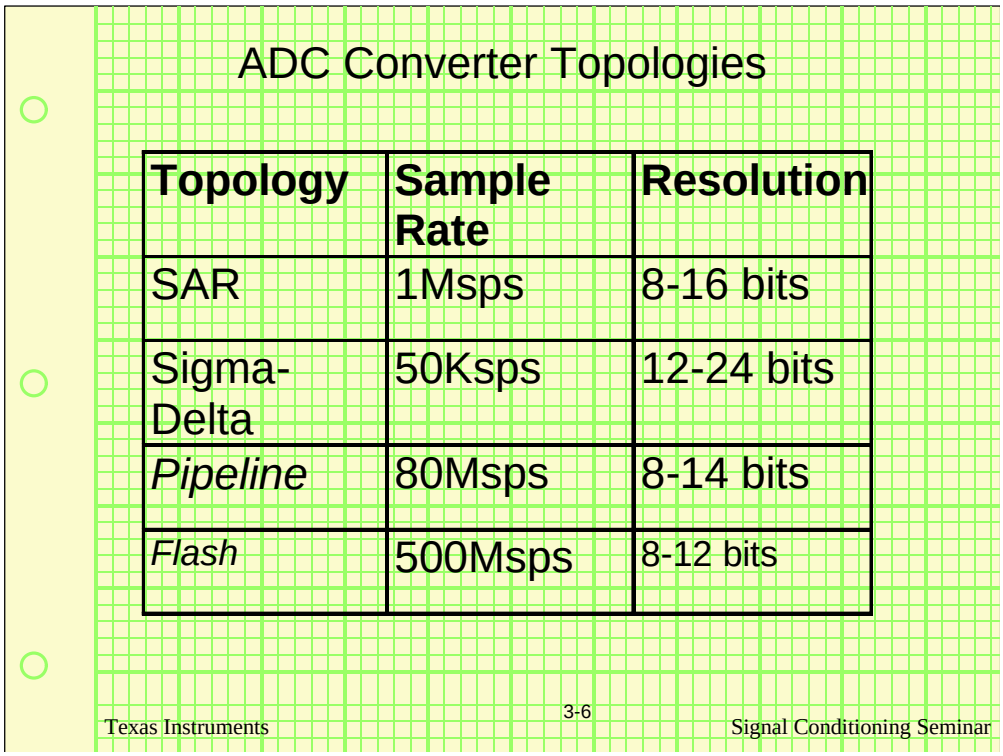
TRANSDUCER TEMPERATURE	TRANSDUCER OUTPUT VOLTAGE	ANALOG INTERFACE AMPLIFIER INPUT VOLTAGE
–25°C	650 mV	V_{IN1} = 650 mV
25°C	550 mV	550 mV
100°C	400 mV	V_{IN2} = 400 mV

When the temperature transducer is biased correctly it yields the temperature/voltage relationship shown in the table. There is an error term that is not accounted for in the table, but it does not enter into the design at this point because the error is adjusted out in the final circuit. Correct bias insures that the transducer meets its specifications, so the design meets specification. The transducer output resistance can form a voltage divider with the amplifier's input resistance, thus it is calculated here as a parameter to be used in the op amp selection.



The selection of the ADC involves several factors. These factors are often system rather than circuit design concerns because the ADC may be used for several applications within a design by multiplexing. The design type determines if missing codes are allowable and what degree of monotonicity is required. System specifications identify the required accuracy, and the circuit must conform to the system specifications.

The interface decision, serial or parallel, is dependent on the processor or logic rather than circuit restraints. Parallel interfaces are faster but they require lots of interface lines, while serial interfaces are slower with fewer interface lines. Internal references are generally preferred to reduce component count, but external references have higher precision.



Resolution and accuracy are not identical. An ADC may have 16 bits resolution, i.e. the output can be resolved into 2^{16} bits, but the ADC or circuit accuracy may be much less than the resolution because internal or external error sources. An example is illustrated by the equivalent number of bits formula. The ADC may be advertised as 12 bits, but at the actual operating frequency it may be accurate to 10 bits.

The Input During Conversion

Consider an ADC without a S/H amplifier

Maximum frequency sine wave can be accurately digitized?

Input signal $e_{in}(t) = \frac{E_{FS}}{2}\sin(2\pi ft)$

Slew Rate $\frac{de_{in}}{dt} = 2\pi f \frac{E_{FS}}{2}\cos(2\pi ft)$

Max SR at cos=1 $f = \frac{\frac{de_{in}}{dt}}{\pi E_{FS}}$

In terms of ADC $f = \frac{\frac{1}{2}LSB}{\pi T(2^N LSB)}$

12 bit, 1µsec ADC $f = \frac{1}{\pi 2^{12+1}(1\mu sec)} = 38.9Hz$

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There are many different methods of constructing an ADC. The SAR converter initially assumes a midscale value and does a loop calculation to determine the value of each bit. This type converter is accurate but slow because it requires n-bit loop calculations to produce an n-bit ADC. The sigma delta ADC has an integrating feedback loop that drives errors to zero if enough calculations are made. Typically the sigma delta ADC is the slowest ADC because it over samples by such a large margin, but it is the most accurate ADC.

A flash converter consists of a string of comparators with an input of each comparator connected to a resistive voltage divider fed by a precision voltage reference. The input voltage is connected to the other comparator inputs, so the output of the comparators is low until the input voltage equals the reference voltage where the output voltage goes high. This type of flash ADC has no protection features, and it requires 2^{n-1} comparators. A pipeline converter contains a small flash converter, and it applies the flash converter to the input signal in steps. Each step yields part of the output solution, so the answer comes out in pipeline form. A flash is the fastest ADC and the pipeline is the next fastest ADC.

ADC Characteristics

- System Engineer Selected: TLV2544
- Rin = 20 kW
- VOS = ± 150 mV
- Drift = 800 ppm
- Sampling Frequency = 100 kHz

ADC INPUT VOLTAGE	DIGITAL OUTPUT	ANALOG AMPLIFIER OUTPUT VOLTAGE
0 V	000000000000	V_{OUT1} = 0 V
4 V	111111111111	V_{OUT2} = 4 V

The system engineer selected the TLV2544 ADC because it can be multiplexed over meets the system requirements, and it can be used in the single shot mode where the ADC input resistance is 20K. The effective sampling rate after allowing for the multiplexing is 100kHz. The data rate is less than 1Hz, thus because of the high sampling rate a single pole low pass filter serves the anti-aliasing function.

The offset voltage is expressed in mV because it can be adjusted out, but the ADC drift is expressed as bits because it is an error that decreases accuracy. The ADC output voltage range sets the required amplifier input voltage range because the input signal must cover the complete ADC input range to obtain maximum accuracy.

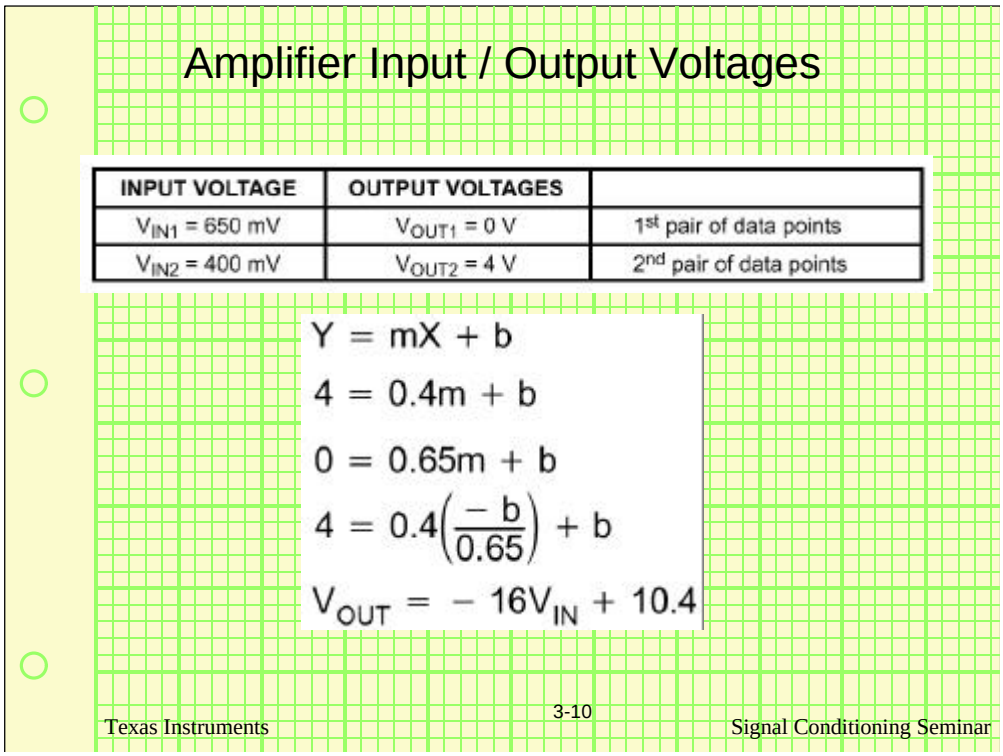
Op Amp Selection

DESIGN SPECIFICATION	ESTIMATED VALUE	CANDIDATE OP AMP: TLV247X
R_{IN}	10^6 (13) Ω	10^{12} Ω
V_T	350 mV to 700 mV	–0.2 V to 5.2 V
R_{OUT}		1.8 Ω
V_{INADC}	0 V to 4 V	0.15 V to 4.85 V
V_{OS}	—	2.2 mV
I_B	—	100 pA
V_N	—	$\frac{28\ nV}{\sqrt{Hz}}$
I_N	—	$\frac{0.39\ pA}{\sqrt{Hz}}$
Analog noise	—	10 mV
k_{SVR}	—	63 dB

The TLV247x is a candidate op amp for the amplifier job, thus its salient specifications are listed in the table. A million times the sensing diode resistance yields an acceptable error from voltage divider action between the diode and op amp input. The op amp has $10^{12}\Omega$ input resistance so divider action is minimal. The transducer output voltage, VT, is 350mV to 700mV, and this range is overlapped by the op amp's input voltage range, hence no error results from this source. The op amp's output resistance is 1.8Ω. This resistance forms a voltage divider with the ADC input resistance (20kΩ), and the voltage divider action is minimal because of the resistances values.

The ADC expects to see an input voltage of 0V to 4V, and the op amp output voltage is guaranteed to span the output voltage range of 0.15V to 4.85V. This problem could be solved by increasing the op amp power supply voltage, by choosing another op amp, or by shifting the ADC input up. None of these solutions are required because the high ADC input resistance enables us to use the nominal value of V_{OL} = 85mV, and the resultant error is acceptable. Offset voltages and currents would not be considered because they can be adjusted out, but they are so small that they add very little error to the design.

The noise specifications for the op amp are excellent but meaningless in this design because the cable noise overshadows them. Power supply noise rejection is acceptable, thus this op amp is selected for the design.

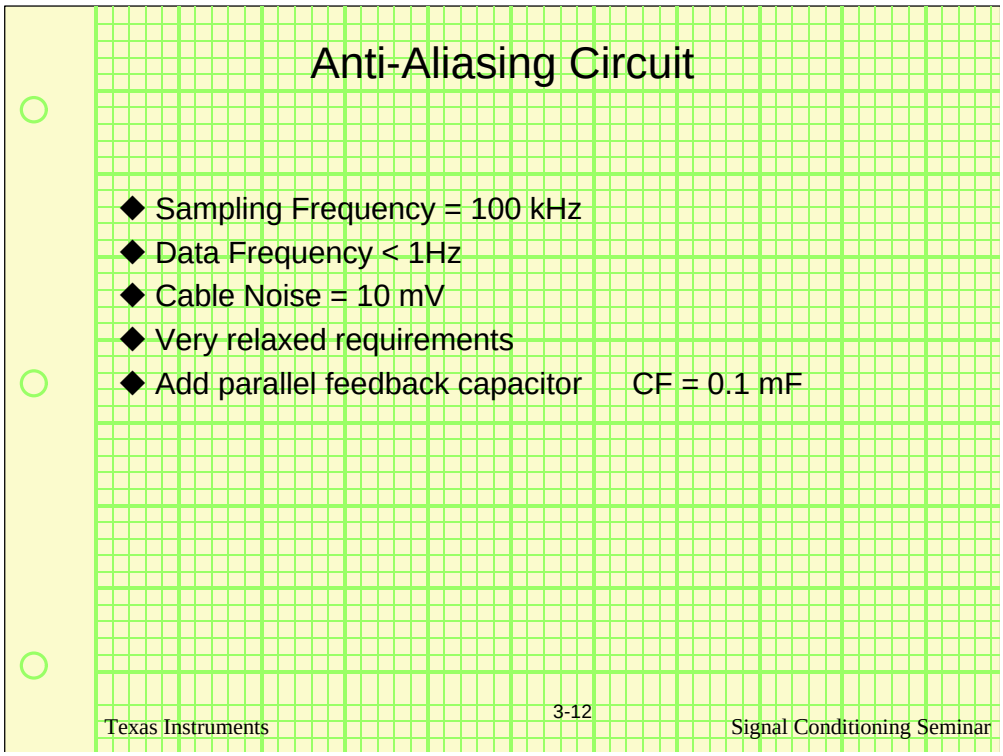


The op amp input voltage (sensor output voltage) and op amp output voltage (ADC input voltage range) are matched up as two data points on a straight line. Then the equation of a straight line and simultaneous equations are employed to obtain the final equation for the op amp. The case three circuit is selected for the design, and component values are calculated as previously shown.

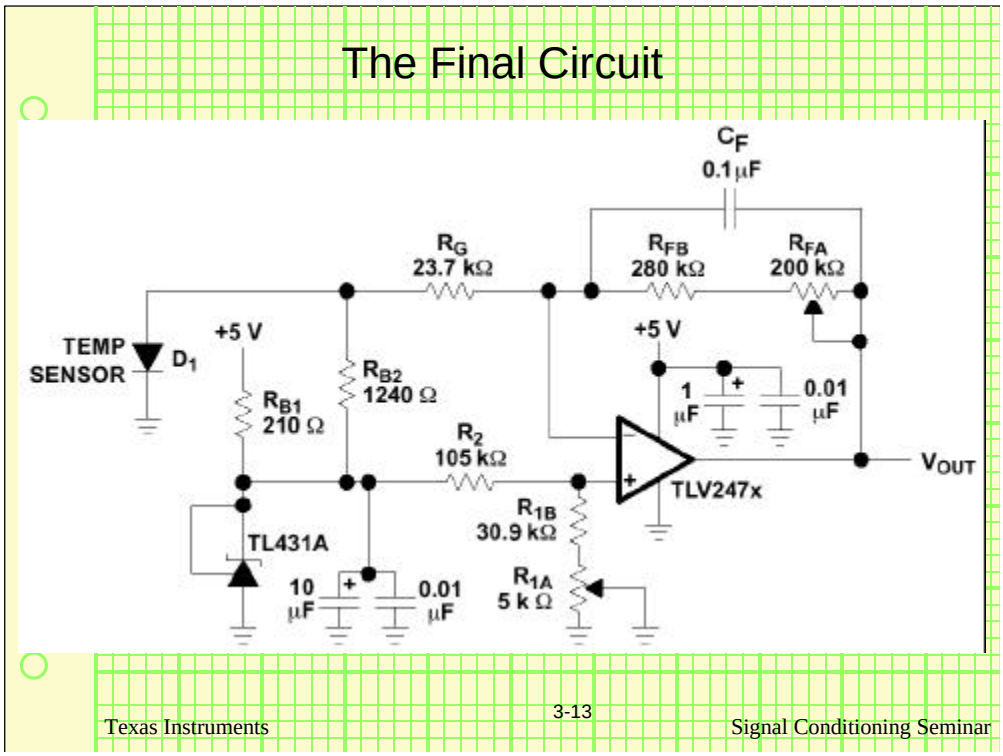
Offset and Gain Error Budget

ERROR PARAMETER	INTERCEPT	GAIN	DRIFT
V_{REF}	±25 mV		
V_{REF} drift			7.41 mV = 8 LSB
Transducer offset		± 50 mV	
Transducer R_{OUT}			13 Ω = 0 LSB
ADC reference		± 150 mV	1 LSB
Total unadjusted ADC error			2 LSB
Gain error		1.6 LSB	
ADC drift			4 LSB
V_{OS} op amp	2.2 mV		
I_B op amp	100 pA		
V_N op amp			$\frac{28\ nV}{\sqrt{Hz}}$ = 1 LSB
I_N op amp			$\frac{139\ pA}{\sqrt{Hz}}$ = 0 LSB
V_{NPS} PS noise			10 mV = 2 LSB
R_{OUT} op amp			1.8 Ω = 0 LSB
$V_{OUT\ LOW}$ op amp			70 mV = 72 LSB
Total error			18 LSB

The offset errors are tabulated in the intercept column. The gain errors are tabulated in the gain column. After the ideal component values are calculated potentiometer values are chosen so the offset and gain errors can be adjusted out. Notice that drift errors accumulate and subtract from the accuracy of the design.



Because of the relative difference between the sampling and data frequencies, and because the cable noise over shadows other noise concerns, picking an anti-aliasing filter is easy. Use a feedback capacitor across the feedback resistor because this acts as a low pass filter and improves stability. Select the value of the feedback capacitance as 0.1μF because this value is available in ceramic, stable, and inexpensive.



Two reference supply filter capacitors and two decoupling capacitors are shown in the final schematic because practical consideration require them. Splitting the value of RG and adding a capacitor at the junction of the two resistors can filter the sensor diode output. This decision is normally reserved until the actual hardware testing is completed. Notice that two adjustment resistors have been added to the design.