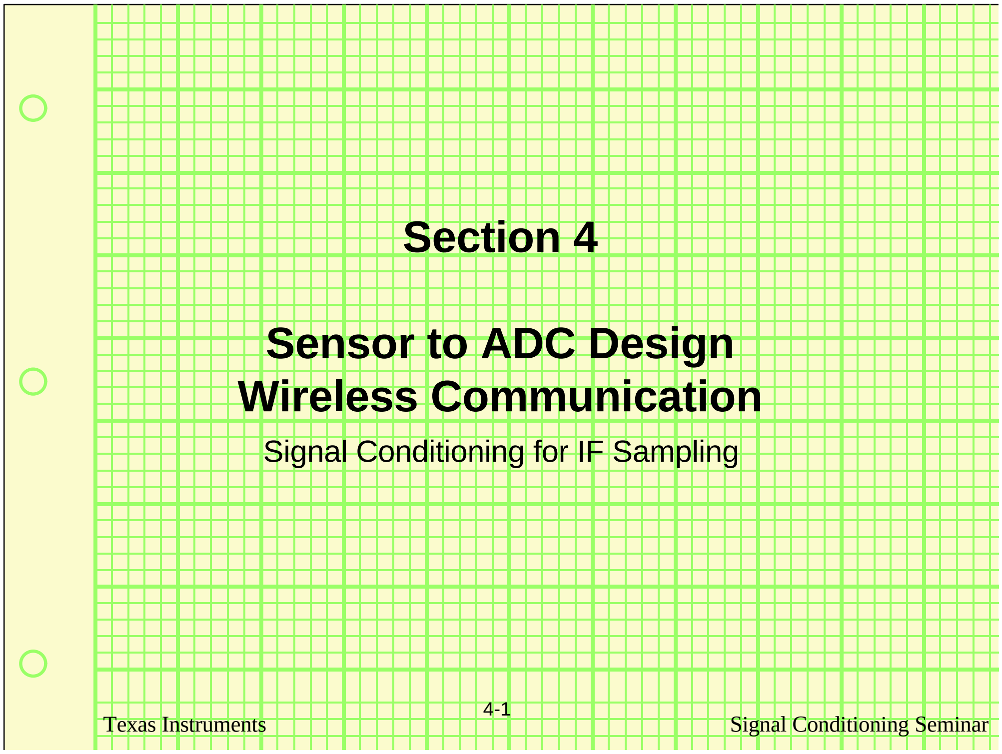


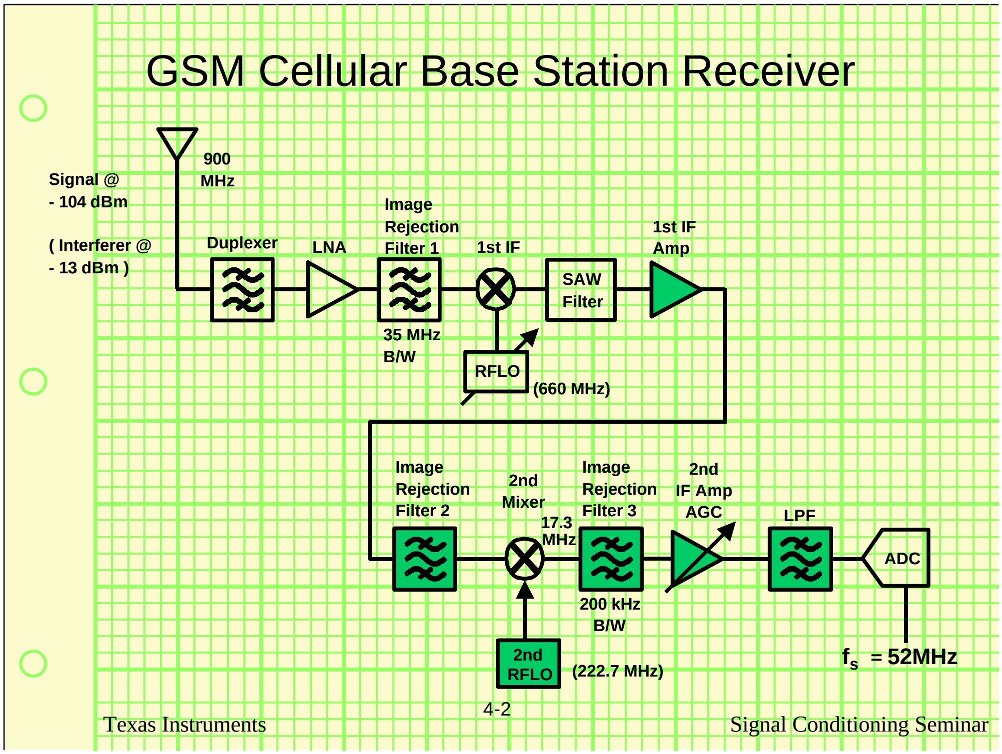
Section 4

Sensor to ADC Design
Wireless Communication

Signal Conditioning for IF Sampling

Texas Instruments 4-1 Signal Conditioning Seminar

High-speed op amps are used extensively in wireless communications. These amplifiers usually operate below 500MHz, and often they operate at 25MHz and below. Applications for high-speed op amps include filtering circuits, IF amplifiers, cable drivers, ADC drivers, and mixers.

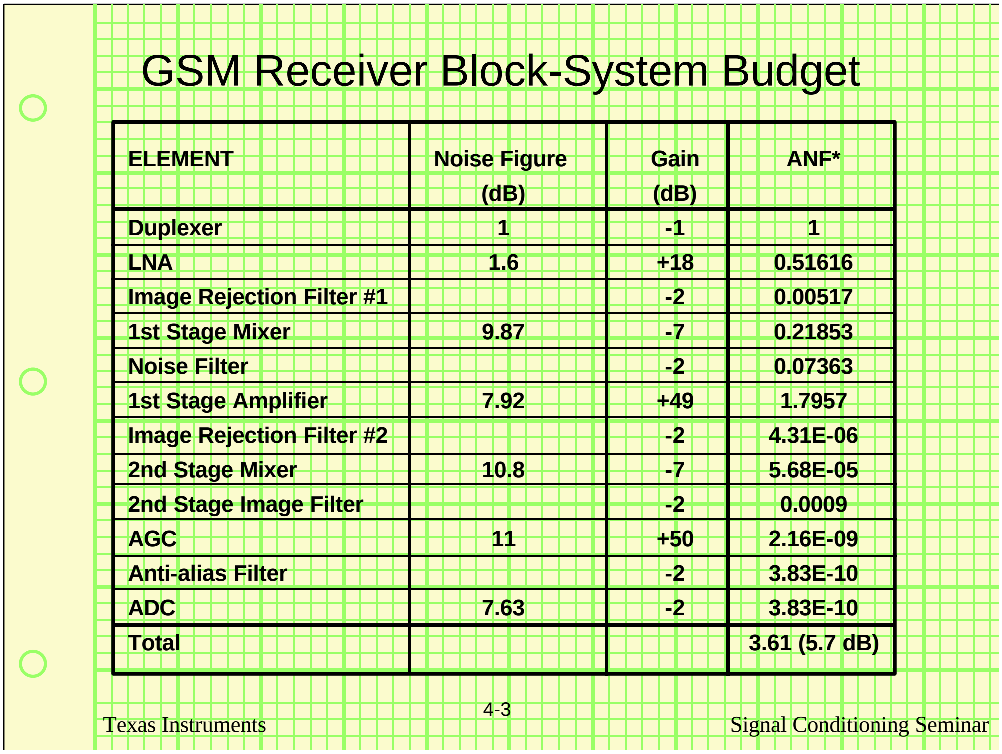


GSM Cellular Base Station Receiver

Texas Instruments 4-2 Signal Conditioning Seminar

Several stages with different IF frequencies are used in a dual IF receiver. The receiver converts the RF input to a base band signal. Receiver performance is measured in terms of receiver sensitivity, which is the ratio of the power of the desired baseband signal to the power of all undesirable signals (measured at the ADC output).

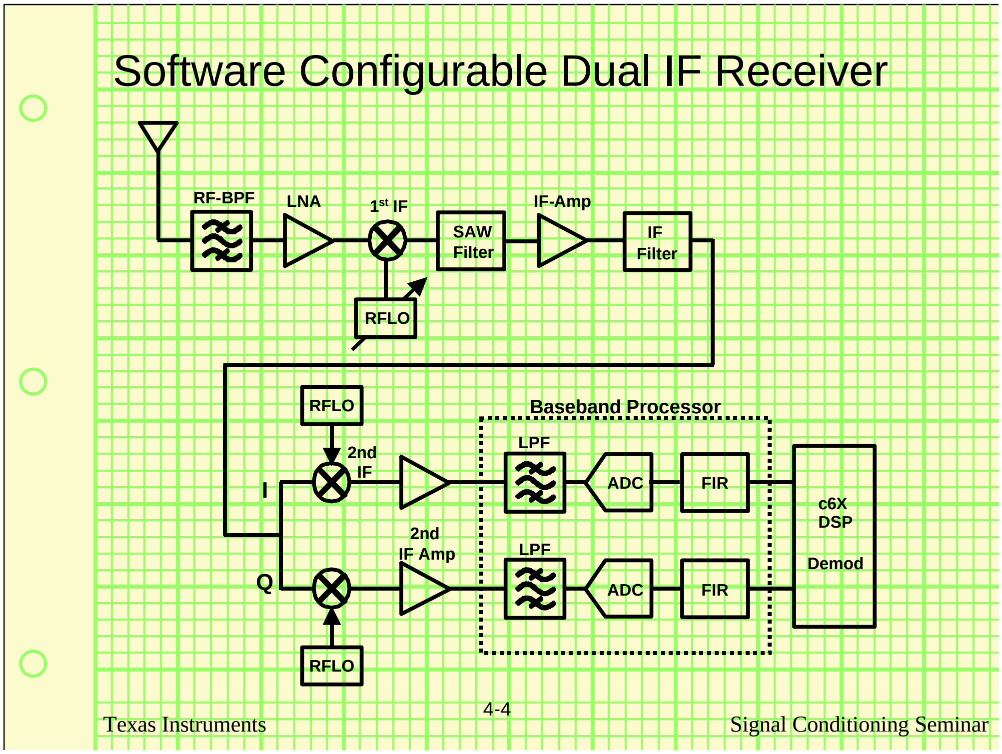
The 900MHz RF signal is received by the antenna and amplified by the low noise amplifier (LNA). The signal is then bandpass filtered to obtain image rejection and selectivity. The first mixer converts the band limited RF and local oscillator frequency (660MHz) into a difference frequency (240MHz). The first stage IF filter selects the difference frequency while rejecting noise, sum, original, and spurious frequencies. The first stage IF frequency passes through another image rejection filter and is mixed with the second local oscillator (222.7MHz). The next image rejection filter constrains the IF choice to a range of 10 to 20MHz. The signal is then amplified, gain controlled, and passed through a low pass filter to the ADC.



GSM Receiver Block-System Budget

ELEMENT	Noise Figure (dB)	Gain (dB)	ANF*
Duplexer	1	-1	1
LNA	1.6	+18	0.51616
Image Rejection Filter #1		-2	0.00517
1st Stage Mixer	9.87	-7	0.21853
Noise Filter		-2	0.07363
1st Stage Amplifier	7.92	+49	1.7957
Image Rejection Filter #2		-2	4.31E-06
2nd Stage Mixer	10.8	-7	5.68E-05
2nd Stage Image Filter		-2	0.0009
AGC	11	+50	2.16E-09
Anti-alias Filter		-2	3.83E-10
ADC	7.63	-2	3.83E-10
Total			3.61 (5.7 dB)

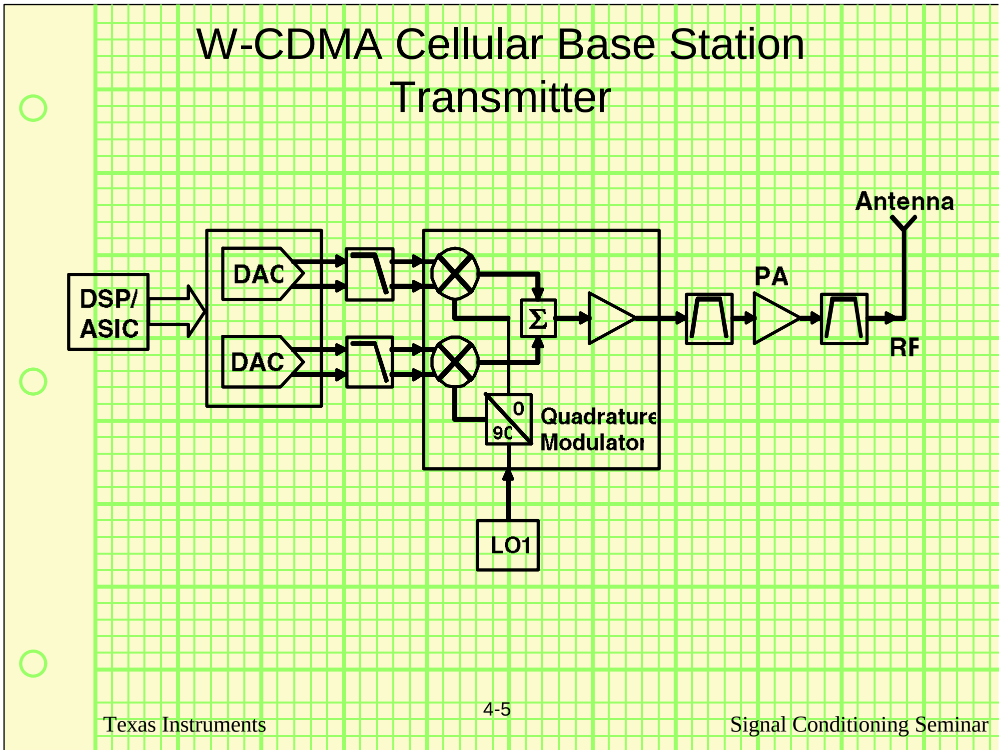
This table is a tabulation of the contribution of each stage to the system level error budget for a typical GSM receiver.



Software Configurable Dual IF Receiver

Texas Instruments 4-4 Signal Conditioning Seminar

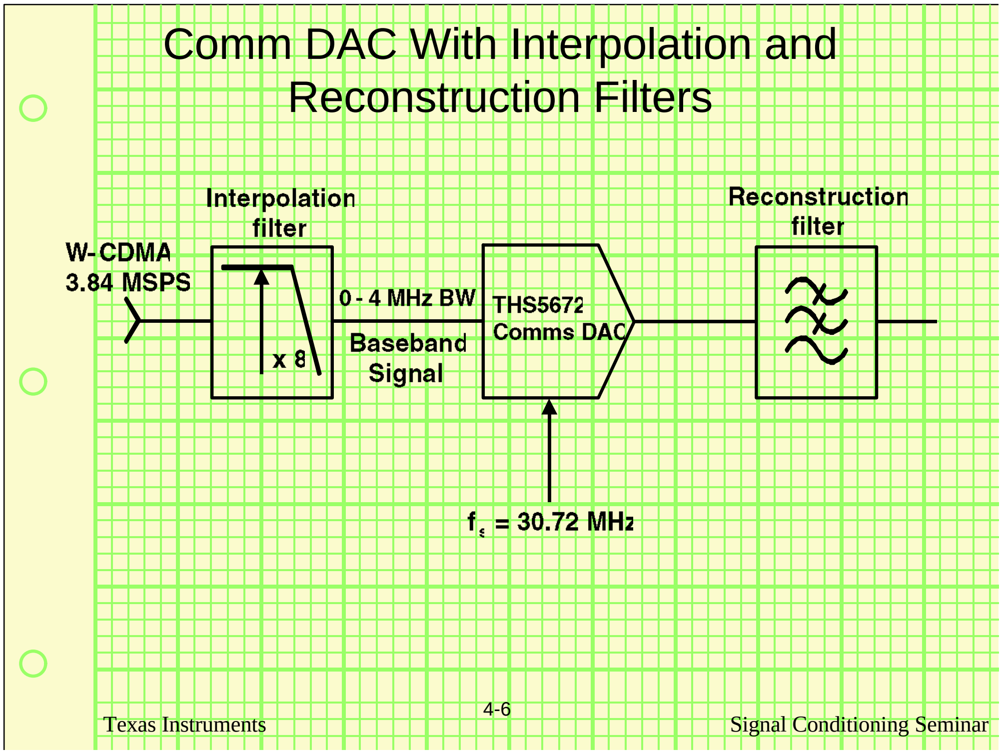
The digital signal processor (DSP) enables more flexibility in the receiver. The DSP allows a single receiver to access several different wireless systems through changes in software configuration.



W-CDMA Cellular Base Station Transmitter

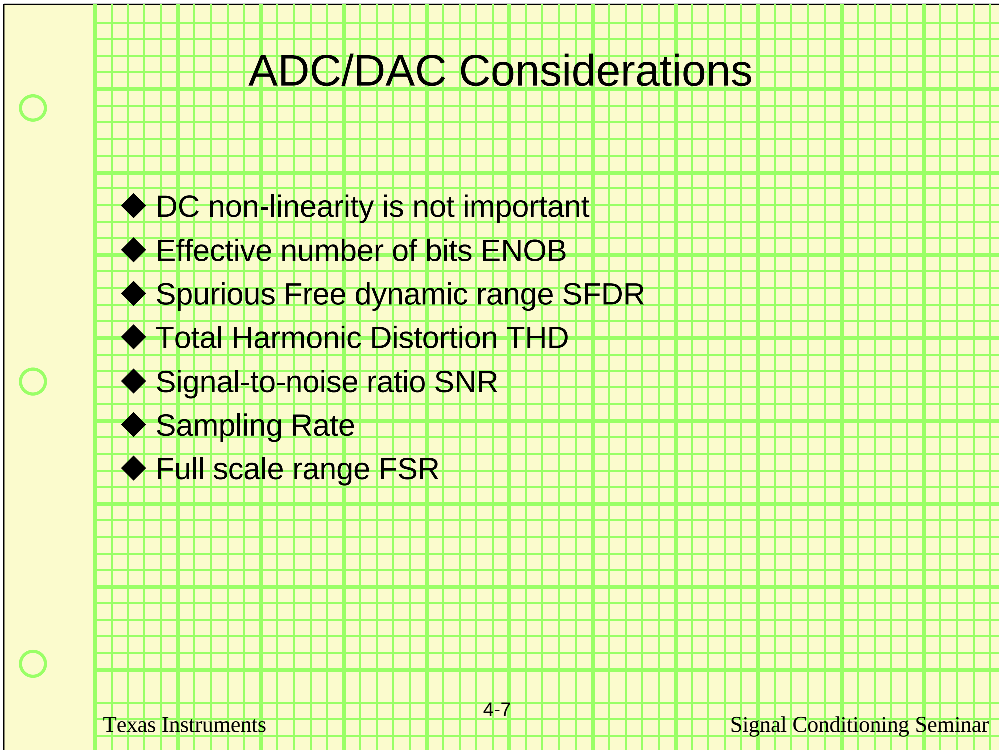
A voiceband coder-decoder (CODEC), op amps and DSP are used to digitize and band limit the audio signal. The digitized signal is compressed to the desired data rate in hardware or by software implemented on a DSP. Redundancy (error correction) , encryption, and modulation (QPSK for W-CDMA or GMSK for GSM) are added to the compressed digitized signal.

The DAC converts the modulated bit stream to analog; often two DACs are used, one for the I channel and one the Q channel. The modulator block converts the baseband I and Q signal to the appropriate carrier frequency, typically 864MHz. The up converted signal is amplified by the power amp (PA) which drives the RF amplifier and antenna. The RF amplifier is a large signal amplifier with power gain on the order of 50% for GSM and 30% for code division multiple access (CDMA).



Comm DAC With Interpolation and Reconstruction Filters

Assuming that the modulated bit stream is a 3.84 MSPS W-CMDA signal, for 8x interpolation, the sampling clock frequency must be 30.72MHz. The reconstruction filter at the DAC output is usually a high order Bessel or elliptic filter, and it filters the DAC transitions out the analog signal.

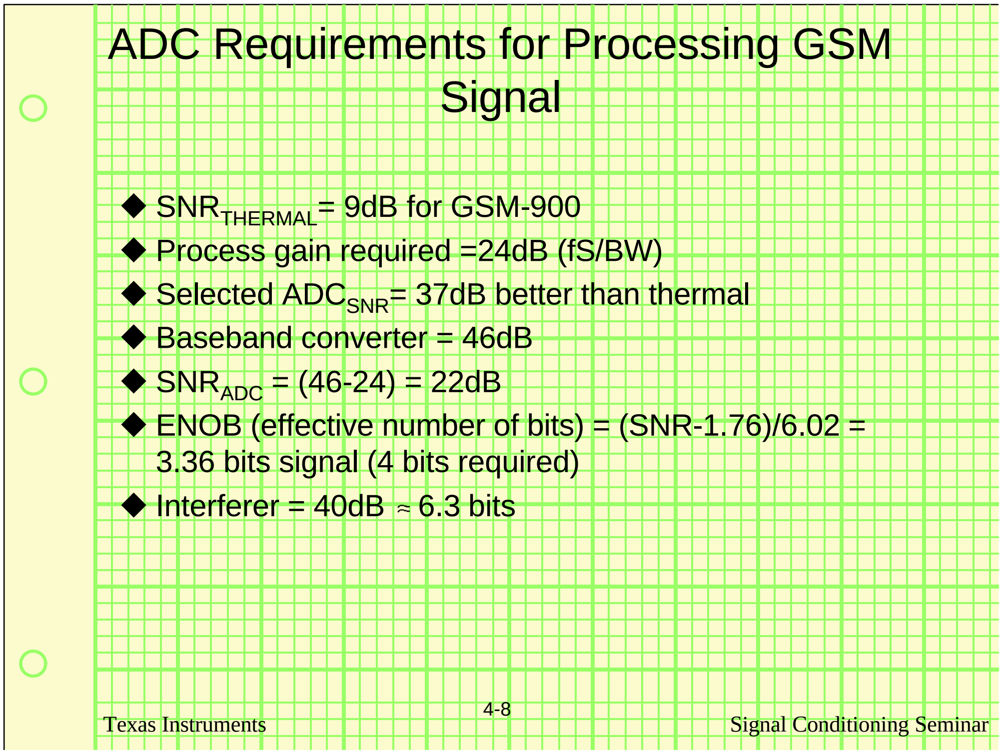


ADC/DAC Considerations

- DC non-linearity is not important
- Effective number of bits ENOB
- Spurious Free dynamic range SFDR
- Total Harmonic Distortion THD
- Signal-to-noise ratio SNR
- Sampling Rate
- Full scale range FSR

The dc non-linearity performance is not nearly as important in a communications ADC as it is in an instrumentation ADC because signal are band limited. The dynamic performance of the ADC is critical in communications applications. The overall receiver system specifications depend heavily on ADC dynamic performance parameters such as the effective number of bits (ENOB). ENOB is usually measured and specified at the system operating frequency, so it is a real performance measurement.

Spurious free dynamic range (SFDR) determines the ADC’s ability to separate an incoming signal from ADC noise spikes. Total harmonic distortion (THD) is a measure of the distortion that the ADC adds to the signal. Signal-to noise ratio (SNR) includes ADC noise and noise from other sources.



ADC Requirements for Processing GSM Signal

- $SNR_{THERMAL}$= 9dB for GSM-900
- Process gain required =24dB (fS/BW)
- Selected ADC_{SNR}= 37dB better than thermal
- Baseband converter = 46dB
- SNR_{ADC} = (46-24) = 22dB
- ENOB (effective number of bits) = (SNR-1.76)/6.02 = 3.36 bits signal (4 bits required)
- Interferer = 40dB ≈ 6.3 bits

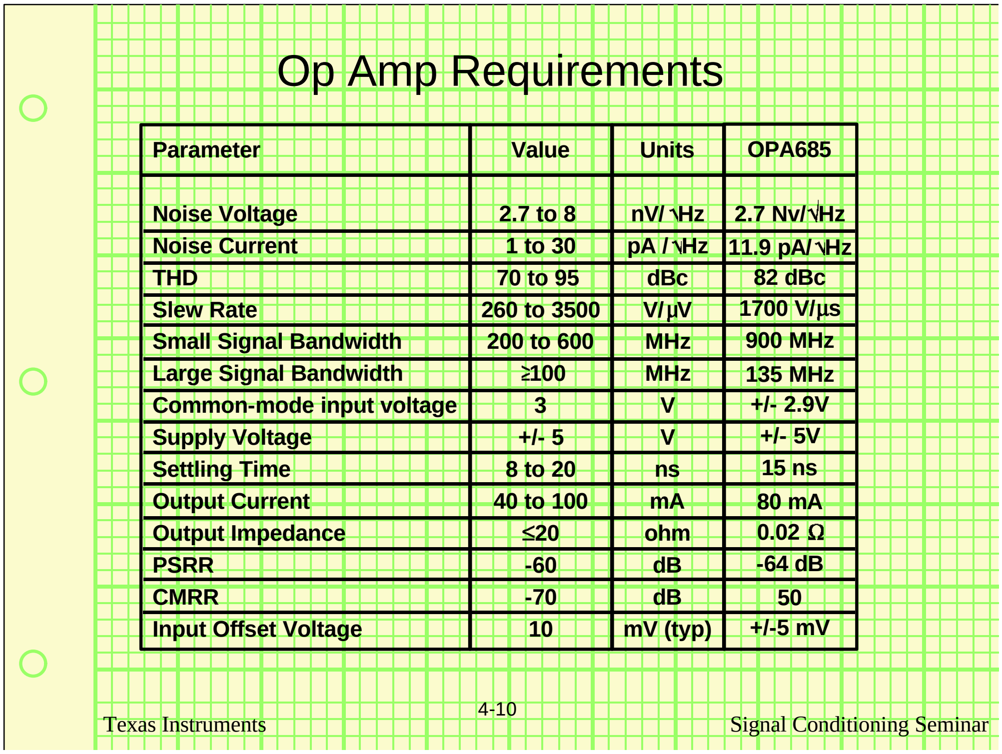
Texas Instruments 4-8 Signal Conditioning Seminar

The mean squared quantization power is $P_{qn} = q_s^2 / 12R$ where q_s is the quantization step size and R is the ADC input resistance, typically 600Ω to 1000Ω. Communication ADCs similar to the THS1052 and THS1265 typically have a full-scale range (FSR) of 1Vp-p to 2Vp-p. Based on the assumption of a 50Ω input/output termination, the quantization noise power for a 12 bit, 65MSPS ADC is –74dBm. The receiver noise power in a noise-limited receiver can be computed as the thermal noise power in the given receiver BW plus the receiver noise figure.

For 200kHz BW (GSM channel), $T_A = 25^oC$, and 4 to 6dB NF the receiver noise power is –115dBm. To boost the receiver noise to the quantization noise power level requires a gain of 42dB. The smallest 1% bit error-rate (BER) for GSM-900 is –104dBm, thus the SNR at baseband due to the thermal noise component is given by $SNR_{THERMAL} = E_b/N_0$ = -104dBm +115dBm = 9dBm. For a raw BER to be 1% in a GSM system, testing and standard curves indicate that a baseband SNR of 9dB is needed for this performance.

The process gain is $G_p = f_S/BW = 52x10^6/200x10^3 = 2.6x10^2 = 24dB$ where the GSM channel BW is 200kHz and f_S is 52MHz (ADC sampling frequency). The converter noise at baseband should be much better than the radio noise (thermal noise plus process gain), hence the converter noise at baseband = SNR_{ADC} + process gain (G_p).

SNR_{ADC} is selected as 37dB better than $SNR_{THERMAL}$; baseband converter noise is 9dB + 37dB = 45dB. SNR_{ADC} required to meet the GSM-900 standard is (46-24)dB = 22dB. The ENOB of the ADC must be = (SNR-1.76)/6.02 $\cong$ 4 bits. Assuming that the filter attenuates the interferer by 50dB, the interferer drops from 113dBm to –53dBm, or 40dB above the GSM signal. The number of bits required to accommodate the interferer is 40dB/6db/bit =6.3 bits. Six bits are required to accommodate the interferer, 4 bits are required for the GSM signal, and 2 bits are required for headroom, so we need a 12 bit converter.

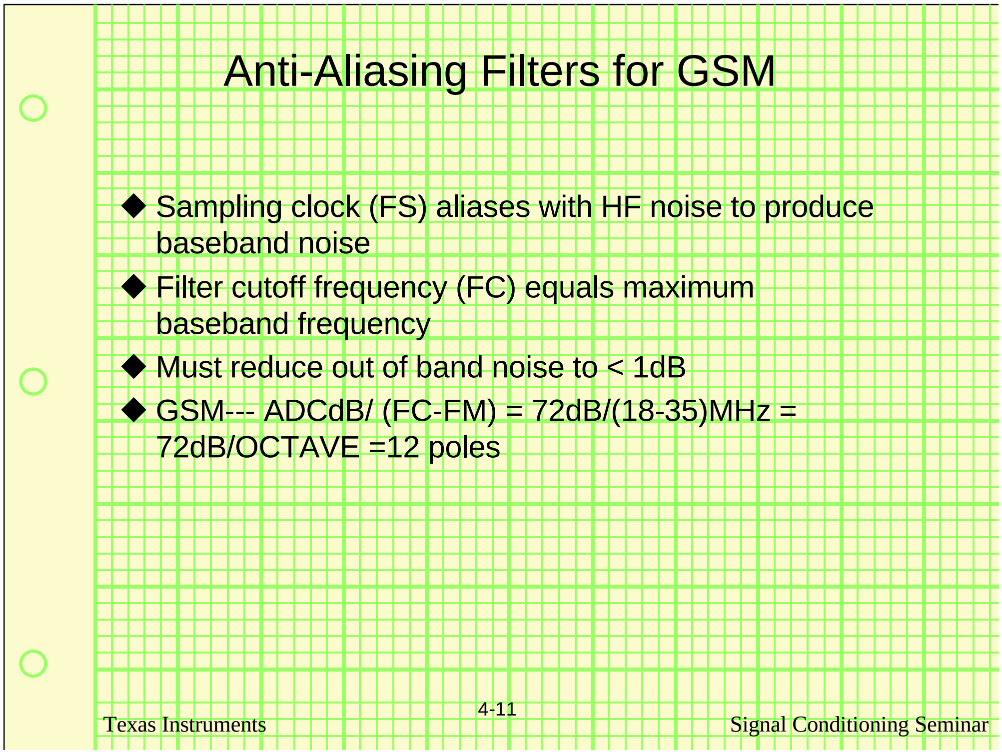


Op Amp Requirements

Parameter	Value	Units	OPA685
Noise Voltage	2.7 to 8	nV/ √Hz	2.7 Nv/√Hz
Noise Current	1 to 30	pA / √Hz	11.9 pA/ √Hz
THD	70 to 95	dBc	82 dBc
Slew Rate	260 to 3500	V/µV	1700 V/µs
Small Signal Bandwidth	200 to 600	MHz	900 MHz
Large Signal Bandwidth	≥100	MHz	135 MHz
Common-mode input voltage	3	V	+/- 2.9V
Supply Voltage	+/- 5	V	+/- 5V
Settling Time	8 to 20	ns	15 ns
Output Current	40 to 100	mA	80 mA
Output Impedance	≤20	ohm	0.02 Ω
PSRR	-60	dB	-64 dB
CMRR	-70	dB	50
Input Offset Voltage	10	mV (typ)	+/-5 mV

The SFDR and IMD are the key ADC/DAC parameters that influence op amp selection. A minimum requirement is that the op amp's SFDR or IMD, measured at the operating frequency, be 5dB to 10dB better than the converter's equivalent specifications. A perfect 12 bit ADC has a SFDR or IMD of 72dB, and the op amp should have a SFDR or IMD of 77dB to 82dB. Fast settling time is mandatory because the ADC must settle within a fraction of an LSB in the ADC sampling time.

Low voltage systems are popular now, and the designer must be aware that ac specifications are only valid at the test supply voltage. Operating the op amp at different supply voltages changes their ac specifications.



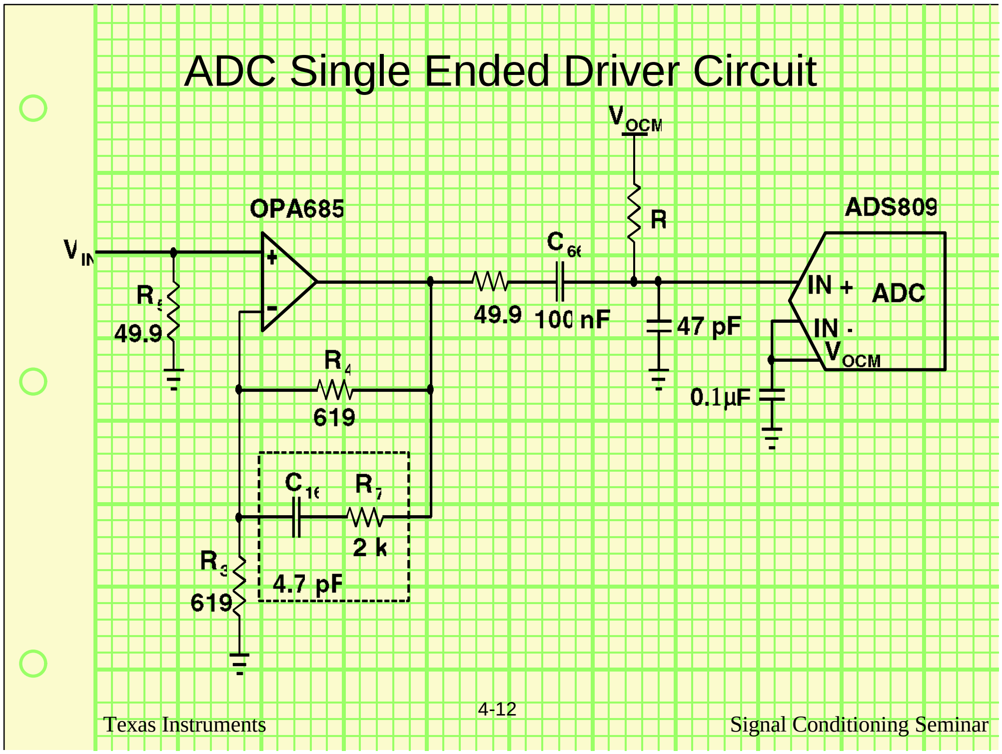
Anti-Aliasing Filters for GSM

- Sampling clock (FS) aliases with HF noise to produce baseband noise
- Filter cutoff frequency (FC) equals maximum baseband frequency
- Must reduce out of band noise to < 1dB
- GSM--- ADCdB/ (FC-FM) = 72dB/(18-35)MHz = 72dB/OCTAVE =12 poles

Texas Instruments 4-11 Signal Conditioning Seminar

Spurious signals (>$f_S/2$) must be prevented from getting into the ADC (sampling at Nyquist rate f_s) where they cause aliasing errors in the ADC output. A suitable anti-alias low pass filter placed before the ADC prevents frequency components capable of aliasing from reaching the ADC. The anti-alias filter cutoff frequency (f_C)is set to the highest baseband frequency of interest (f_{MAX}) so that $f_C = f_{MAX}$. The Nyquist sampling theorem requires the ADC sampling rate t be twice the maximum baseband frequency ($f_S = 2f_{MAX}$). Only an ideal “brickwall” filter can meet these criteria of filtering out all aliasing frequencies, thus reality dictates $f_C > 2f_{MAX}$.

The highest signal frequency of interest sets the cutoff frequency. Suppose the input frequency to be sampled is 12 bit accuracy with a sampling frequency of 52MHz, and the IF frequency is 17MHz, then an 18MHz filter –3dB cutoff frequency could be chosen. All frequencies above the Nyquist frequency should be attenuated to < 1/2LSB. Only the frequencies above the ADC’s resolution limit are a problem; i. e., f_{ALIAS} = (52-17) = 35 MHz. The frequency roll off is 18 to 35 MHz (about an octave) and the required attenuation is 72dB (12 bit ADC), so approximately a 12th order filter is required. Practical anti-aliasing filters are limited to 6th order, and that is why f_S usually exceeds f_{MAX} by a large margin.



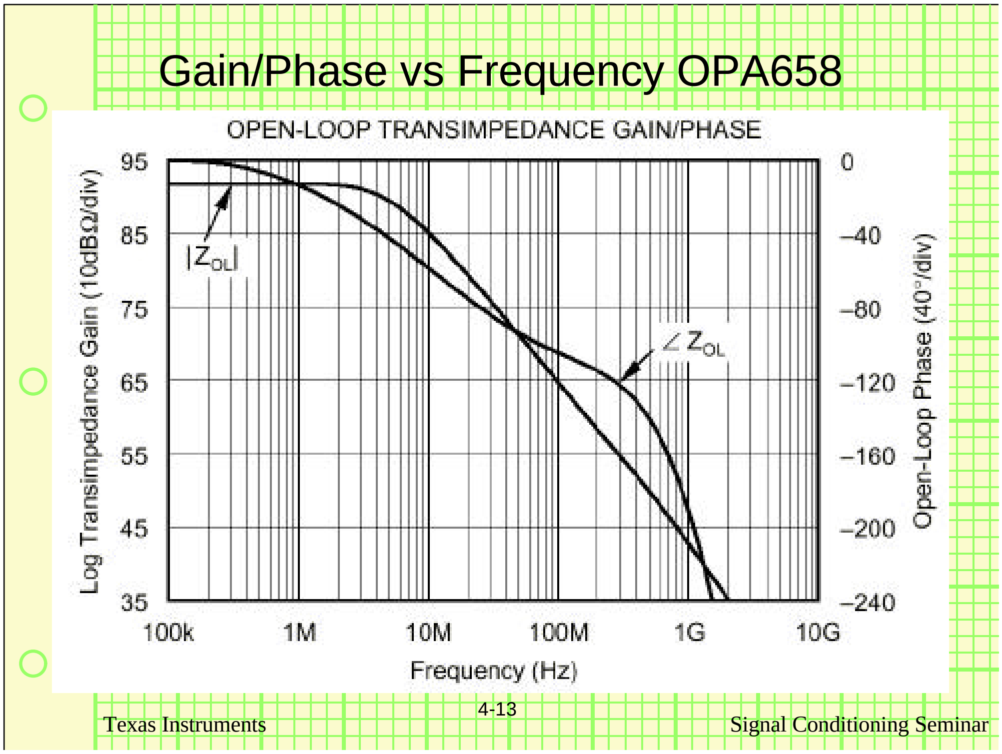
ADC Single Ended Driver Circuit

An op amp voltage follower circuit is often used to interface the external precision voltage reference supplying the ADC/DAC. V_{IN} is the output from a precision voltage reference such as Thaler Corp. VRE3050. The low pass filter formed by R_1 and C_1 eliminates noise coming from the reference and buffer. The –3dB corner frequency (f_C) of the filter is $1/2\pi C_1R_1$, and the transfer function for the circuit is given below.

$$\frac{V_O}{V_{IN}} = \frac{1+sC_1R_1}{\left(s^2+\frac{sC_2R_2}{C_1R_1C_2R_2}+\frac{1}{C_1R_1C_2R_2}\right)C_1R_1C_2R_2}$$

When $C_2R_2 = 2C_1R_1$ the resultant poles are:

$$P_1,P_2 = -\frac{1}{2C_1R_1} \pm j\frac{1}{2C_1R_1}$$



Gain/Phase vs Frequency OPA658

Texas Instruments 4-13 Signal Conditioning Seminar

Design example; Let C_1 = 1.2μF and R_1 = 42.2Ω, and C_2's value should be approximately 5% of C_1"s value, so C_2 = .047μF and R_2 = 2.15kΩ. The calculated –3dB BW is 3.1kHz, and this value agrees with the frequency response plot. This circuit is an excellent selection for driving large capacitive loads because C_1 adds to the load capacitance, and the zero containing C_2 stabilizes the circuit.