Key Parameters

Key ADC Specifications

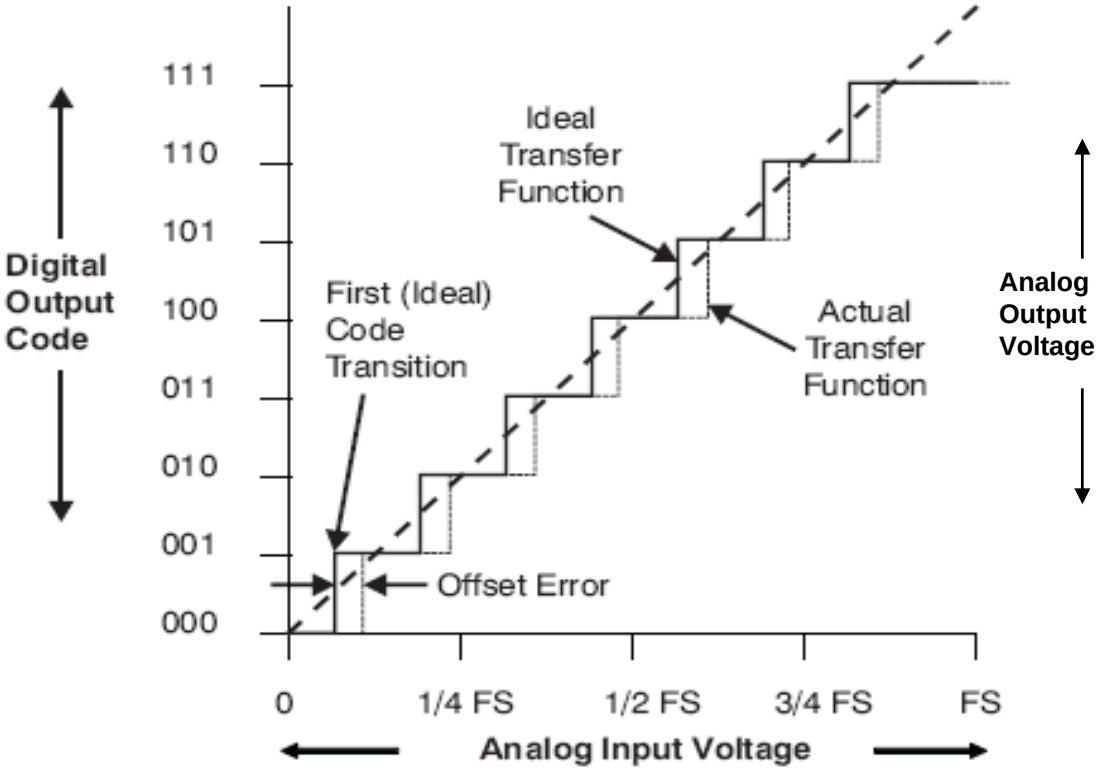
- Static Specifications
  - Offset / Full-scale / Gain
  - Differential Non-linearity (DNL) / Integral Non-linearity (INL)
  - No Missing Codes
- Dynamic Specifications
  - Signal to Noise Ration (SNR)
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD) / SIgnal to Noise And Distortion (SINAD)
  - Effective Number Of Bits (ENOB)

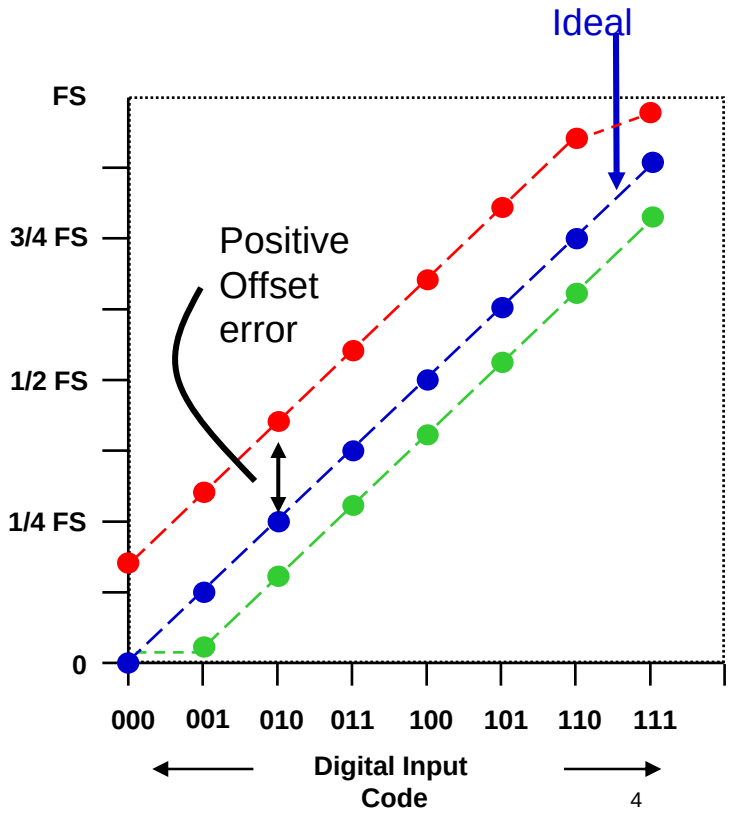
Key DAC Specifications

- Static Specifications
  - Zero-Code / Offset / Full-scale / Gain
  - Differential Non-linearity (DNL) / Integral Non-linearity (INL)
  - Monotonicity
- Dynamic Specifications
  - Glitch impulse
  - Settling time
  - Update rate

Offset Error

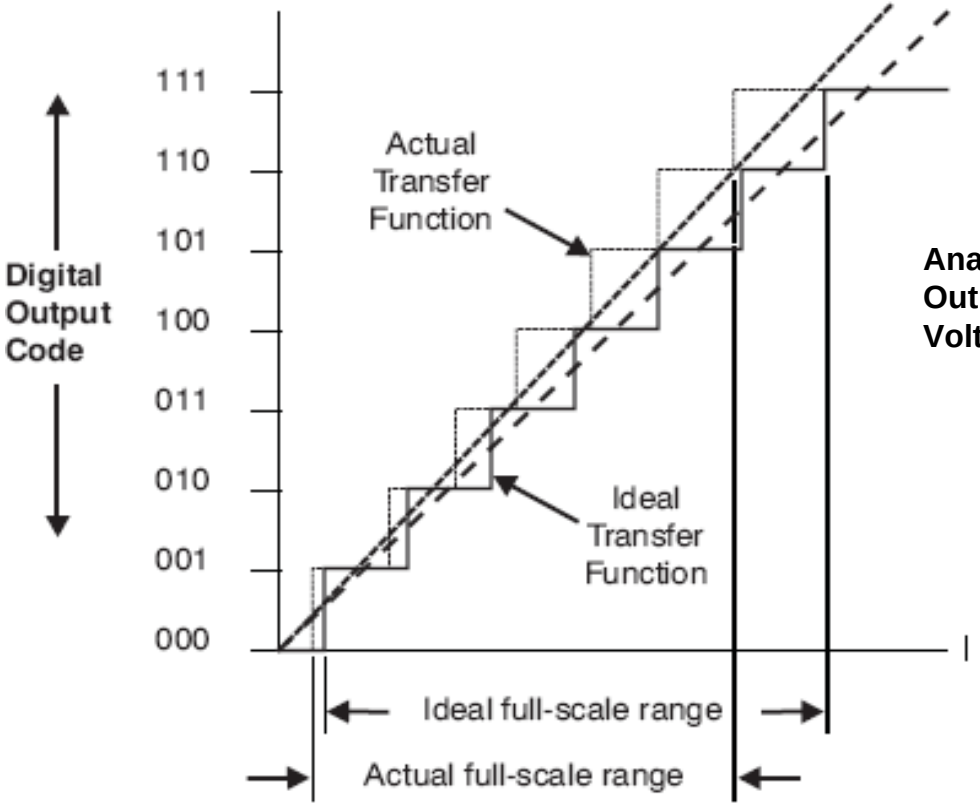
Offset error is the difference in voltage between the ideal first code transition and the actual code transition of an ADC, respectively the difference to the reference at code 000xxx in case of a DAC

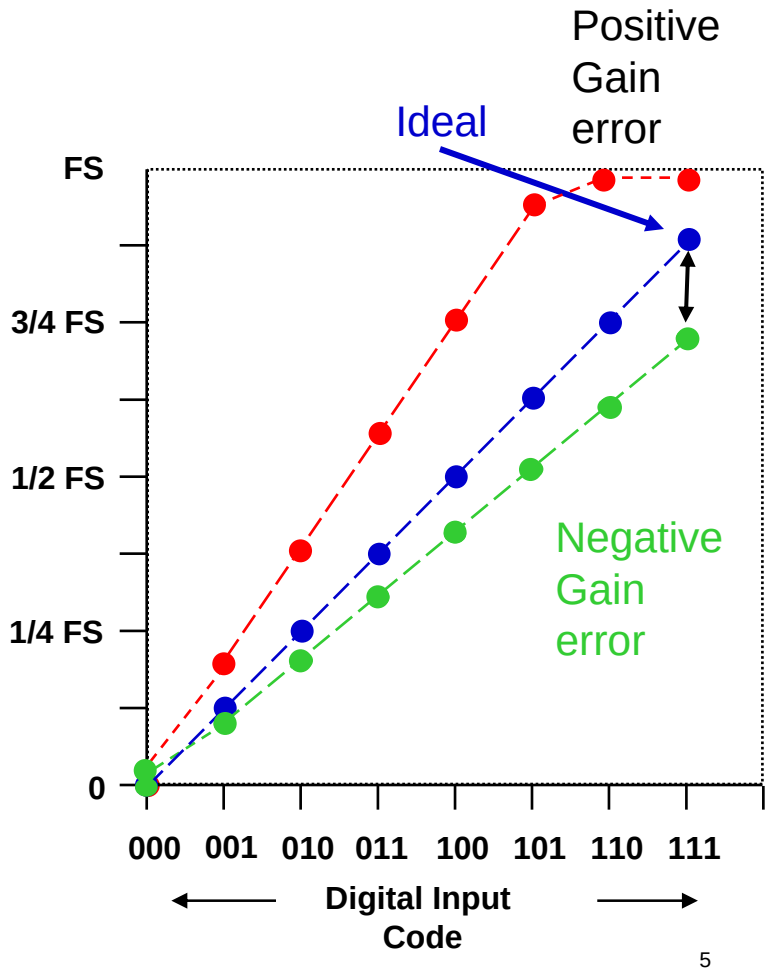




Gain Error (Full Scale Error)

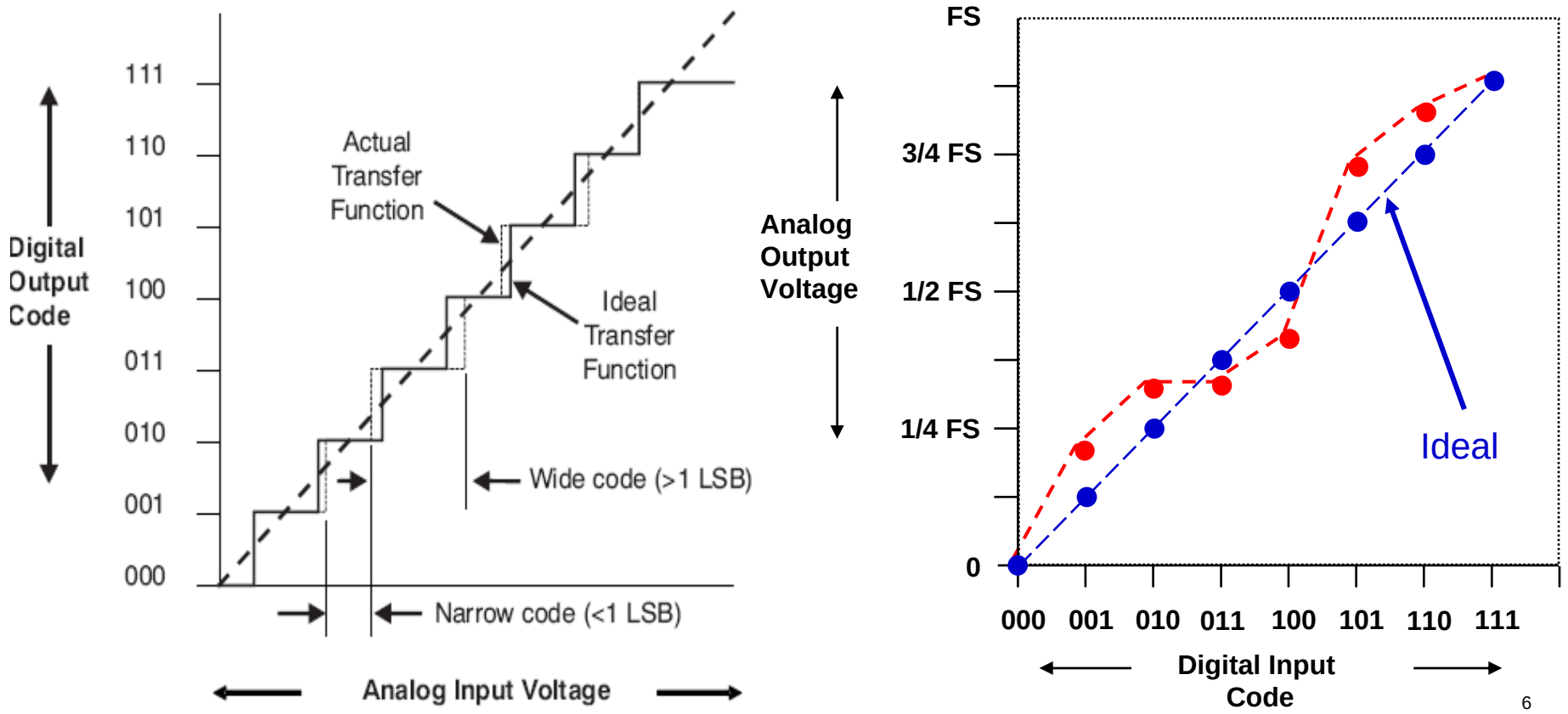
Gain Error = Full-scale Error - Offset Error



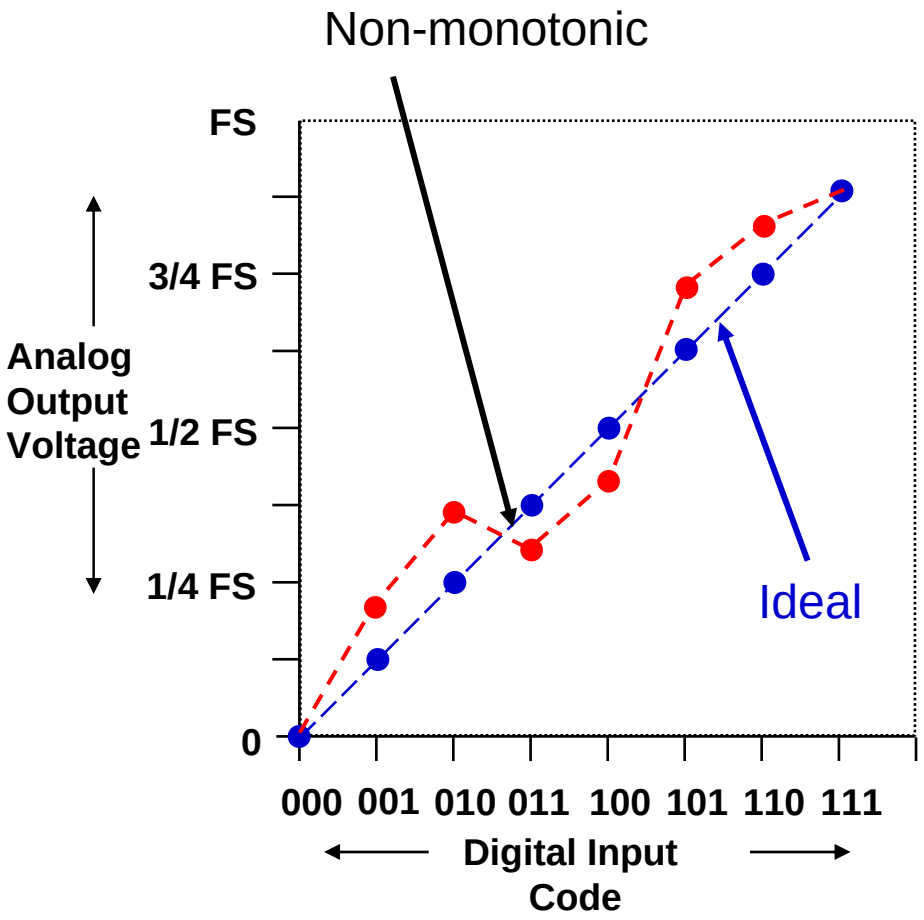


Differential Nonlinearity (DNL):

A DNL error beyond +/-1LSB can cause missing codes in an ADC or Non-Monotonic behavior of a DAC..



DAC Monotonicity

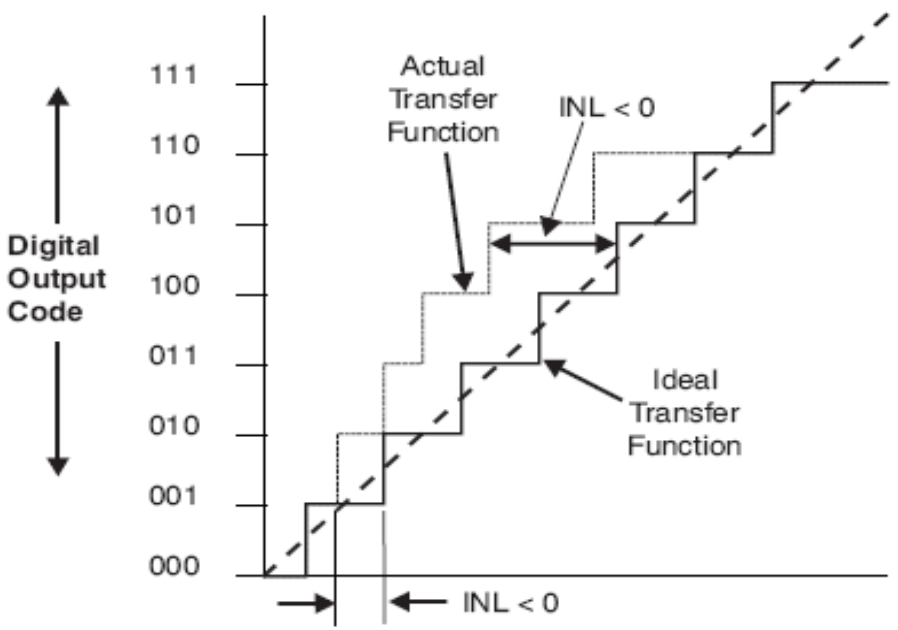


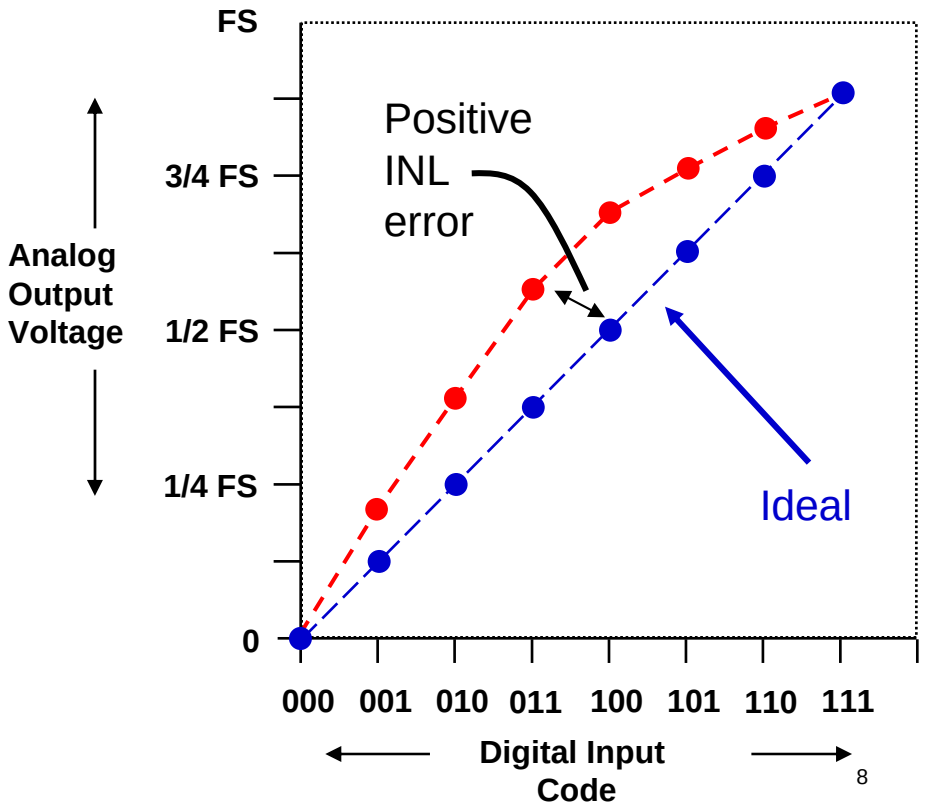
Non-monotonic DAC's are not appropriate for control loop Applications!

DNL < -1

Integral Nonlinearity INL

An **INL** error is the maximum deviation of a transition point from the corresponding point of the ideal transfer curve, with the measured offset and gain errors zeroed.





AC Applications

Six popular specifications for quantifying ADC dynamic performance are:

- SINAD (signal-to-noise-and-distortion ratio),
- ENOB (effective number of bits),
- SNR (signal-to-noise ratio),
- THD (total harmonic distortion),
- THD + N (total harmonic distortion plus noise),
- SFDR (spurious free dynamic range).

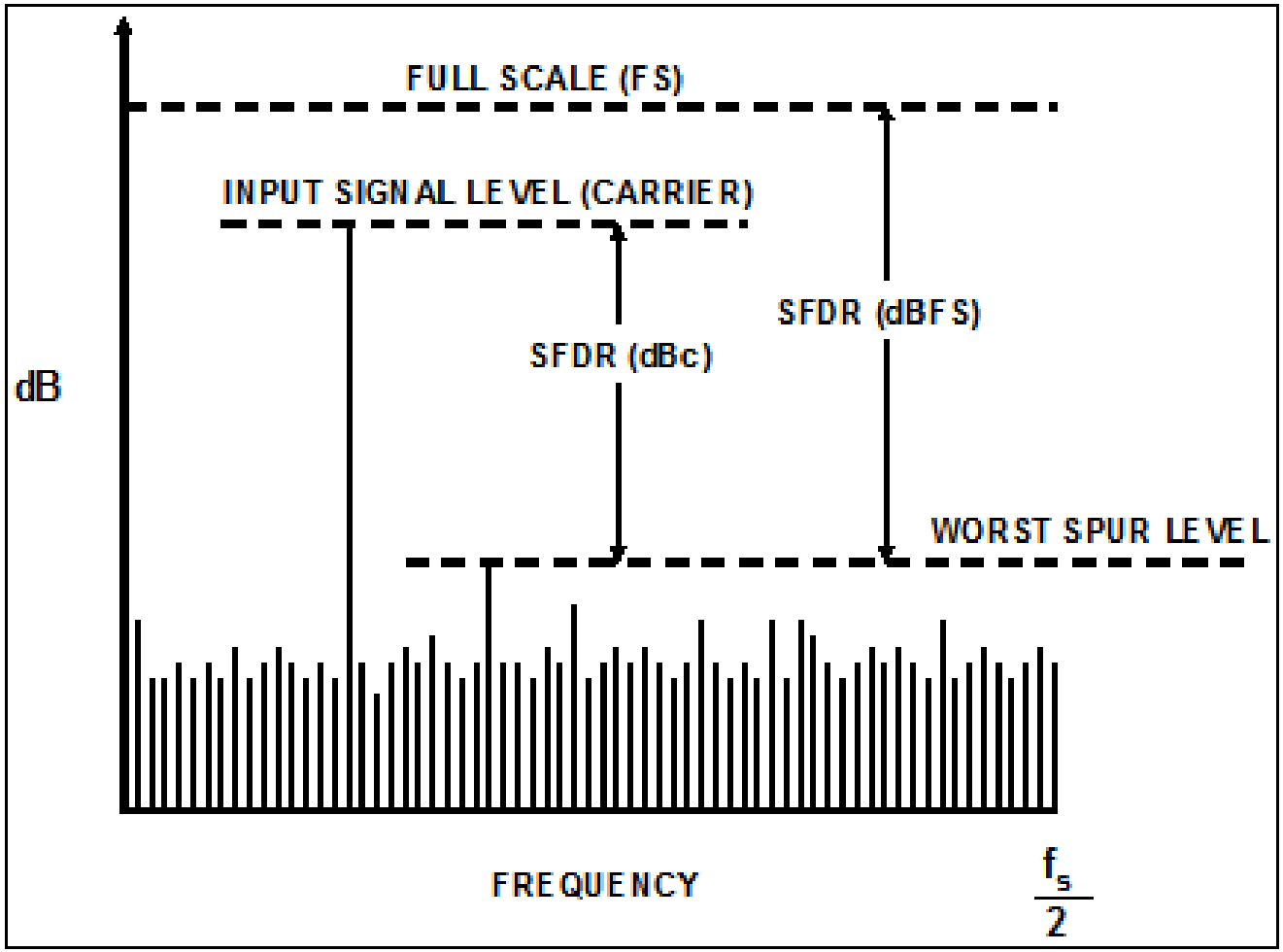
Spurious-Free Dynamic Range (SFDR)

SFDR = ratio

RMS value of the signal

to

RMS value of worst spur



Signal-to-Noise Ratio (SNR)

$$SNR_{dB} = 20\log_{10}\left(\frac{\text{value of } F_s \text{ input}[rms]}{\text{value of quantization noise}[rms]}\right)$$

$$F_s \text{ INPUT} = v(t) = \left[\frac{q2^N}{2}\right]\sin(2\pi ft)$$

$$\text{RMS Value of } F_s \text{Sinewave} = \frac{q2^N}{2\sqrt{2}}$$

$$\text{RMS Value of Quantization Noise} = \frac{q}{\sqrt{12}}$$

$$SNR = 6.02N + 1{,}76dB$$

THD and THD+N

Total harmonic distortion (plus noise):

power ratio of single tone vs. sum of harmonics

THD+N includes Noise as well

$$THD + N = 20\log_{10}\left(\frac{\sqrt{\left(A^2_{HD_2[rms]} + A^2_{HD_3[rms]} + \ldots + A^2_{HD_n[rms]} + Noise^2_{[rms]}\right)}}{A_{fin[rms]}}\right)$$

Signal-to-Noise and Distortion Ratio (SINAD) and ENOB

SINAD = ratio of RMS signal vs.
mean of the root-sum-squares (RSS) of all other spectral components

ENOB is calculated from SINAD

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

dBc vs dBFS

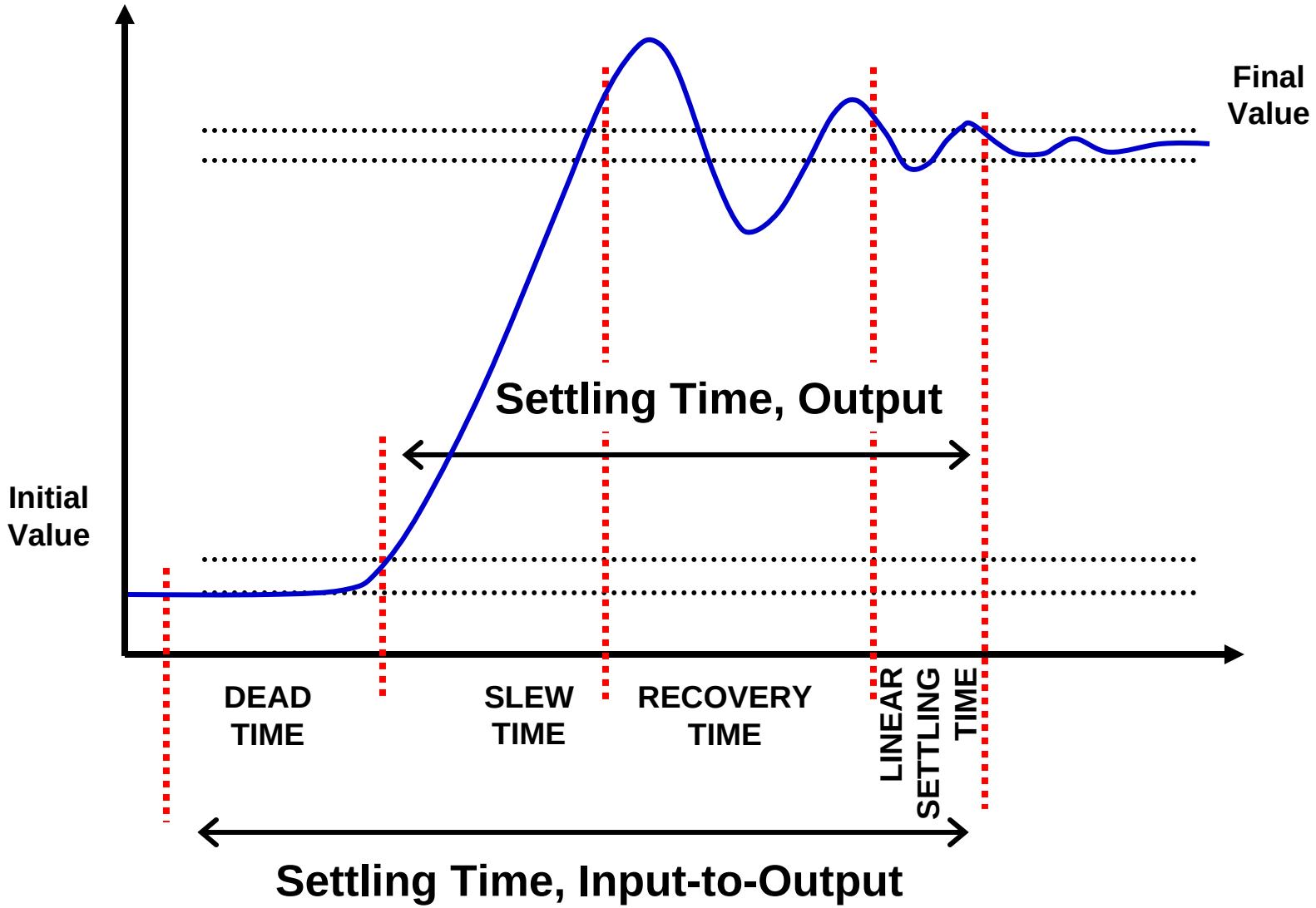
- **dBc – measurement made relative to the carrier power**
- **dBFS – measurement made relative to the converter's Full Scale**
  - **full scale is 0dBFS,**
    but it is common to use -1dBFS,
    allowing some headroom in case there is noise or a slight DC shift

ADC Clock Rates

- ADC clock rates: *usually* specified as xSPS
- analog input frequency: specified in Hz

- But, xSPS is still xHz
- 100MSPS = 100MHz clock
- 1GSPS = 1GHz clock
- 100kSPS = 100 kHz clock.

Settling Time Determines Bandwidth

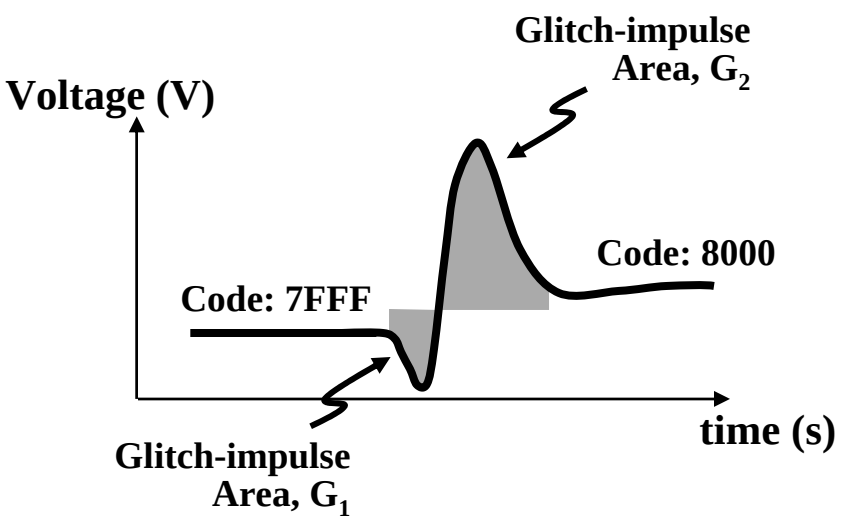


Settling Time vs. Update Rate

- Settling time: the time the output takes to reach the final state
  - usually given in a unit of time.
- Update Rate: the speed of the interface
  - usually given in a unit of frequency, Hz or SPS

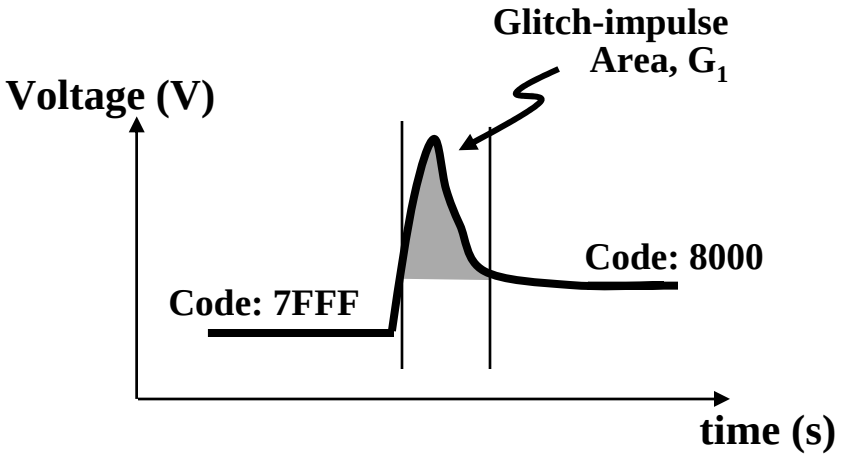
- Settling time should be shorter than the period time, otherwise dynamic performance suffers, in particular at full-scale-swings

Glitch Impulse Defined



Glitch-impulse = $G_2 - G_1$

a.)



Glitch-impulse = G_1

b.)