

Challenges of designing high-frequency, high-input-voltage DC/DC converters

By Richard Nowakowski, Power Management Product Marketing, and Brian King, Applications Engineer, Member Group Technical Staff

DC/DC converters are being designed with ever faster switching frequencies in an effort to decrease the size of the output capacitor and inductor to save board space. Because of this, more DC/DC converters that operate at higher input voltages are now on the market that provide protection from line transients, making lower voltages difficult to achieve at faster frequencies due to the lower duty cycle. Many manufacturers of power integrated circuits (ICs) are aggressively marketing high-frequency DC/DC converters that they claim reduce board space. A DC/DC converter operating at 1 or 2 MHz seems like a great idea, but the switching frequency impacts the power-supply system in more ways than just its size and efficiency. This article presents several design examples that demonstrate the benefits and challenges of switching at higher frequencies.

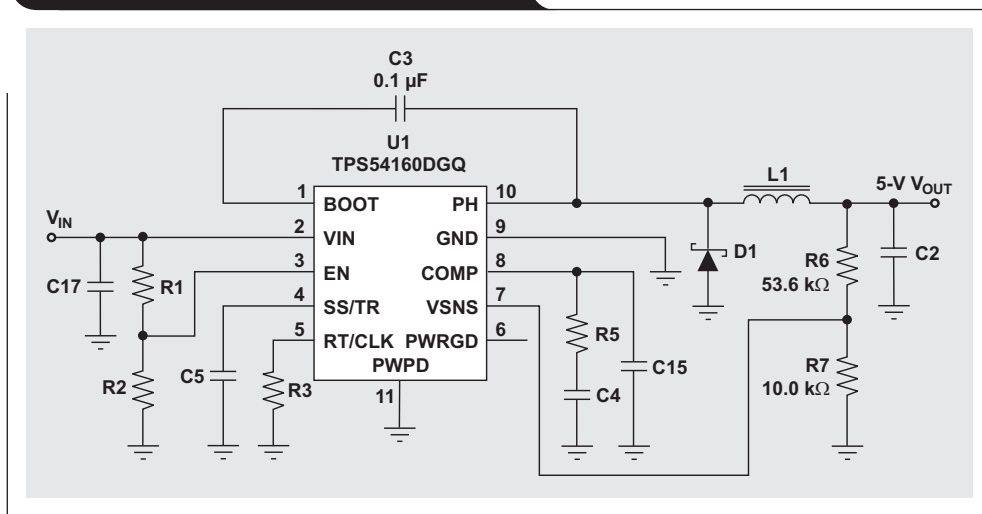
Selecting an application

To show the trade-offs of using high switching frequencies, three independent power supplies were designed and built with respective operating frequencies of 100, 300, and 750 kHz. For all three designs, the input voltage was 48 V, the output voltage was 5 V, and the output current was 1 A. These requirements are typical for powering a 5-V logic USB or an intermediate, general 5-V bus to be used by other DC/DC converters, such as low-dropout regulators. To establish design limitations, the allowable ripple voltage chosen was 50 mV, which was about 1% of the output voltage; and a peak-to-peak inductor current of 0.5 A was chosen. The Texas Instruments TPS54160, which is a 2.5-MHz, 60-V, 1.5-A step-down DC/DC converter with an integrated MOSFET, was used as the regulator in each design. The TPS54160, featuring external compensation and a fast programmable frequency, is intended for industrial applications with high input voltages.

Selecting the inductor and capacitor

The inductor and capacitor for each scenario were chosen according to the following four simplified formulas:

Figure 1. TPS54160 reference schematic



For the inductor,

$$V = L \times di/dt. \quad (1a)$$

This can be rearranged as

$$L \geq (V_{OUT} + V_{Diode}) \times \frac{1-D}{\Delta I \times f_s}, \quad (1b)$$

where D (the duty cycle) = 5 V/48 V = 0.104, and $\Delta I = 0.5$ A peak to peak.

For the capacitor,

$$I = C \times dv/dt. \quad (2a)$$

This can be rearranged as

$$C \geq \frac{2 \times \Delta I}{8 \times f_s \times \Delta V}, \quad (2b)$$

where $\Delta I = 0.5$ A peak to peak, and $\Delta V = 50$ mV.

For Equation 2b it is assumed that the capacitor chosen has negligible equivalent series resistance (ESR), which is true for ceramic capacitors. Ceramic capacitors were chosen for all three designs because of their low resistance and small size. The multiplier of 2 in the numerator of Equation 2b accounts for the capacitance drop associated with DC bias, since this effect is not accounted for in the datasheets of most ceramic capacitors.

The circuit in Figure 1 was used to evaluate the performance of each design on the bench. The components in the schematic that do not have values are the components that were modified in each design. The output filter consists of

L1 and C2. The values of these components for all three designs are listed in Table 1 and were chosen based on the results from Equations 1a through 2b. Note that the DC resistance of each inductor decreased as the frequency increased. This is due to less copper length being needed for fewer turns. The error amplifier's compensation components were designed independently for each switching frequency. The calculations for selecting the compensation values are beyond the scope of this article.

Minimum ON time

DC/DC converter ICs are characterized by a limit on the minimum controllable ON time, which is the narrowest achievable pulse width of the pulse-width-modulation (PWM) circuit. In a buck converter, the percentage of time that the power MOSFET is on during a switching cycle is called the duty cycle and is equal to the ratio of the output voltage to the input voltage. For the TPS54160 converter, the duty cycle is 0.104 (5 V/48 V), and the minimum ON time as shown in the datasheet is 130 ns. The limit for the controllable pulse width results in a minimum achievable duty cycle, which can be easily calculated by multiplying the minimum ON time by the switching frequency. Once the minimum duty cycle is known, the lowest achievable output voltage can be calculated by multiplying V_{IN} by the minimum duty cycle. The lowest output voltage is also limited by the reference voltage of the converter, which is 0.8 V for the TPS54160.

In this example, a 5-V output can be generated with a 750-kHz switching frequency (see Table 2). However, if the frequency is 1 MHz, the lowest possible output voltage is limited to about 6 V; otherwise the DC/DC converter will skip pulses. The alternative is to lower the input voltage or the frequency. It is a good idea to check the DC/DC converter datasheet for a guaranteed minimum controllable ON time before selecting a switching frequency.

Pulse skipping

Pulse skipping occurs when the DC/DC converter cannot extinguish the gate-drive pulses fast enough to maintain the desired duty cycle. The power supply will try to regulate the output voltage, but the ripple voltage will increase due to the pulses being further apart. Due to the pulse skipping, the output ripple will exhibit subharmonic components, which may present noise issues. It is also possible that the current-limiting circuit will no longer work properly, since the IC may not respond to a large current spike. In some cases, the control loop may be unstable if the controller is not performing properly.

Efficiency and power dissipation

The efficiency of a DC/DC converter is one of the most important attributes to consider when designing a power supply. Poor efficiency translates into higher power dissipation, which has to be managed with separate heat sinks or additional copper on the printed circuit board (PCB). Power dissipation also places a higher demand on the power supply upstream. Power dissipation has several components, shown in Table 3.

The loss components of interest from the three examples come from the FET driving loss, the FET switching loss, and the inductor loss. The FET resistance and IC loss are consistent since the same IC is used in all three designs. Since ceramic capacitors with low ESR were chosen in

Table 1. Capacitor and inductor selections for three example power-supply designs

| SWITCHING FREQUENCY (kHz) | C2 (μF)/SIZE | L1 (μH) | L1 DC RESISTANCE (max) (mΩ) |
|---------------------------|--------------|---------|-----------------------------|
| 100 | 47/1206 | 100 | 240.9 |
| 300 | 10/0805 | 33 | 180 |
| 750 | 4.7/0603 | 15 | 135 |

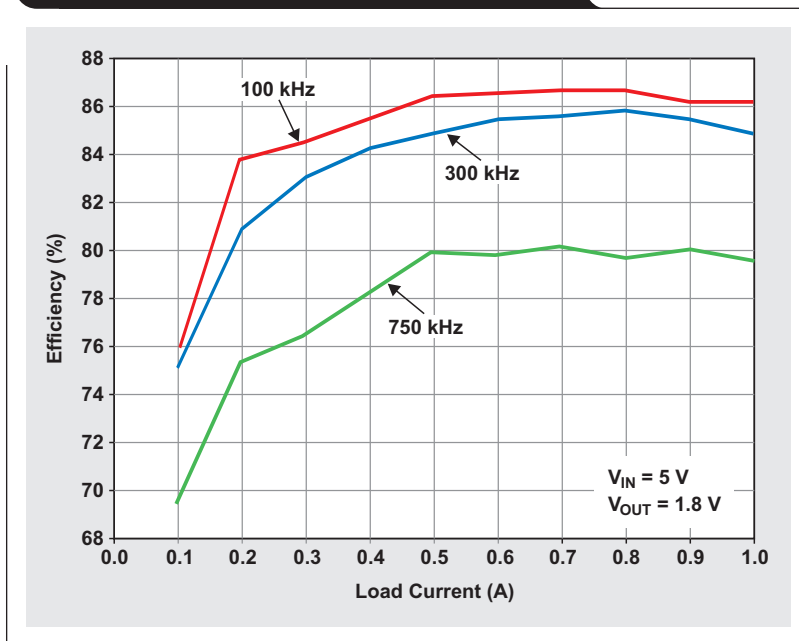
Table 2. Minimum output voltage with 130-ns minimum ON time

| SWITCHING FREQUENCY | MINIMUM DUTY CYCLE | MINIMUM V_{OUT} at 48 V_{IN} (V) |
|---------------------|--------------------|--------------------------------------|
| 100 kHz | 0.013 | 0.8 (V_{REF}) |
| 300 kHz | 0.039 | 1.87 |
| 750 kHz | 0.098 | 4.7 |
| 1 MHz | 0.13 | 6 |

Table 3. Power-dissipation components

| LOSS COMPONENT | FACTORS |
|--------------------|--|
| FET driving loss | Function of gate charge, drive voltage, frequency |
| FET switching loss | Function of V_{IN} , I_{OUT} , FET rise/fall time, frequency |
| FET resistance | $I^2 \times R_{DS(on)}$ |
| Diode loss | $V_f \times I_{OUT} \times (1 - D)$ |
| Inductor loss | $I^2 \times DC \text{ resistance} + AC \text{ core loss}$ |
| Capacitor loss | $I_{RMS}^2 \times ESR$ |
| IC loss (I_Q) | Datasheet specification for I_Q for when the IC is operating |

Figure 2. Efficiency of TPS54160 at the three example frequencies



each example, the capacitor loss is negligible. To show the effects of high-frequency switching, the efficiency of each example was measured and is illustrated in Figure 2. The figure clearly shows that the efficiency decreases as switching frequency is increased. To improve efficiency at any frequency, look for a DC/DC converter with a low drain-to-source ON resistance, a gate charge, or a quiescent-current specification at full load; or search for capacitors and inductors with lower equivalent resistance.

Component size

Table 4 shows the total board area required for the three designs along with the pad areas of the capacitor and inductor. The recommended pad area of a capacitor or inductor is slightly larger than the individual component itself and is accounted for in each of the three design examples. The total area was derived by adding the area occupied by each component, which includes the pad sizes for the IC, the filter, and all other small resistors

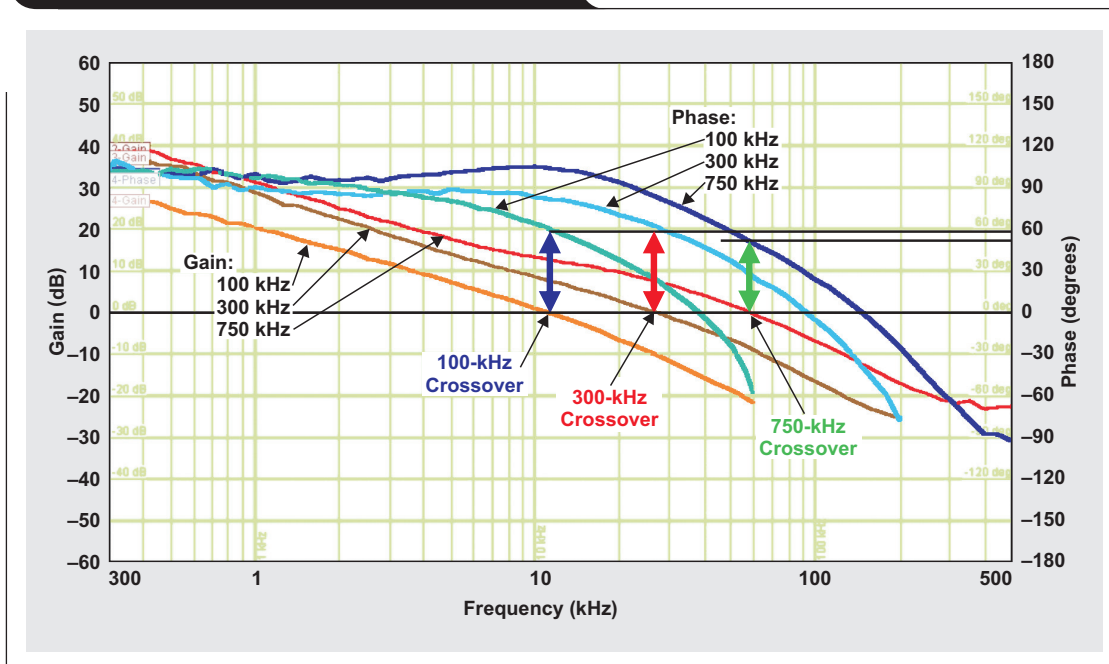
and capacitors, and multiplying the result by a factor of 2 to account for component spacing. The total area savings of almost 250 mm² between the 100-kHz and 750-kHz designs is significant, providing a 50% reduction in filter size and a 55% reduction in board space. However, the law of diminishing returns applies, since the capacitance and inductance values cannot be reduced to nothing! In other words, pushing the frequency higher will not continually reduce the overall size, since there is a limit to the availability of appropriately sized, mass-produced inductors and capacitors. Note that the 33-μH and 15-μH inductors occupy the same area. This is possible because the 33-μH inductor is 3.5 mm tall, whereas the 15-μH inductor is only 2.4 mm tall. These two inductors were chosen to illustrate the point that the inductance is proportional to the volume.

Transient response

The transient response is a good indicator of the performance level of a power supply. A Bode plot of each power

Table 4. Component size and total area requirements

| SWITCHING FREQUENCY (kHz) | CAPACITOR C2 (μF)/SIZE | CAPACITOR AREA (mm ²) | INDUCTOR L1 (μH) | INDUCTOR AREA (mm ²) | TOTAL AREA (mm ²) |
|---------------------------|------------------------|-----------------------------------|------------------|----------------------------------|-------------------------------|
| 100 | 47/1206 | 18.9 | 100 | 150 | 420 |
| 300 | 10/0805 | 11.5 | 33 | 43.5 | 192 |
| 750 | 4.7/0603 | 6.5 | 15 | 43.5 | 182 |

Figure 3. Bode plots at 100, 300, and 750 kHz

supply was taken to show a comparison at higher switching frequencies (see Figure 3). As shown, the phase margin of each power supply is between 45 and 55°, indicating a well-damped transient response. The crossover frequency is approximately one-eighth of the switching frequency. When using a fast switching DC/DC converter, the designer should make sure the power IC's error amplifier has enough bandwidth to support a high crossover frequency. The unity gain bandwidth of the TPS54160's error amplifier is typically 2.7 MHz. The actual transient-response times are shown in Table 5 with the associated values for voltage-peak overshoot. The overshoot value is significantly lower with the higher switching frequency, due to the wider bandwidth.

Jitter considerations

Noise can be a problem with high conversion ratios and higher frequencies. When selecting a high switching frequency, the designer should consider jitter and the minimum ON time of the DC/DC converter. Jitter noise becomes a larger percentage of the switching pulse when the duty cycle is small. Table 6 shows the ratio of the jitter to the ON time for a 48-V-to-5-V conversion. A 0.5-V diode drop and a 20-ns jitter on the phase node are assumed.

Conclusion

There are trade-offs to designing high-frequency switching converters. Some of the advantages shown in this article are smaller size, faster transient response, and smaller voltage over-/undershoots. The main penalties paid for these are reduced efficiency and increased heat dissipation. There are also potential pitfalls in pushing the envelope,

Table 5. Transient response

| SWITCHING FREQUENCY (kHz) | CROSSOVER FREQUENCY (kHz) | PHASE MARGIN (degrees) | RESPONSE TIME (μs) | VOLTAGE PEAK (mV) |
|---------------------------|---------------------------|------------------------|--------------------|-------------------|
| 100 | 10 | 60 | 1000 | 350 |
| 300 | 30 | 60 | 300 | 300 |
| 750 | 60 | 50 | 150 | 240 |

Table 6. Ratio of jitter to ON time at small duty cycles

| SWITCHING FREQUENCY (kHz) | ON TIME | JITTER/ON TIME (%) |
|---------------------------|---------|--------------------|
| 100 | 1.1 μs | 2 |
| 300 | 365 ns | 5 |
| 750 | 150 ns | 13 |

such as pulse skipping and noise issues. Before a wide-input-voltage DC/DC converter for high-frequency applications is selected, the manufacturer's datasheet should be checked for important specifications such as the minimum ON time, the gain bandwidth of the error amplifier, the FET resistance, and the FET switching loss. ICs that perform well with these specifications will cost a premium but will be worth the price and much easier to use when the designer is cornered with a tough design problem.

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS54160

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