

# CSD19537Q3 100-V N-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-low  $Q_g$  and  $Q_{gd}$
- Low thermal resistance
- Avalanche rated
- Lead free terminal plating
- RoHS compliant
- Halogen free
- SON 3.3-mm × 3.3-mm plastic package

## 2 Applications

- Primary Side Isolated Converters
- Motor Control

## 3 Description

This 100-V, 12.1-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

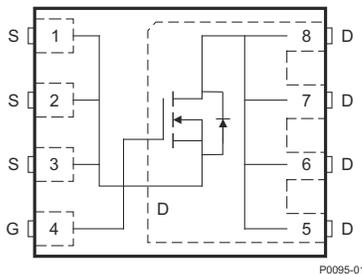


Figure 3-1. Top View

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$Q_g$	Gate Charge Total (10 V)	16	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	2.9	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{ V}$	13.8 mΩ
		$V_{GS} = 10\text{ V}$	12.1 mΩ
$V_{GS(th)}$	Threshold Voltage	3	V

## Ordering Information<sup>(1)</sup>

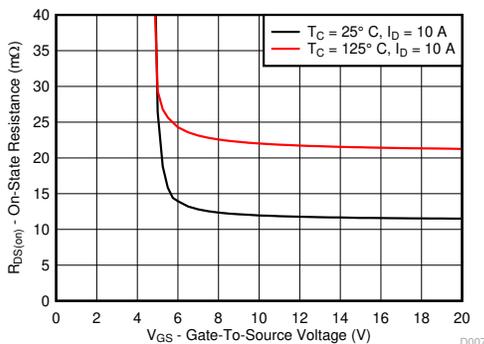
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD19537Q3	13-Inch Reel	2500	SON 3.3- x 3.3-mm Plastic Package	Tape and Reel
CSD19537Q3T	13-Inch Reel	250		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

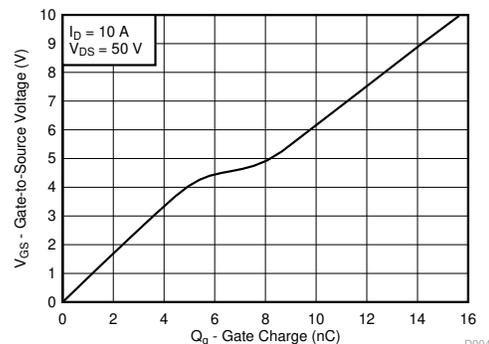
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package Limited)	50	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	53	A
	Continuous Drain Current <sup>(1)</sup>	9.7	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	219	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	83	W
$T_J$ , $T_{stg}$	Operating Junction Temperature, Storage Temperature	-55 to 150	°C
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 33\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$	55	mJ

- (1) Typical  $R_{\theta JA} = 45^\circ\text{C/W}$  on a 1-in<sup>2</sup>, 2-oz Cu pad on a 0.06-in thick FR4 PCB.  
 (2) Max  $R_{\theta JC} = 1.5^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .



$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

### Changes from Revision A (May 2016) to Revision B (November 2022) Page

- Corrected legend on [Figure 5-11](#) ..... **4**

### Changes from Revision \* (August 2015) to Revision A (May 2016) Page

- Corrected typo in X axis legend on [Figure 5-11](#) ..... **4**

## 5 Specifications

### 5.1 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V			1	μA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.6	3	3.6	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 6 V, I <sub>D</sub> = 10 A		13.8	16.6	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		12.1	14.5	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A		45		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz		1290	1680	pF
C <sub>oss</sub>	Output capacitance			251	326	pF
C <sub>rss</sub>	Reverse transfer capacitance			13.3	17.3	pF
R <sub>G</sub>	Series gate resistance			1.2	2.4	Ω
Q <sub>g</sub>	Gate charge total (10 V)	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 10 A		16	21	nC
Q <sub>gd</sub>	Gate charge gate-to-drain			2.9		nC
Q <sub>gs</sub>	Gate charge gate-to-source			5.5		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			3.8		nC
Q <sub>oss</sub>	Output charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		44		nC
t <sub>d(on)</sub>	Turn on delay time	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 10 A, R <sub>G</sub> = 0 Ω		5		ns
t <sub>r</sub>	Rise time			3		ns
t <sub>d(off)</sub>	Turn off delay time			10		ns
t <sub>f</sub>	Fall time			3		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 10 A, V <sub>GS</sub> = 0 V		0.8	1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 50 V, I <sub>F</sub> = 10 A, di/dt = 300 A/μs		134		nC
t <sub>rr</sub>	Reverse recovery time			36		ns

### 5.2 Thermal Information

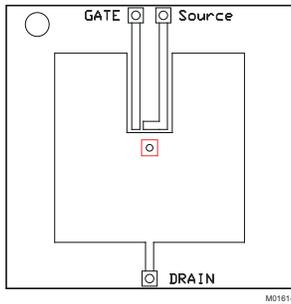
T<sub>A</sub> = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-case thermal resistance <sup>(1)</sup>			1.5	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance, Note 1 and Note 2 <sup>(1) (2)</sup>			55	°C/W

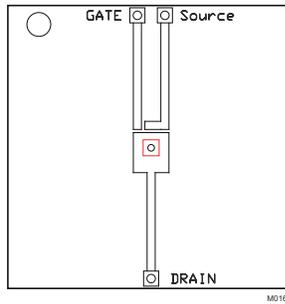
- (1) R<sub>θJC</sub> is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

**CSD19537Q3**

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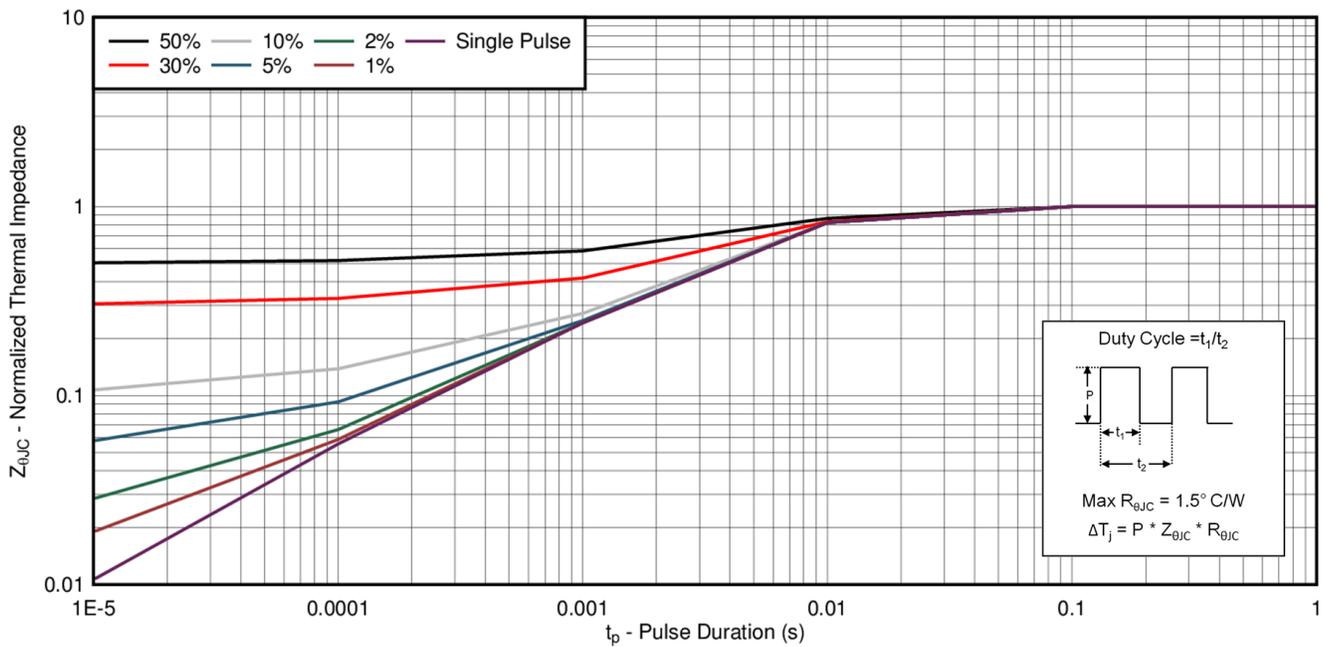
Max  $R_{\theta JA} = 55^{\circ}\text{C/W}$  when mounted on 1 in<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-oz (0.071-mm) thick Cu.



Max  $R_{\theta JA} = 160^{\circ}\text{C/W}$  when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

**5.3 Typical MOSFET Characteristics**

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)



**Figure 5-1. Transient Thermal Impedance**

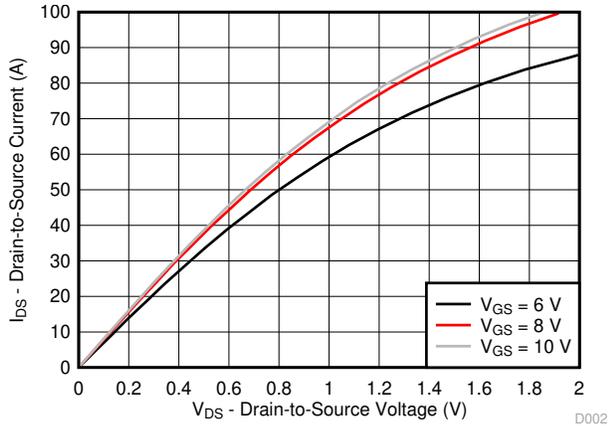


Figure 5-2. Saturation Characteristics

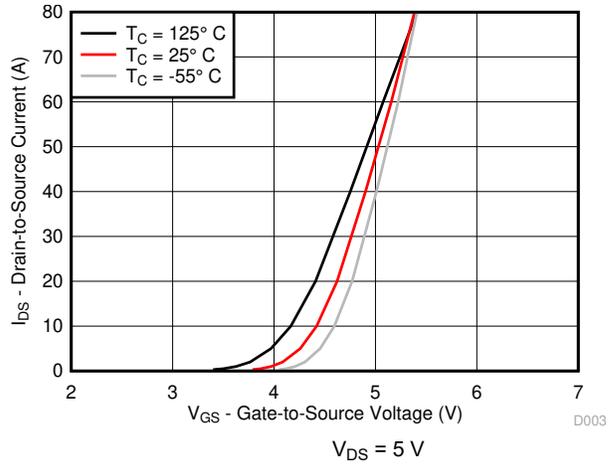


Figure 5-3. Transfer Characteristics

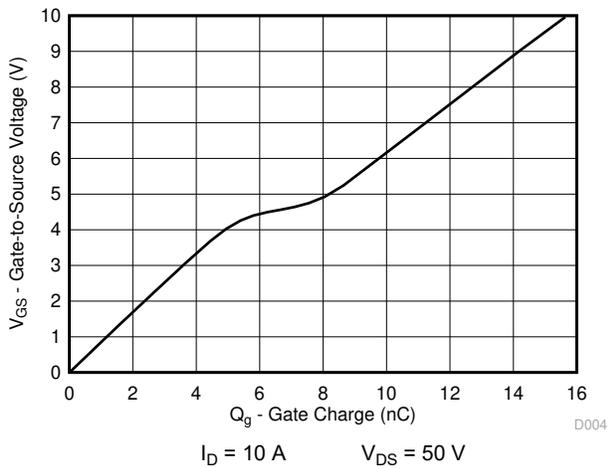


Figure 5-4. Gate Charge

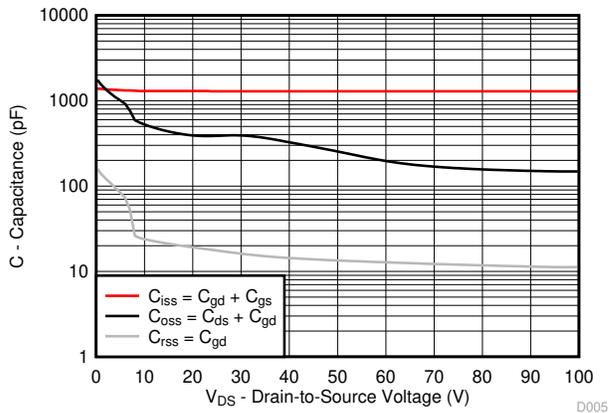


Figure 5-5. Capacitance

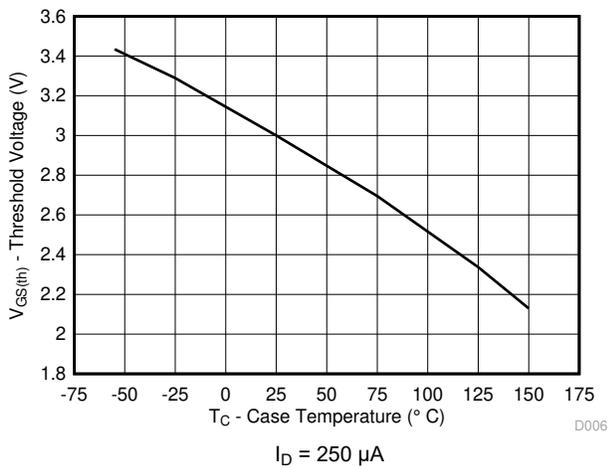


Figure 5-6. Threshold Voltage vs Temperature

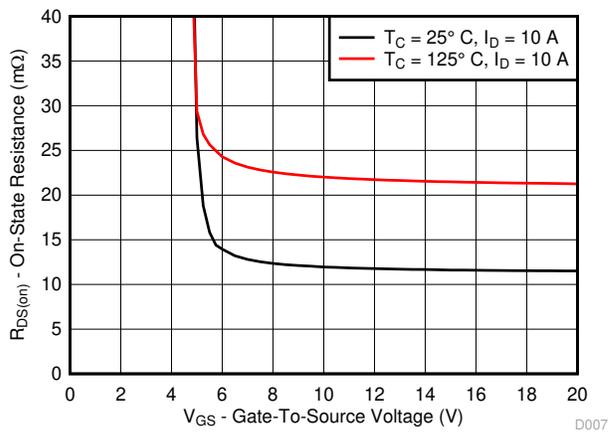
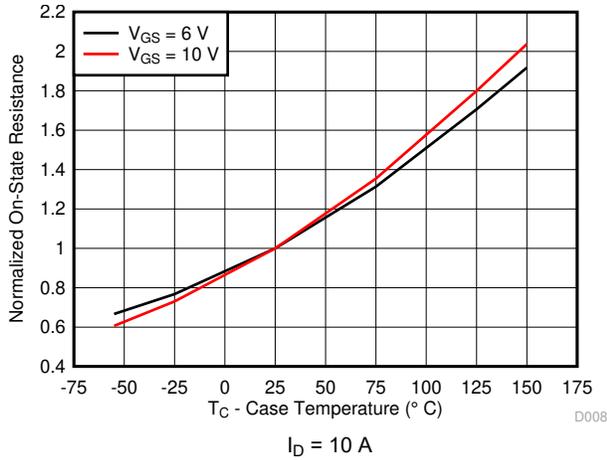
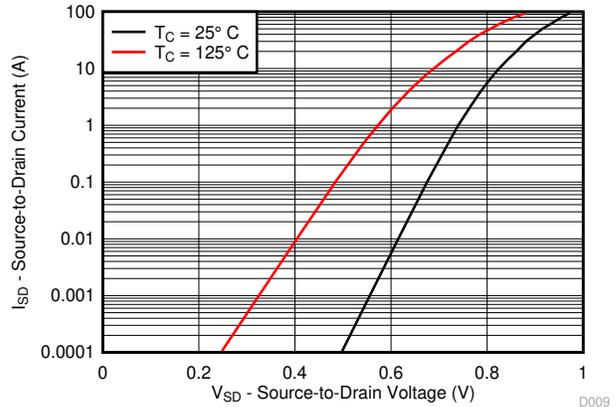


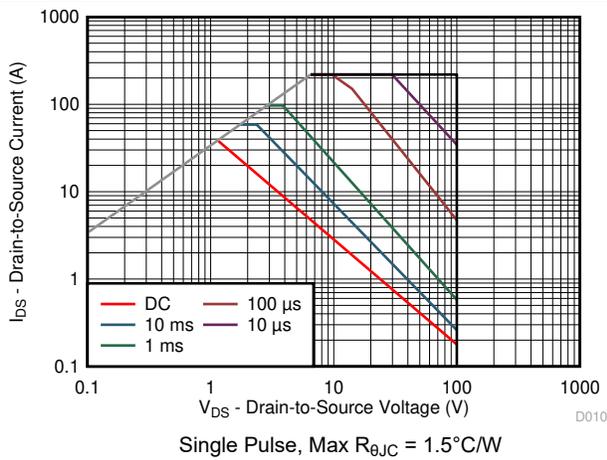
Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



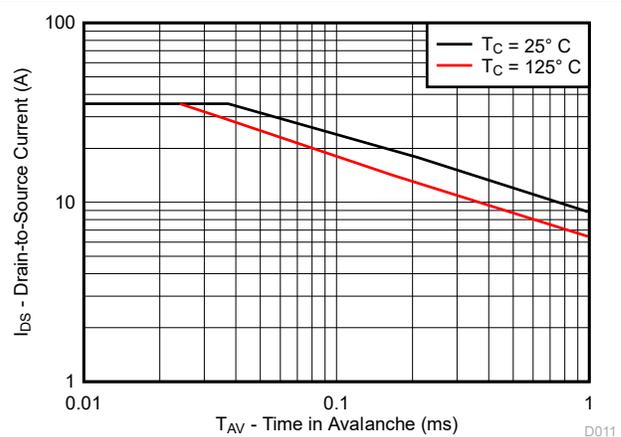
**Figure 5-8. Normalized On-State Resistance vs Temperature**



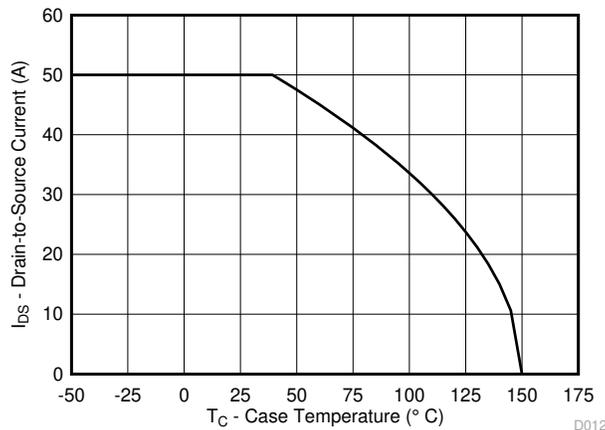
**Figure 5-9. Typical Diode Forward Voltage**



**Figure 5-10. Maximum Safe Operating Area**



**Figure 5-11. Single Pulse Unclamped Inductive Switching**



**Figure 5-12. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

[TI E2E™ Online Community](#) TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[Design Support](#) TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.2 Trademarks

NexFET™ is a trademark of Texas Instruments.

E2E™ are trademarks of Texas Instruments.

All trademarks are the property of their respective owners.

### 6.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

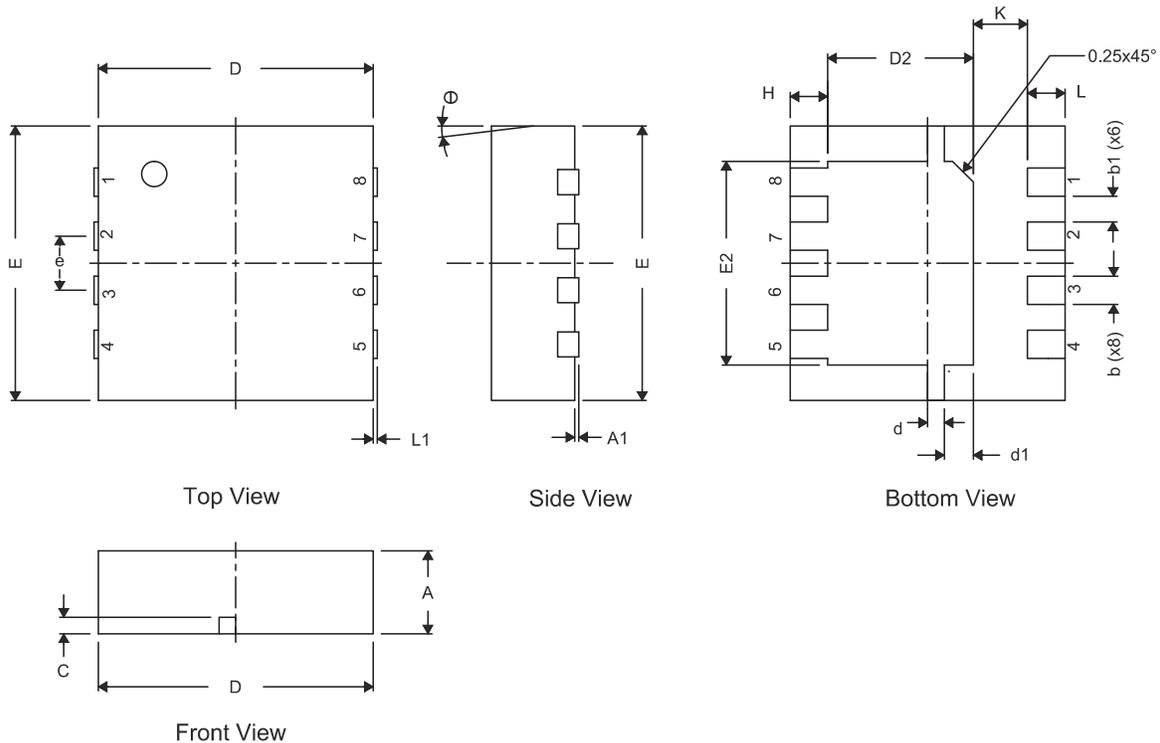
### 6.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

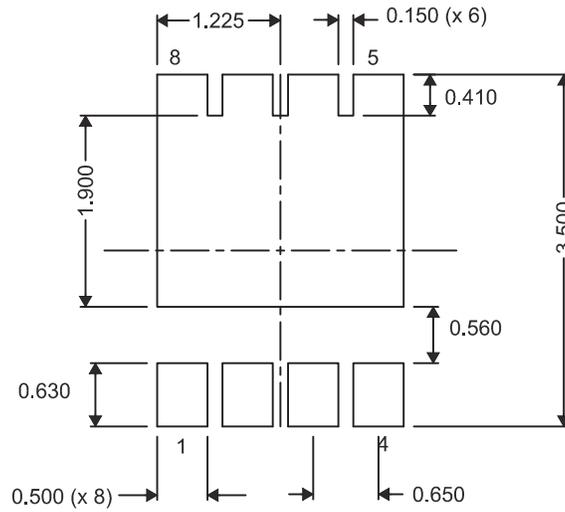
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q3 Package Dimensions



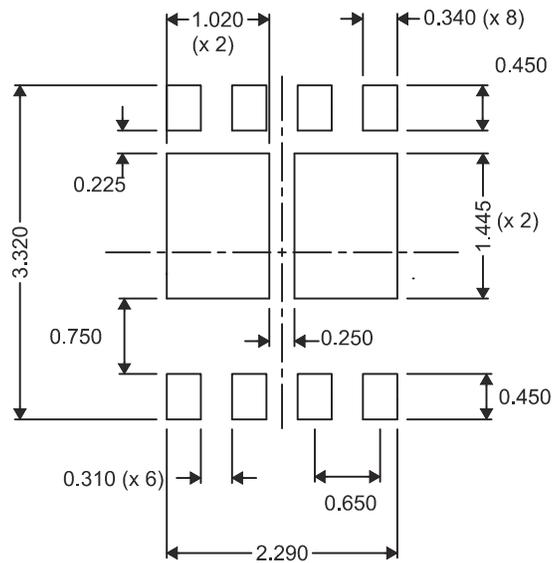
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
$\theta$	0	—	0	0	—	0

## 7.2 Recommended PCB Pattern



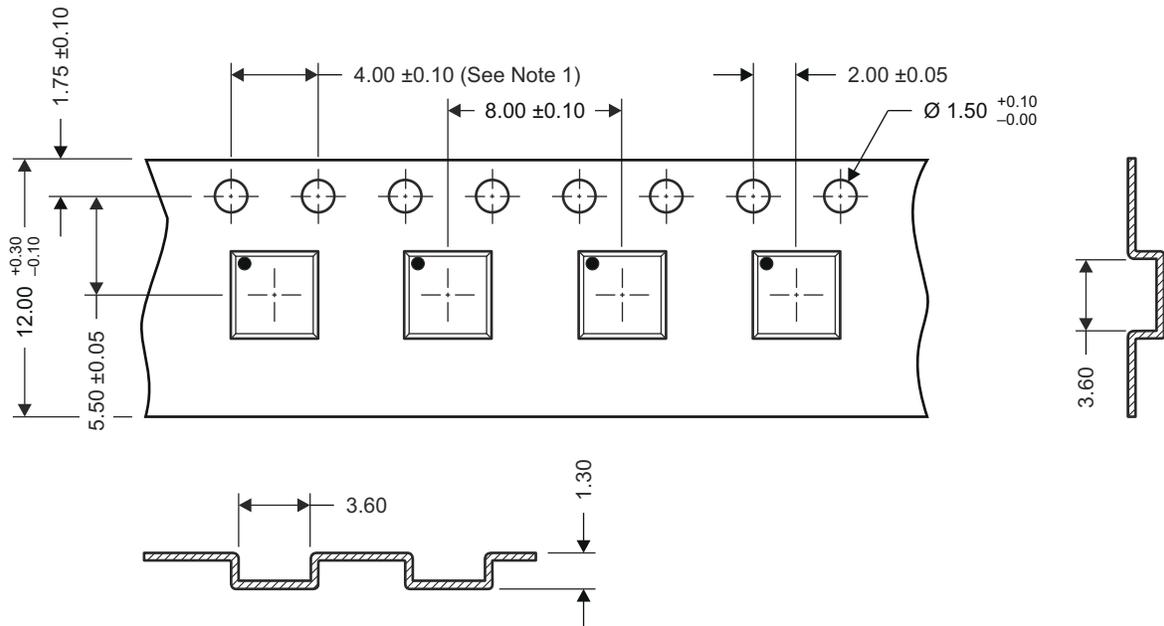
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

## 7.4 Q3 Tape and Reel Information



M0144-01

### Notes:

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness:  $0.30 \pm 0.05$  mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19537Q3	ACTIVE	VSON-CLIP	DQG	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537	<a href="#">Samples</a>
CSD19537Q3T	ACTIVE	VSON-CLIP	DQG	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD19537	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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