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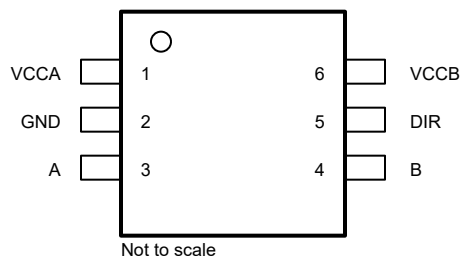
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2017) to Revision E (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated the thermals in the <i>Thermal Information</i> section.....	5
• Updated the <i>Switching Characteristics</i> sections: extended some minimum specifications for lower delays.....	7
Changes from Revision C (September 2016) to Revision D (July 2017)	Page
• Added Junction temperature, T_J in <i>Absolute Maximum Ratings</i>	4
• Added revised steps for power-up sequence in <i>Power Supply Recommendations</i>	16
Changes from Revision B (September 2012) to Revision C (September 2016)	Page
• Changed data sheet title From: SN74LVC1T45-Q1 Single-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs To: SN74LVC1T45-Q1 1.65-V to 5.5-V Single-Bit Dual-Supply Level Shifter.....	1
• Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted Ordering Information table; see POA the end of the data sheet.....	1

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 5-1. DCK Package, 6-Pin SC70 (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A	3	I/O	Output level depends on V_{CC1} voltage
B	4	I/O	Input threshold value depends on V_{CC2} voltage
DIR	5	I	GND (low level) determines B-port to A-port direction
GND	2	G	Device GND
V_{CCA}	1	P	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
V_{CCB}	6	P	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, V_{CCA} , V_{CCB}		−0.5	6.5	V
Input voltage, V_I ⁽²⁾		−0.5	6.5	V
Voltage applied to any output in the high-impedance or power-off state, V_O ⁽²⁾		−0.5	6.5	V
Voltage applied to any output in the high or low state, V_O ⁽²⁾ ⁽³⁾	A port	−0.5	$V_{CCA} + 0.5$	V
	B port	−0.5	$V_{CCB} + 0.5$	
Input clamp current, I_{IK} ($V_I < 0$)			−50	mA
Output clamp current, I_{OK} ($V_O < 0$)			−50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾ ⁽²⁾ ⁽³⁾

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	1.65	5.5	V
V_{CCB}	Supply voltage	1.65	5.5	V
V_{IH}	High-level input voltage, data inputs ⁽⁴⁾	$V_{CCI} = 1.65\text{ V to }1.95\text{ V}$	$V_{CCI} \times 0.65$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	2	
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$V_{CCI} \times 0.7$	
V_{IL}	Low-level input voltage, data inputs ⁽⁴⁾	$V_{CCI} = 1.65\text{ V to }1.95\text{ V}$	$V_{CCI} \times 0.35$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	0.8	
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$V_{CCI} \times 0.3$	
V_{IH}	High-level input voltage, DIR (referenced to V_{CCA}) ⁽⁵⁾	$V_{CCI} = 1.65\text{ V to }1.95\text{ V}$	$V_{CCA} \times 0.65$	V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	2	
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	$V_{CCA} \times 0.7$	

6.3 Recommended Operating Conditions (continued)

See ⁽¹⁾ ⁽²⁾ ⁽³⁾

			MIN	MAX	UNIT
V _{IL}	Low-level input voltage, DIR (referenced to V _{CCA}) ⁽⁵⁾	V _{CCI} = 1.65 V to 1.95 V	V _{CCA} × 0.35		V
		V _{CCI} = 2.3 V to 2.7 V	0.7		
		V _{CCI} = 3 V to 3.6 V	0.8		
		V _{CCI} = 4.5 V to 5.5 V	V _{CCA} × 0.3		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CCO}	V
I _{OH}	High-level output current	V _{CCO} = 1.65 V to 1.95 V	−4		mA
		V _{CCO} = 2.3 V to 2.7 V	−8		
		V _{CCO} = 3 V to 3.6 V	−24		
		V _{CCO} = 4.5 V to 5.5 V	−32		
I _{OL}	Low-level output current	V _{CCO} = 1.65 V to 1.95 V	4		mA
		V _{CCO} = 2.3 V to 2.7 V	8		
		V _{CCO} = 3 V to 3.6 V	24		
		V _{CCO} = 4.5 V to 5.5 V	32		
Δt/Δv	Input transition rise or fall rate	Data inputs	V _{CCI} = 1.65 V to 1.95 V	20	ns/V
			V _{CCI} = 2.3 V to 2.7 V	20	
			V _{CCI} = 3 V to 3.6 V	10	
			V _{CCI} = 4.5 V to 5.5 V	5	
		Control inputs, V _{CCI} = 1.65 V to 5.5 V		5	
T _A	Operating free-air temperature		−40	125	°C

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) All unused data inputs of the device must be held at V_{CCI} or GND to assure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).
- (4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
- (5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1T45-Q1	UNIT
		DCK (SC70)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	210.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	139.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	72	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	54.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	71.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range with all limits at $T_A = -40^\circ\text{C}$ to 125°C (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _{OH}	V _I = V _{IH}	I _{OH} = −100 μA, V _{CCA} = 1.65 V to 4.5 V, V _{CCB} = 1.65 V to 4.5 V		V _{CCO} − 0.1		V	
		I _{OH} = −4 mA, V _{CCA} = 1.65 V, V _{CCB} = 1.65 V		1.2			
		I _{OH} = −8 mA, V _{CCA} = 2.3 V, V _{CCB} = 2.3 V		1.9			
		I _{OH} = −24 mA, V _{CCA} = 3 V, V _{CCB} = 3 V		2.3			
		I _{OH} = −32 mA, V _{CCA} = 4.5 V, V _{CCB} = 4.5 V		3.8			
V _{OL}	V _I = V _{IL}	I _{OL} = 100 μA, V _{CCA} = 1.65 V to 4.5 V, V _{CCB} = 1.65 V to 4.5 V		0.1		V	
		I _{OL} = 4 mA, V _{CCA} = 1.65 V, V _{CCB} = 1.65 V		0.45			
		I _{OL} = 8 mA, V _{CCA} = 2.3 V, V _{CCB} = 2.3 V		0.4			
		I _{OL} = 24 mA, V _{CCA} = 3 V, V _{CCB} = 3 V		0.65			
		I _{OL} = 32 mA, V _{CCA} = 4.5 V, V _{CCB} = 4.5 V		0.65			
I _I	DIR at V _I = V _{CCA} or GND, V _{CCA} = 1.65 V to 5.5 V, V _{CCB} = 1.65 V to 5.5 V		T _A = 25°C		±1		μA
			T _A = −40°C to 125°C		±4		
I _{off}	V _I or V _O = 0 to 5.5 V	A port at V _{CCA} = 0 V, V _{CCB} = 0 to 5.5 V	T _A = 25°C		±1		μA
			T _A = −40°C to 125°C		±10		
		B port at V _{CCA} = 0 to 5.5 V, V _{CCB} = 0 V	T _A = 25°C		±1		
			T _A = −40°C to 125°C		±10		
I _{OZ}	A or B port at V _O = V _{CCO} or GND, V _{CCA} = 1.65 V to 5.5 V, V _{CCB} = 1.65 V to 5.5 V		T _A = 25°C		±1		μA
			T _A = −40°C to 125°C		±10		
I _{CCA}	V _I = V _{CCI} or GND, I _O = 0	V _{CCA} = 1.65 V to 5.5 V, V _{CCB} = 1.65 V to 5.5 V		10		μA	
		V _{CCA} = 5.5 V, V _{CCB} = 0 V		4			
		V _{CCA} = 0 V, V _{CCB} = 5.5 V		−10			
I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	V _{CCA} = 1.65 V to 5.5 V, V _{CCB} = 1.65 V to 5.5 V		10		μA	
		V _{CCA} = 5.5 V, V _{CCB} = 0 V		−10			
		V _{CCA} = 0 V, V _{CCB} = 5.5 V		4			
I _{CCA} + I _{CCB}	V _I = V _{CCI} or GND, I _O = 0, V _{CCA} = 1.65 V to 5.5 V, V _{CCB} = 1.65 V to 5.5 V				20	μA	
ΔI _{CCA}	V _{CCA} = 3 V to 5.5 V, V _{CCB} = 3 V to 5.5 V	A port at V _{CCA} − 0.6 V, DIR at V _{CCA} , B port = open		50		μA	
		DIR at V _{CCA} − 0.6 V, B port = open, A port at V _{CCA} or GND		50			
ΔI _{CCB}	B port at V _{CCB} − 0.6 V, DIR at GND, A port = open, V _{CCA} = 3 V to 5.5 V, V _{CCB} = 3 V to 5.5 V				50	μA	
C _i	DIR at V _I = V _{CCA} or GND, T _A = 25°C, V _{CCA} = 3.3 V, V _{CCB} = 3.3 V			2.5		pF	
C _{io}	A or B port at V _O = V _{CCA/B} or GND, T _A = 25°C, V _{CCA} = 3.3 V, V _{CCB} = 3.3 V			6		pF	
C _{pdA} ⁽³⁾	C _L = 0 pF, f = 10 MHz, t _r = t _f = 1 ns	A-port input, B-port output	V _{CCA} = V _{CCB} = 1.8 V		3		pF
			V _{CCA} = V _{CCB} = 2.5 V		4		
			V _{CCA} = V _{CCB} = 3.3 V		4		
			V _{CCA} = V _{CCB} = 5 V		4		
		B-port input, A-port output	V _{CCA} = V _{CCB} = 1.8 V		18		
			V _{CCA} = V _{CCB} = 2.5 V		19		
			V _{CCA} = V _{CCB} = 3.3 V		20		
			V _{CCA} = V _{CCB} = 5 V		21		

6.5 Electrical Characteristics (continued)

over operating free-air temperature range with all limits at $T_A = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pdB} ⁽³⁾	$C_L = 0\text{ pF}$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	A-port input, B-port output	$V_{CCA} = V_{CCB} = 1.8\text{ V}$		18		pF
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$		19		
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$		20		
			$V_{CCA} = V_{CCB} = 5\text{ V}$		21		
		B-port input, A-port output	$V_{CCA} = V_{CCB} = 1.8\text{ V}$		3		
			$V_{CCA} = V_{CCB} = 2.5\text{ V}$		4		
			$V_{CCA} = V_{CCB} = 3.3\text{ V}$		4		
			$V_{CCA} = V_{CCB} = 5\text{ V}$		4		

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

(3) Power dissipation capacitance per transceiver

6.6 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2	ns
t_{PHL}			2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	
t_{PLH}	B	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	ns
t_{PHL}			2.8	17.3	2.1	15.9	2	15.6	1.8	15.2	
t_{PHZ}	DIR	A	5.2	22.7	4.8	21.5	4.7	21.4	5.1	20.1	ns
t_{PLZ}			2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	
t_{PHZ}	DIR	B	5.2	27.9	4.9	14.5	3.6	13.3	2.3	11.2	ns
t_{PLZ}			4.2	19	2.2	12.2	2.3	11.4	2	9.4	
t_{PZH} ⁽¹⁾	DIR	A		39.7		31.2		29.9		27.5	ns
t_{PZL} ⁽¹⁾				45.2		30.4		28.9		26.4	
t_{PZH} ⁽¹⁾	DIR	B		34.2		26.8		25		24.1	ns
t_{PZL} ⁽¹⁾				40.7		33		31.5		30.1	

(1) The enable time is a calculated value, derived using the formula shown in Section 8.1.1.

6.7 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over operating free-air temperature range (unless otherwise noted; see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	ns
t_{PHL}			2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	
t_{PLH}	B	A	2.2	13.3	1.5	11.5	1.4	11	1	10.5	ns
t_{PHL}			2.2	11.5	1.4	10.7	1.3	10	0.9	9.2	
t_{PHZ}	DIR	A	3	11.1	3.1	11.1	2.8	11.1	3.2	11.1	ns
t_{PLZ}			1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	
t_{PHZ}	DIR	B	5.2	26.7	4.1	14.4	3.9	13.2	2.4	10.1	ns
t_{PLZ}			3.9	21.9	3.2	12.6	2.8	11.4	1.8	8.3	

6.7 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (continued)

over operating free-air temperature range (unless otherwise noted; see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ±0.15 V		V _{CCB} = 2.5 V ±0.2 V		V _{CCB} = 3.3 V ±0.3 V		V _{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PZH} ⁽¹⁾	DIR	A	35.2		24.1		22.4		18.8		ns
t _{PZL} ⁽¹⁾			38.2		24.9		23.2		19.3		
t _{PZH} ⁽¹⁾	DIR	B	27.9		20.4		18.3		16.9		ns
t _{PZL} ⁽¹⁾			27		21.6		19.5		18.7		

6.8 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over operating free-air temperature range (unless otherwise noted; see [Figure 7-1](#))

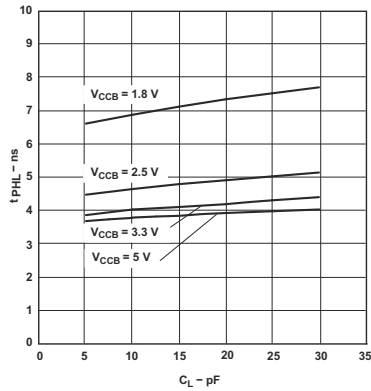
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ±0.15 V		V _{CCB} = 2.5 V ±0.2 V		V _{CCB} = 3.3 V ±0.3 V		V _{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	ns
t _{PHL}			2	15.6	1.3	10	0.8	8	0.7	7	
t _{PLH}	B	A	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	ns
t _{PHL}			1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	
t _{PHZ}	DIR	A	2.9	10.3	3	10.3	2.8	10.3	3.4	10.3	ns
t _{PLZ}			1.8	8.6	1.6	8.6	2.2	8.7	2.2	8.7	
t _{PHZ}	DIR	B	5.4	27.5	3.9	13.1	2.9	11.8	2.4	9.8	ns
t _{PLZ}			3.3	17.5	2.9	10.8	2.4	10.1	1.7	7.9	
t _{PZH} ⁽¹⁾	DIR	A	26.8		20.2		18.9		16.3		ns
t _{PZL} ⁽¹⁾			37.6		21.5		19.8		17.3		
t _{PZH} ⁽¹⁾	DIR	B	27.1		19.6		17.5		16.1		ns
t _{PZL} ⁽¹⁾			25.9		20.3		18.3		17.3		

6.9 Switching Characteristics: $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range (unless otherwise noted; see [Figure 7-1](#))

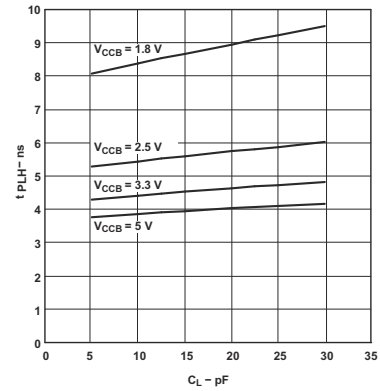
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ±0.15 V		V _{CCB} = 2.5 V ±0.2 V		V _{CCB} = 3.3 V ±0.3 V		V _{CCB} = 5 V ±0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t _{PHL}			1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	
t _{PLH}	B	A	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	ns
t _{PHL}			1.7	10	0.9	7.6	0.7	7	0.5	6.5	
t _{PHZ}	DIR	A	2.1	8.4	2.2	8.4	2.2	8.5	2.2	8.4	ns
t _{PLZ}			0.9	6.8	1	6.8	0.7	6.7	0.7	6.7	
t _{PHZ}	DIR	B	4.8	26.2	2.5	14.8	1	11.5	2.5	9.5	ns
t _{PLZ}			3.2	17.8	2.5	10.4	2.5	10	1.6	7.5	
t _{PZH} ⁽¹⁾	DIR	A	28		18.5		17.4		14.4		ns
t _{PZL} ⁽¹⁾			36.2		22.4		18.5		16		
t _{PZH} ⁽¹⁾	DIR	B	24.9		17.3		15.1		13.6		ns
t _{PZL} ⁽¹⁾			23.6		17.6		16		14.9		

6.10 Typical Characteristics



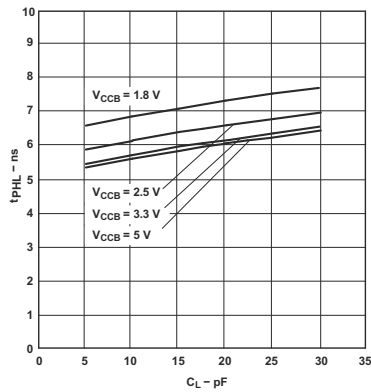
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 6-1. Typical Propagation Delay (A to B) vs Load Capacitance



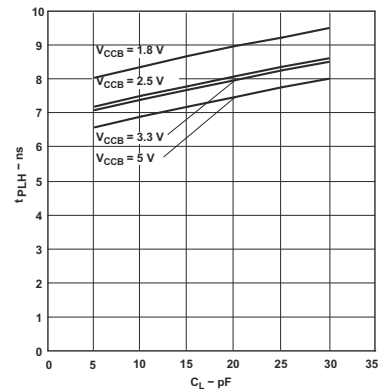
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 6-2. Typical Propagation Delay (A to B) vs Load Capacitance



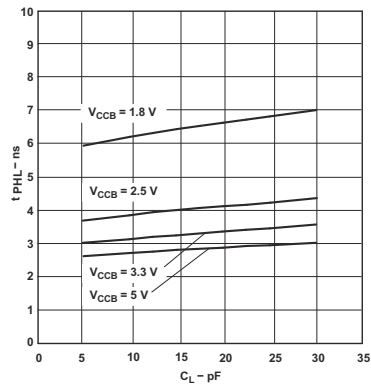
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 6-3. Typical Propagation Delay (B to A) vs Load Capacitance



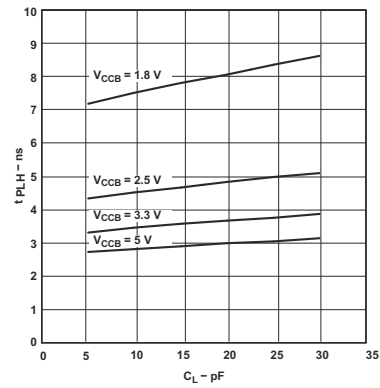
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 6-4. Typical Propagation Delay (B to A) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

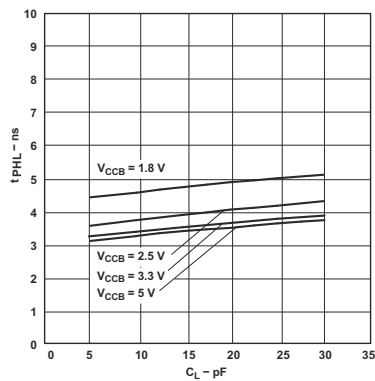
Figure 6-5. Typical Propagation Delay (A to B) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

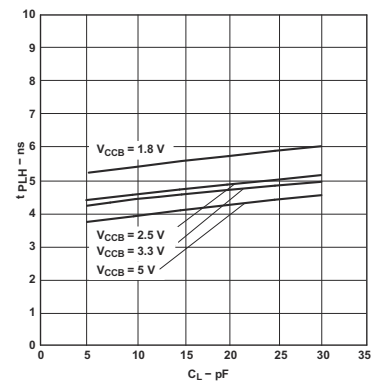
Figure 6-6. Typical Propagation Delay (A to B) vs Load Capacitance

6.10 Typical Characteristics (continued)



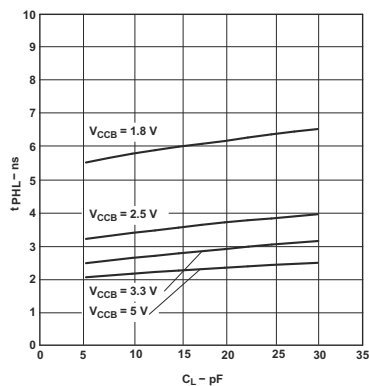
$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

Figure 6-7. Typical Propagation Delay (B to A) vs Load Capacitance



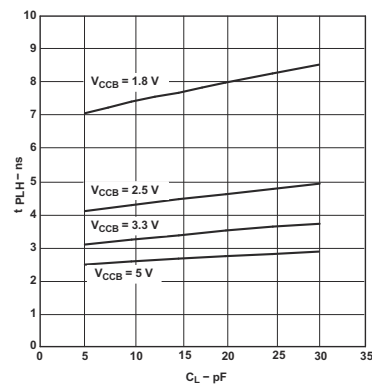
$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

Figure 6-8. Typical Propagation Delay (B to A) vs Load Capacitance



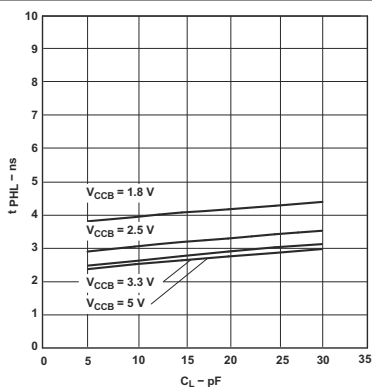
$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

Figure 6-9. Typical Propagation Delay (A to B) vs Load Capacitance



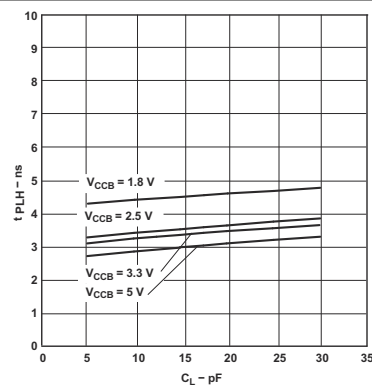
$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

Figure 6-10. Typical Propagation Delay (A to B) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

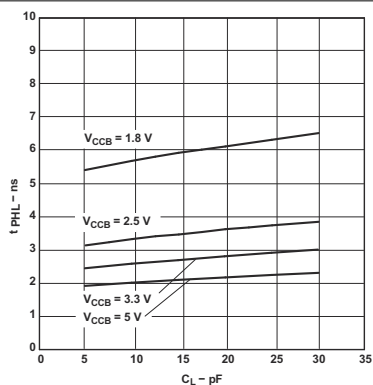
Figure 6-11. Typical Propagation Delay (B to A) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

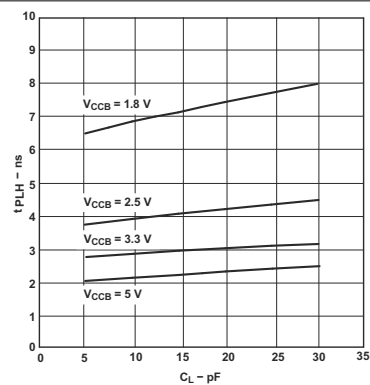
Figure 6-12. Typical Propagation Delay (B to A) vs Load Capacitance

6.10 Typical Characteristics (continued)



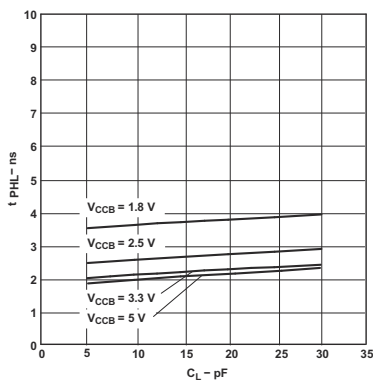
$T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

Figure 6-13. Typical Propagation Delay (A to B) vs Load Capacitance



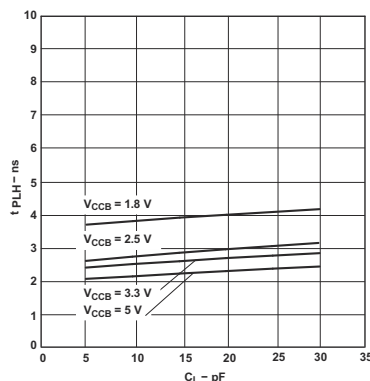
$T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

Figure 6-14. Typical Propagation Delay (A to B) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

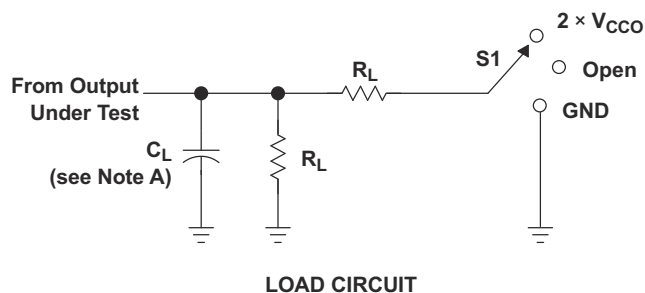
Figure 6-15. Typical Propagation Delay (B to A) vs Load Capacitance



$T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

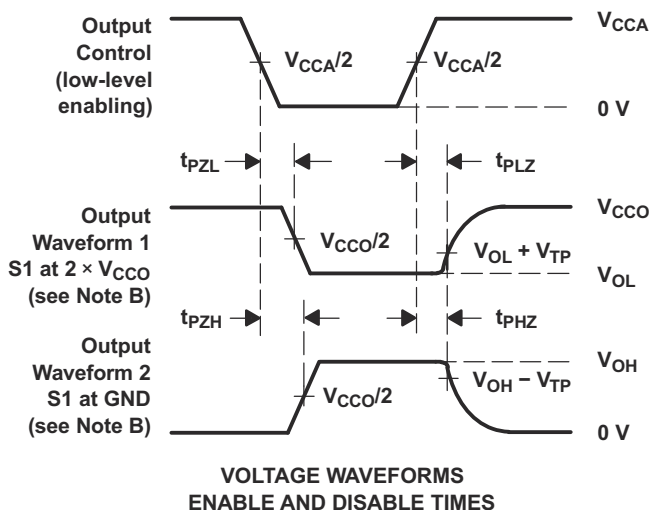
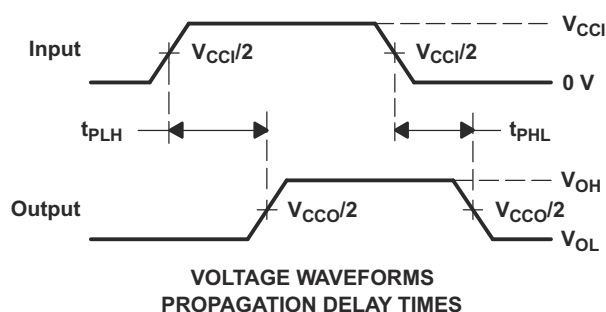
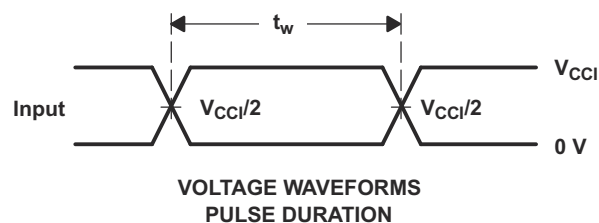
Figure 6-16. Typical Propagation Delay (B to A) vs Load Capacitance

Parameter Measurement Information



V_{CCO}	C_L	R_L	V_{TP}
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V
5 V \pm 0.5 V	15 pF	2 k Ω	0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1T45-Q1 is single-bit, dual-supply, non-inverting voltage level translation. Pin A and that direction control pin (DIR) are supported by V_{CCA} and pin B is supported by V_{CCB} . The A port is able to accept I/O voltages ranging from 1.65 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The high on the DIR allows data transmissions from A to B and a low on the DIR allows data transmissions from B to A.

7.2 Functional Block Diagram

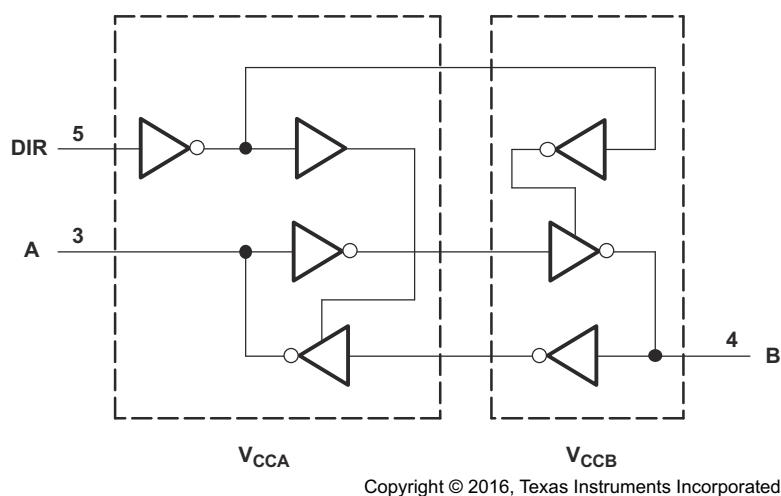


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The SN74LVC1T45-Q1 has a fully configurable dual-rail design that allows each port to operate over the full 1.65-V to 5.5-V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8-V, 2.5-V, 3.3-V, and 5-V).

SN74LVC1T45-Q1 can support high data rate applications. The translated signal data rate can be up to 420 Mbps when the signal is translated from 3.3 V to 5 V.

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

7.4 Device Functional Modes

Table 7-1 lists the operational modes of SN74LVC1T45-Q1.

Table 7-1. Function Table⁽¹⁾

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The max data rate can be up to 420 Mbps when device translates signals from 3.3 V to 5 V.

8.1.1 Enable Times

Calculate the enable times for the SN74LVC1T45-Q1 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

Figure 8-1 shows an example of the SN74LVC1T45-Q1 being used in a unidirectional logic level-shifting application.

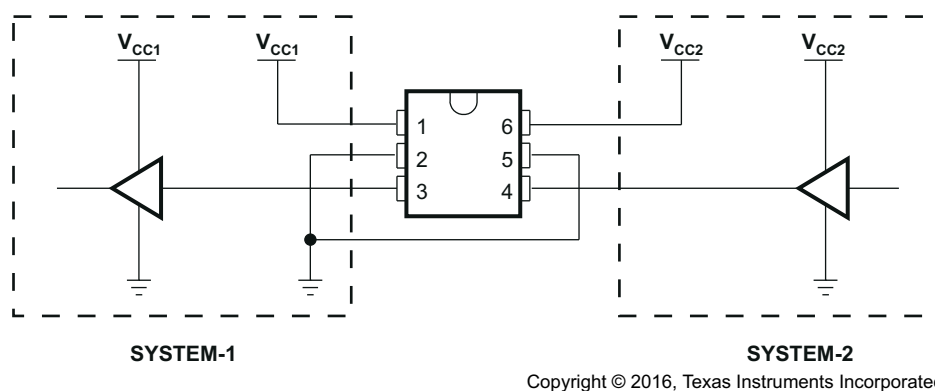


Figure 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the SN74LVC1T45-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74LVC1T45-Q1 device is driving to determine the output voltage range.

8.2.1.3 Application Curves

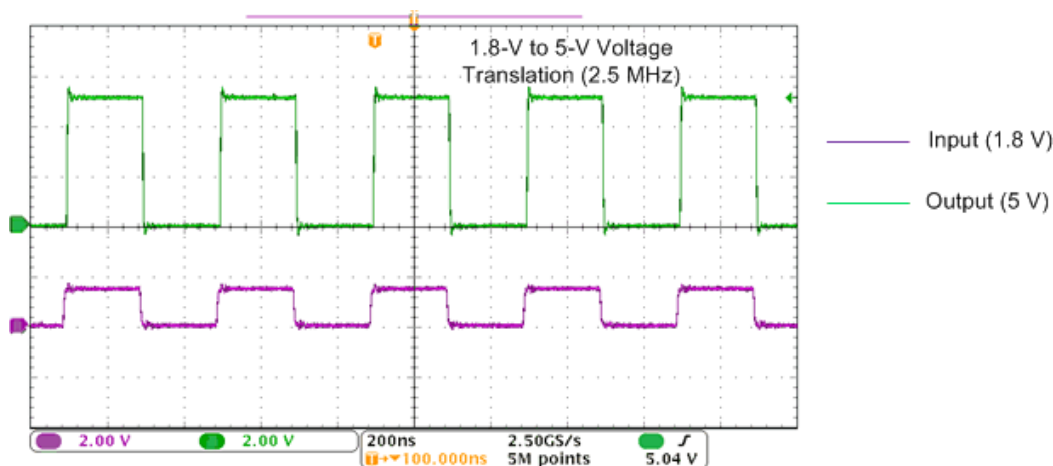


Figure 8-2. Translation Up (1.8 V to 5 V) at 2.5 MHz

8.2.2 Bidirectional Logic Level-Shifting Application

Figure 8-3 shows the SN74LVC1T45-Q1 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45-Q1 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

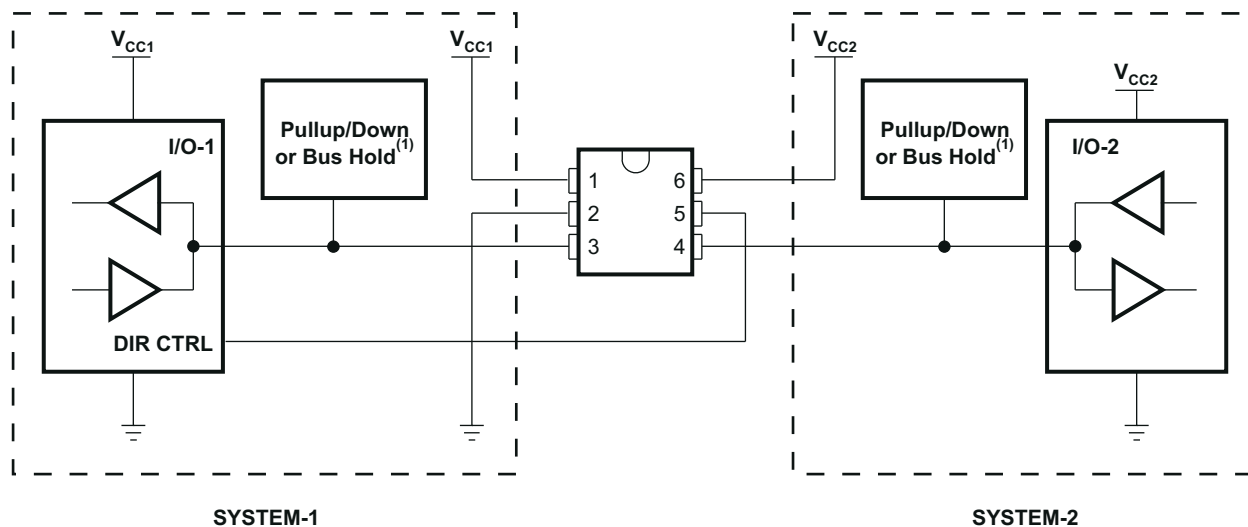


Figure 8-3. Bidirectional Logic Level-Shifting Application

8.2.2.1 Detailed Design Procedure

Table 8-2 shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 8-2. Data Transmission

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2 Application Curves

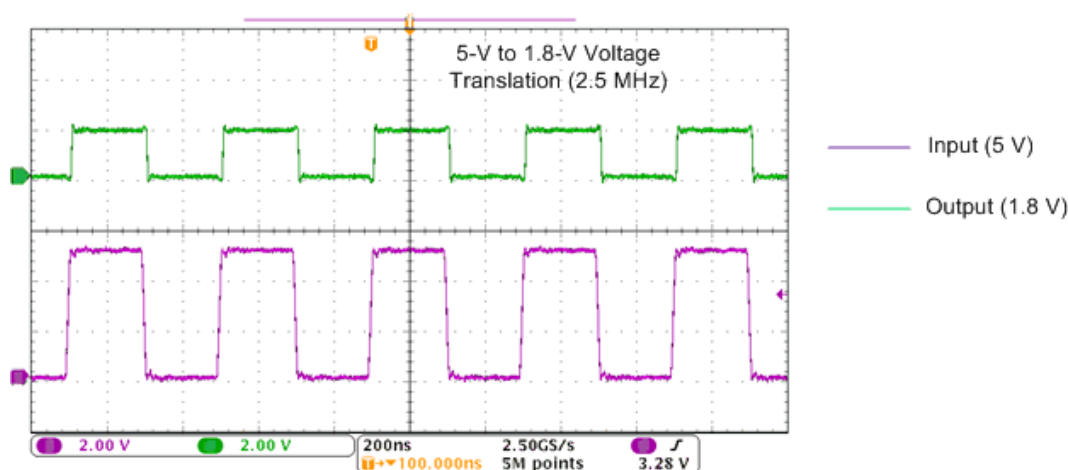


Figure 8-4. Translation Down (5 V to 1.8 V) at 2.5 MHz

8 Power Supply Recommendations

The SN74LVC1T45-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V, and V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. The A port and B port are designed to track V_{CCA} and V_{CCB} , respectively allowing for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For multiple V_{CC} pins then 0.01- μ F or 0.022- μ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

A proper power-up sequence is advisable as listed in the following:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCB} .
3. V_{CCA} can be ramped up along with V_{CCB} .

TI recommends that the inputs are grounded during power up. Take care to assure that any state changes do not affect system level operation.

9 Layout

9.1 Layout Guidelines

To assure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors must be used on power supplies.
- Short trace lengths must be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depends on the system requirements.

9.2 Layout Example

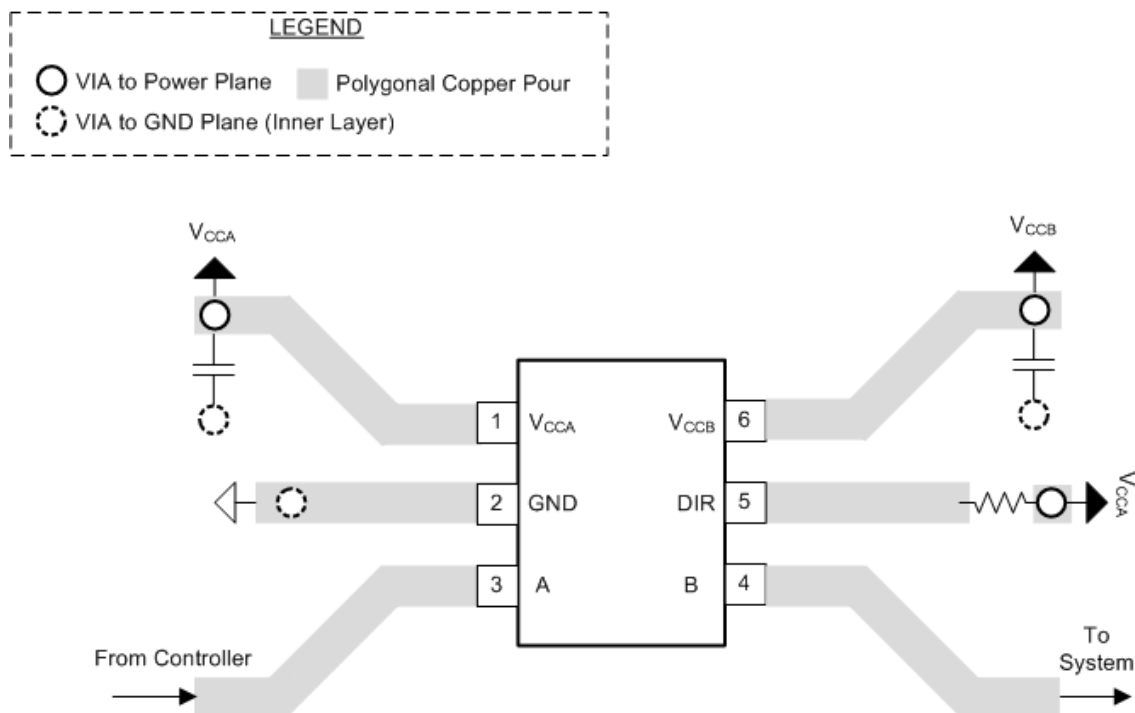


Figure 9-1. Layout Schematic

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1T45QDCKRQ1	ACTIVE	SC70	DKK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5TR	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1T45-Q1 :

- Catalog : [SN74LVC1T45](#)
- Enhanced Product : [SN74LVC1T45-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

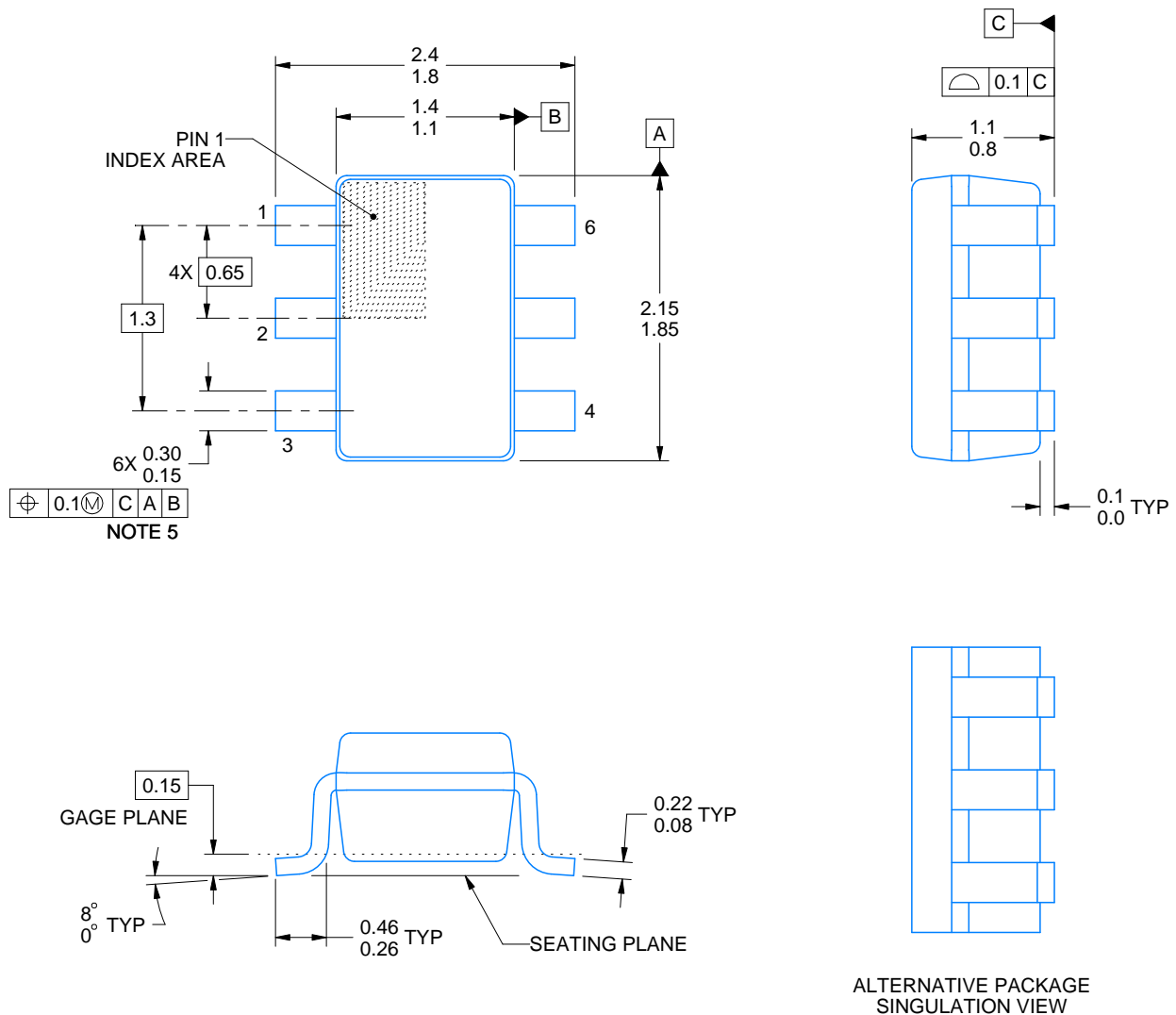
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

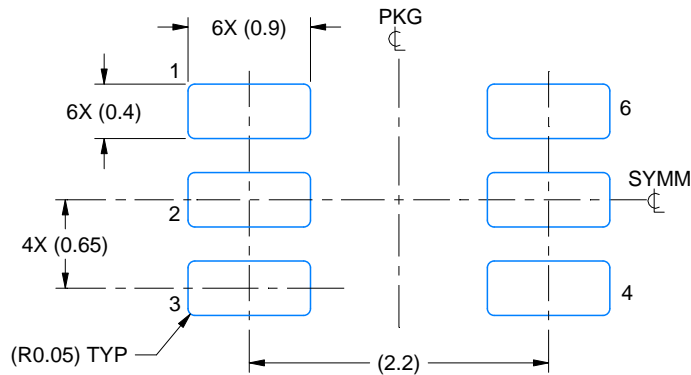
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0



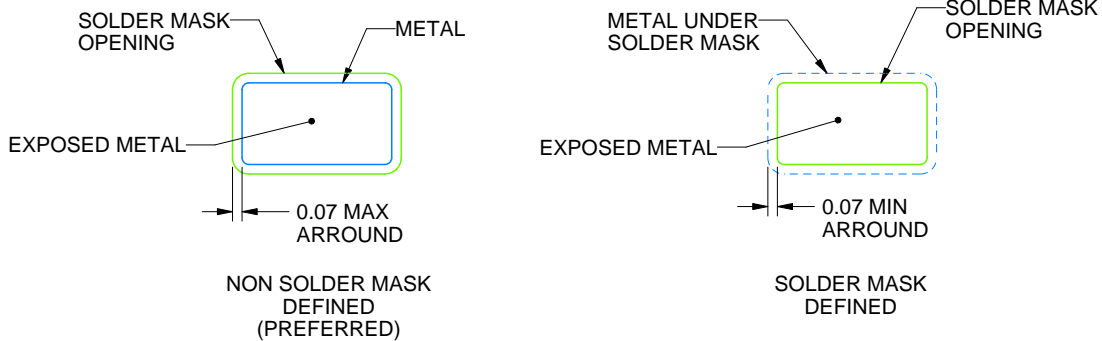
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

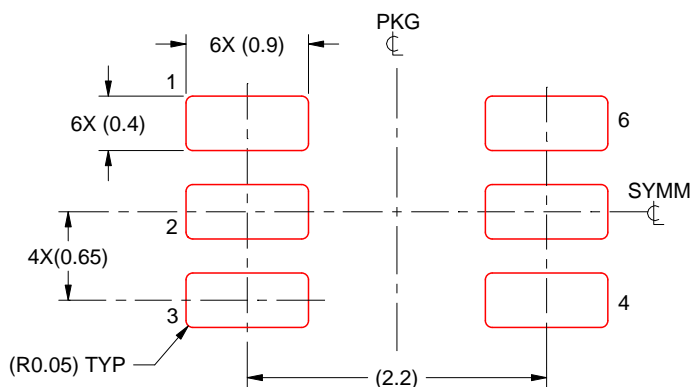


SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 THICK STENCIL
 SCALE:18X

4214835/B 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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