TPS65296-Complete LPDDR4/LPDDR4X Memory Power Solution

1 Features

- Synchronous buck converter (VDD2)
  - Input voltage range: 4.5 V to 18 V
  - Output voltage fixed at 1.1 V
  - D-CAP3™ mode control for fast transient response
  - Continual output current: 8 A
  - Advanced Eco-mode™ pulse skip
  - Integrated 22-mΩ / 8.6-mΩ $R_{DS(on)}$ internal power switch
  - 600-kHz switching frequency
  - Internal soft start: 1.6 ms
  - Cycle-by-cycle overcurrent protection
  - Latched output OV/UV protections
- Synchronous buck converter (VDD1)
  - Input voltage range: 3 V to 5.5 V
  - Output voltage fixed at 1.8 V
  - D-CAP3™ mode control for fast transient response
  - Continual output current: 1 A
  - Advanced Eco-mode™ pulse skip
  - Integrated 150-mΩ /120-mΩ $R_{DS(on)}$ internal power switch
  - 580-kHz switching frequency
  - Internal soft start: 1 ms
  - Cycle-by-cycle overcurrent protection
  - Latched output OV/UV protections
- 1.5-A LDO (VDDQ)
  - 1.5-A continual output current
  - Requires only 10 µF of ceramic output capacitor
  - Support high-Z in S3
  - ±30-mV VDDQ output accuracy (DC+AC)
- Low quiescent current: 150 µA
- Power good indicator
- Output discharge function
- Power up and power down sequencing control
- Non-latch for OT and UVLO protections
- 18-pin 3.0-mm × 3.0-mm HotRod™ VQFN package

2 Applications

- Notebook, PC computers, and servers
- Ultrabook, tablet computers
- Single-board computer, industrial PC
- Distributed power systems

3 Description

The TPS65296 device provides a complete power solution for LPDDR4/LPDDR4X memory system with the lowest total cost and minimum space. It meets the JEDEC standard for LPDDR4/LPDDR4X power-up and power-down sequence requirement. The TPS65296 integrates two synchronous buck converters (VDD1 and VDD2) and a 1.5-A LDO (VDDQ).

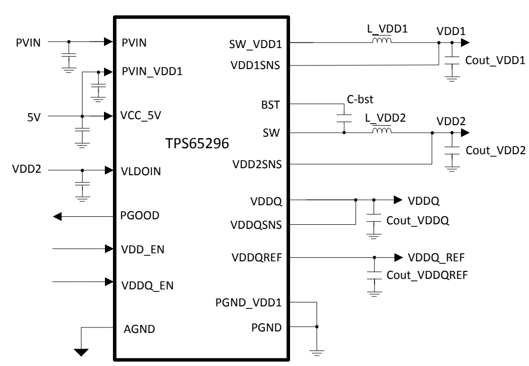
The TPS65296 employs D-CAP3™ mode with 600-kHz switching frequency for fast transient, good load/line regulation, and support for ceramic output capacitors without an external compensation circuit.

The TPS65296 provides rich functions as well as good efficiency with internal low Rdson power MOSFETs. It supports flexible power state control, placing VDDQ at high-Z in S3 and discharging VDD1, VDD2, and VDDQ in S4/S5 state. Full protection features include OVP, UVP, OCP, UVLO and thermal shutdown protection. The part is available in a thermally enhanced 18-pin HotRod™ VQFN package and is designed to operate under the –40°C to 125°C junction temperature range.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65296	VQFN (18)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2019) to Revision A (October 2020) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document........1
- Updated Package Information - package outline for pin 16 and pin 18........29
- Updated Package Information - example board layout for pin 16 and pin 18........29
- Updated Package Information - example stencil design for pin 16 and pin 18........29

5 Pin Configuration and Functions

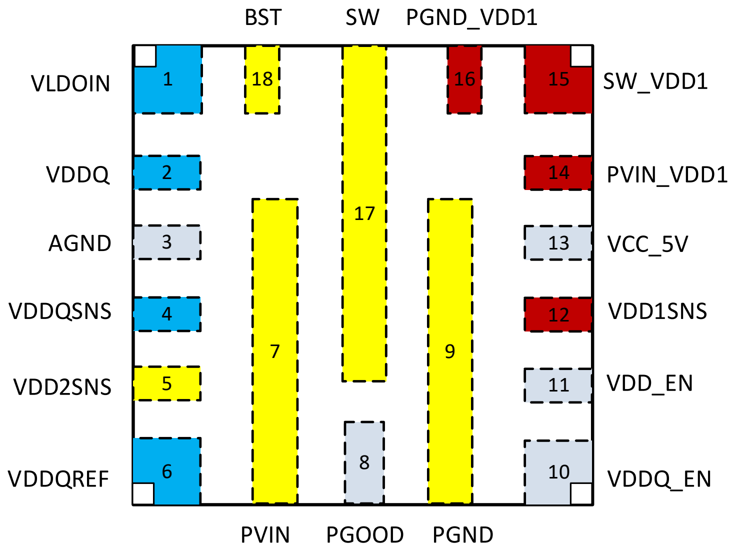


Figure 5-1. 18-Pin VQFN RJE Package (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VLDOIN	1	P	Power supply input for VDDQ LDO. Connect VDD2 in typical application.
VDDQ	2	O	VDDQ 1.5-A LDO output. It is recommended to connect to 10-µF or larger capacitance for stability.
AGND	3	G	Signal ground
VDDQSNS	4	I	VDDQ output voltage feedback
VDD2SNS	5	I	VDD2 output voltage feedback
VDDQREF	6	O	Internal reference for VDDQ. Recommend to connect to 0.22-µF or larger capacitance for stability.
PVIN	7	P	Input power supply for VDD2 buck
PGOOD	8	O	Power good signal open-drain output. PGOOD goes high when VDD1 and VDD2 output voltage are within the target range.
PGND	9	G	Power ground for VDD2 buck
VDDQ_EN	10	I	VDDQ_EN signal input for VDDQ LDO enable control. For detail control setup, refer to Table 7-1.
VDD_EN	11	I	VDD_EN signal input for VDD1 buck and VDD2 buck enable control. For detail control setup, refer to Table 7-1.
VDD1SNS	12	I	VDD1 output voltage feedback
VCC_5V	13	P	Power supply for VDD1 and VDD2 buck converter control logic circuit
PVIN_VDD1	14	P	Input power supply for VDD1 buck
SW_VDD1	15	O	VDD1 switching node connection to the inductor and bootstrap capacitor
PGND_VDD1	16	G	Power ground for VDD1 buck
SW	17	O	VDD2 switching node connection to the inductor and bootstrap capacitor
BST	18	I	High-side MOSFET gate driver bootstrap voltage input for VDD2 buck. Connect a capacitor between the BST pin and the SW pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
	Input voltage	PVIN	–0.3	20	V
		VBST	–0.3	25	V
		VBST-SW	–0.3	6	V
		VDD_EN, VDDQ_EN, VCC_5V, PVIN_VDD1, VLDOIN, VDD1SNS, VDD2SNS, VDDQSNS	–0.3	6	V
		PGND, AGND, PGND_VDD1	–0.3	0.3	V
	Output voltage	SW	–0.3	20	V
		SW (10-ns transient)	–3	22	V
		SW_VDD1	–0.3	7	V
		SW_VDD1 (10-ns transient)	–3	8	V
		PGOOD, VDDQ, VDDQREF	–0.3	6	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- V C101[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	PVIN	4.5	18	V
		VBST	–0.3	23	V
		VBST-SW	–0.3	5.5	V
		VDD_EN, VDDQ_EN, VCC_5V, PVIN_VDD1, VLDOIN, VDD1SNS, VDD2SNS, VDDQSNS	–0.3	5.5	V
		PGND, AGND, PGND_VDD1	–0.3	0.3	V
	Output voltage	SW	–0.3	18	V
		SW (10-ns transient)	–3	20	V
		SW_VDD1	–0.3	6	V
		SW_VDD1 (10-ns transient)	–2	7	V
		PGOOD, VDDQ, VDDQREF	–0.3	5.5	V
$I_{VDD2OUT}$	VDD2 Output current			8	A
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS65296 RJE (VQFN) 18 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	58.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	17.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	17.7	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

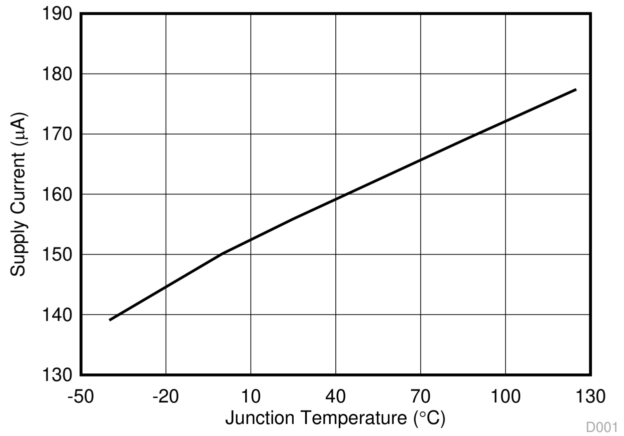
T_J=-40°C to 125°C, V_{PVIN}=12V, V_{PVIN_VDD1}=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
I_{VCC_5V}	VCC_5V supply current	V_{VDD_EN} = V_{VDDQ_EN} = 0 V		5		µA
		V_{VDD_EN} = 5 V, V_{VDDQ_EN} = 0 V, no load		110		µA
		V_{VDD_EN} = V_{VDDQ_EN} = 5 V, no load		150		µA
VIN	PVIN input voltage range		4.5		18	V
UVLO						
UVLO	VCC_5V under-voltage lockout	Wake up VCC_5V voltage		4.1	4.5	V
		Shut down VCC_5V voltage	3.3	3.6		V
		Hysteresis VCC_5V voltage		500		mV
VDD2						
$V_{VDD2SNS}$	VDD2 sense voltage		1.1	1.115	1.13	V
$I_{VDD2SNS}$	VDD2SNS input current	$V_{VDD2SNS}$ =1.1 V		40		µA
$I_{VDD2DIS}$	VDD2 discharge current	V_{VDD_EN} = V_{VDDQ_EN} = 0 V, $V_{VDD2SNS}$ = 0.5 V		12		mA
t_{VDD2SS}	VDD2 soft-start time			1.6	2.65	ms
$t_{VDD2DLY}$	VDD2 ramp up delay time		1.3	2	3.5	ms
R_{DSONH}	High-side switch resistance	T_J = 25°C, V_{VCC_5V} = 5V		22		mΩ
R_{DSONL}	Low-side switch resistance	T_J = 25°C, V_{VCC_5V} = 5V		8.6		mΩ
$I_{VDD2OCL}$	Low-side valley current limited	V_{OUT} = 1.1 V, L = 0.68 µH	8.2	9.8	11.5	A
f_{sw}	VDD2 switching freqency			600		kHz
$t_{OFF(MIN)}$	Minimum off time			198		ns
PGOOD (VDD2, VDD1)						
V_{THPG}	PGOOD threshold	VDD2SNS / VDD1SNS falling (Fault)		87		%
		VDD2SNS / VDD1SNS rising (Good)		93		%
		VDD2SNS / VDD1SNS rising (Fault)		115		%
		VDD2SNS / VDD1SNS falling (Good)		110		%
I_{PGMAX}	PG sink current	V_{PGOOD} =0.5V, V_{VDD_EN} =V_{VDDQ_EN} = 5 V, no load		46		mA
t_{PGDLY}	PG start-up delay	PG from low to high		1		ms
VDD1						
$V_{VDD1SNS}$	VDD1 sense voltage		1.75	1.8	1.85	V
$I_{VDD1SNS}$	VDD1SNS input current	$V_{VDD1SNS}$ =1.8 V		20		µA

T_J=-40ºC to 125ºC, V_{PVIN}=12V, V_{PVIN_VDD1}=5V (unless otherwise noted)

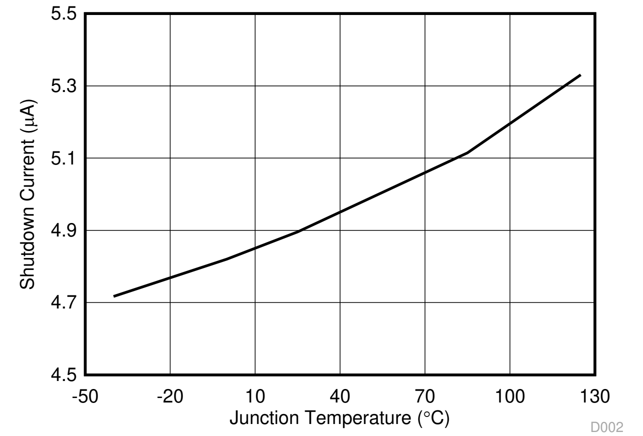
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1DIS}$	VDD1 discharge current	V_{VDD_EN} = V_{VDDQ_EN} = 0 V, $V_{VDD1SNS}$ = 0.5 V		12		mA
t_{VDD1SS}	VDD1 soft-start time			1.0	2	ms
R_{DSONH}	High-side switch resistance	T_J = 25°C, V_{PVIN_VDD1} = 5V, V_{VCC_5V} = 5V		150		mΩ
R_{DSONL}	Low-side switch resistance	T_J = 25°C, V_{PVIN_VDD1}=5V, V_{VCC_5V} = 5V		120		mΩ
$I_{VDD1OCL}$	Low-side valley current limited	$V_{VDD1SNS}$ = 1.8 V, L = 4.7 µH	1.05	1.6	2.1	A
f_{sw}	VDD1 switching frequency			580		kHz
$t_{OFF(MIN)}$	Minimum off time			195		ns
t_{OOA}	OOA mode operation period	$V_{VDD1SNS}$ =1.8 V		31		µs
OVP AND UVP (VDD2, VDD1)						
V_{OVP}	OVP threshold voltage	OVP detect voltage	120	125	130	%
V_{UVP1}	UVP threshold voltage	UVP detect voltage	57.5	62.5	67.5	%
t_{OVPDLY}	OVP delay			20		µs
t_{UVPDLY}	UVP delay			250		µs
VDDQ OUTPUT						
V_{VDDQ}	Output voltage	T_J = 25°C, I_{VDDQ} ≤1.5A	0.57	0.6	0.63	V
$I_{VDDQOCLSRC}$	Source current limit	$V_{VDD2SNS}$ = 1.1 V, V_{VDDQ}= $V_{VDDQSNS}$= 0.5 V	1.7	2.2		A
I_{VDDQLK}	Leakage current	T_J = 25°C, V_{VDD_EN} = 5 V, V_{VDDQ_EN} = 5 V			5	µA
$I_{VDDQSNSBIAS}$	VDDQSNS input bias current	V_{VDD_EN} = 5 V, V_{VDDQ_EN} = 5 V	–0.5	0	0.5	
$I_{VDDQSNSLK}$	VDDQSNS leakage current	V_{VDD_EN} = 5 V, V_{VDDQ_EN} = 0 V	–1	0	1	
$I_{VDDQDLY}$	VDDQ output delay relative to VDDQ_EN				35	us
$I_{VDDQDIS}$	VDDQ discharge current	T_J = 25°C, V_{VDD_EN} = V_{VDDQ_EN} = 0 V, $V_{VDD2SNS}$ = 1.1 V, V_{VDDQ} =0.5V		5.7		mA
VDD_EN, VDDQ_EN LOGIC THRESHOLD						
V_{IH}	VDD_EN/VDDQ_EN high-level voltage		1.35			V
V_{IL}	VDD_EN/VDDQ_EN low-level voltage				0.5	V
R_{TOGND}	VDD_EN/VDDQ_EN resistance to GND			500		kΩ
THERMAL PROTECTION						
T_{OTP}	OTP trip threshold			150		°C
T_{OTPHSY}	OTP hysteresis			20		°C

6.6 Typical Characteristics



V_{VDD_EN} = 5 V V_{VDDQ_EN} = 5 V

Figure 6-1. VCC_5V Supply Current vs Junction Temperature



V_{VDD_EN} = 0 V V_{VDDQ_EN} = 0 V

Figure 6-2. VCC_5V Shutdown Current vs Temperature

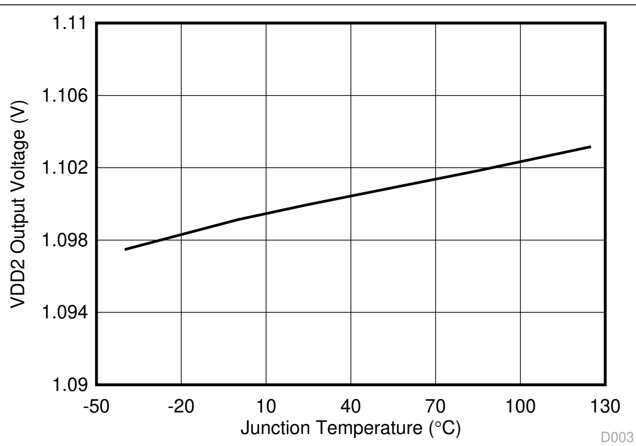


Figure 6-3. VDD2 Output Voltage vs Junction Temperature

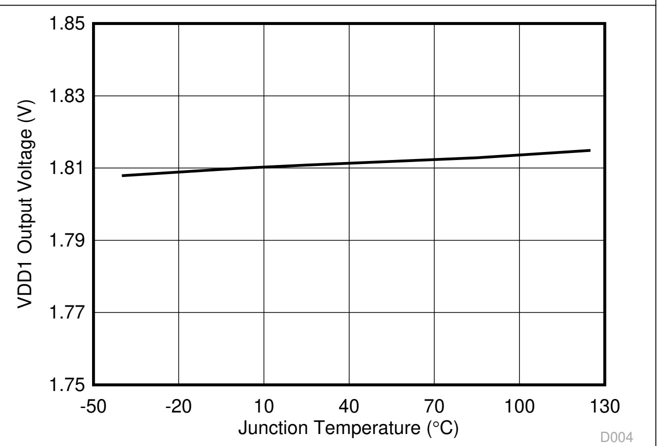


Figure 6-4. VDD1 Output Voltage vs Junction Temperature

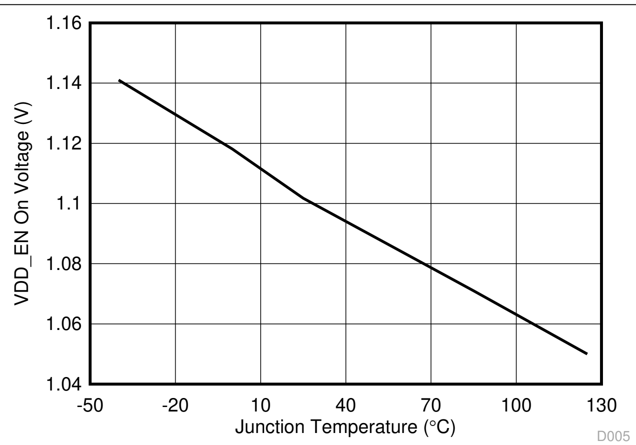


Figure 6-5. Enable On Voltage (VDD_EN) vs Junction Temperature

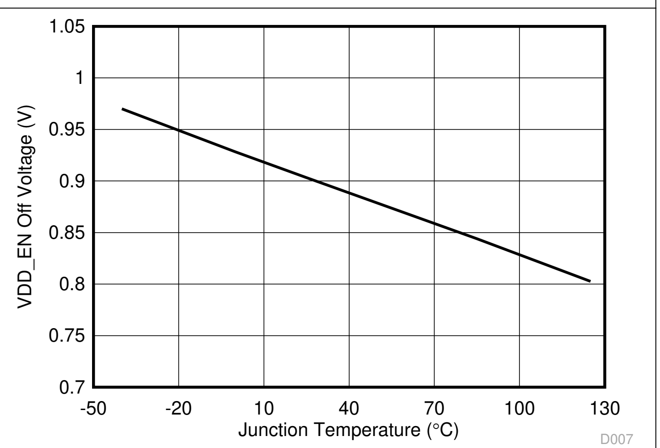


Figure 6-6. Enable Off Voltage (VDD_EN) vs Junction Temperature

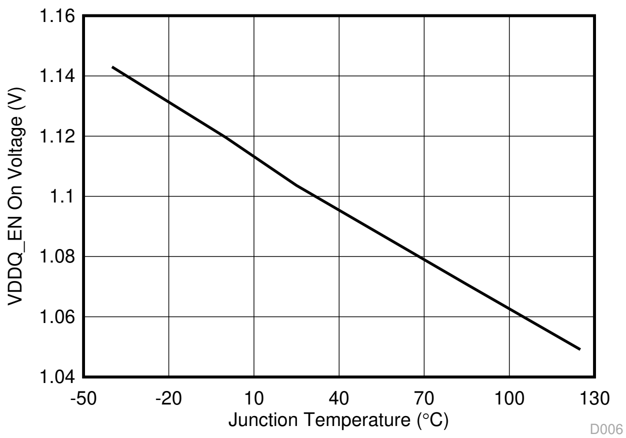


Figure 6-7. Enable On Voltage (VDDQ_EN) vs Junction Temperature

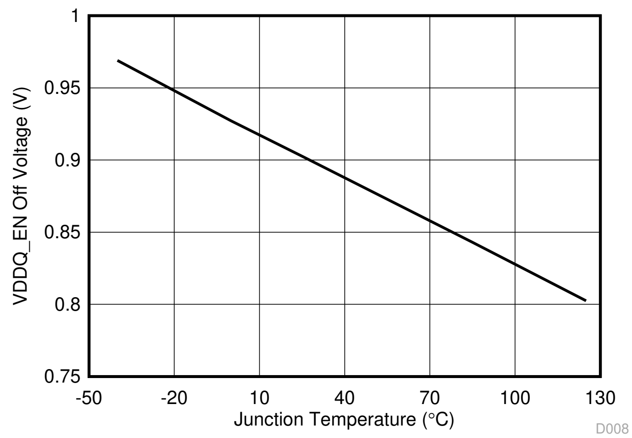


Figure 6-8. Enable Off Voltage (VDDQ_EN) vs Junction Temperature

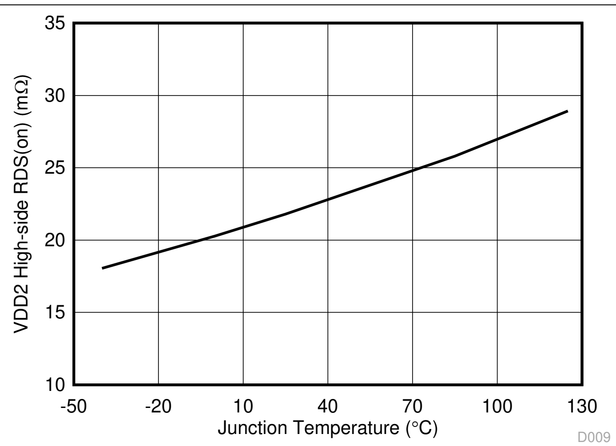


Figure 6-9. VDD2 High-Side $R_{DS(on)}$ vs Junction Temperature

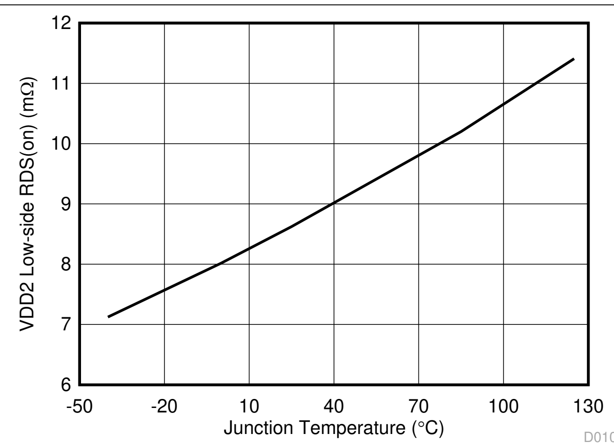


Figure 6-10. VDD2 Low-Side $R_{DS(on)}$ vs Junction Temperature

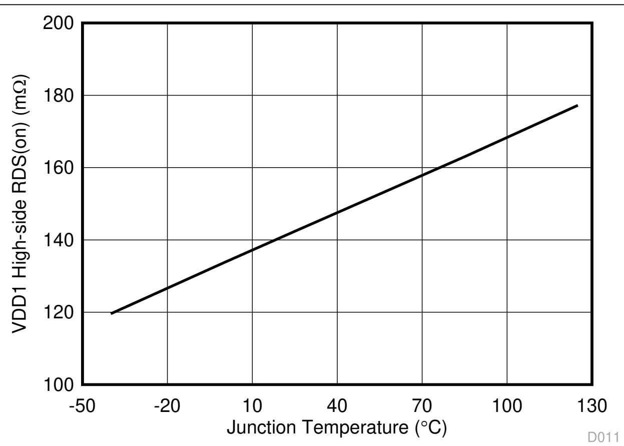


Figure 6-11. VDD1 High-Side $R_{DS(on)}$ vs Junction Temperature

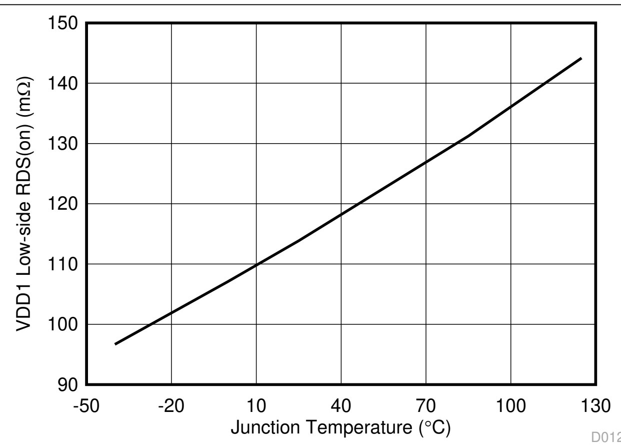


Figure 6-12. VDD1 Low-Side $R_{DS(on)}$ vs Junction Temperature

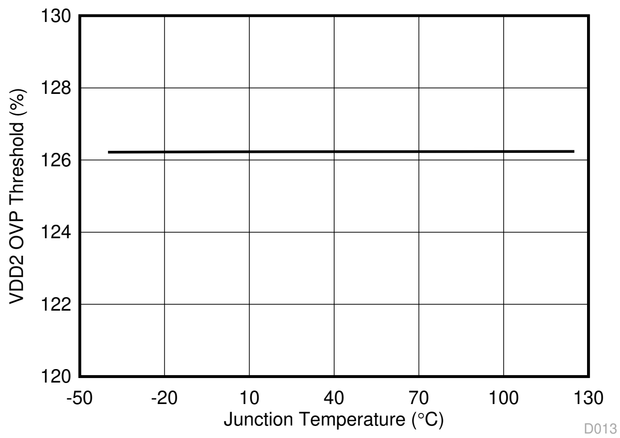


Figure 6-13. VDD2 OVP Threshold vs Junction Temperature

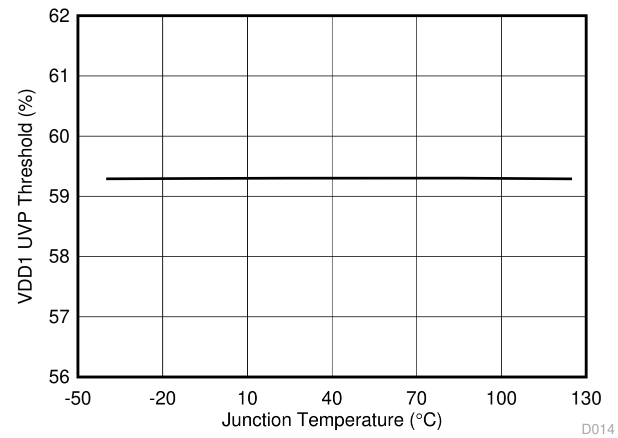


Figure 6-14. VDD2 UVP Threshold vs Junction Temperature

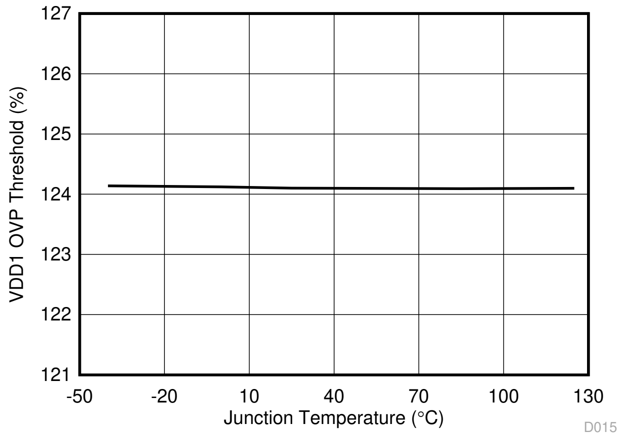


Figure 6-15. VDD1 OVP Threshold vs Junction Temperature

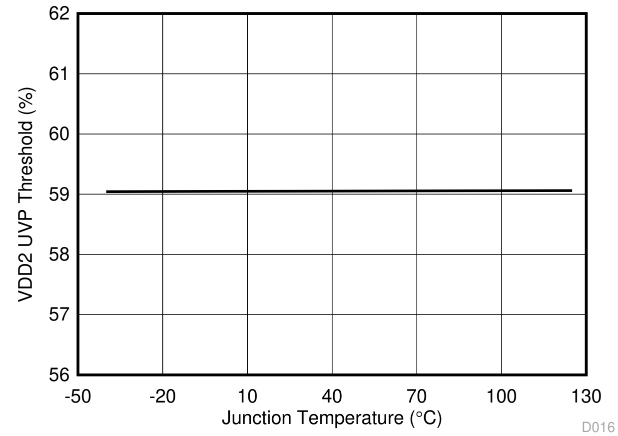


Figure 6-16. VDD1 UVP Threshold vs Junction Temperature

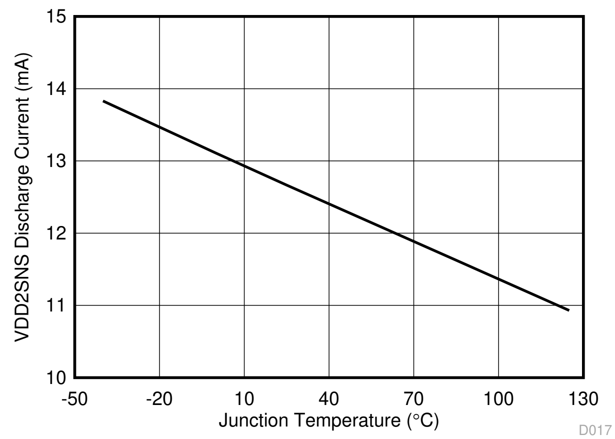


Figure 6-17. VDD2SNS Discharge Current vs Junction Temperature

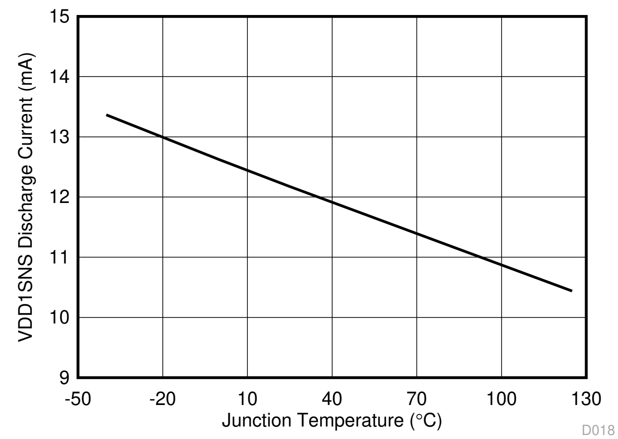


Figure 6-18. VDD1SNS Discharge Current vs Junction Temperature

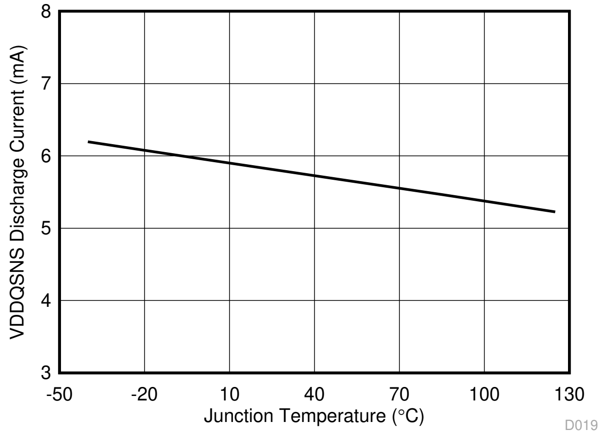


Figure 6-19. VDDQSNS Discharge Current vs Junction Temperature

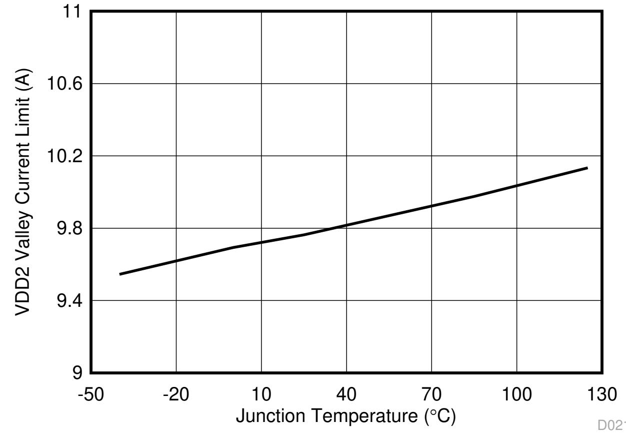


Figure 6-20. VDD2 Valley Current Limit vs Junction Temperature

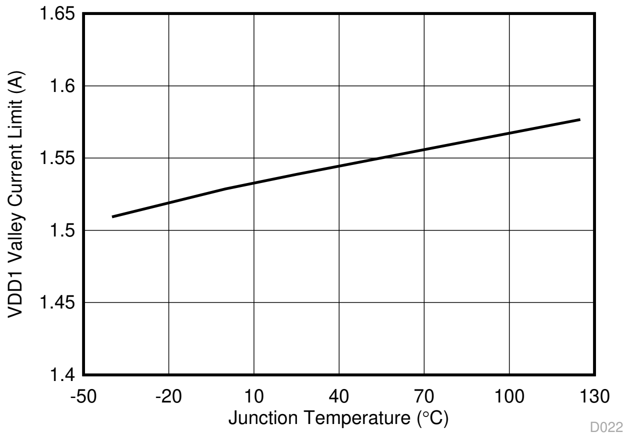


Figure 6-21. VDD1 Valley Current Limit vs Junction Temperature

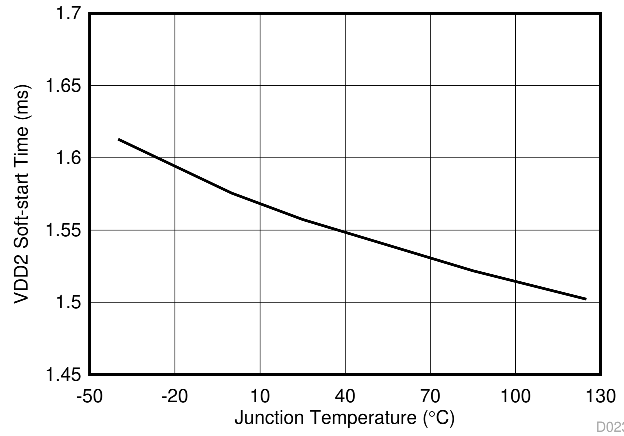


Figure 6-22. VDD2 Soft-Start Time vs Junction Temperature

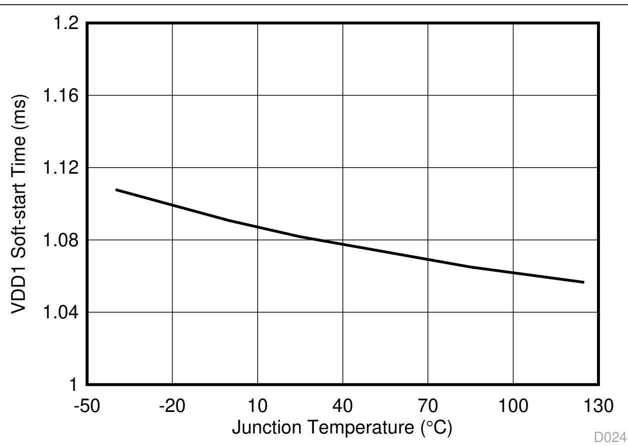
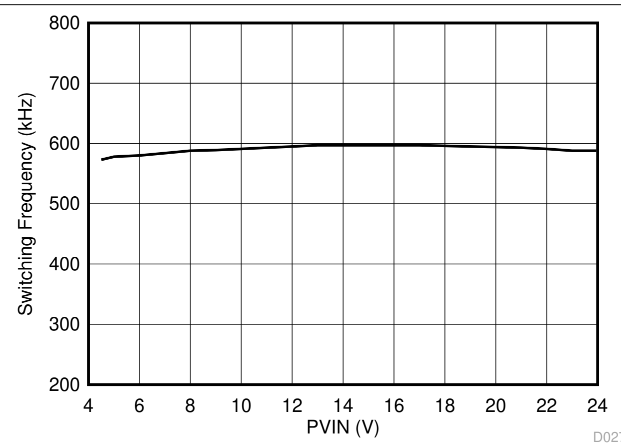
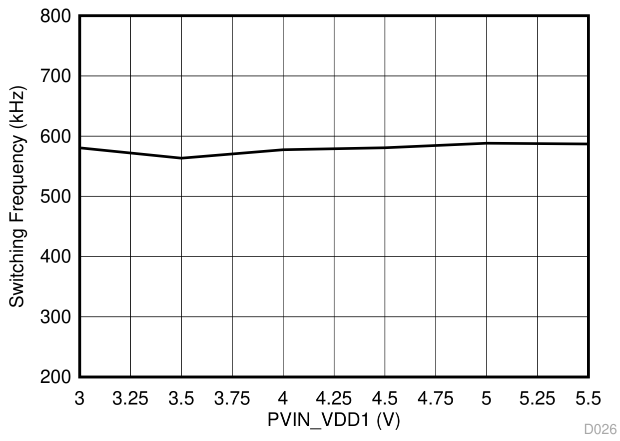


Figure 6-23. VDD1 Soft-Start Time vs Junction Temperature



I_{OUT} = 8 A

Figure 6-24. VDD2 Switching Frequency vs Input Voltage



I_{OUT} = 1 A

Figure 6-25. VDD1 Switching Frequency vs Input Voltage

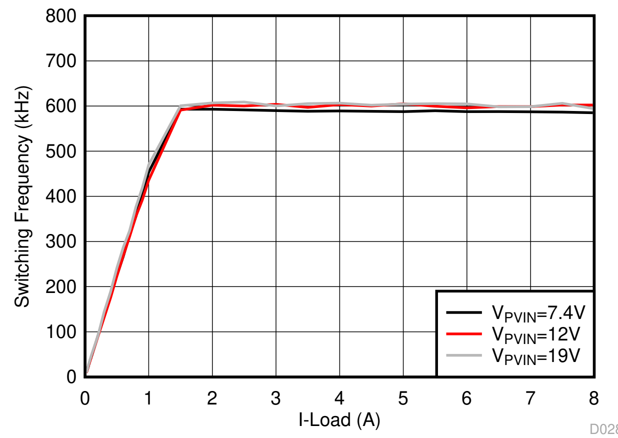


Figure 6-26. VDD2 Switching Frequency vs Load Current

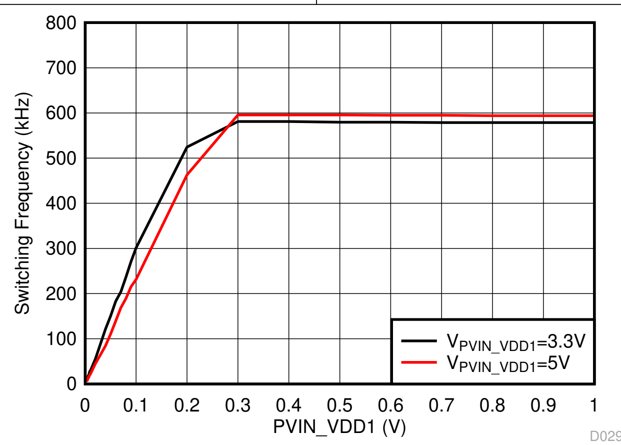


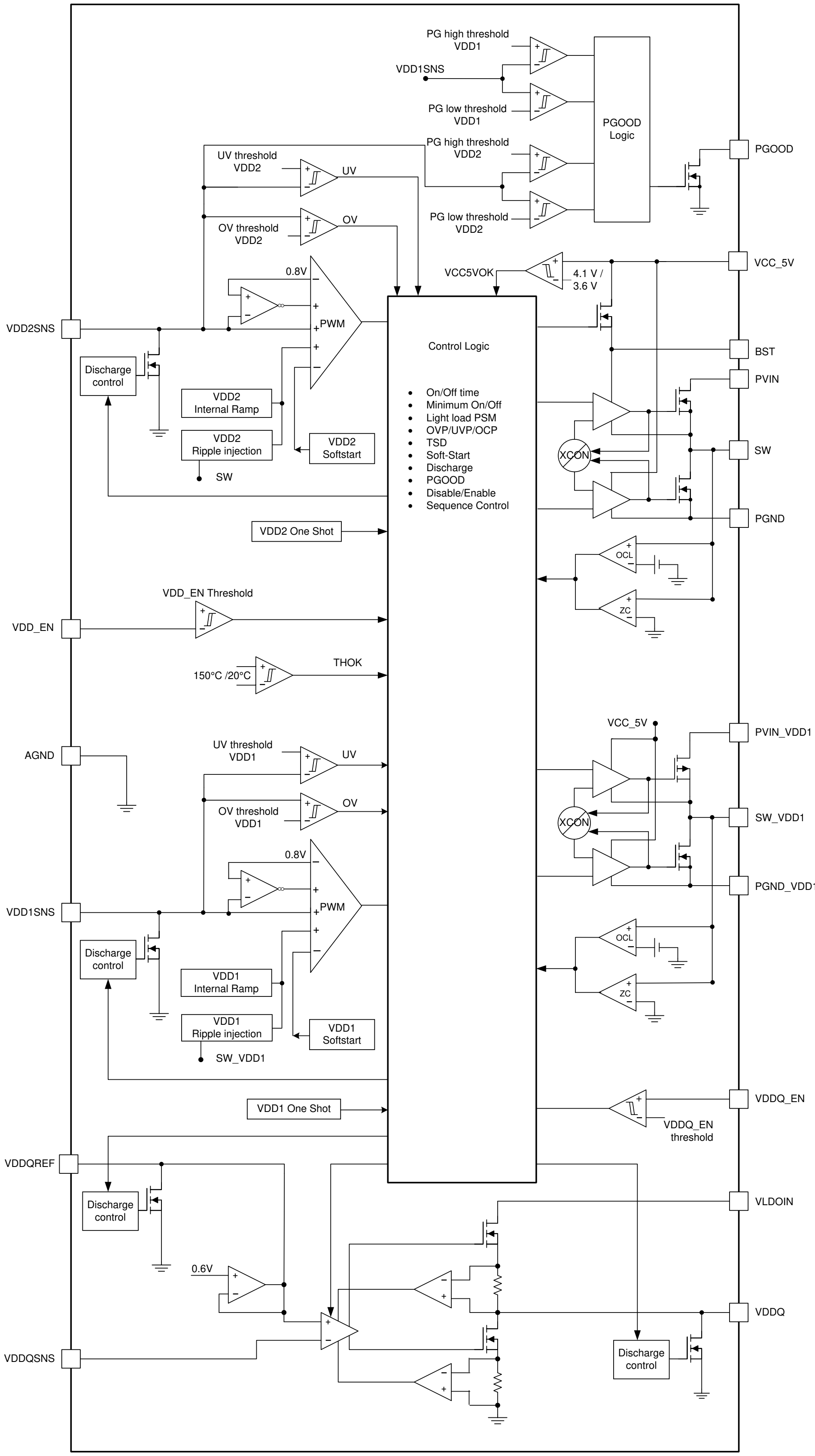
Figure 6-27. VDD1 Switching Frequency vs Load Current

7 Detailed Description

7.1 Overview

The TPS65296 integrates two synchronous step-down buck converters and a LDO to support complete LPDDR4/LPDDR4X power solution. The VDD2 buck converter has fixed 1.1-V output and supports continuous 8-A output current, and it can operate from 4.5-V to 18-V PVIN input voltage. The VDD1 buck converter has the fixed 1.8-V output and supports continuous 1-A output current, and can operate from 3-V to 5.5-V PVIN_VDD1 input voltage. The VDDQ LDO has continuous 1.5-A output current capability.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control

The main control loop of the two bucks is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3 mode control. The DCAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS65296 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, VIN, and is inversely proportional to the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

Both VDD1 buck and VDD2 buck include an error amplifier that makes the output voltage very accurate. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS65296 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the internal output set-point resistor divider network and the internal gain of the TPS65296. The low-frequency L-C double pole has a 180 degree in-phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high-frequency zero is related to the switching frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the high-frequency zero, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

7.3.2 Advanced Eco-mode Control

The VDD1 buck and VDD2 buck are designed with advanced Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode, so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$) can be calculated from Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application). It is also important to size the inductor properly so that the valley current does not hit the negative low-side current limit.

7.3.3 Soft Start and Prebiased Soft Start

The VDD2 buck has an internal 1.6-ms soft start and VDD1 buck has an internal 1-ms soft start. Provide the voltage supply to PVIN, PVIN_VDD1, and VCC_5V before asserting VDD_EN to be high. When the VDD_EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Power Good

The Power Good (PGOOD) pin is an open-drain output. Once the VDD1SNS and VDD2SNS pins voltage are between 90% and 110% of the target output voltage, the PGOOD is deasserted and floats after a 1-ms de-glitch time. A pullup resistor of 100 kΩ is recommended to pull the voltage up to VCC_5V. The PGOOD pin is pulled low when:

- the VDD1SNS pin voltage or VDD2SNS pin voltage is lower than 85% or greater than 115% of the target output voltage,
- in an OVP, UVP, or thermal shutdown event,
- or during the soft-start period.

7.3.5 Overcurrent Protection and Undervoltage Protection

Both VDD1 and VDD2 bucks have the overcurrent protection and undervoltage protection, and the implementation is same. The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the output will be discharged and latched after a wait time of 256 µs. When the overcurrent condition is removed, the output voltage is latched till the VDD_EN is toggled or repower the VCC_5V power input.

7.3.6 Overvoltage Protection

Both VDD1 and VDD2 bucks have the overvoltage protection feature and have the same implementation. When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high, and then the output will be discharged and latched after a wait time of 20 µs. When the over current condition is removed, the output voltage is latched till the VDD_EN is toggled or repower the VCC_5V power input.

7.3.7 UVLO Protection

Undervoltage Lockout protection (UVLO) monitors the VCC_5V power input. When the voltage is lower than UVLO threshold voltage, the device is shut off and outputs are discharged. This is a non-latch protection.

7.3.8 Output Voltage Discharge

The VDD1 buck, VDD2 buck, and VDDQ LDO block all have the discharge function by using internal MOSFETs, which are connected to the corresponding output terminals VDD1SNS, VDD2SNS, and VDDQ. The discharge is slow due to the lower current capability of these MOSFETs.

7.3.9 Thermal Shutdown

The TPS65296 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 150°C), the device is shut off and the output will be discharged. This is a non-latch protection. The device restarts switching when the temperature goes below the thermal shutdown recover threshold.

7.4 Device Functional Modes

7.4.1 Light Load Operation for VDD1 Buck and VDD2 Buck

When the load is light on the VDD1 or VDD2 output, the buck enters pulse skip mode after the inductor current crosses zero. This is the Eco-mode which improves the efficiency at light load with a lower switching frequency. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VDD1SNS or VDD2SNS voltage falls below the Eco-mode threshold voltage. As the output current decreases, the period time between switching pulses increases.

7.4.2 Output State Control

The TPS65296 has two enable input pins (VDD_EN and VDDQ_EN) to provide simple control scheme of output state. All of VDD1, VDD2, and VDDQ are turned on at S0 state (VDD_EN=VDDQ_EN=high). In S3 state (VDDQ_EN=low, VDD_EN=high), VDD1 and VDD2 voltages are kept on while VDDQ is turned off and left at high impedance state (high-Z). The VDDQ output floats and does not source current in this state. In S4/S5 states (VDD_EN=VDDQ_EN =low), all of the three outputs are turned off and discharged to GND. Each state code represents as follows: S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF (see Table 7-1).

Table 7-1. VDDQ_EN and VDD_EN Control for Output State

STATE	VDDQ_EN	VDD_EN	VDD1	VDD2	VDDQ
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)

7.4.3 Output Sequence Control

There are specific sequencing requirements for the LPDDR4/LPDDR4X VDD1 and VDD2 rails. The TPS65296 follows the power rail sequence requirements as shown in Figure 7-1 and Figure 7-2. VDD1 is greater than VDD2 at all times during ramp up, operating, and ramp down. The VDDQ output ramp and stable within 35 µs after VDDQ_EN asserted.

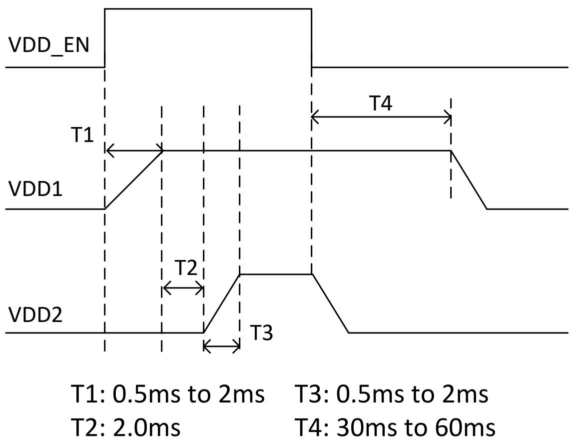


Figure 7-1. Power Sequence, VDD1 and VDD2 versus VDD_EN

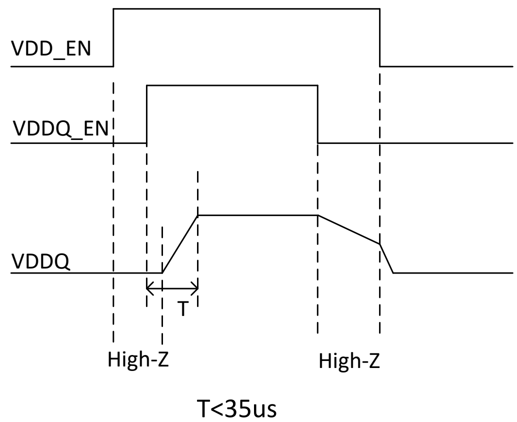


Figure 7-2. Power Sequence, VDDQ versus VDDQ_EN

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65296 device provides a complete power solution for LPDDR4/LPDDR4X memory system. Table 8-1 shows the power requirements for LPDDR4 and LPDDR4X.

Table 8-1. LPDDR4/LPDDR4X Application

	VDD1	VDD2	VDDQ
LPDDR4	YES	YES	NO(Leave this pin floating)
LPDDR4X	YES	YES	YES

The schematic of Figure 8-1 shows a typical application for LPDDR4X. For VDD2 buck, the PVIN supports 4.5-V to 18-V input range with 1.1-V VDD2 output, the continuous current capability is 8 A. Usually the PVIN_VDD1 and VCC_5V can share one 5-V power input and supports 1.8-V VDD1 output with 1-A continuous current capability, and the PVIN_VDD1 can be lowered down to a 3.3-V power supply. The VLDOIN power input usually is connected to VDD2 output, while also it can be connected to external 1.1-V power supply input. The schematic of Figure 8-2 shows a typical application for LPDDR4. The TPS65296 can be used for LPDDR4 when connecting VDDQ_EN pin to GND to disable the LDO and leave VDDQ/VDDQSNS pin floating. It doesn't need input cap for VLDOIN and output cap for VDDQ compare with the application in LPDDR4X. While it also need to connect VLDOIN to VDD2 or external 1.1-V power supply for internal power supply.

8.2 Typical Application

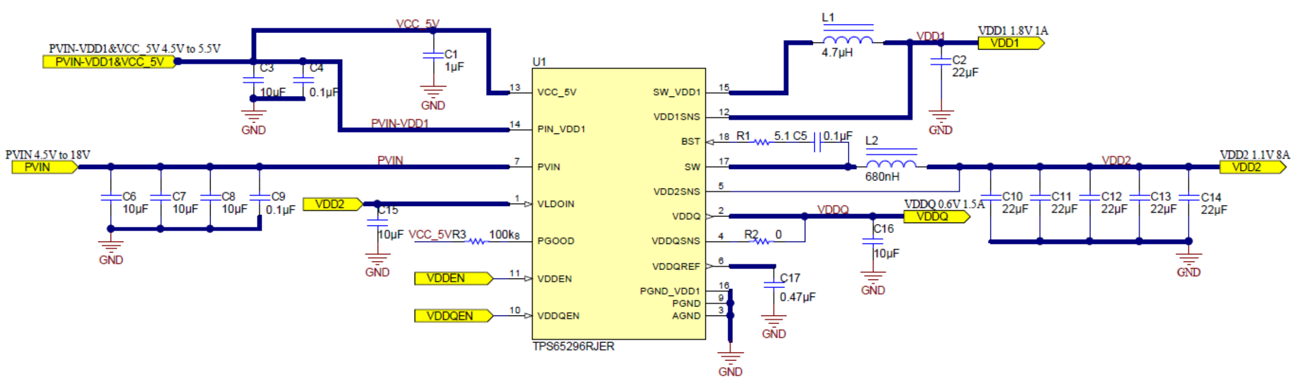


Figure 8-1. LPDDR4X Application Schematic

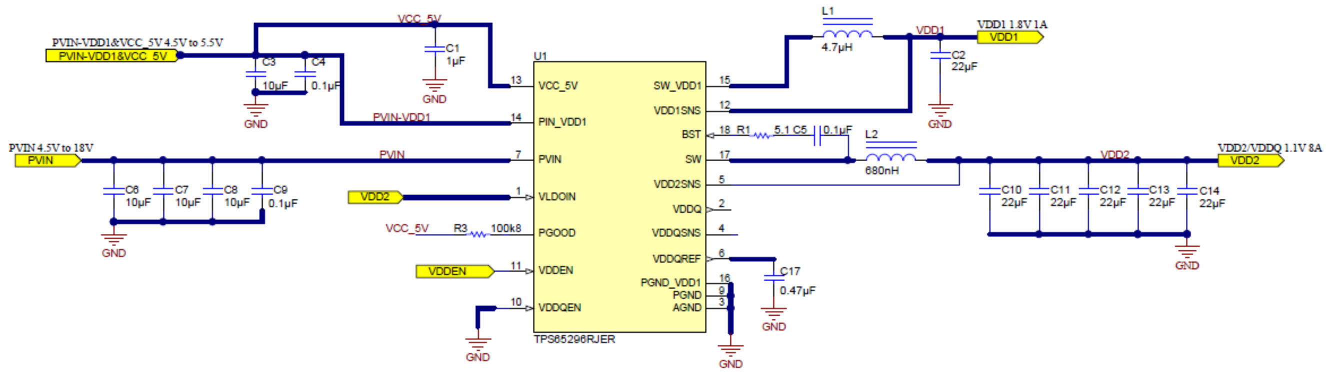


Figure 8-2. LPDDR4 Application Schematic

8.2.1 Design Requirements

Table 8-2 lists the design parameters for this example.

Table 8-2. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
VDD2 OUTPUT						
V_{OUT}	Output voltage			1.115		V
I_{OUT}	Output current			8		A
ΔV_{OUT}	Transient response	8-A load step		±55		mV
V_{IN}	Input voltage		4.5	12	18	V
$V_{OUT(ripple)}$	Output voltage ripple			30		$mV_{(P-P)}$
F_{SW}	Switching frequency			600		kHz
VDD1 OUTPUT						
V_{OUT}	Output voltage			1.8		V
I_{OUT}	Output current			1		A
ΔV_{OUT}	Transient response	1-A load step		±90		mV
V_{IN}	Input voltage		3	5	5.5	V
$V_{OUT(ripple)}$	Output voltage ripple			30		$mV_{(P-P)}$
F_{SW}	Switching frequency			580		kHz
OTHERS						
V_{VCC_5V}	Start VCC_5V input voltage	VCC_5V Input voltage rising		Internal UVLO		V
	Stop VCC_5V input voltage	VCC_5V Input voltage falling		Internal UVLO		V
	Light load operating mode			ECO		

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 8-3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 3 and Equation 4. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

During transient and short-circuit conditions, the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.2 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In DCAP3, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 8-3.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

Table 8-3. Recommended Component Values

V_{OUT} (V)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)
1.1	600	0.68	88	142
	600	0.56	88	142
	600	0.47	88	142
1.8	580	6.8	20	66
	580	4.7	20	66
	580	3.3	20	66

For VDDQ output, high quality X5R or X7R 10-µF capacitor is recommended and a 0.47 µF is recommended for VDDQREF output.

8.2.2.1.3 Input Capacitor Selection

The TPS65296 requires input decoupling capacitors on both power supply input PVIN and PVIN_VDD1, and the bulk capacitors are needed depending on the application. The minimum input capacitance required is given in Equation 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of 30 µF on the VDD2 buck input voltage pin PVIN, and 10 µF on the VDD1 buck input voltage pin PVIN_VDD1. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 6:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (6)$$

An additional 0.1-µF capacitor from PVIN to ground and from PVIN_VDD1 to ground is optional to provide additional high frequency filtering. One ceramic capacitor of 10 µF is recommended for the decoupling capacitor on VLDOIN pin for providing stable power on VDDQ LDO block. A 1-µF ceramic capacitor is needed for the decoupling capacitor on VCC_5V input.

8.2.2.1.4 Bootstrap Capacitor and Resistor Selection

A 0.1-µF ceramic capacitor serialized with a 5.1-Ω resistor is recommended between the BST and SW pin for proper operation. TI recommends using a ceramic capacitor.

8.2.3 Application Curves

Figure 8-3 through Figure 8-30 apply to the circuit of Figure 8-1. V_{IN} = 12 V. T_A = 25°C unless otherwise specified.

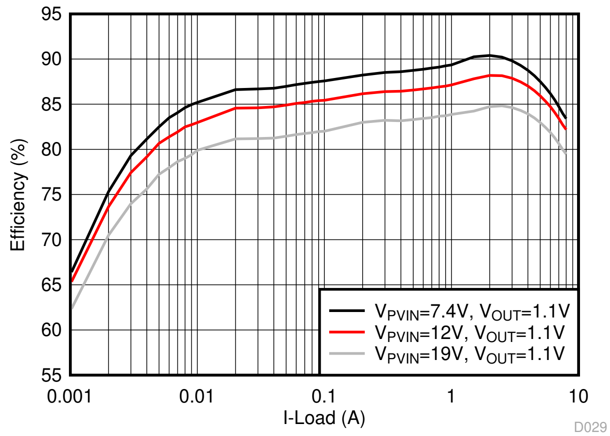


Figure 8-3. VDD2 Efficiency Curve, V_{OUT} = 1.1 V

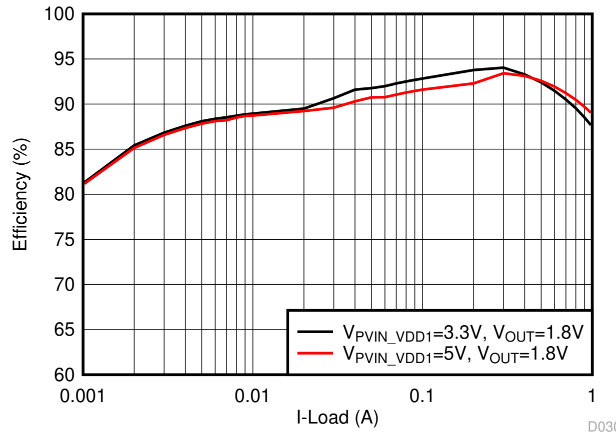


Figure 8-4. VDD1 Efficiency Curve, V_{OUT} = 1.8 V

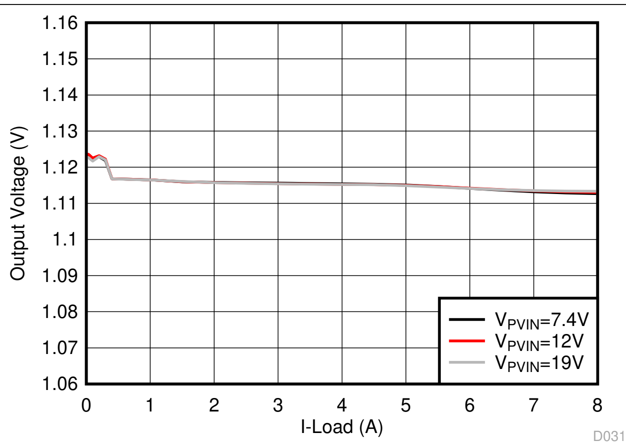


Figure 8-5. VDD2 Load Regulation, V_{OUT} = 1.1 V

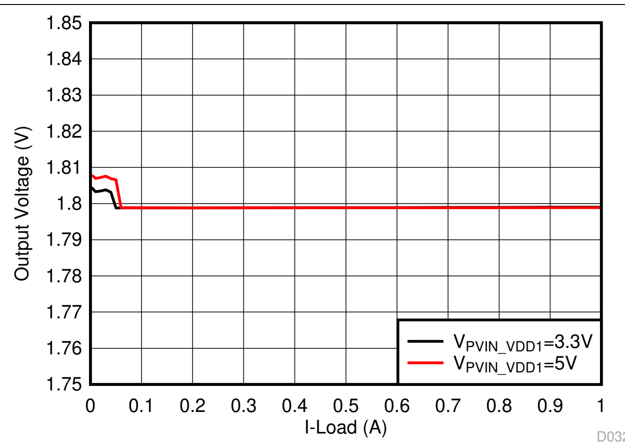


Figure 8-6. VDD1 Load Regulation, V_{OUT} = 1.8 V

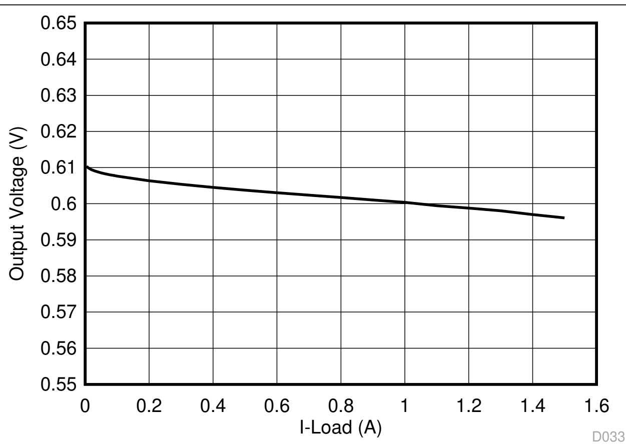


Figure 8-7. VDDQ Load Regulation, V_{OUT} = 0.6 V

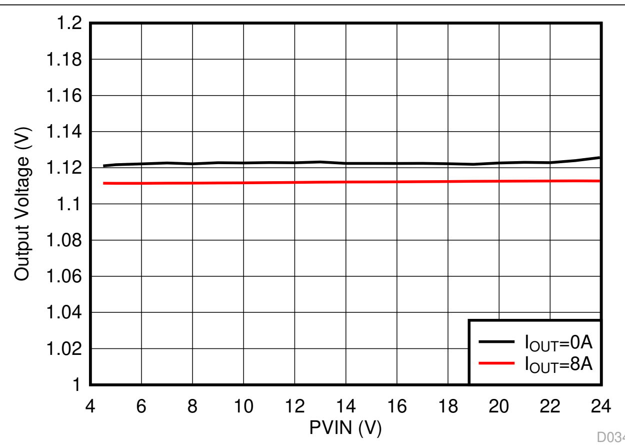


Figure 8-8. VDD2 Line Regulation,V_{OUT} = 1.1 V

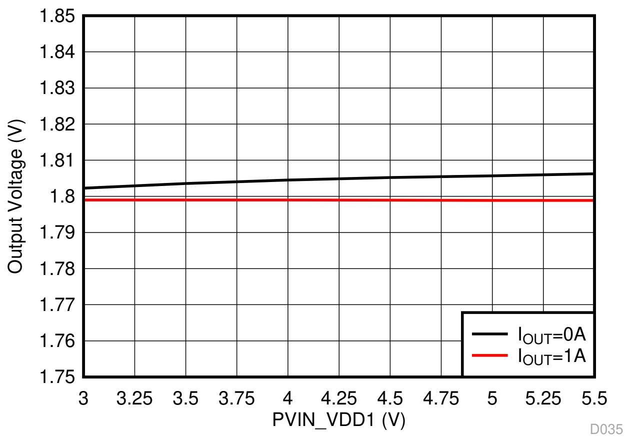


Figure 8-9. VDD1 Line Regulation, V_{OUT} = 1.8 V

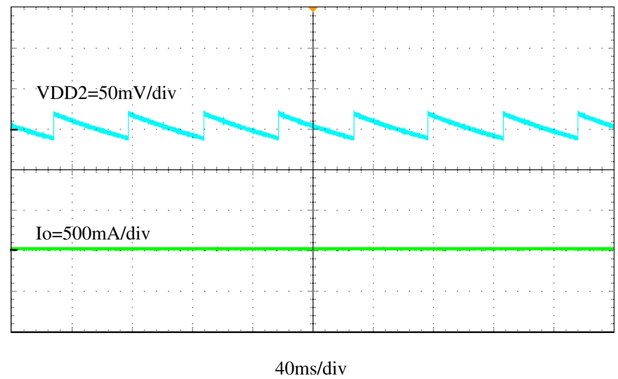


Figure 8-10. VDD2 Output Voltage Ripple, I_{OUT} = 0 A

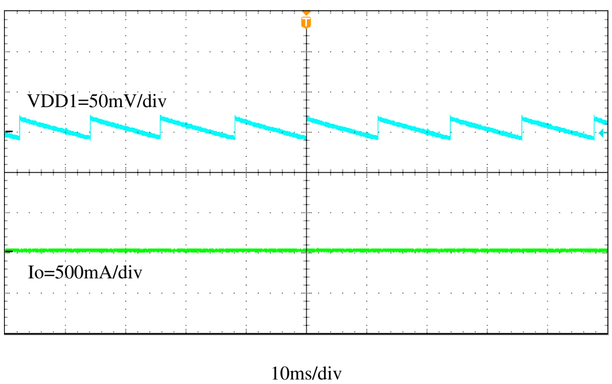


Figure 8-11. VDD1 Output Voltage Ripple, I_{OUT} = 0 A

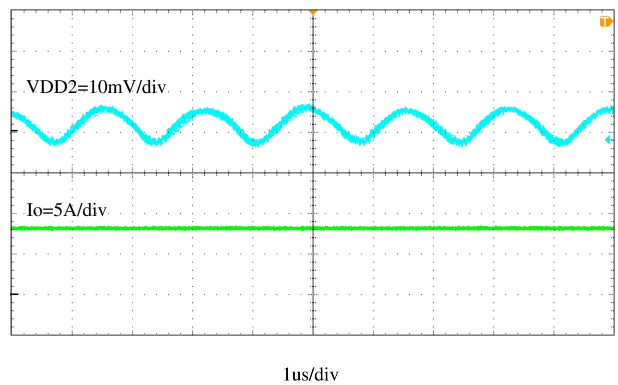


Figure 8-12. VDD2 Output Voltage Ripple, I_{OUT} = 8 A

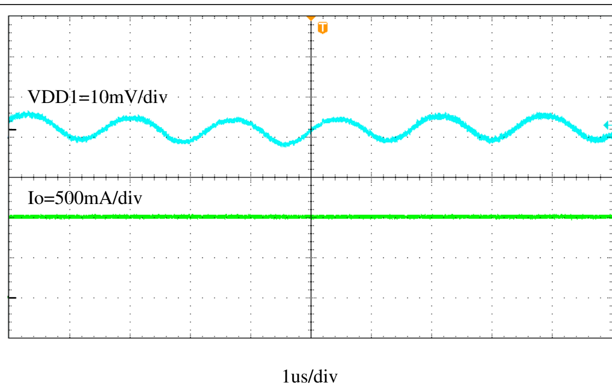


Figure 8-13. VDD1 Output Voltage Ripple, I_{OUT} = 1 A

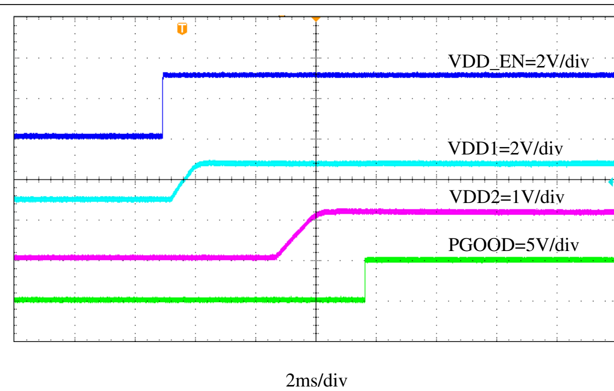


Figure 8-14. Start-Up Through VDD_EN, $I_{VDD1OUT}$ = 0 A, $I_{VDD2OUT}$ = 0 A

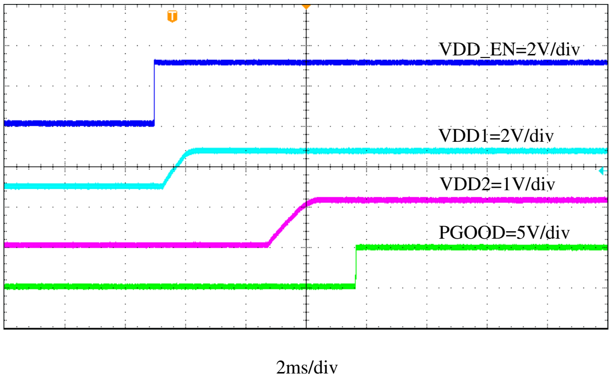


Figure 8-15. Start-Up Through VDD_EN, $I_{VDD1OUT}$ = 1 A, $I_{VDD2OUT}$ = 8 A

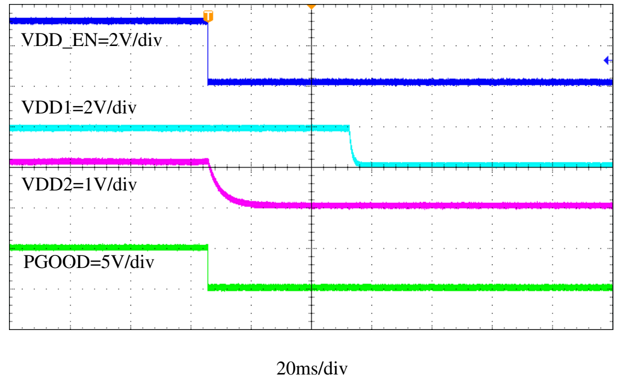


Figure 8-16. Shutdown Through VDD_EN, $I_{VDD1OUT}$ = 0 A, $I_{VDD2OUT}$ = 0 A

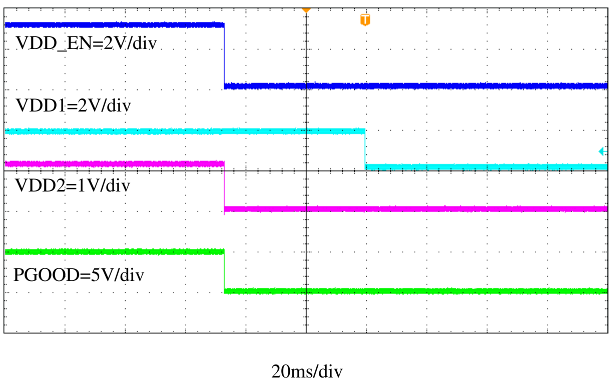
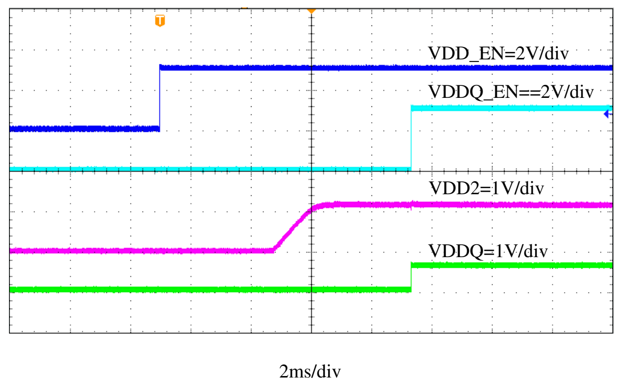
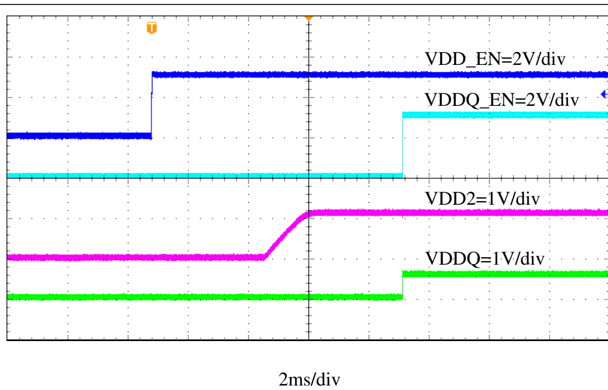


Figure 8-17. Shutdown Through VDD_EN, $I_{VDD1OUT}$ = 1 A, $I_{VDD2OUT}$ = 8 A



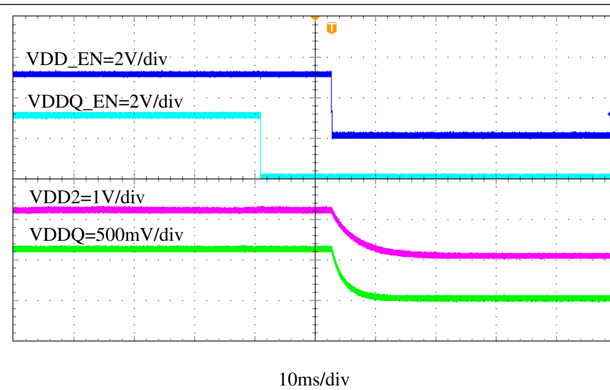
$I_{VDD2OUT}$ = 0 A I_{VDDQ} = 0 A

Figure 8-18. VDDQ Start-Up Through VDDQ_EN



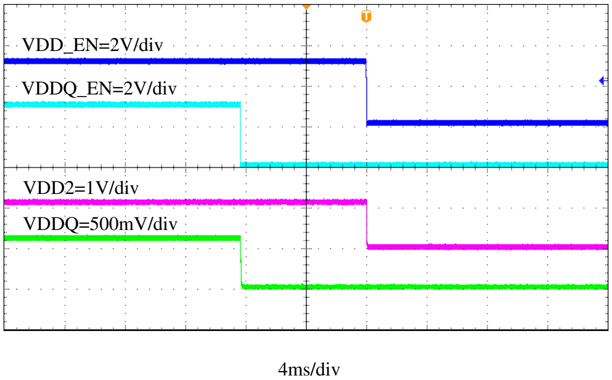
$I_{VDD2OUT}$ = 8 A I_{VDDQ} = 1.5 A

Figure 8-19. VDDQ Start-Up Through VDDQ_EN



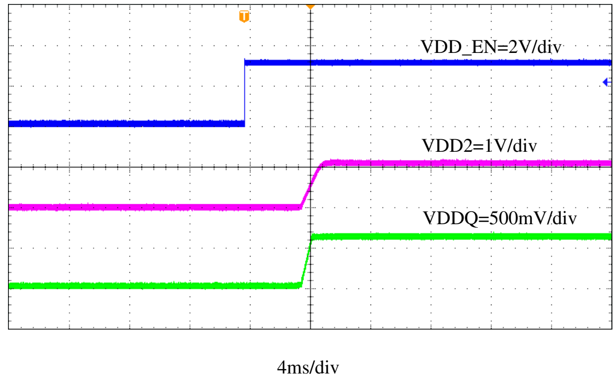
$I_{VDD2OUT}$ = 0 A I_{VDDQ} = 0 A

Figure 8-20. VDDQ Shutdown Through VDDQ_EN



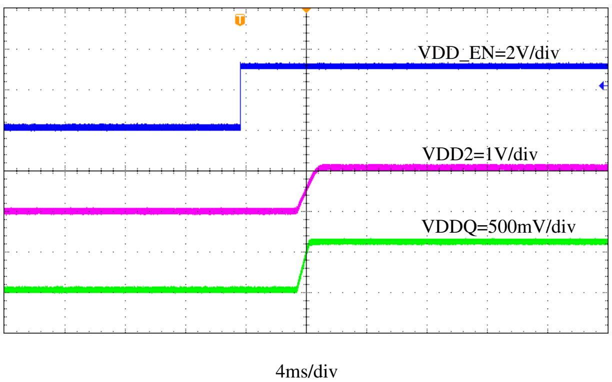
$I_{VDD2OUT}$ = 8 A I_{VDDQ} = 1.5 A

Figure 8-21. VDDQ Shutdown Through VDDQ_EN



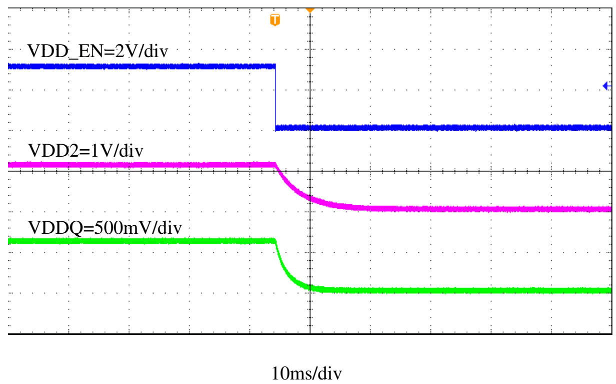
$I_{VDD2OUT}$ = 0 A I_{VDDQ} = 0 A

Figure 8-22. VDDQ Start-Up Through VDD_EN



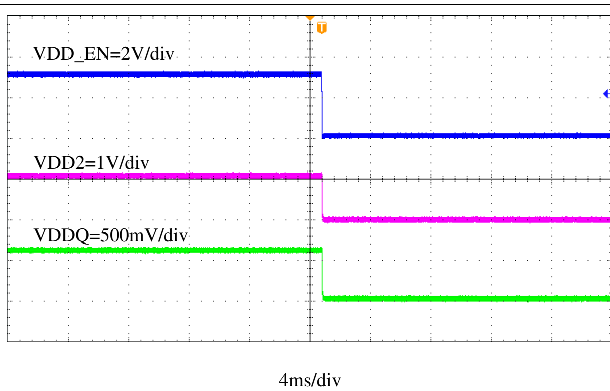
$I_{VDD2OUT}$ = 8 A I_{VDDQ} = 1.5 A

Figure 8-23. VDDQ Start-Up Through VDD_EN



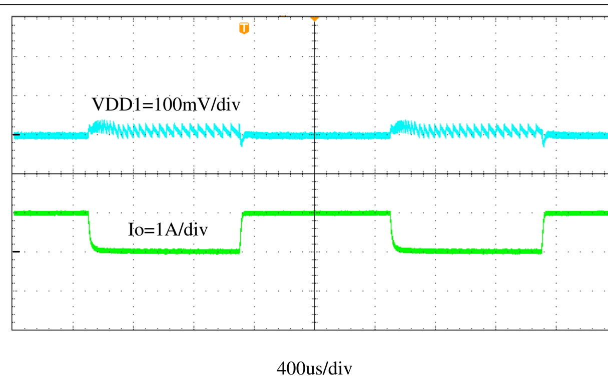
$I_{VDD2OUT}$ = 0 A I_{VDDQ} = 0 A

Figure 8-24. VDDQ Shutdown Through VDD_EN



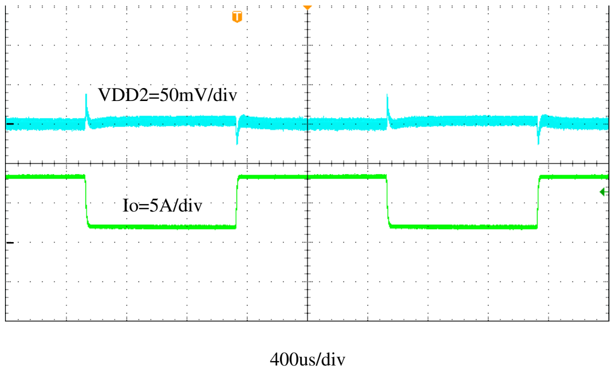
$I_{VDD2OUT}$ = 8 A I_{VDDQ} = 1.5 A

Figure 8-25. VDDQ Shutdown Through VDD_EN



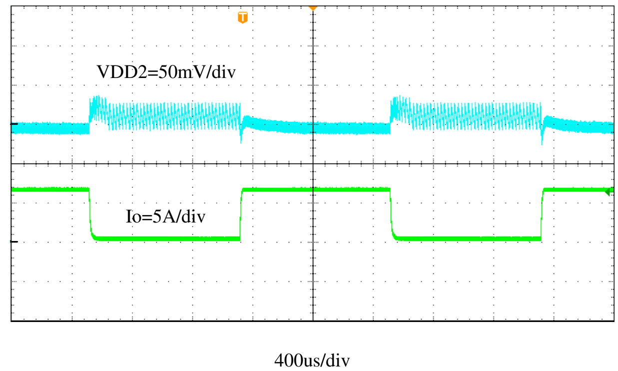
Slew Rate=2.5A/us

Figure 8-26. VDD1 Transient Response, 0 A to 1 A



Slew Rate=2.5A/us

Figure 8-27. VDD2 Transient Response, 1.6 A to 8 A



Slew Rate=2.5A/us

Figure 8-28. VDD2 Transient Response, 0.1 A to 6.4 A

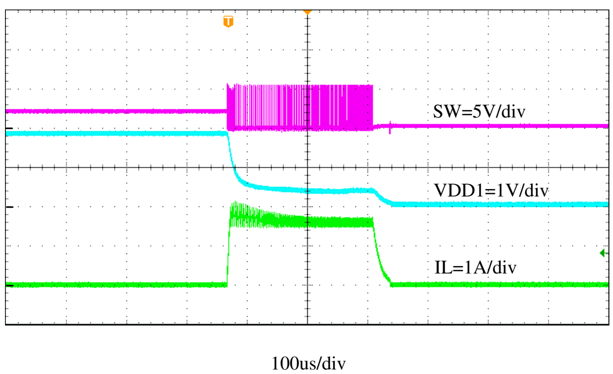


Figure 8-29. VDD1 Normal Operation to Output Hard Short

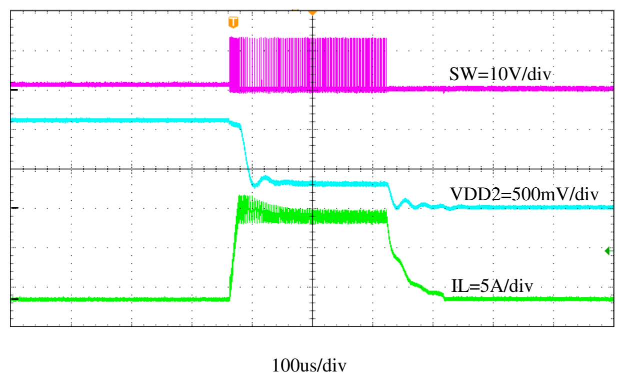


Figure 8-30. VDD2 Normal Operation to Output Hard Short

9 Power Supply Recommendations

The TPS65296 is designed for LPDDR4/LPDDR4X complete power solution. PVIN is the power input for VDD2 buck, PVIN_VDD1 is the power input for VDD1 buck, VLDOIN input is for VDDQ LDO power supply, VCC_5V is power supply for internal control logic. Below lists the power on sequence scenarios.

- VDD_EN is high before PVIN or PVIN_VDD1 has the power input, VCC_5V power supply must be provided after or same time with PVIN or PVIN_VDD1, otherwise the output will be latched. This latch can be recovered by toggling the VDD_EN pin or re-power the VCC_5V.
- VDD_EN is low before PVIN and PVIN_VDD1 has the power input, then there is no power supply input sequence requirement for VCC_5V, PVIN and PVIN_VDD1.

10 Layout

10.1 Layout Guidelines

- A four-layer PCB is recommended for good thermal performance and with maximum ground plane. 3-inch × 3-inch, four-layer PCB with 2-oz. copper is used as example.
- Place the decoupling capacitors right across PVIN, PVIN_VDD1, and VLDOIN as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a width plane to carry big current, enough vias should be added to the PGND connection of output capacitor and also as close to the output pin as possible. Reserve some space between VDD1 choke and VDD2 choke, just minimize radiation crosstalk.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- VDD1SNS/VDD2SNS/VDDQSNS can be 10 mil and must be routed away from the switching node, BST node or other high efficiency signal.
- PVIN and PVIN_VDD1 trace must be wide to reduce the trace impedance and provide enough current capability.
- Output capacitors for VDDQ and VDDQREF should be put as close as output pin.

10.2 Layout Example

Figure 10-1 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in Figure 8-1.

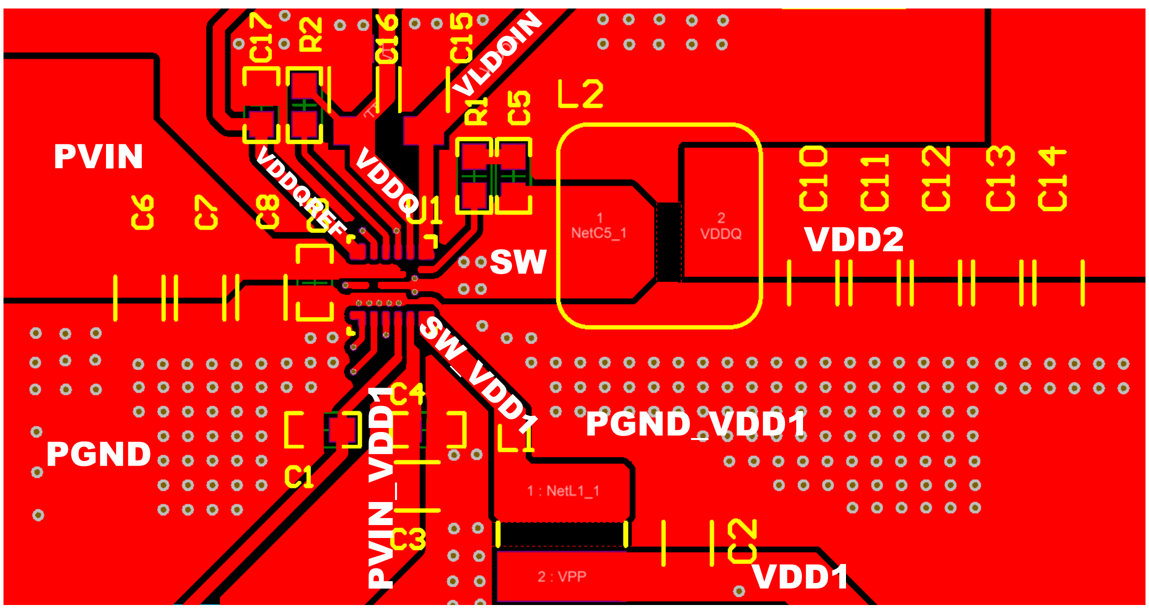


Figure 10-1. Top-Side Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Trademarks

D-CAP3™, Eco-mode™, HotRod™, TI E2E™ are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65296RJER	ACTIVE	VQFN-HR	RJE	18	3000	RoHS & Green	Call TI | SN | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65296	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

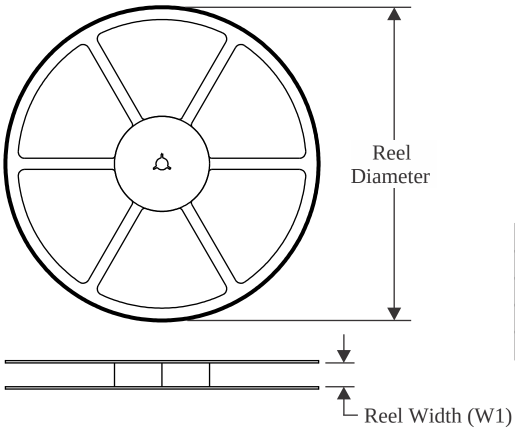
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

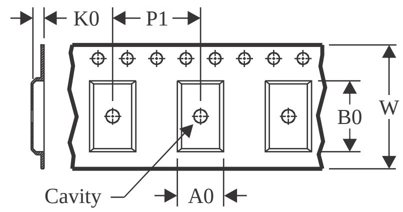
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

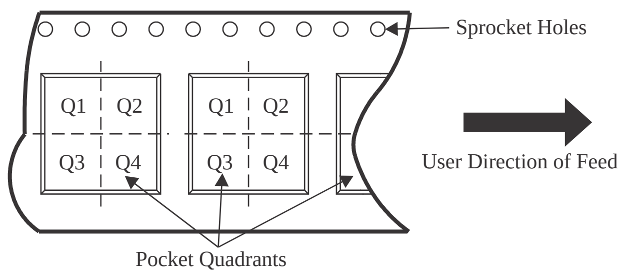


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

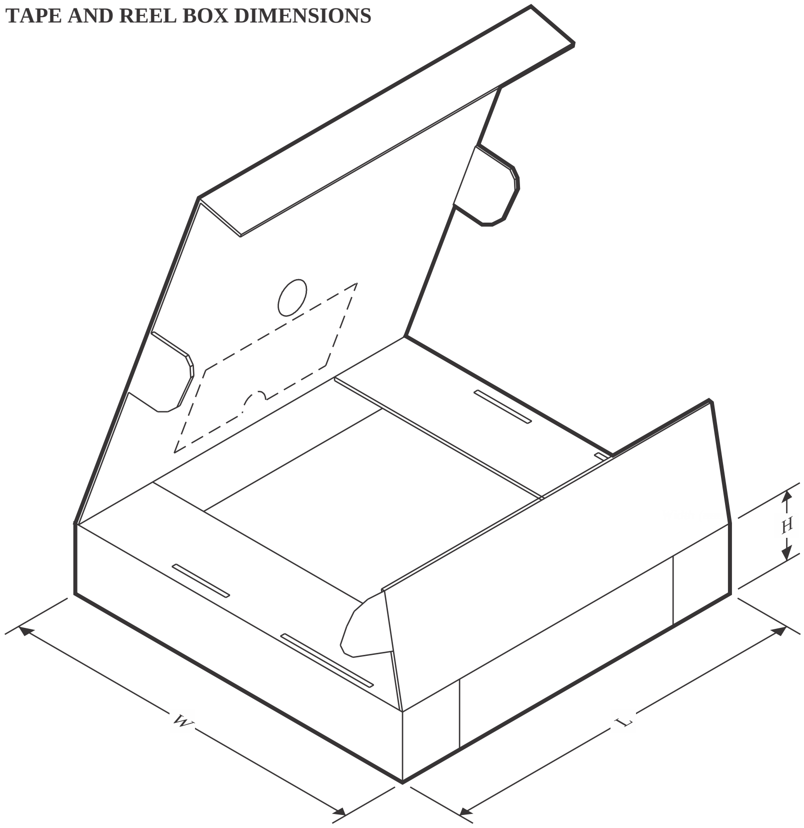
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

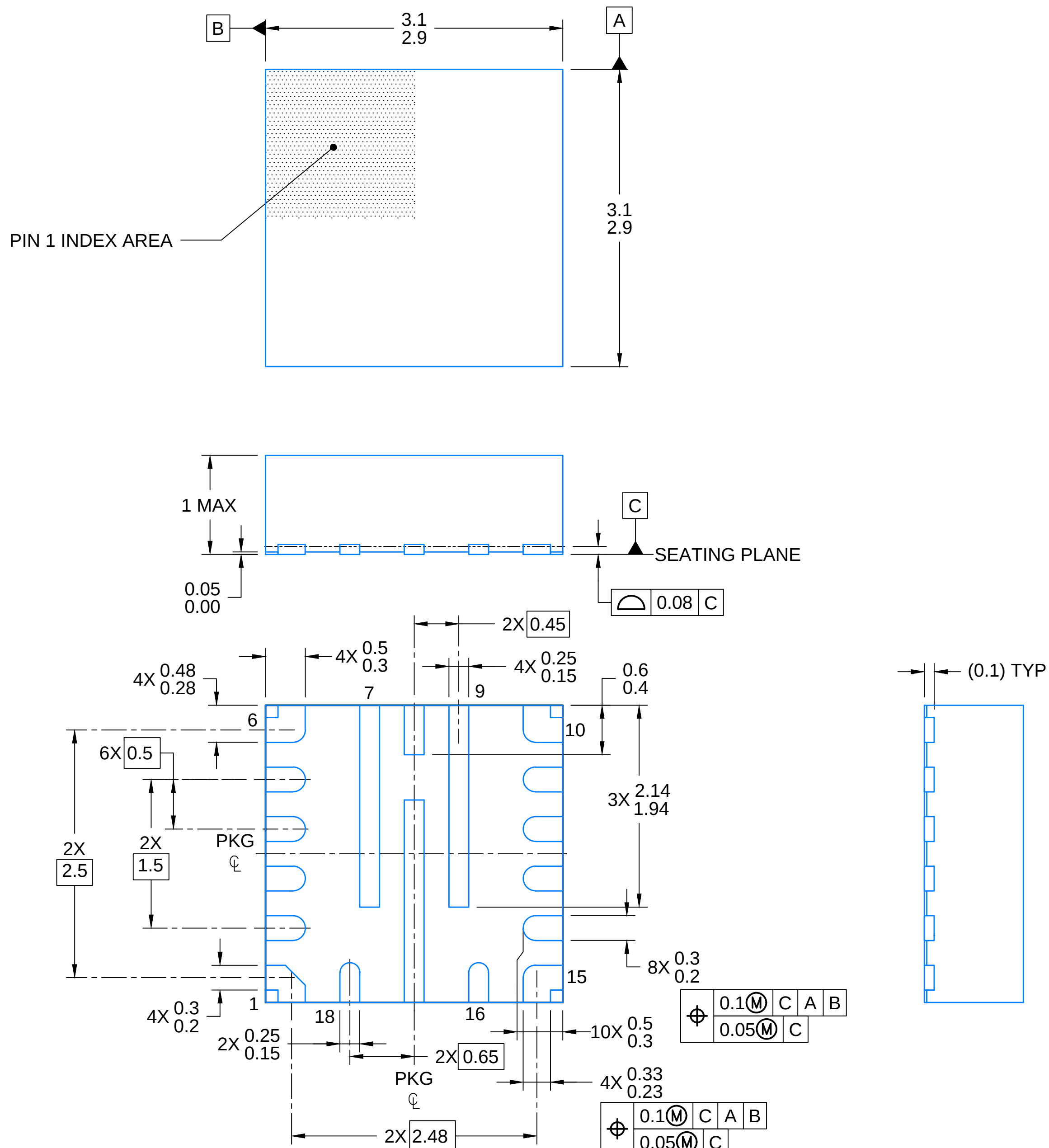
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65296RJER	VQFN-HR	RJE	18	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65296RJER	VQFN-HR	RJE	18	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

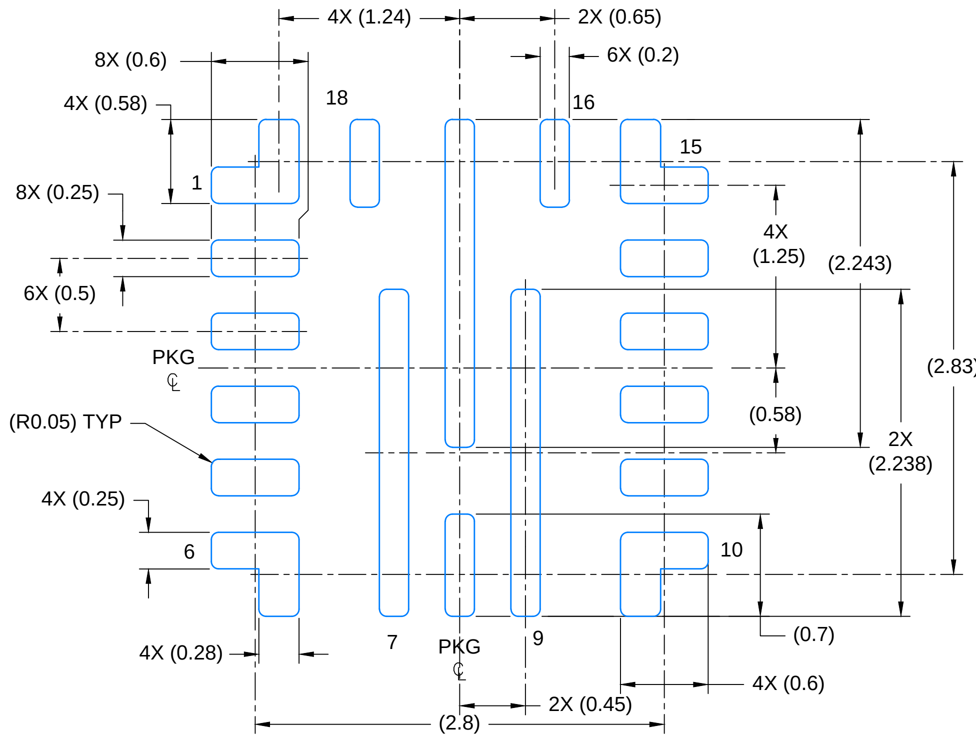
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65296RJER	VQFN-HR	RJE	18	3000	367.0	367.0	35.0
TPS65296RJER	VQFN-HR	RJE	18	3000	346.0	346.0	33.0



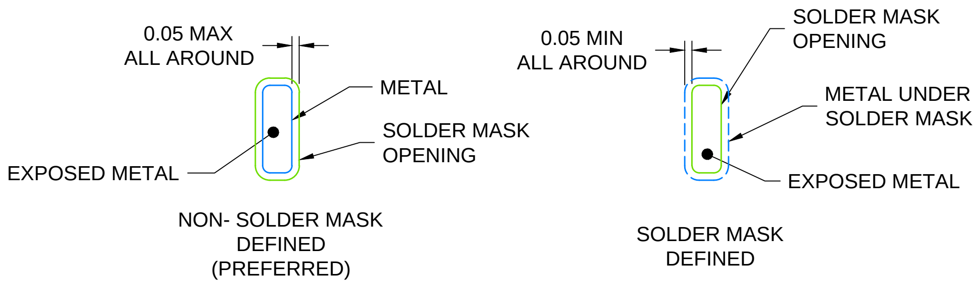
4223865 / C 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

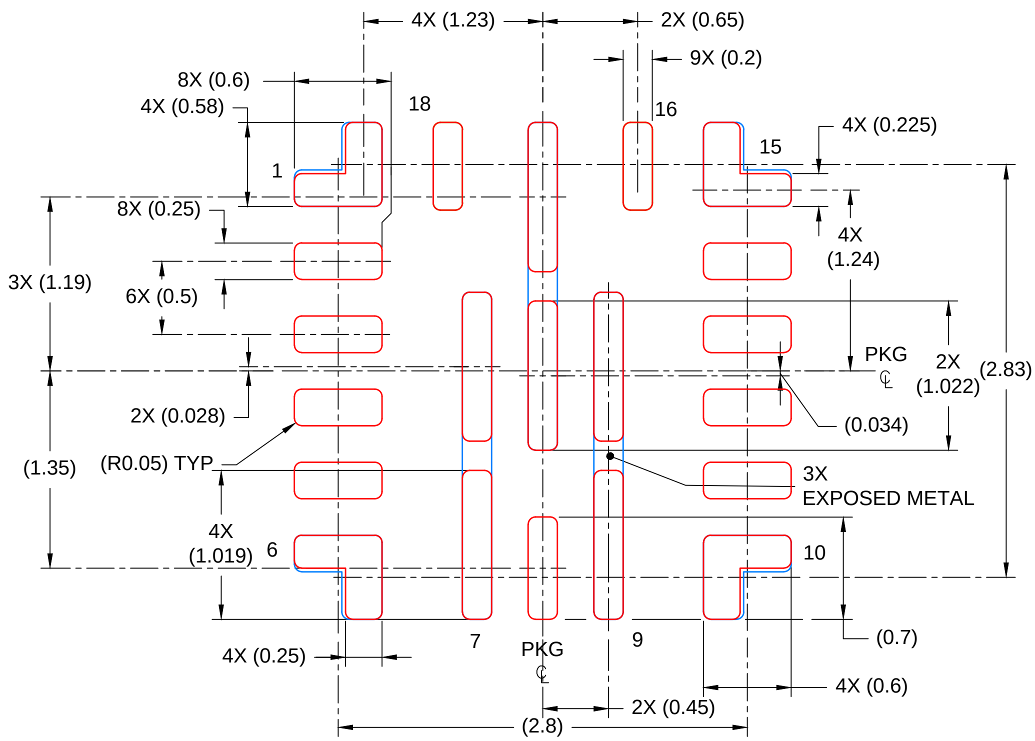


SOLDER MASK DETAILS

4223865 / C 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 6, 10 &15: 93% & PADS 7-9,17:89%
SCALE: 20X

4223865 / C 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..