LF412-N-MIL Low Offset, Low Drift Dual JFET Input Operational Amplifier

1 Features

- Internally Trimmed Offset Voltage: 1 mV (Max)
- Input Offset Voltage Drift: 7 µV/°C (Typ)
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA / $\sqrt{Hz}$
- Wide Gain Bandwidth: 3 MHz (Min)
- High Slew Rate: 10V/µs (Min)
- Low Supply Current: 1.8 mA/Amplifier
- High Input Impedance: 10^{12} Ω
- Low Total Harmonic Distortion: ≤ 0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 µs

2 Applications

- High Speed Integrators
- Fast D/A Converters
- Sample and Hold Circuits

3 Description

These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412-N-MIL dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF412-N-MIL	PDIP (8)	9.59 mm × 6.35 mm
	TO (8)	9.14 mm diameter

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Inverting Amplifier

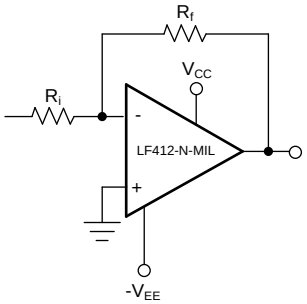


Table of Contents

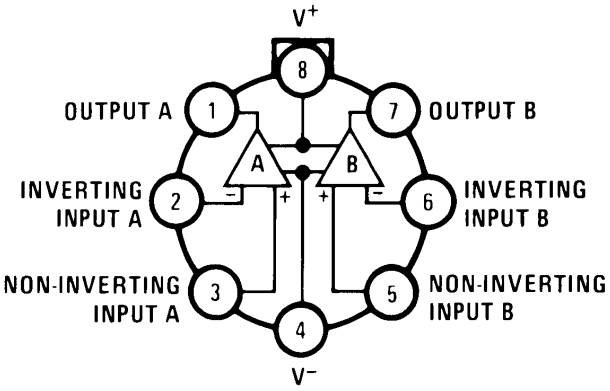
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2017	*	Initial release.

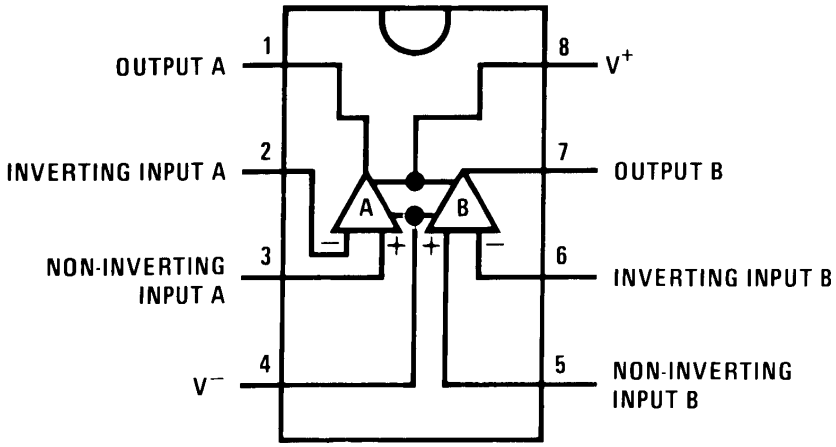
5 Pin Configuration and Functions

LMC Package
8-Pin TO
Top View



Note. Pin 4 connected to case.

P Package
8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Inverting input A	2	I	Amplifier A inverting input
Inverting input B	6	I	Amplifier B inverting input
Noninverting input A	3	I	Amplifier A noninverting input
Noninverting input B	5	I	Amplifier B noninverting input
Output A	1	O	Amplifier A output
Output B	7	O	Amplifier B output
V+	8	P	Positive supply
V-	4	P	Negative supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–18	18	V
Differential input voltage	–30	30	V
Input voltage range			
Output short circuit duration	Continuous		
Power dissipation	670		mW
T_J maximum		115	°C
Operating temperature range	See *Thermal Information*		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1700	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1700 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1700 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage			±15	V

6.4 Thermal Information

THERMAL METRIC(1)		LF412-N-MIL		UNIT
		LMC (TO)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (typical)	152	115	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LF412-N-MIL (1)			UNIT
				MIN	TYP	MAX	
V_{OS}	Input offset voltage	R_S =10 kΩ, T_A = 25°C			1	3	mV
$\Delta V_{OS}/\Delta T$	Average TC of input offset voltage	R_S = 10 kΩ			7		µV/°C
I_{OS}	Input offset current	V_S = ±15 V (2)	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
			T_J = 125°C			25	nA
I_B	Input bias current	V_S=±15V (2) (2)	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
			T_J = 125°C			50	nA
R_{IN}	Input resistance	T_J = 25°C			10^{12}		Ω
A_{VOL}	Large signal voltage gain	R_L = 2 k, T_A = 25°C, V_S = ±15 V, V_O = ±10 V		25	200		V/mV
		Over temperature		15	200		
V_O	Output voltage swing	V_S = ±15 V, R_L = 10 k		±12	±13.5		V
V_{CM}	Input common-mode voltage range			±11	14.5		V
					−11.5		V
CMRR	Common-mode rejection ratio	R_S ≤ 10 k		70	100		dB
PSRR	Supply voltage rejection ratio			(3)70	100		dB
I_S	Supply current	V_O = 0 V, R_L = ∞			3.6	6.5	mA

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±15 V for the LF412-N-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

(2) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(3) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6 V to ±15 V.

6.6 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	LF412-N-MIL (1)			UNIT
			MIN	TYP	MAX	
	Amplifier to amplifier coupling	T_A = 25°C f = 1 Hz – 20 kHz (Input referred)		−120		dB
SR	Slew rate	V_S = ±15 V T_A = 25°C	8	15		V/μs
GBW	Gain-bandwidth product	V_S = ±15 V T_A = 25°C	2.7	4		MHz
THD	Total harmonic dist	A_V = 10 R_L = 10 k V_O = 20 Vp-p BW = 20 Hz – 20 kHz		≤0.02%		
e_n	Equivalent input noise voltage	T_A = 25°C R_S = 100 Ω f = 1 kHz		25		nV / $\sqrt{Hz}$
i_n	Equivalent input noise current	T_A = 25°C, f = 1 kHz		0.01		pA / $\sqrt{Hz}$

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S = ±15 V for the LF412-N-MIL. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

6.7 Typical Characteristics

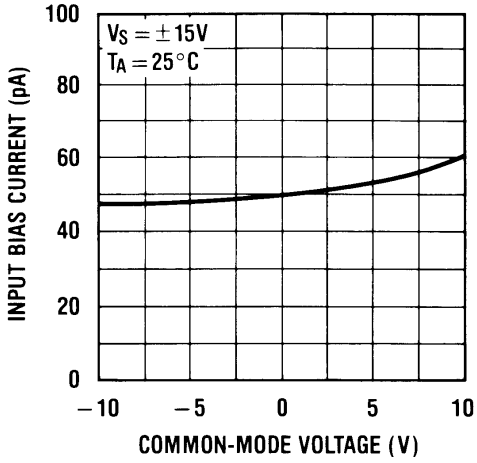


Figure 1. Input Bias Current

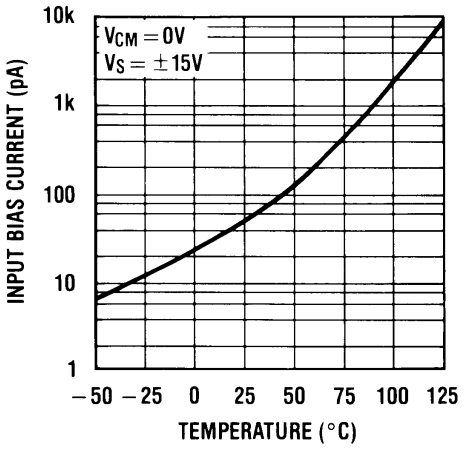


Figure 2. Input Bias Current

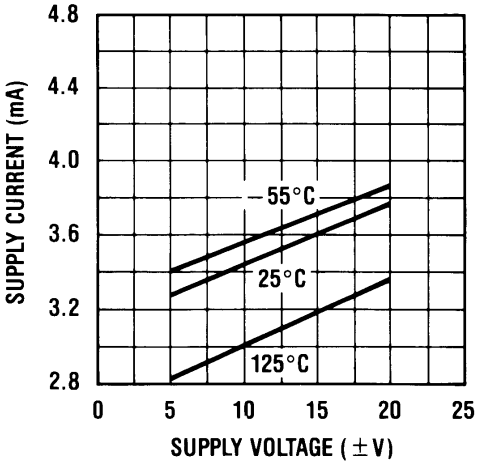


Figure 3. Supply Current

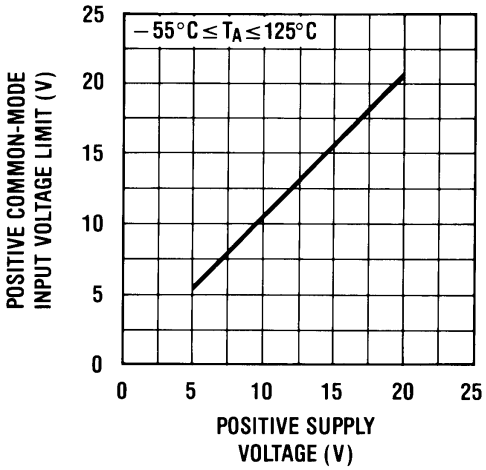


Figure 4. Positive Common-Mode Input Voltage Limit

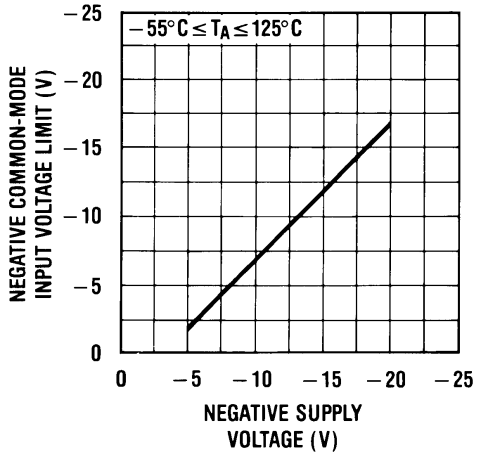


Figure 5. Negative Common-Mode Input Voltage Limit

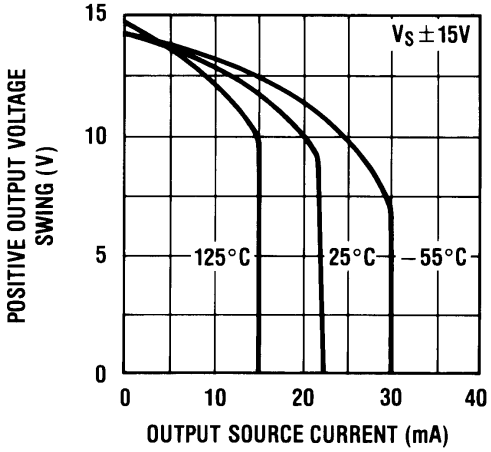


Figure 6. Positive Current Limit

Typical Characteristics (continued)

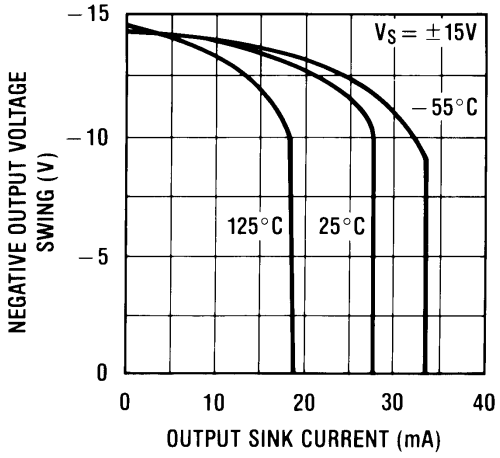


Figure 7. Negative Current Limit

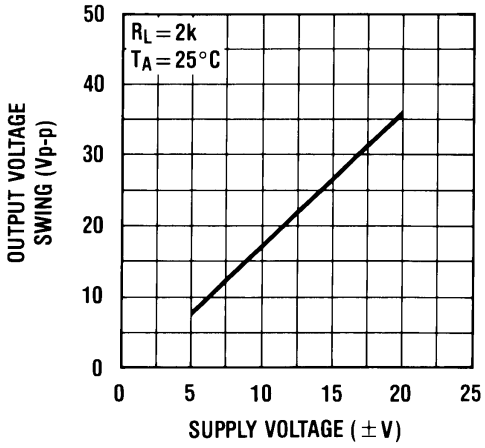


Figure 8. Output Voltage Swing

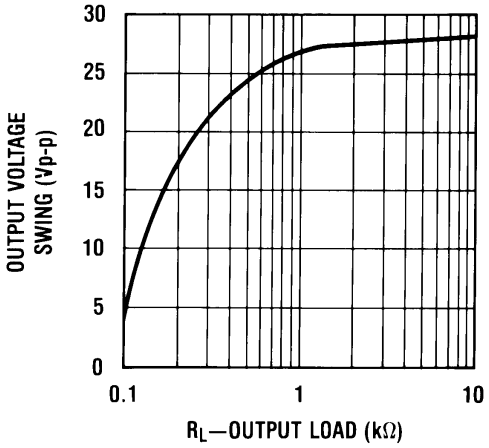


Figure 9. Output Voltage Swing

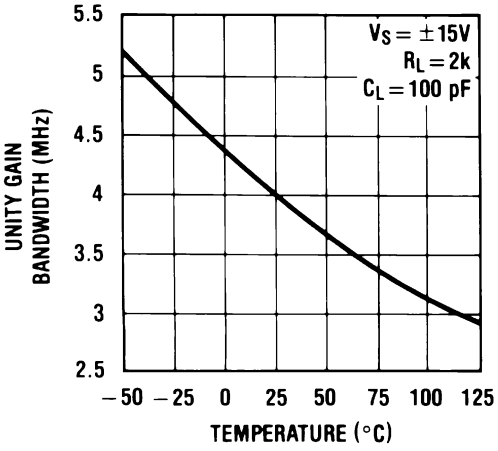


Figure 10. Gain Bandwidth

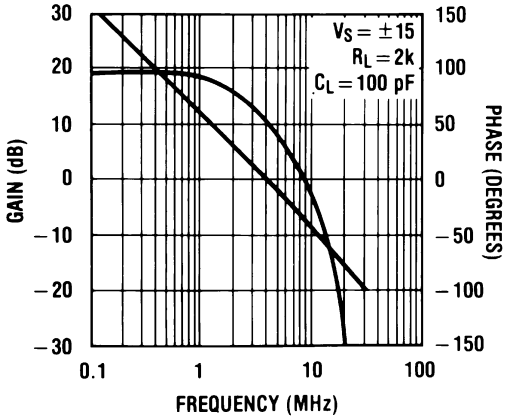


Figure 11. Bode Plot

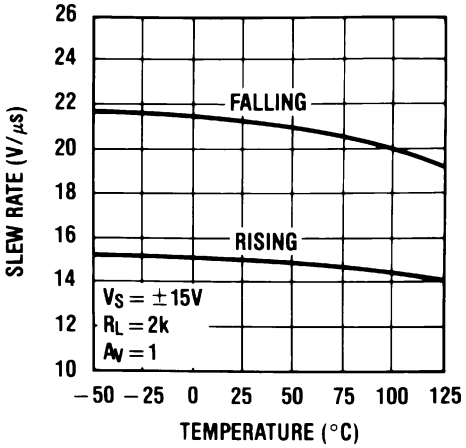


Figure 12. Slew Rate

Typical Characteristics (continued)

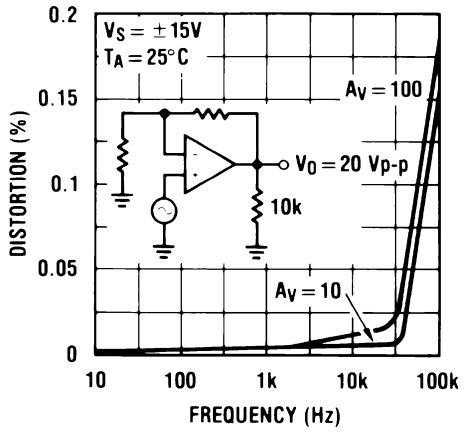


Figure 13. Distortion vs Frequency

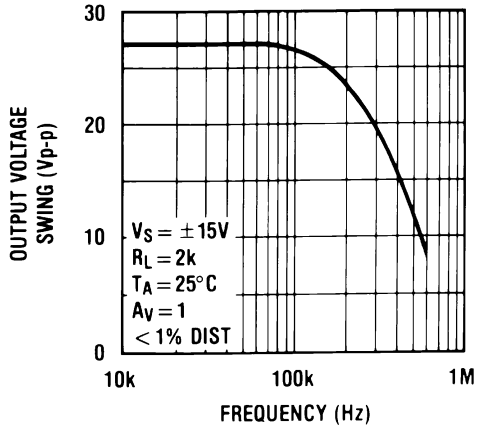


Figure 14. Undistorted Output Voltage Swing

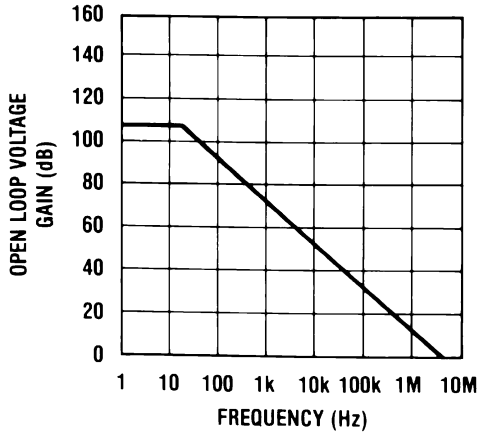


Figure 15. Open Loop Frequency Response

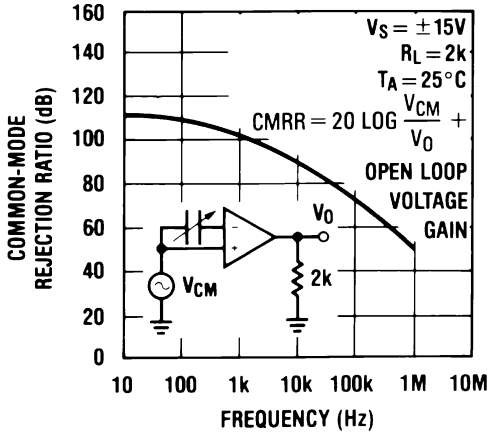


Figure 16. Common-Mode Rejection Ratio

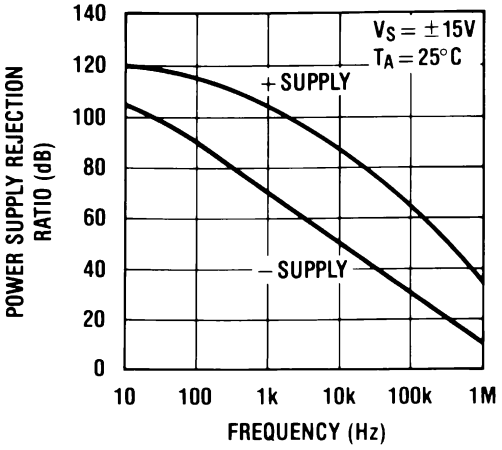


Figure 17. Power Supply Rejection Ratio

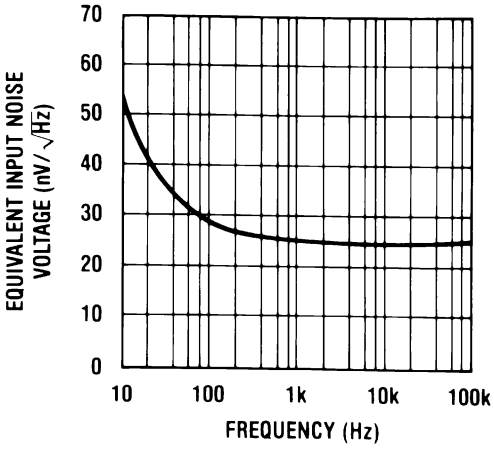


Figure 18. Equivalent Input Noise Voltage

Typical Characteristics (continued)

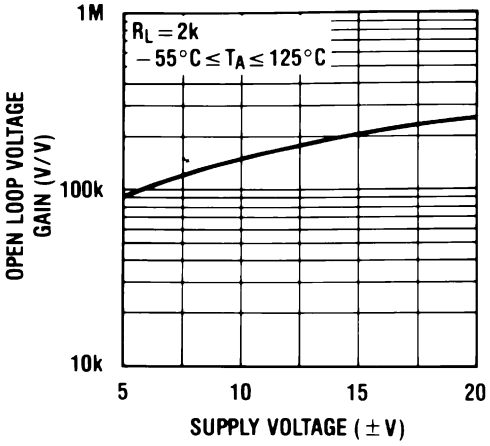


Figure 19. Open Loop Voltage Gain

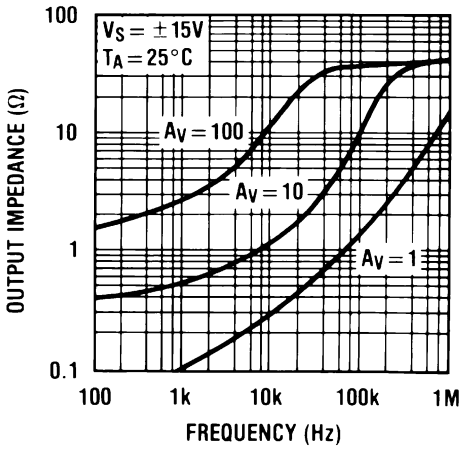


Figure 20. Output Impedance

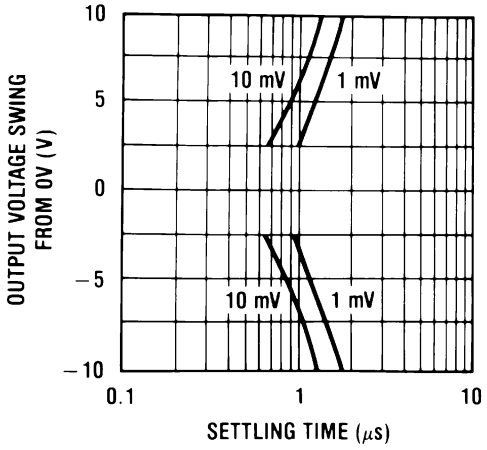
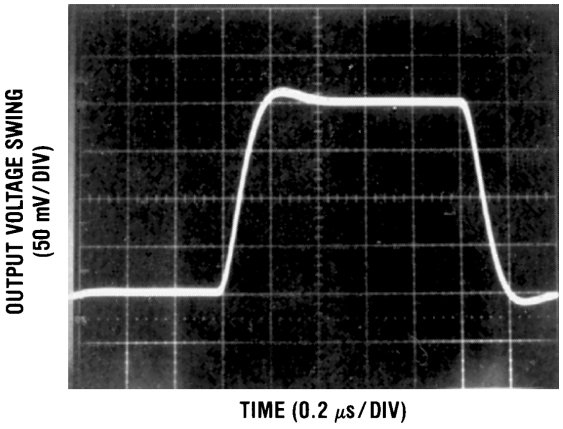
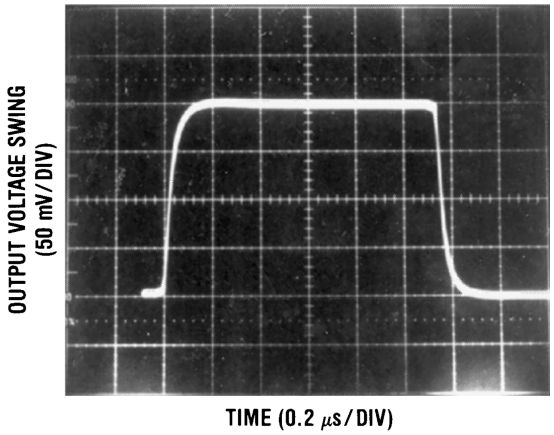


Figure 21. Inverter Settling Time



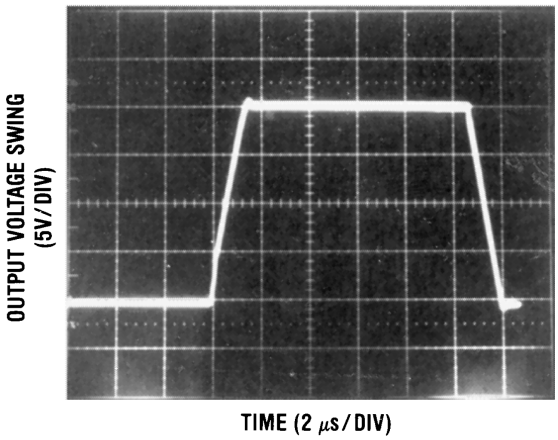
R_L = 2 kΩ C_L = 10 pF

Figure 22. Small Signal Inverting



R_L = 2 kΩ C_L = 10 pF

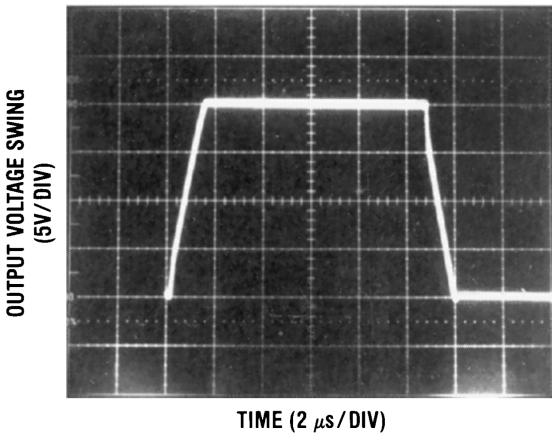
Figure 23. Small Signal Non-Inverting



R_L = 2 kΩ C_L = 10 pF

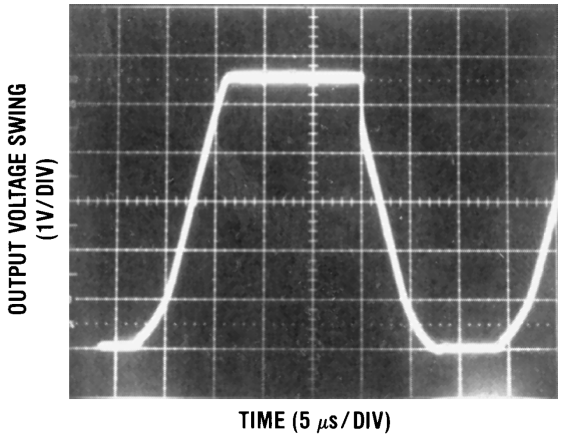
Figure 24. Large Signal Inverting

Typical Characteristics (continued)



R_L = 2 kΩ C_L = 10 pF

Figure 25. Large Signal Non-Inverting



R_L = 100 Ω C_L = 10 pF

Figure 26. Current Limit

7 Detailed Description

7.1 Overview

The LF412-N-MIL devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412-N-MIL dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

7.2 Functional Block Diagram

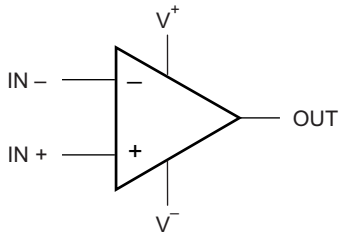


Figure 27. Each Amplifier

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

7.4 Device Functional Modes

7.4.1 Input and Output Stage

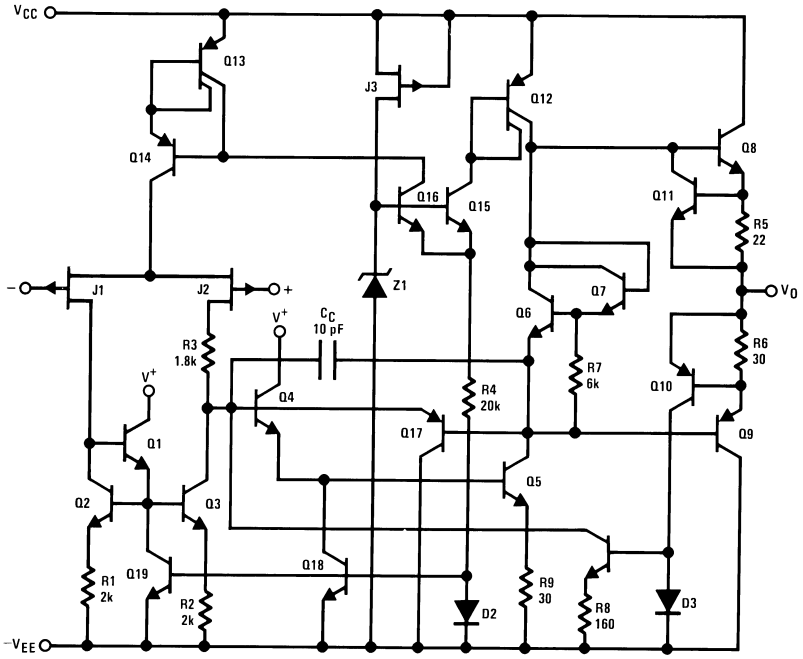


Figure 28. 1/2 Dual LF412-N-MIL

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF412-N-MIL series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

8.2 Typical Application

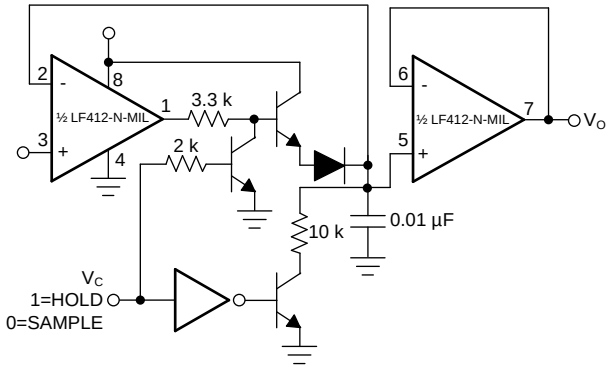


Figure 29. Single-Supply Sample and Hold

8.2.1 Design Requirements

Single-supply.

8.2.2 Detailed Design Procedure

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6 V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

Typical Application (continued)

The amplifiers will drive a 2 kΩ load resistance to ±10 V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2.3 Application Curves

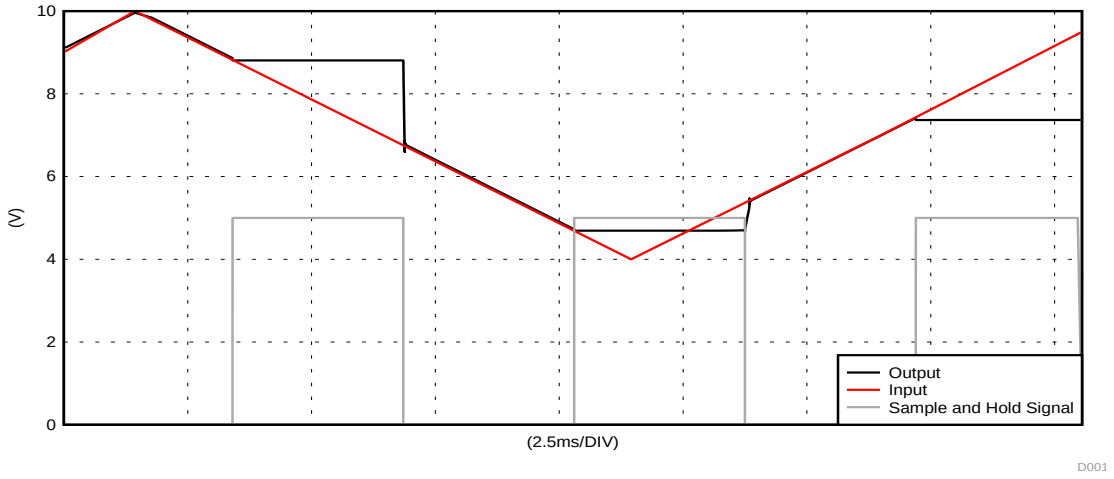


Figure 30. Sample and Hold Waveforms

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1 µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5 V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

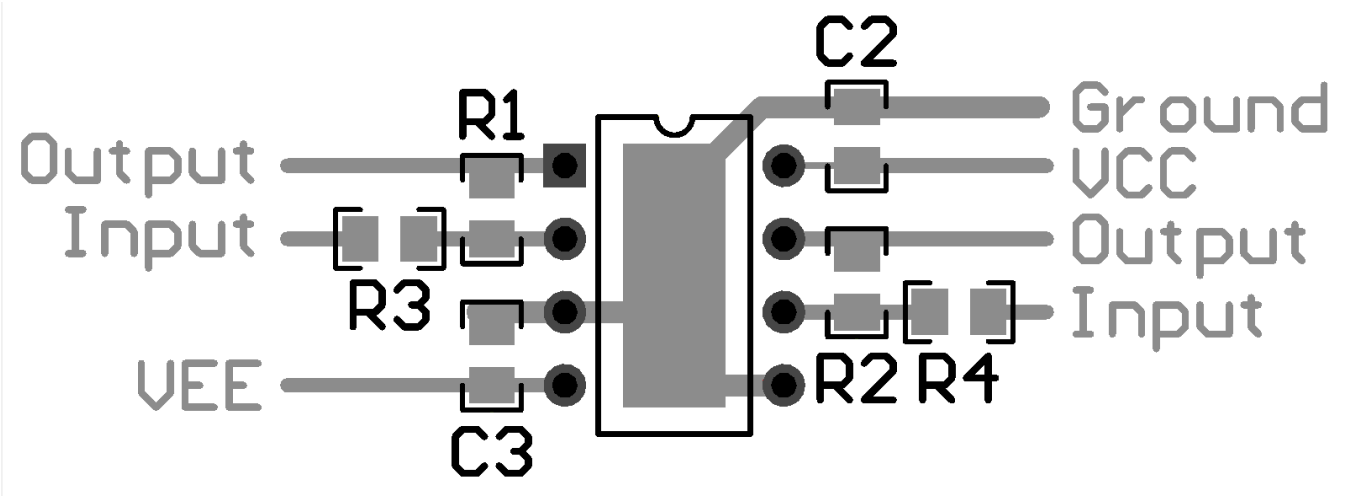


Figure 31. LF412-N-MIL Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

BI-FET II, E2E are trademarks of Texas Instruments.
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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF412MH	ACTIVE	TO-99	LMC	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF412MH, LF412MH)	Samples
LF412MH/NOPB	ACTIVE	TO-99	LMC	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF412MH, LF412MH)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

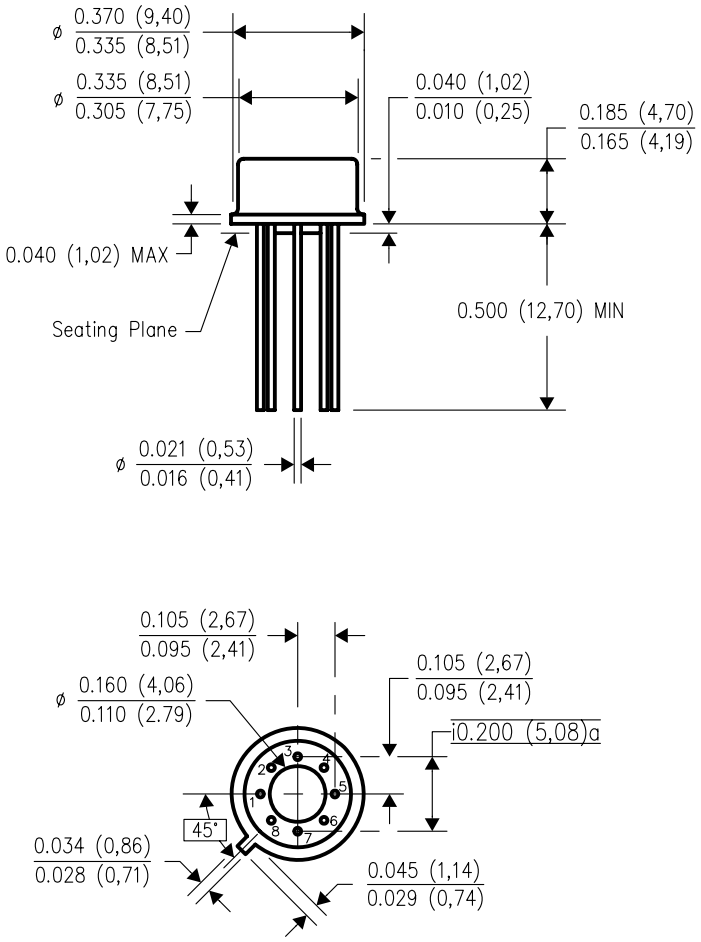
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

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