

## Hex Schmitt-Trigger Inverters

### 1 Features

- $V_{CC}$  operation of 2 V to 6 V
- Inputs accept voltages to 6 V
- Max  $t_{pd}$  of 9.5 ns at 5 V

### 2 Applications

- Synchronize inverted clock inputs
- Debounce a switch
- Invert a digital signal

### 3 Description

These Schmitt-trigger devices contain six independent inverters.

#### Package Information

| PART NUMBER | PACKAGE | BODY SIZE (NOM)   |
|-------------|---------|-------------------|
| SNx4AC14    | SOIC    | 8.65 mm x 3.9 mm  |
|             | SSOP    | 6.2 mm x 1.95 mm  |
|             | PDIP    | 19.3 mm x 6.35 mm |
|             | SOP     | 10.3 mm x 5.3 mm  |
|             | TSSOP   | 5.00 mm x 4.4 mm  |



Logic Diagram (Positive Logic)



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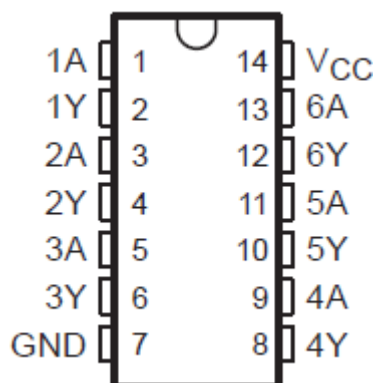
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## 4 Revision History

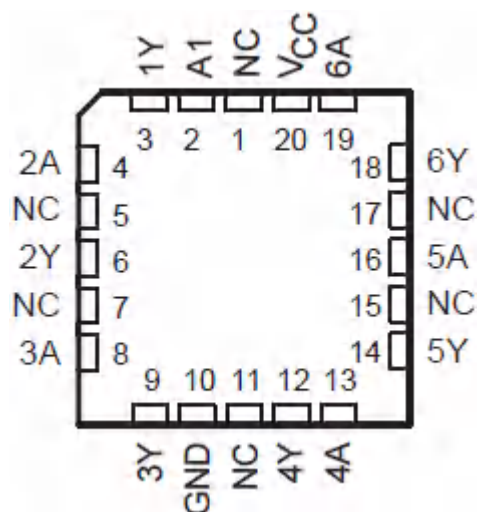
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision G (August 2008) to Revision H (January 2023)</b>  | <b>Page</b> |
|--|-------------|
| <ul style="list-style-type: none"> <li>Added <i>Applications</i>, <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i>, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....</li> </ul> | <b>1</b>    |

## 5 Pin Configuration and Functions



**Figure 5-1. SN54AC14 J or W Package and SN74AC14 D, DB, N, NS, or PW Package Top View**



NC – No internal connection

**Figure 5-2. SN54AC14 FK Package Top View**

## Pin Functions

| PIN             |                                 |                        | I/O    | DESCRIPTION              |
|-----------------|---------------------------------|------------------------|--------|--------------------------|
| NAME            | D, DB, N,<br>NS, PW, J,<br>or W | FK                     |        |                          |
| 1A              | 1                               | 2                      | Input  | Channel 1, Input A       |
| 1Y              | 2                               | 3                      | Output | Channel 1, Output Y      |
| 2A              | 3                               | 4                      | Input  | Channel 2, Input A       |
| 2Y              | 4                               | 6                      | Output | Channel 2, Output Y      |
| 3A              | 5                               | 8                      | Input  | Channel 3, Input A       |
| 3Y              | 6                               | 9                      | Output | Channel 3, Output Y      |
| GND             | 7                               | 10                     | —      | Ground                   |
| 4Y              | 8                               | 12                     | Output | Channel 4, Output Y      |
| 4A              | 9                               | 13                     | Input  | Channel 4, Input A       |
| 5Y              | 10                              | 14                     | Output | Channel 5, Output Y      |
| 5A              | 11                              | 16                     | Input  | Channel 5, Input A       |
| 6Y              | 12                              | 18                     | Output | Channel 6, Output Y      |
| 6A              | 13                              | 19                     | Input  | Channel 6, Input A       |
| V <sub>CC</sub> | 14                              | 20                     | —      | Positive Supply          |
| NC              |                                 | 1, 5, 7, 11, 15,<br>17 | —      | Not internally connected |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted<sup>(1)</sup>)

|  |                          | UNIT |
|--|--------------------------|------|
| Supply voltage range, $V_{CC}$                                 | -0.5 V to 7              | V    |
| Input voltage range, $V_I$ <sup>(2)</sup>                      | -0.5 V to $V_{CC} + 0.5$ | V    |
| Output voltage range, $V_O$ <sup>(2)</sup>                     | -0.5 V to $V_{CC} + 0.5$ | V    |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )  | $\pm 20$                 | mA   |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) | $\pm 20$                 | mA   |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )     | $\pm 50$                 | mA   |
| Continuous current through $V_{CC}$ or GND                     | $\pm 200$                | mA   |
| Storage temperature range, $T_{stg}$                           | -65 to 150               | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|             |                         |  | VALUE      | UNIT |
|-------------|-------------------------|--|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | $\pm 4000$ | V    |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | $\pm 2000$ |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommend Operating Conditions

|                 |                                |                         | SN54AC14 |                 | SN74AC14 |                 | UNIT |
|-----------------|--------------------------------|-------------------------|----------|-----------------|----------|-----------------|------|
|                 |                                |                         | MIN      | MAX             | MIN      | MAX             |      |
| V <sub>CC</sub> | Supply voltage                 |                         | 2        | 6               | 2        | 6               | V    |
| V <sub>I</sub>  | Input voltage                  |                         | 0        | V <sub>CC</sub> | 0        | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                 |                         | 0        | V <sub>CC</sub> | 0        | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current      | V <sub>CC</sub> = 3 V   | -12      |                 | -12      |                 | mA   |
|                 |                                | V <sub>CC</sub> = 4.5 V | -24      |                 | -24      |                 |      |
|                 |                                | V <sub>CC</sub> = 5.5 V | -24      |                 | -24      |                 |      |
| I <sub>OL</sub> | Low-level output current       | V <sub>CC</sub> = 3 V   | 12       |                 | 12       |                 | mA   |
|                 |                                | V <sub>CC</sub> = 4.5 V | 24       |                 | 24       |                 |      |
|                 |                                | V <sub>CC</sub> = 5.5 V | 24       |                 | 24       |                 |      |
| T <sub>A</sub>  | Operating free-air temperature |                         | -55      | 125             | -40      | 85              | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | SNx4AC14 |           |          |         |            | UNIT |
|-------------------------------|--|----------|-----------|----------|---------|------------|------|
|                               |  | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) |      |
|                               |  | 14 PINS  |           |          |         |            |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 86       | 96        | 80       | 76      | 113        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54AC14 |     | SN74AC14 |     | UNIT |
|---|---|-----------------|-----------------------|-----|-----|----------|-----|----------|-----|------|
|   |   |                 | MIN                   | TYP | MAX | MIN      | MAX | MIN      | MAX |      |
| V <sub>T+</sub><br>Positive-going threshold                           |   | 3 V             | 0.8                   | 1.8 | 2.2 | 0.8      | 2.2 | 0.8      | 2.2 | V    |
|   |   | 4.5 V           | 1.5                   | 2.6 | 3.2 | 1.5      | 3.2 | 1.5      | 3.2 |      |
|   |   | 5.5 V           | 1.6                   | 3.2 | 3.9 | 1.6      | 3.9 | 1.6      | 3.9 |      |
| V <sub>T-</sub><br>Negative-going threshold                           |   | 3 V             | 0.5                   | 0.8 | 1   | 0.5      | 1.2 | 0.5      | 1   | V    |
|   |   | 4.5 V           | 0.9                   | 1.4 | 1.8 | 0.9      | 1.8 | 0.9      | 1.8 |      |
|   |   | 5.5 V           | 1.1                   | 1.8 | 2.3 | 1.1      | 2.3 | 1.1      | 2.3 |      |
| ΔV <sub>T</sub><br>Hysteresis<br>(V <sub>T+</sub> - V <sub>T-</sub> ) |   | 3 V             | 0.3                   | 1   | 1.2 | 0.3      | 1.2 | 0.3      | 1.2 | V    |
|   |   | 4.5 V           | 0.4                   | 1.2 | 1.4 | 0.4      | 1.4 | 0.4      | 1.4 |      |
|   |   | 5.5 V           | 0.5                   | 1.4 | 1.6 | 0.5      | 1.6 | 0.5      | 1.6 |      |
| V <sub>OH</sub>   | I <sub>OH</sub> = -50 μA                                    | 3 V             | 2.9                   |     |     | 2.9      |     | 2.9      |     | V    |
|   |   | 4.5 V           | 4.4                   |     |     | 4.4      |     | 4.4      |     |      |
|   |   | 5.5 V           | 5.4                   |     |     | 5.4      |     | 5.4      |     |      |
|   | I <sub>OH</sub> = -12 mA                                    | 3 V             | 2.56                  |     |     | 2.4      |     | 2.48     |     |      |
|   | I <sub>OH</sub> = -24 mA                                    | 4.5 V           | 3.86                  |     |     | 3.7      |     | 3.8      |     |      |
|   |   | 5.5 V           | 4.86                  |     |     | 4.7      |     | 4.8      |     |      |
|   | I <sub>OH</sub> = -50 mA <sup>(1)</sup>                     | 5.5 V           |                       |     |     | 3.85     |     |          |     |      |
|   | I <sub>OH</sub> = -75 mA <sup>(1)</sup>                     |                 |                       |     |     |          |     | 3.85     |     |      |
| V <sub>OL</sub>   | I <sub>OL</sub> = 50 μA                                     | 3 V             | 0.1                   |     |     | 0.1      |     | 0.1      |     | V    |
|   |   | 4.5 V           | 0.1                   |     |     | 0.1      |     | 0.1      |     |      |
|   |   | 5.5 V           | 0.1                   |     |     | 0.1      |     | 0.1      |     |      |
|   | I <sub>OL</sub> = 12 mA                                     | 3 V             | 0.36                  |     |     | 0.44     |     | 0.44     |     |      |
|   | I <sub>OL</sub> = 24 mA                                     | 4.5 V           | 0.36                  |     |     | 0.44     |     | 0.44     |     |      |
|   |   | 5.5 V           | 0.36                  |     |     | 0.44     |     | 0.44     |     |      |
|   | I <sub>OL</sub> = 50 mA <sup>(1)</sup>                      | 5.5 V           |                       |     |     | 1.65     |     |          |     |      |
|   | I <sub>OL</sub> = 75 mA <sup>(1)</sup>                      |                 |                       |     |     |          |     | 1.65     |     |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           | ±0.1                  |     |     | ±1       |     | ±1       |     | μA   |
| I <sub>CC</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 2                     |     |     | 40       |     | 20       |     | μA   |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             | 4.5                   |     |     |          |     |          |     | pF   |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | T <sub>A</sub> = 25°C |     |      | SN54AC14 |     | SN74AC14 |     | UNIT |
|------------------|--------------|-------------|-----------------------|-----|------|----------|-----|----------|-----|------|
|                  |              |             | MIN                   | TYP | MAX  | MIN      | MAX | MIN      | MAX |      |
| t <sub>PLH</sub> | A            | Y           | 1.5                   | 6   | 13.5 | 1        | 16  | 1.5      | 15  | ns   |
| t <sub>PHL</sub> |              |             | 1.5                   | 6   | 11.5 | 1        | 14  | 1.5      | 13  |      |

## 6.7 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $T_A = 25^\circ\text{C}$ |     |     | SN54AC14 |     | SN74AC14 |     | UNIT |
|-----------|-----------------|----------------|--------------------------|-----|-----|----------|-----|----------|-----|------|
|           |                 |                | MIN                      | TYP | MAX | MIN      | MAX | MIN      | MAX |      |
| $t_{PLH}$ | A               | Y              | 1.5                      | 5   | 10  | 1.5      | 12  | 1.5      | 11  | ns   |
| $t_{PHL}$ |                 |                | 1.5                      | 5   | 8.5 | 1.5      | 10  | 1.5      | 9.5 |      |

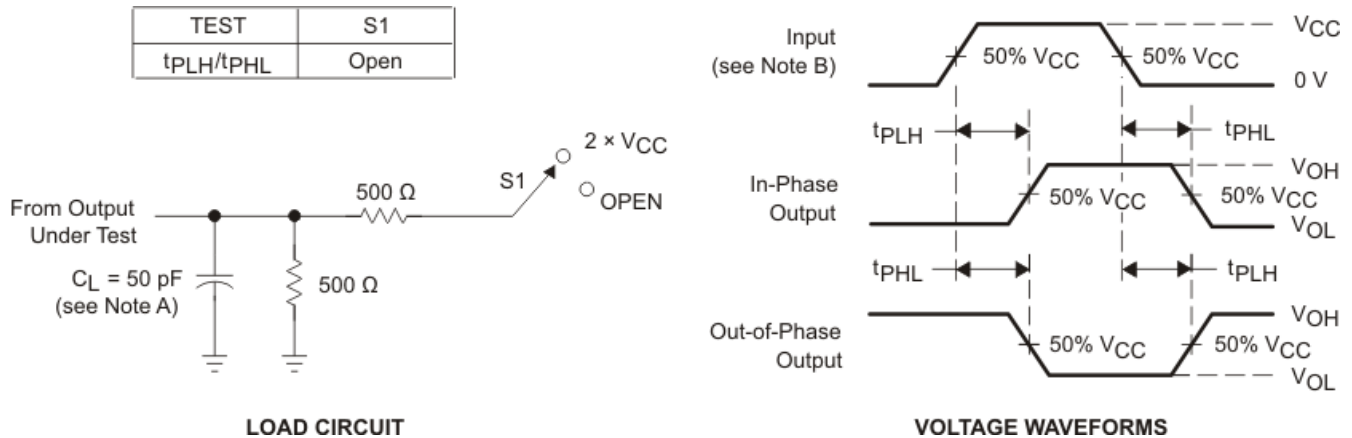
## 6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS                           | TYP | UNIT |
|-----------|-------------------------------|---|-----|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 25  | pF   |

## 7 Parameter Measurement Information

### 7.1



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- C. The outputs are measured one at a time with one input transition per measurement.

**Figure 7-1. Load Circuit and Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

These 'AC14 devices perform the Boolean function  $Y = \bar{A}$ . Because of the Schmitt action, they have different input threshold levels for positive-going ( $V_{T+}$ ) and for negative-going ( $V_{T-}$ ) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- $V_{CC}$  is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs accept  $V_{IH}$  levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

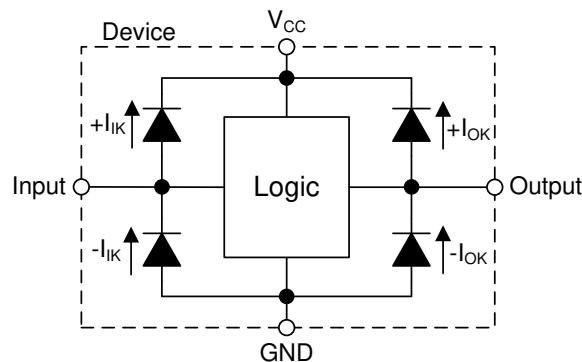
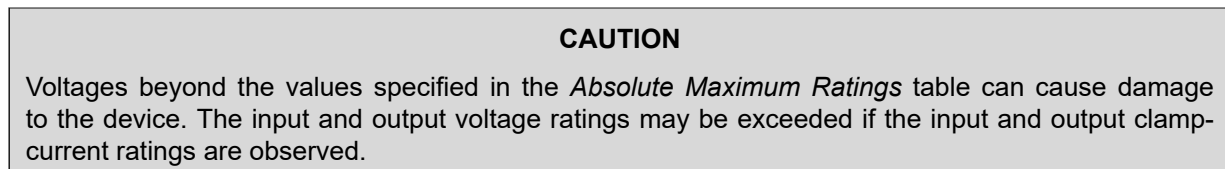
#### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

#### 8.3.2 Clamp Diode Structure

As shown in [Figure 8-1](#), the inputs and outputs to this device have both positive and negative clamping diodes.



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Function Table**

| INPUT | OUTPUT |
|-------|--------|
| A     | Y      |
| H     | L      |
| L     | H      |

## 9 Application Information Disclaimer

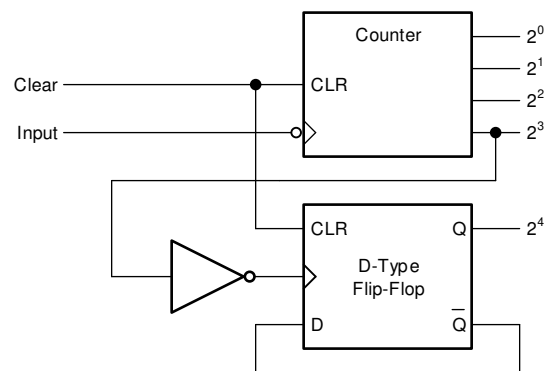
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4AC14 device is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid  $V_{CC}$ . This feature makes it ideal for translating down to the  $V_{CC}$  level. [Switching Characteristics Comparison](#) shows the reduction in ringing compared to higher drive parts such as AC.

### 9.2 Typical Application



**Figure 9-1. Typical Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Section 6.3](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Section 6.3](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## 9.2.3 Application Curves

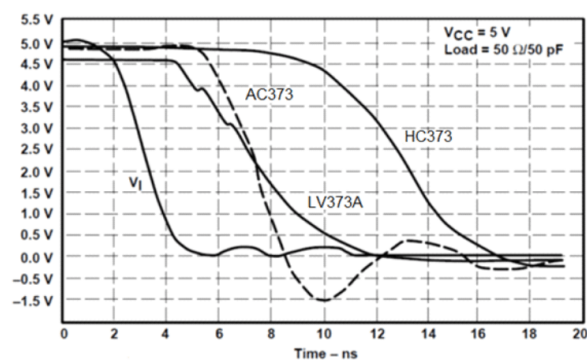


Figure 9-2. Switching Characteristics Comparison

## 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 6.3](#).

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

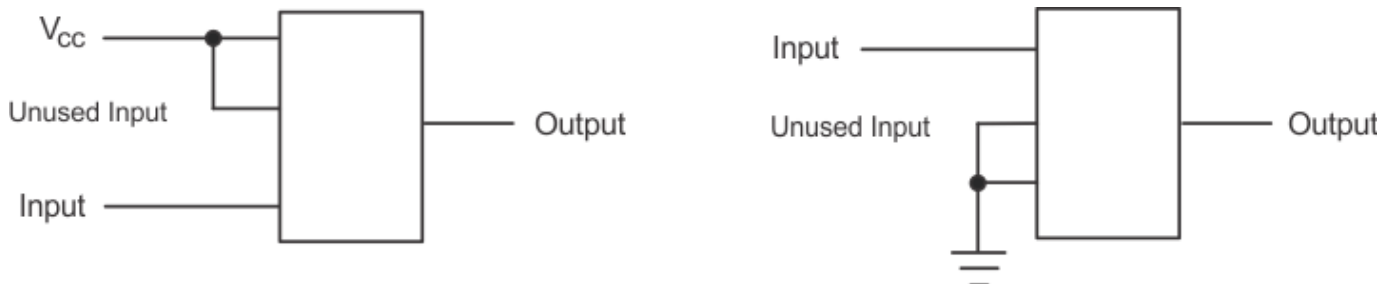
## 9.4 Layout

### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Layout Diagram](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 9.4.2 Layout Example



**Figure 9-3. Layout Diagram**

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 10-1. Related Links**

| PARTS    | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AC14 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74AC14 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

#### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)               | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|---------------------------------------|-------------------------|
| 5962-87624012A   | ACTIVE        | LCCC         | FK                 | 20   | 55             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>87624012A<br>SNJ54AC<br>14FK | <a href="#">Samples</a> |
| 5962-8762401CA   | ACTIVE        | CDIP         | J                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401CA<br>SNJ54AC14J          | <a href="#">Samples</a> |
| 5962-8762401DA   | ACTIVE        | CFP          | W                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401DA<br>SNJ54AC14W          | <a href="#">Samples</a> |
| 5962-8762401VCA  | ACTIVE        | CDIP         | J                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401VC<br>A<br>SNV54AC14J     | <a href="#">Samples</a> |
| 5962-8762401VDA  | ACTIVE        | CFP          | W                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401VD<br>A<br>SNV54AC14W     | <a href="#">Samples</a> |
| 5962-8762402VCA  | ACTIVE        | CDIP         | J                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762402VC<br>A<br>SNV54AC14J     | <a href="#">Samples</a> |
| 5962-8762402VDA  | ACTIVE        | CFP          | W                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762402VD<br>A<br>SNV54AC14W     | <a href="#">Samples</a> |
| SN74AC14DBR      | ACTIVE        | SSOP         | DB                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC14                                  | <a href="#">Samples</a> |
| SN74AC14DR       | ACTIVE        | SOIC         | D                  | 14   | 2500           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC14                                  | <a href="#">Samples</a> |
| SN74AC14N        | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74AC14N                             | <a href="#">Samples</a> |
| SN74AC14NSR      | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC14                                  | <a href="#">Samples</a> |
| SN74AC14NSRG4    | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC14                                  | <a href="#">Samples</a> |
| SN74AC14PWR      | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | AC14                                  | <a href="#">Samples</a> |
| SNJ54AC14FK      | ACTIVE        | LCCC         | FK                 | 20   | 55             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>87624012A<br>SNJ54AC<br>14FK | <a href="#">Samples</a> |



| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)      | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------|-------------------------|
| SNJ54AC14J       | ACTIVE        | CDIP         | J                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401CA<br>SNJ54AC14J | <a href="#">Samples</a> |
| SNJ54AC14W       | ACTIVE        | CFP          | W                  | 14   | 25             | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8762401DA<br>SNJ54AC14W | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC14, SN54AC14-SP, SN74AC14 :**

- Catalog : [SN74AC14](#), [SN54AC14](#)
- Automotive : [SN74AC14-Q1](#), [SN74AC14-Q1](#)
- Military : [SN54AC14](#)
- Space : [SN54AC14-SP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC14DBR | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74AC14DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AC14DR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74AC14NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74AC14PWR | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC14DBR | SSOP         | DB              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AC14DR  | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74AC14DR  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74AC14NSR | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AC14PWR | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87624012A  | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-8762401DA  | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8762401VDA | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8762402VDA | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74AC14N       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AC14N       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AC14N       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AC14N       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54AC14FK     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54AC14W      | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\



**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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