Application Report
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HSTL Clock Buffer Using the CDCV850

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ABSTRACT

The demand for driving 1.5-V HSTL signals for high-integrated and low-voltage digital logic is increasing. Most current systems use LVDS, LVPECL, or 2.5-V LVCMOS signaling levels. Therefore, a solution is needed to convert these clock signals into HSTL signal swing.

The purpose this report is to show how to generate an HSTL compliant clock signal using the CDCV850. This clock buffer accepts LVDS, LVPECL, SSTL2, or 2.5-V LVCMOS signals on its input.

The CDCV850 runs from a power supply of 2.5 V. A few additional resistors and capacitors are required to shift the voltage level to HSTL and provide the correct attenuation factor to the CDCV850 output to meet HSTL signal swing.

HSTL Specification

The HSTL specification EIA/JESD8-6 (August 1995) and JESD8-11 (October 2000) has been used as reference.

CDCV850 Output Compliance to HSTL Specification

After comparing the CDCV850 device output specification with the HSTL output requirement, it has been determined that an attenuation factor of 1.4 ensures the CDCV850 output to be fully compliant with HSTL output specifications. In addition, the output signal must be ac-coupled to shift the common mode voltage to Vref of the HSTL input buffer (typically 750 mV). The drawings below show a complete interface circuit to provide signal attenuation and level shifting.

Two cases are shown, one for signal termination at the line end and another for serial transmission line termination. The termination of the signal at the HSTL input stage is the better approach to assure minimal signal reflections and best possible jitter performance. However, if the application demands serial termination because board space is limited at the HSTL input buffer, drawing (c) shows a solution to the problem. The transmitter side is impedance matched to 50 Ω and ensures proper line termination.

CDCV850 Input

The CDCV850 provides internal ac-coupling of the inputs. Therefore, the CDCV850 can handle a wide range of differential input signals as LVDS, LVPECL, or SSTL2. In addition, the user can drive the CDCV850 by a single ended signal like 2.5-V LVCMOS. In this case, it is recommended to tie the second input directly to GND when using the CDCV850 in PLL mode or tie it to Vcc/2 when used in buffered mode (AVDD=GND).

Calculations and Support

For the calculations of how these resistor values have been derived please contact the TI clock distribution team (f-alicke@ti.com or kalmustafa@ti.com). Also, there are additional clock drivers from TI available to support HSTL signaling levels. If your HSTL clock input is only single ended, TI can provide further assistance.

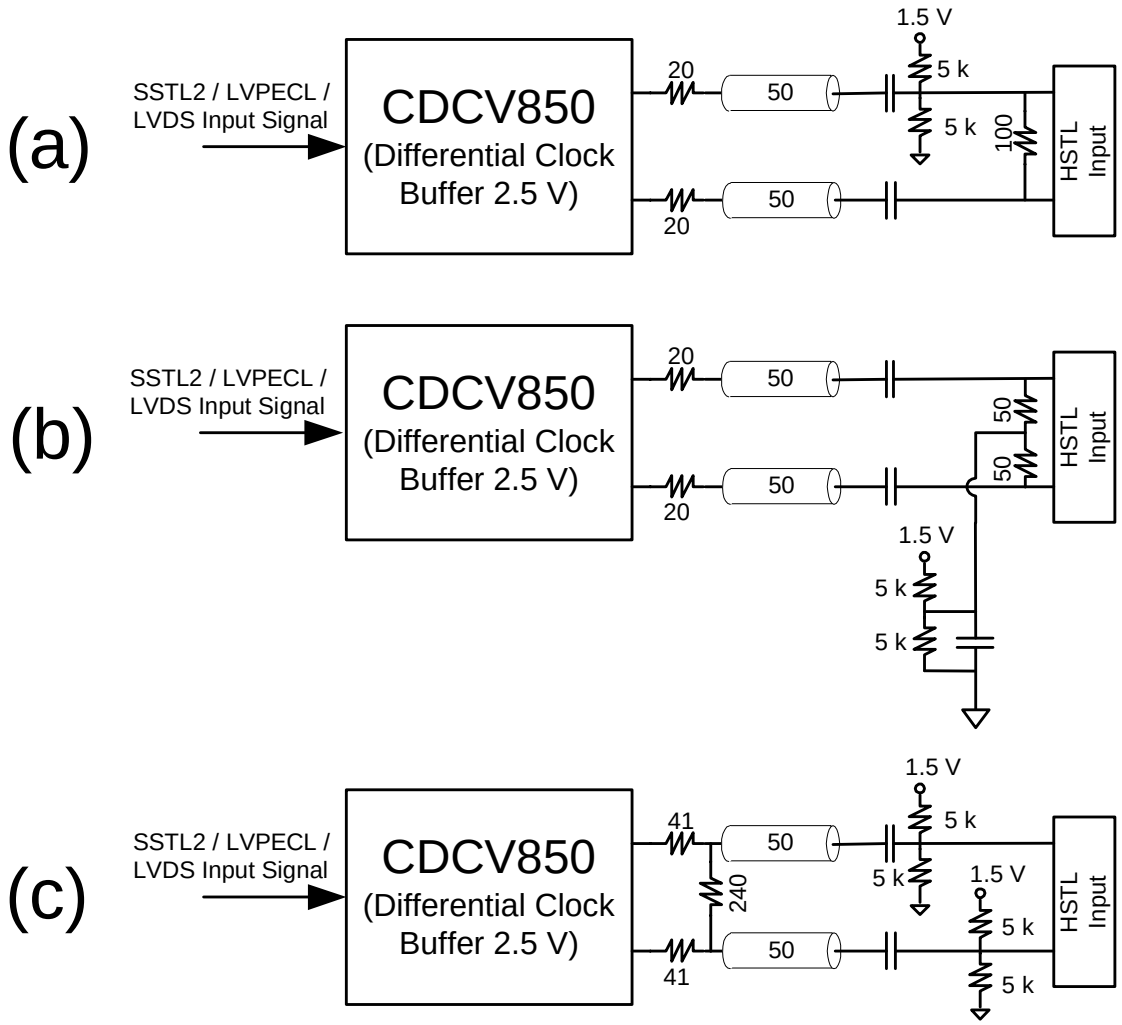

Figure (a): HSTL signal generation with line termination at the receiver; the transmitter stage has a combined output impedance of ~65 Ω (45R+20R)

Figure (b): Same as Figure (a) but with an improved receiver termination network to properly terminate any odd-mode noise (noise that couples into only one transmission line or transmitter differential signal mismatch)

Figure (c): HSTL signal generation with serial transmission line termination; combined output impedance is matched to 50 Ω (45+41||120)

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