Migrating from TMS320VC549 to TMS320VC5410

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC549 to the TMS320VC5410. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets and/or the *TMS320C54x DSP CPU and Peripherals, Reference Set, Volume 1* (SPRU131).

Migration issues from the ’VC549 to ’VC5410 are indicated with the following symbols, which are included at the beginning of each section:

[S] means software modification is required.

[H] means hardware modification is required.

[D] means the ’VC549 and ’VC5410 are different (usually due to added features on the ’VC5410) but no modification is necessary for migration (that is, the devices are different but compatible).

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1 Package and Pinout Compatibility [D]

The ’VC5410 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 176-pin GGW ball grid array MicroStar BGA™

The PGE package is pin compatible (same footprint and pinout) with the ’VC549.

2 Power Supply

The ’VC5410 operates from the same power supply requirements as the ’VC549. CVdd is operated at 2.5 V and DVdd is operated at 3.3 V.

3 Software Wait State Generator [D]

3.1 Wait State Generation

The ’VC549 is capable of generating up to seven wait states. The ’VC5410 is capable of generating up to 14 software wait states. This is achieved with the software wait state multiplier (SWSM) bit which, when set to 1, multiplies the programmed number of software wait states by two.

The location and field definitions of the software wait state register (SWWSR) are identical on the ’VC549 and ’VC5410.

The SWSM bit is located in the software wait state control register (SWCR) at address 0x2B in data space. The structure of this register is shown below.

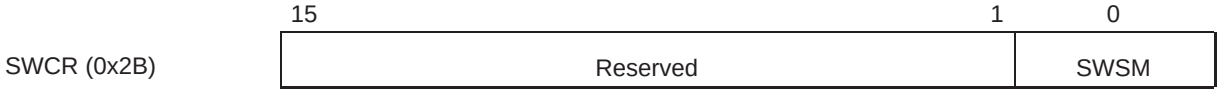

Figure 1. SWCR

SWSM multiplies the number of software wait state set in the SWWSR by 2. Therefore, the ’VC5410 can be programmed to generate 0, 1, 2, 3, 4, 5, 6, 7,8,10,12 or 14 wait states.

The SWSM bit is cleared at reset. Consequently, the wait state generation scheme on the ’VC5410 is fully compatible with the ’VC549.

4 Bank Switching Control Register Differences [S]

The Bank Switching Control Registers (BSCR) on the ’VC549 and ’VC5410 are different. The BSCRs for both devices are shown below.

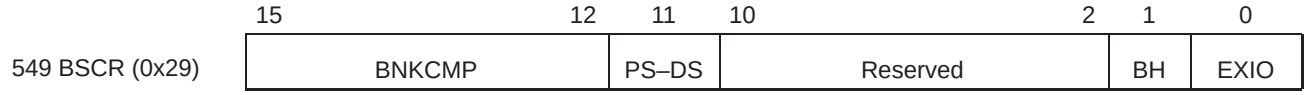

Figure 2. ’VC549 BSCR

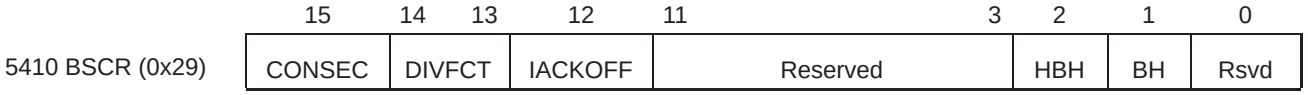

Figure 3. ’VC5410 BSCR

Due to the differences between the two versions of the BSCR, software modification is necessary.

The BNKCMP and PS-DS fields of the ’VC549 BSCR are replaced functionally with the CONSEC field of the ’VC5410 BSCR. The ’VC5410 has a different external parallel interface from that of the ’VC549. The signals are identical but the operation of the signals is different. All external accesses (memory read, memory write, I/O read and I/O write) have a leading and trailing cycle when CONSEC = 1. If CONSEC = 0, consecutive memory reads are single cycle with only a leading cycle before the entire sequence and a trailing cycle after the entire sequence. Accesses other than memory reads are not affected by the state of CONSEC.

New fields in the ’VC5410 BSCR:

DIVFCT	controls the ability to divide down the CLKOUT by 1,2,3 or 4
IACKOFF	enables or disables the IACK pin
HBH	enables or disables the HPI8 data bus holders

The EXIO field and function in the ’VC549 BSCR no longer exists in the ’VC5410.

On the ’VC5410, the bank size is always 32K. An additional bank switching cycle is added when the following conditions occur:

- A memory read followed by another memory read from a different bank.
- A program memory read followed by a data memory read.
- A data memory read followed by a program memory read.
- A program memory read followed by another program memory read from a different page.

5 External Parallel Interface (XIO2) [D]

The signals on the ’VC5410 external parallel interface are identical to those on the ’VC549 and have the same functions.

The timing of these signals is different on the ’VC5410. The ’VC5410 interface inserts additional leading and trailing cycles on external accesses. This is generally not a compatibility issue with the ’VC549 other than fact that the accesses now take a different amount of time than before on the ’VC549.

’VC5410 external access cycle times (for n accesses):

- Memory read (CONSEC = 0) : 2+n cycles
- Memory read (CONSEC = 1) : 3n cycles
- All memory writes: 3n cycles
- All I/O reads : 3n cycles
- All I/O writes : 3n cycles

This difference should be considered if the application to be migrated is highly bandwidth–limited based on the operation of the external parallel interface. Otherwise, the ’VC5410 interface is compatible.

For single–cycle memory reads in consecutive mode, the parameter $\mathbf{t_{a(A)M2}}$ on the ’VC5410 is comparable to the parameter $\mathbf{t_{a(A)M}}$ on the 548/9. This is the parameter upon which the choice of SRAM speed is based.

6 CLKOUT Division [H/S]

As mentioned in the previous section, the DIVFCT field in the BSCR on the ’VC5410 controls whether the CLKOUT represents the CPU clock divided by 1, 2, 3 or 4. Following reset, this value is set to 4. On the ’VC549, CLKOUT always represents the CPU clock.

Since the external parallel interface is timed to CLKOUT (not the CPU clock), the interface will operate slower than on the ’VC549. To make the CLKOUT and the external interface operate at the equivalent speed to that of the ’VC549, the DIVFCT field should be set to 00b (divide–by–1).

7 PLL Clocking Options

The PLL programming and operation on the ’VC5410 are identical to that of the ’VC549. The CLKMD1/2/3 = 1/1/1 option is still reserved on the ’VC5410 (similar to the ’VC549).

8 Multichannel Buffered Serial Port (McBSP) [H/S]

On the ’VC5410, the McBSP replaces all of the serial ports available on the ’VC549.

8.1 Register Subaddressing [S]

The entire set of control registers for the McBSP is different from that for the previous serial ports. This change was necessary to accommodate the highly programmable capability of the McBSP. Most of the control registers on the McBSP are now accessed through register subaddressing. Only the data receive registers (DRR1 and DRR2) and the data transmit registers (DXR1 and DXR2) are directly accessed (not subaddressed).

DRR1 on each McBSP is still mapped to the same location as the ’VC549 DRRs.

DXR1 on each McBSP is still mapped to the same location as the ’VC549 DXRs.

Due to register subaddressing, software modification is necessary to configure the McBSPs properly. Software references to DRR and DXR still work correctly as long as the word length used on the McBSP is 16 bits or less (because DRR2 and DXR2 are only used for word lengths greater than 16 bits).

8.2 McBSP External Interface [D]

The external signals associated with the McBSP (BCLKX, BCLKR, BFSX, BFSR, BDX, BDR) are the same as those on the previous ’C54x serial ports. CLKS is an additional reference clock on the McBSP. The McBSP can also be programmed to ignore CLKS.

There is no hardware migration issue associated with these signals unless the use of CLKS is desired on the migrated design. The CLKS signal is not available on the PGE package of the ’VC5410.

8.3 Triple Buffered Receive Path [D]

The receive path on the McBSP is now triple buffered compared to the double buffered paths of the previous ’C54x serial ports.

- ’VC549 receive path: Receive shift register (RSR) $\rightarrow$ Data receive register (DRR)
- ’VC5410 receive path: (RSR) $\rightarrow$ Receive buffer register (RBR) $\rightarrow$ (DRR)

This structural change manifests itself in two ways:

- The time delay between the data being shifted in and the data becoming available in the DRR is different. This difference has no impact on applications that either use the receive interrupt or poll the RRDY flag to determine when data is ready.
- The McBSP receiver can receive an additional word (compared to the ’VC549 serial ports) before overflow occurs. The RFULL flag is now triggered when DRR and RBR are full and DRR is not read before the end of the third word being shifted into RSR.

These differences generally do not affect the operation of most applications.

8.4 TDM Port to McBSP Migration [H/S]

The ’VC5410 has no dedicated TDM serial port. The McBSP can be programmed to perform a multi–channel function similar to the TDM port but it is not identical. The McBSP cannot generate a signal comparable to the TADD signal on the TDM port. Consequently, both hardware and software changes are necessary to migrate the ’VC549 TDM port function to the ’VC5410 McBSP.

8.5 Buffered Serial Port (BSP) to McBSP Migration [S]

The ’VC5410 McBSP has replaced the ’VC549 BSP. The data buffering function provided by the BSP autobuffering unit is now accomplished by using the DMA in conjunction with the McBSP. The McBSP performs the serial port function and the DMA controller performs the autobuffering function. Software modifications are required to configure the McBSP and the DMA to operate in this manner. Since autobuffering is accomplished through the DMA, the McBSP data can be buffered anywhere in the DMA memory map and is no longer limited to a 2K block of words as on the BSP.

No hardware changes are necessary to transition from the BSP to the McBSP because the set of externals signals associated with the two ports is the same.

9 ’VC549 HPI to ’VC5410 HPI8 Migration

9.1 Expanded Memory Map [S]

The enhanced 8–bit host port interface (HPI8) on the ’VC5410 is very similar to the standard HPI with the exception that the HPI8 is not limited to a 2K block of internal memory. The HPI8 uses the DMA controller to gain access to the entire on–chip memory, eliminating the 2K limitation.

The HPI8 can access the ’VC5410 on–chip memory on program page 1 by setting the XHPIA field in the HPIC to one. The XHPIA field is not present on the ’VC549. The XHPIA is not initialized at reset, so it is the responsibility of the host to set this field appropriately. For this reason, some host software modification may be required to utilize the expanded HPI8 memory map on the ’VC5410.

The external signals associated with the HPI8 are identical to those on the standard HPI so no hardware modification is necessary.

9.2 HPI8 Does not Support Host-only Mode (HOM) [S]

The HPI8 no longer supports HOM. The SMODE bit in the HPIC should be set to 1 (SAM). This bit position is reserved on the ’VC5410.

Data can still be loaded via the HPI8 during reset, but HOM is not available during normal operation.

10 Memory Map [D]

The memory map of the ’VC5410 is similar to the ’VC549 with the following exceptions:

- 32K of additional on-chip SARAM is mapped into addresses 0018000h – 001FFFFh in program space (designated SARAM2 in the data sheet).
- Setting the DROM bit maps SARAM2 into data space instead of mapping the ROM into data space as on the ’VC549.

11 Bootloader/ROM Contents [D]

The bootloader options available on the ’VC5410 are similar but not identical to those on the ’VC549.

- **HPI8 boot**. The ’VC5410 bootloader supports the same HPI boot function as the ’VC549 with the exception that the entry point is set to 2000h instead of 1000h to align it with the start of SARAM1.
- **Parallel boot**. The ’VC5410 bootloader supports the same parallel boot mode as the ’VC549 with the following exception. On the ’VC549, when the location of the boot table is read from I/O address 0FFFFh, the bootloader uses the least significant six bits of the word read as the

most significant six bits of the boot table address with the lower bits forced to zeroes. On the ’VC5410, the word read from I/O space is used without modification as the address of the boot table.

- **Serial boot**. The ’VC5410 bootloader supports serial boot through the McBSPs. McBSP0 is dedicated to 16–bit data loads and McBSP2 is dedicated to 8–bit data loads. McBSP1 is reserved for addition of a future serial boot mode. TDM boot mode is not supported on the ’VC5410. The McBSPs are configured to boot in the manner of the standard ’C54x serial port.
- **I/O boot**. The ’VC5410 support for this mode is identical to the ’VC549.

The ’VC5410 standard ROM contents other than the bootloader are the same as the ’VC549.

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