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MACROMODELS FOR RF OP AMPS ARE A POWERFUL DESIGN TOOL

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Simulation is a particularly effective way to design and test high-frequency circuits. Increasingly powerful computers and the wide use of the circuit simulator, PSpice®, make simulation with PSpice a practical method to test the various parameters of a circuit. Good simulation models are essential, however, to achieve realistic results. Burr-Brown now offers PSpice models for a number of new RF circuits that far exceed the usual simulation standards in scope and details. The macromodel for the Diamond Transistor OPA660 gives an example of the structure and performance of these new PSpice models.

A prerequisite for PSpice simulation is an exact model of the internal structure of the component. These models are usually called macromodels and have differing levels of complexity. A type of simulation using transistors to reproduce the real performance of an analog circuit with a reasonable simulation time offers a good deal of accuracy and has become the "industry standard". Many models, however, fall far short of this standard; they are so simplified that they can not come close to predicting the exact performance of a circuit. A number of mathematical models, for example, are able to reproduce the exact gain-phase relation ratio of an op amp, while providing only poor simulation of the amplifier's noise and distortion. Thus such models are often insufficient for an engineer's need.

In contrast, the model for the OPA660, which is made up of transistors, out performs even the industry standard. PSpice models are also available for the high-speed components BUF600/1, MPC100, OPA622, and OPA623, each with the same structure as that for the OPA660. Each model contains a simplified simulation option (S) and a comfortable option (C) on a 5-1/4" disk (or 3-1/2" disk upon request). These simulation versions, which differ in their simulation accuracy and required simulation times, deliver enough flexibility and accuracy to analyze a large number of circuit characteristics, while remaining simple enough to ensure fast simulations.

THE DIAMOND TRANSISTOR OPA660

Analog circuit technology often uses integrated circuits such as op amps to solve a circuit problem. Because they require feedback, op amps generally fall behind open-loop amplifiers in processing steep input pulses. Open-loop amplifiers, however, do not always provide the required DC accuracy and are susceptible to aging effects and temperature variation. The OPA660 unites the advantages of both methods. This operational transconductance amplifier contains the Diamond Transistor (DT) and Diamond Buffer (DB) in an 8-pin SO or DIL package together with the biasing circuitry (BC). With these independent macroelements, the OPA660 can be used in circuits designed to process high-frequency signals of up to 500MHz. Figure 1 shows a block diagram of the OPA660, while Figure 2 shows a more detailed circuit diagram. The numbering of the inner and outer connection pins shown in the figures matches that used in the macromodel.

The Diamond Transistor is a voltage-controlled, wide-band current source, which functions as an ideal transistor. It contains a high-impedance input (base), a low-impedance input/output (emitter), and a high-impedance current source output (collector). In contrast to a bipolar transistor, this amplifier allows operation over all four quadrants. All of its pins are at 0V with no input signal; all working points are fixed and stable over temperature; the emitter circuit functions in inverting mode and the base circuit in noninverting mode; the transconductance, hence the ratio between output current variation and input current variation, is extremely constant over the entire input voltage range and can be programmed by an external resistor.

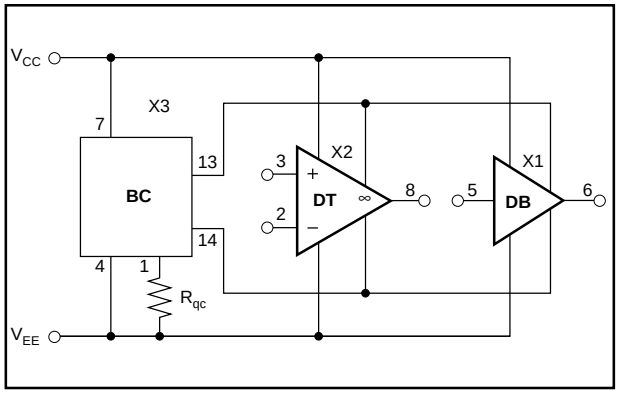

FIGURE 1. Block Diagram of the OPA660.

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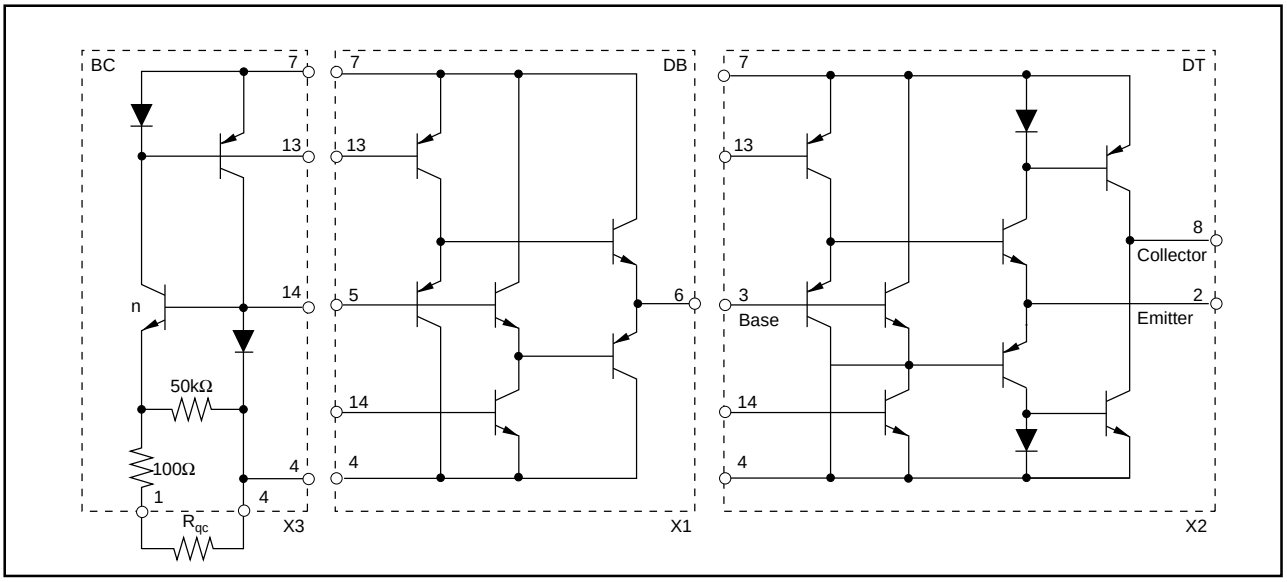

FIGURE 2. Schematic of the Macros X_1, X_2, and X_3.

As can be seen in Figure 2, the DB is an abridged version of the DT. This two-stage, complementary emitter follower is the ideal complement to the DT. It decouples nonloadable, high-impedance circuit points with no loss in bandwidth and prevents feedback from the output to the signal processing. The low-impedance voltage output can drive a cable, a low-impedance input resistance, or a feedback network.

Table I lists the most important parameters of the Diamond Transistor as given in the data sheet.

PARAMETERS OF THE DIAMOND TRANSISTOR

PARAMETERS	UNIT (typ.)
DT Transconductance	125mA/V
Offset Voltage	+7mV
Offset Drift	50µV/°C
Input Bias Current	–2.1µA
Output Bias Current	±10µA
Input Impedance	1MΩ || 2.1pF
Output Impedance	25kΩ || 4.2pF
Differential Gain	0.06%
Differential Phase	0.02°
Quiescent Current	1mA to 20mA

TABLE I. Specifications of the Diamond Transistor.

"C" AND "S" MODELS

All of these parameters can be easily tested by installing the two models and starting the simulations, whose results are automatically displayed on the screen. As already mentioned, the PSpice OPA660 disk contains two subdirectories with one macromodel each. Subdirectory COPA660 contains the more comfortable model labeled C, which delivers very accurate results within a reasonable simulation time. This version is particularly useful in optimizing the function of individual circuit blocks. Subdirectory SOPA660 contains the simpler model labeled S. Up to certain parameter limits, this model delivers simulation results corresponding to actual component values, while requiring less computer storage and shorter simulation times. The S model is especially practical in simulating function chains. The structure and commands and most of the simulation parameters of the two models are identical.

INSTALLING THE MODEL DISK

The first step is to enter the directory in which your PSpice program is installed and make subdirectories COPA660 and SOPA660. Then copy the contents from each subdirectory on the disk into the corresponding subdirectories in your PSpice® program. Now the choice is yours whether to work with the more precise, slightly more time-consuming COPA660 model or the simplified SOPA660 model. The following discussion will deal only with the COPA660 version, since its structure and commands are identical to those of the S model. After entering the directory, it is possible either to create CIR files of your own circuit designs or to start one of the example simulations. The command 'RUN CDRDF2", for example, starts the simulation of the DC sweep response (CDR) of the direct-feedback amplifier (DF2). The commands are the same in both models except for the first letter—"C" for comfortable and "S" for simple.

The command "SG" for show graphics lets the user display the results of already executed simulations (e.g. SG CARDB). With the command "PAR", it is possible to display up to nine simulation results at the same time.

MACROMODEL STRUCTURE

An essential part of any macromodel is the macromodel CIR file, which describes the connections between the individual components that make up the macromodel and often also contains descriptions of the transistors used and information

about the ambient temperature. The user can define the macromodel as a subcircuit (SUBCKT) and integrate it into the main test or applications circuit. Varying the type of signal excitation and analysis enables a large number of simulations. The models presented here, however, go a step further. They are part of a shell, so that it is not necessary for users to generate a circuit file for each simulation. In addition to the macromodels and test circuits for the OPA660 function blocks Diamond Transistor and Diamond Buffer, the disk also contains a whole row of completely dimensioned application circuits. Table II lists these applications, while Table III gives the simulation parameters for the Diamond Transistor with that start commands for the S and C models. The start commands are made up of abbreviations for the model version, the simulation parameter, and the application circuit. Thus the command CARDF2 for the C model (C) starts the AC sweep response (AR) for the OPA660 as a noninverting direct-feedback amplifier (DF2). For simulations with the S model, simply change the "C" at the beginning to an "S" after switching to subdirectory SOPA660. Since all applications are designed for a gain of +2, the user can compare the various versions directly. It is easy to change an application circuit or the dimensions of a particular component using the text editor, which displays the CIR file the user is currently working on. By changing components or adding new ones, the user can produce a new customized circuit. PSpice can also integrate the CIR file for the OPA660 (S/C OPA660.CIR) into their own applications by defining it as a subcircuit and copying it into the appropriate directory.

APPLICATION	FILE
Diamond Buffer	DB
Diamond Transistor	DT
Diamond Transistor	DT1
Forward Amplifier	FA1
Forward Amplifier	FA2
Forward Amplifier	FA3
Forward Amplifier	FA4
Direct-Feedback Buffer	DF1
Direct-Feedback Amplifier	DF2
Direct-Feedback Amplifier	DF3
Current-Feedback Amplifier	CF1
Voltage-Feedback Amplifier	VF1

TABLE II. OPA660 Application Circuits.

DIAMOND TRANSISTOR	RUN COMMAND C MODEL	RUN COMMAND S MODEL
DC Transfer Function	CDTDT	SDTDT
Voltage Graphic Analysis	CFG0DT	SVG0DT
DC Sweep Response	CDRDT	SDRDT
AC Sweep Response	CARDT	SARDT
Transient Sine Response	CTX1DT	STX1DT
Transient Ramp Response	CRX2DT	SRX2DT
Gaussian Response	CGX2DT	SGX2DT
Buffer Output Impedance	CBIDT	SBIDT
Transconductance Impedance	CTIDT	STIDT
Open-Loop Gain	COGDT	SOGDT
Noise Analysis	CNADT	SNADT
Supply Rejection	CSPDT	SSPDT
Enable Transient Analysis	CETDT	SETDT
Common-Mode Gain	CCGDT	SCGDT

TABLE III. Simulation Examples for DB and DT.

MACROMODEL COPA660

Figure 3 shows the comfortable macromodel for the OPA660. It consists of the subcircuits DT, DB, and BC. BC, the biasing circuit, supplies current to the transistor stages in the DT and DB via nodes 13 and 14. Figure 4 shows the CIR file. The circuit diagrams show the nodes of the CIR file, which describe the links between the macromodel components.

AN APPLICATION EXAMPLE: ANALYZING THE DIRECT-FEEDBACK AMPLIFIER CONFIGURATION WITH PSPICE

To demonstrate how practical it can be to simulate circuits with PSpice, the next section examines the RF amplifier from Figure 5, which illustrates the simulation of the DC sweep response. This amplifier has direct feedback from the collector to the emitter. In the noninverting version shown in the figure, the Diamond Transistor is controlled from the base (Pin 3). The resistors R_{f8} and R_2 provide feedback and adjust the voltage gain. In a real circuit, the feedback loop from the collector (Pin 8) to the emitter (Pin 2) must be very short with low stray capacitance to allow the construction of stable, wide-band amplifiers. DB decouples the relatively high-impedance collector output and provides the necessary drive power for low-impedance load resistors. The capacitor C_2, parallel to R_2, raises the gain at 250MHz and above, and compensates the falling frequency response that would otherwise arise from internal and external parasitic capacitances.

SIMULATION RESULTS

Figure 6 presents the simulation results in graphic form. The output voltage is shown divided by 2 on the x-axis to put it into relation to the input voltage at gain 2. The values for the differential gain error can also be seen in Figure 6. Figure 7 illustrates the circuit diagram for the frequency response analysis (CARDF2). As in all other simulated applications, the amplifier operates here with a quiescent current (I_Q) of ±20mA, which can be reprogrammed to other values if necessary. The generator sweep range is 10MHz to 3GHz. As shown in Figure 8, the Direct-Feedback Amplifier, DF2, achieves a –3dB bandwidth of 586MHz at the collector output and 571MHz at the low-impedance buffer output.

Of all pulse forms, Gauss-shaped pulses require the smallest bandwidth at given rise and fall times. As interesting and easy-to-use as frequency responses and rectangular pulses are, they are not the product of natural sources (such as sensors) but rather of special measuring devices. Users generally want to know to what extent real existing amplifier pulses are transmitted (rising and falling edges, overshooting, etc.) Figure 9 shows the simulation circuit for Gauss pulse transmission (CG22DF2). The rise and fall times of the input pulse are 2ns each, and the pulse repetition is 50MHz.

As can be seen in Figure 10, the DF2 transmits these Gauss-shaped pulses with no visible pulse distortion or overshoot-

ing. Interestingly, the quality of the pulse transmission is dependent upon the ratio between the Gauss pulse rise time and the delay time of the feedback amplifier structures. The delay time of the DF2 is 594ps without the subsequent amplifier, which is not located in the amplifier feedback loop. Usable pulse responses result when the rise time of the input pulse is at least four times the delay time.

Finally, to keep the simulations rooted in reality, we recommend testing the simulations in practice with the demo board DEM-OPA660-3GC (Figure 11). This demo board contains the DF2 circuit dimensioned for 2V/V. According to the OPA660 data sheet, the –3dB bandwidth is 552MHz at ±1.4V, and the pulse responses shown at a 2ns slew rate impressively confirm the simulation.

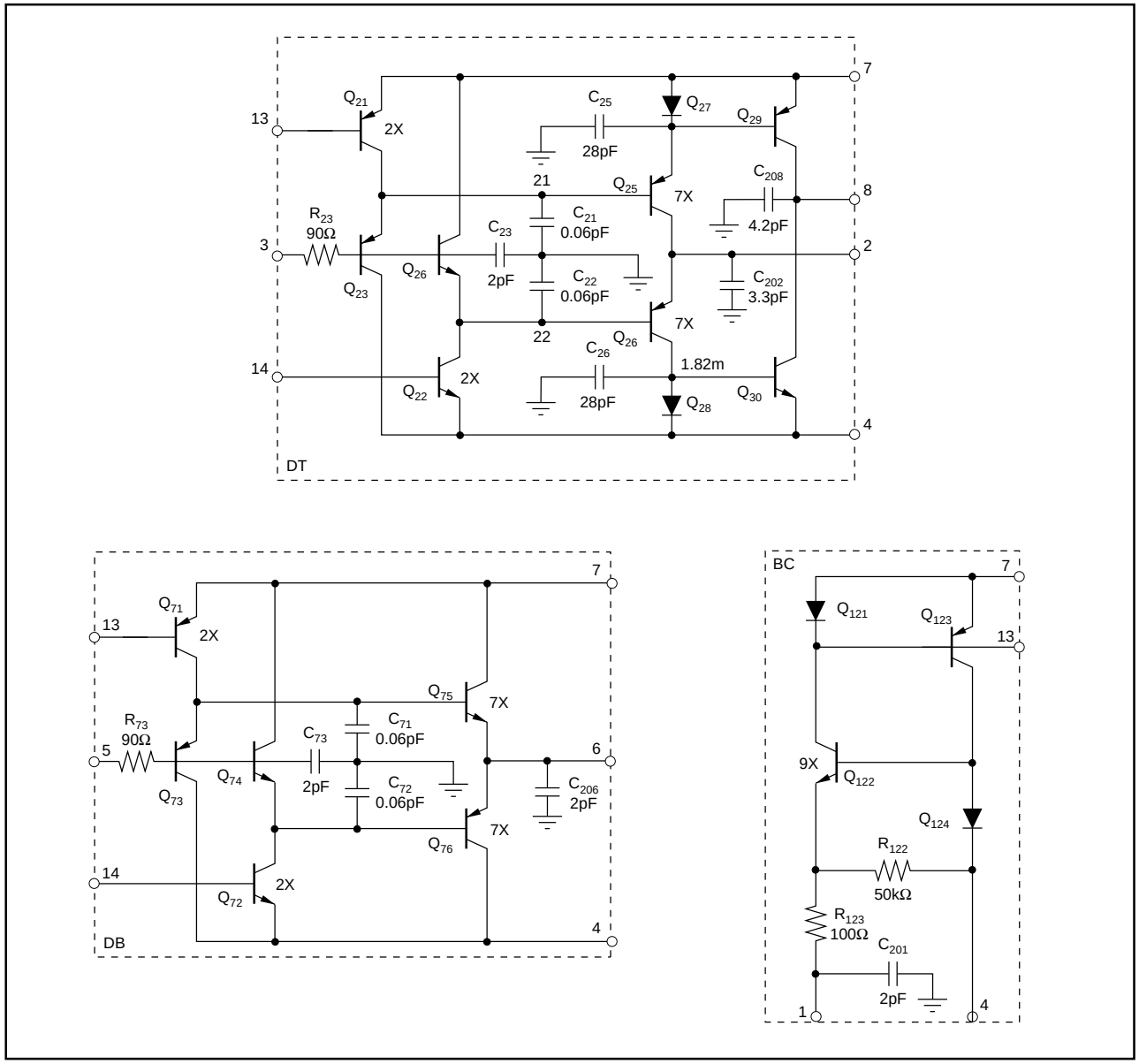

FIGURE 3. OPA660 Macromodel Consisting of the Subcircuits DT, DB, and BC.

```
*+Inc file circuit                 :  COPA660.CIR
*****************************************************************************************************************
   X1 4    5    6    7    13   14        CDB660;   Diamond Buffer DB
   X2 2    3    4    7    8    13   14   CDT660;   Diamond Transistor DT
   X3 1    4    7    13   14             CBC660;   Biasing Circuit BC
**
 C201     1    0    2pF
 C202     2    0    2pF
 C203     3    0    2pF
 C205     5    0    2pF
 C206     6    0    2pF
 C208     8    0    2pF
*****************************************************************************************************************
 **Diamond Buffer CDB660
**
 .SUBCKT CDB660 4 5 6 7 13 14
**
 R77 77 5 25
**
 Q71 74   13   7    7    PI   2.8
 Q72 73   14   4    4    NI   2.8
 Q73 73   73   7    7    PIJ  18
 Q74 74   74   4    4    NIJ  18
 Q75 79   73   7    7    PIJ  18
 Q76 80   74   4    4    NIJ  18
 Q77 74   77   79   7    PIJ
 Q78 73   77   80   4    NIJ
 Q79 79   79   78   4    NIJ  6
 Q80 80   80   78   7    PIJ  6
 Q81 7    79   6    4    NIJ  18
 Q82 4    80   6    7    PIJ  18
**
 .ENDS CDB660
*****************************************************************************************************************
**Diamond Transistor CDT660
**
 .SUBCKT CDT660 2 3 4 7 8 13 14
**
 R27 27   3    25
 R33 33   7    50
 R34 34   4    50
 R35 35   7    50
 R36 36   4    50
**
 C38 2    0    2.2pF
**
 Q21 24   13   7    7    PI   2.8
 Q22 23   14   4    4    NI   2.8
 Q23 23   23   7    7    PIJ  18
 Q24 24   24   4    4    NIJ  18
 Q25 29   23   7    7    PIJ  18
 Q26 30   24   4    4    NIJ  18
 Q27 24   27   29   7    PIJ
 Q28 23   27   30   4    NIJ
 Q29 29   29   28   4    NIJ  6
 Q30 30   30   28   7    PIJ  6
 Q31 31   29   2    4    NIJ  18
 Q32 32   30   2    7    PIJ  18
 Q33 31   31   33   7    PIJ  18
 Q34 32   32   34   4    NIJ  18
 Q35 8    31   35   7    PIJ  18
 Q36 8    32   36   4    NIJ  18
**
 .ENDS CDT660
```

FIGURE 4. CIR File COPA660.CIR

```
*****************************************************************************************************************
**Biasing Circuit CBC660
**
 .SUBCKT CBC660 1 4 7 13 14
**
 R122     122  4    50k
 R123     122  1    100
**
 C121     121  0    10pF
 C124     124  0    10pF
**
 *I121    121  124  0.1µA
**
 E13      13   0    121  0    1
 E14      14   0    124  0    1
**
 Q121     121  121  7    7    PI
 Q122     121  124  122  4    NI   27
 Q123     124  121  7    7    PI
 Q124     124  124  4    4    NI
 Q125     4    13   7    7    PI   32
**
 .ENDS CBC660
*****************************************************************************************************************
 **Model COPA660
**
 .SUBCKT COPA660 1 2 3 4 5 6 7 8
**
   X1     4    5    6    7    13   14        CDB660; Diamond Buffer DB
   X2     2    3    4    7    8    13   14   CDT660; Diamond Transistor DT
   X3     1    4    7    13   14             CBC660; Biasing Circuit BC
**
 C201     1    0    2pF
 C202     2    0    2pF
 C203     3    0    2pF
 C205     5    0    2pF
 C206     6    0    2pF
 C208     8    0    2pF
**
 .ENDS COPA660
*****************************************************************************************************************
 .NODESET V(13)=+4.2632  V(14)=+4.2637
*****************************************************************************************************************
**End
```

FIGURE 4. CIR File COPA660.CIR (cont.)

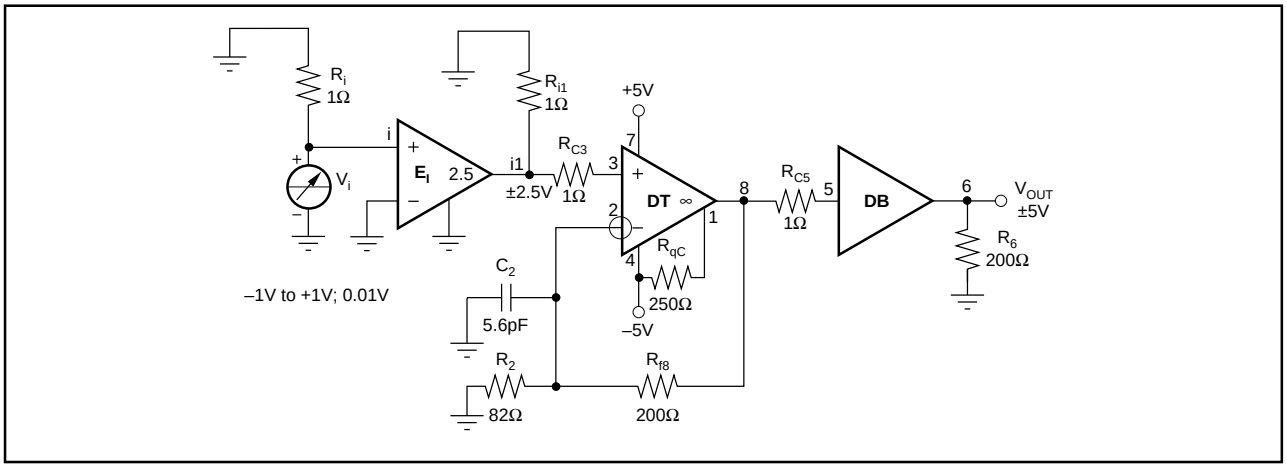

FIGURE 5. DC Sweep Response CDRDF2 of the Direct-Feedback Amplifier.

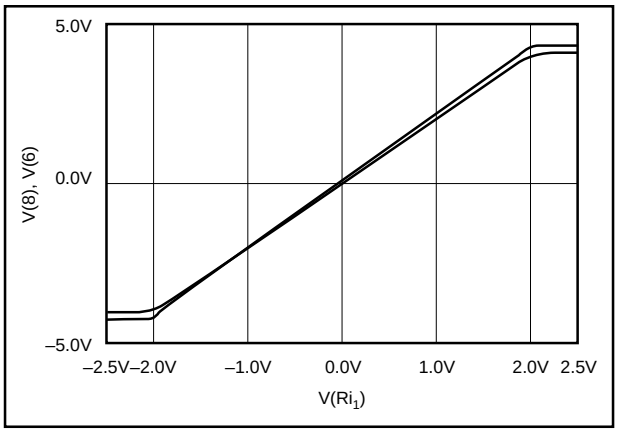

FIGURE 6. Simulation Results of the DC Sweep Response CDRDF2 in Graphic Form.

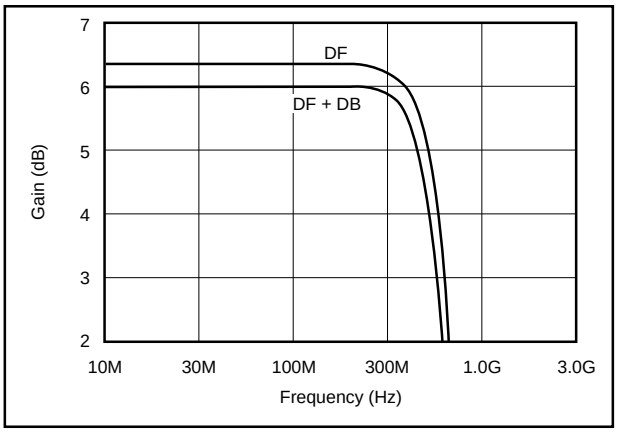

FIGURE 8. Simulation Result of the AC Sweep Response CARDF2.

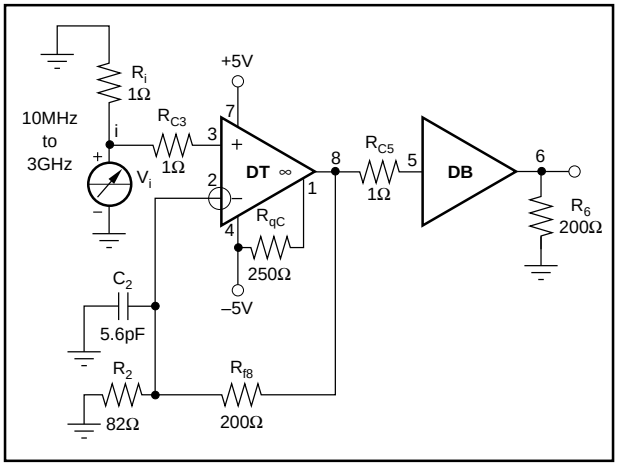

FIGURE 7. Frequency Response Analysis (CARDF2).

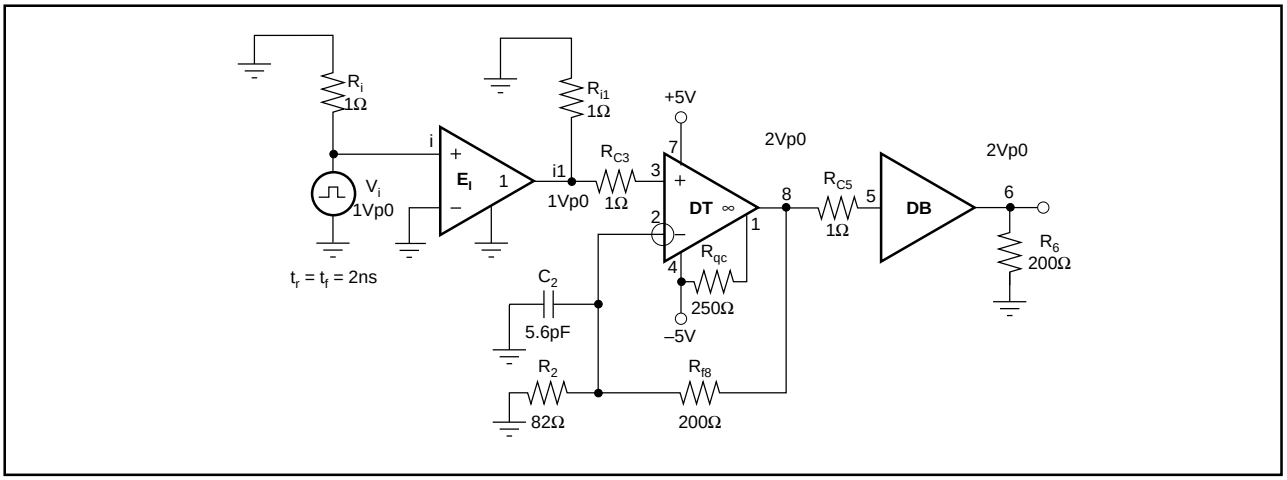

FIGURE 9. Simulation Circuit for Gauss Pulse Transmission (CG22DF2).

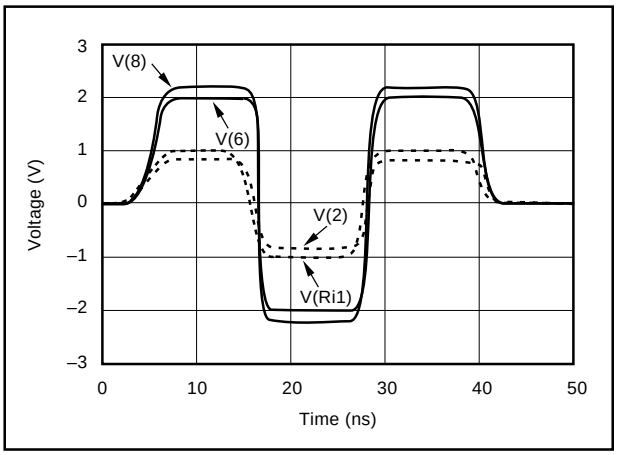

FIGURE 10. Simulation Result for Gauss Pulse Transmission.

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