Reliability Implications of Derating High-Complexity Microcircuits

It's now common practice to upscreen COTS components for use in harsh environment military systems. But while derating ICs in order to make them work outside of the manufacturer's data sheet feels like a safe way to ensure reliability, there are some downsides that system designers should consider.

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As a result of acquisition reform initiatives, OEMs of military systems were authorized to use performance-based specifications for component procurement. At first, the industry was suddenly faced with a dilemma—to continue designing with tried and proven military-grade components or accept the risk of using COTS components in a manner historically considered unacceptable. But since then, there have been volumes of papers authored and presented on the topic of using COTS microcircuits in traditional military environments.

But the trouble is, not all COTS ICs work in all military applications. Besides the issues of plastic package hermeticity and long-term storage, making nonmilitary devices work in wider-than-data-sheet environments has spawned a movement of derating components in order to upscreen them. And with today's state-of-the-art submicron technologies and package configurations, the derating of high-complexity, leading-edge components such as microprocessors and DSPs has become very complex, and there's much more involved in the process than meets the eye (Figure 1).

In a number of applications, such as military ground-based communication systems, the environment might be the same as seen in commercial applications. In these cases COTS plastic-encapsulated microcircuits (PEMS) might be an acceptable choice. They might be used as is with good results—providing that obsolescence issues are addressed. But in other applications, such as missile systems, the use of COTS components often requires the OEM to operate the components outside the component manufacturer's data sheet specifications.

Historically, military OEMs have had established methods of estimating component reliability under various operating conditions. And even though efforts are now underway by multiple OEMs and third-party research organizations to develop "cookbook" methodologies to uprate or upscreen COTS components, the design margins for state-of-the-art devices that military OEMs once understood and came to rely on are no longer always valid. Even worse, reliability may suffer if the proper derating assumptions aren't applied. Education, knowledge, testing and questioning assumptions are critical steps to consider when derating components.

OEM and IC Manufacturer's Product Liability Concerns

Manufacturers of military systems and components might, in certain cases, be shielded from product liability issues by the system of government-approved military specifications. If design, procurement,

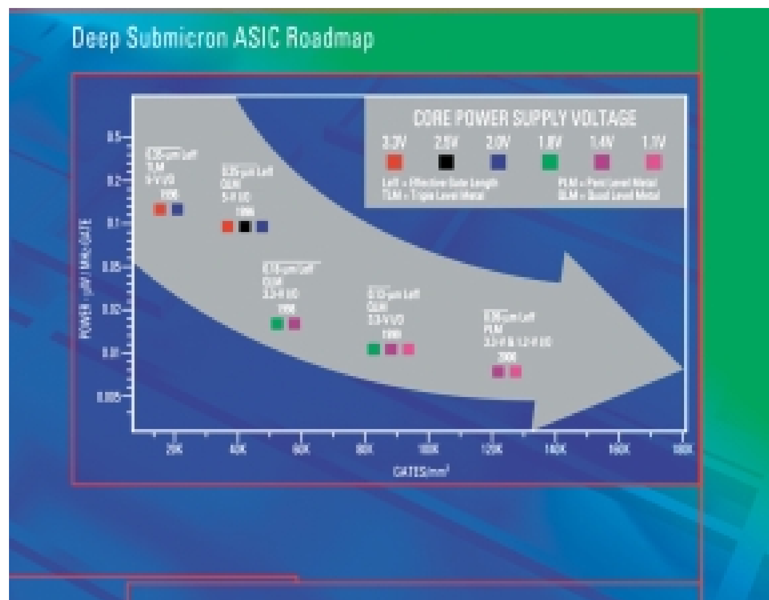

Figure 1

Technology advancements are changing and challenging the uprating paradigm.

manufacturing and qualification are performed in accordance with these specifications, the government, not the manufacturer, accepts the risk. But if the OEM elects to use nonmilitary components, then that OEM could assume the product liability risks. This liability could also extend to the component manufacturer supporting the use of nonmilitary-grade devices in these applications.

Therefore, a large number of major semiconductor manufacturers have elected to shield themselves from this potential liability. These companies typically have disclaimers similar to that published by Texas Instruments (TI):

Plastic encapsulated TI semiconductor devices are not designed and are not warranted to be suitable for use in some military applications and/or military environments. Use of plastic encapsulated TI semiconductor devices in military applications and/or military environments in lieu of hermetically sealed ceramic devices is understood to be fully at the risk of the Buyer.

In some cases, semiconductor suppliers have elected to further shield themselves by not selling commercial components directly to military OEMs. In addition, these suppliers are specifically not providing any information to military OEMs that might be construed as facilitating the use of components outside published specifications. In cases where this information is provided, it's usually accompanied by a disclaimer similar to that used by TI for information released to commercial OEMs:

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IC Reliability in End Applications: External Factors

Operating life, also referred to as Mean Time Between Failures (MTBF), of an IC is affected by multiple factors. The operating environment affects package-related reliability due to factors such as moisture-induced corrosion or thermo-mechanical stress. Materials used in the encapsulation of microcircuits, such as mold compounds, might not be suitable for use at extended temperatures. End users often make the mistake of assuming that life test results alone are sufficient to estimate field reliability.

Overall, most high-complexity microcircuits exhibit aggregate life test failure rates of significantly less than 50 Failures In Time (FIT), or failures per billion device hours, when calculated to a derated operating temperature of 55°C using a 60% confidence level. This would lead the user to assume a very long device life.

However, the conditions found during a life test, such as constant high temperature, low or no ambient humidity and continuous device operation, don't address humidity-induced failure mechanisms or temperature cycling-induced failure mechanisms that are found in non-benign environments. These are addressed by Highly Accelerated Stress Testing (HAST) or Biased Humidity Testing (85°C/85% RH), Autoclave and Temperature Cycling/Thermal Shock. Therefore, life test data must be supplemented with other environmental test data to determine the functionality of a plastic-encapsulated device in a given environment.

To further complicate matters, the life test itself is typically performed at 125°C/1,000-hour equivalent under nominal operating conditions rather than worst-case recommended operating conditions. Results of the life test are therefore more representative of typical device use with environmental conditions excluded and not continuous operation at maximum conditions. For purposes of this discussion, "maximum recommended operating conditions" is the term used to define the parameters for a given device under which that device is warranted to operate. "Absolute maximum ratings" are the conditions to which a device can be exposed for a short period without damage. Typically,

Package	Mold Compound	Chemistry	Intermetallic Life in Years					Activation Energy
			150°C	140°C	135°C	115°C	105°C	
PQFP	A	Multifunction	>7.1	>25	>190	>783	>352	1.90 eV
TQFP	B C D	Biphenyl Biphenyl Biphenyl	0.3 0.4 0.6	0.5 0.8 1.2	1.7 2.5 3.7	4.1 5.6 8	9.5 12.7 18.4	1.12 eV 1.04 eV 1.04 eV
PBGA	E	Multifunction	5.2	16.5	104	407	1426	1.74 eV

Table 1

Au/Al intermetallic life vs. package encapsulant. Mold compound A exhibits the longest life at all temperatures. The activation energy shown was used to calculate the compound longevities.

the continued use of a device at absolute maximum ratings damages the device.

Package Materials Considerations

One item often overlooked when attempting to uprate or upscreen PEMs is the physical properties of the encapsulation (or mold compound) material itself. The type of encapsulant used is dictated by multiple factors. These include the flow properties during the mold process, cure characteristics, thermomechanical stress of the die, high-temperature performance and moisture performance. Trade-offs must be considered since a single encapsulant can't meet all requirements. In some cases, a mold compound is selected for optimal performance, and only the commercial or industrial temperature ranges are considered.

Encapsulants consist of multiple components including resins, fillers, flame retardants and mold-release agents. The flame retardants are of particular interest with respect to device reliability. Brominated epoxies release bromine when heated. Bromine has the effect of accelerating intermetallic formation between the gold bond wires and the aluminum die bond pads (Kirkendall voiding or "purple plague"). TI performed a study of Au/Al intermetallic life vs. various package encapsulants used for high pin count packages. The results are shown in Table 1.

As can be seen in the Table, encapsulant chemistry has a very direct affect on component life. While all these encapsulants yield acceptable performance over the commercial temperature range, some exhibit a very high failure rate when exposed to higher temperatures. Some encapsulants have a glass transition temperature (TG) well under 125°C. Exposure to temperatures in excess of the specified glass transition temperature accelerates the release of bromine that in turn accelerates intermetallic formation. Note that in actual operation, the junction temperature of the die must be considered in addition to the ambient or case temperature because the encapsulant is in contact with the die surface.

IC Die-Level Failure Mechanisms

If the environmental failure mechanisms are ignored, then the discussion can focus on microcircuit die wear-out mechanisms. Assuming no extrinsic reliability defects, the failure mechanisms are typically gate oxide wear-out and metal line electromigration. The actual MTBF varies among device families and sometimes from one device type to another in the same family. This is due to both the technology/process node, defined in part by feature size, oxide thickness and core-operating voltage; the actual design of the device, including current density; and the wafer fabrication process. Failures due to wear-out might or might not be catastrophic with respect to the application.

In cases involving oxide wear-out, the failure is relatively sudden as the oxide breaks down. But for electromigration, the device might fail suddenly if a metal line opens. More typically, however, the failure is due to resistance increases in contacts or vias, and the device might exhibit a more gradual failure. In this case the internal circuitry of the device subjected to worse case stress would fail to source or sink enough current to maintain internal device AC timing.

This mechanism could exhibit itself as an intermittent problem in the system due to timing glitches as the device timing slowly degrades until the device no longer meets the AC timing required to operate in the system. It's important to note that current generations of leading-edge components such as DSPs have much tighter timing requirements than past generations. Therefore, these devices are much more susceptible to internal timing degradation or arbitrary derating of AC parameters.

IC Die-Level Design for Reliability

IC manufacturers design devices in accordance with a formal set of design rules. The computer verifies these design rules at numerous points during die design, layout and photomask generation. While the specifics of these design rules are a trade secret, some generalities are applicable to any manufacturer.

A design model is developed for a specific technology node, whereas a device reliability model is developed that's driven by predetermined reliability goals. These goals are typically set to meet the expectations of the commercial-end customers. This model defines a specific set of maximum design conditions required to meet the reliability goals. The various components of the model, such as gate oxide wear-out or electromigration factors, are determined empirically.

A reliability model for electromigration, for example, would be developed for a specific metal system. The model would specify a maximum current density at a given junction temperature in the various metal lines, vias and contacts. Adherence to the model results in an acceptable wear-out failure rate over the life of the product. The model would be used in conjunction with other models to establish limits for the layout of the device with respect to current density. As previously stated, the actual factors used in these models are determined based on the technology node and are typically proprietary.

If the device is designed well inside the model limits, then the overall product life might reasonably be expected to meet or exceed the model when derated for use beyond the IC manufacturer's recommended operating conditions. If the design is near the limits of the model, then the device would be expected to only meet worst-case model reliability when used within the manufacturer's recommended operating conditions. An example of such a design would be in which the device is designed with the smallest geometry possible to maximize speed. Arbitrary derating of such a device results in extreme operating life degradation.

Example Calculations for Electromigration Current Density Reliability

For the purposes of creating an example, assume an electromigration reliability goal of less than a 0.5% or 1.0% cumulative failures during 10 power-on-years at a maximum junction temperature of 105°C. A maximum current density specification, J_D is established for the metal system in question. For this example, a maximum current density of 5.0 x 10^5 A/cm^2 is used. To simplify calculations, only DC current density in metal lines will be considered.

Substituting empirically derived values for the variables of interest generates the failure rate data shown in Table 2.

For the example shown, a 30°C increase of junction temperature results in a drastic reduction of product life. For a design typical of low-complexity mature products with much more margin, the same increase in temperature might not be an issue.

Real-World IC Die-Level Reliability

In actual applications, the silicon life expectancy of a device is affected by a number of conditions. DC power, AC power,

Current density is calculated from the following equation:

$$J_D = J_S \bullet \left[\frac{t_{50} \bullet e^{\left[\frac{E_A}{k} \bullet \left[\frac{1}{T_D} - \frac{1}{T_S}\right]\right]}}{t_{pl} \bullet e^{(-Z_p \bullet \sigma)}} \right]^{\frac{1}{N}}$$

Where:

- J_D = Design Current Density (A/cm^2)
- J_S = Stress Current Density (A/cm^2)
- T_D = Junction Temperature (°K)
- T_S = Stress Temperature (°K)
- t_{pl} = Product Lifetime (Hours)
- t_{50} = Median Time To Fail (MTF) (Hours)
- Σ = Log-normal Shape Parm
- k = Boltzman's Constant eV/°K
- E_A = Activation Energy (eV)
- N = Exponent in MTF Equation
- Z_p = -2.23 for 1.0%
- Z_p = -2.58 for 0.5%

The MTF, t_{50}, has been observed to fit the following empirical calculation:

$$t_{50} = K \bullet J^{-N} e^{\left[\frac{E_A}{k \bullet T}\right]}$$

Where:

- K = Proportional Constant
- J = Current Density
- T = Stress Temperature
- E_A = Activation Energy
- k = Boltzman's Constant

duty cycle and junction temperature come into effect. Use of the device above or below data sheet recommended operating conditions affects the MTBF. The Arrhenius Model is often used for thermal derating calculations and the McPherson and/or Berkley Models for gate oxide derating out calculations. But neither method is accurate for derating complex devices without a thorough understanding of the device design and process node. The fact that a device functions at temperatures above those specified in the manufacturer's data sheet doesn't mean that the device functions reliably.

For example, operating a typical high-complexity IC such as a microprocessor or DSP at lower speeds at a given temperature will decrease power consumption thereby reducing electromigration. Due to the complexity of these types of devices, very detailed information regarding the device design is needed to establish the derating factors. For example, reducing the operating frequency or power consumption doesn't significantly affect gate oxide wear-out since this mechanism is related to gate-oxide thickness and the field potential across the oxide.

As previously noted, however, most IC manufacturers don't release design details or derating factors so that it's not possible for the end user to determine reliable operating conditions accurately outside of data sheet limits or to calculate expected MTBF under reduced operating conditions. If the application has frequent power-up and power-down cycles, tertiary effects such as cumulative damage by supply line transients must also be considered.

Ensuring microcircuit component reliability is a multifaceted discipline that requires involvement of diverse technologists. Factors affecting leading-edge component reliability extend well beyond the tried and proven approaches used by military OEMs in the past. Proper derating of a highly complex device is beyond the scope of most end users since the semiconductor manufacturers deem the needed information as a trade secret.

Junction Temperature °C	Current Density A/cm^2	Failure Rate in Years	
		50 FIT 0.5% fail	100 FIT 1.0% fail
85	5.0×10^5	47.0	50.0
95	5.0×10^5	21.3	22.6
105	5.0×10^5	10.0	10.7
115	5.0×10^5	4.9	5.2
125	5.0×10^5	2.5	2.7
135	5.0×10^5	1.3	1.4
145	5.0×10^5	0.7	0.8
85	2.0×10^5	293.5	312.3
95	2.0×10^5	132.8	141.3
105	2.0×10^5	62.7	66.7
115	2.0×10^5	30.8	32.7
125	2.0×10^5	15.6	16.6
135	2.0×10^5	8.2	8.7
145	2.0×10^5	4.5	4.7

Table 2

Device reliability vs. operating conditions. A lower FIT rate is desired.

If a user elects to operate a device beyond the device manufacturer's data sheet conditions, product reliability will be degraded, possibly to the point in which end-system reliability no longer meets acceptable limits. Furthermore, depending on the failure mechanisms involved, system operation might become erratic because of the gradual deterioration of a component prior to total loss of functionality.

Due to the multiple variations in field operating conditions, a component manufacturer can only base estimates of product life on models and the results of package and die level qualification. The end users must evaluate their application of the device and determine if a candidate device is suitable for use in that application. End users are advised to operate devices within the manufacturer's data sheet recommended operating conditions and select a device designed for the end-system environment. ▌▌

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