Analog Engineer's Circuit

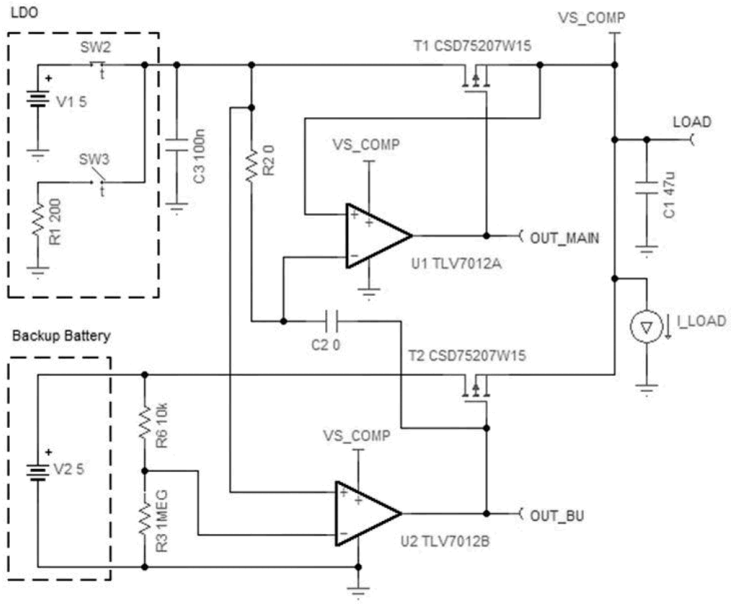
ORing MOSFET Controller with Comparator Circuit

Design Goals

LDO Output			Supply Voltages		Resistors		
R_1	C_1	C_3	V_1	V_2	R_2	R_3	R_6
200 Ω	47 µF	100 nF	5 V	5 V	1 kΩ	1 MΩ	10 kΩ

Design Description

Comparators can be used in an ORing configuration to choose between different sources. With a relatively simple circuit and smart switches, the comparator can be used to always maintain a supply voltage to the load. For low voltage applications, comparators have a better edge over diodes because there is no voltage drop. This circuit is designed for a system connected to a wall outlet with an incorporated backup battery. If the main power is ever cut, then the back up battery will supply power to the load to ensure the device is always on. The switch network on the left side of the circuit is used to model the LDO output.

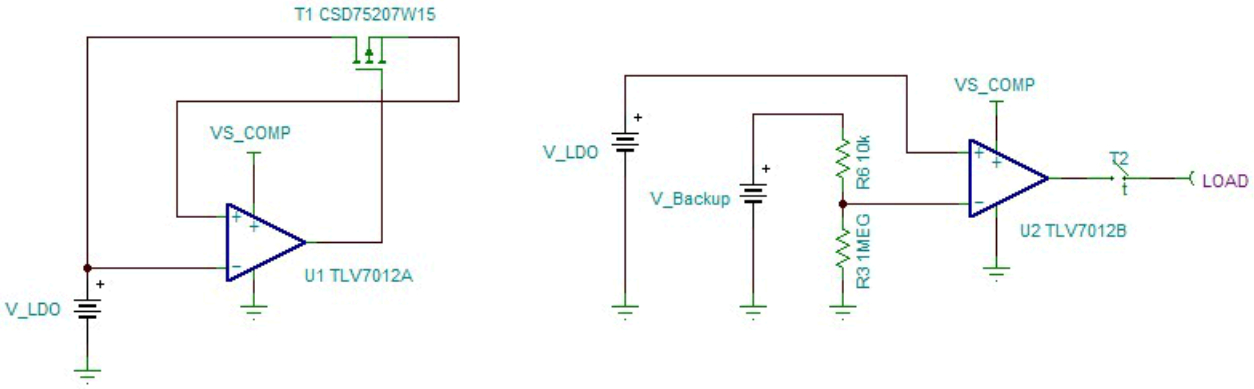


Design Notes

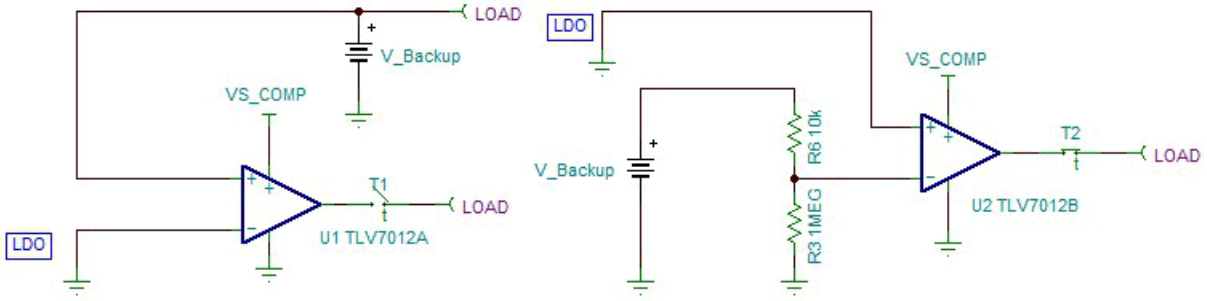
1. Use a push-pull comparator that has rail-to-rail input range.
2. Use a dual PMOS with common source configuration such as CSD75207W15.
3. Ensure the V_{th} of the PMOS is lower than the voltage at the output of the comparator.
4. Follow the data sheet recommendations for power filtering and stability at the output of the LDO for C_1 and C_3.
5. Use the LDO data sheet to determine the R1 value. It may be specified as the resistor used to connect the output to GND in the case of an undervoltage event.

Design Steps

1. The box highlighting R1, V1, and SW3 are used to model the LDO output behavior. R1 signifies the impedance of the LDO which can be found in the data sheet. V1 is the LDO output voltage, so set V1 accordingly. SW3 is used for modeling the case when the LDO suddenly loses power and the output will be pulled to ground through R1. It is also used for modeling the case when the LDO is powered back up and supplying a voltage. C3 is added to the circuit because it is the typically recommended capacitor value to help with loop stability that should be right next to the output. Set this value according to the LDO data sheet recommendations. C1 is added at the load because the larger capacitor value does not need to be right at the LDO output node. Set this value according to the LDO data sheet recommendations.
2. During the initialization of the circuit, as the comparator powers on, the current will flow through the body diodes of T1 to supply power to the load. Current will stop flowing through the diode when the drop across the diode is less than approximately 0.7 V. Then, the comparator will output low and turn on the PMOS switch.
3. Under normal or typical conditions, the LDO is used as the main power supply. In the following image, there is a simplified circuit model to explain the function of U1 and U2. The (-) node sees the LDO voltage, and the (+) node sees the source node of T1. The comparator output will stay low because the (+) node is slightly smaller than the drain node from the $R_{DS(on)}$ drop of T1. Since the comparator pulls the gate low, T1 will act like a closed switch, allowing the LDO to power the load.
   During this time, U2 will be controlling T2, making it act like an open switch. The box highlighting V2 models the back up battery. V2 is the back up battery voltage, so set V2 accordingly. R3 and R6 form a voltage divider, so that the (-) node sees a 0.99 × V2. When the LDO is on and providing power, if the back up battery and the LDO are at the same potential, T2 must act like an open switch to prevent both sources from being loaded. The (-) node sees a divided down voltage of V2 and the (+) node sees the LDO voltage. To make sure that the comparator output is high so that T2 is turned off, then the (-) node < (+) node.



4. When the LDO loses power, the back up battery is connected to the load so that there is always a constant source of power. In the following image, there is a simplified circuit model to explain the function of U1 and U2. Now that the LDO output is pulled to low, the (+) node of U2 sees ground and the (-) node of U2 sees a divided down version of the back up battery. This will force the comparator output low and close the switch so that the back up battery can source to the load. During this time, U1 will be disconnected from the load. In the following image, there is a simplified circuit model to explain the function of U1. The (-) node sees ground since the LDO output is pulled low, and the (+) node sees the back up battery. The comparator output will transition high and turn off T1 so it acts like an open switch.



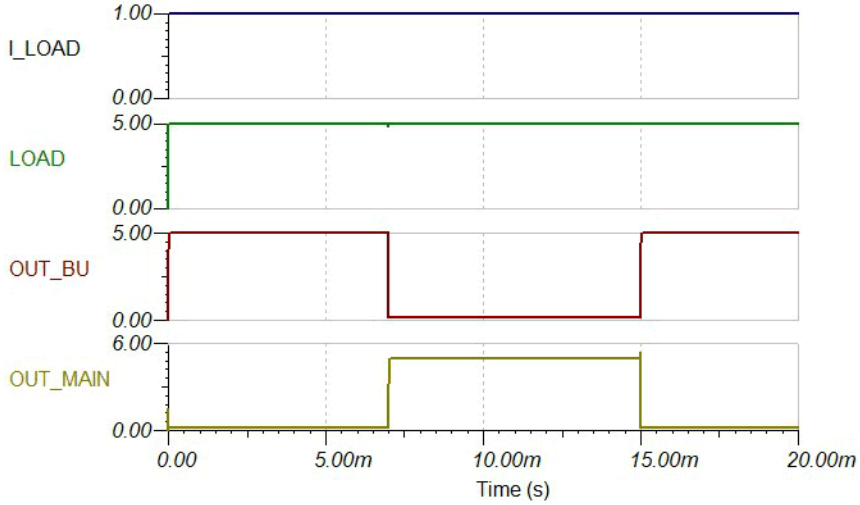
5. Set the voltage divider created by R_3 and R_6 for a ratio of 1%. Set the ratio for 1% so that U2 can quickly switch once the LDO loses power. During normal operation, OUT_BU will stay high because the inverting input will be 1% less than inverting input. When the main supply loses power, OUT_BU will go high because the non-inverting input is connected to the output of the LDO.
   The R_{total} (R_3 + R_6) should be such that the current through the divider is at least 100 times higher than the input bias current (I_{bias}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

$$\frac{R_3}{R_3 + R_6} = 1\,\%$$

6. Now looking at the details, R2 and C2 functionality is described. R2 is used here to isolate the LDO output from the (-) node of U1. When the LDO loses power, SW3 closes and pulls the LDO output to GND. If R2 is shorted, then T1 always stays on because there is contention between both sides of C2. As the LDO output tries to sink to ground, the output of U2 is also transitioning low. Because there is some delay to the LDO output, the (-) node of U1 will struggle and the node will oscillate around the load voltage. Setting R2 to 1 kΩ is sufficient enough to isolate the node. If R2 is too small, there will be wasted power. If R2 is too large, the (-) node of U1 transitions too slowly so that it is not able to switch T1 on. U1 never turns on T1 and the power to the load is supplied through the body diode instead. When the LDO output transitions (either losing power or regaining power), C2 is used to yank the (-) node of U1 so that it is able to transition quickly and turn U1 on or off. Without C2, the delay from the LDO transitioning causes U1 to never switch. Set C2 to the same value as C3.

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File: SBOR017.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range see TI Precision Labs - Op amps.

Design Featured Comparator

TLV7011, TLV7012	
Output Type	PP
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{os}	±.5 mV
V_{HYS}	4.2 mV
I_q	5 µA/Ch
t_{pd}	260 ns
#Channels	1 and 2
TLV7011 Product Page, TLV7012 Product Page	

Design Alternate Comparator

TLV1805	
Output Type	PP
V_{cc}	3.3 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{HYS}	14 mV
V_{os}	±500 µV
I_q	135 µA
t_{pd}	250 ns
#Channels	1
TLV1805 Product Page	

TLV7031, TLV7032	
Output Type	PP
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{HYS}	7 mv, 10 mV
V_{os}	±1 mV
I_q	335 nA, 315 nA
t_{pd}	3 µs
#Channels	1 and 2
TLV7031 Product Page, TLV7032 Product Page	

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265