Application Report
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Generating Early Clock Using TI's CDCVF2509/CDCVF2510 PLLs

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ABSTRACT

This application brief presents various different methods of achieving certain relationships between the reference clock and the output clock of TI's CDCVF250xx family of zero-delay PLL-based buffers. It focuses on variable trace lengths in the PLL feedback loop in generating early clock. Early clock is defined such that the PLL output phase is advanced in relation to the input reference clock.

1 How to Tune for Zero Delay

There are four methods that are used to adjust phase in PLL-based clock buffers

1. By adjusting the feedback trace length
2. By varying the capacitive load on the feedback pin
3. By varying the capacitive load on the output clock
4. By adjusting the trace on the output clock

This report discusses the first three methods.

The FBOUT (pin 12) and FBIN (pin13) and CLK (pin 24) completes the feedback loop of the PLL. This connection is made external to the PLL and FBIN must be connected to FBOUT. For course tuning, FBIN trace length can be adjusted to advance or delay the Yn outputs relative to the input CLK. Fine tuning in sub-Pico-seconds are best handled by capacitive loading on FBIN, this is method 2 in the following text.

2 PLL Phase Adjustments

In order to have a positive phase error (i.e. CLK leads the Y outputs), the FBIN pin should be loaded more lightly than the Yn outputs. On the other hand if a more negative phase error is desired (i.e. the Yn outputs leading the reference input CLK), the FBIN pin should be loaded more heavily than the Y outputs.

As a rule of thumb, a one pF will induce about 50 to 60ps delay and a trace of one inch is about 3pF parasitic capacitance, which is approximately 150-180ps delay.

Depending on the application and the delay requirements, the designer can advance the Yn outputs by increasing the FBIN trace length, hence generating an early clock. On the other hand; shortening the trace length on the feedback will advance the reference input clock CLK relative to Yn.

It is important to note that the capacitive loading on the feedback is the best way to fine tune the phase error and this loading should be placed as close to the FBIN pin as physically possible. Adjusting the trace length of the feedback loop should do the course tuning of phase error. For instant if a phase lead (CLK lead Yn) is required, then the trace length of the Y outputs should be increased. Conversely increasing the trace length of the feedback path, (FBIN) will decrease the phase error; in this case the Yn outputs will be advanced relative to the reference clock input (CLK).

3 Application Examples

In the following section three examples are presented. The first shows zero-delay while the second and the third show delay adjustment of Yn outputs and CLKIN respectively.

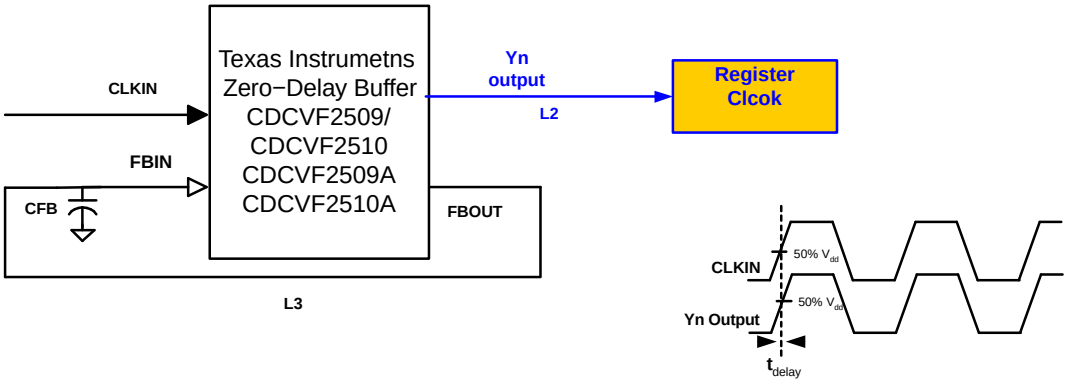

Figure 1. L2=L3, Zero Phase Delay Between CLKIN and Yn

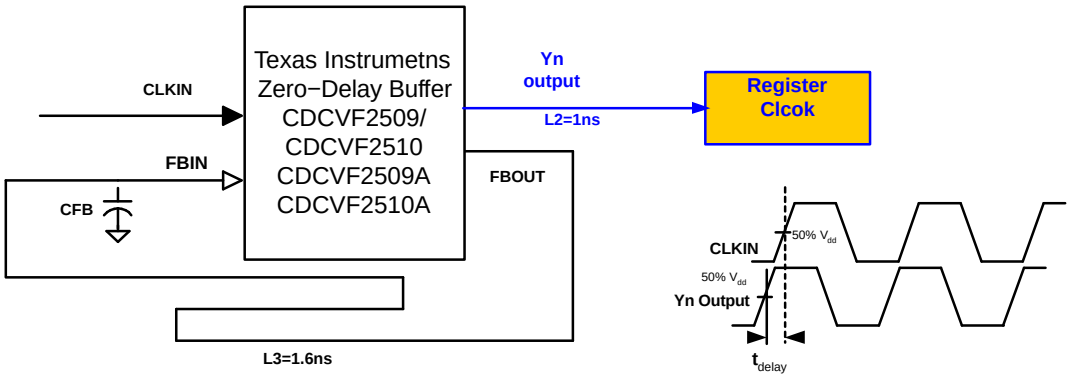

Figure 2. L3 Longer than L2 by 0.5 ns

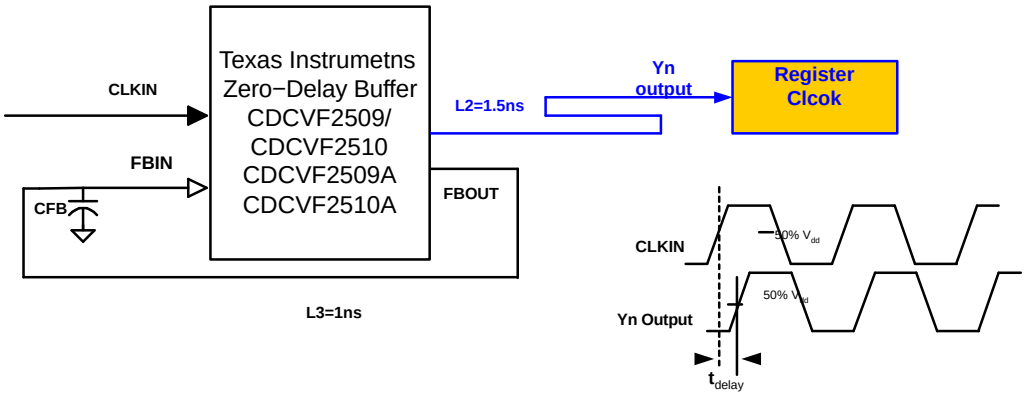

Figure 3. L2 Longer than L3 by 0.5 ns

4 Delay Data for CDC2509/CDCVF2510

The following Excel sheet show various delay measurements with various trace lengths. Also included are adjustments of feedback capacitance CFB as well as Yn load capacitance CL.

Table 1. Delay Data

Delta Feedback Trace Length (inch)	Feedback Trace Width (mil)	Feedback Capacitance (pF)	PLL OUTPUT_CLK Load (pF)	PLL INPUT_CLK Load (pF)	Delta Propagation Delay from PLL_INPUT_Clk to PLL OUTPUT_CLK (ns)	V_{CC}	Base Delay	New Delay
BASE	NA	0	4.7	0	NA	3.3	-1.516	NA
BASE	NA	2.2	4.7	0	-0.144	3.3	-1.516	-1.372
2.9	5	0	4.7	0	-0.732	3.3	-1.516	-0.784
2.9	7	0	4.7	0	-0.721	3.3	-1.516	-0.795
5.9	5	0	4.7	0	-1.221	3.3	-1.516	-0.295
5.9	7	0	4.7	0	-1.226	3.3	-1.516	-0.290
11.9	5	0	4.7	0	-2.424	3.3	-1.516	0.908
23.9	5	0	4.7	0	-4.43	3.3	-1.516	2.914
35.9	5	0	4.7	0	-6.645	3.3	-1.516	5.129
2.9	5	2.2	4.7	0	-0.921	3.3	-1.516	-0.595
5.9	5	2.2	4.7	0	-1.392	3.3	-1.516	-0.124
11.9	5	2.2	4.7	0	-2.565	3.3	-1.516	1.049
23.9	5	2.2	4.7	0	-4621	3.3	-1.516	3.105
35.9	5	2.2	4.7	0	-6.807	3.3	-1.516	5.291
BASE	NA	0	15	0	NA	3.3	-1.925	NA
BASE	NA	2.2	15	0	-0.162	3.3	-1.925	-1.763
2.9	5	0	15	0	-0.747	3.3	-1.925	-1.178
2.9	7	0	15	0	-0.737	3.3	-1.925	-1.188
5.9	5	0	15	0	-1.239	3.3	-1.925	-0.686
11.9	5	0	15	0	-2.43	3.3	-1.925	0.505
23.9	5	0	15	0	-4.445	3.3	-1.925	2.52
2.9	5	2.2	15	0	-0.94	3.3	-1.925	-0.985
5.9	5	2.2	15	0	-1.407	3.3	-1.925	-0.518
11.9	5	2.2	15	0	-2.577	3.3	-1.925	0.652
23.9	5	2.2	15	0	-4.631	3.3	-1.925	2.706
35.9	5	2.2	15	0	-6.812	3.3	-1.925	4.887
BASE	NA	0	25	0	NA	3.3	-2.172	NA
BASE	NA	2.2	25	0	-0.161	3.3	-2.172	-2.011
2.9	5	0	25	0	-0.747	3.3	-2.172	-1.425
2.9	7	0	25	0	-0.736	3.3	-2.172	-1.436
2.9	10	0	25	0	-0.723	3.3	-2.172	-1.449
5.9	5	0	25	0	-1.246	3.3	-2.172	-0.926
11.9	5	0	25	0	-2.431	3.3	-2.172	0.259
23.9	5	0	25	0	-4.444	3.3	-2.172	2.272
BASE	NA	0	25	0	NA	3.0	-2.214	NA
2.9	5	0	25	0	-0.746	3.0	-2.214	-1.468
2.9	7	0	25	0	-0.732	3.0	-2.214	-1.482
BASE	NA	0	25	0	NA	3.6	-2.142	NA
2.9	5	0	25	0	-0.802	3.6	-2.214	-1.412
2.9	7	0	25	0	-0.794	3.6	-2.214	-1.42
2.9	10	0	25	0	-0.787	3.6	-2.214	-1.427

5 Layout Guidelines

- Isolate the power planes of the clock driver from the power plane of the board by a ferrite bead. The ferrite blocks high frequency noise from reaching the main power supply.
- Where possible create a localized ground planes for the clock traces on the PCB board top layer. These localized planes provide a return path for RF current.
- Minimize EMI by avoiding the use of vias to route clock signals, vias add unwanted inductance to the trace and in general reduce the effectiveness of bypass capacitors.
- Keep trace impedance short and balanced to minimize reflections, and ringing.
- Place clock signals far a way from I/O area.
- Load all outputs equally.
- Avoid routing traces near the edge of PCB board.
- Clock traces should not intersect each other, they should be of equal length to minimize clock skew.
- Route clock traces to each load when driving multiple loads and terminate them individually.
- Keep power and ground planes adjacent. This reduces power supply noise.
- Place power supply decoupling capacitors and filter components as close to VCC as possible. For decoupling, it is recommended to use low-inductance, low-ESR (Equivalent Series Resistance) capacitors as they provide best performance.
- Avoid using right angle bends, they increase capacitive loading of a transmission line, which causes unwanted reflection, ringing, overshoot and degrade signal rise-time. use smooth rounded or chamfer traces instead.

6 References

- Johnson, H.W., and Gram, M. “High-Speed Digital Design”. Prentice Hall, 1993
- Application and Design Considerations for the CDC5XX Platform of Phase-Lock Loop Clock Drivers. Texas Instruments CDC Data Book, 1999, SCA028, 1996
- EMI Prevention in Clock-Distribution Circuits, Texas Instruments CDC Data Book, 1999, SCAA031, 1994
- Using CDC2509/2510A PLL with Spread Spectrum Clocking (SSC) Application Note, Texas Instruments CDC Data Book, 1999, Literature Number SCAA039, 1998

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