

# Ethernet Clock Generation Using the CDCM6100x

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ICP - Clock Distribution Circuits

## ABSTRACT

This application report is a guide for using Texas Instruments CDCM6100x in an Ethernet LAN and WAN application as a clock distributor and clock synthesizer along with measured jitter performance results.

## Background

Today's networking boxes require clock generation and buffering. Traditional methods involved a clock oscillator and a clock buffer. For LAN applications, a typical 156.25-MHz clock is needed, and for WAN applications a 155.52-MHz clock is used. Due to the low jitter and accuracy needed for these clock oscillators, their cost are high. So how does a designer lower cost but maintain low jitter, high accuracy, and clock buffering in a single solution? The CDCM6100x answers this question.

## Functional Description

The CDCM6100x is a highly versatile, low-jitter frequency synthesizer which can generate low-jitter clock outputs, selectable among LVPECL, LVDS, or LVCMOS, from a low-frequency crystal or LVCMOS input for a variety of wireline and data communication applications. The CDCM6100x features an on-chip PLL that can be easily configured solely through control pins. The overall output jitter performance is less than 1 ps, rms or 35 ps, pk-pk, thus making the device a perfect choice for use in demanding applications like SONET, Ethernet, Fibre Channel, and SAN. The CDCM6100x is packaged in a small 32-pin, 5-mm × 5-mm QFN package. The CDCM6100x is available in one-, two-, and four- output versions.

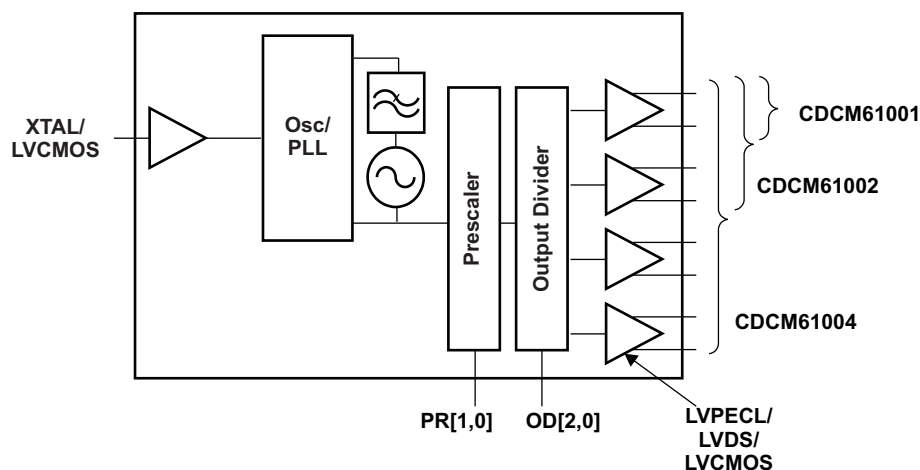


Figure 1. CDCM6100x Functional Block Diagram

## Application

Today's networking LAN and WAN clocking require low jitter (typ < 1ps rms or lower). Typical clock speeds for LAN applications are 625 MHz, 312.5 MHz, 156.25 MHz, and 125 MHz. For WAN applications, 622.08 MHz, 311.04 MHz, 155.52 MHz, and 77.76 MHz are commonly used. For both LAN and WAN systems, the output signal type needed can be differential (LVPECL or LVDS) or single-ended 3.3-V LVCMOS. This application report demonstrates solutions that can meet these needs while also offering a lower cost solution to today's high priced oscillators and clock buffers.

## Test Equipment and Setup

All the measurements discussed in this application report were taken under normal operating conditions using a 3.3-V power supply and at room temperature.

Equipment used:

- Agilent E5052A Signal Source Analyzer
- Power supply
- CDCM6100x EVM

## Block Diagram and Jitter Test Results of LAN Solutions

The following four solutions show how to generate networking LAN clocks from the CDCM6100x devices and a low-cost, standard 25-MHz crystal. The 25 MHz is fed into the CDCM6100x VCO core to generate a 625-MHz, 312.5-MHz, 156.25-MHz, or a 125-MHz frequency available to the output buffer. The output signal type can be native LVPECL, LVDS, or LVCMOS. These examples select LVPECL for the output buffers, but also included are some LVDS and LVCMOS measurements at the end of this applications report.

### LAN Solution 1 Block Diagram:

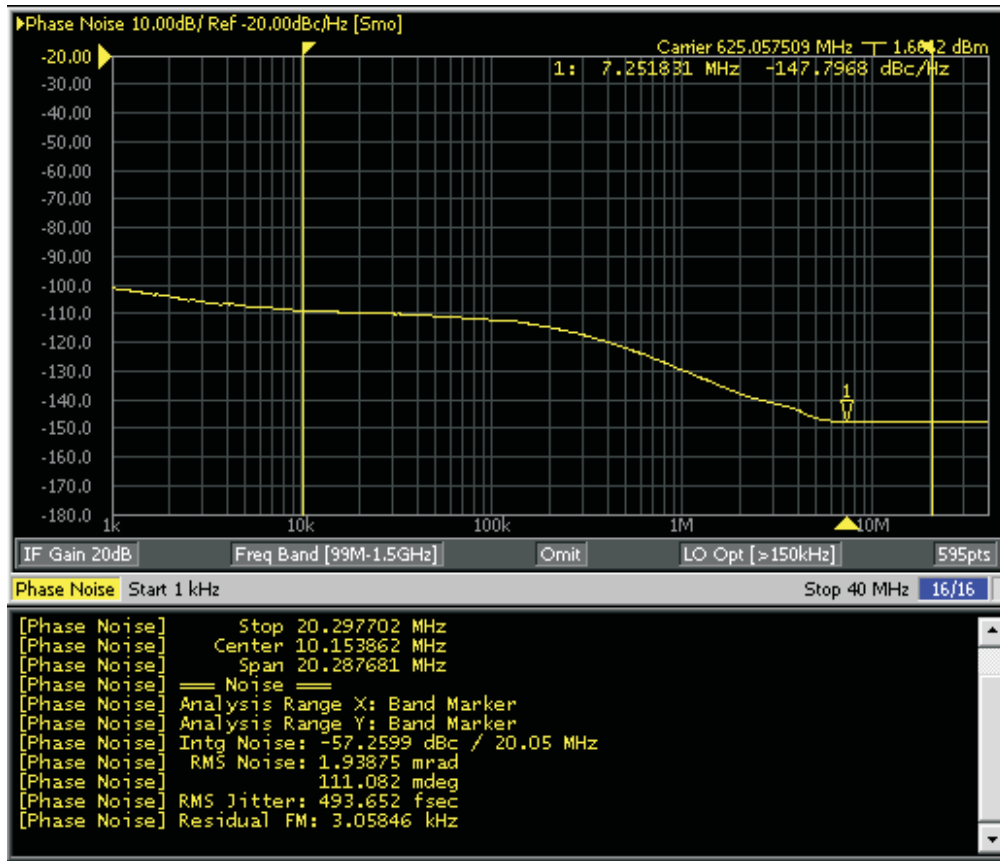
This solution uses the one-output version CDCM61001 to generate 625 MHz. If more outputs are needed, the CDCM61002 and CDCM61004 can supply two or four outputs, respectively.



Figure 2. LAN Block Diagram 1

**LAN Solution 1 Jitter Test Results:**

**OUT\_0 = 625-MHz LVPEL – RMS Jitter is 494 fsec (10 kHz–20 MHz)**



**LAN Solution 2 Block Diagram**

This solution uses the one output version CDCM61001 to generate 312.5 MHz. If more outputs are needed, the CDCM61002 and CDCM61004 can supply two or four outputs, respectively

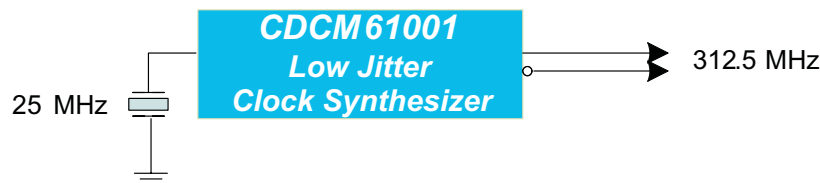
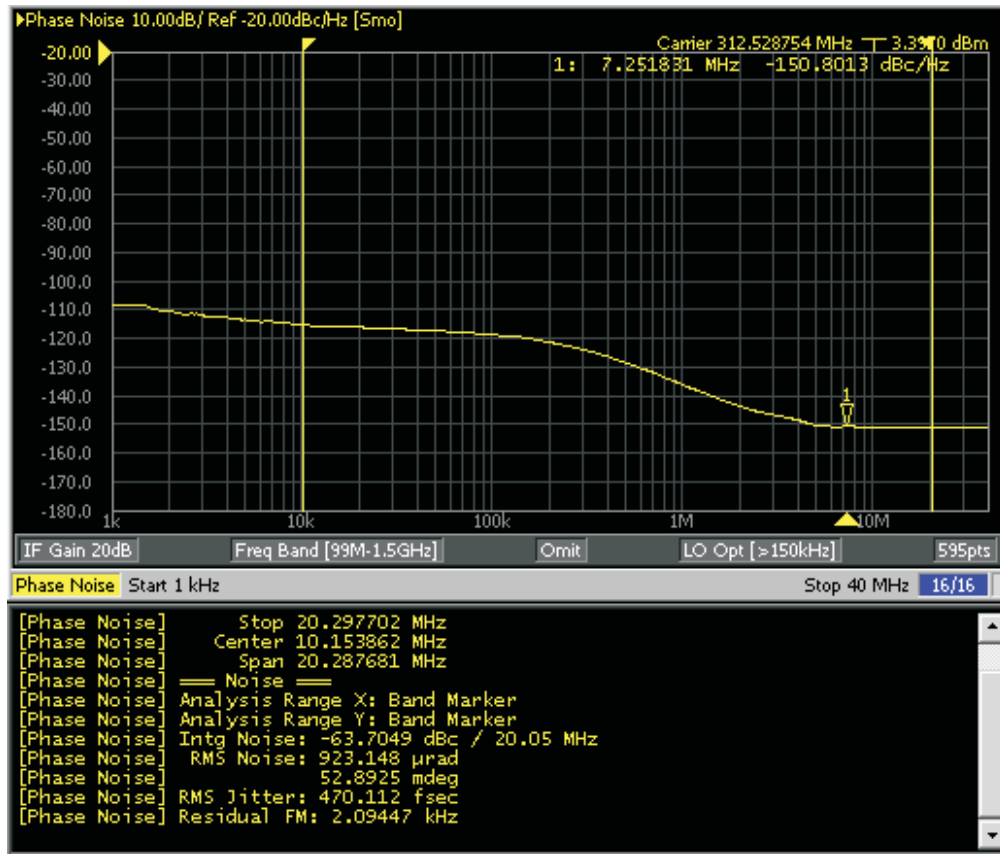


Figure 3. LAN Block Diagram 2

**LAN Solution 2 Jitter Test Results:**

**OUT\_0 = 312.5-MHz LVPEL – RMS Jitter is 470 fsec (10 kHz–20 MHz)**



**LAN Solution 3 Block Diagram:**

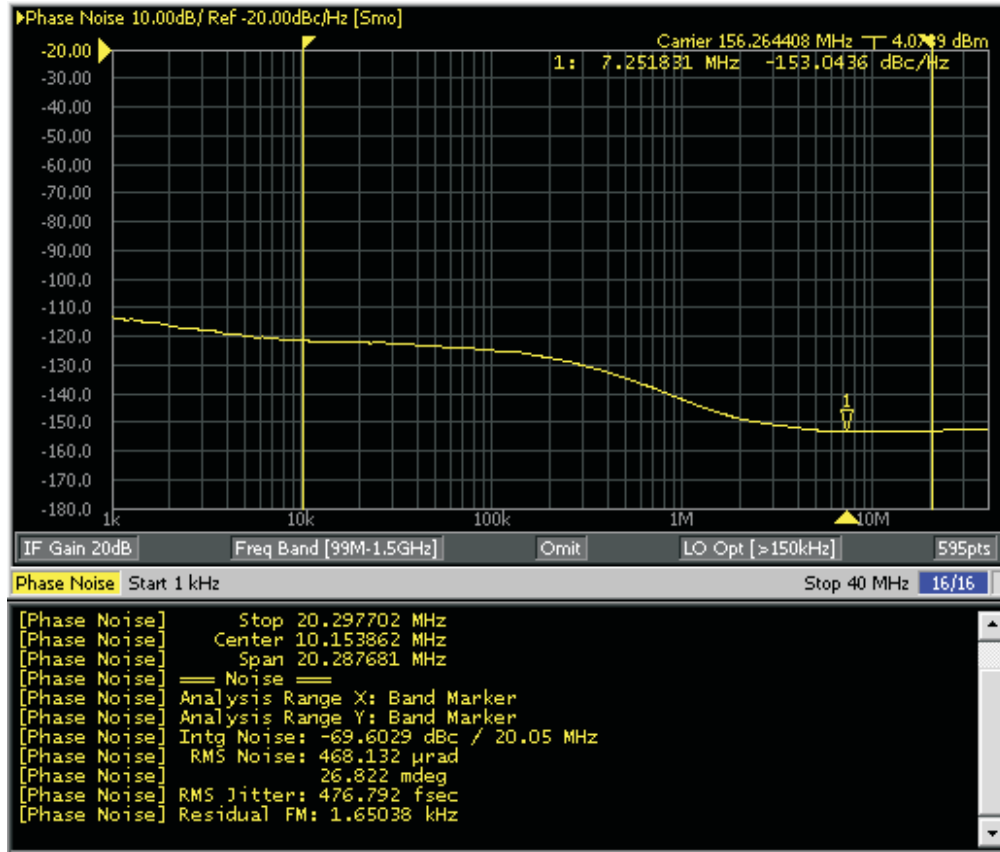
This solution uses the two-output version CDCM61002 to generate two copies of 156.25 MHz. If more or less outputs are needed, the CDCM61001 and CDCM61004 can supply one or four outputs, respectively.



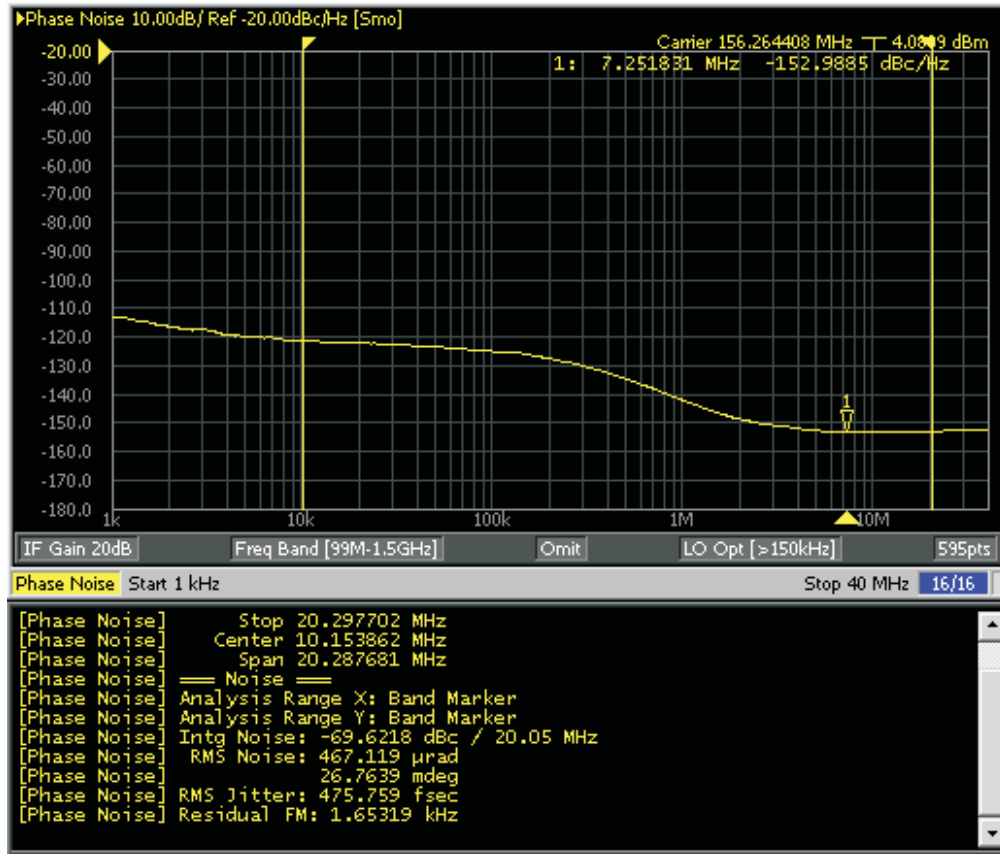
Figure 4. LAN Block Diagram 3

**LAN Solution 3 Jitter Test Results:**

**OUT\_0 = 156.25-MHz LVPEL – RMS Jitter is 477 fsec (10 kHz–20 MHz)**



**OUT\_1 = 156.25-MHz LVPEL – RMS Jitter is 476 fsec (10 kHz–20 MHz)**



**LAN Solution 4 Block Diagram:**

This solution uses the four-output version CDCM61004 to generate four copies of 125 MHz. If less outputs are needed, the CDCM61001 and CDCM61002 can supply one or two outputs, respectively.

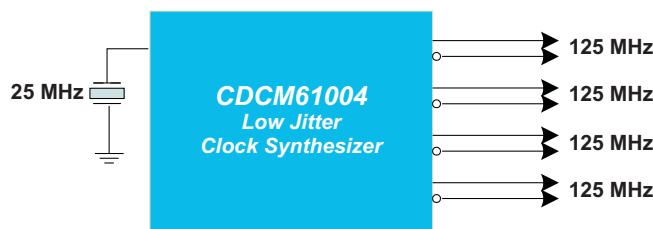
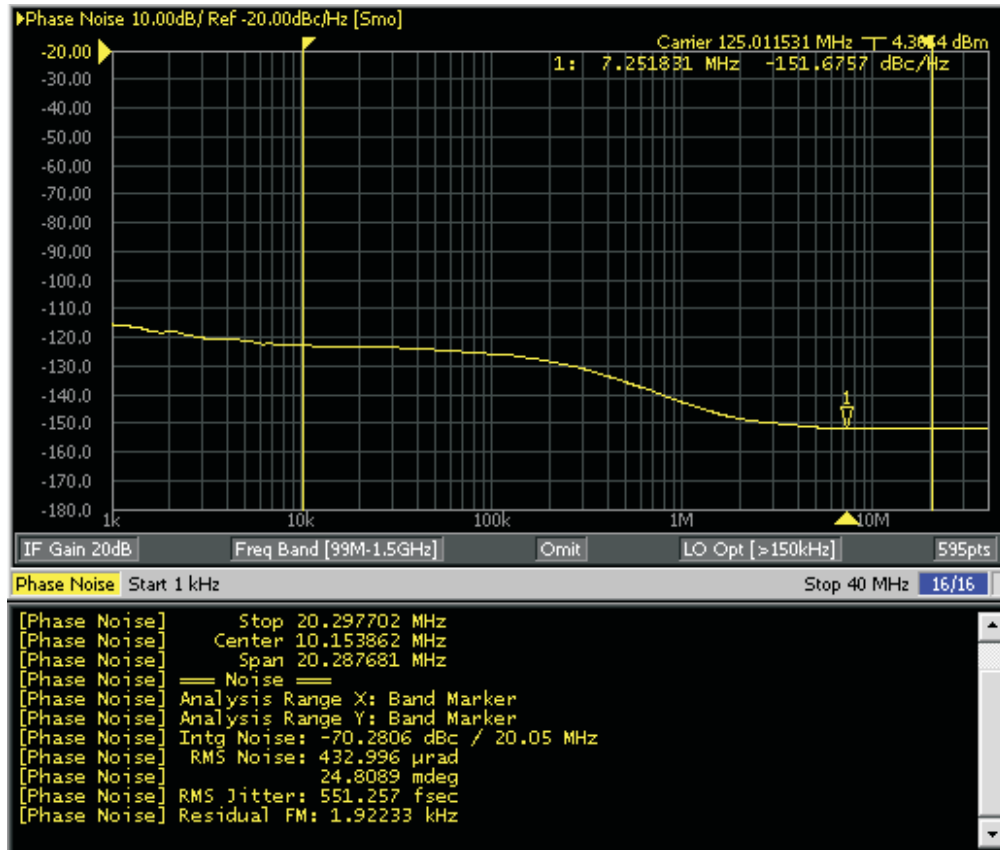


Figure 5. LAN Block Diagram 4

**LAN Solution 4 Jitter Test Results:**

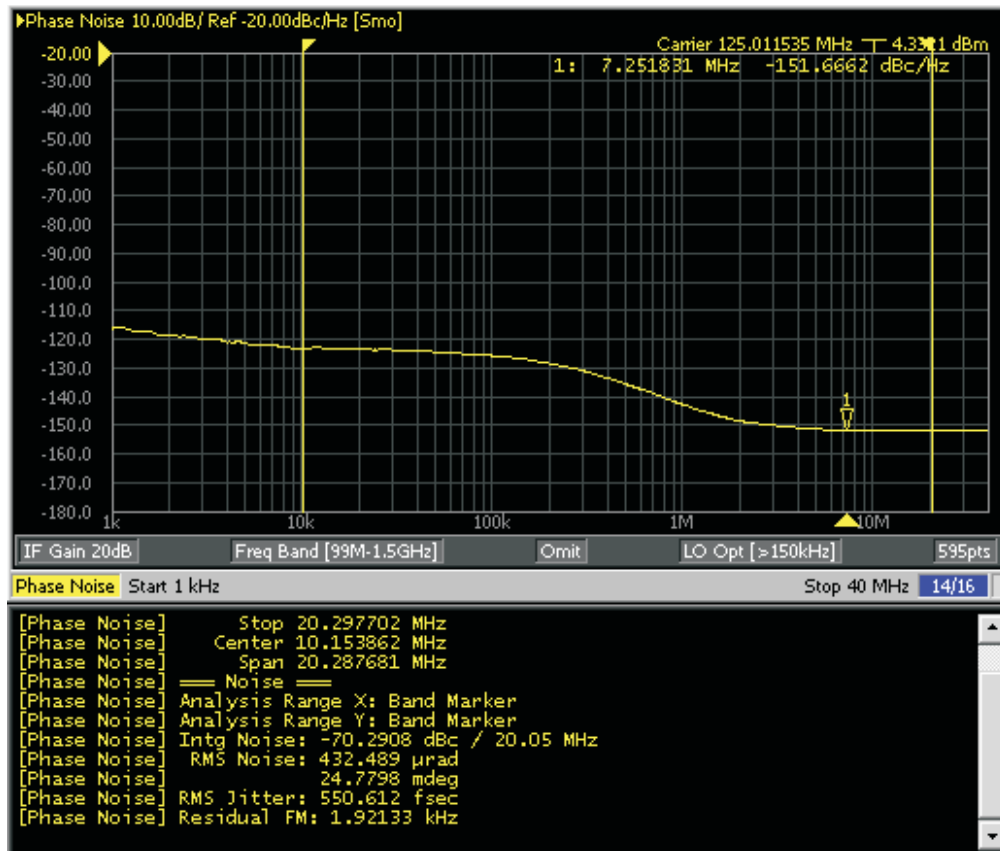
**OUT\_0 = 125-MHz LVPECL – RMS Jitter is 551 fsec (10 kHz–20 MHz)**



OUT\_1 = 125-MHz LVPECL – RMS Jitter is 551 fsec (10 kHz–20MHz)

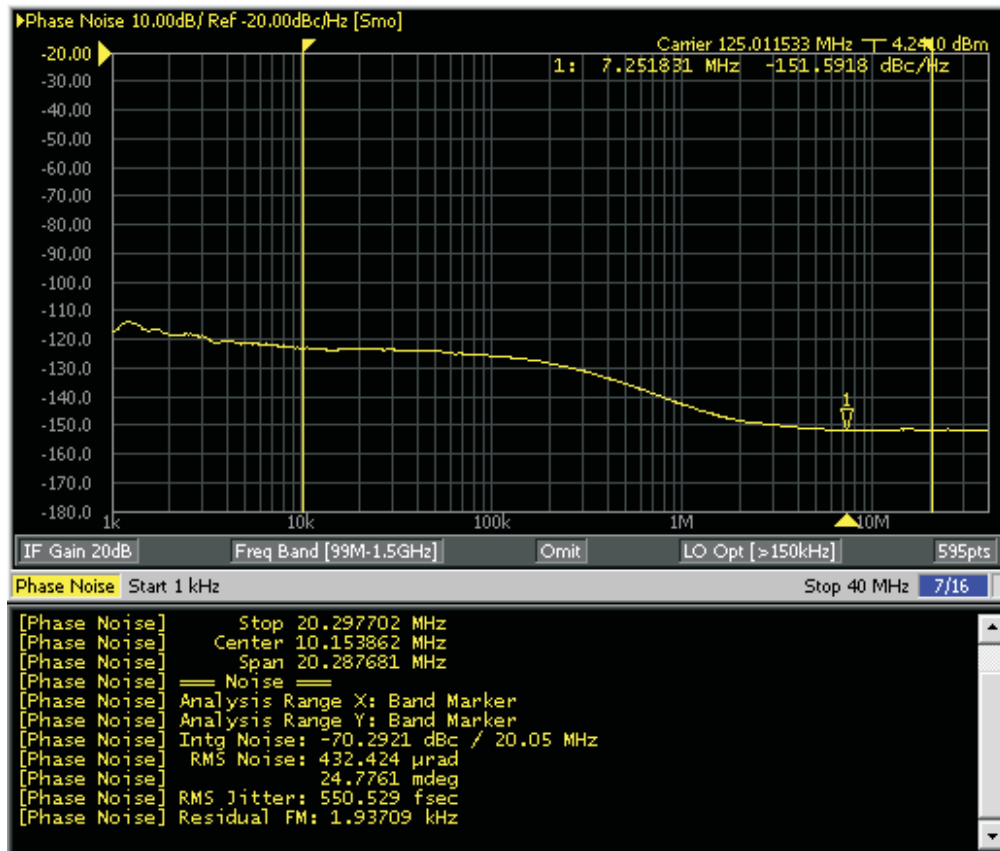
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**OUT\_1 = 125-MHz LVPECL – RMS Jitter is 551 fsec (10 kHz–20MHz)**

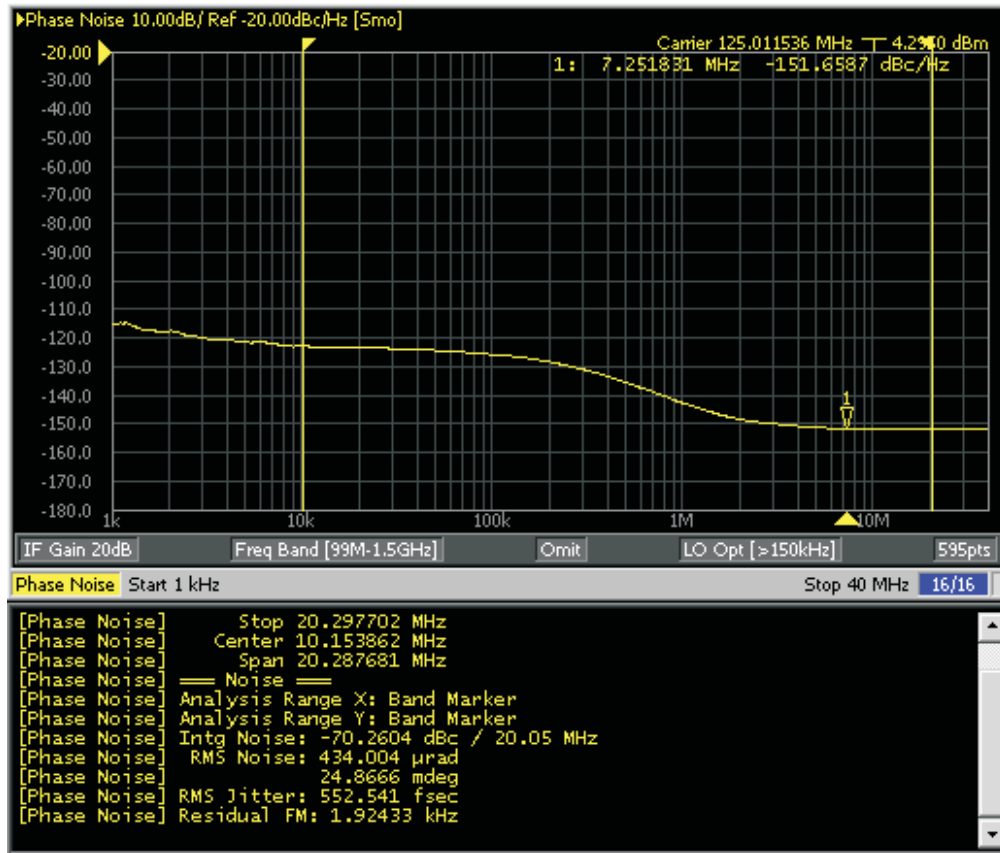




OUT\_2 = 125-MHz LVPECL – RMS Jitter is 551 fsec (10 kHz–20 MHz)



**OUT\_3 = 125-MHz LVPECL – RMS Jitter is 553 fsec (10 kHz–20 MHz)**



**Block Diagram and Jitter Test Results of WAN Solutions**

The following four solutions show how to generate networking WAN clocks from the CDCM6100x devices and a low-cost, standard 24.8832-MHz crystal. The 24.8832 MHz is fed into the CDCM6100x VCO core to generate a 622.08-MHz, 311.04 MHz, 155.52 MHz, or 77.76-MHz frequency available to the output buffer. The output signal type can be native LVPECL, LVDS, or LVC MOS. These examples select LVPECL for the output buffers.

**WAN Solution 1 Block Diagram:**

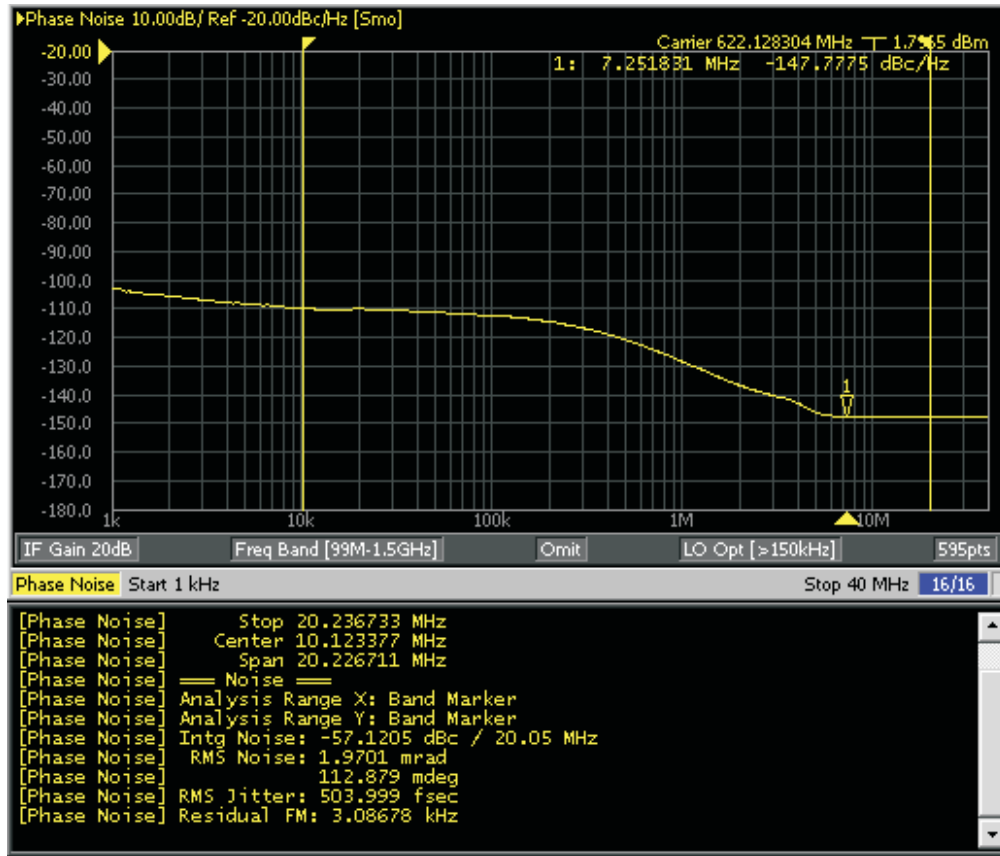
This solution uses the one output version CDCM61001 to generate 622.08 MHz. If more outputs are needed, the CDCM61002 and CDCM61004 can supply two or four outputs, respectively.



Figure 6. WAN Block Diagram 1

**WAN Solution 1 Jitter Test Results:**

**OUT\_0 = 622.08-MHz LVPECL – RMS Jitter is 504 fsec (10 kHz–20 MHz)**



**WAN Solution 2 Block Diagram:**

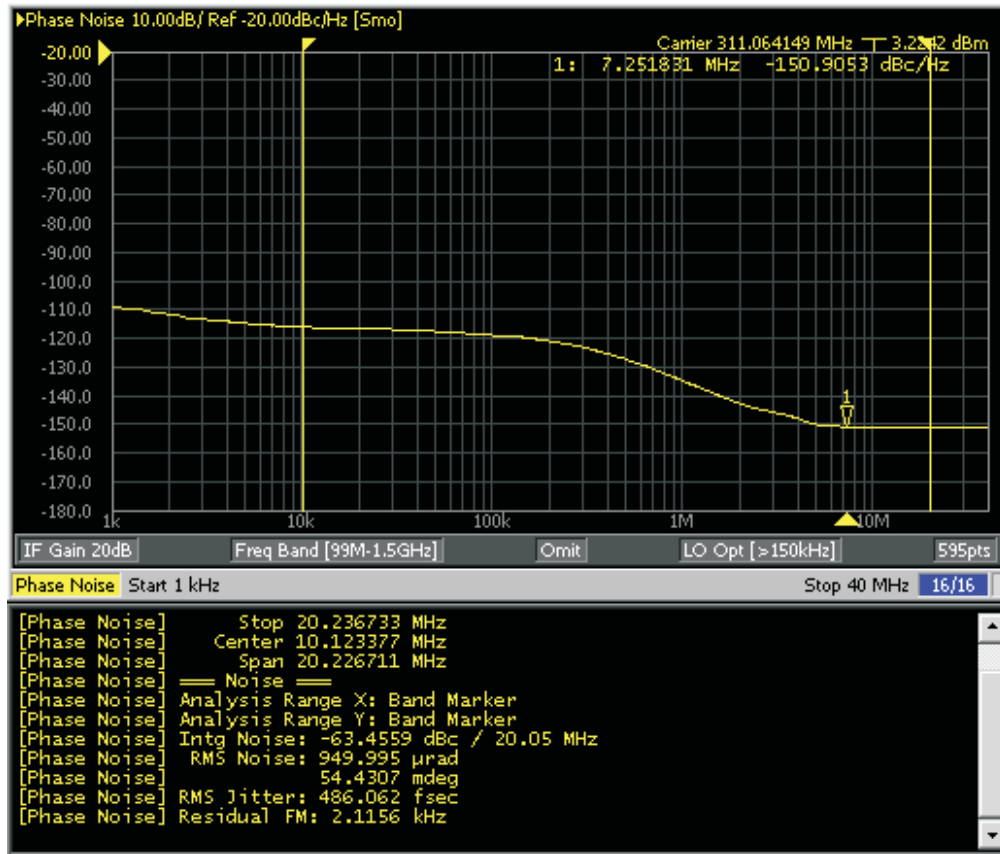
This solution uses the one-output version CDCM61001 to generate 311.04 MHz. If more outputs are needed, the CDCM61002 and CDCM61004 can supply two or four outputs, respectively.



Figure 7. WAN Block Diagram 2

**WAN Solution 2 Jitter Test Results:**

**OUT\_0 = 311.04-MHz LVPECL – RMS Jitter is 486 fsec (10 kHz–20 MHz)**



**WAN Solution 3 Block Diagram:**

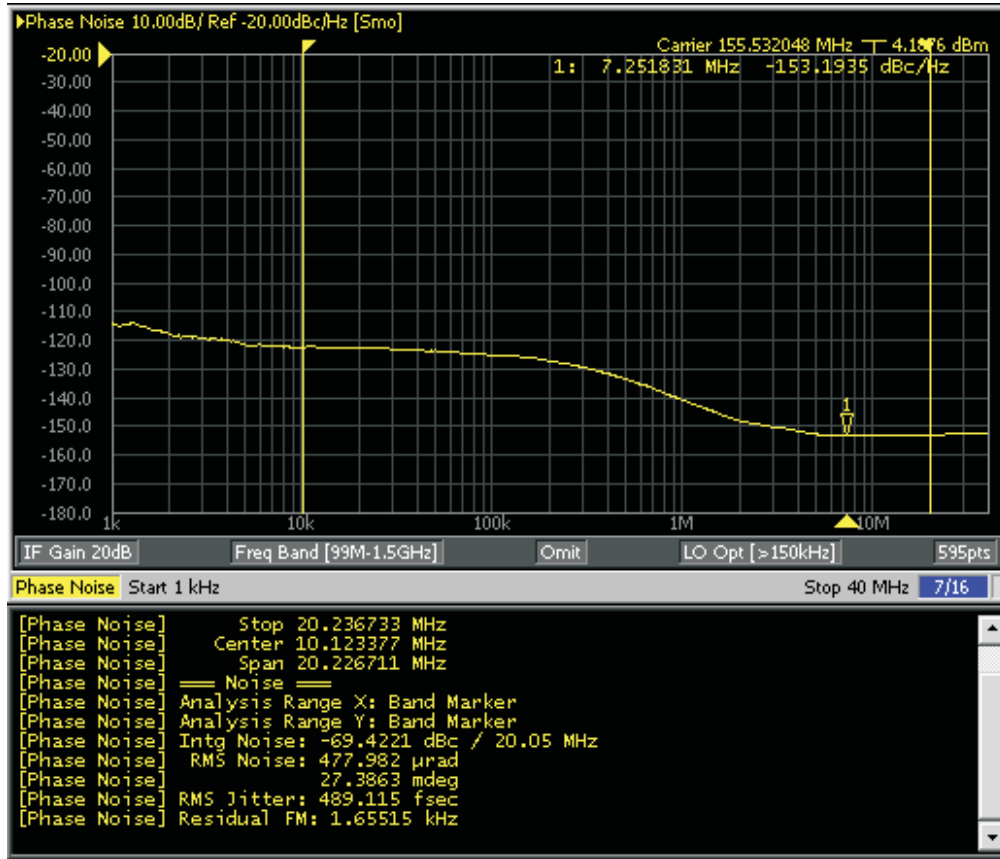
This solution uses the two-output version CDCM61002 to generate two copies of 155.22 MHz. If more or less outputs are needed, the CDCM61001 and CDCM61004 can supply one or four outputs, respectively.



Figure 8. WAN Block Diagram 3

WAN Solution 3 Jitter Test Results:

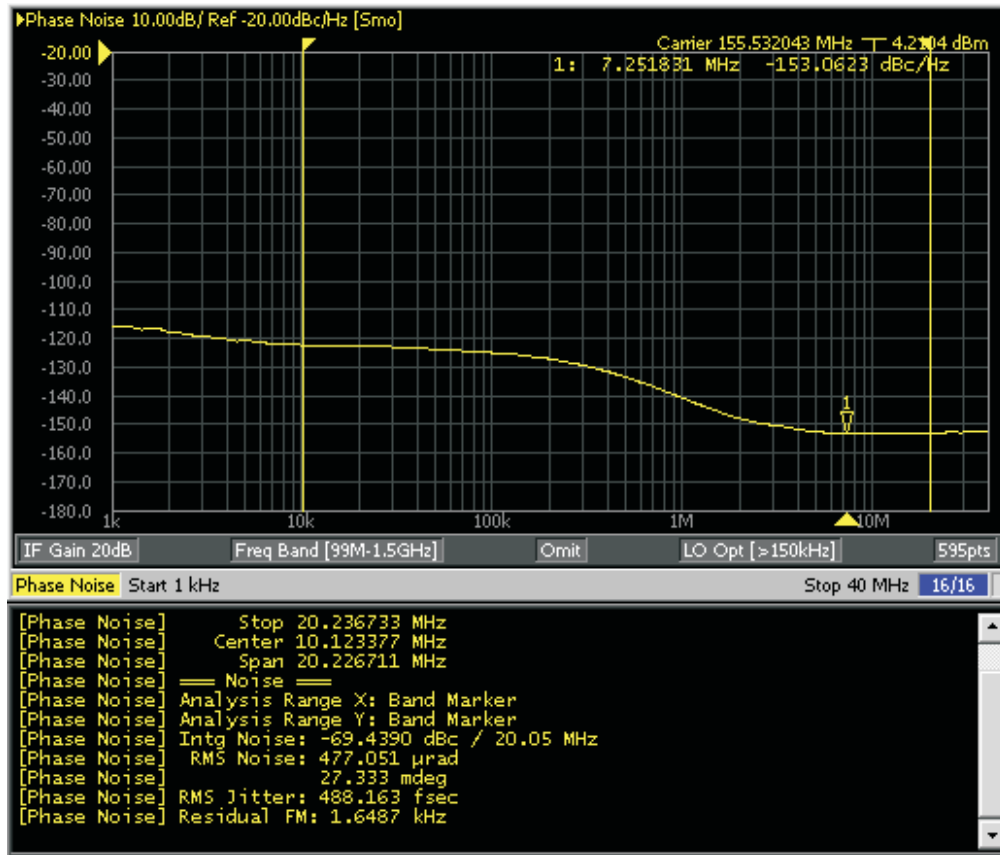
OUT\_0 = 155.52-MHz LVPECL – RMS Jitter is 489 fsec (10 kHz–20 MHz)



OUT\_1 = 155.52-MHz LVPECL – RMS Jitter is 488 fsec (10 kHz–20 MHz)

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**OUT\_1 = 155.52-MHz LVPECL – RMS Jitter is 488 fsec (10 kHz–20 MHz)**



**WAN Solution 4 Block Diagram:**

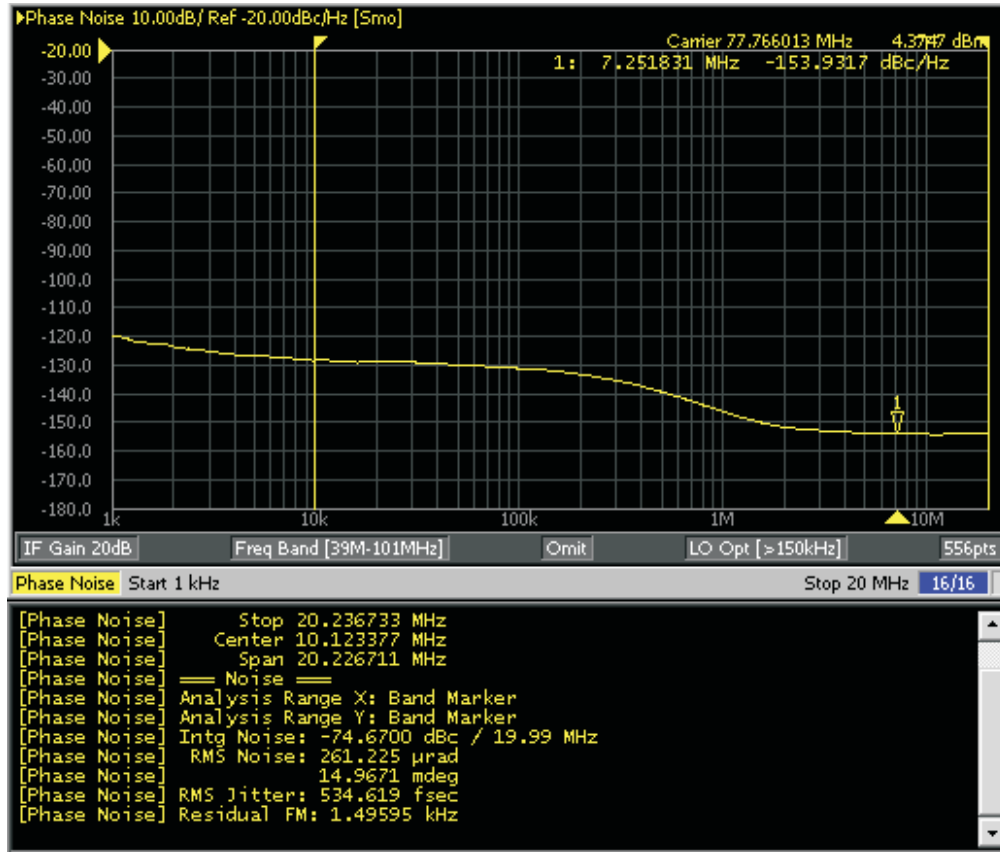
This solution uses the four-output version CDCM61004 to generate four copies of 77.76 MHz. If less outputs are needed, the CDCM61001 and CDCM61002 can supply one or two outputs, respectively.



Figure 9. WAN Block Diagram 4

WAN Solution 4 Jitter Test Results:

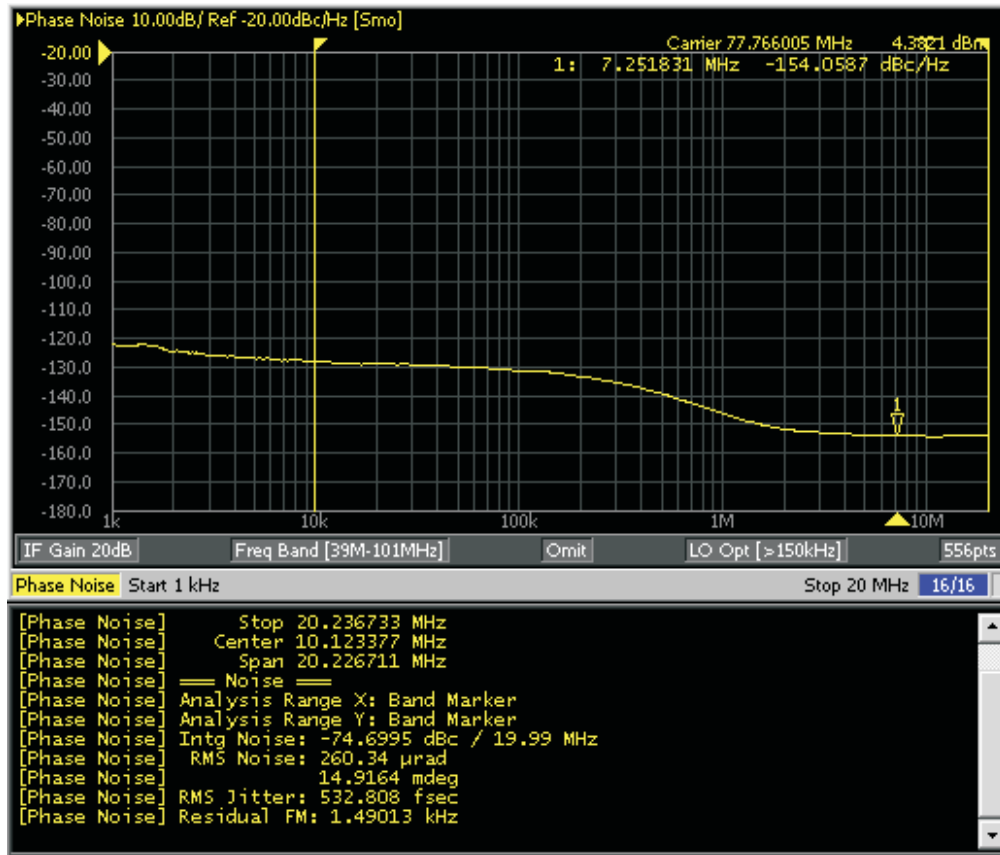
OUT\_0 = 77.76-MHz LVPECL – RMS Jitter is 535 fsec (10 kHz–20 MHz)



OUT\_1 = 77.76-MHz LVPECL – RMS Jitter is 533 fsec (10 kHz–20 MHz)

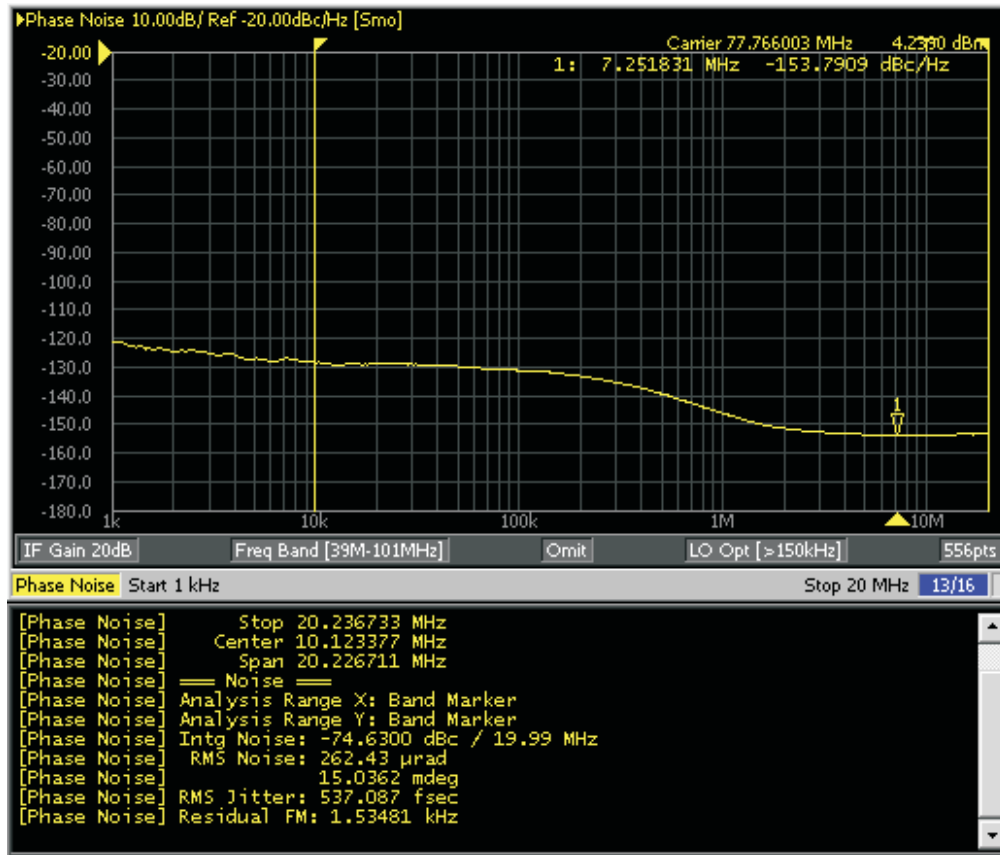
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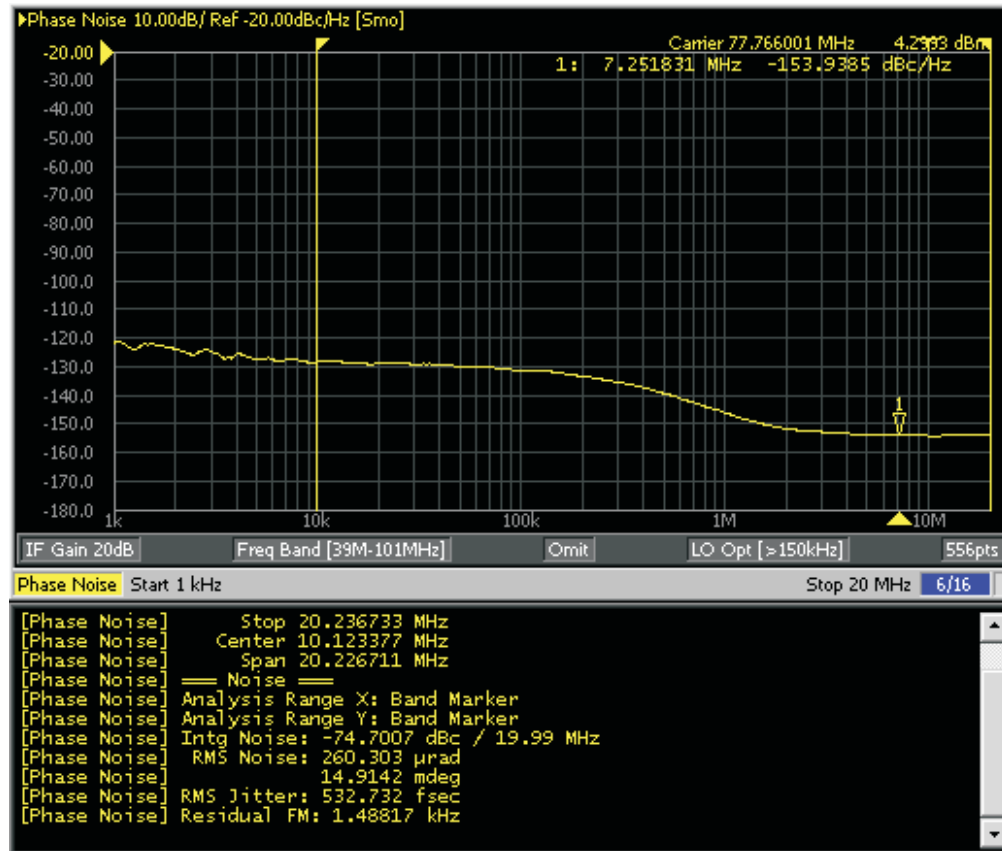
**OUT\_1 = 77.76-MHz LVPECL – RMS Jitter is 533 fsec (10 kHz–20 MHz)**





**OUT\_2 = 77.76-MHz LVPECL – RMS Jitter is 537 fsec (10 kHz–20 MHz)**



**OUT\_3 = 77.76-MHz LVPECL – RMS Jitter is 533 fsec (10 kHz–20 MHz)**


## Performance Summary

### LAN Configurations

Performance results of this LAN configuration are:

1. **CDCM61001 = 625 MHz**  
OUT\_0 = 625-MHz LVPECL – **RMS Jitter is 494 fsec** (10 kHz–0 MHz)
2. **CDCM61001 = 312.5 MHz**  
OUT\_0 = 312.5-MHz LVPECL – **RMS Jitter is 470 fsec** (10 kHz–20 MHz)
3. **CDCM61002 = 2 × 156.25 MHz**  
OUT\_0 = 156.25-MHz LVPECL – **RMS Jitter is 477 fsec** (10 kHz–20 MHz)  
OUT\_1 = 156.25-MHz LVPECL – **RMS Jitter is 476 fsec** (10 kHz–20 MHz)
4. **CDCM61004 = 4 × 125 MHz**  
OUT\_0 = 125-MHz LVPECL – **RMS Jitter is 551 fsec** (10 kHz–20 MHz)  
OUT\_1 = 125-MHz LVPECL – **RMS Jitter is 551 fsec** (10 kHz–20 MHz)  
OUT\_2 = 125-MHz LVPECL – **RMS Jitter is 551 fsec** (10 kHz–20 MHz)  
OUT\_3 = 125-MHz LVPECL – **RMS Jitter is 553 fsec** (10 kHz–20 MHz)

### WAN Configurations

Performance results of this WAN configuration are:

1. **CDCM61001 = 622.08 MHz**  
OUT\_0 = 622.08-MHz LVPECL – **RMS Jitter is 504 fsec** (10 kHz–20 MHz)
2. **CDCM61001 = 311.04 MHz**  
OUT\_0 = 311.04-MHz LVPECL – **RMS Jitter is 486 fsec** (10 kHz–20 MHz)
3. **CDCM61002 = 2 × 155.52 MHz**

OUT\_0 = 155.52-MHz LVPECL – **RMS Jitter is 489 fsec** (10 kHz–20 MHz)  
 OUT\_1 = 155.52-MHz LVPECL – **RMS Jitter is 488 fsec** (10 kHz–20 MHz)

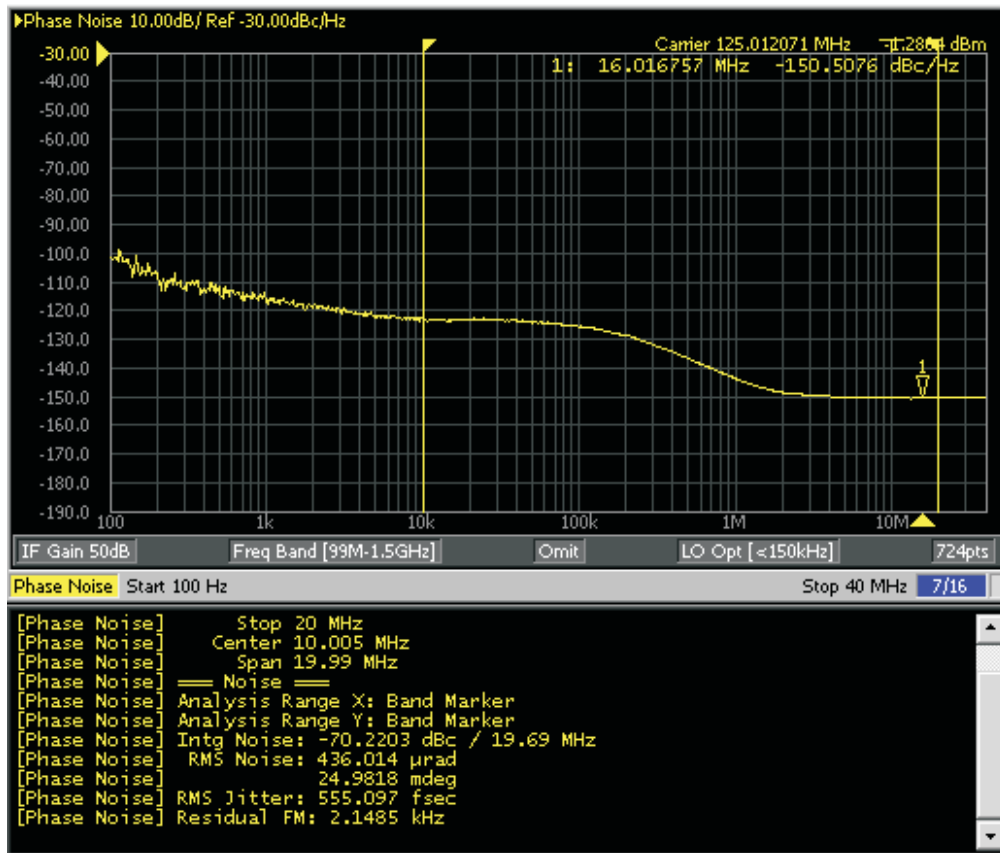
4. **CDCM61004 = 4 × 77.76 MHz**

OUT\_0 = 77.76-MHz LVPECL – **RMS Jitter is 535 fsec** (10 kHz–20 MHz)  
 OUT\_1 = 77.76-MHz LVPECL – **RMS Jitter is 533 fsec** (10 kHz–20 MHz)  
 OUT\_2 = 77.76-MHz LVPECL – **RMS Jitter is 537 fsec** (10 kHz–20 MHz)  
 OUT\_3 = 77.76-MHz LVPECL – **RMS Jitter is 533 fsec** (10 kHz–20 MHz)

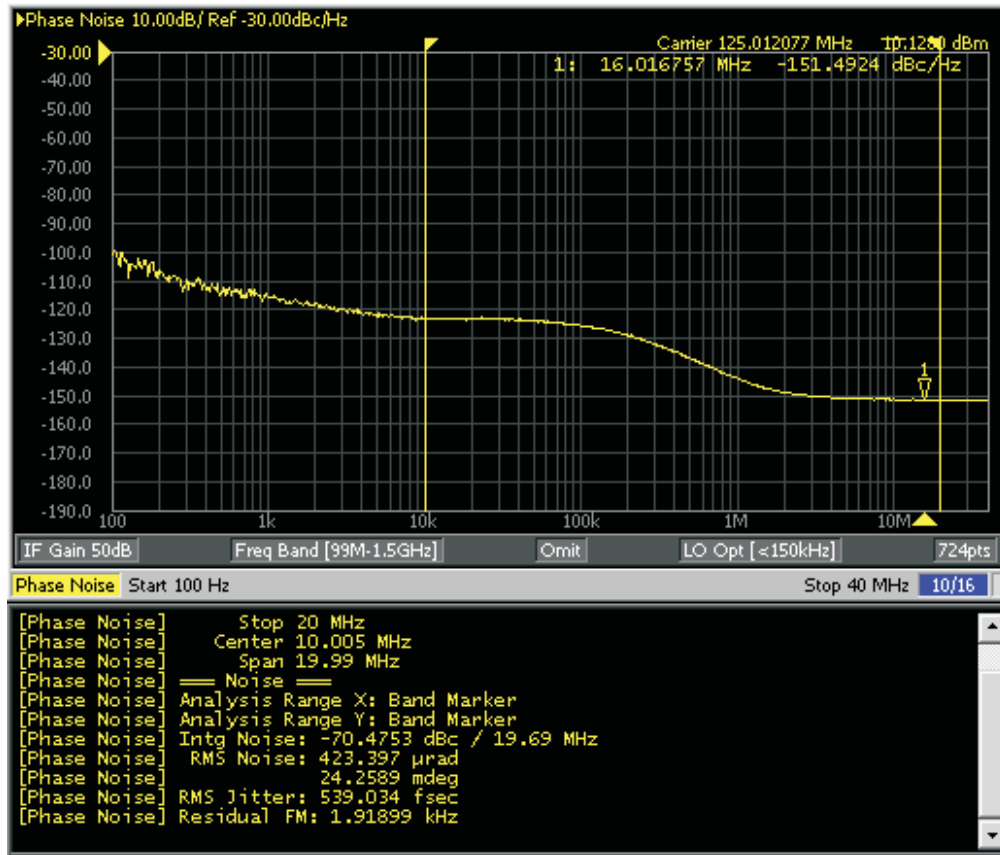
**Additional Data**

As previously mentioned, the CDCM6100x output type can be configured to LVPECL, LVDS, or LVCMOS. The following are some additional jitter measurements with LVDS and LVCMOS outputs.

**125-MHz LVDS – RMS Jitter is 555 fsec (10 kHz–20 MHz)**

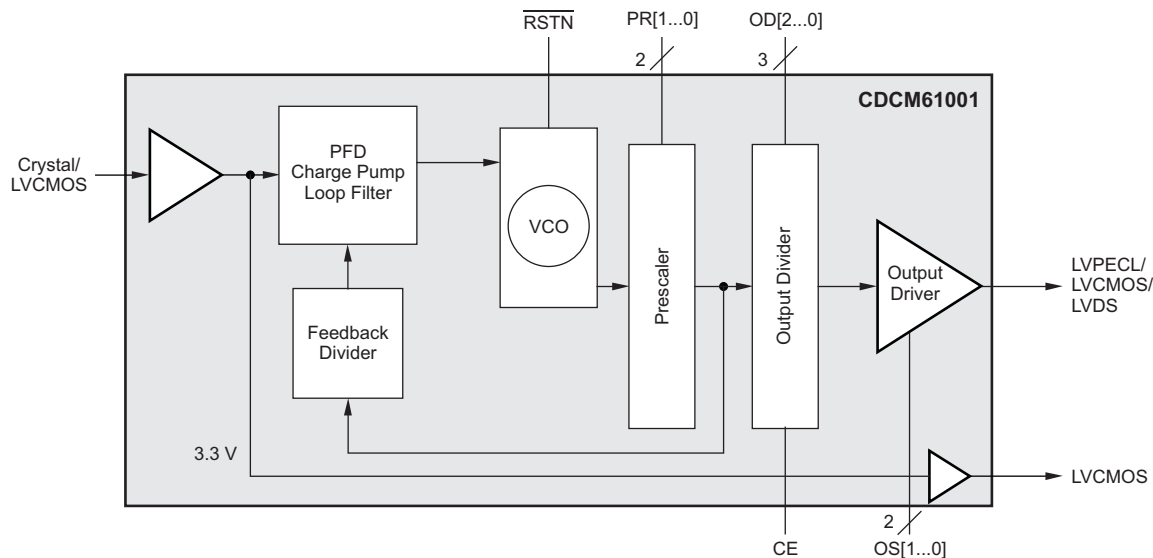


### 125-MHz LVCMOS – RMS Jitter is 539 fsec (10 kHz–20 MHz)

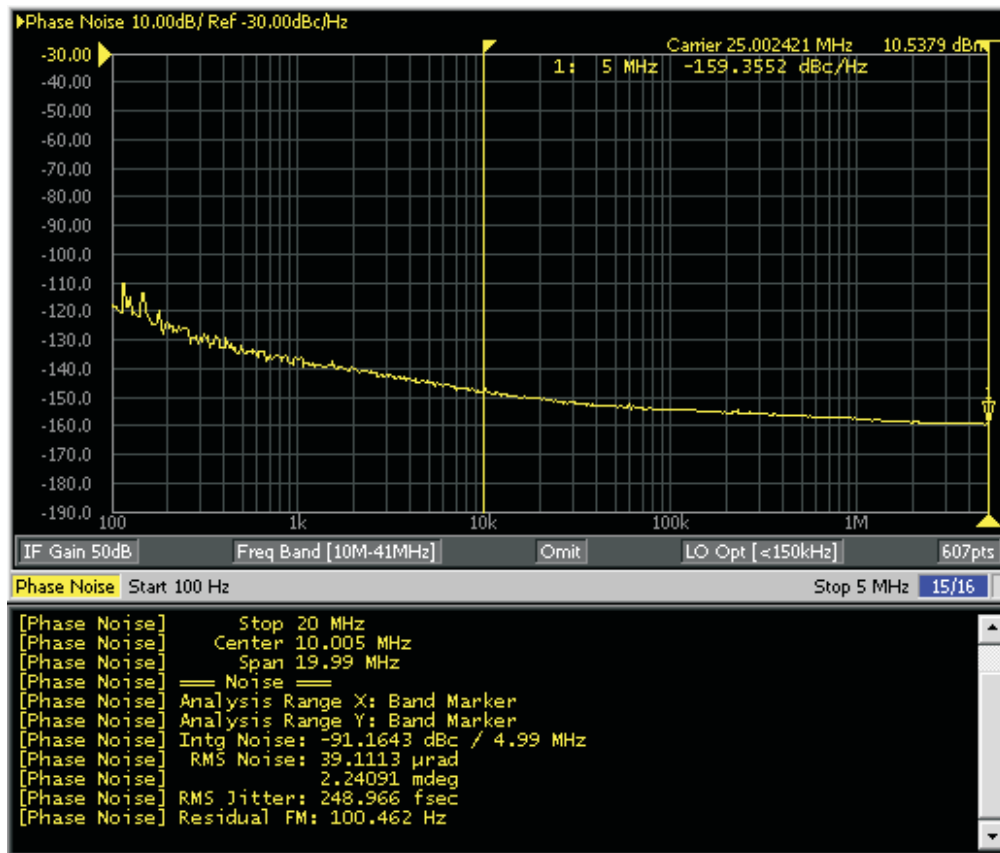


### Crystal Bypassed Output

The CDCM6100x also has a unique feature that is worth noting. The device includes a bypassed output of the crystal frequency that is LVCMOS. OSC\_OUT is an LVCMOS output that can be used in test mode to monitor proper loading of the input crystal to achieve the necessary crystal frequency with least error. This bypassed output is only available when the main outputs are selected on the LVPECL level. The output buffer is disabled during VCO calibration and is enabled only after calibration is complete. A 25-MHz input crystal was used in these examples.



**25-MHz LVCMOS – RMS Jitter is 249 fsec (10 kHz–5 MHz)**



**Conclusion**

The CDCM6100x performance meets today’s networking frequencies and low-jitter requirements <1 ps rms. It is a simple hardware configurable device that requires no preprogramming. The CDCM6100x is offered in a 32-pin, 5-mm × 5-mm QFN package. This single, 3.3-V device can replace the functionality of expensive oscillators and buffers. The CDCM6100x also offers an additional LVCMOS output at crystal frequency.

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