

SSTL for DIMM Applications

SCBA014
December 1997



Introduction

The stub series-terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The primary application for SSTL devices is to interface with SDRAMs.

Texas Instruments (TI™) is the first logic vendor to design and produce a device that meets the SSTL switching standard. Currently, customers are successfully using the only available SSTL device, TI's SSTL16837, to interface to SDRAMs on dual in-line memory modules (DIMMs). As operating frequencies increase and as the demand for faster memory interfaces continues to grow, a wide acceptance of the SSTL interface standard is anticipated. With this in mind, TI is committed to providing the required functionality to meet and exceed customer expectations.

This application report discusses the SSTL interface standard and, in particular, the SSTL16837. This device is not only the first SSTL-compliant device on the market, but is also the only SSTL device currently being manufactured. (TI released the SSTL16837 to production in 2Q97 and plans to release the SSTL16847 in 1Q98.) The main topics discussed in this application report are:

- Background
- Technology and design
- Uniqueness of device
- Features
- Typical design applications
- Laboratory testing technique
- Results
- Competition analysis
- SPICE/IBIS models
- Package information
- Frequently asked questions
- Conclusion
- Glossary
- References

Background

The problem is simple. Designers are constantly trying to get the most out of their designs in the most cost-effective means. As faster versions of a particular CPU become available, the designer will often try to improve the throughput of an existing design simply by increasing the CPU clock frequency.^[1]

After a certain point, the speed of the system's main memory...becomes the limiting factor in the throughput of the system....^[1]

Of course, this problem can be fixed through the use of fast main memory. The only question remaining is what speed of main memory must be used to support the fastest possible operation.^[1]

These issues resulted in JEDEC defining the first official SSTL switching standard. This standard (JC-16-97-04) specified a supply voltage equal to 3.3 V and was accepted by JEDEC in early 1997.

The standard specified a particular termination scheme with appropriate values for the resistors and capacitor. Two resistors in parallel are used to establish a voltage level such that differential voltage swings can be utilized and two may be utilized and two different resistor value configurations are acceptable. Class I specifies an acceptable value of 50 ohms for the terminating resistor

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R_T , and Class II specifies an acceptable value of 25 ohms. The standard states that for each value of R_T , a capacitive load equal to 10 pF or 30 pF can be used. Additionally, a series resistor R_S is specified at 25 ohms.

Figure 1 illustrates a simplified output buffer/driver, Class II environment for a SSTL device.

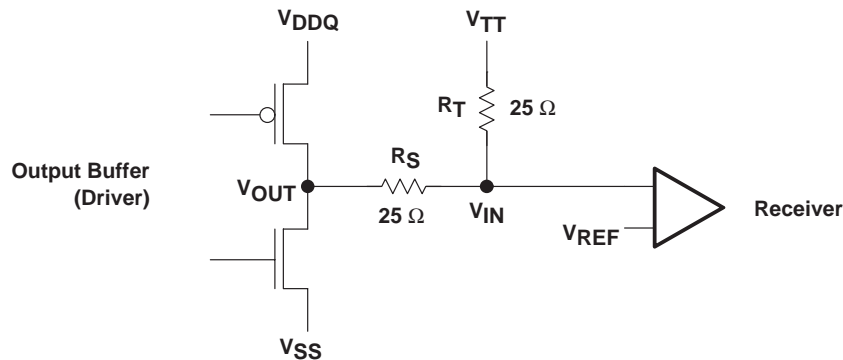


Figure 1. SSTL Simplified Output Buffer/Driver, Class II Environment

Core supply voltages are migrating from 5 V to 3.3 V. As this trend continues, manufacturers have begun to use 2.5-V supply levels and are beginning to consider supply voltages of 1.8 V. Memory supply-voltage levels generally tend to lag core-supply voltages, and although memory is still predominantly at a 5-V supply level, memory is beginning to migrate to 3.3 V eventually reaching the 2.5-V and 1.8-V supply-voltage levels. The need for a 2.5-V specification for SSTL was foreseen and as a result, JEDEC defined a 2.5-V SSTL specification (JC-16-97-58). The primary differences between the 3.3-V and the 2.5-V SSTL specifications are provided in Table 1.

Table 1. Convention for 3.3-V Versus 2.5-V SSTL Device Identification

PARAMETER	V _{CC} = 3.3 V	V _{CC} = 2.5 V
V _{REF}	1.5	1.25
V _{IH} (min)	V _{REF} + 0.2	V _{REF} + 0.18
V _{IL} (max)	V _{REF} - 0.2	V _{REF} - 0.18

As noted in Table 1, the values of V_{REF} and the corresponding differential input ranges vary from 3.3 V to 2.5 V. For the 3.3-V specification, the reference voltage is 1.5 V with the magnitude of the differential from the reference voltage to an input high or low level being 200 mV. The 2.5-V specification utilizes a reference voltage of 1.25 V with the magnitude of the differential from the reference voltage to an input high or low level being 180 mV.

Technology and Design

The SSTL16837 is a 3.3-V BiCMOS device with differential inputs. To reduce the power consumption of the device, all of the data inputs, as well as the output-enable pin, are CMOS. For speed considerations, the latch-enable and clock-input pins are BiCMOS. The output circuitry is a totem-pole CMOS design, but is converted to SSTL levels by using the appropriate configuration and values of the resistors R_S and R_T , as shown in Figure 1.

Uniqueness of Device

The SSTL16837 is a 20-bit universal bus driver (UBD) with 3-state outputs. As a UBD, it can operate in three different modes: transparent, latch, and flip-flop. In the transparent mode, the device operates as a flow-through buffer when the latch-enable pin is not activated. In the latch mode, input data is latched if the latch-enable pin is activated and the clock is held at a high or low level. In the flip-flop mode, input data is stored in the flip-flop on the low-to-high transition of the clock.

The SSTL16837 was designed to reduce power consumption. A bias generator was specifically added to the circuitry to adjust for variances in process, temperature, and V_{CC} . Additionally, the device pinout is arranged for reduced noise, e.g., control inputs (the reference voltage, the output enable, the latch enable, and the clock) are positioned so that package parasitics would be reduced and less power consumed. The clock input was centered to minimize the clock-to-Y propagation delay variances in all output pins.

The SSTL16837 promotes uniformity across ac specifications. More specifically, although only one input pin for the clock exists, the internal implementation uses four clocks to reduce the distance required for the signal to travel from the clock to the various internal circuits. Each clock was strategically placed by its own set of five bits, thereby further reducing potential skew and enhancing device consistency and signal uniformity.

In addition to the SSTL16837, TI is developing a second device that conforms to SSTL specifications; the SSTL16847 is a 20-bit buffer with 3-state outputs that is optimized at a supply voltage equal to 3.3 V.

Features

The SSTL interface standard was created specifically for high-speed interfacing to SDRAMs. As such, the SSTL16837 features a maximum frequency specification of 200 MHz. In attaining this frequency, the input high and low voltage levels (V_{IH} and V_{IL}) are $V_{REF}+200\text{ mV}$ and $V_{REF}-200\text{ mV}$, respectively. This 400-mV input voltage swing allows much faster operation of the device than is normally possible using the standard 1.2-V difference in LVTTL levels where V_{IH} and V_{IL} equal 2 V and 0.8 V, respectively.

The SSTL16837 supports both SSTL and LVTTL switching levels. Although the data sheet provides specifications where SSTL levels are used for the input and output levels, the device can operate under any combination of SSTL/LVTTL levels as inputs and outputs. When the device is operated using the SSTL level as the output level, it functions noticeably faster than when LVTTL levels are used. When LVTTL levels are used for the outputs, the device's propagation delay is increased by approximately 2 ns. Regardless of whether SSTL or LVTTL is used as the input switching level, V_{REF} still must be established and provided on the appropriate input pin. Irrespective of the input and output switching levels however, the characteristic high-level and low-level output drive current of 20 mA is maintained.

The SSTL16837 was designed and optimized to operate with a supply voltage of 3.3 volts, and it is to this value that the data sheet specifications apply. However, laboratory testing shows the device also operates at a supply voltage of 2.5 V, with only a minimal amount of degradation in the propagation delay values. (The results are discussed in the *Results* section). The power supply was reduced to 1.8 V and the SSTL16837 continued to function correctly. (A standard for 1.8 V has not been defined in the electronics industry, but a calculated estimation of appropriate switching levels was used when conducting the laboratory tests.) These results also are discussed in the *Results* section.

All SSTL16837 totem-pole outputs have a dedicated V_{DDQ} supply that (as stated in the SSTL_3 JEDEC standard), can be lower than or equal to V_{DD} , but never greater than V_{DD} . This feature allows for the internal circuitry supply voltage to be raised to 3.6 V for maximum speed performance, while lowering V_{DDQ} to prevent the device from dissipating large amounts of power in the output stage.

Typical Design Applications

As a universal bus driver, the SSTL16837 is used for buffering address lines to memory and can be operated in a transparent, latch, or flip-flop mode. Various factors influence whether buffering is required, including drive strength of the core logic, frequency, capacitive load, physical length from the driver to the receiver, and the resulting reflection that may occur. Buffering address and data lines ensures adequate current is supplied to the receiver and assists in quieting noisy circuits. The flip-flop mode is commonly used to ensure the minimum skew between address lines.

Although the SSTL switching standard is still relatively new and the number of observed applications is limited, the SSTL16837 usually resides directly on the DIMM. In some systems, however, it is located on the motherboard. Current applications use one SSTL device per DIMM to drive up to 18 SDRAMs.

The SSTL16837 can operate at both LVTTTL and SSTL levels on the input and output ports. Although a switching level for a given range of frequencies is not specified by JEDEC, the general trend is to use the LVTTTL switching level for systems that use frequencies less than 100 MHz. For systems with frequencies greater than 125 MHz, SSTL is more commonly used. Systems implementing frequencies between 100 MHz and 125 MHz commonly use either LVTTTL or SSTL.

Laboratory Testing Technique

To demonstrate the operation of TI's SSTL device, testing the SSTL16837 with V_{CC} equal to 3.3 V, 2.5 V, and 1.8 V was desired. For this particular device, the worst-case readings are obtained at high V_{CC} , high temperature, and high capacitive loading. The resultant V_{CC} values were then set to 3.6 V and 2.7 V, with C_L set to 30 pF and with the temperature at 70°C. (Since a standard for the 1.8-V switching level has not been identified, V_{CC} was set to 1.8 V for that level.) As the level of V_{CC} varied, appropriate changes were made to V_{REF} , V_{TT} , V_{IH} , and V_{IL} . For all tests, R_S and R_T remained constant at 25 ohms meeting SSTL Class II specifications), and T_A was held constant at 70°C. Table 2 summarizes the laboratory setup that was implemented.

Table 2. Laboratory Testing Setup Parameters

PARAMETER	$V_{CC} = V_{DDQ} = 3.6\text{ V}$ $V_{REF} = 1.5\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 1.37\text{ V}$ $V_{IH} = 1.68\text{ V}$ $C_L = 30\text{ pF}$	$V_{CC} = V_{DDQ} = 2.7\text{ V}$ $V_{REF} = 1.35\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 1.17\text{ V}$ $V_{IH} = 1.53\text{ V}$ $C_L = 30\text{ pF}$	$V_{CC} = V_{DDQ} = 1.8\text{ V}$ $V_{REF} = 0.9\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 0.72\text{ V}$ $V_{IH} = 1.08\text{ V}$ $C_L = 30\text{ pF}$
V_{DD}	3.6 V	2.7 V	1.8 V
V_{REF}	1.5 V	1.35 V	0.9 V
V_{TT}	1.5 V	1.35 V	0.9 V
V_{IH}	1.68 V	1.53 V	1.08 V
V_{IL}	1.37 V	1.17 V	0.72 V
R_S	25 Ω	25 Ω	25 Ω
R_T	25 Ω	25 Ω	25 Ω
C_L	30 pF	30 pF	30 pF
T_A	70°C	70°C	70°C

Results

Using the conditions provided in Table 2, data was taken for high-to-low and low-to-high transitions for propagation delay from the input to the output (A to Y), for propagation delay from the clock to the output (CLK to Y), for propagation delay from the latch enable to the output (LE to Y), and for enable and disable times (OE to Y). Additionally, timing specifications also were measured for setup and hold times under a variety of conditions, as specified in the SSTL16837 data sheet and provided in Table 3. Finally, data taken was for levels of the output high and low voltages, V_{OH} and V_{OL} respectively, under steady-state conditions.

The results obtained when V_{CC} was set to 3.6 V were well within the data-sheet maximum specification values; for propagation delay, the laboratory results were approximately 1 ns faster than shown in the data sheet. For enable time, the laboratory results were approximately 1.5 ns faster and for disable time, the laboratory results were approximately 1.5 ns faster. Setup times measured in the laboratory under the above conditions decreased from 200 ps to 700 ps and hold times decreased by 400 ps.

The SSTL16837 was designed and optimized to operate with a supply voltage of 3.3 V. Even when the supply voltage was reduced to 2.5 V, however, the speed did not degrade substantially. The propagation delays increased by approximately 300 ps, the enable time increased by approximately 1 ns, and the disable time decreased by approximately 500 ps. (In most instances, an increase in disable time would be expected; however, the decrease in disable time may have been due to differential voltage levels between the input and output trip points.) Table 3 lists setup-time and hold-time values measured in the laboratory under the above conditions.

The propagation delay times slightly more than doubled when V_{CC} was set to 1.8 V when compared to the 3.6-V supply voltage values. The enable time increased around 65% and the disable time increased by around 50%. Table 3 lists setup-time and hold-time values measured in the laboratory under the above conditions.

The results obtained from the laboratory, with their appropriate testing conditions, are summarized in Table 3.

Table 3. Results of Laboratory Testing

PARAMETER	$V_{CC} = V_{DDQ} = 3.6\text{ V}$ $V_{REF} = 1.5\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 1.37\text{ V}$ $V_{IH} = 1.68\text{ V}$	$V_{CC} = V_{DDQ} = 2.7\text{ V}$ $V_{REF} = 1.35\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 1.17\text{ V}$ $V_{IH} = 1.53\text{ V}$	$V_{CC} = V_{DDQ} = 1.8\text{ V}$ $V_{REF} = 0.9\text{ V}$ $T_A = 70^\circ\text{C}$ $V_{IL} = 0.72\text{ V}$ $V_{IH} = 1.08\text{ V}$
$t_{PLH}\text{ A}\rightarrow\text{Y}$	3.3 ns	3.64 ns	6.3 ns
$t_{PHL}\text{ A}\rightarrow\text{Y}$	2.41 ns	2.95 ns	5.35 ns
$t_{PLH}\text{ CLK}\rightarrow\text{Y}$	1.9 ns	2.1 ns	4.21 ns
$t_{PHL}\text{ CLK}\rightarrow\text{Y}$	2.02 ns	1.9 ns	4.74 ns
$t_{PLH}\text{ LE}\rightarrow\text{Y}$	2.79 ns	3.19 ns	7.47 ns
$t_{PHL}\text{ LE}\rightarrow\text{Y}$	2.48 ns	2.87 ns	6.15 ns
$t_{PLZ}\text{ OE}\rightarrow\text{Y}$	4.13 ns	3.66 ns	6.15 ns
$t_{PZL}\text{ OE}\rightarrow\text{Y}$	3.73 ns	4.69 ns	6.12 ns
$t_{PHZ}\text{ OE}\rightarrow\text{Y}$	4.65 ns	4.04 ns	6.78 ns
$t_{PZH}\text{ OE}\rightarrow\text{Y}$	4.06 ns	5.1 ns	6.64 ns
$t_{su}\text{ A before CLK}\uparrow\text{ and LE low}$	1.3 ns	0.44 ns	0.9 ns
$t_{su}\text{ A before LE}\downarrow\text{ and CLK high}$	1.1 ns	0.96 ns	1.08 ns
$t_{su}\text{ A before LE}\downarrow\text{ and CLK low}$	1.3 ns	1.89 ns	2 ns
$t_h\text{ A after CLK}\uparrow\text{ and LE low}$	0.6 ns	0.36 ns	0.7 ns
$t_h\text{ A after LE}\downarrow$	0.6 ns	0.46 ns	0.72 ns
V_{OH}	2.88 V	2.19 V	1.38 V
V_{OL}	0.44 V	0.37 V	0.79 V

Competition Analysis

TI is committed to being the market leader for SSTL and is striving to be the vendor of choice for design engineers who require SSTL logic to meet the requirements of their systems. TI has released a device to production, has a second SSTL device scheduled to be released, and is conducting research to determine and define the next sequence of SSTL devices.

SPICE/IBIS Models

SPICE and IBIS models are available for the SSTL16837. The SPICE model is a level-13 model, consists of the input and output stages, and can be obtained by contacting your local TI sales representative. The IBIS model consists of the input and output stages and can be obtained by accessing <http://www.ti.com/sc/docs/asl/models/ibis.htm>.

Package Information

The SSTL16837 and the SSTL16847 are 64-pin devices in a thin shrink small-outline package (TSSOP) DGG package. A pinout of the SSTL16837 is shown in Figure 2.

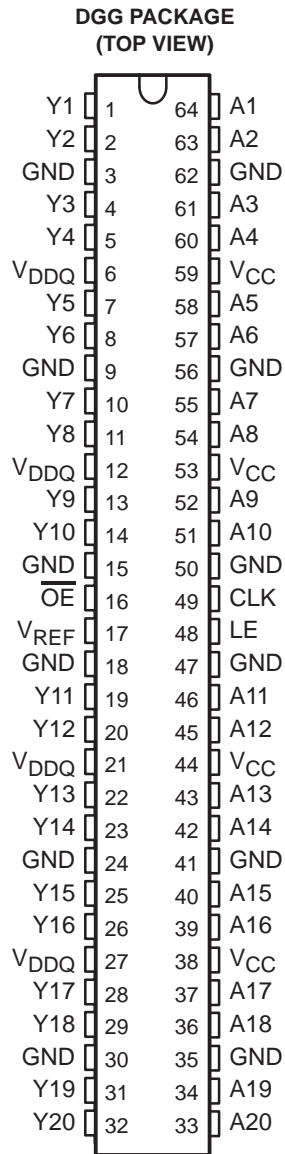


Figure 2. SSTL16837 Pinout

The DGG package has a lead pitch of 0.5 mm and measures nominally 17 millimeters in length by 8.1 millimeters (including pin length) in width; this conforms to JEDEC MO-153.

Frequently Asked Questions

Question: How do I get a copy of the SSTL16837 data sheet and samples?

Answer: The SSTL16837 data sheet can be obtained by accessing <http://www.ti.com/sc/docs/psheets/pids.htm>. Samples of the SSTL16837 can be obtained by contacting your local TI sales representative.

Question: How do I get a copy of the SSTL16837 SPICE and IBIS models?

Answer: The SPICE model for the SSTL16837 can be obtained by contacting your local TI sales representative. The IBIS model can be obtained by accessing <http://www.ti.com/sc/docs/asl/models/ibis.htm>.

Question: Are there any plans to release other SSTL devices?

Answer: Yes. TI currently is designing the SSTL16847, which is a 20-bit buffer/driver. It conforms to the SSTL interface standard, has 20-mA drive, and is planned to be released to production in 1Q98. Furthermore, TI is conducting market research to determine the next series of required SSTL devices.

Question: Why is SSTL considered a high-frequency switching standard?

Answer: The SSTL switching standard was defined for interfacing with SDRAMs at high frequencies. Features such as the usage of differential inputs and a specifically prescribed bus-termination scheme, which reduces the output voltage swing required for a high or low state, allows SSTL devices to operate at high frequencies.

Question: Can I run the SSTL16837 device at LVTTTL levels?

Answer: Yes, the SSTL16837 device operates at LVTTTL levels, both on the input switching level and on the output switching level. When LVTTTL levels are used for the output switching level, however, the device's propagation delay is increased by approximately 2 ns.

Question: What does the future hold for SSTL, specifically double data rate (DDR) SDRAMs?

Answer: SSTL is envisioned to be the switching standard of the future for interfacing with high-speed memory. As SSTL continues to grow and become more widely used, designers may find that implementing SSTL in their designs is necessary to remain competitive. The DDR scheme utilizes both the rising and the falling edges of the clock, allowing data to be processed at twice the typical speed. This arrangement is expected to be widely used in systems since it essentially doubles the throughput.

Conclusion

The SSTL standard specifies a method of interfacing with high-speed SDRAMs. It employs a reduced voltage swing on the inputs by specifying a reference voltage with a 400-mV total differential voltage from a high-level input to a low-level input, and a unique termination scheme on the output. SSTL is envisioned to be the switching standard of the future for interfacing with SDRAMs.

Although designed and optimized for a supply voltage of 3.3 V, the SSTL16837 also can operate at supply voltage levels of 2.5 V and 1.8 V. Additionally, only a slight degradation in performance from 3.3 V to 2.5 V was observed.

The SSTL16837 and the SSTL16847 are address drivers and can be used to buffer address lines when interfacing to SDRAMs.

Glossary

DDR	Double data rate
DIMM	Dual in-line memory module
IBIS	I/O buffer information specification
JEDEC	Joint Electron Devices Engineering Councils
LVTTL	Low-voltage transistor-transistor logic
SDRAM	Synchronous dynamic random access memory
SPICE	Simulation program with integrated circuit emphasis
SSTL	Stub series-terminated logic
TI	Texas Instruments
TSSOP	Thin shrink small-outline package
TTL	Transistor-transistor logic
UBD	Universal bus driver

References

1. Handy, Jim, *The Cache Memory Book*, Academic Press, Inc., Harcourt Brace & Company, Publishers, 1993.
2. *Stub Series-Terminated Logic for 3.3 Volts (SSTL_3)* JC-16-97-04
3. *Stub Series-Terminated Logic for 2.5 Volts (SSTL_2)* JC-16-97-58
4. *Semiconductor Group Package Outlines*, 1997, literature number SSYU001C

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