Design Tradeoffs When Implementing IEEE 1149.1

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Introduction

This paper explores the many design tradeoffs that occur when implementing the IEEE 1149.1 test bus in integrated circuits (IC), printed wiring boards (PWB), and systems. As with any design task, tradeoffs must be made to achieve the best mix of functionality, testability, reliability, producibility, and maintainability. As an industry-wide standard, the IEEE 1149.1 test bus and boundary-scan architecture allows a consistent method for circuit controllability and observability across all levels of development and test. Test and debug operations can be performed via the IEEE 1149.1 test bus and boundary-scan architecture in many areas including design verification, fault troubleshooting, factory board and system test, and field test without requiring actual physical access. Embedded test features, which previously could be accessed only at one test level, can be accessed easily at each level of integration (i.e., IC, board, subsystem, and system).

Test Considerations – Ad Hoc/Structured

There are two fundamental ways to apply testability to a design: ad hoc (or unstructured) and structured. Ad hoc testability is simply intended to solve a particular test problem (i.e., adding a test point to observe a signal line during board test). While this may be useful for a particular test environment, in this case factory board test, it may not be useful for any other test environment, such as IC or system test. Structured testability, on the other hand, is designed to be useful at several levels of test. For instance, an IC with built-in self test (BIST) and a standard test interface can be used for IC test, board test, and system test. This type of testability is considered structured because it is standardized and can be used in several test environments.

What is IEEE 1149.1?

The IEEE 1149.1 test bus and boundary-scan architecture allow an IC, and similarly a board or system, to be controlled via a standard four-wire interface. Each IEEE 1149.1-compliant IC incorporates a feature known as boundary scan that allows each functional pin of the IC to be controlled and observed via the four-wire interface. Test, debug, or initialization patterns can be loaded serially into the appropriate IC(s) via the IEEE 1149.1 test bus. This allows IC, board, or system functions to be observed or controlled without actual physical access.

The IEEE 1149.1 test bus comprises two main elements: a test access port (TAP), which interfaces internal IC logic with the external world via a four-wire (optionally, five-wire) bus; and a boundary-scan architecture, which defines standard boundary cells to drive and receive data at the IC pins. IEEE 1149.1 also defines both mandatory and optional opcodes and test features. The test bus signals are: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), Test Data Out (TDO), and the optional Test Logic Reset (TRST). The IEEE 1149.1 specification also specifies that the ICs can be connected in either a ring or star configuration. A simplified block diagram of the architecture is shown in Figure 1.

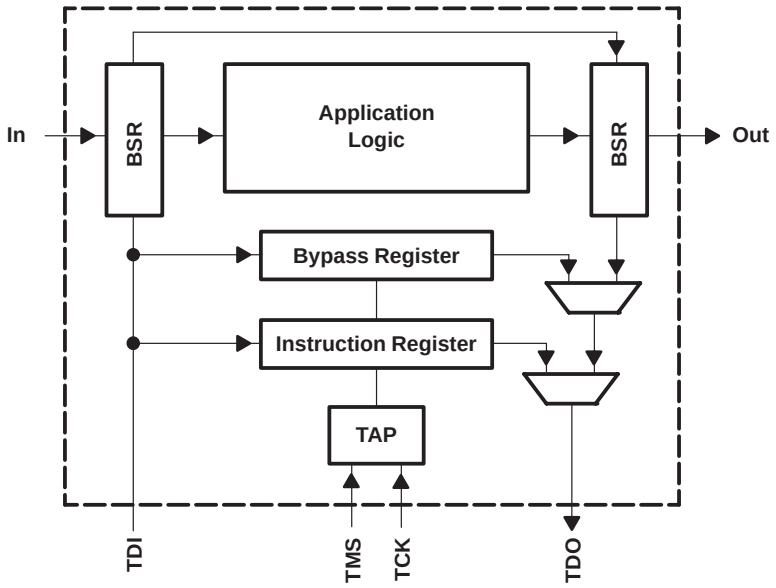


Figure 1. IEEE 1149.1 Scan-Bus and Boundary-Scan Architecture

Overview

Design Costs Versus Test Costs

Cost is a driving requirement when designing any system. Design costs are easily calculated in terms of part costs, manufacturing assembly, engineering design labor, etc. Test costs are also quantifiable but may not be done as easily. Certainly, test equipment and test software development costs can be readily calculated, but test times, troubleshooting, and repair are not as obvious. In complex designs or designs that have long service lives, the life-cycle costs (LCC) of the product are dominated by test and maintenance costs, not design and production costs. It is typical to "invest" time and money to design for test, which then saves production and maintenance costs. To provide an easy and cost-effective method to include IEEE 1149.1 testability into any design, Texas Instruments (TI) has developed a family of testable ICs and Application-Specific Integrated Circuit (ASIC) cells, These ICs and ASIC cells are members of the System Controllability, Observability, and Partitioning Environment (SCOPE™) family.

Use of Scannable Parts

Two complementary techniques are used when designing IEEE 1149.1 into a system: off-the-shelf parts (i.e., TI SCOPE bus-interface products) and ASICs. Each satisfies a particular application, but both can be used together in the same design. TI SCOPE bus-interface products and other off-the-shelf parts are suitable when testability is needed in a functionally equivalent device. Consider a simple PWB with a processor and memory. Without testable SCOPE bus-interface products, the address and data buses would have to be tested indirectly by writing and reading memory via the processor. The embedded address and data buses buffered by '244 and '245 parts can be replaced by functionally-equivalent IEEE 1149.1-compliant TI SCOPE bus-interface products. Now, tests of the address and data buses can be achieved by controlling and observing the SCOPE bus-interface products via the IEEE 1149.1 test bus. Addresses and data can be explicitly loaded and driven by the SCOPE bus-interface products or functionally-driven addresses and data can be captured and read via the IEEE 1149.1 test bus.

The other technique used to incorporate IEEE 1149.1 features into a design is by designing it into ASICs. If ASICs are used, adding IEEE 1149.1 is a straightforward and efficient method of implementing testability into a design.

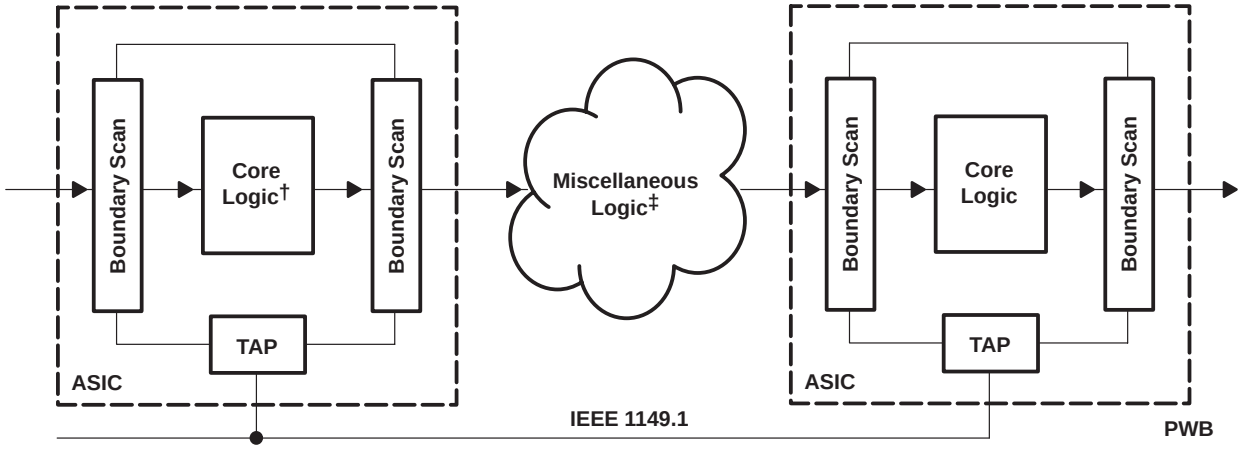
TI also produces several other IEEE 1149.1-compliant test ICs to support PWB and system test. A test-bus controller (TBC) is available to drive the IEEE 1149.1 test bus. Other members of the SCOPE family include scan-path selectors (SPS) to partition long scan paths into multiple small chains and a digital bus monitor (DBM) to monitor and capture data in real time.

Design Tradeoffs in Implementing IEEE 1149.1 IC Level

The following paragraphs present IEEE 1149.1 design tradeoff information at the IC level. While this data is useful in simply comparing IEEE 1149.1 ICs to non-IEEE 1149.1 ICs, this one-to-one comparison is not as useful as comparing the total advantages/disadvantages at the PWB and system levels. Total PWB and system-level tradeoffs, not IC tradeoffs, should be used to determine the final implementation strategy.

Controllability and Observability

Obviously, in addition to performing their functional tasks, the SCOPE family of test products provides a level of controllability and observability that was previously unachievable. During design verification, test, or troubleshooting, signal states may be sampled or controlled via the IEEE 1149.1 interface. Testing can be accomplished on the internal IC logic via pins-in testing, or tests on external IC logic or interconnects via pins-out testing. Pins-in testing is accomplished by loading IC input pins via the IEEE 1149.1 interface, driving the internal logic of the IC, capturing the output pin states, and scanning out the results. Pins-in testing is accomplished by loading IC output pins via the IEEE 1149.1 interface, driving the IC outputs and interconnects, capturing the data at the next IEEE 1149.1 ICs input pins, and scanning out the results. Pins-in and pins-out testing is shown in Figure 2.



† Pins-in testing is accomplished by loading test patterns at IC inputs, driving data across IC logic, and capturing patterns at IC outputs.
‡ Pins-out testing is accomplished by loading/driving test patterns at IC outputs and capturing patterns at the next IC's inputs.

Figure 2. IEEE 1149.1 Pins-In and Pins-Out Testing Via Boundary Scan

BIST/Additional Hooks

In addition to the standard four-wire interface and boundary-scan architecture that IEEE 1149.1 defines, other test or debug "hooks" can be implemented and controlled. For ASICs, it is very common to include some form of BIST to assist in device testing. IEEE 1149.1 provides a standard interface to initiate BIST and retrieve results. Two common BIST methods known as pseudorandom pattern generation (PRPG) and parallel signature analysis (PSA) are supported in the SCOPE bus-interface products and ASIC standard cell libraries. PRPG provides the capability to generate pseudorandom patterns to stimulate a circuit under test. PSA allows a stream of patterns to be collected and compressed into a unique signature. In addition to boundary scan, ASICs and other special-purpose ICs may incorporate internal scan within the IEEE 1149.1 architecture. Internal scan may be used to partition the IC into more easily testable functions, write/read internal registers, etc. TI's later generations of digital signal processors (DSPs) incorporate internal scan to provide built-in in-circuit-emulation features for test and debug. Via the IEEE 1149.1 interface, registers can be loaded/examined and the processor execution can be controlled to RUN/STOP, SINGLE-STEP, etc.

IC Pins/Package Size

The first requirement when implementing IEEE 1149.1 is the addition of four extra pins. This overhead is always required, but is less obvious in larger package devices. Table 1 shows the percent of additional pins per package size.

Table 1. 1149.1 IC Package/Pin Ratio

IC PACKAGE SIZE (NO. OF PINS)	IEEE 1149.1 IC PINS VS TOTAL IC PINS (%)
24	16.7
40	10
64	6.3
100	4
132	3
160	2.5
208	1.9

Gate Count

The number of gates to implement IEEE 1149.1 is driven primarily by the number of IC I/O pins. The reason is that IEEE 1149.1 requires each functional I/O pin to have a boundary cell. Naturally, low-gate-count ICs with a high number of I/O pins will have proportionally more gates to implement IEEE 1149.1. Some typical gate counts from a 1.0-µm standard-cell and gate-array library are shown in Table 2.

Table 2. ASIC SCOPE Cell Gate Count

IEEE 1149.1 FUNCTION	NUMBER OF GATES
Test access port (TAP)	≈183
Instruction register	≈20 gates/bit
Bypass register	≈8 gates
Unidirectional SCOPE boundary cell (hard macro) (standard cell)	≈15 gates/pin
Bidirectional SCOPE boundary cell (standard cell)	≈19 gates/pin
Unidirectional SCOPE boundary cell (soft macro) (standard cell)	≈24 gates/pin

The formula below can be used to estimate the IEEE 1149.1 gate count overhead. (Remember to count only the number of functional I/O pins, not power, ground, or unused pins).

$$\text{Total IEEE 1149.1 gate count} = \text{TAP} + (\text{IR} \times \text{IR bit width}) + \text{BR} + (\text{no. I/O pins} \times \text{no. gates/pin}) \quad (1)$$

Figures 3 and 4 show the relationship between functional gate count versus IEEE 1149.1 test logic versus pin-count increase for both standard-cell and gate-array designs.

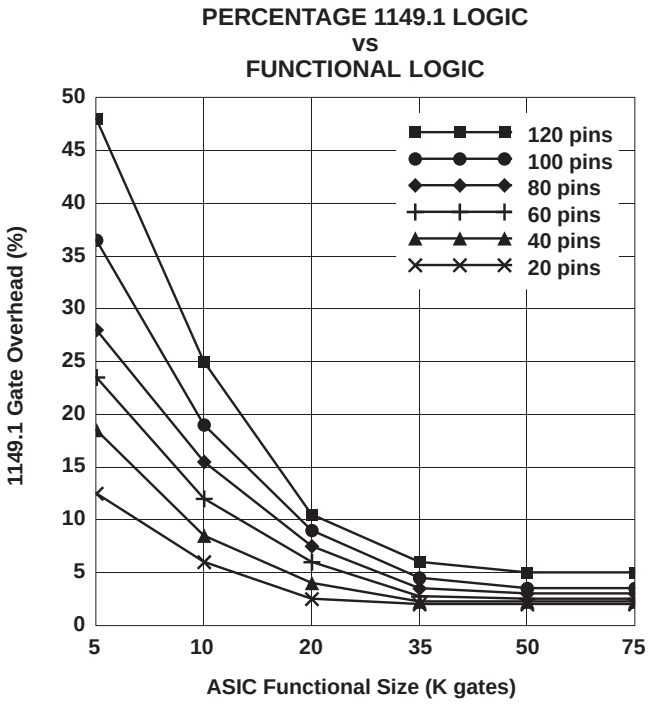


Figure 3. Standard-Cell ASIC 1149.1 Overhead

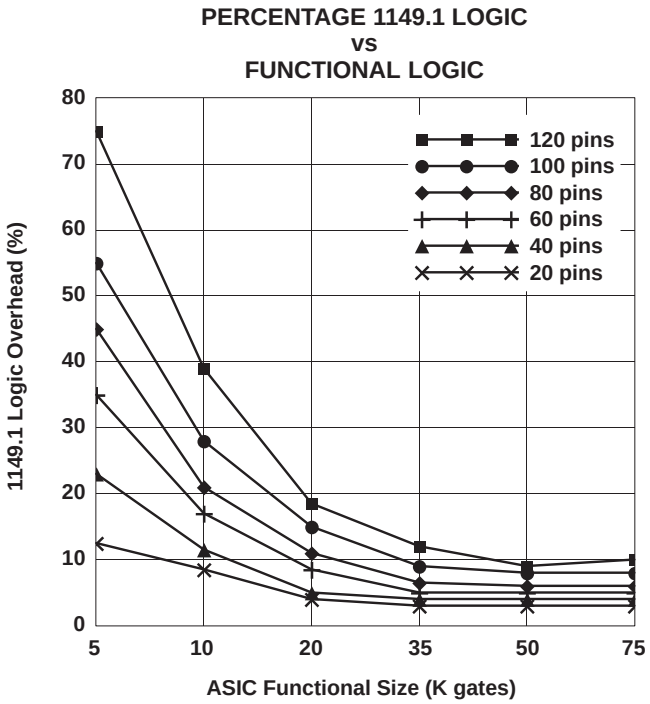


Figure 4. Gate-Array ASIC 1149.1 Overhead

Some actual ASIC examples are shown in Table 3. The first small ASIC was implemented in a gate array. The gate-array boundary cells were constructed as soft macros and therefore required more gates per pin to implement than the SCOPE hard macros. Although the IEEE 1149.1 overhead of the first ASIC may seem excessive, this ASIC acted as a translator and buffer between a processor and memory bus. The IEEE 1149.1 boundary scan provided partitioning and allowed independent testing of the functions via IEEE 1149.1. Since the first ASIC was implemented in a 6K gate array, the gates to implement IEEE 1149.1 were essentially free (they were already on the silicon). The second and third ASICs were implemented as standard-cell hard macros. Also notice that they implement BIST functions to autonomously test functions within the ASICs.

Table 3. Overhead Examples of Implementing IEEE 1149.1 and BIST

ASIC SIZE	IC FUNCTION	1149.1†	BIST	TEST TOTAL	TEST AS % OF TOTAL
4,753 gates‡	2,263	2,490	0	2,490	52.4
20,000 gates§¶	18,350¶	1,650¶	1,000¶	2,650	13.3
87,000 gates§	84,262	1,634	1,104	2,738	3.1

† All ASICs have 70 I/O pins.
‡ Implemented in gate array
§ Implemented in standard cell
¶ Gate count estimated.

Propagation Delay

The controllability and observability achievable with IEEE 1149.1 is accomplished by adding a 2-to-1 multiplexer in the normal data path. This simple solution minimizes propagation delays, yet still allows signal lines to be sampled or driven. The propagation delay of the 2-to-1 multiplexer is dependent on the technology used to implement the device. The propagation delays for a 1.0-µm CMOS ASIC library are approximately 1.0 ns (typical) for a standard-cell hard macro and approximately 1.8 ns (typical) for a gate-array soft macro. Propagation delays will naturally continue to decrease as technology matures.

Reliability

Increased gate count will slightly reduce IC reliability. However, the only functional reliability impact will come from the 2-to-1 multiplexer in the functional data path. This 2-to-1 multiplexer accounts only for two gates per boundary cell. For example, in an 8,000-gate ASIC with 100 functional pins, the 2-to-1 multiplexer only amounts to a 2.5% gate-count increase in the functional data path. This is a very small reliability impact.

Power

Power dissipation is driven by the technology used and the amount of additional IEEE 1149.1 logic. For CMOS technologies, power dissipation increases with clock frequency and gate count. Since most of the test logic (except the 2-to-1 multiplexer in the functional path) remains in a static state, the power consumption of the test logic is small.

Test Costs

The costs of IC test for IC production test and incoming inspection varies greatly with the complexity of the IC. For simple ICs, such as the SCOPE bus-interface products, there is only a slight advantage in using IEEE 1149.1 in an IC-level test. For medium- to high-complexity ICs, such as ASICs and VLSI devices, an IC test using IEEE 1149.1 provides several benefits. First, ASIC and VLSI devices can be tested statically or at low frequencies using the IEEE 1149.1 pins-in and pins-out test methods. Actually, an IEEE 1149.1-based pins-in tester has been demonstrated that simply consists of an IC socket with power, ground, and an IEEE 1149.1 TBC. Test patterns are loaded and captured inside the IC via the IEEE 1149.1 test bus. This method provides a quick, inexpensive method to verify basic IC functionality.

IC test-development costs can be greatly reduced by using the same test patterns used for IC design verification, simulation, and IC tests. The simulation patterns, or a subset, are applied via the IEEE 1149.1 test bus as previously described. The second major benefit of the IEEE 1149.1 test bus is the ability to control and examine internal nodes or states of ASIC and VLSI devices. Hard-to-test functions can be partitioned via internal scan and tested independently with smaller, easier-to-test partitions. An ASIC that may require 2^{20} (1 million) test patterns just to test a 20-bit counter can be tested in a fraction of the patterns by implementing internal scan on the counter. Patterns can be downloaded directly via scan to test any count sequence. A recently developed ASIC with very long counter chains saved over four-million test patterns by implementing internal partitioning controlled via the IEEE 1149.1 test bus.

IC Costs

IC purchase costs with IEEE 1149.1 are higher than their equivalent untestable versions. The cost delta varies, depending on the proportion of IC pins and test logic to functional pins and logic. For larger ASICs, the cost increase is small, but even in small ASIC designs the PWB and system test benefits are realizable. For I/O-limited ASICs (ASICs that have unused core gates), the cost increase is typically less than the proportional gate increase. For core-limited ASICs (ASICs that do not have spare gates), the cost may be proportional to the increase in gates, or possibly higher.

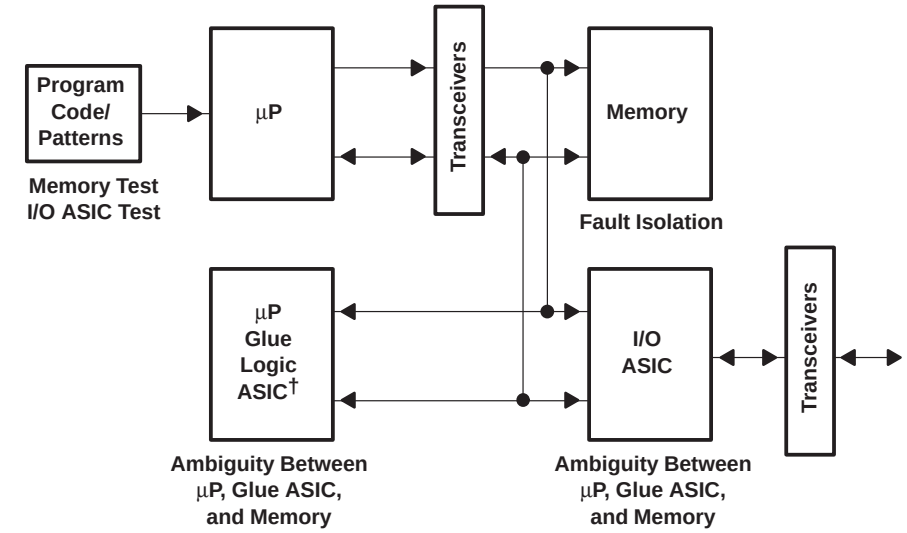
PWB Design

The following paragraphs review PWB-level advantages/disadvantages when implementing designs with the IEEE 1149.1 test bus. PWB test advantages using the IEEE 1149.1 test bus are much more obvious since PWB test problems are more challenging.

Partitioning

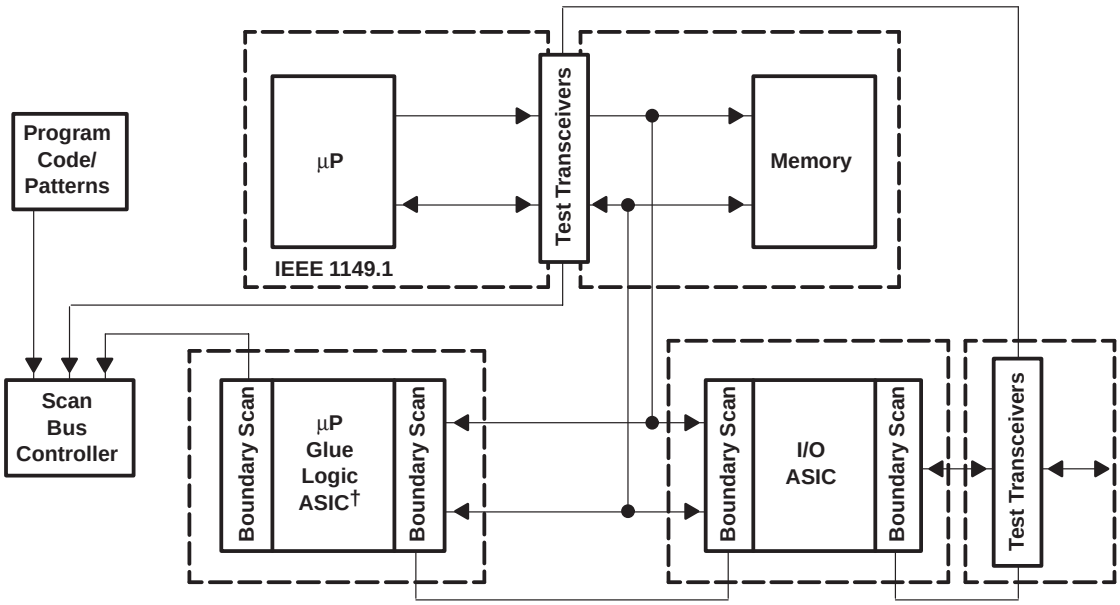
Partitioning is always a very important design consideration for PWB test. Any medium-to-high complexity PWB must have adequate partitioning to allow independent testing of major logic functions. In most designs, testable partitions can be created by simply replacing the normal buffers and transceivers, which are already required in the design, with SCOPE bus-interface products. The SCOPE bus-interface products perform the same buffer, latch, or transceiver function, but now they can be controlled via the IEEE 1149.1 test bus to load or sample signal states during design verification, test, and debug.

For instance, consider the simple microprocessor board design shown in Figure 5. In order to execute test software, the processor, memory, glue-logic ASIC, IC, and PWB interconnects must be fault free. If a fault exists on the memory data bus, the processor will execute bad code and control will be lost. By adding boundary scan in the ASICs and replacing the bus transceivers with SCOPE bus-interface products, as shown in Figure 6, the processor, memory, and ASICs can be tested independently. This reduces the ambiguity group and results in better fault isolation. Repair and replacement savings can be realized by faster troubleshooting and fault isolation to fewer components. By using the partitioning provided by the SCOPE bus-interface products and ASICs with IEEE 1149.1, PWB failures can be detected and isolated with less probing or arbitrary part substitution.



† Memory, decode, I/O decode, etc.

Figure 5. Simple Processor PWB Design



† Memory, decode, I/O decode, etc.

Figure 6. Design Partition Via Boundary Scan

Real Estate

The PWB test-logic real-estate impact can be minimized and, in some cases, PWB real estate can be gained by using IEEE 1149.1 to test functions. PWB real-estate savings can be accomplished by replacing an IC added for test purposes with boundary scan embedded in the IC silicon. Test logic that is added to meet fault detection or fault isolation can be efficiently implemented and controlled via the IEEE 1149.1 test bus.

In a recent design, several latches were added to capture and buffer some key internal bus-control signals for PWB test. If the internal bus is buffered by ASICs with boundary-scan or SCOPE bus-interface products, the signal states can be observed via the boundary-scan cells. This eliminates the need to add components for test purposes.

Test Points/Connector Size

IEEE 1149.1 boundary scan can be used to reduce or eliminate the number of test points or test pins on a PWB. When the four-wire IEEE 1149.1 test bus is brought out to the connector, many previously “hidden” internal nodes become visible. Boundary-scan cells can be thought of as virtual test points that can sample or control a node as shown in Figure 7. These virtual test points allow signal states to be scanned out and examined. Similarly, signal states can be scanned in and driven across circuit logic and interconnects. These control and observe operations can be performed via the IEEE 1149.1 test bus without the need to physically probe or route the signals under test to a test connector.

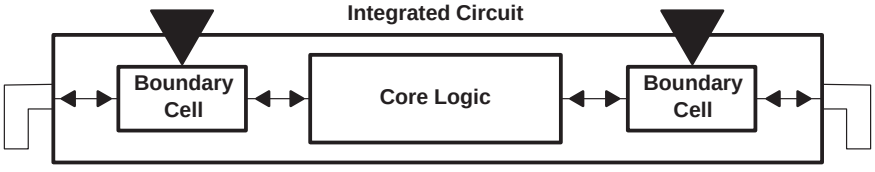


Figure 7. Virtual Test Points Via IEEE 1149.1 Boundary Scan

Two main advantages are obvious when using IEEE 1149.1 boundary scan as virtual test points. The first advantage is that fewer test points are required if critical signals are buffered by SCOPE bus-interface products or ASIC boundary cells. The second advantage is that boundary cells are not subject to the potential noise problems that may be caused by additional etch and pins of test points.

Reliability

PWB reliability usually will not increase significantly by adding IEEE 1149.1 to the design. The small increase in silicon gates may not be notable when compared at the PWB level. In fact, reliability may increase when ad hoc testability is replaced by IEEE 1149.1. Also, remember that the only impact to device functional logic reliability is the addition of the 2-to-1 multiplexer in the data path.

Another key factor to consider along with reliability is system availability. A small decrease in system reliability may not be important if system availability increases. Consider a system with a 200-hour MTBF and a repair time of ten hours. The system will have an availability of 1-10/200 = 95 percent. Now consider a more testable system that has a 195-hour MTBF and a repair time of only five hours. The system will have an availability of 1-5/195 = 97.5 percent.

Test Costs

PWB test costs can vary greatly with the complexity and testability of the design. Even simple designs without adequate testability can cause production slowdowns and cost overruns. Production test costs can account for a significant portion of the final product costs. In some businesses, it is estimated that 25% of the product costs result from test costs. Consider the following PWB-production test scenarios. A PWB has an ambiguity group of three high-cost parts using conventional functional-based test techniques. If the failure can be isolated to one device with boundary scan, savings can be realized because several good parts were saved as well as the labor and time required for unnecessary replacement. In another scenario, an hour of technician's labor, including overhead, is $20/hour, and a PWB test requires 10 minutes per PWB, producing 5,000 PWBs/month. If the added testability of IEEE 1149.1 provides a 20% reduction in PWB test times, the production test savings equal $3340 ($20 $\times$ 0.167 $\times$ 5,000 $\times$ 0.2) per month.

System Test

IEEE 1149.1 can also be used for system-level tests. The increased access afforded by the test and boundary scan allow control and observability in a closed system. Tests that previously required physical access using probe clips or extender boards can be performed via the IEEE 1149.1 bus. This reduces faults caused by the additional loading of test probes, electromagnetic interference, and manually-inducted removal and replacement.

PWB-to-PWB Interfaces

Extending the IEEE 1149.1 bus between PWBs can be accomplished by two basic methods: ring and star. The ring configuration allows a simple method to extend the PWB-level scan ring. However, this method has several drawbacks; the scan bus may become very long, which can slow test throughput, and a single-point failure caused by a broken connection or missing PWB will break the scan ring. The ring configuration from PWB-to-PWB interfacing is most practical for a small number of PWBs, typically four or less.

An IEEE 1149.1 star configuration between PWBs allows each PWB scan ring to be addressed without the overhead of additional PWBs in the scan path. However, this method requires additional backplane signals and allows only one PWB at a time to be addressed. Multiple PWBs cannot be scanned simultaneously with a star configuration.

There are several methods to efficiently partition scan rings from PWB to PWB. The simplest solution is to use the 'ACT8997 scan-path linkers or 'ACT8999 scan-path selectors to partition PWB scan rings. These devices allow a complete PWB scan ring to act as one device in bypass mode. This shortens a PWB scan ring to just one bit in the scan path. For more information on using scan-path selectors, see the article *Partitioning Designs With 1149.1 Scan Capabilities*.

Test-Bus Controllers (TBC)

Control of the IEEE 1149.1 test bus for system test can be accomplished via either an external TBC or via an internal embedded TBC. Figure 8 shows an example system with internal and external TBCs. For factory- or maintenance-type testing, a single external TBC will suffice as the IEEE 1149.1 master. Naturally, in this configuration, scan-based test can be performed only under external control.

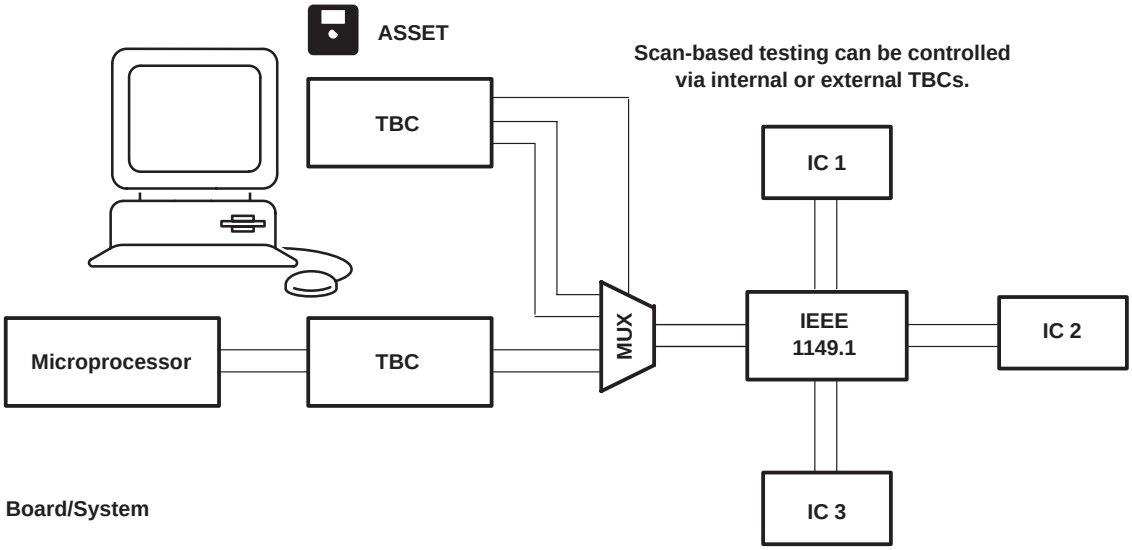


Figure 8. IEEE 1149.1 TBCs

The other option, an embedded TBC, allows autonomous testing under control of the embedded TBC. For small systems (less than four boards), a single TBC may be sufficient to test the system quickly. For larger or more complex systems, multiple TBCs may be required to test the system within an allocated time limit. The actual implementation method depends on the requirements for test execution time, real-estate limits, and fault tolerance.

Conclusion

Considering all the advantages that a standard test-bus and boundary-scan architecture provides, IEEE 1149.1 should be seriously considered as a test solution. While the capabilities gained are not free, the tradeoffs should be investigated. Advantages include increased controllability and observability, test reuse, better fault detection and isolation, and consistent test methods across multiple test environments. Impacts include cost, propagation delay of one 2-to-1 multiplexer in the signal path, and increased gate count for test logic. Although IEEE 1149.1 is suitable for all logic design sizes, implementing IEEE 1149.1 typically is easier to justify on larger designs. In the tradeoff analysis consider hidden costs such as fault-isolation size, test-development time, test-execution time, repair time, and life-cycle repair and maintenance cost. These costs should not be underestimated. Using the capabilities of the IEEE 1149.1, test bus and boundary scan provide advantages that help reduce the total cost of ownership.

Acknowledgment

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