Digital Phase-Locked Loop Design Using SN54/74LS297

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Digital Phase-Locked Loop Design Using SN54/74LS297

Author
Donald G. Troha

Contributors
James D. Gallia
Low Power Schottky Applications Group

INTRODUCTION

Although the concept of the phase-locked loop (PLL) has been in existence for several decades, until recently the PLL function has been implemented by predominantly analog methods. Recent emphasis on digital methods of signal processing has made it desirable to perform the PLL function digitally. For example, the use of a digital phase-locked loop (DPLL) in place of an analog loop in a digital system would eliminate the need for A-to-D and D-to-A conversion.

The SN54/74LS297 described below performs the first-order phase-locked loop function with a high degree of accuracy and a minimum of external components. Features of the 'LS297 DPLL include:

- Entirely digital design
- Accuracy is not affected by temperature and supply voltage variations
- Bandwidth and center frequency are digitally programmable
- Narrow bandwidth (high Q) loops are feasible
- Ripple cancellation features are provided
- Higher order loops can be constructed by cascading.

The divide-by-N counter required by the DPLL is not provided in the 'LS297 package so that the user may choose a counter to meet his specific needs. For example, a divide-by-N counter with parallel outputs provides a direct digital readout of phase error information, while a programmable divide-by-N allows real-time control of loop center frequency. Both Exclusive-OR and edge-triggered phase detectors are provided in the 'LS297. Either phase detector may be used to construct a loop, or the two may be used together in ripple cancellation schemes. The DPLL phase-detector output provides a second means of extracting phase data from the loop in the form of a pulse-width modulated signal.

Although the DPLL and analog PLL perform the phase-locked function by entirely different methods, linear control system models for the loops are analogous, enabling the DPLL user to take advantage of work that has already been done with analog PLLs.

DEVICE DESCRIPTION

As shown in Figure 1, the basic digital phase-locked loop consists of four elements. a phase detector, a K-counter, an increment/decrement circuit, and a divide-by-N counter. With the exception of the divide-by-N counter, these elements are provided in a single 'LS297 package. Two external clocks must be provided to the 'LS297: a K-clock and an I/D-clock. However, in many DPLL applications, the two clocks may be common.

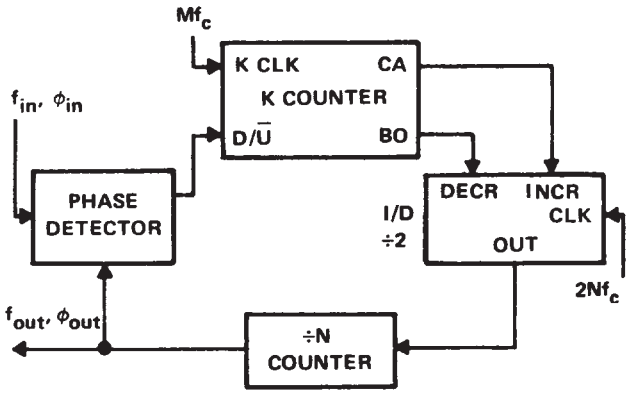


Figure 1. First Order Digital Phase-Locked Loop

As indicated in the data sheet, the phase detector compares the phase of the incoming signal, ϕ_{in}, with the phase of the signal produced by the DPLL, ϕ_{out}, and outputs an error signal, $k_d\phi_e$, where k_d is the gain of the phase detector and ϕ_e is the phase error ($\phi_{in} - \phi_{out}$). Two types of phase detectors are provided with the 'LS297: a conventional Exclusive-OR (EXOR) gate and an edge-

controlled phase detector (ECPD). The ECPD is a flip-flop which functions as follows: A high-to-low transition at ϕ_B will produce a high-level output, while a high-to-low transition at ϕ_{A2} will produce a low-level output. The phase error, ϕ_e, is defined to be zero when the phase detector output has a 50% duty cycle. Figure 2 illustrates that for $\phi_e = 0$, the absolute phase difference between f_{in} and f_{out} is 1/4 cycle for the EXOR case and 1/2 cycle for the ECPD case. The EXOR phase detector has a gain, k_d, of 4 and phase error limit of ±90°. The ECPD has a k_d of 2 and a phase error limit of ±180°.

The K-counter works together with the I/D circuit to produce a signal which is fed back through the divide-by-N counter to the phase detector to be compared with the incoming signal. The K-counter consists of an up-counter, and a down-counter with respective carry and borrow outputs. The D/$\overline{U}$ input to the K-counter controls which half (up or down) of the K-counter is in operation at a particular instant. In a typical DPLL configuration, the output of the phase detector connects to the D/$\overline{U}$ input of the K-counter.

The carry and borrow outputs of the K-counter are internally connected to the increment and decrement inputs of the I/D circuit, respectively, A pulse to the decrement input causes one half-cycle to be deleted from the I/D output, while a pulse to the increment input will result in a half-cycle being added to the I/D output. The I/D circuit produces an output frequency equal to one-half I/D clock when no increment or decrement is in process. This is illustrated in Figure 3.

An example of basic DPLL operation is as follows: If the inputs, f_{in} and f_{out}, to the phase detector are such that the phase detector output is low, then the "up" portion of the K-counter operates, eventually producing a carry pulse. This carry pulse is fed to the increment input of I/D circuit causing one half-cycle to be added to the I/D output. Similarly, a high at the phase detector output enables the "down" portion of the K-counter, eventually producing a borrow pulse to the decrement input which deletes one half-cycle from the I/D output. The DPLL continually adjusts the phase of f_{out} in this fashion so that in the lock condition a definite phase difference will exist between f_{in} and f_{out}.

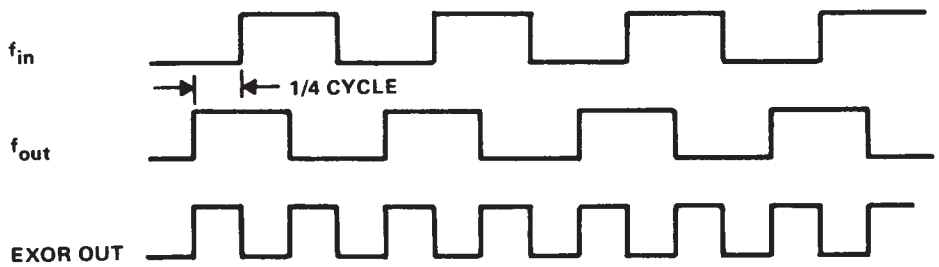
First Order DPLL Equations

The block diagram of a first order digital phase-locked loop is illustrated in Figure 1. The K-clock has a frequency of Mf_c and the I/D-clock has a frequency of $2Nf_c$, where M is a constant, f_c is the loop center frequency, and N is the modulus of the divide-by-N counter. The I/D-clock, frequency and divide-by-N modulus will therefore determine the loop center frequency:

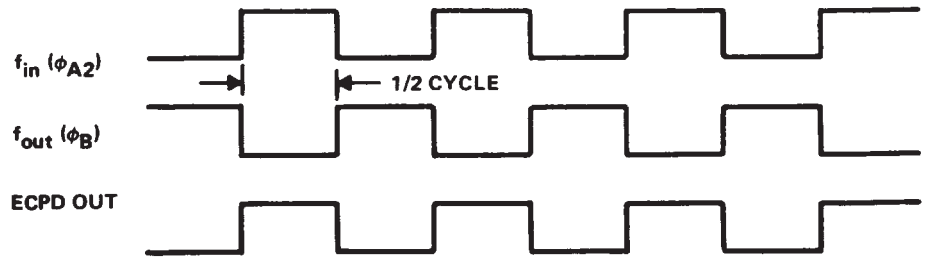
$$f_c = \text{I/D Clock}/2N \quad \text{Hz} \tag{1}$$

From the data sheet, we have expressions for the K-counter and I/D circuit outputs:

$$K_{out} = (k_d \phi_e Mf_c)/K \quad \text{Hz} \tag{2}$$



(a) ϕ_e = 0 USING EXCLUSIVE-OR PHASE DETECTOR



(b) ϕ_e = 0 USING EDGE-TRIGGERED PHASE DETECTOR

Figure 2. Phase Detector Input vs Output with Zero Phase Error

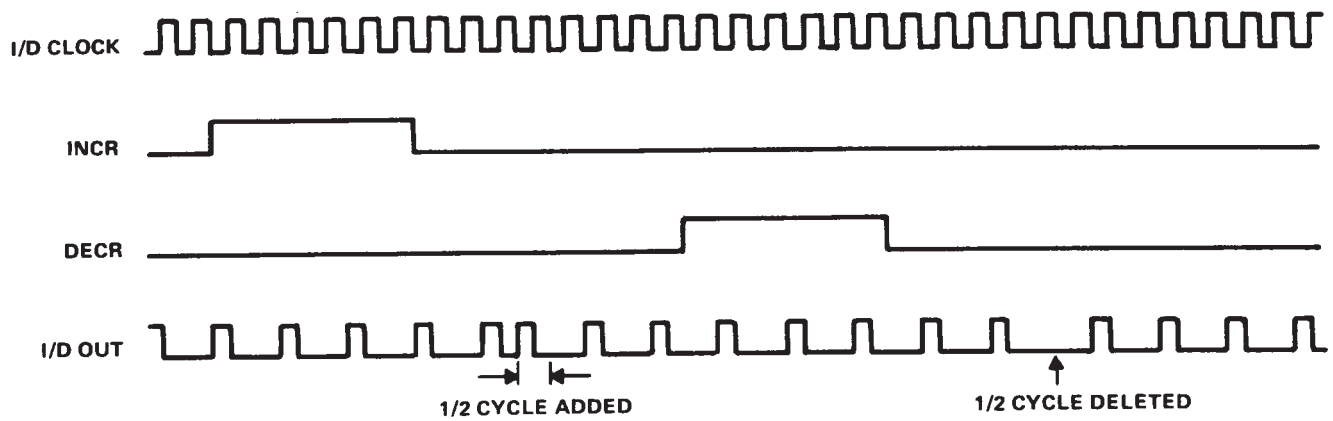


Figure 3. I/D Circuit Waveforms

$$I/D_{out} = Nf_c + (k_d \phi_e Mf_c)/2K \quad Hz \qquad (3)$$

where k_d is the phase detector gain, ϕ_e is the phase error, and K is the modulus of the K-counter.

The loop output is:

$$f_{out} = f_c + (k_d \phi_e Mf_c)/2KN \quad Hz \qquad (4)$$

From this equation we can derive the tracking frequency range Δf_{max}. At the limit of lock range, $k_d \phi_e$ is ±1. Therefore:

$$\Delta f_{max} = (f_{out})_{max} - f_c = Mf_c/2KN \quad Hz \qquad (5)$$

It is evident from the above equation that the lock range of the loop may be adjusted by adjusting K, the modulus of the K-counter.

When the DPLL is in the lock condition, f_{out} equals f_{in}, and a definite phase error, ϕ_e, will exist between the two signals. From equation (4) we obtain:

$$\phi_e = 2KN (f_{in} - f_c)/k_d Mf_c \quad cycles \qquad (6)$$

which is the phase error between f_{in} and f_{out} under lock. This is illustrated in Figure 4. For a phase error of zero, f_{in} must equal the center frequency, f_c.

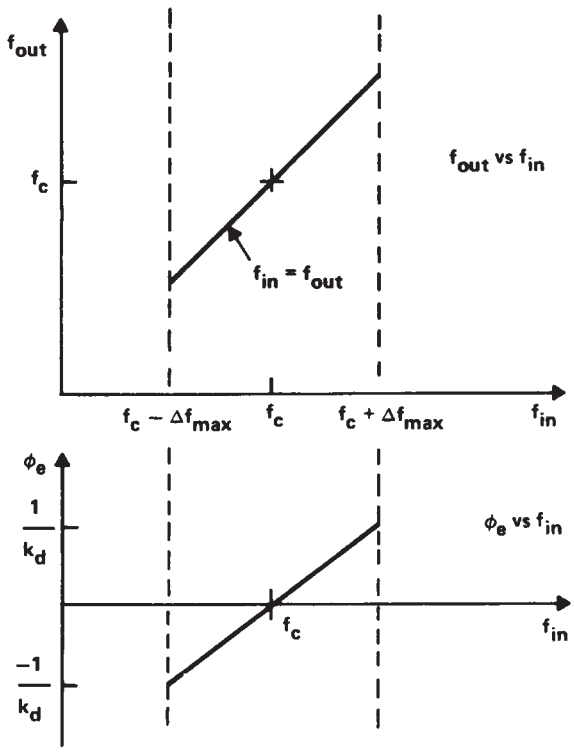


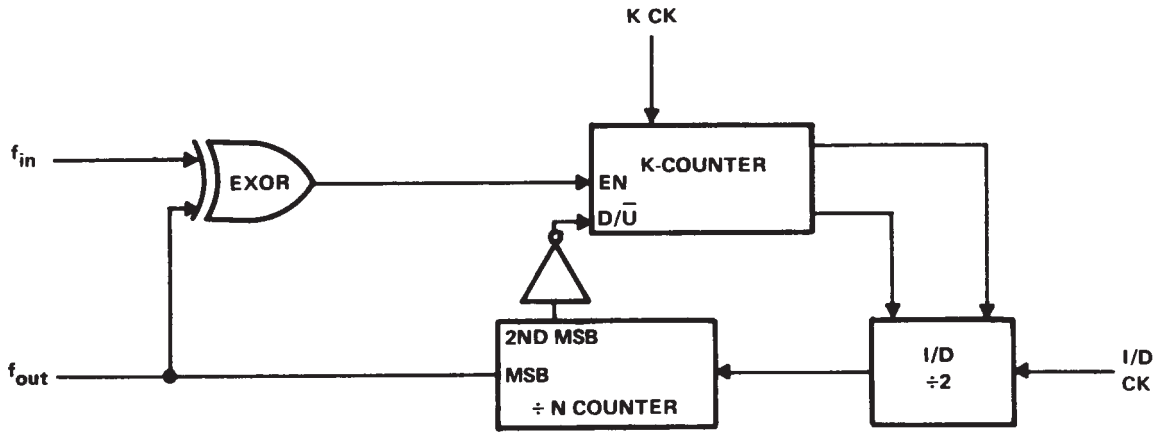
Figure 4. DPLL Transfer Characteristics (in lock)

Ripple Cancellation

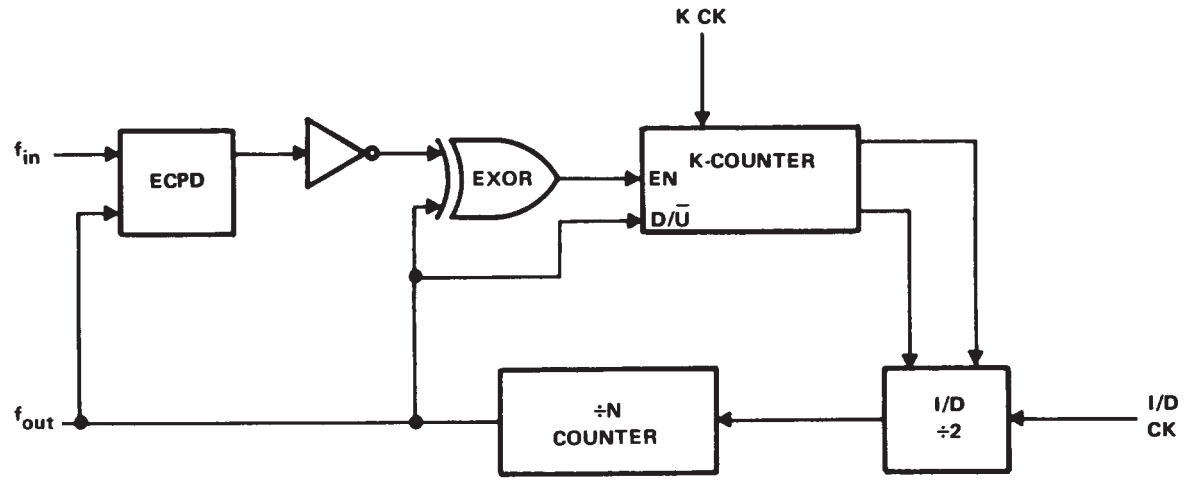
Examining the basic DPLL configuration in Figure 1, we see that the K-counter should continue to function, producing periodic carry and borrow pulses, even if the loop is locked with zero phase error. If K is too small, the K counters will recycle too often, producing repeated carry pulses followed by repeated borrow pulses. This will result in a duty cycle error called ripple in the DPLL output. This ripple may be reduced to a value of 1/N cycles at the divide-by-N counter output by making K sufficiently large, specifically K > M/4 for DPLL circuits utilizing the EXOR phase detector and K > M/2 for ECPD circuits, so that the phase correction pulses will cancel in the lower order bits of the divide-by-N counter.

Alternatively, one of the ripple cancellation circuits shown in Figure 5 may be used to minimize ripple. When either of these schemes is implemented, the K-counter is disabled when the DPLL is in a lock condition with zero phase error. While these circuits act to minimize ripple, they also have the effect of narrowing the lock range of the loop. The loop phase error limit (±90° for EXOR DPLLs and ±180° for ECPD DPLLs) is reduced by a factor of 1/(1 + 1/2K), and the phase detector gain, k_d is reduced by 1/2. This results in an adjusted lock range of:

$$\Delta f_{max} = Mf_c/(1 + 1/2K)\, 4KN \quad Hz \qquad (7)$$



(a) RIPPLE CANCELLATION WITH EXOR PHASE DETECTOR



(b) RIPPLE CANCELLATION WITH ECPD

Figure 5. Ripple Cancellation Circuits

Loop Transfer Functions and Q-Factor

In the lock condition, the DPLL simulates a linear control system analogous to a first order analog phase-locked loop, (Figure 6). The K-counter of the DPLL acts as an integrator in this system. From Figure 6 the open loop transfer function G(s) can be written:

$$G(s) = k_V/s \tag{8}$$

where k_V is the total loop gain:

$$k_V = k_d\, Mf_c/2KN \quad \text{rad/s} \tag{9}$$

The closed loop transfer function is thus:

$$H(s) = k_V/(s + k_V) \tag{10}$$

The 3-dB bandwidth, $\omega_{3\ dB}$, is therefore equal to k_V, the total loop gain.

The digital phase-lock loop may be thought of as a filter because it filters out high frequency phase changes from the input signal. Conventional filters are characterized by a quality factor "Q," which relates filter bandwidth and center frequency. The Q of a DPLL is similarly defined:

$$Q = \omega_c/2\omega_{3\ dB} = 2\,\pi\, KN/k_d\, M \tag{11}$$

If the K-clock and I/D-clock are common (M = 2N), the expression for Q simplifies to:

$$Q = \pi\, K/k_d \tag{12}$$

Since K can be programmed to a value of 2^3 to 2^{17}, a common clock, first order, DPLL can have a Q ranging from 6 to over 205,000.

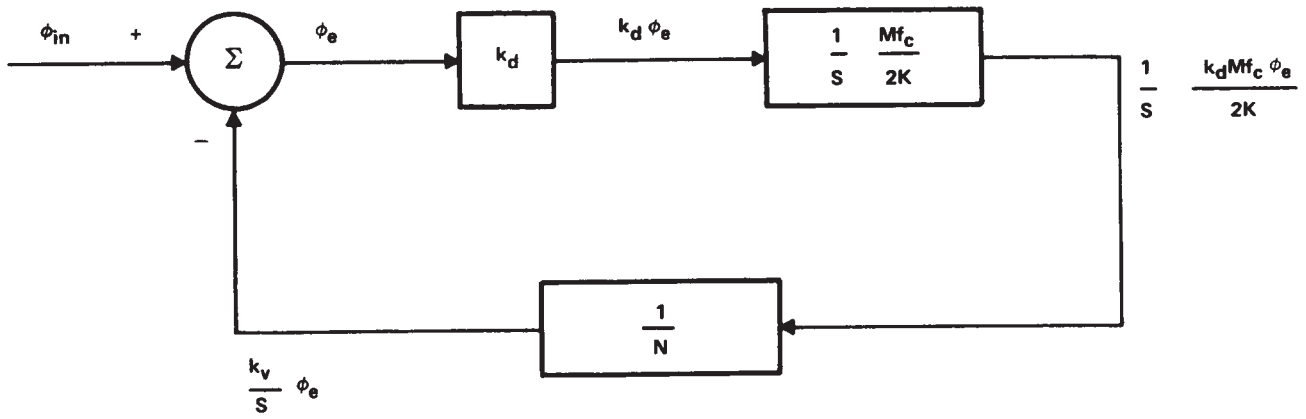


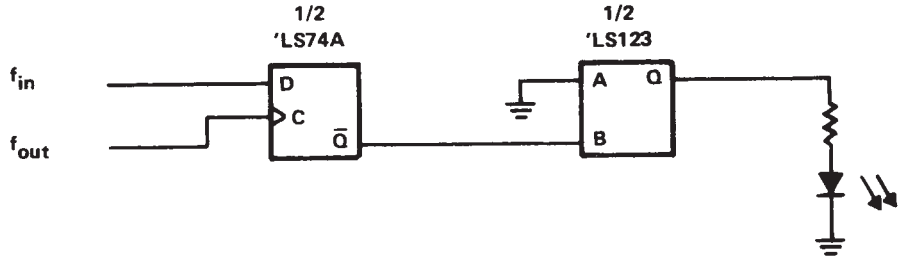
Figure 6. Linear Control System Representation of First Order DPLL

DPLL CIRCUIT IMPLEMENTATIONS AND APPLICATIONS

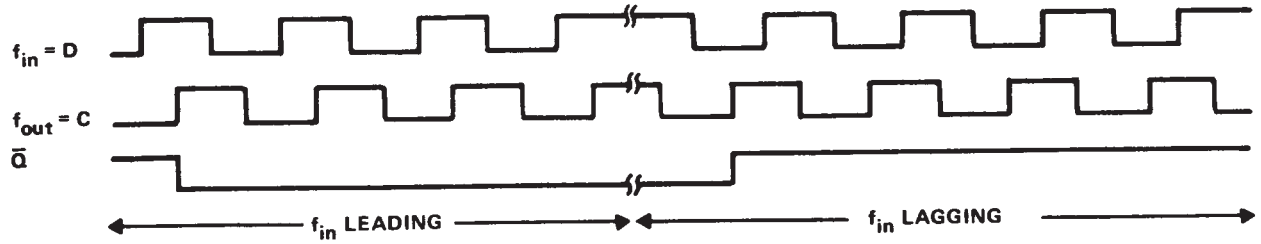
Lock Detection

Figure 7(a) illustrates a simple lock detection circuit which can be built with a D-type flip-flop and a monostable multivibrator. Waveforms in Figure 7(b) illustrate that if the DPLL is in lock, $\overline{Q}$ from the D flip-flop will be either high or low, depending on the phase difference between f_{in} and f_{out}. The result is that the monostable does not fire, and the LED does not light up. An out-of-lock condition is illustrated in Figure 7(c). In this condition, the D flip-flop will output a series of pulses which will repeatedly fire the monostable and light the LED.

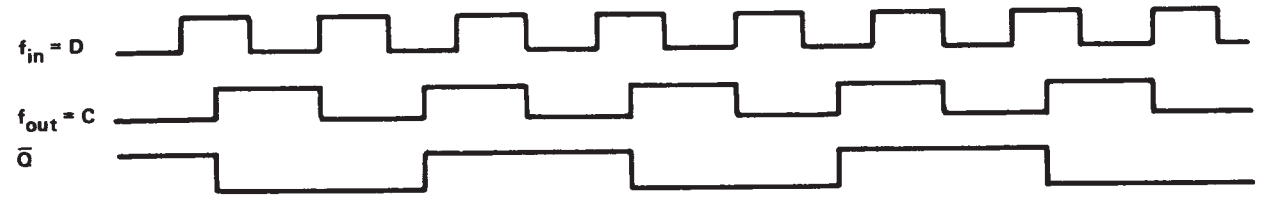
In ECPD DPLL circuits, this lock detection circuit works well for all frequencies within the lock range except at $f_{in} = f_c$. If f_{in} varies around f_c, a false out-of-lock indication will result. This circuit works at all frequencies within the lock range of EXOR phase detector loops.



(a) LOCK DETECTION CIRCUIT



(b) LOCK CONDITION WAVEFORMS

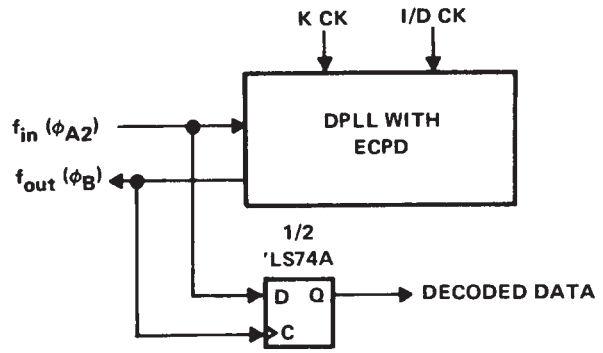


(c) OUT-OF-LOCK WAVEFORMS

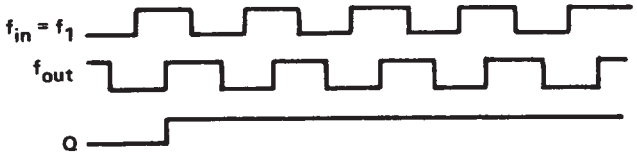
Figure 7. Lock Detection Circuit and Waveforms

FSK Decoding

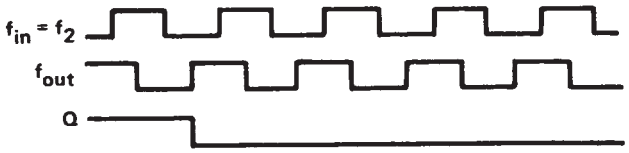
A DPLL with edge-triggered phase detection and a single D-type flip-flop can be used to decode FSK signals, (Figure 8). For example, suppose we have a signal f_{in} which alternates between two frequencies f_1 and f_2. The center frequency f_c should be chosen such that $f_1 < f_c < f_2$. If the incoming signal f_{in} is equal to f_1, a negative phase error ϕ_e will result (f_{in} lags f_{out}), and a "1" will be latched into the D flip-flop. Likewise, if $f_{in} = f_2$, ϕ_e will be positive (f_{in} leads f_{out}), and a "0" will be latched into the D flip-flop.



(a) FSK DECODER CIRCUIT



(b) $f_{in} = f_1$ LOCKS Q HIGH



(c) $f_{in} = f_2$ LOCKS Q LOW

Figure 8. FSK Decoder and Waveforms

DPLL with Parallel Readout of Phase Data

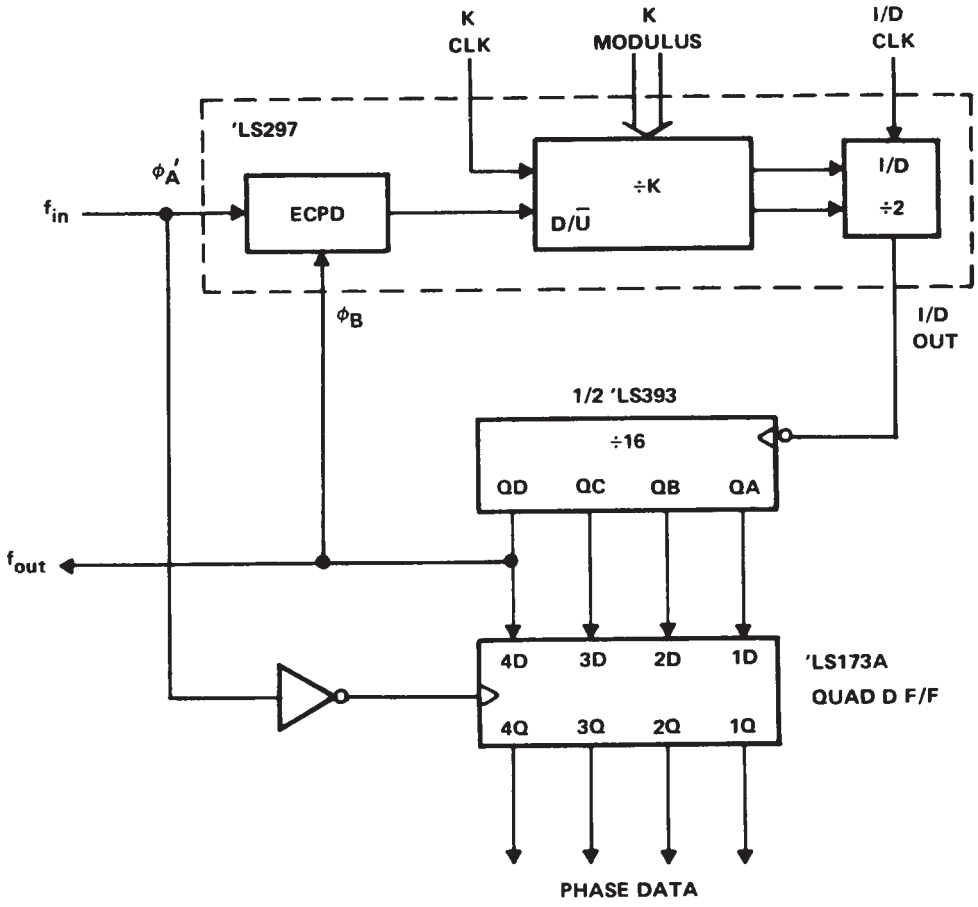
The concept used to implement the FSK decoder can be extended to perform direct readout of phase error information. When a DPLL is in lock, a definite phase error will exist between f_{in} and f_{out} and any intermediate stage of the divide-by- N counter. If a divide-by-N counter with parallel outputs is incorporated into the phase-locked loop, the phase error information can be latched into a bank of registers by f_{in}. An example of a circuit which accomplishes this is illustrated in Figure 9(a). This circuit latches the four outputs of the divide-by-N (n = 16) counter on a falling edge of f_{in} into a 4-bit register. The falling edge is used as the strobe because ECPD measures phase error by comparing falling edges of f_{in} and f_{out}. The output of the register can then be decoded to give the phase error, ϕ_e, from which the input frequency can be calculated. Because ϕ_e is defined to be zero when f_{in} and f_{out} are one-half cycle out of phase, the absolute phase difference between f_{in} and f_{out} will always differ from the phase error, ϕ_e, by one-half cycle. For example, in Figure 9(b), f_{in} is leading f_{out} by between 7/8 and 15/16 cycle, but the phase error, ϕ_e, is actually between 3/8 and 7/16 cycle. When f_{in} goes from high to low, the outputs of the divide-by-16 counter are latched into the register, giving a register reading of LLLH. In Figure 9(c), f_{in} is leading f_{out} by 7/16 to 1/2 cycle, and ϕ_e is in the 0 to $-1/16$ range. In this case, the register reading is HLLL.

Table I lists all possible register readings for circuit in Figure 9(a) along with phase error values and absolute phase difference values. The absolute phase difference is the fraction of a cycle by which f_{in} leads f_{out}, and the phase error, ϕ_e, is the absolute phase difference minus one-half cycle. The register output may be related to the absolute difference between f_{in} and f_{out} by considering the register output to be an inverted data binary fraction expression for the absolute phase difference. The phase error, ϕ_e, may thus be computed by inverting the bits of the output register to obtain a binary fraction reading of the absolute phase difference, then subtracting a binary one-half. The computed phase error could then be used in Eq. (6) to compute the input frequency f_{in}.

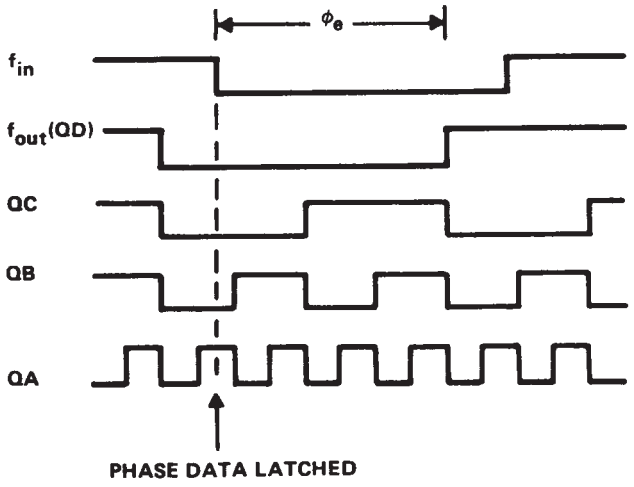
A higher degree of accuracy may be attained by adding more stages to the divide-by-N counter and register. To minimize error due to ripple, more counter stages could be placed between the I/D circuit and the parallel output counter. This circuit could be used for FM demodulation.

Table 1. Register Output vs Phase Error

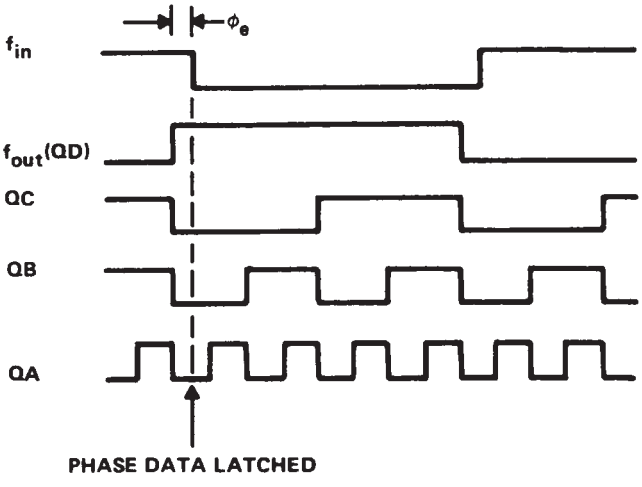
Absolute Phase Difference (Cycles)	Register Output 4Q	3Q	2Q	1Q	ϕ_e (Cycles)
15/16 to 1	L	L	L	L	7/16 to 1/2
7/8 to 15/16	L	L	L	H	3/8 to 7/16
13/16 to 7/8	L	L	H	L	5/16 to 3/8
3/4 to 13/16	L	L	H	H	1/4 to 5/16
11/16 to 3/4	L	H	L	L	3/16 to 1/4
5/8 to 11/16	L	H	L	H	1/8 to 3/16
9/16 to 5/8	L	H	H	L	1/16 to 1/8
1/2 to 9/16	L	H	H	H	0 to 1/16
7/16 to 1/2	H	L	L	L	−1/16 to 0
3/8 to 7/16	H	L	L	H	−1/8 to −1/16
5/16 to 3/8	H	L	H	L	−3/16 to −1/8
1/4 to 5/16	H	L	H	H	−1/4 to −3/16
3/16 to 1/4	H	H	L	L	−5/16 to −1/4
1/8 to 3/16	H	H	L	H	−3/8 to −5/16
1/16 to 1/8	H	H	H	L	−7/16 to −3/8
0 to 1/16	H	H	H	H	−1/2 to −7/16



(a) CIRCUIT DIAGRAM



(b) A PHASE ERROR OF BETWEEN 3/8 AND 7/16 CYCLE LATCHES LLLH INTO THE D FLIP-FLOPS



(c) A PHASE ERROR OF 0 to −1/16 CYCLE LATCHES HLLL INTO THE D FLIP-FLOPS

Figure 9. DPLL with Latched Phase Data

DPLL with Real-Time Control of Lock Range and Center Frequency

Figure 10 suggests a method for constructing a DPLL with lock range and center frequency controlled dynamically by a microprocessor. In this circuit, the divide-by-N counter is split between a parallel output counter with direct readout of phase data and a programmable counter for controlling the loop center frequency. Here, the use of the SN54/74LS292/4 is suggested as the programmable portion of the divide-by-N counter.

As an application for this circuit, consider an input signal, f_{in}, to be demodulated by the DPLL, which can take on any one of several frequencies within a certain band. An out-of-lock condition indicated by the lock detector tells the microprocessor to widen the DPLL lock range by decreasing the K-counter modulus. When a lock condition is reached, the processor reads the phase error, ϕ_e, from the divide-by-N counter latch and adjusts the loop center frequency by changing the modulus of the programmable counter until a minimum phase error is reached. The processor can then reduce the loop lock range to the desired level by increasing the K-counter modulus.

Phase Demodulation

Figure 11 illustrates a DPLL circuit used to demodulate a constant frequency, phase-modulated input signal. The loop center frequency, f_c, is chosen to be equal to incoming frequency. Phase changes in the input signal may be detected by latching the contents of the divide-by-N counter with a strobe of constant phase, and constant frequency, f_c. For an

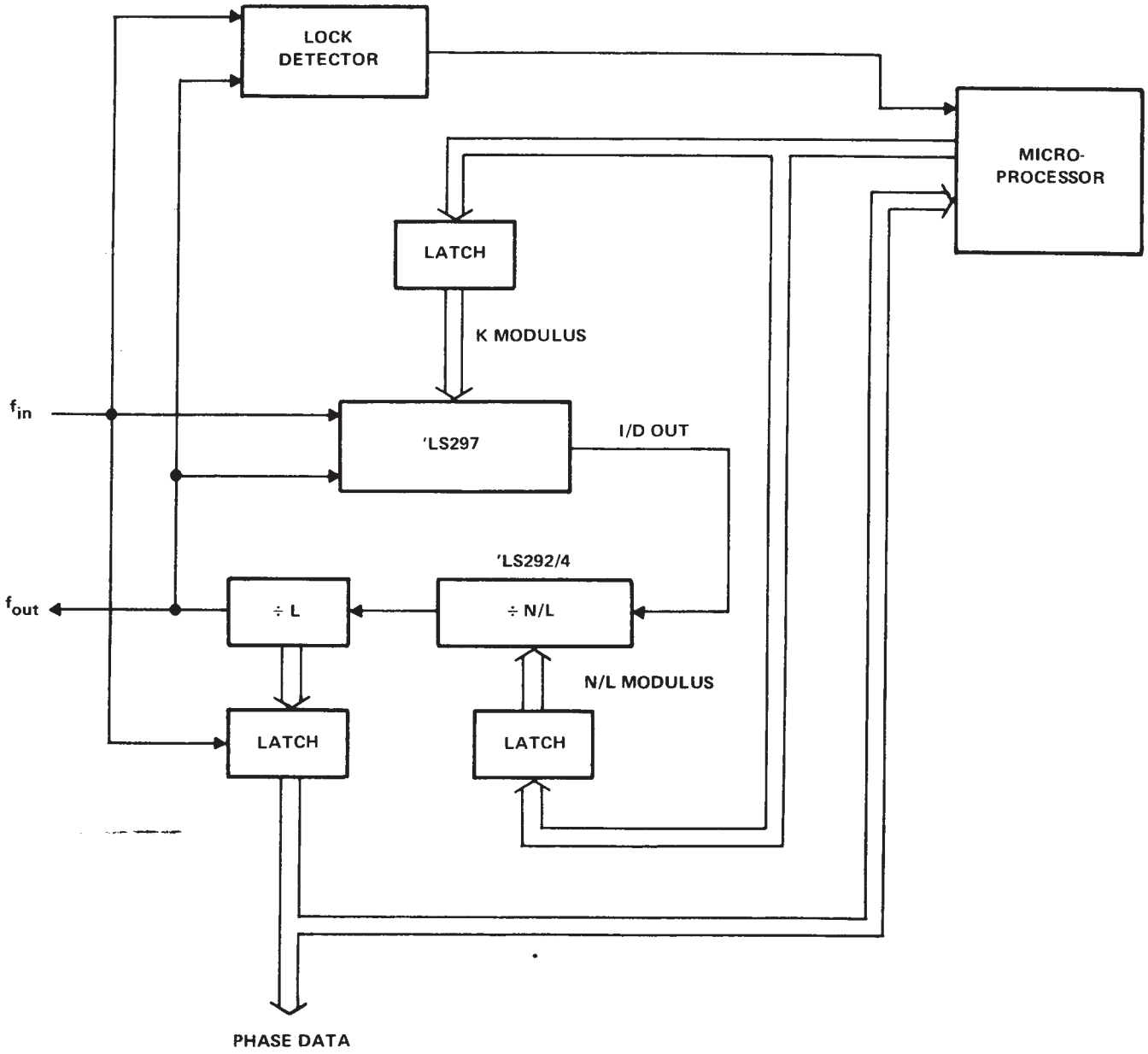


Figure 10. DPLL with Microprocessor Control of Bandwidth and Center Frequency

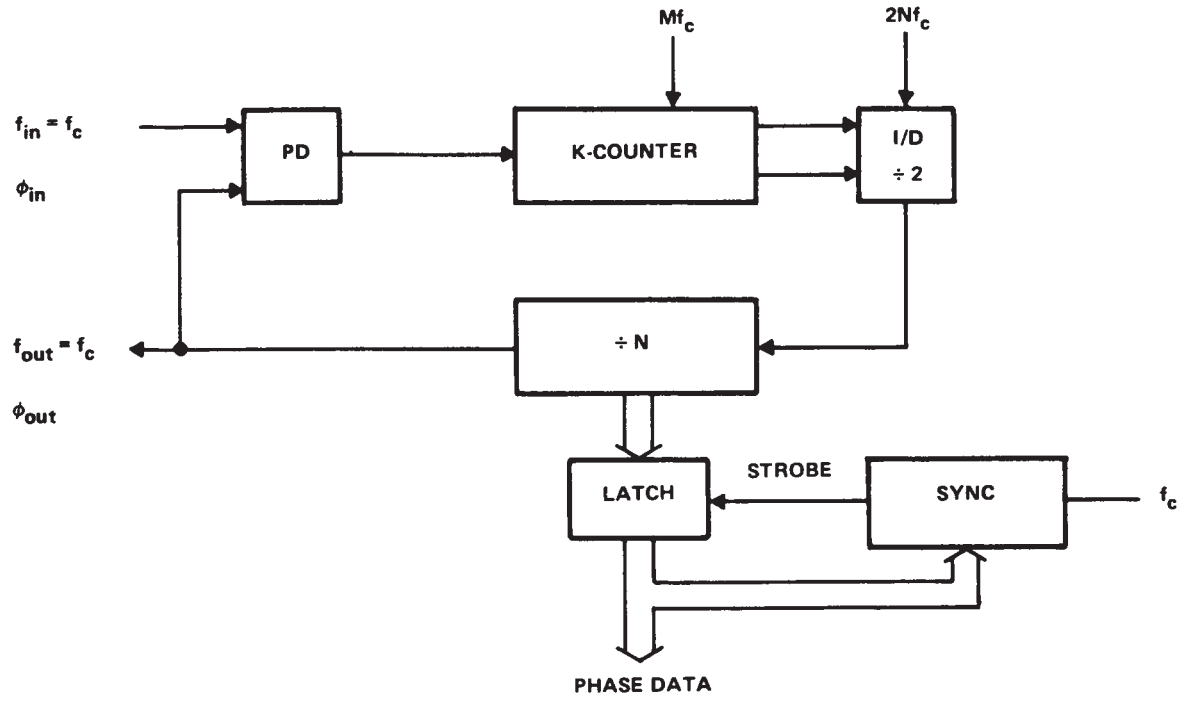


Figure 11. Phase-Shift Demodulator

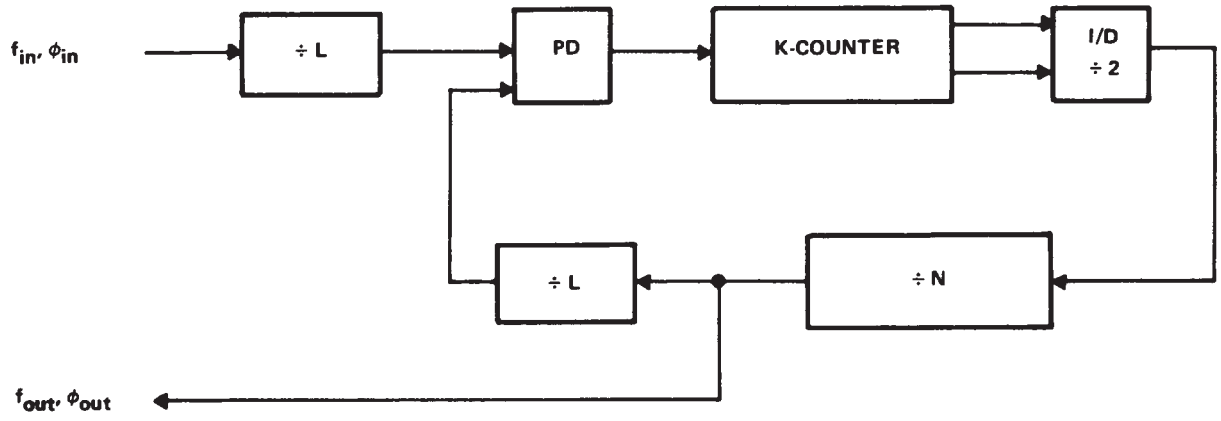


Figure 12. Lock Range Extension

accurate digital readout of phase data, some synchronizing circuitry will be required to synchronize the phase of the latch strobe with the phase of the incoming signal. Reference 4 elaborates on the use of this method of phase demodulation in Omega receivers.

Lock Range Extension

By placing counters of equal modulo (L) on each of the two phase detector inputs as shown in Figure 12, the DPLL 3-dB bandwidth as given by Eq. (9) is decreased by the factor L. In order to obtain the same 3-dB bandwidth as a loop without the divide-by-L counters, the K-counter modulus must be decreased by a factor of L. This has the effect of widening the loop lock range as given by Eq. (5).

'LS297 CLOCK SYNCHRONIZER FOR TMS 9909 FLOPPY DISK CONTROLLER

The floppy disk (Figure 13) puts out read data at 250 kbits/s but it is a nonperiodic waveform. A logical one is presented as two pulses at 2-μs separation while a logical zero is two pulses 4 μs apart. Other control signals are 1 μs apart. The TMS 9909 requires the reconstructed data baseline frequency in order to synchronize and properly control the floppy disk. The 'LS297 is used in this application to solve this classic phase-locked loop problem of extracting a frequency baseline from a nonperiodic waveform. (The baseline frequency happens to be 1 MHz in this application.)

To minimize phase-lock jitter and to increase the lock range, the 'LS122 is used to stretch the typical 200 ns read data pulses to 500 ns. The 'LS297 is operated at maximum K-clock and I/D clock frequencies to further minimize the output jitter. ($\overline{RKM}$ input or the 1 MHz DPLL output has jitter equal to ± 1 μs divided by the ratio of the I/D clock frequency to the 1 MHz $\overline{RKM}$ frequency. This equals to ± 1 μs divided by 15 or ± 66.7 ns.)

SN54/74LS297 FIRST-ORDER DPLL LOCK TEST DATA

Tables 2, 3, 4, and 5* present 'LS297 lock test data taken for the circuits in Figures 1 and 5. The input signal, f_{in}, was supplied by a frequency synthesizer with microhertz resolution. The output signal f_{out}, was monitored by a frequency counter which also had microhertz accuracy. The 'LS297 I/D clock and K-clock inputs were driven by a 10.000 000 000 MHz crystal-controlled clock. The divide-by-N modulus was set at 256, and the K-counter modulus was varied as listed in the tables.

*Reprinted from Ref. 5.

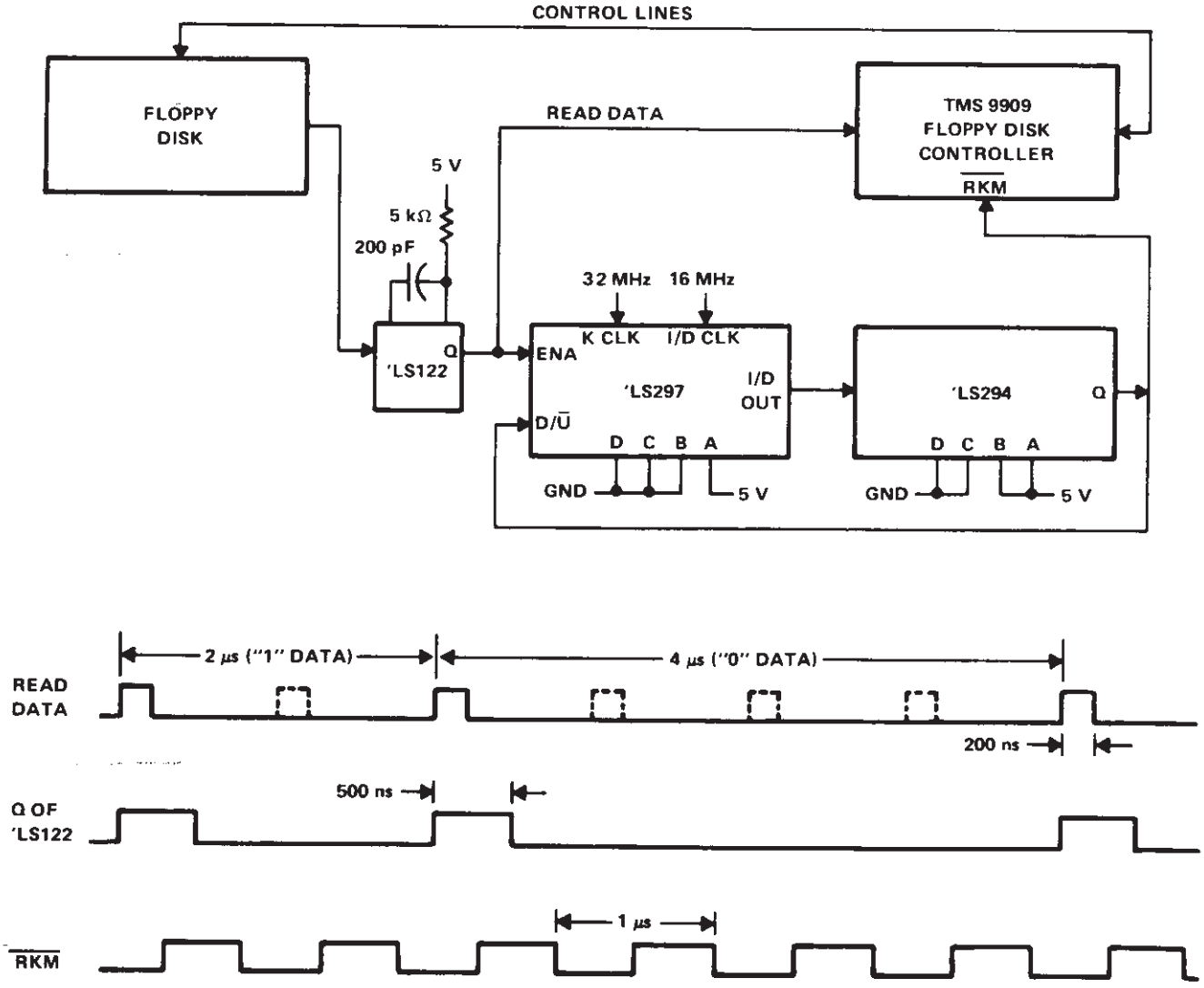


Figure 13. Floppy Disk Controller Application

Table 2. 'LS297 Phase Lock Test Data — EXOR Phase Detector DPLL Circuit [Figure 1] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	6.3	±0.70	19.07	90 ± 89.3	2422.33276	21953.58276	17108.91724	8/N
2^5	25.1	±0.70	4.76	90 ± 89.3	605.58319	20136.83319	18925.66681	2/N
2^7	100.5	±0.70	1.19	90 ± 89.3	151.39579	19682.64580	19379.85420	1/N
2^9	402.1	±0.70	2.98×10^{-1}	90 ± 89.3	37.84894	19569.09895	19493.40105	1/N
2^{11}	1608.5	±0.70	7.45×10^{-2}	90 ± 89.3	9.46223	19540.71224	19521.78776	1/N
2^{13}	6434	±0.70	1.86×10^{-2}	90 ± 89.3	2.36555	19533.61556	19528.88444	1/N
2^{15}	25736	±0.70	4.65×10^{-3}	90 ± 89.3	0.59138	19531.84139	19530.65861	1/N
2^{17}	102944	±0.70	1.16×10^{-3}	90 ± 89.3	0.14784	19531.39785	19531.10215	1/N

Table 3. 'LS297 Phase Lock Test Data — Edge Controlled Phase Detector DPLL Circuit [Figure 1] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	12.6	±0.70	9.53	180 ± 177.9	2412.79602	21953.58276	17118.45398	16/N
2^5	50.3	±0.70	2.38	180 ± 177.9	603.19900	20136.83319	18928.05099	4/N
2^7	201.1	±0.70	5.96×10^{-1}	180 ± 177.9	150.79975	19682.64580	19380.45025	1/N
2^9	804.2	±0.70	1.49×10^{-1}	180 ± 177.9	37.69993	19569.09895	19493.55006	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	180 ± 177.9	9.42498	19540.71224	19521.82502	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	180 ± 177.9	2.35624	19533.61556	19528.89375	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	180 ± 177.9	0.58906	19531.84139	19530.66094	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	180 ± 177.9	0.14726	19531.39785	19531.10273	1/N

Table 4. 'LS297 Phase Lock Test Data — EXOR Ripple Cancellation DPLL Circuit [Figure 5(a)] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	ϕ_E max Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	f_{OUT} max Maximum Lock Frequency (Hz)	f_{OUT} min Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	12.6	±0.70	9.53	0 ± 84.0	1139.36031	20670.61032	18320.08362	1/N
2^5	50.3	±0.70	2.38	0 ± 87.9	298.09658	19829.34658	19228.45840	1/N
2^7	201.1	±0.70	5.96×10^{-1}	0 ± 88.9	75.40103	19606.65110	19455.55210	1/N
2^9	804.2	±0.70	1.49×10^{-1}	0 ± 89.3	18.92447	19550.17447	19512.32553	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	0 ± 89.3	4.73111	19535.98112	19526.51888	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	0 ± 89.3	1.18277	19532.43278	19530.06722	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	0 ± 89.3	0.29569	19531.54569	19530.95431	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	0 ± 89.3	0.07923	19531.32392	19531.17608	1/N

Table 5. 'LS297 Phase Lock Test Data — Edge Controlled Ripple Cancellation DPLL Circuit [Figure 5(b)] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	ϕ_E max Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	f_{OUT} max Maximum Lock Frequency (Hz)	f_{OUT} min Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	25.1	±0.70	4.76	180 ± 168.0	1139.36031	20670.61032	18320.08362	1/N
2^5	100.5	±0.70	1.19	180 ± 175.9	298.09658	19829.34658	19228.45840	1/N
2^7	402.1	±0.70	2.9×10^{-1}	180 ± 177.9	75.40103	19606.65110	19455.55210	1/N
2^9	1608.5	±0.70	7.4×10^{-2}	180 ± 178.6	18.92447	19550.17447	19512.32553	1/N
2^{11}	6434	±0.70	1.8×10^{-2}	180 ± 178.6	4.73111	19535.98112	19526.51888	1/N
2^{13}	25736	±0.70	4.6×10^{-3}	180 ± 178.6	1.18277	19532.43278	19530.06722	1/N
2^{15}	102944	±0.70	1.2×10^{-3}	180 ± 178.6	0.29569	19531.54569	19530.95431	1/N
2^{17}	411774	±0.70	2.9×10^{-4}	180 ± 178.6	0.07923	19531.32392	19531.17608	1/N

Calculated values for Q are listed in the tables along with measured values of phase error resolution; frequency resolution, Δf; phase error range; frequency lock range; maximum and minimum lock frequencies; and ripple. Phase error resolution, and frequency resolution can be best understood by recalling that the phase of the I/D circuit output is adjusted by half-cycles. This means that the phase of the output signal, f_{out}, will have an uncertainty or resolution of $\pm 1/2N$ cycles. For the data presented, N was set at 256, giving a phase resolution, $\Delta\phi$, of ± 0.70 degrees. For a $\pm 1/2N$ phase resolution, Eq. (4) implies that the output frequency will have an uncertainty Δf of

$$\Delta f = \Delta\phi\, k_d\, Mf_c/2KN \quad Hz$$
$$= k_d\, Mf_c/4KN^2 \quad Hz \qquad (13)$$

For common clock circuits (M = 2N), the expression simplifies to:

$$\Delta f = k_d\, f_c/2KN \quad Hz \qquad (14)$$

The phase error lock range data in Tables 2, 3, 4, and 5 indicate that the lock ranges were reduced from the theoretical limits by the phase resolution factor $1/2N$ and loop propagation delays along with the factor of $1/(1 + 1/2K)$ mentioned earlier for ripple cancellation circuits. The lock frequency range, and minimum and maximum lock frequency data from the tables can be compared to theoretical limits expressed by Eq. (5) and Eq. (7).

DESIGN CONSIDERATIONS

The design of a first-order DPLL can be simplified by considering a few points. Having a common clock for the K-counter and I/D circuits simplifies calculations. However, making the K-clock higher in frequency than the I/D clock has the effect of widening the loop lock range, and vice versa. The phase detector should be chosen according to the input signal characteristics. The EXOR phase detector requires square wave inputs but is less sensitive to noise than the ECPD. The ECPD, while being more sensitive to the effects of noise, has a wider phase-error range, and has no duty cycle requirements. Recalling that the DPLL output frequency has a phase resolution of $\pm 1/2N$ cycles, the modulus (N) of the divide-by-N counter should be chosen such that phase resolution requirements are met.

Once the center frequency, lock range, phase detector, and divide-by-N modulus have been chosen, Eq. (1) yields the required clock frequency, and Eq. (5) yields the required K-counter modulus. Note that the loop lock range may have to be altered in order to set K equal to a power of two. Also note that setting the clocks equal (M = 2N) constrains the lock range to a maximum value of $\pm f_c/8$. If the chosen settings for M and K do not satisfy the ripple inequalities presented earlier ($K > M/4$ for EXOR, and $K > M/2$ for ECPD), the output signal will exhibit ripple. If such is the case, the user may elect to adjust M or K, or use a ripple cancellation circuit.

HIGHER ORDER DIGITAL PHASE-LOCKED LOOPS

A higher order analog PLL is typically constructed by inserting a filter in the PLL feedback loop. Higher order DPLLs can be constructed by cascading 'LS297 devices. An example of a second-order DPLL circuit configuration is illustrated in Figure 14, along with its associated control system representation.

The circuit shown in Figure 14(a) is composed of two first-order DPLLs which have been labeled Loop 1 and Loop 2. The overall DPLL center frequency and the Loop 2 center frequency are determined by the Loop 2 I/D clock. Since the Loop 1 I/D clock is connected to the I/D output of Loop 2, the Loop 1 center frequency will be determined by the frequency of the Loop 2 I/D output. A close inspection of Figure 14(a) reveals that if both loops are locked, the Loop 1 center frequency will be equal to the incoming frequency, f_{in}. This means the second-order DPLL will track its incoming signal with zero phase error within its lock range. The second-order DPLL lock range is determined by Loop 2:

$$\Delta f_{max} = \frac{Mf_c}{4K_2N} \quad Hz \qquad (15)$$

The phase error ϕ_e, in Loop 2 is proportional to the difference in frequency between f_{in} and f_c:

$$(f_{in} - f_c) = \frac{k_{d2}\, Mf_c}{4K_2N}\ \phi_e \quad Hz \qquad (16)$$

Frequency offset data may therefore be obtained by latching the contents of the Loop 2 feedback counter as described earlier for first-order DPLLs.

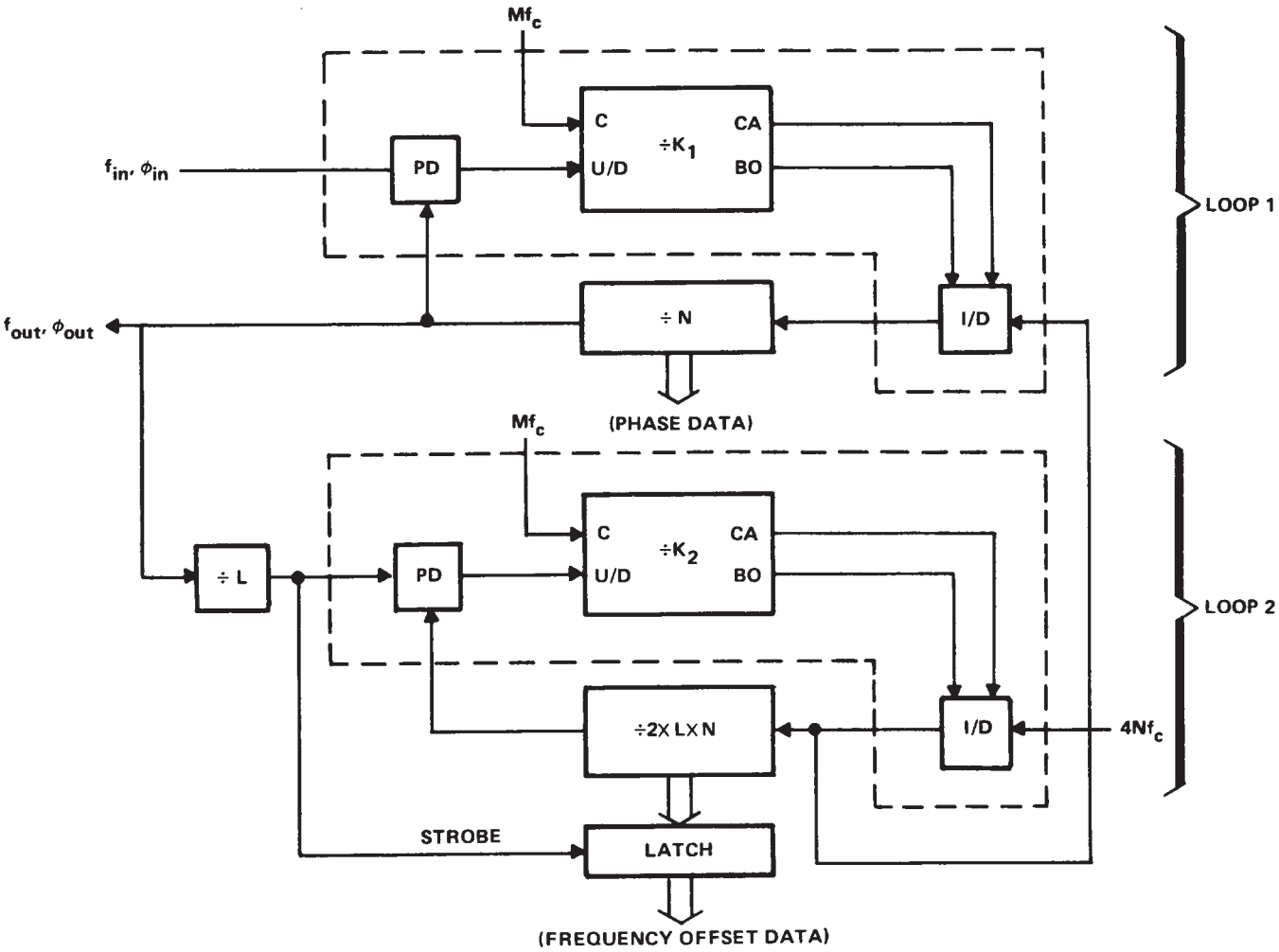
The transfer function for this loop can be shown to be:

$$H(S) = \frac{\phi_{out}(S)}{\phi_{in}(S)} = \frac{\omega_1 S + \omega_1\omega_2}{S^2 + \omega_1 S + \omega_1\omega_2} \qquad (17)$$

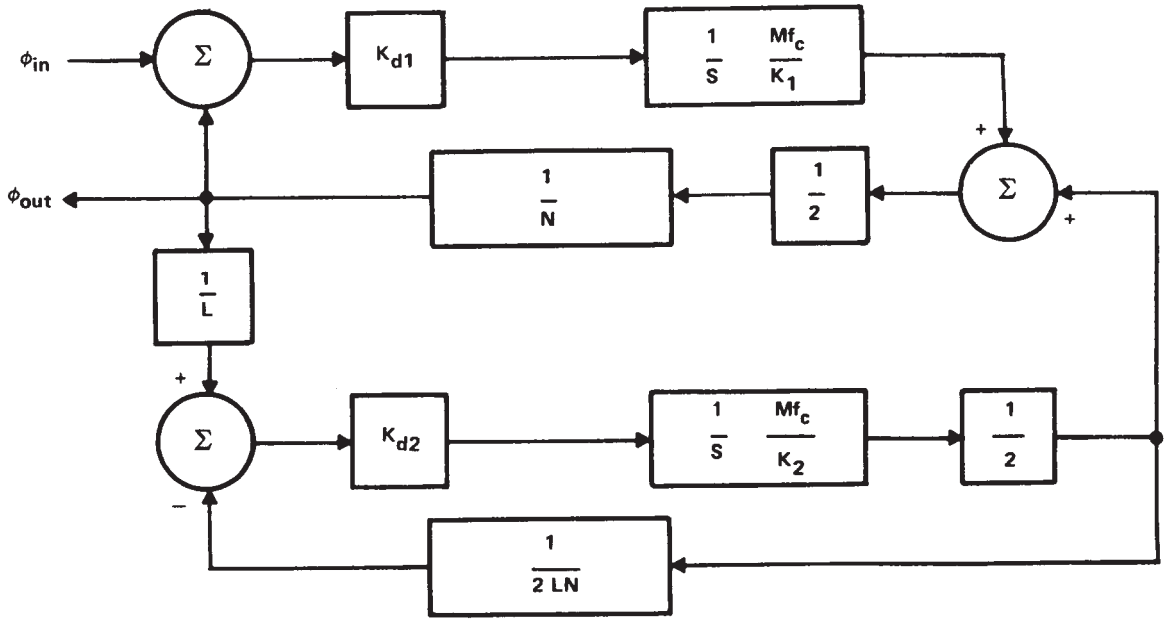
where ω_1 and ω_2 are defined:

$$\omega_1 = \frac{k_{d1}\, Mf_c}{2K_1N} \quad rad/s \qquad (18)$$

$$\omega_2 = \frac{k_{d2}\, Mf_c}{4K_2LN} \quad rad/s \qquad (19)$$



(a) BLOCK DIAGRAM



(b) CONTROL SYSTEM REPRESENTATION

Figure 14. Second Order DPLL

This can be compared to the general equation for a second-order, active filter analog PLL:

$$H(S) = \frac{\phi_{out}}{\phi_{in}} = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \quad (20)$$

where ω_n is the loop natural frequency and ζ is the damping factor. By equating (17) and (20), expressions for the natural frequency and damping factor of a second-order DPLL can be obtained:

$$\omega_n = (\omega_1\omega_2)^{1/2} \quad \text{rad/s} \quad (21)$$

$$\zeta = \frac{1}{2}(\omega_1/\omega_2)^{1/2} \quad (22)$$

Some of the effects of natural frequency and damping factor on loop performance have been presented in Reference 3.

Higher order DPLLs may be constructed in a similar manner by cascading.

SUMMARY

The operation of the 'LS297 has been presented as a basic building block in a digital phase-locked loop along with some ideas of how to extract phase data from the DPLL. A first-order DPLL may be constructed with one 'LS297 device, an external feedback counter, and an external clock. The accuracy of the DPLL is dependent upon the accuracy of the loop clocks, and loop center frequency and lock range are digitally programmable. A direct digital readout of phase information can be made available by latching the contents of the DPLL divide-by-N counter with a strobe of appropriate phase and frequency. Possible applications for the 'LS297 include motor speed control, noise filtering, tone recognition, data synchronization, frequency synchronization and multiplication, and position indicators, along with frequency and phase demodulation suggested earlier. The versatility of the DPLL can be greatly enhanced by the use of microprocessor control of lock range and center frequency.

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