

# Solving Enumeration Errors in USB Audio DAC and CODEC Designs

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## ABSTRACT

TI's portfolio of audio digital-to-analog converters (DACs) and coder/decoders (codecs) with integrated USB interfaces offers an excellent building block for any streaming USB audio system. When designing with the [PCM270x](#) and [PCM29xx](#) devices, careful attention must be given to both the clocking and USB hardware configurations in order to ensure proper host to device communication.

This application report outlines two common design mistakes that can lead to enumeration errors between the host and device. Concise descriptions are provided to help diagnose and correct enumeration errors so that designers can move forward with the overall system architecture process.

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## 1 Enumeration

*Enumeration* is the process by which a system host determines the operating characteristics of a device that is connected to that USB host. For the PCM270x stereo audio DACs and PCM29xx stereo audio codecs, these characteristics include the connected device USB version compatibility, class, end points, and power-supply requirements. (For a more thorough description of the information stored in the device, configuration, and string descriptors, see the USB Interface section of the respective device data sheet.) After these parameters have been exchanged, a communication address for the device will be determined and used for data transfer via the bus.

## 1.1 Hardware Considerations for Enumeration

Although the enumeration process is typically emphasized in the related literature as a firmware-related topic, there are still important hardware considerations that must be made in order to ensure proper system operation. The following two requirements, in particular, must be met for proper USB enumeration to occur:

1. **Reference clock frequency:** The PCM270x and PCM290x both require a 12-MHz clock with an accuracy of  $\pm 500$  ppm. The PCM2912A requires a 6-MHz clock with an accuracy of  $\pm 500$  ppm. This reference frequency is typically provided by connecting a crystal to the XTI and XTO pins of the device.
2. **Proper USB data line logic levels:** USB communication protocol requires LV-TTL logic levels (3.3 V) for both of the D+ and D– data lines.

The following section outlines some possible design errors that could lead to a violation of the above requirements.

## 2 Design Considerations

When working with the PCM270x and PCM29xx USB audio devices, it is important to adhere to good hardware design practices with regards to reference clock frequency and USB communications in order to avoid enumeration errors.

### 2.1 Capacitive Loading on Crystal

Connecting an external crystal to the device XTI and XTO pins is the most common method for generating a reference clock frequency. The device internal oscillator circuit will provide the excitation necessary for the crystal. The external crystal also requires a 1-M $\Omega$  resistor connected in parallel to the crystal as well as two smaller capacitors (typically 10 pF to 33 pF) connected from each pin to ground (for a complete description, see the Clock and Reset sections of the respective device data sheet).

Failure to use load capacitors of the correct value required by the external crystal can result in frequency inaccuracies. Changes in the value of the load capacitors will effectively modify the output frequency of the complete oscillator circuit. Therefore, if the values of the load capacitors used with the crystal are sufficiently different than recommended, it is possible for the output frequency to be *pulled out* of the frequency tolerance range of the PCM270x and PCM29xx.

If a reference clock frequency outside of the device tolerance range is used, consequently the internal timing necessary for USB communication will be inaccurate, and the device will not be able to communicate properly with the host. This condition will lead directly to enumeration errors between the device and the host.

When troubleshooting an enumeration error, be sure to verify that the load capacitors used in the system are within the range recommended by the respective crystal data sheet. The PCM270x and PCM29xx families each have  $\sim 5$  pF of inherent capacitance on the XTI and XTO pins, so the device will see a load capacitance that is approximately 5 pF higher than the capacitor value alone. However, because the PCM270x and PCM29xx devices have a wide frequency tolerance range, it will take a very significant mismatch in value between a crystal's recommended load capacitor and the actual load capacitor used in a design to pull a 12-MHz or 6-MHz crystal out of the prescribed range.

Nevertheless, the load capacitance required can vary significantly from crystal to crystal, so problems can arise when changing crystals without subsequently changing load capacitors in a design.

## 2.2 USB Communication

Proper hardware implementation for USB communication is achieved with differential LV-TTL (3.3-V) signaling levels between the D+ and D- lines. For the D+ line, this logic level is achieved by connecting the line to the digital voltage supply ( $V_{DDi}$ ) through a 1.5-k $\Omega$  pull-up resistor. Figure 1 displays typical waveforms for D+ and D-.

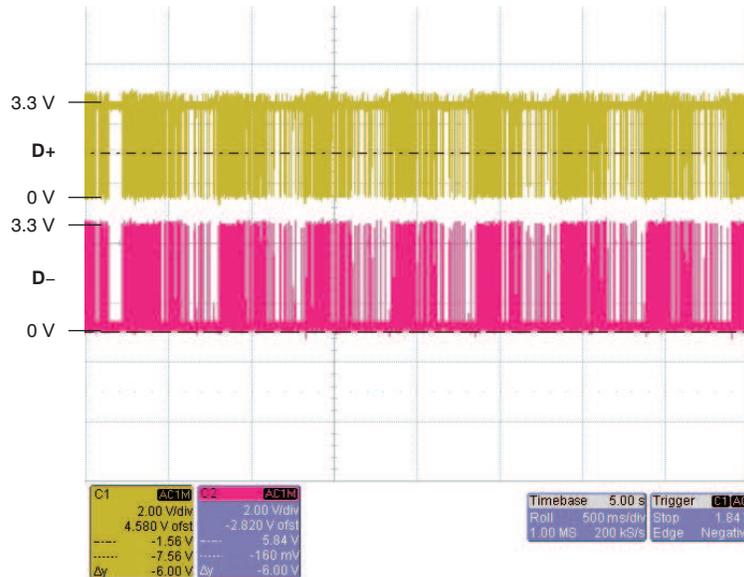


Figure 1. Proper Signaling Levels for USB Communication Lines D+ and D-

$V_{DDi}$  is generated from  $V_{BUS}$  with a voltage regulator that is internal to the PCM270x and PCM29xx devices. If the stability and/or level of  $V_{DDi}$  are compromised, D+ will not maintain proper signaling levels and enumeration errors can occur.

Because  $V_{DDi}$  is generated internal to the device, most of the power-supply functions required to provide a stable voltage rail are removed from the responsibility of the design engineer. However, it is crucial that the recommendation for the value of the  $V_{DDi}$  external capacitor be followed. The internal voltage regulator for  $V_{DDi}$  (as well as each of the internal regulators for the additional analog power-supply rails) is designed to provide a clean, stable voltage with a capacitance of 1  $\mu$ F at the output. Varying this external capacitance can result in oscillations at the output. When these oscillations are present on  $V_{DDi}$ , the system may encounter enumeration errors. When these oscillations are present on the analog power-supply rails, the system may experience greatly degraded codec performance. Figure 2 and Figure 3 show an example of when  $V_{DDi}$  has a 1-nF external capacitor instead of the recommended 1- $\mu$ F value.

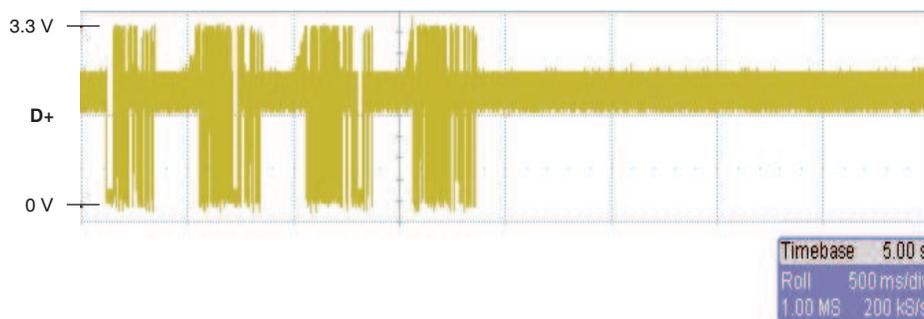
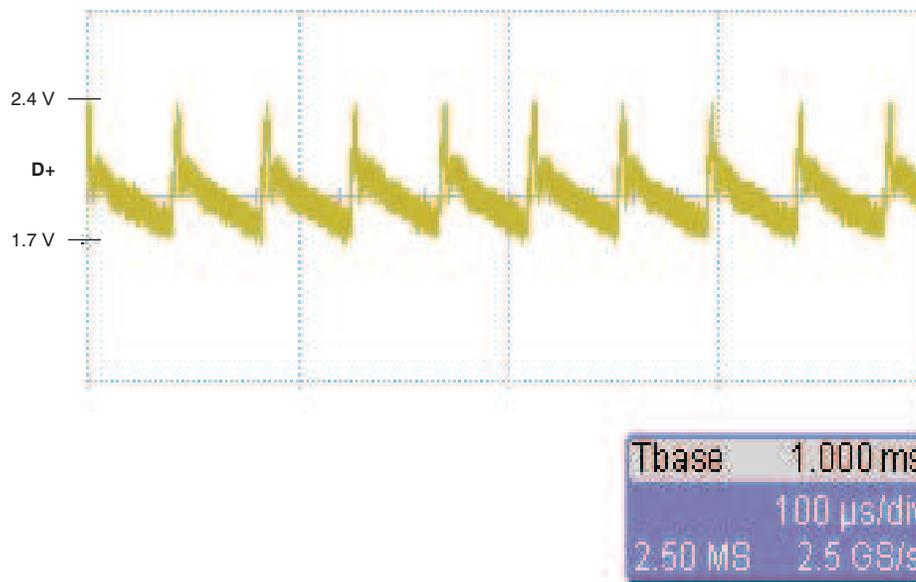


Figure 2. Oscillations on D+ Line as a Result of an Unstable  $V_{DDi}$



**Figure 3. Oscillations on D+ Line as a Result of an Unstable  $V_{DD1}$  (Enlarged)**

As [Figure 2](#) and [Figure 3](#) illustrate, a 1-nF capacitor on  $V_{DD1}$  led to large oscillations of approximately 0.7 V on the supply rail. This capacitor directly caused an enumeration error and USB communication could not be established. Smaller instabilities in  $V_{DD1}$  may also lead to periodic enumeration errors between the device and host, so it is important not to deviate from the recommended capacitance for the internally-generated voltage supply rails. See the Application Information section of the PCM270x and PCM29xx product data sheets (available for download at [www.ti.com](http://www.ti.com)) for reference schematics and a thorough description of the recommended capacitor values for each respective device.

### 3 Summary

Proper USB communication between a host and the PCM270x and PCM29xx devices requires precision in both timing and signaling levels. Therefore, it is crucial to have a design that employs an accurate reference frequency as well as stable, clean voltage supply rails. Two possible causes for enumeration errors (incorrect capacitive loading on the reference crystal and incorrect external capacitor values for internally-generated voltage supply rails) have been presented and design solutions have been recommended. For additional information, refer to the respective PCM270x and PCM29xx product data sheets.

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