Industrial Automation
TI Industrial Packaging

Application Report

Literature Number: SLDA019
November 2013–Revised January 2014

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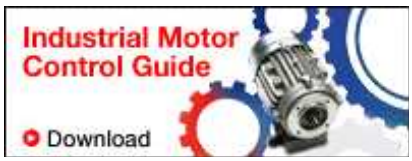
ABSTRACT

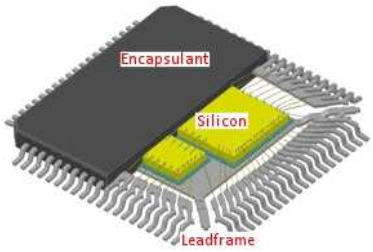
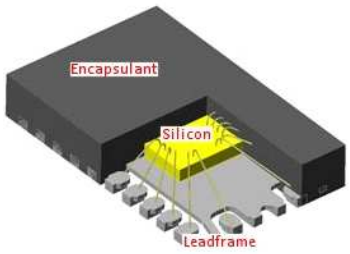
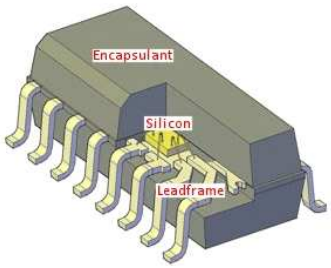
At Texas Instruments, semiconductor packaging is an integral part of the design process and strategic differentiator for our Industrial products. TI's innovative packaging technologies are designed to easily solve our customers' most challenging industrial needs by delivering advances in miniaturization, integration, high reliability, high performance, and low power. TI offers a broad Industrial packaging portfolio, built upon decades of packaging expertise developed from supporting thousands of diversified packaging configurations and technologies. Ranging from traditional to the most advanced embedded silicon technologies and more, TI is committed to delivering packaging technologies that advance our products today while anticipating our customers' needs in the future.

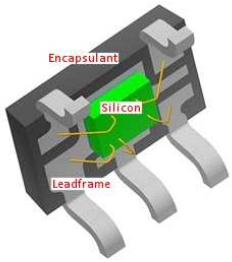
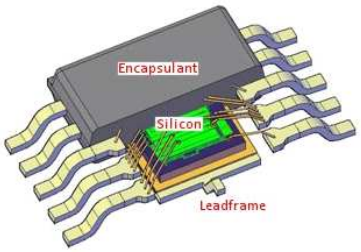
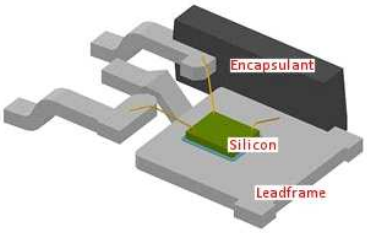
Within TI's broad Industrial packaging portfolio various form factors are offered to accommodate the ever changing needs of our customers. Ranging from traditional monolithic silicon packaging solutions to the most advanced embedded multi-silicon technologies and more, TI is committed to delivering robust packaging technologies that fulfill our customers' needs today while anticipating new packaging needs for the future.

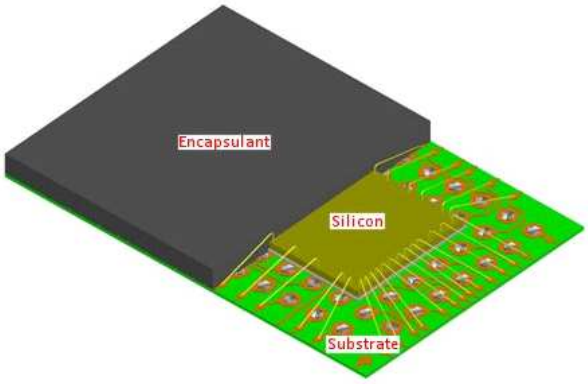
This document offers a variety of subjects such as a consolidated summary of the packaging families categorized by pin count density and form factor, TI's definition of Green and ROHS compliance, Illustration with explanation of TI's moisture sensitivity label, Various figures of merit such as thermal performance metrics, and a tabulated listing of packages with various descriptors to quickly help our customers identify their package of interest.

TI's diverse Industrial Product Portfolio Includes

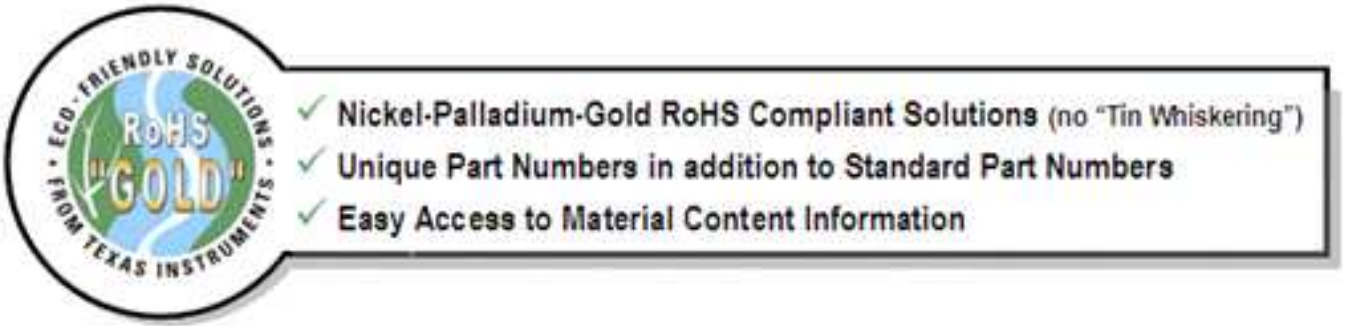


	QFP	QFN/SON	DIP
Package Type	 Encapsulant Partially Removed For Illustration Proposes	 Encapsulant Partially Removed For Illustration Proposes	 Encapsulant Partially Removed For Illustration Proposes
Benefits	**Leaded high Pin Count configurations with efficient Thermal Path**	**Space saving from higher Area Ratio configuration**	**Industry package outlines results in a large portfolio of devices available**

	SOT	TSSOP	TO
Package Type	 Encapsulant Removed From package base side for Illustration Proposes	 Encapsulant Partially Removed For Illustration Proposes	 Encapsulant Partially Removed For Illustration Proposes
Benefits	**Small form factor for leaded low pin count devices**	**Offers a condensed size in leaded package outline**	**Higher Voltage & thermal applications**

	uBGA	To the most Intergrated / Complex functions
Package Type	 Encapsulant Partially Removed For Illustration Proposes	
Benefits	**Ball Grid Area product lines allow maximum board consolidation with routing ease**	**From simplest form / function to highest Integrated configurations, Texas Instruments offers solutions for the most demanding Industrial integration needs**

RoHS Compliant Solutions & Lead-Free (Pb-Free) Devices from Texas Instruments



TI's NiPdAu (Nickel Palladium Gold) leadfree solution is perfect for the most demanding industrial environments. NiPdAu offers immunity to "tin whiskers" since electroplated tin is not present.

Moisture Sensitivity Level Example

Position Statement—For further information regarding TI's commitment, please see this page.

RoHS Material Declaration Certificate—Signed TI compliance certificate addressing RoHS (EU 2002/95/EC through 2011/65/EU), the Joint Industry Guide (JIG-101) and EU Directive 2004/12/EC (Packing Materials).

Product Content & Schedule Search Tool—Signed TI compliance certificate addressing RoHS (EU 2002/95/EC through 2011/65/EU), the Joint Industry Guide (JIG-101) and EU Directive 2004/12/EC (Packing Materials).

Lead-Free (PB-Free) FAQs -— Contains answers to Lead-free (Pb-free) Frequently Asked Questions.

China RoHA and Chasing Arrow Information—Contains information on China RoHS requirements and how it affects TI IC finished products.

Chasing Arrows PCN 20070518001 Details—Chasing arrow symbol added to TI labels, effective July 21, 2007.

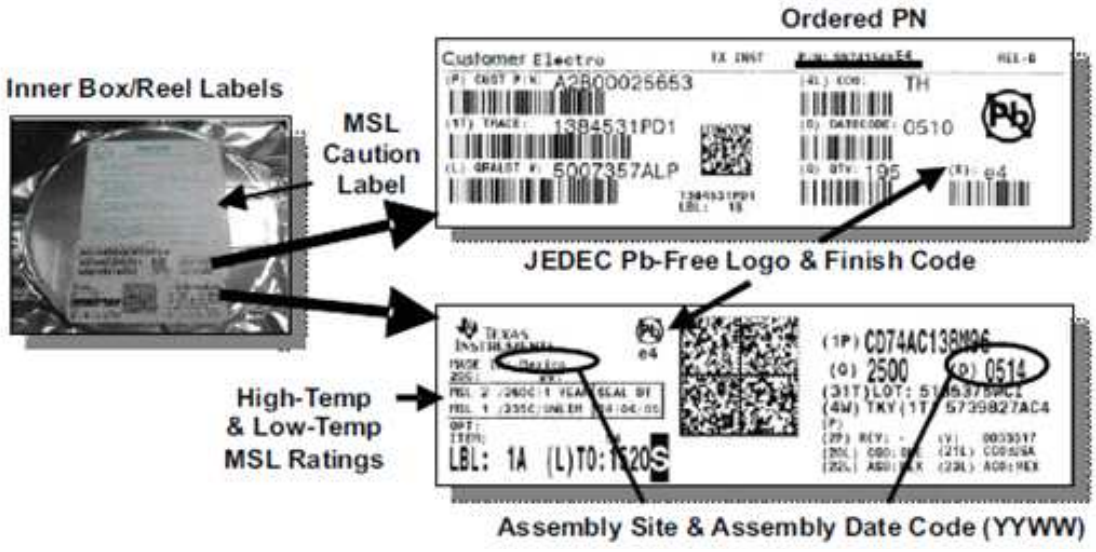
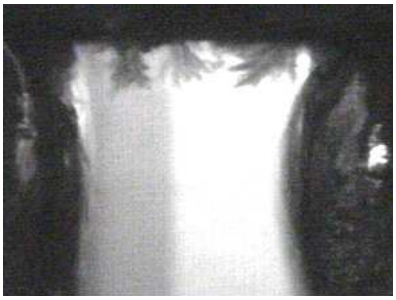


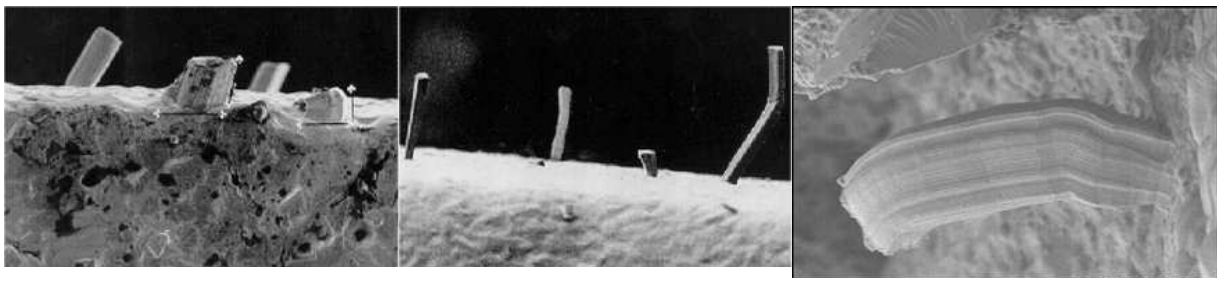
Figure 1. Packing Material Label Information With Moisture Sensitivity Level (MSL)

Silver Dendrites - Backlit Image of silver dendrite flowers on surface of printed circuit board.



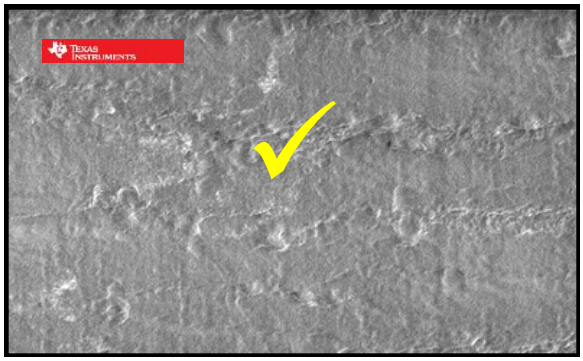
Dendrites - Backlit Image of silver dendrite flowers on surface of printed circuit board. Growth observed on surfaces containing silver during bias and humidity. Diurnal temperature inversions creating condensing moisture can accelerate the formation of silver dendrites therefore TI's NiPdAu finish is highly recommended.

Whiskering of Sn (Tin) Plated Parts – SEM image of in whisker filaments from plated surface.

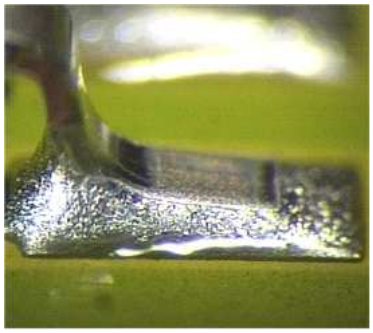


Matte Sn finish, 51C/85RH + Bias, 3000 hours exposure

NiPdAu Board Mount: Visual



Robust industrial environment ready. No whiskering or dendrites observed on NiPdAu finished parts.

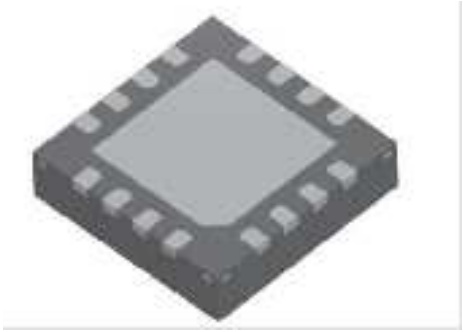


Typical wetting NiPdAu finished components with SnAgCu solder, NiAu PWB finish.

JEDEC/IPC Joint Publication No. 002 (JP002) – Identifies Nickel Palladium Gold as a non-whiskering solution.

Visual Appearance Results: The gold layer is translucent at the thicknesses plated and therefore the surface luster is representative of the palladium layer. Post solder processing the NiPdAu exhibited a heel fillet height with evidence of wetting to the sides of the leads. This performance would be considered acceptable for all 3 classes of products identified in IPC-A-610.

QFN Package Solutions



TI's QFN Packages offer space savings benefits for the most challenging form factor assemblies where space is critical. Our QFN package solution can be easily integrated into a design using recommendations published in the device level datasheet. Examples of the land pattern with typical solder joint geometries are given below in Figure 2 - Figure 5.

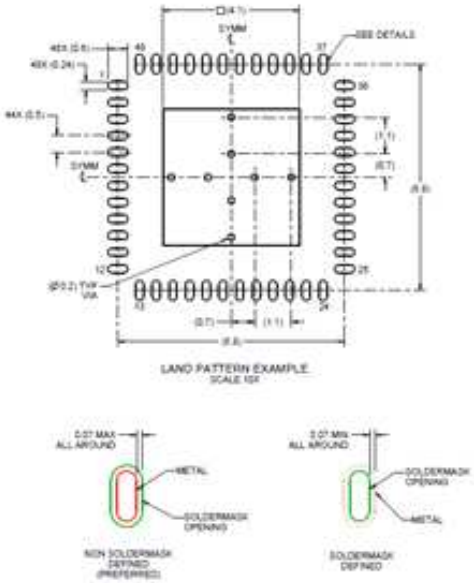


Figure 2. Typical Land Pattern Design from device datasheet

Figure 3. Image of Solder Joint Formation

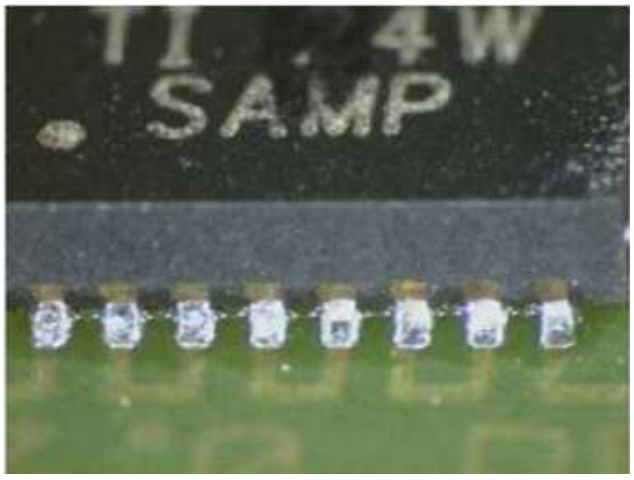


Figure 4. Image of solder joint formation

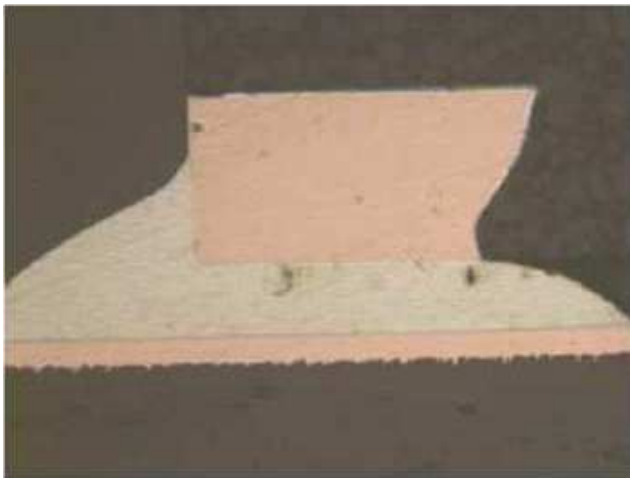


Figure 5. Cross section of a periphery lead with solder joint visible.

Tape and Reel

Tape and reel − The tape-and-reel configuration is used for transport and storage from the manufacturer of the electronic components to the customer, and for use in the customer manufacturing plant. The configuration is designed for feeding components to automatic-placement machines for surface mounting on board assemblies and can be used for most all SMT packages. Tape provides component lead isolation during shipping, handling, and processing. The complete configuration consists of a carrier tape with sequential individual cavities that hold individual components, and a cover tape that seals the carrier tape to retain the components in the cavities.

Figure 6. Reel With Carrier Tape

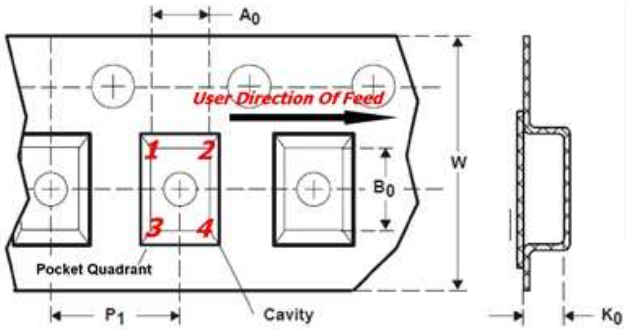


Figure 7. Carrier-Tape Dimensions and Pocket Quadrant Definition

- Carrier tape design is defined largely by the component length, width, and thickness. The following component dimensions are the basis for common industry dimension variables for carrier tape: Figure 7
- A0 = Dimension designed to accommodate the component width
- B0 = Dimension designed to accommodate the component length
- K0 = Dimension designed to accommodate the component thickness. For cavities with bottom pedestals, a K1 dimension is specified to identify the required pedestal height.
- W = Overall width of the carrier tape. This must conform to accepted industry standards
- P1 = Pitch between successive cavity centers. This dimension must conform to industry standards
- Packet Quadrant Definition (Figure 3) - Component orientation in the carrier-tape pocket is governed by EIA-783, which states that the following orientation rules shall be followed, sequentially, until no other variation is possible:

1. The largest axis of the component outline shall be perpendicular to the tape length.
2. The edge of the package containing termination 1 shall be oriented toward the round sprocket holes.
3. For the components where rule 1 and rule 2 do not establish a unique orientation, termination 1 shall be in quadrant 1.

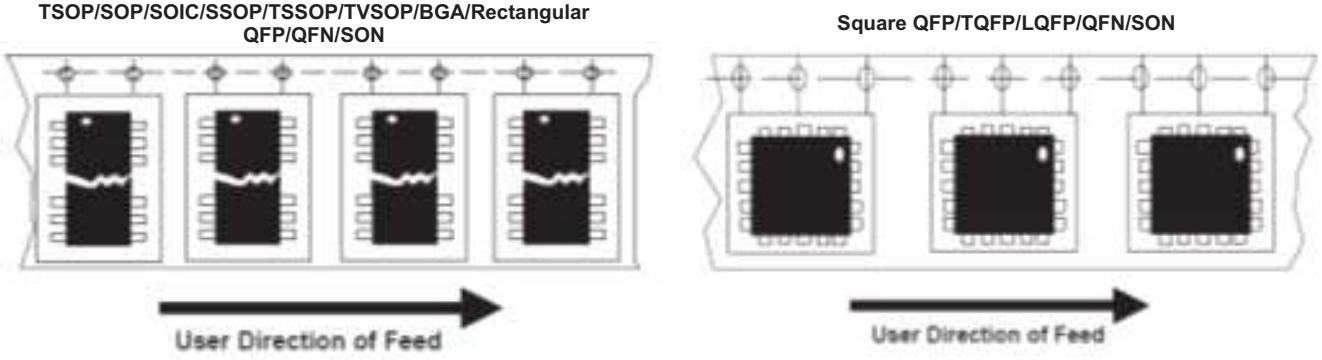


Figure 8. Typical TI Component Orientations for Tape-and-Reel Packing

Thermal Calculations

Measuring parts on a PCB:

Using Case temperature →

$$T_J = T_C + \text{Power} \times \Psi_{JT}$$

Estimating Tj for a new design (options):

Using PCB temperature →

$$T_J = T_B + \text{Power} \times \Psi_{JB}$$

System thermal modeling

PCB calculator

2R or Delphi model

Approximations based on existing device/system

Where:

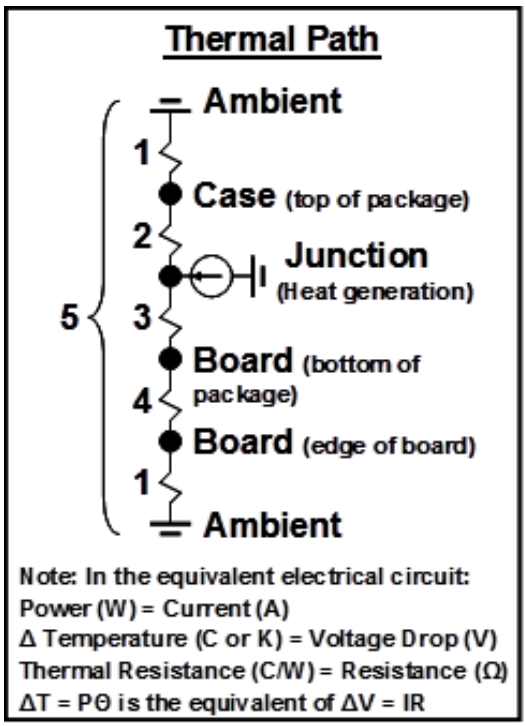
T_J= Junction Temp: max for performance, reliability, etc.

T_C= Case Temperature (measured)

Power: estimated or measured power

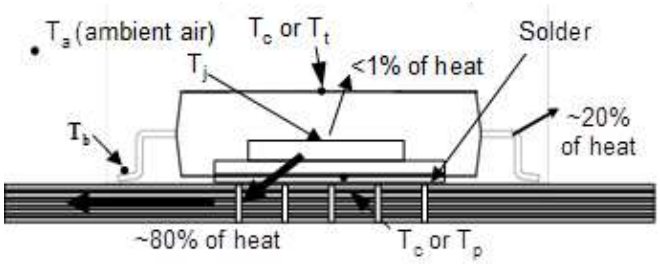
Psi-JT/ΨJT: Thermal delta, device to case/top, in system

Psi-JB/ΨJB :Thermal delta, device to PCB, in system, near device



Useful Links:

- www.ti.com/thermal
- **TI Apps note**: SPRA953A
- **PCB Apps note**: SLMA002
- **TI E2E Community**
- **JEDEC JESD51 Specs**



Description and Use of Common Terms

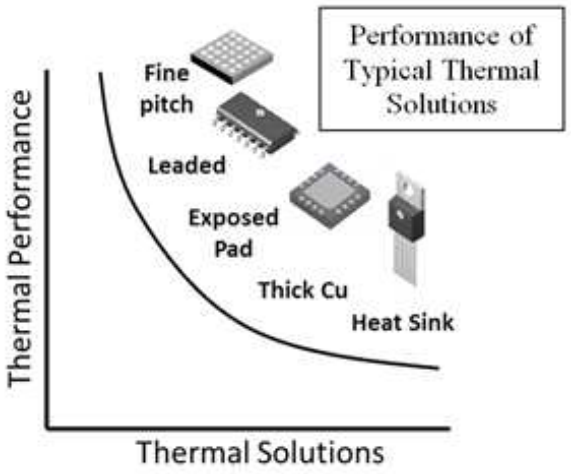
Theta-JA: (Tj – Ta) / Power. Defined by JEDEC 51-2A. Unique for each device. For comparison of devices and/or packages in a standardized environment. Not for calculation of Tj.

Theta-JA,effective: Non-JEDEC custom environment, such as EVM or specific end application.

Theta-JC,top: (Tj – Tc) / Power. True thermal resistance to top of part. Only used with a heat sink.

Psi-JT: (Tj – Tc) / Power. Measurement parameter. Used to calculate Tj based on a measured Tc.

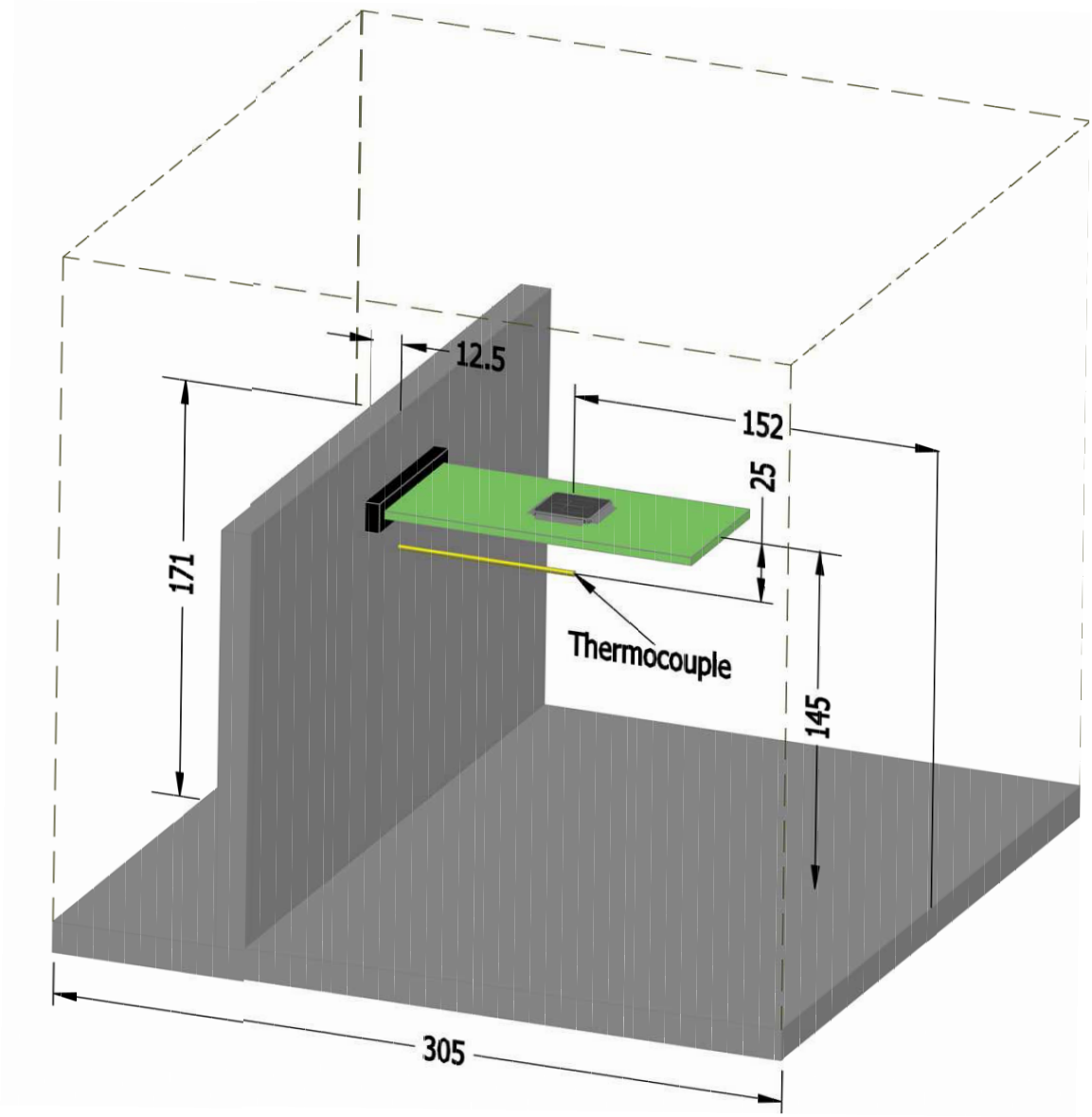
Theta-JB/Psi-JB: (Tj – Tb) / Power. Resistance or measurement parameter based on board temperature. Useful for early estimates of a new part in a known end application.



System Thermal Enhancements

- Spread out hot devices on PCB
- Maximize GND layer in PCB
- No breaks in heat flow through planes
- Increase PCB layers or thickness
- Widen PCB traces near device
- PCB vias under or near device
- System air vents near to device
- Airflow (global and local)
- Heat sink (individual, group, chassis)
- Gap filler materials up to chassis

Theta-JA,top: (Tj – Ta) / Power. Junction to ambient temperature characterization based on a fixed volumetric environment. Used only for calculating the junction temperature.



Theta-JB,Board: (Tj – Tb) / Power. The true thermal resistance to lead of the package. Used only for calculating the flow of heat up at the leads.

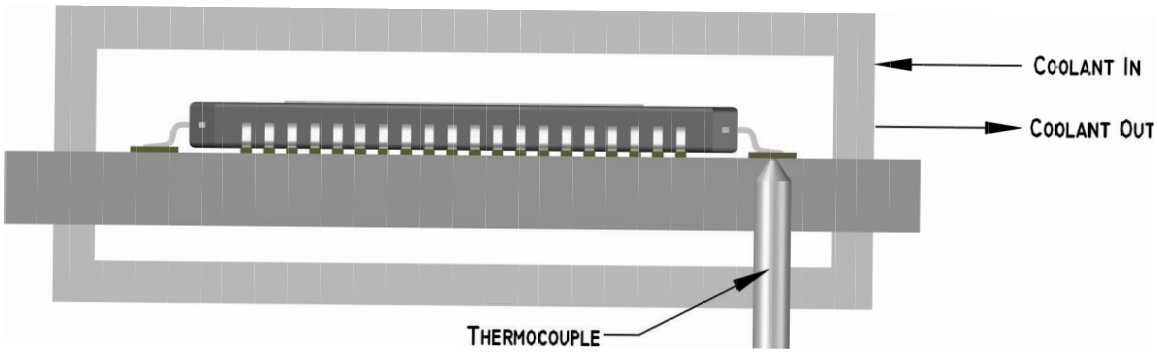


Figure 9. Thermal Measurement Method

Theta-JC,top: (Tj – Tc) / Power. The true thermal resistance to the top of a package. Used only for calculating the flow of heat up to a heat sink.

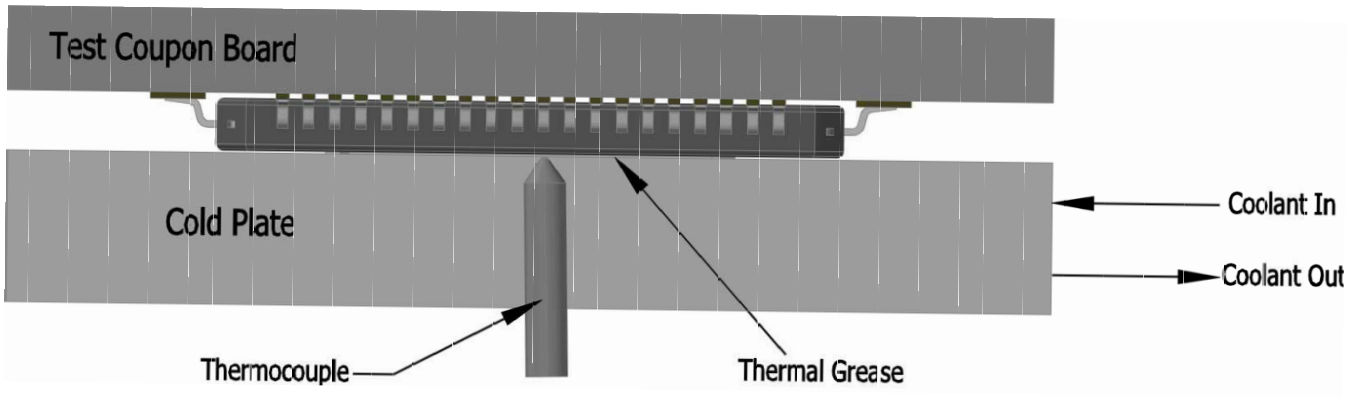


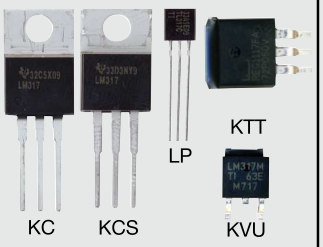
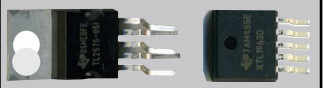
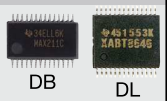
Figure 10. Cu Cold Plate Measurement Process

Pin count	Package type	TI package designator	Body length (mm)		Body width (mm)		Lead width (mm)		Pitch (mm)	Lead foot (mm)		Pkg width (mm)		Height (mm)
			Min	Max	Min	Max	Min	Max	Nom	Min	Max	Min	Max	Max
2	PowerFLEX	KTP	5.91	6.17	6.02	6.27	0.63	0.79	2.29	0.94	1.19	9.42	9.68	2.03
3	PFM/DPAK	KVU	6.5	6.7	5.97	6.22	0.76	0.89	2.29	1.4	1.78	9.8	10.41	2.39
3	PFM/TO—263/DDPAK	KTT	9.65	10.67	8.38	9.65	0.66	0.91	2.54	1.78	2.79	14.6	15.88	4.83
3	PowerFLEX	KTE	9.27	9.52	7.87	8.13	0.63	0.79	2.54	0.79	1.04	10.41	10.67	2.03
3	SOT/SC-70	DCK	1.85	2.15	1.10	1.40	0.15	0.30	0.65	0.26	0.46	1.80	2.40	1.10
3	SOT/SOT-23	DBZ	2.8	3.04	1.2	1.4	0.37	0.51	0.95	0.4	0.6	2.1	2.64	1.12
3	SOT	DRT	0.95	1.05	0.75	0.85	0.10	0.20	0.35	0.10	0.20	0.95	1.05	0.50
3	SOT/SOT-89	PK	4.4	4.6	2.4	2.6	0.36	0.53	1.5	0.8	1.2	3.94	4.25	1.6
3	TO-220	KC	9.65	10.67	8.38	9.02	0.71	0.89	2.54	—	—	26.92	31.24	4.7
3	TO-220	KCS	9.65	10.67	8.38	9.02	0.71	0.89	2.54	—	—	26.92	31.24	4.7
3	TO-92	LP	4.44	5.21	4.32	5.34	0.41	0.56	1.27	—	—	4.44	5.212	5.34
4	DSLGA (PicoStar™)	YFM	0.74	0.8	0.74	0.8	0.18	0.22	0.4	—	—	0.74	0.8	0.15
4	SOT/SOT-223	DCY	6.3	6.7	3.3	3.7	0.66	0.84	2.3	0.75	—	6.7	7.3	1.8
4	SOT-143	DZD	2.8	3.04	1.2	1.4	0.3	0.5	1.92	0.2	0.6	2.1	2.64	1.22
4	WCSP/NanoStar™	YDC	1.09	1.15	1.09	1.15	0.15*	0.19*	0.50	—	—	1.09	1.15	0.40
4	WCSP/NanoStar	YFP	0.74	0.8	0.74	0.8	0.21*	0.25*	0.4	—	—	0.74	0.8	0.5
4	WCSP/NanoStar	YZV	0.85	0.95	0.85	0.95	0.2*	0.25*	0.5	—	—	0.85	0.95	0.5
5	PFM	KV	9.65	10.67	8.38	9.25	0.75	1.02	1.7	—	—	24.64	25.15	4.7
5	PFM/TO-263/DDPAK	KTT	9.65	10.67	8.2	9.65	0.66	0.91	1.7	1.78	2.79	14.6	15.88	4.83
5	PowerFLEX	KTG	9.27	9.52	7.87	8.13	0.63	0.79	1.7	0.79	1.04	10.41	10.67	2.03
5	SOT/SC-70	DCK	1.85	2.15	1.1	1.4	0.15	0.3	0.65	0.26	0.46	1.8	2.4	1.1
5	SOT/SOT-23	DBV	2.8	3	1.5	1.7	0.3	0.5	0.95	0.35	0.55	2.6	3	1.45
5	SOT	DRL	1.5	1.7	1.1	1.3	0.15	0.25	0.5	0.2	0.4	1.5	1.7	0.6
5	SOT	DRT	0.95	1.05	0.75	0.85	0.1	0.2	0.35	0.1	0.2	0.95	1.05	0.5
5	TO-220	KC	9.65	10.67	7.67	9.25	0.64	1.02	1.7	—	—	26.51	31.24	4.83
5	WCSP/NanoStar	YFK	1.28	1.34	0.88	0.94	0.20*	0.30*	0.40	—	—	0.88	0.94	0.63
5	WCSP/NanoStar	YZP	1.35	1.45	0.85	0.95	0.21*	0.25*	0.50	—	—	0.85	0.95	0.50
5	WCSP/NanoStar	YZU	1.25	1.75	0.95	1.45	0.25*	0.35*	0.5	—	—	0.95	1.45	0.75
5	WCSP/NanoStar	YEU	1.25	1.75	0.95	1.45	0.25*	0.35*	0.5	—	—	0.95	1.45	0.75
5	WCSP/NanoStar	YEQ	1.17	1.67	0.8	1.3	0.15*	0.2*	0.5	—	—	0.8	1.3	0.63
6	PicoStar™	YFM	1.16	1.85	0.76	1.45	0.18	0.22	0.40	—	—	0.76	1.45	0.15
6	SOT/SC-70	DCK	1.85	2.15	1.1	1.4	0.15	0.3	0.65	0.26	0.46	1.8	2.4	1.1
6	SOT/SOT-23	DBV	2.8	3	1.5	1.7	0.25	0.5	0.95	0.35	0.55	2.6	3	1.45
6	SOT	DRL	1.5	1.7	1.1	1.3	0.15	0.25	0.5	0.2	0.4	1.5	1.7	0.6
6	SOT	DRT	0.95	1.05	0.75	0.85	0.1	0.2	0.35	0.1	0.2	0.95	1.05	0.5
6	SOT-223	DCQ	6.45	6.55	3.45	3.55	0.41	0.51	1.27	0.91	1.14	6.86	7.26	1.8
6	USON (Small Scale SON)	DRY	1.4	1.5	0.95	1.05	0.15	0.25	0.5	0.25	0.35	0.95	1.05	0.6
6	WCSP/NanoStar	YFJ	1.14	1.20	0.74	0.80	0.10*	0.14*	0.40	—	—	0.74	0.80	0.30
6	WCSP/NanoStar	YFP	1.14	1.2	0.74	0.8	0.21*	0.25*	0.4	—	—	0.74	0.8	0.5
6	WCSP/NanoStar	YFC	1.14	1.2	0.74	0.8	0.21*	0.25*	0.4	—	—	0.74	0.8	0.63
6	WCSP/NanoStar	YZP	1.35	1.45	0.85	0.95	0.21*	0.25*	0.5	—	—	0.85	0.95	0.5
6	WSON	DRS	2.85	3.15	2.85	3.15	0.3	0.4	0.95	0.45	0.55	2.85	3.15	0.8
6	WSON (Small Scale SON)	DRV	1.90	2.10	1.90	2.10	0.25	0.35	0.65	0.20	0.30	1.90	2.10	0.80
6	X2SON (Small Scale SON)	DSF	0.95	1.05	0.95	1.05	0.14	0.2	0.35	0.35	0.45	0.95	1.05	0.4
8	MSOP	DGN	2.9	3.1	2.9	3.1	0.25	0.38	0.65	0.4	0.7	4.75	5.05	1.1
8	SOIC	D	4.8	5	3.81	4	0.35	0.51	1.27	0.4	1.12	5.8	6.2	1.75
8	WSON	DRJ	3.9	4.1	3.9	4.1	0.25	0.35	0.8	0.4	0.6	3.9	4.1	0.8
8	WSON	DRG	2.9	3.1	2.9	3.1	0.2	0.3	0.5	0.4	0.6	2.9	3.1	0.8
8	SOP	PS	5.9	6.5	5	5.6	0.35	0.51	1.27	0.55	0.95	7.4	8.2	2
8	SOT-23	DCN	2.8	3	1.45	1.75	0.22	0.38	0.65	0.3	0.6	2.6	3	1.45

Pin count	Package type	TI package designator	Body length (mm)		Body width (mm)		Lead width (mm)		Pitch (mm)	Lead foot (mm)		Pkg width (mm)		Height (mm)
			Min	Max	Min	Max	Min	Max	Nom	Min	Max	Min	Max	Max
8	SSOP/SM8	DCT	2.75	3.15	2.7	2.9	0.15	0.3	0.65	0.2	0.6	3.75	4.25	1.3
8	TSSOP	PW	2.9	3.1	4.3	4.5	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
8	UQFN (Small Scale QFN)	RSE	1.45	1.55	1.45	1.55	0.2	0.3	0.5	0.3	0.4	1.45	1.55	0.6
8	VSSOP/MSOP	DGK	2.9	3.1	2.9	3.1	0.25	0.38	0.65	0.4	0.7	4.75	5.05	1.1
8	VSSOP/US8	DDU	1.9	2.1	2.2	2.4	0.17	0.25	0.5	0.2	0.35	3	3.2	0.9
8	WCSP/NanoStar	YFP	1.54	1.6	0.74	0.8	0.21	0.25	0.4	—	—	0.74	0.8	0.5
8	WSON (Small Scale SON)	DQD	1.60	1.80	1.25	1.45	0.15	0.25	0.40	0.15	0.35	1.25	1.45	0.80
8	WSON	DRG	2.9	3.1	2.9	3.1	0.2	0.3	0.5	0.4	0.6	2.9	3.1	0.8
8	WSON	DRJ	3.9	4.1	3.9	4.1	0.25	0.35	0.8	0.4	0.6	3.9	4.1	0.8
8	X2QFN (Small Scale QFN)	RUG	1.45	1.55	1.45	1.55	0.2	0.3	0.5	0.3	0.4	1.45	1.55	0.4
8	X2SON	DQE	1.35	1.45	0.95	1.05	0.15	0.20	0.35	0.25	0.35	0.95	1.05	0.40
8	X2SON (Small Scale SON)	DQL	1.95	2.05	1.35	1.45	0.15	0.25	0.50	0.30	0.40	1.35	1.45	0.40
8	X2SON (Small Scale SON)	DQM	1.75	1.85	1.15	1.25	0.15	0.25	0.40	0.45	0.55	1.15	1.25	0.40
9	WCSP/NanoStar	YFP	1.14	1.2	1.14	1.2	0.21	0.25	0.4	—	—	1.14	1.2	0.5
10	MSOP	DGS	2.9	3.1	2.9	3.1	0.17	0.27	0.5	0.4	0.7	4.75	5.05	1.1
10	UQFN (Small Scale QFN)	RSW	1.75	1.85	1.35	1.45	0.15	0.25	0.4	0.35	0.45	1.35	1.45	0.55
10	UQFN (Small Scale QFN)	RSE	1.95	2.05	1.45	1.55	0.2	0.3	0.5	0.3	0.4	1.45	1.55	0.6
10	USON (Small Scale SON)	DQA	2.40	2.60	0.90	1.10	0.15	0.25	0.50	0.30	0.43	0.90	1.10	0.55
10	VSON	DRC	2.85	3.15	2.85	3.15	0.18	0.3	0.5	0.3	0.5	2.85	3.15	1
10	WCSP/NanoStar	YZP	1.84	1.9	1.34	1.4	0.21	0.25	0.5	—	—	1.34	1.4	0.5
10	WCSP/NanoStar	YFU	1.53	1.59	1.02	1.08	0.21	0.25	0.40	—	—	1.02	1.08	0.32
10	WQFN (Small Scale QFN)	RSD	1.95	2.05	1.45	1.55	0.20	0.30	0.50	0.30	0.40	1.45	1.55	0.80
10	X2QFN (Small Scale QFN)	RUG	1.95	2.05	1.45	1.55	0.2	0.3	0.5	0.3	0.4	1.45	1.55	0.4
12	UFBGA/MicroStar Jr. BGA	ZXU	2.4	2.6	1.9	2.1	0.25	0.35	0.5	—	—	1.9	2.1	0.61
12	UQFN (Small Scale QFN)	RUT	1.90	2.10	1.60	1.80	0.15	0.25	0.40	0.45	0.55	1.60	1.80	0.55
12	WCSP/NanoStar	YFC	1.54	1.6	1.14	1.2	0.21	0.25	0.4	—	—	1.14	1.2	0.63
12	WCSP/NanoStar	YFF	1.53	1.59	1.13	1.19	0.20	0.30	0.40	—	—	1.13	1.19	0.63
12	WCSP/NanoStar	YZP	1.84	1.9	1.34	1.4	0.21	0.25	0.5	—	—	1.34	1.4	0.5
12	WCSP/NanoStar	YZT	1.84	1.9	1.34	1.4	0.21	0.25	0.5	—	—	1.34	1.4	0.63
12	WQFN	RSF	3.85	4.15	3.85	4.15	0.25	0.35	0.8	0.45	0.65	3.85	4.15	0.8
12	WSON (Small Scale SON)	DQD	2.40	2.60	1.25	1.45	0.15	0.25	0.40	0.15	0.35	1.25	1.45	0.80
12	WSON (Small Scale SON)	DSV	2.90	3.10	1.25	1.45	0.20	0.25	0.50	0.20	0.30	1.25	1.45	0.80
12	X2QFN (Small Scale QFN)	RUE	1.95	2.05	1.35	1.45	0.15	0.25	0.4	0.35	0.45	1.35	1.45	0.4
14	PDIP	N	18.92	19.69	6.10	6.60	0.38	0.53	2.54	—	—	7.62	8.26	5.08
14	VQFN	RGY	3.35	3.65	3.35	3.65	0.18	0.3	0.5	0.3	0.5	3.35	3.65	1
14	SOIC	D	8.55	8.75	3.81	4	0.35	0.51	1.27	0.4	1.12	5.8	6.2	1.75
14	SOP	NS	9.9	10.5	5	5.6	0.35	0.51	1.27	0.55	1.05	7.4	8.2	2
14	SSOP	DB	5.9	6.5	5	5.6	0.22	0.38	0.65	0.55	0.95	7.4	8.2	2
14	TSSOP	PW	4.9	5.1	4.3	4.5	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
14	TVSOP	DGV	3.5	3.7	4.3	4.5	0.13	0.23	0.4	0.5	0.75	6.2	6.6	1.2
14	X2QFN (Small Scale QFN)	RUC	1.95	2.05	1.95	2.05	0.15	0.25	0.4	0.35	0.45	1.95	2.05	0.4
14	X2QFN (Small Scale QFN)	RUD	1.65	1.75	1.45	1.55	0.14	0.2	0.35	0.25	0.35	1.45	1.55	0.4
15	WCSP/NanoStar	YFU	2.33	2.39	1.02	1.08	0.21	0.25	0.40	—	—	1.02	1.08	0.32
16	PDIP	N	18.92	19.69	6.10	6.60	0.38	0.53	2.54	—	—	7.62	8.26	5.08
16	VQFN	RGY	3.85	4.15	3.35	3.65	0.18	0.3	0.5	0.3	0.5	3.35	3.65	1
16	QSOP	DBQ	4.8	5	3.81	3.99	0.2	0.3	0.64	0.4	0.89	5.8	6.2	1.75
16	SOIC	DW	10.16	10.41	7.4	7.6	0.35	0.51	1.27	0.4	1.27	10.15	10.63	2.65
16	SOIC	D	9.8	10	3.81	4	0.35	0.51	1.27	0.4	1.12	5.8	6.2	1.75
16	SOP	NS	9.9	10.5	5	5.6	0.35	0.51	1.27	0.55	1.05	7.4	8.2	2

Pin count	Package type	TI package designator	Body length (mm)		Body width (mm)		Lead width (mm)		Pitch (mm)	Lead foot (mm)		Pkg width (mm)		Height (mm)
			Min	Max	Min	Max	Min	Max	Nom	Min	Max	Min	Max	Max
16	SSOP	DB	5.9	6.5	5	5.6	0.22	0.38	0.65	0.55	0.95	7.4	8.2	2
16	TSSOP	PW	4.9	5.1	4.3	4.5	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
16	TVSOP	DGV	3.5	3.7	4.3	4.5	0.13	0.23	0.4	0.5	0.75	6.2	6.6	1.2
16	UQFN (Small Scale QFN)	RSV	2.55	2.65	1.75	1.85	0.15	0.25	0.4	0.35	0.45	1.75	1.85	0.55
16	VQFN	RGT	2.85	3.15	2.85	3.15	0.18	0.3	0.5	0.3	0.5	2.85	3.15	1
16	VQFN	RGV	3.85	4.15	3.85	4.15	0.23	0.38	0.65	0.45	0.65	3.85	4.15	1
16	WCSP/NanoStar	YFP	1.54	1.60	1.54	1.60	0.21	0.25	0.40	—	—	1.54	1.60	0.50
16	WQFN	RTZ	2.9	3.1	2.9	3.1	0.25	0.35	0.5	0.25	0.35	2.9	3.1	0.8
16	WQFN	RTE	2.85	3.15	2.85	3.15	0.18	0.3	0.5	0.3	0.5	2.85	3.15	0.8
16	WSON	DQD	3.20	3.40	1.25	1.45	0.15	0.25	0.40	0.15	0.35	1.25	1.45	0.80
18	PDIP	N	21.59	23.37	6.10	6.60	0.38	0.53	2.54	—	—	7.62	8.26	5.08
18	SOIC	DW	11.51	11.73	7.4	7.6	0.35	0.51	1.27	0.4	1.27	10.15	10.63	2.65
20	MicroStar Jr.™ ZT BGA	ZXY	2.9	3.1	2.4	2.6	0.25	0.35	0.5	—	—	2.4	2.6	0.61
20	PDIP	N	23.88	26.92	6.10	6.60	0.38	0.53	2.54	---	---	7.62	8.26	5.08
20	VQFN	RGY	4.35	4.65	3.35	3.65	0.18	0.3	0.5	0.3	0.5	3.35	3.65	1
20	QSOP	DBQ	8.56	8.74	3.81	3.99	0.2	0.3	0.64	0.4	0.89	5.8	6.2	1.75
20	SOIC	DW	12.7	12.95	7.39	7.59	0.35	0.51	1.27	0.4	1.27	10.15	10.65	2.65
20	SOP	NS	12.3	12.9	5	5.6	0.35	0.51	1.27	0.55	1.05	7.4	8.2	2
20	SSOP	DB	6.9	7.5	5	5.6	0.22	0.38	0.65	0.55	0.95	7.4	8.2	2
20	TSSOP	PW	6.4	6.6	4.3	4.5	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
20	TVSOP	DGV	4.9	5.1	4.3	4.5	0.13	0.23	0.4	0.5	0.75	6.2	6.6	1.2
20	USON	DQS	3.95	4.05	1.95	2.05	0.15	0.25	0.40	0.50	0.60	1.95	2.05	0.55
20	VFBGA/MicroStar Jr.™ BGA	GQN	3.9	4.1	2.9	3.1	0.35	0.45	0.65	—	—	2.9	3.1	1
20	VQFN	RGW	4.85	5.15	4.85	5.15	0.23	0.38	0.65	0.45	0.65	4.85	5.15	1
20	WCSP/NanoStar™	YFP	1.94	2	1.54	1.6	0.21	0.25	0.4	—	—	1.54	1.6	0.5
20	WCSP/NanoStar	YZP	2.37	2.43	1.87	1.93	0.21	0.25	0.50	—	—	1.87	1.93	0.50
20	WQFN	RVC	3.90	4.10	2.90	3.10	0.15	0.25	0.50	0.35	0.45	2.90	3.10	0.80
24	PDIP	NT	31.24	32	6.35	7.11	0.38	0.53	2.54	—	—	7.62	8.26	5.08
24	QSOP	DBQ	8.56	8.74	3.81	3.99	0.2	0.3	0.64	0.4	0.89	5.8	6.2	1.75
24	SOIC	DW	15.24	15.49	7.4	7.6	0.35	0.51	1.27	0.4	1.27	10.15	10.63	2.65
24	SOP	NS	14.7	15.3	5	5.6	0.35	0.51	1.27	0.55	1.05	7.4	8.2	2
24	SSOP	DB	7.9	8.5	5	5.6	0.22	0.38	0.65	0.55	0.95	7.4	8.2	2
24	TSSOP	PW	7.7	7.9	4.3	4.6	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
24	TVSOP	DGV	4.9	5.1	4.3	4.6	0.13	0.23	0.4	0.5	0.75	6.2	6.6	1.2
24	VFBGA/MicroStar Jr. BGA	ZQS	2.9	3.1	2.9	3.1	0.25	0.35	0.5	—	—	2.9	3.1	0.77
24	VQFN	RGE	3.85	4.15	3.85	4.15	0.18	0.3	0.5	0.3	0.5	3.85	4.15	1
24	VQFN	RHL	5.35	5.65	3.35	3.65	0.18	0.30	0.50	0.30	0.50	3.35	3.65	1
24	WQFN	RTW	3.85	4.15	3.85	4.15	0.18	0.3	0.5	0.3	0.5	3.85	4.15	0.8
25	WCSP/NanoStar	YFP	1.94	2.1	1.94	2.1	0.21	0.25	0.4	—	—	1.94	2.1	0.5
28	SOIC	DW	17.78	18.03	7.4	7.6	0.35	0.51	1.27	0.4	1.27	10.15	10.63	2.65
28	SSOP	DB	9.9	10.5	5	5.6	0.22	0.38	0.65	0.55	0.95	7.4	8.2	2
28	TSSOP	PW	9.6	9.8	4.3	4.5	0.19	0.3	0.65	0.5	0.75	6.2	6.6	1.2
28	WQFN	RHR	5.40	5.60	3.40	3.60	0.20	0.30	0.50	0.30	0.50	3.40	3.60	0.80
28	WCSP/NanoStar	YFF	2.73	2.79	1.53	1.59	0.20	0.30	0.40	—	—	1.53	1.59	0.63
29	WCSP/NanoStar	YFF	2.61	2.67	2.13	2.19	0.20	0.30	0.40	—	—	2.13	2.19	0.63
30	WCSP/NanoStar	YFC	2.54	2.6	2.44	2.5	0.21	0.25	0.4	—	—	2.44	2.5	0.63
32	UQFN	RGJ	4.85	5.15	4.85	5.15	0.18	0.3	0.5	0.3	0.5	4.85	5.15	0.6
32	VQFN	RHB	4.85	5.15	4.85	5.15	0.18	0.3	0.5	0.3	0.5	4.85	5.15	1
32	VQFN	RSM	3.85	4.15	3.85	4.15	0.15	0.25	0.4	0.3	0.5	3.85	4.15	1
32	WQFN	RTG	5.90	6.10	2.90	3.10	0.15	0.25	0.40	0.20	0.40	2.90	3.10	0.80
36	VQFN	RHH	5.85	6.15	5.85	6.15	0.18	0.3	0.5	0.45	0.65	5.85	6.15	1
38	TSSOP	DBT	9.6	9.8	4.3	4.5	0.17	0.27	0.5	0.5	0.75	6.2	6.6	1.2
42	WQFN	RUA	8.9	9.1	3.4	3.6	0.2	0.3	0.5	0.3	0.5	3.4	3.6	0.8
48	nfBGA	ZAH	4.9	5.1	4.9	5.1	0.25	0.35	0.5	—	—	4.9	5.1	1.2
48	SSOP	DL	15.75	16	7.39	7.59	0.2	0.34	0.64	0.51	1.02	10.03	10.67	2.79
48	TSSOP	DGG	12.4	12.6	6	6.2	0.17	0.27	0.5	0.5	0.75	7.9	8.3	1.2

Pin count	Package type	TI package designator	Body length (mm)		Body width (mm)		Lead width (mm)		Pitch (mm) Nom	Lead foot (mm)		Pkg width (mm)		Height (mm) Max
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	
48	TVSOP	DGV	9.6	9.8	4.3	7.59	0.13	0.23	0.4	0.5	0.75	6.2	4.6	1.2
48	VFBGA/MicroStar Jr. BGA	ZQL	6.9	7.1	4.4	4.5	0.35	0.45	0.65	—	—	4.4	6.6	1
48	VFBGA/MicroStar Jr. BGA	GQL	6.9	7.1	4.4	6.2	0.35	0.45	0.65	—	—	4.4	8.3	1
48	VFBGA/MicroStar Jr. BGA	ZQC	3.9	4.1	3.9	4.1	0.25	0.35	0.5	—	—	3.9	4.1	0.77
49	WCSP/NanoStar	YFF	2.73	2.79	2.73	2.79	0.20	0.30	0.40	—	—	2.73	2.79	0.63
54	TFBGA/MicroStar Jr. BGA	ZRD	7.9	8.1	5.4	5.6	0.45	0.55	0.8	—	—	5.4	5.6	1.2
56	SSOP	DL	18.29	18.54	7.39	7.59	0.2	0.34	0.64	0.51	1.02	10.03	10.67	2.79
56	TSSOP	DGG	13.9	14.1	6	6.2	0.17	0.27	0.5	0.5	0.75	7.9	8.3	1.2
56	TVSOP	DGV	11.2	11.4	4.3	4.5	0.13	0.23	0.4	0.5	0.75	6.2	6.6	1.2
56	VFBGA/MicroStar Jr. BGA	ZQL	6.9	7.1	4.4	4.6	0.35	0.45	0.65	—	—	4.4	4.6	1
56	VFBGA/MicroStar Jr. BGA	GQL	6.9	7.1	4.4	4.6	0.35	0.45	0.65	—	—	4.4	4.6	1
56	VQFN	RGQ	7.85	8.15	7.85	8.15	0.18	0.3	0.5	0.3	0.5	7.85	8.15	1
56	WQFN	RHU	10.85	11.15	4.85	5.15	0.18	0.3	0.5	0.3	0.5	4.85	5.15	0.8
64	TSSOP	DGG	16.9	17.1	6	6.2	0.17	0.27	0.5	0.5	0.75	7.9	8.3	1.2
80	TSSOP	DBB	16.9	17.1	6	6.2	0.13	0.23	0.4	0.45	0.75	7.9	8.3	1.2
81	WCSP/NanoStar	YFF	3.73	3.79	3.63	3.69	0.20	0.30	0.40	—	—	3.63	3.69	0.63
83	VFBGA/MicroStar Jr. BGA	ZRG	9.9	10.1	4.4	4.6	0.35	0.45	0.65	—	—	4.4	4.6	1
96	LFBGA/MicroStar BGA	GKE	13.4	13.6	5.4	5.6	0.45	0.55	0.8	—	—	5.4	5.6	1.4
96	LFBGA/MicroStar BGA	ZKE	13.4	13.6	5.4	5.6	0.45	0.55	0.8	—	—	5.4	5.6	1.4
96	MicroStar Jr. ZT BGA	ZRL	8.4	8.6	3.4	3.6	0.25	0.35	0.5	—	—	3.4	3.6	0.61
114	LFBGA/MicroStar BGA	GKF	15.9	16.1	5.4	5.6	0.45	0.55	0.8	—	—	5.4	5.6	1.4
114	LFBGA/MicroStar BGA	ZKF	15.9	16.1	5.4	5.6	0.45	0.55	0.8	—	—	5.4	5.6	1.4

Pin	TO	PDIP	SOIC	SOP	SSOP	QSOP	TSSOP
3	 KC KCS LP KTT KVU						
5	 KV KTT						
8		 P	 D	 PS	DCT		 PW
8			 D	 NS	 DB		 PW
14		 N	 D				
16		 NE	 DW	 NS	 DB	 DBQ	 PW
18		 N	 DW				
18		 N	 DW	 NS	 DB	 DBQ	 PW
20		 NT	 DW	 NS	 DB	 DBQ	 PW
24			 DW		 DB DL		 PW
28							 DBT
38					 DL		
48							 DGG
56					 DL		DGG
64							DGG
80							DBB

Pin	µSON	VSSOP	TVSOP	SOT	PicoStar™	QFN	µQFN
3				DRT SC70 DCK PK DBZ			
4				DCY DZD			
5				DBV DCK DRT DRL			
6	DRY			DCK DCQ DRL DBV DRT	YFM		
8		DGN DCU DDU DGK		DCN			RSE
9							
10	DQA	DGS				DRC	RSE
12							RUT
14			DGV			RGY	
15							
16			DGV			RGT RGY	RSV
20	DQS		DGV			RGW RGY	
24			DGV			RGE RHL	
25							
28							
29							
30							
32						RSM RHB	RGJ
36						RHH	
42							
48							
49							
54			DGV				
56			DGV			RGQ	
81							
83							
96							
114							

Pin	WQFN	WCSP	X2SON	WSON	XLGA	X2QFN	BGA
3							
4		YFP YZV YDC			YFM		
5		YFK YFP YZP					
6		YZP YFP YFC YFJ	DSF	DRS DRV			
8		YFP YZP	DQE DQM DQM DQL DQL	DRJ DRG DQD			
9		YFP					
10	RSD	YZP YFU					
12	RSF	YFC YFF YZT		DQD DSV		RUE	ZXU
14						RUC	
15		YFU					
16	RTE	YFP		DQD			
20	RVC	YZP YFP					ZXY VFBGA GQN/ZQN
24	RTW	YFP					ZQS VFBGA GQL/ZQL
25		YFP					
28	RHR	YFF					
29		YFF					
30		YFC					
32	RTG						
36							
42	RUA						
48							ZAH ZQC
49		YFF					
54							ZRD
56	RHU						VFBGA GQL/ZQL
81		YFF					
83							ZRG
96							VFBGA GKE/ZKE ZRL
114							VFBGA GKF/ZKF

Package type	Pins	Package Designator											
		TI	ADI	Fairchild	IDT	Maxim	National	NXP	ON Sem	Pericom	Richtek	STM	Toshiba
LFBGA (MicroStar)	96	GKE/ZKE		G	BF			EC		NB			
	114	GKF/ZKF			BF			EC					
VSSOP	8	DCU		K8				DC	US	D			FK
	8	DDU											
	8	DGK	RM	MU		UA	MM			M / U			
	8	DGN				UA							
	8	DGS							MN				
NFBGA	48	ZAH											
	48	ZQC											
	54	ZRD											
	83	ZRG											
	96	ZRL											
PICOSTAR™	4	YFM											
PDIP	8	P	N	N		PA	P / N		N (Logic) P / PL (Analog)	P	N	N	P
	14, 16, 20	N	N	N, PC	P	PD, PE	DQR (14), P (16), PC (16/20), N (20)	N / P	N (Logic) P / PL (Analog)	P	N	X	
	24, 28	NT	N	N	PT			N2	N (Logic) P / PL (Analog)	P		F	
QFN	8, 12, 16	DQD						GU		ZJ		M	
	10	DRC						TK		ZE	QW		
	8	DRG										PU	
	8	DRJ							MN			PU	
	4	DRS											
	24	RGE						BS		ZD	QW	QT	
	32	RGJ											
	16	RGT											
	16	RGV			NDG	TE		BS					
	20	RGW				TP		BS					
	14, 16, 20, 24	RGY		BQ				BQ / BX	MN	ZH			
	32	RHB				TJ		BS		ZH	QW		
	36	RHH											
	20, 24	RHL								ZH			
	56	RHU				TN		HF		ZF		QT	
	12	RSF				TC							
	32	RSM											
	16	RTE								ZH			FTG
	32	RTG						HF		ZL			
	24	RTW				TG		HF					FTG
	16	RTZ											
	42	RUA				TO				ZH		QT	
	20	RVC											
QSOP	16, 20, 24	DBQ		QSC	PC			DS (16/20) DK (24)		Q		PT	
SOIC	8, 14, 16	D	RG	M, SC	DC (14), SO (16)	SA, SD, SE	MA / MX (8) CX (14) M (14/16) SC / SX (16)	D / T	D	W	S	D, MN	FN
	16, 20, 24, 28	DW	RW	SC, WM	SO, DC (20)	WE, WG, WI, WN, WP	SC, SX SJX, WM	D / T	DW	S		MT, XD	FW
SOP	14, 16, 20, 24	NS		SJ			SJ (20), LQ (24)						F
	8	PS											
SOT	5, 6	DBV	RJ	M5, M6	DZG	UK, CY, UR	M5 (5), MF (5/6), M6 (6)	GW	DF (Logic) SQ (Analog)	T	BR / J5 (5), E / J6 (6)	LT	
	Pi	DBZ		S3, CM		UR	M3				V		
	3, 5, 6	DCK	KS	P5, P6	DY	XK	M7 (5), MG (6)	GW	DF (Logic), SN (Analog)	C	U	CT	FU
	8	DCN											
	8	DCT									V8		
	4	DZD											
	4	DCY	KC	S		Z	MP, EMP		ST		G	Z	
	5, 6	DRL			DY				XV5 / XV6	TA			FE
	3, 5	DRT											FSV

Package type	Pins	Package Designator											
		TI	ADI	Fairchild	IDT	Maxim	National	NXP	ON Sem	Pericom	Richtek	STM	Toshiba
SSOP	14, 16, 20, 24, 28, 30, 38, 114	DB	RS	MSA, MSC		AG, AP	MSA	DB / TS	SD, DB (Analog)	H	A		FS
	16, 20, 24	DBQ						DS		Q			
	28, 48, 56	DL		SSC, MEA		UM		DL	DT (Logic)	V			
TO / POWER	3, 5	KC									T		
	3	KCS				CR	T / TA		T		T	CV	W
	3	KTE											
	5	KTG											
	2	KTP											
	3, 5	KTT		S / SM, S2S / S3S			TS / S		DS		M	T4	
	5	KV				CK	T / TA		T			T	W
	3	KVU		S / SM, CCS / D3S			TD / DT				L	DT, ZT	
	3	PK	RK								X		
	3	LP	T-3			CR	Z / ZA / R					ZR	
TSSOP	8, 14, 16, 20, 24, 28	PW	RU	MTC	PG	UD, UE, UP	MT	DP / PW	DT (Logic), DB (Analog)	L	C	TT, DW	FS, FT
	48, 56, 64	DGG	RV	MTD	PA	UM (48) UN (56)	MTD	DGG	DT (Logic), DA (Analog)	A		TT	FT
TVSOP	14, 16, 20, 24, 48, 56	DGV			PF			DGV		K			
	80	DBB			DF			DGB					
µQFN	10	DQA											
	8	DQE		L8				GF					
	8	DRF				TA				ZA	QW		
	10	DPZ				TB							
	8	DQL											
	8	DQM											
	20	DQS											
	6	DRV											
	6	DRY		L6				GM		ZA		M6	
	6	DSF						GS					
	8, 10	RSE						GM		XA			
	16	RSV						GU				QT	
	10	RSW						GU		ZM			
	14	RUC											
	8, 10	RUG							MU				
VFBGA (MicroStar Jr)	48	ZQC											
	24, 56	ZQL						EV					
	20	ZQN											
	54	ZRD											
	83	ZRG											
	96	ZRL											
	12	ZXU											
	20	ZXY											
WCSP (NanoStar)	29, 81	YFF	CB			BG (81)							
	4, 6, 8, 9, 16, 20, 25	YFP	CB	AC		BS (4), BT (6), BA (8/25), BL (9), BE (16), BP (20)			C			CS	WBG
	5, 6, 8, 10, 20	YZP	CB	AA		BK (5), BT (6), BA (8), BB (10), BP (20)	BL		C	GA / GB		CS	WBG
TAPE & REEL		R		X	T/R 8	T /TR	X	T	T1 / T3 / T4 R1 / R2 / RL	X		R, TR	EL

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