Application Report
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Using the TAS5086 PurePath Digital™ PWM Processor

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ABSTRACT

This application report describes some of the I²C registers of the TAS5086 and how to use them in a PurePath Digital audio system.

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1 Introduction

The TAS5086 PurePath Digital PWM processor inputs eight channels of stereo serial data and outputs six channels of PWM data and two channels of I^2S data.

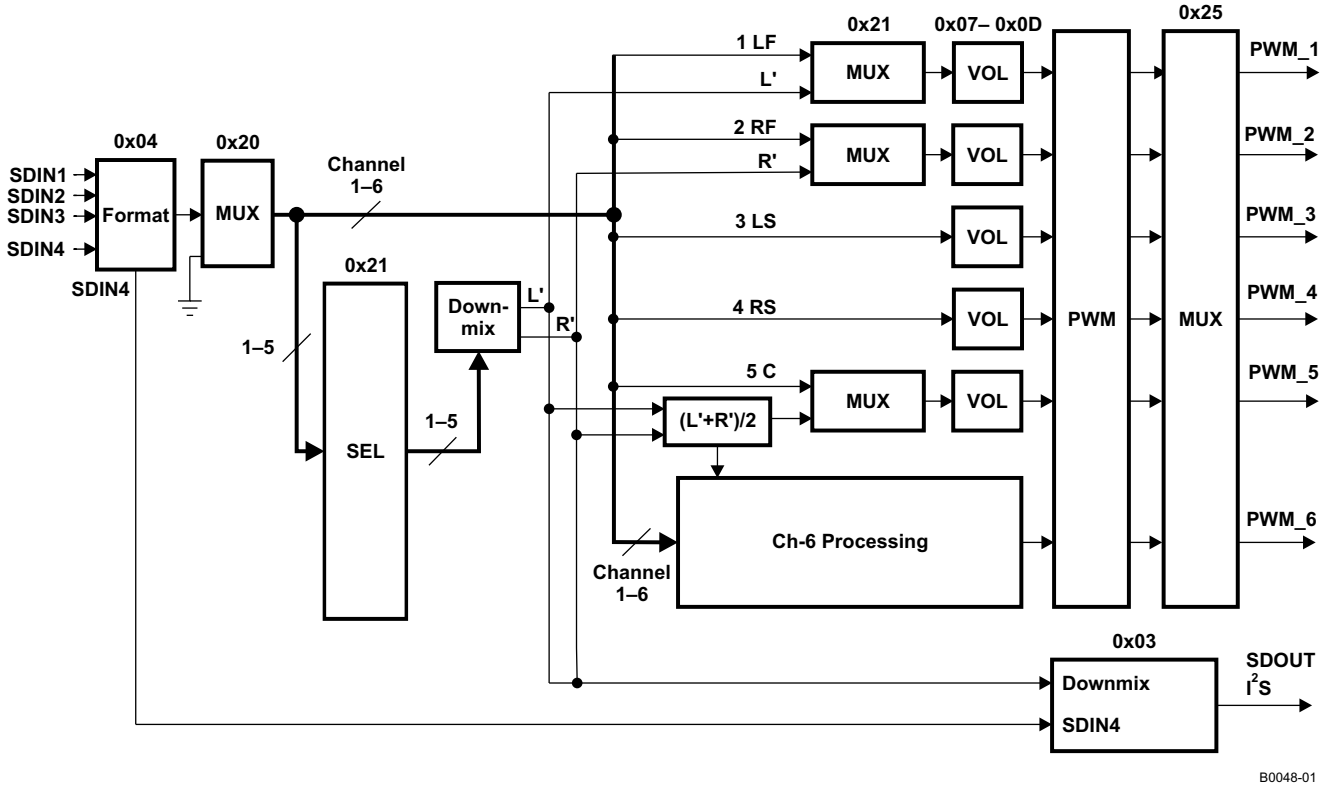

Figure 1. TAS5086 Processing Block Diagram

2 TAS5086 Architecture

Figure 1 shows the high-level TAS5086 processing diagram.

2.1 Serial Data Input

The TAS5086 supports nine different serial stereo modes (see *Serial Interface Control Register 0x04*, Section 4.5). Data is input via stereo inputs SDIN1, SDIN2, and SDIN3. SDIN4 is a pass-through data input only, selected by register 0x03 bit D4.

The six channels input from SDIN1, SDIN2, and SDIN3 are selected for internal processing by the input multiplexer register (register 0x20). Figure 2 shows the TAS5086 GUI panel for register 0x20 used to select which input channel is routed to which internal TAS5086 channel. Note that each multiplexer allows selection of SDIN1-L, SDIN1-R, SDIN2-L, SDIN2-R, SDIN3-L, SDIN3-R, or ZERO data to each TAS5086 internal channel.

Note that the TAS5086 internal channels are dedicated so that channel 1 is left front, channel 2 is right front, channel 3 is left surround, channel 4 is right surround, channel 5 is center, and channel 6 is subwoofer.

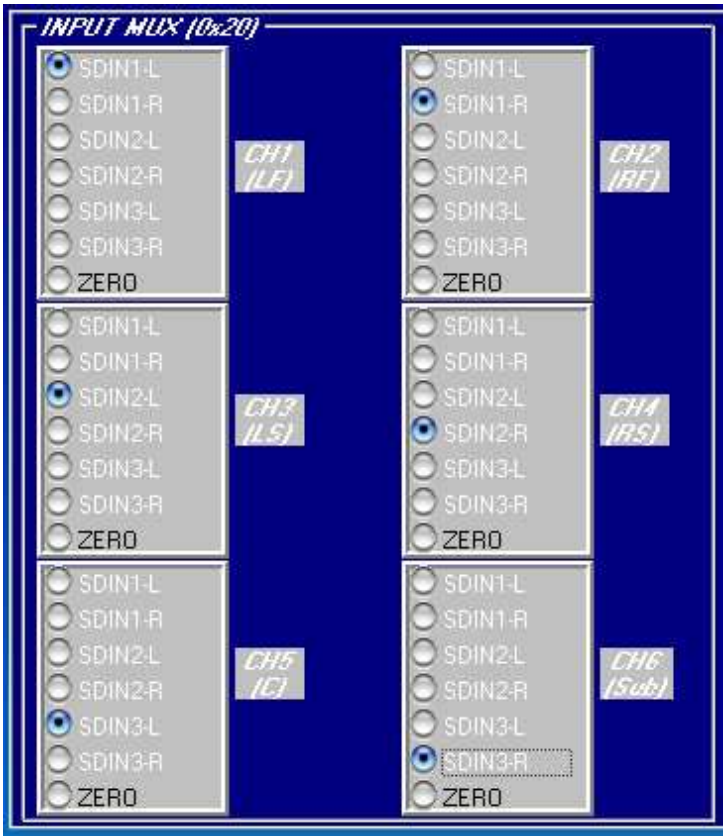

Figure 2. TAS5086 Input Mux (Register 0x20) as Seen in TAS5086 GUI

2.2 Downmix Block

The downmix block takes as input any combination of the internal TAS5086 channels. Figure 3 shows the input multiplexers and how the selected channels are input to the downmix block.

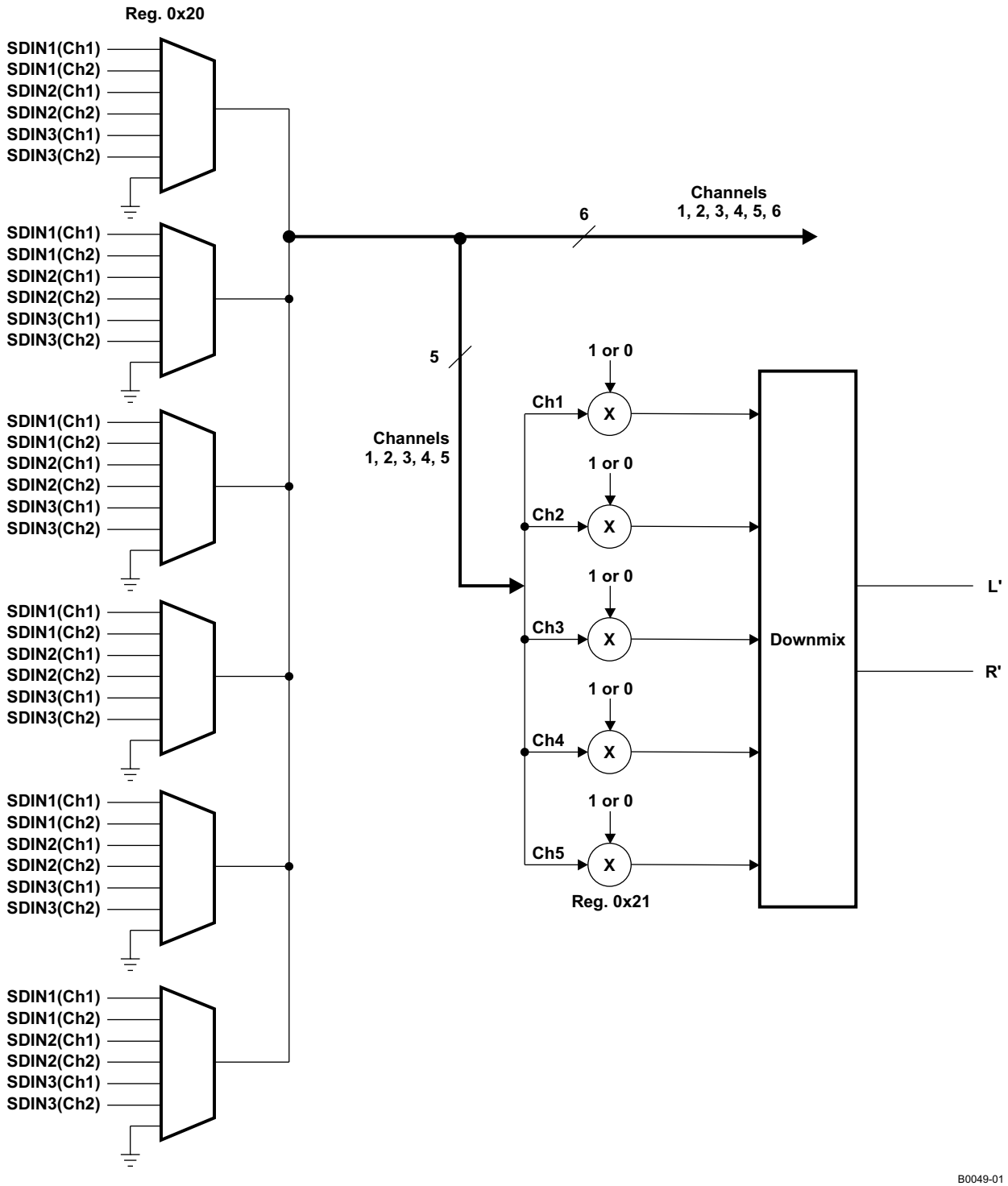

Figure 3. TAS5086 Downmix Block and Input Multiplexers

Note that any or all of channels 1, 2, 3, 4, and 5 can be selected as inputs to the downmix block. Channel 6 is dedicated to the subwoofer channel and is not available for the downmix. The output from the downmix block is downmix-left (L') and downmix-right (R'). Table 1 shows the expected downmix outputs for each combination.

Table 1. Table of Expected Downmix Outputs (in dB)

TAS5086 I²C Register 0x21 (select channels for downmix processing: 1 = process; 0 = do not process)					Downmix Output (Theoretical Values)		
D4 (Ch5-C)	D3 (Ch4-RS)	D2 (Ch3-LS)	D1 (Ch2-R)	D0 (Ch1-L)	L' (dB)	R' (dB)	(L'+R')/2 (dB)
1	1	1	1	1	–20.5	0.0	–5.2
1	1	1	1	0	–12.9	0.0	–8.3
1	1	1	0	1	–20.5	–3.4	–8.3
1	1	1	0	0	–12.9	–3.4	–12.9
1	1	0	1	1	–9.9	–2.2	–5.2
1	1	0	1	0	–∞	–2.2	–8.3
1	1	0	0	1	–9.9	–6.9	–8.3
1	1	0	0	0	–∞	–6.9	–12.9
1	0	1	1	1	–9.9	–2.2	–5.2
1	0	1	1	0	–∞	–2.2	–8.3
1	0	1	0	1	–9.9	–6.9	–8.3
1	0	1	0	0	–∞	–6.9	–12.9
1	0	0	1	1	–5.2	–5.2	–5.2
1	0	0	1	0	–12.9	–5.2	–8.3
1	0	0	0	1	–5.2	–12.9	–8.3
1	0	0	0	0	–12.9	–12.9	–12.9
0	1	1	1	1	–17.5	–2.2	–9.9
0	1	1	1	0	–6.9	–2.2	–15.9
0	1	1	0	1	–17.5	–6.9	–15.9
0	1	1	0	0	–6.9	–6.9	–∞
0	1	0	1	1	–20.5	–5.2	–9.9
0	1	0	1	0	–12.9	–5.2	–15.9
0	1	0	0	1	–20.5	–12.9	–15.9
0	1	0	0	0	–12.9	–12.9	–∞
0	0	1	1	1	–20.5	–5.2	–9.9
0	0	1	1	0	–12.9	–5.2	–15.9
0	0	1	0	1	–20.5	–12.9	–15.9
0	0	1	0	0	–12.9	–12.9	–∞
0	0	0	1	1	–9.9	–9.9	–9.9
0	0	0	1	0	–∞	–9.9	–15.9
0	0	0	0	1	–9.9	–∞	–15.9
0	0	0	0	0	–∞	–∞	–∞

2.3 Channel-6 (Subwoofer) Processing

Figure 4 shows the channel-6 (subwoofer) processing block diagram. This processing includes bass management, an average of downmix processing [(L' + R')/2], channel-6 input multiplexer, volume, gain-compensated biquad, and low-pass biquad. Figure 5 shows the processing panel from the TAS5086 GUI.

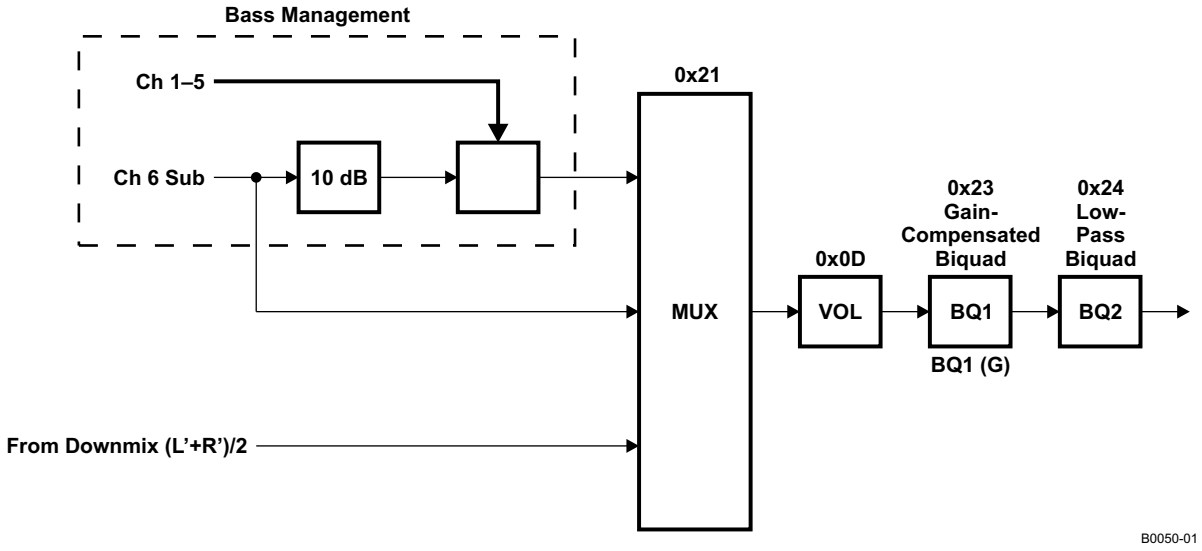

Figure 4. Channel-6 (Subwoofer) Processing Block Diagram

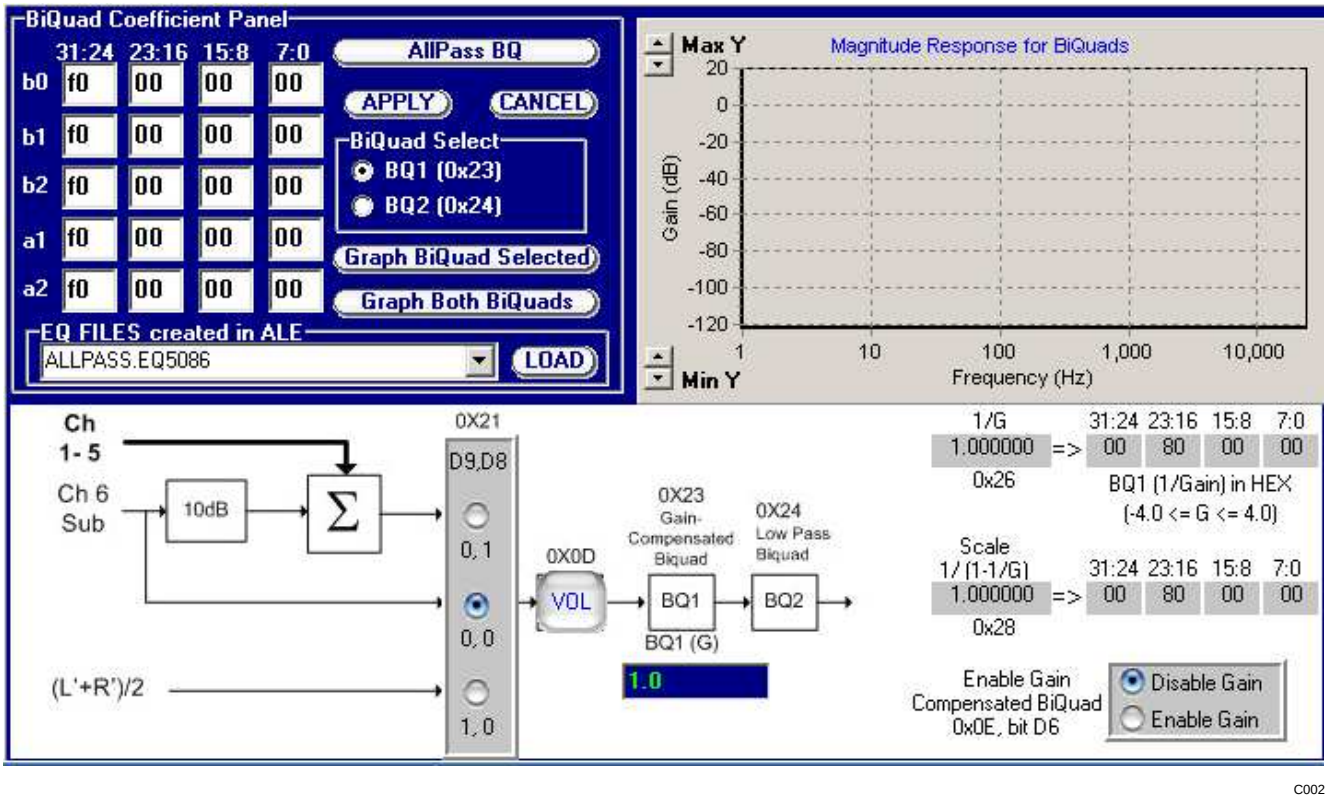

Figure 5. Channel-6 Processing Input Panel From TAS5086 GUI

2.3.1 Bass Management Processing

Figure 6 shows the TAS5086 bass management processing architecture. Note that the only user-programmable blocks are the two biquad filters, BQ1 and BQ2. Bass management processing amplifies the subwoofer by 10 dB and sums in the other five channels. This sum contains low-frequency subwoofer information and full-range information from the other 5 channels. Therefore, the biquad-1 and biquad-2 filters are provided for low-pass filtering the sum before it is output to the subwoofer power amplifier.

Note that biquad 2 (BQ2 – register 0x24) is a regular second-order biquad. Biquad 1 (BQ1 – register 0x23) can also be used as a regular biquad or it can be used as a gain-compensated biquad. See Section 2.3.3 for more information on the gain-compensated biquad.

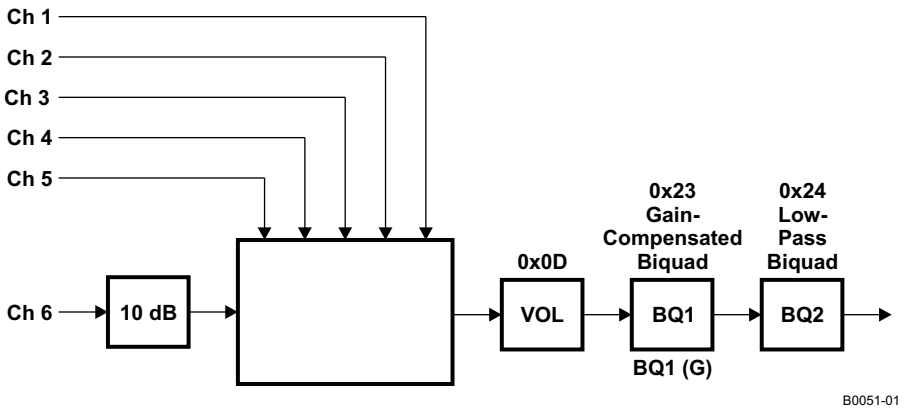

Figure 6. Bass Management Processing

2.3.2 Downmix Input to Channel 6

Another input is the average value of the left (L') and right (R') outputs from the downmix block. This is calculated as (L' + R') / 2. See Table 1 for the theoretical values for this mix.

2.3.3 Gain-Compensated Biquad (Register 0x23)

The gain-compensated biquad provides volume compensation similar to a loudness function. Depending on the BQ1 transfer function, this processing can provide a gain in the bass when the volume is decreased.

The gain-compensated biquad can be loaded into the I^2C register 0x23 as shown in Table 2. Each gain coefficient is in 26-bit (3.23) format; so, 0x800000 is a gain of 1 with a maximum gain of ±4. Each gain coefficient is written as a 32-bit word with the upper six bits not used.

The TAS5086 GUI provides an easy way to try out different biquads.

Table 2 shows the format for register 0x23 and 0x24 biquads BQ1 and BQ2, with the biquad filter structure diagrammed in Figure 7. Note that the default value is unity or all-pass.

Table 2. Biquad Format for Register 0x23 (BQ1) and 0x24 (BQ2)

DESCRIPTION	REGISTER FIELD CONTENTS	DEFAULT GAIN COEFFICIENT VALUES	
		DECIMAL	HEX
b_0 coefficient	u(31:26), b0(25:24), b0(23:16), b0(15:8), b0(7:0)	**1.0**	0x00, **0x80**, 0x00, 0x00
b_1 coefficient	u(31:26), b1(27524), b1(23:16), b1(15:8), b1(7:0)	0.0	0x00, 0x00, 0x00, 0x00
b_2 coefficient	u(31:26), b2(25:24), b2(23:16), b2 (15:8), b2(7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_1 coefficient	u(31:26), a1(25:24), a1(23:16), a1(15:8), a1(7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_1 coefficient	u(31:26), a2(25:24), a2(23:16), a2(15:8) a2(7:0)	0.0	0x00, 0x00, 0x00, 0x00

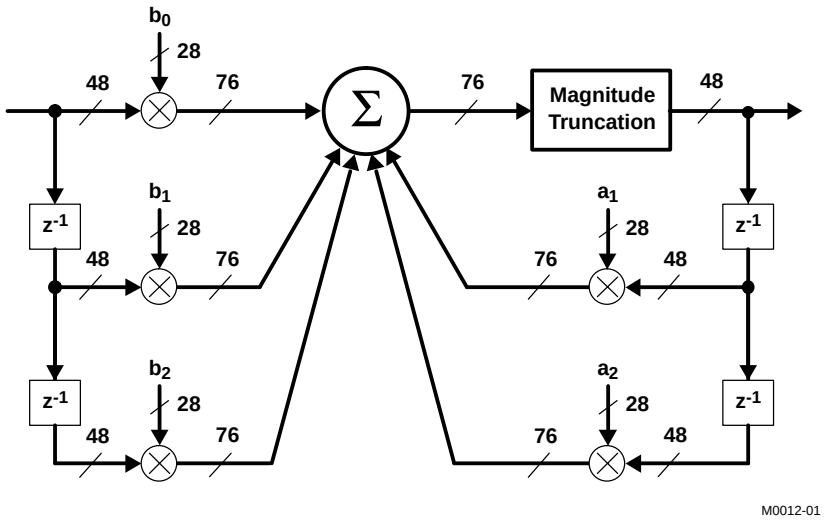

Figure 7. Biquad Filter Structure

Table 3 shows the four registers that must be programmed to use the gain-compensated biquad.

Table 3. Data Registers for Gain-Compensated BQ1 (0x23)

I²C REGISTER	USAGE	DATA FORMAT	COMMENTS
0x0E, bit D6	Enable/disable gain compensation for BQ1	One bit	D6 = 0 disables gain compensation (default) D6 = 1 enables gain compensation
0x23	BQ1 filter coefficients (see Table 2)	3.23 format	Max/min gain = ±4
0x26	1/G	3.23 format	G is the gain of BQ1
0x28	Scale = 1 / (1 – 1/G)	3.23 format	G is the gain of BQ1

3 TAS5086 Oscillator Setup Procedure (READ ME FIRST)

The TAS5086 PWM processor contains an internal oscillator for PLL reference. This reduces system cost because an external reference is not required. Currently, TI recommends a trim resistor value of 18.2 kΩ (1%). This should be connected between TAS5086 pin 14 (OSC_RES) and pin 12 (DVSS).

Two procedures are available for trimming the internal oscillator. The factory-trim procedure is recommended for most users. This procedure simply enables the factory trim that was previously done at the TAS5086 factory.

Note that only one trim procedure should be used. It should always be run following reset of the TAS5086.

3.1 Oscillator Factory-Trim Enable Procedure Example

1. Reset the TAS5086 (power up or toggle the RESET pin).
2. Write data 0x00 to register 0x1B (enable factory trim).
3. Write data 0x20 to register 0x05 (start all channels).
4. Write data 0x30 to register 0x07 (un-mute and set master volume to 0 dB).

3.2 Oscillator Field-Trim Procedure Example (Use only if input LRCLK frequency is known)

1. Reset the TAS5086 (power up or toggle the RESET pin).
2. Provide a known LRCLK (e.g., 48 kHz).
3. Write LRCLK frequency to register 0x00 (e.g., for 48 kHz, write 0x6D to register 0x00). For information on register values for the various clock frequencies, see *Clock Control Register (0x00)* in the *Serial Control Interface Register Summary* section of the *TAS5086 PurePath Digital Audio Six-Channel PWM Processor* data sheet (SLES131).
4. Write data 0x03 to register 0x1B (field-trim command).
5. Write data 0x20 to register 0x05 (start all channels).
6. Write data 0x30 to register 0x07 (un-mute and set master volume to 0 dB).

CAUTION

The oscillator setup procedure must be done only once for each reset of the TAS5086. Doing multiple trim procedures without resetting first can cause unknown effects.

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