Application Report
SLEA103–July 2010

TVP5151 VBI Quick Start

ABSTRACT

The TVP5151 video decoder has an internal vertical data processor (VDP) that can be used to slice various VBI data services such as V-Chip, Teletext (WST, NABTS), closed captioning (CC), wide screen signaling (WSS), copy generation management system (CGMS), video program system (VPS), electronic program guide (EPG or Gemstar), program delivery control (PDC) and vertical interval time code (VITC). This application report provides an introduction to the VBI data slicing capabilities of the TVP5151 and focuses on configuring the TVP5151 for the more commonly used VBI data services.

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1 Introduction

The TVP5151 video decoder has an internal Vertical Data Processor (VDP) that can be used to slice various VBI data services such as V-Chip, Teletext (WST, NABTS), Closed Captioning (CC), Wide Screen Signaling (WSS), Copy Generation Management System (CGMS), Video Program System (VPS), Electronic Program Guide (EPG or Gemstar), Program Delivery Control (PDC), and Vertical Interval Time Code (VITC). These data services are typically transmitted during the vertical blanking interval of the video frame. Table 1 provides a summary of the supported data services including the line numbers on which they are typically transmitted.

Table 1. Supported Data Services

VBI System	Standard	Line Number	Number of Bytes	Specification
Teletext WST A	SECAM	6-23 (field 1, 2)	38	ITU-R BT 653-3
Teletext WST B	PAL	6-22 (field 1, 2)	43	ITU-R BT 653-3
Teletext NABTS C	NTSC-M	10-21 (field 1, 2)	34	ITU-R BT 653-3
Teletext NABTS D	NTSC-J	10-21 (field 1, 2)	35	ITU-R BT 653-3
Closed Caption	PAL	22 (field 1, 2)	2	EIA-608-D
Closed Caption	NTSC	21 (field 1, 2)	2	EIA-608-D
WSS/CGMS	PAL	23 (field 1, 2)	14 bits	ITU-R BT 1119-1
WSS/CGMS	NTSC	20 (field 1, 2)	20 bits	IEC 61880
VITC	PAL	6-22	9	SMPTE 12M-1999
VITC	NTSC	10-20	9	SMPTE 12M-1999
VPS (PDC)	PAL	16	13	ETS 300 231
V-ChiP	NTSC	21 (field 2)	2	EIA-744-A
Gemstar 1x	NTSC		2	
Gemstar 2x	NTSC		5 with frame byte	
User	Any	Programmable	Programmable	

A host or backend receiver can retrieve the sliced data using one of three methods:

- I^2C access of dedicated Closed Caption, WSS, CGMS, VPS, Gemstar, VITC, and V-Chip data registers.
- I^2C access of an internal 512-byte FIFO used primarily for high-bandwidth data services such as full-field teletext.
- As ITU-R BT.656 ancillary data, inserted by the TVP5151 in the data stream during the horizontal blanking interval.

Note: This document will focus primarily on the more commonly used dedicated I^2C data registers.

Prior to accessing the VBI sliced data, the TVP5151 must be configured for the desired VBI data service. This includes loading of the VDP Configuration RAM (C-RAM) and the Line Mode registers that are used to enable various data services. Detailed descriptions of the VBI related I^2C registers are shown in Appendix A.

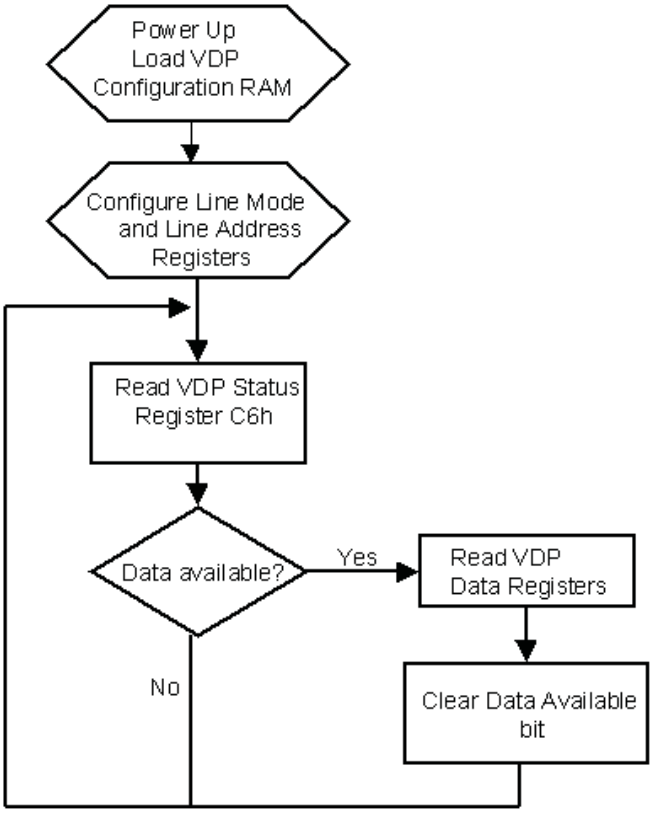

Figure 1. The VDP Configuration RAM is Loaded Prior to Line Mode Register Setup

2 VDP Configuration RAM

The first step in configuring the TVP5151 for VBI data slicing is to load the VDP Configuration RAM (C-RAM). The C-RAM defines the data slicing modes for the various data services, with each mode having its own unique RAM address and 16 byte block of memory. Table 2 shows the recommended setup values for the various data services that are supported. Prior to loading the C-RAM, the Line Mode registers must all be programmed with a value of FFh to avoid conflict between the VDP and microprocessor during the load process. Full field mode must also be disabled in I^2C register CFh.

Table 2. Configuration RAM Recommended Settings

Index	Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Reserved	000h	Reserved															
WST SECAM	010h	AA	AA	FF	FF	E7	2E	20	A6	E4	B4	OE	0	7	0	10	0
Reserved	020h	Reserved															
WST PAL B	030h	AA	AA	FF	FF	27	2E	20	AB	A4	72	10	0	7	0	10	0
Reserved	040h	Reserved															
WST PAL C	050h	AA	AA	FF	FF	E7	2E	20	22	A4	98	0D	0	0	0	10	0
Reserved	060h	Reserved															
WST NTSC	070h	AA	AA	FF	FF	27	2E	20	23	63	93	0D	0	0	0	10	0
Reserved	080h	Reserved															
NABTS, NTSC	090h	AA	AA	FF	FF	E7	2E	20	A2	63	93	0D	0	7	0	15	0
Reserved	0A0h	Reserved															
NABTS, NTSC-J	0B0h	AA	AA	FF	FF	A7	2E	20	A3	63	93	0D	0	7	0	10	0
Reserved	0C0h	Reserved															
CC, PAL/SECAM	0D0h	AA	2A	FF	3F	04	51	6E	02	A4	7B	09	0	0	0	27	0
Reserved	0E0h	Reserved															
CC, NTSC	0F0h	AA	2A	FF	3F	04	51	6E	02	63	8C	09	0	0	0	27	0
Reserved	100h	Reserved															
WSS/CGMS, PAL/SECAM	110h	5B	55	C5	FF	0	71	6E	42	A4	CD	0F	0	0	0	3A	0
Reserved	120h	Reserved															
WSS/CGMS, NTSC C	130h	38	0	3F	0	0	71	6E	43	63	7C	08	0	0	0	39	0
Reserved	140h	Reserved															
VITC, PAL/SECAM	150h	0	0	0	0	0	8F	6D	49	A4	85	08	0	0	0	4C	0
Reserved	160h	Reserved															
VITC, NTSC	170h	0	0	0	0	0	8F	6D	49	63	94	08	0	0	0	4C	0
Reserved	180h	Reserved															
VPS, PAL	190h	AA	AA	FF	FF	BA	CE	2B	8D	A4	DA	0B	0	7	0	60	0
Reserved	1A0h	Reserved															
Gemstar Custom 1	1B0h	99	99	FF	FF	05	51	6E	05	63	18	13	80	0	0	60	0

The C-RAM is accessed through the use of three I^2C registers (C3h-C5h). Registers C4h and C5h must be programmed with the 9-bit starting address of the block of C-RAM to be programmed. I^2C read and write operations are then performed indirectly using register C3h. The C-RAM address is automatically incremented following each I^2C transaction. Only the portion of the C-RAM that includes the data service to be used needs to be programmed. If WSS/CGMS for NTSC is the only desired data service, for example, only the 16 bytes starting at C-RAM address 130h need to be programmed. Figure 2 shows example C code for loading the WSS/CGMS C-RAM.

Configuration RAM I²C Access Registers

Address	C3h-C5h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address [7:0]							
C5h	Reserved							RAM address 8

Example: (Write 2 data bytes starting at C-RAM address 130h)

1. Set C-RAM starting address.
   (a) Write 30h to register C4h (C-RAM address [7:0]).
   (b) Write 01h to register C5h (C-RAM address [8]).
2. Write the two bytes (38h and 00h)
   (a) Write 38h to register C3h. Write first byte to C-RAM address 130h.
   (b) Write 00h to register C3h. Write next byte to C-RAM address 131h.

```
// TVP5151 NTSC WSS/CGMS C-RAM Load Example

#define TVP5151 0xB8;                      // TVP5151 main I2C address
byte I2C_Data;
int CRAM_Address, count;

byte I2CData ={0x14,0x02};

// recommended WSS/CGMS settings
byte WSS_ARRAY[]={0x38,0,0x3F,0,0,0x71,0x6E,0x43,0x63,0x7C,0x08,0,0,0,0x39,0};

I2C_RegAddress = 0xD0;                      // starting address of Line Mode registers
I2C_Data = 0xFF;
For (count = 0; count < 44; count ++)
{
  I2CWriteByte(TVP5151, I2C_RegAddress, I2C_Data);  //write FFh to Line Mode registers
I2C_RegAddress ++;
}
I2CWriteByte(TVP5151, 0xCF, 0);                 // disable full field mode
CRAM_Address = 0x130;                            // address of NTSC WSS/CGMS C-RAM block

I2CWriteByte(TVP5151, 0xC4, 0x30);              // load C4h with C-RAM address[7:0]

I2CWriteByte(TVP5151, 0xC5, 0x01);              // load C5h with C-RAM address[8]

For (count = 0; count < 16; count++)
{
  I2CWriteByte(TVP5151, 0xC3, WSS_ARRAY[count]);  // write 16 bytes of WSS/CGMS C-RAM
}                                                  // data to register C3h.
```

Figure 2. Example Load of WSS/CGMS Configuration RAM

3 Line Mode Registers

After the VDP Configuration RAM is loaded, the Line Mode Registers (D0h-FBh) must be properly configured for the desired VBI data service. Each register in this register bank is linked to a specific video line number and video field. Video lines 6 through 27 of both Field 1 and Field 2 are supported. For each desired data service, the proper mode configuration bits need to be loaded into the line mode register that is linked to the correct video line number. Additional data slicing options such as filtering, error correction, and FIFO routing are also available in the line mode registers. Unused line mode and line address registers must be programmed with FFh. A detailed description of these registers is shown in Appendix A.

The TVP5151 VDP is based on an NTSC line numbering convention, resulting in a 3-line VDP offset relative to actual PAL line numbers. For PAL systems, the Line Mode register for line "N+3" must be used to configure a data service transmitted on line N of the input source. Figure 3 shows example C code for configuring WSS/CGMS data services for NTSC and PAL. Included in this example is an I^2C write to the Pixel Alignment Registers (CBh-CCh), which define the horizontal position where data slicing begins. The value used (4Eh) is recommended for all data services.

Table 3. Line Mode Configuration Bits for Supported Modes

Line Mode Register (D0h-FCh) Bits [3:0]	Name	Video Line Number	Description
0000b	WST SECAM	6-23 (field 1, 2)	Teletext, SECAM
0001b	WST PAL B	6-22 (field 1, 2)	Teletext, PAL, System B
0010b	WST PAL C	6-22 (field 1, 2)	Teletext, PAL, System C
0011b	WST, NTSC B	10-21 (field 1, 2)	Teletext, NTSC, System B
0100b	NABTS, NTSC C	10-21 (field 1, 2)	Teletext, NTSC, System C
0101b	NABTS, NTSC D	10-21 (field 1, 2)	Teletext, NTSC, System D (Japan)
0110b	CC, PAL/SECAM	22 (field 1, 2)	Closed caption PAL/SECAM
0111b	CC, NTSC	21 (field 1, 2)	Closed caption NTSC
1000b	WSS/CGMS, PAL/SECAM	23 (field 1, 2)	Wide-screen signal, PAL/SECAM
1001b	WSS/CGMS, NTSC	20 (field 1, 2)	Wide-screen signal, NTSC
1010b	VITC, PAL/SECAM	6-22	Vertical interval timecode, PAL/SECAM
1011b	VITC, NTSC	10-20	Vertical interval timecode, NTSC
1100b	VPS, PAL	16	Video program system, PAL
1101b	EPG/Gemstar		Electronic program guide - Custom mode
1110b	x	x	Reserved
1111b	Active Video	Active Video	Active video/full field

```
// Example C Code for setting up WSS/CGMS Line Mode Registers
//
// Load C-RAM
//
// NTSC WSS/CGMS Line Mode setup for line 20 of both fields

I2CWriteByte(TVP5151, 0xEC, 0x09);  // line 20 field 1 (0xEC), mode bits = 0x09
I2CWriteByte(TVP5151, 0xED, 0x09);  // line 20 field 2 (0xED), mode bits = 0x09

I2CWriteByte(TVP5151, 0xCB, 0x4E);  // Set Pixel Alignment [7:0]to 0x4E
I2CWriteByte(TVP5151, 0xCC, 0x00);  // Set Pixel Alignment [9:8]to 0x00

// PAL WSS/CGMS Line Mode setup for line 23 (source input) of both fields.
// PAL line numbering has 3 line offset so the Line 26 line mode registers are used.

I2CWriteByte(TVP5151, 0xF8, 0x08);  // line 26 field 1 (0xF8), mode bits = 0x08
I2CWriteByte(TVP5151, 0xF9, 0x08);  // line 26 field 2 (0xF9), mode bits = 0x08

I2CWriteByte(TVP5151, 0xCB, 0x4E);  // Set Pixel Alignment [7:0]to 0x4E
I2CWriteByte(TVP5151, 0xCC, 0x00);  // Set Pixel Alignment [9:8]to 0x00
```

Figure 3. Line Mode Setup for WSS/CGMS

4 Sliced Data Retrieval

The TVP5151 provides dedicated I²C registers (see Table 4) for the retrieval of sliced data. Due to higher bandwidth requirements, teletext data is stored in a 512-byte FIFO. With all other data services, sliced data can be automatically sent to the dedicated registers or to the FIFO depending on the line mode setup. The WSS/CGMS example in Figure 3 results in WSS/CGMS data being routed to the dedicated WSS/CGMS data registers.

Table 4. Dedicated VDP Data Registers

Register Name	I²C Address
VDP Closed Caption Data (field 1)	90h - 91h
VDP Closed Caption Data (field 2)	92h - 93h
VDP WSS/CGMS Data (field 1)	94h - 96h
VDP WSS/CGMS Data (field 2)	97h - 99h
VDP VPS (PAL) /Gemstar 2x (NTSC) Data	9Ah - A6h
VDP VITC Data	A7h - AFh

The internal 512-byte FIFO is used primarily for high-bandwidth teletext acquisition but can also be used for capture of the other data services if enable in the Line Mode register. A header containing information about the sliced data precedes all sliced data that is routed to the FIFO. The FIFO can be directly accessed by the host at I²C address B0h. Bit 0 of the FIFO output control register (CDh) must be set to a logic1 to enable host access to the FIFO.

5 Managing Data Retrieval

The VDP Status Registers (C6h) can be used to determine if sliced data is available. Unmasked data available bits for the supported data services are available in this register.

VDP Status Register

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS/CGMS available	VPS/Gemstar 2x available	VITC available

A logic 1 indicates that sliced data is available. Once set, these bits need to be cleared after data retrieval. Writing a 1 to the appropriate bit(s) in this register clears the status bit. Figure 4 shows an example WSS/CGMS data retrieval.

```
// Example C Code for WSS/CGMS NTSC Sliced Data Read

// Load C-RAM

// Configure Line Mode Registers

byte Status;
byte WSSData[3];

I2CReadBuffer(TVP5151,0xC6,&Status,1);  //read 1 byte(status)from register C6h

if ((Status & 0x20) == 1)
{
  I2CReadBuffer(TVP5151,0x94,&WSSData[0],3);  // if WSS/CGMS bit set,
                                               // read the 3 WSS/CGMS bytes
                                               // at WSS/CGMS data registers 94h-96h.
  I2CWriteByte(TVP5151,0xC6,0x20);            // clear WSS/CGMS available status bit
}
```

Figure 4. Example WSS/CGMS Data Retrieval

6 FIFO Access

The internal 512-byte FIFO is used primarily for high-bandwidth teletext acquisition but can also be used for capture of the other data services. The FIFO can be directly accessed by the host at I^2C address B0h. Bit 0 of the VDP FIFO output control register (CDh) must be set to logic 1 to enable host access to the FIFO. A header containing information about the sliced data precedes all sliced data that is routed to the FIFO. A VDP FIFO Interrupt threshold register (C8h), FIFO word count register (C7h), and FIFO full/empty status bits (C6h) are available for managing FIFO data flow.

7 Ancillary Data

An option is available to enable transmission of sliced VBI data as ancillary data in the ITU-R BT.656 video data stream. In this mode, the sliced data is inserted on the Y[7:0] output terminals during the horizontal blanking interval. An 8-byte header containing information about the sliced data is also inserted in the data stream prior to the sliced data. The header includes a 00h, FFh, FFh preamble that identifies the data as VBI ancillary data, so the host or backend must be able to distinguish between this preamble and the ITU-R BT.656 embedded sync codes (FFh, 00h, 00h, E/SAV). The first header byte is inserted immediately following the EAV code during the horizontal blanking interval of the digital line where it occurred. The ancillary data header is summarized in Table 5.

The ancillary data mode is enabled by setting bit 6 in the appropriate line-mode register to a logic 1 and the host-access enable bit (bit 0) in register CDh to a logic 0. When the ancillary data mode is enabled in register CDh, sliced data is not routed to the internal 512-byte FIFO.

Table 5. Ancillary Data Header

Byte No.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	Description	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal Data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video Line # [9:8]		Internal Data ID1 (IDID1)	
8	1. Data								Data byte	1st word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
...	...								...	
	m-1. Data								Data byte	Nth word
	m. Data								Data byte	
	CS [7:0]								Checksum	
4N + 7	0	0	0	0	0	0	0	0	Fill byte	

EP: Even parity for D0-D5

NEP: Negate even parity

DID: 91h: Sliced data from the vertical blanking interval of first field

53h: Sliced data from outside of the vertical blanking interval of first field

55h: Sliced data from the vertical blanking interval of second field

97h: Sliced data from outside of the vertical blanking interval of second field

SDID: This field holds the data format taken from the line-mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4N+7. Note that each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1: Transaction video line number [9:8].

Bit 2: Match 2 flag.

Bit 3: Match 1 flag.

Bit 4: Value = 1 if a single error was detected in the EDC block. Value = 0 if no error was detected.

CS: Sum of D0-D7 of 1.Data through last data byte.

Fill byte: Fill byte makes a multiple of 4 bytes from byte zero to last fill byte.

Note: The number of bytes (m) varies depending on the VBI data service.

8 Full-Field Mode

Some teletext services transmit data on multiple video lines occurring anywhere in the video field. The TVP5151 provides a full-field mode which arms VDP slicing for all lines in the video field. When full-field mode is enabled, all video lines excluding those defined in the line-mode registers are sliced as specified in the VDP full-field mode register (FCh). The full-field mode register uses the same mode configuration format as the line-mode registers. Full-field mode is enabled by setting the full-field enable bit in register CFh to a logic 1. Sliced data is then retrieved by I^2C FIFO access or as ancillary data in the ITU-R BT.656 data stream.

9 VBI Raw Data Mode

The TVP5151 offers a VBI raw data mode for use in systems where VBI data slicing and processing is handled in the digital backend receiver instead of the video decoder. In this mode of operation, the decoders are configured to output raw 2x over-sampled luma data on the ITU-R BT.656 output during the defined VBLK (vertical blanking) interval. The raw, un-sliced A/D video data is transmitted during the active video portion of the line with chroma samples being replaced with the luma samples.

The default VBLK interval for Field 1 is defined as lines 1 through 20 for 525-line video formats and lines 623 through 23 for 625-line video formats. This interval may be adjusted to include additional lines. Support for NTSC line 21 closed caption data, for example, requires extension of the VBLK interval to include line 21.

The default VBLK interval for the TVP5151 is defined as lines 1 through 20 for 525-line video formats and lines 623 through 23 for 625-line formats. The TVP5151 VBLK interval can be adjusted with the VBLK Start and Stop registers (18h-19h). The TVP5151 VBLK Start and Stop registers provide relative adjustments to the default VBLK interval. After configuring the desire VBLK interval, the Luma bypass (bit 4) in the Luminance Processing Control #1 register (07h) must be set to a logic 1 to enable raw data output. Table 6 shows the default I^2C registers with a modified VBLK interval for Line 21 inclusion, while Table 7 shows the default 625-line setup. Also shown in Figure 5 and Figure 6 are digital captures of the TVP5151 ITU-R BT.656 output for comparison of normal operation and raw data operation. Insertion of a 4-byte preamble (00h FFh FFh 60h) prior to the start of the raw data is optional in I^2C register 07h.

Table 6. 525-Line Raw Data Setup to Include Line 21

I^2C Subaddress	Default	I^2C Data	Description
07h	00h	10h	Enable raw data (Luma bypass) and Preamble
18h	00h	00h	VBLK Start = default line 1
19h	00h	01h	VBLK Stop = default +1 to include line 21

Table 7. 625-Line Raw Data Setup

I^2C Subaddress	Default	I^2C Data	Description
07h	00h	10h	Enable raw data (Luma bypass) and Preamble
18h	00h	00h	VBLK Start LSB = default line 623
19h	00h	00h	VBLK Stop = default

Note: Detailed descriptions of the TVP5151 I^2C registers related to VBI Raw Data Mode are shown in Appendix A.

Example (set up NTSC for raw data on lines 1 through 21)

1. Set up VBLK interval.
   - Write 01h to register 19h to include line 21.
2. Enable Raw Data Mode
   - Write 10h to register 07h to enable raw data mode.

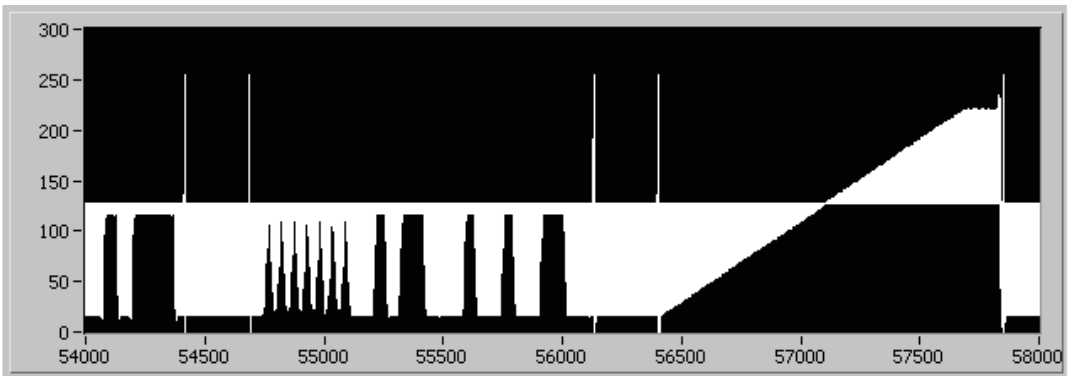

Figure 5. Line 21 Closed Caption ITU-R BT.656 Digital Output Capture with YUV Samples Present Raw Data Mode Disabled

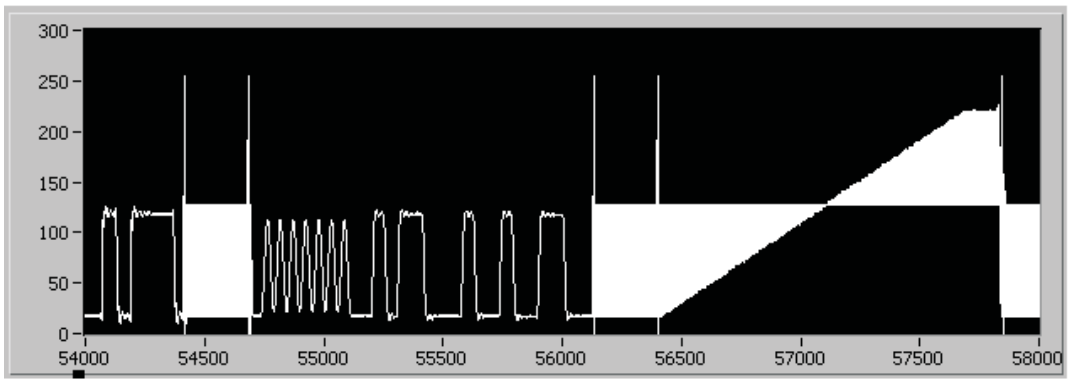

Figure 6. Line 21 Closed Caption ITU-R BT.656 Digital Output Capture in Raw Data Mode UV (Chroma) Data are Replaced with Y (Luma) Data

Note: The full-scale transitions are embedded sync codes.

Appendix A Subset of the TVP5151 VDP I²C Registers

VDP Closed Caption Data

Address	90h-93h

Ready only

Address	7	6	5	4	3	2	1	0
90h	Closed Caption Field 1 byte 1							
91h	Closed Caption Field 1 byte 2							
92h	Closed Caption Field 2 byte 1							
93h	Closed Caption Field 2 byte 2							

These registers contain the closed caption data arranged in bytes per field.

VDP WSS/CGMS Data

Address	94h-99h

WSS/CGMS NTSC:
Read only

Address	7	6	5	4	3	2	1	0	Byte
94h			b5	b4	b4	b2	b1	b0	WSS/CGMS Field 1 byte 1
95h	b13	b12	b11	b10	b9	b8	b7	b6	WSS/CGMS Field 1 byte 2
96h			b19	b18	b17	b16	b15	b14	WSS/CGMS Field 1 byte 3
97h			b5	b4	b4	b2	b1	b0	WSS/CGMS Field 2 byte 1
98h	b13	b12	b11	b10	b9	b8	b7	b6	WSS/CGMS Field 2 byte 2
99h			b19	b18	b17	b16	b15	b14	WSS/CGMS Field 2 byte 3

These registers contain the wide screen signaling data for NTSC.

- Bits 0 - 1 Represent word 0, aspect ratio
- Bits 2 - 5 Represent word 1, header code for word 2
- Bits 6 - 13 Represent word 2, copy control
- Bits 14 - 19 Represent word 3, CRC

WSS/CGMS PAL/SECAM:
Read only

Address	7	6	5	4	3	2	1	0	Byte
94h	b7	b6	b5	b4	b4	b2	b1	b0	WSS/CGMS Field 1 byte 1
95h			b13	b12	b11	b10	b9	b8	WSS/CGMS Field 1 byte 2
96h	Reserved								
97h	b7	b6	b5	b4	b4	b2	b1	b0	WSS/CGMS Field 2 byte 1
98h			b13	b12	b11	b10	b9	b8	WSS/CGMS Field 2 byte 2
99h	Reserved								

These registers contain the wide screen signaling data for PAL/SECAM:

- Bits 0 - 3 Represent group 1, aspect ratio
- Bits 4 - 7 Represent group 2, enhanced services
- Bits 8 - 10 Represent group 3, subtitles
- Bits 11 - 13 Represent group 4, others

VDP VPS, EPG Data

Address	9Ah-A6h

VPS:
Read only

Address	7	6	5	4	3	2	1	0
9Ah	VPS byte 1							
9Bh	VPS byte 2							
9Ch	VPS byte 3							
9Dh	VPS byte 4							
9Eh	VPS byte 5							
9Fh	VPS byte 6							
A0h	VPS byte 7							
A1h	VPS byte 8							
A2h	VPS byte 9							
A3h	VPS byte 10							
A4h	VPS byte 11							
A5h	VPS byte 12							
A6h	VPS byte 13							

These registers contain the entire VPS data line except the clock run-in code or the frame code.

EPG:
Read only

Address	7	6	5	4	3	2	1	0
9Ah	EPG Frame Code							
9Bh	EPG byte 1							
9Ch	EPG byte 2							
9Dh	EPG byte 3							
9Eh	EPG byte 4							
9Fh	Reserved							
A0h	Reserved							
A1h	Reserved							
A2h	Reserved							
A3h	Reserved							
A4h	Reserved							
A5h	Reserved							
A6h	Reserved							

VDP VITC Data

Address	A7h-AFh

Read only

Address	7	6	5	4	3	2	1	0
A7h	VITC Frame byte 1							
A8h	VITC Frame byte 2							
A9h	VITC Seconds byte 1							
AAh	VITC Seconds byte 2							
ABh	VITC Minutes byte 1							
ACh	VITC Minutes byte 2							
ADh	VITC Hours byte 1							
AEh	VITC Hours byte 2							
AFh	VITC CRC byte							

These registers contain the VITC data.

VDP FIFO Read Data

Address	B0h

Read only

7	6	5	4	3	2	1	0
FIFO read data [7:0]							

FIFO read data [7:0]: This register is provided to access VBI FIFO data through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, the FIFO output control register CDh bit 0 must be set to 1.

VDP Configuration RAM Register

Address	C3h-C5h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address [7:0]							
C5h	Reserved							RAM address 8

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes organized as 32 different configurations of 16 bytes each. The first 12 configurations are defined for the current VBI standards. An additional 2 configurations can be used as a custom programmed mode for unique standards like Gemstar.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9-bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h-FBh must all be programmed with FFh, before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

VDP Status

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS/CGMS available	VPS/Gemstar 2x available	VITC available

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

0 No FIFO full error

1 FIFO was full during a write to FIFO.

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, this goes into the FIFO. Even if the full error flag is set.

FIFO empty:

0 FIFO is not empty.

1 FIFO is empty.

TTX available:

0 Teletext data is not available.

1 Teletext data is available.

CC field 1 available:

0 Closed caption data from field 1 is not available.

1 Closed caption data from field 1 is available.

CC field 2 available:

0 Closed caption data from field 2 is not available.

1 Closed caption data from field 2 is available.

WSS/CGMS available:

0 WSS/CGMS data is not available.

1 WSS/CGMS data is available.

VPS/Gemstar 2x available:

0 VPS/Gemstar 2x data is not available.

1 VPS/Gemstar 2x data is available.

VITC available:

0 VITC data is not available.

1 VITC data is available.

VDP FIFO Word Count

Address	C7h

7	6	5	4	3	2	1	0
Number of words							

This register provides the number of words in the FIFO. 1 word equals 2 bytes.

VDP FIFO Interrupt Threshold

Address	C8h

7	6	5	4	3	2	1	0
Number of words							

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. 1 word equals 2 bytes.

VDP FIFO Reset

Address	C9h

7	6	5	4	3	2	1	0
Any data							

Writing any data to this register resets the FIFO and clears any data present.

VDP Line Number Interrupt

Address	CAh

7	6	5	4	3	2	1	0
Field 1 enable	Field 2 enable	Line number					

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. The value of 0 or 1 does not generate an interrupt.

Field 1 enable:

- 0 Disabled (default)
- 1 Enabled

Field 2 enable:

- 0 Disabled (default)
- 1 Enabled

Line number: (default 00h)

VDP Pixel Alignment

Address	CBh-CCh

Address	7	6	5	4	3	2	1	0
CBh	Switch pixel [7:0]							
CCh	Reserved						Switch pixel [9:8]	

These registers form a 10-bit horizontal pixel position from the falling edge of sync, where the VDP controller initiates the program from one line standard to the next line standard. For example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

VDP FIFO Output Control

Address	CDh

Default (00h)

7	6	5	4	3	2	1	0
Reserved							Host access enable

Host access enable: This register is programmed to allow host port access to the FIFO or allow all VDP data to go out the video port.

. 0 Output FIFO data to the video output Y[7:0]

1 Allow host port access to the FIFO data (default)

VDP Full-Field Enable

Address	CFh

Default (00h)

7	6	5	4	3	2	1	0
Reserved							Full field enable

Full field enable:

. 0 Disable full field mode (default)

1 Enable full field mode

This register enables the full-field mode. In this mode, all lines outside the vertical blank area and all lines in the line-mode register programmed with FFh are sliced with the definition of register FCh. Values other than FFh in the line-mode registers allow a different slice mode for that particular line.

VDP Line Mode

Address	D0h-FBh

Address	7	6	5	4	3	2	1	0
D0h	Line 6 Field 1							
D1h	Line 6 Field 2							
D2h	Line 7 Field 1							
D3h	Line 7 Field 2							
D4h	Line 8 Field 1							
D5h	Line 8 Field 2							
D6h	Line 9 Field 1							
D7h	Line 9 Field 2							
D8h	Line 10 Field 1							
D9h	Line 10 Field 2							
DAh	Line 11 Field 1							
DBh	Line 11 Field 2							
DCh	Line 12 Field 1							
DDh	Line 12 Field 2							
DEh	Line 13 Field 1							
DFh	Line 13 Field 2							
E0h	Line 14 Field 1							
E1h	Line 14 Field 2							
E2h	Line 15 Field 1							
E3h	Line 15 Field 2							
E4h	Line 16 Field 1							
E5h	Line 16 Field 2							
E6h	Line 17 Field 1							
E7h	Line 17 Field 2							
E8h	Line 18 Field 1							
E9h	Line 18 Field 2							
EAh	Line 19 Field 1							
EBh	Line 19 Field 2							
ECh	Line 20 Field 1							
EDh	Line 20 Field 2							
EEh	Line 21 Field 1							
EFh	Line 21 Field 2							
F0h	Line 22 Field 1							
F1h	Line 22 Field 2							
F2h	Line 23 Field 1							
F3h	Line 23 Field 2							
F4h	Line 24 Field 1							
F5h	Line 24 Field 2							
F6h	Line 25 Field 1							
F7h	Line 25 Field 2							
F8h	Line 26 Field 1							
F9h	Line 26 Field 2							
FAh	Line 27 Field 1							
FBh	Line 27 Field 2							

(continued)

These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

0 Disable filtering of null bytes in closed caption modes

1 Enable filtering of null bytes in closed caption modes (default)

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, then the data filter passes all data on that line.

Bit 6:

0 Send VBI data to registers only.

1 Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

0 Allow VBI data with errors in the FIFO

1 Do not allow VBI data with errors in the FIFO (default)

Bit 4:

0 Do not enable error detection and correction

1 Enable error detection and correction (when bits [3:0] = 1 2, 3, and 4 only) (default)

Bits [3:0]:

0000 WST SECAM
0001 WST PAL B
0010 WST PAL C
0011 WST NTSC
0100 NABTS NTSC
0101 TTX NTSC
0110 CC PAL
0111 CC NTSC
1000 WSS/CGMS-A PAL
1001 WSS/CGMS NTSC
1010 VITC PAL
1011 VITC NTSC
1100 VPS PAL
1101 Gemstar 2x Custom 1
1110 Custom 2
1111 Active video (VDP off) (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

VDP Full-Field Mode

Address	FCh

Default (7Fh)

7	6	5	4	3	2	1	0
Full field mode [7:0]							

Full field mode [7:0]: This register programs the specific VBI standard for full-field mode. It can be any VBI standard. Individual line settings take priority over the full-field register. This allows each VBI line to be programmed independently but have the remaining lines in full-field mode. The full-field mode register has the same bits definition as line-mode registers. (default 7Fh)

Appendix B Sample WinVCC CMD File for VBI Setup

```
////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////
// These commands can be used with the WinVCC4 EVM software to configure the Line Mode
// registers for a typical NTSC VBI setup.
// The WR_REG commands are direct writes to the I2C registers.
// Each command shown writes 1 byte to the I2C address
// specified in the command line.
BEGIN_DATASET

DATASET_NAME,"TVP5151 NTSC VDP/VBI SETUP"
INCLUDE, VDPRegsIdle.inc                  // Set VDP registers to their default state
INCLUDE, SlicerRAM_601.inc                // Load VDP configuration RAM

WR_REG,VID_DEC,0x01,0xD8,0x44             // Line10 (Field 1)-TTX NTSC
WR_REG,VID_DEC,0x01,0xD9,0x44             // Line10 (Field 2)-TTX NTSC
WR_REG,VID_DEC,0x01,0xE0,0x0B             // Line14 (Field 1)-VITC NTSC
WR_REG,VID_DEC,0x01,0xE1,0x0B             // Line14 (Field 2)-VITC NTSC
WR_REG,VID_DEC,0x01,0xEC,0x09             // Line20 (Field 1)-WSS/CGMS NTSC
WR_REG,VID_DEC,0x01,0xED,0x09             // Line20 (Field 2)-WSS/CGMS NTSC
WR_REG,VID_DEC,0x01,0xEE,0x07             // Line21 (Field 1)-CC NTSC
WR_REG,VID_DEC,0x01,0xEF,0x07             // Line21 (Field 2)-CC NTSC

WR_REG,VID_DEC,0x01,0xCD,0x01             // Enable FIFO access, disable ANC data
WR_REG,VID_DEC,0x01,0xCB,0x4E             // Set Pixel Alignment [7:0] to 4Eh
WR_REG,VID_DEC,0x01,0xCC,0x00             // Set Pixel Alignment [9:8] to 0

END_DATASET
////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////

// These commands can be used with the WinVCC4 EVM software to configure the Line Mode
// registers for a typical PAL VBI setup.  For PAL systems, the Line Mode register has
// a +3 line offset relative to the actual line number.  Each command shown writes
// 1 byte to the I2C address specified in the command line.
////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////
BEGIN_DATASET
DATASET_NAME,"TVP5151 PAL VDP/VBI SETUP"
INCLUDE, VDPRegsIdle.inc                  // Set VDP registers to their default FFh state
INCLUDE, SlicerRAM_601.inc                // Load VDP configuration RAM

WR_REG,VID_DEC,0x01,0xD8,0x41             // Line10 (Field 1)-TTX-B PAL(Line7)
WR_REG,VID_DEC,0x01,0xD9,0x41             // Line10 (Field 2)-TTX-B PAL (Line7
WR_REG,VID_DEC,0x01,0xEA,0x0C             // Line19 (Field 1)-VPS PAL (Line 16)
WR_REG,VID_DEC,0x01,0xEB,0x0C             // Line19 (Field 2)-VPS PAL (Line 16)
WR_REG,VID_DEC,0x01,0xF0,0x0A             // Line22 (Field 1)-VITC PAL(Line 19)
WR_REG,VID_DEC,0x01,0xF1,0x0A             // Line22 (Field 2)-VITC PAL(Line 19)
WR_REG,VID_DEC,0x01,0xF6,0x06             // Line25 (Field 1)-CC PAL(Line 22)
WR_REG,VID_DEC,0x01,0xF7,0x06             // Line25 (Field 2)-CC PAL(Line 22)
WR_REG,VID_DEC,0x01,0xF8,0x08             // Line26 (Field 1)-WSS/CGMS PAL(Line 23)
WR_REG,VID_DEC,0x01,0xF9,0x08             // Line26 (Field 2)-WSS/CGMS PAL(Line 23)

WR_REG,VID_DEC,0x01,0xCD,0x01             // Enable FIFO access, disable ANC data
WR_REG,VID_DEC,0x01,0xCB,0x4E             // Set Pixel Alignment [7:0] to 4Eh
WR_REG,VID_DEC,0x01,0xCC,0x00             // Set pixel Alignment [9:8] to 0
END_DATASET
////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////
```

Appendix C Example TVP5151 C Code

```
// TVP5151 WSS/CGMS Example

#define TVP5151 0xB8;                       // TVP5151 main I2C address
byte I2C_RegAddress,Status;
byte I2C_Data;
int CRAM_Address, count;

// recommended WSS/CGMS settings
byte WSS_ARRAY[]={0x38,0,0x3F,0,0,0x71,0x6E,0x43,0x63,0x7C,0x08,0,0,0,0x39,0};
byte WSSData[3];      // data array for WSS/CGMS

////////////////////////////////////////////////////////////////////////////
// initialize
////////////////////////////////////////////////////////////////////////////
// load WSS/CGMS C-RAM
I2C_RegAddress = 0xD0;                       // starting address of Line Mode registers
I2C_Data = 0xFF;
For (count = 0; count < 44; count ++)
{
  I2CWriteByte(TVP5151, I2C_RegAddress, I2C_Data);  //write FFh to Line Mode registers
  I2C_RegAddress ++;
}
I2CWriteByte(TVP5151, 0xCF, 0);                 // disable full field mode
CRAM_Address = 0x130;                            // address of NTSC WSS/CGMS C-RAM block

I2CWriteByte(TVP5151, 0xC4, 0x30);              // load C4h with C-RAM address[7:0]
I2CWriteByte(TVP5151, 0xC5, 0x01);              // load C5h with C-RAM address[8]

For (count = 0; count < 16; count++)
{
  I2CWriteByte(TVP5151, 0xC3, WSS_ARRAY[count]);  // write 16 bytes of WSS/CGMS C-RAM
}                                                  // data to register C3h.
I2CWriteByte(TVP5151, 0xCB, 0x4E);    // Set Pixel Alignment[7:0]to 0x4E
I2CWriteByte(TVP5151, 0xCC, 0x00);    // Set Pixel Alignment[9:8]to 0x00

// NTSC WSS/CGMS Line Mode setup for line 20 of both fields
I2CWriteByte(TVP5151, 0xEC, 0x09);    // line 20 field 1 (0xEC), mode bits = 0x09
I2CWriteByte(TVP5151, 0xED, 0x09);    // line 20 field 2 (0xED), mode bits = 0x09

// PAL WSS/CGMS Line Mode setup for line 23 (source input) of both fields.
// PAL line numbering has 3 line offset so the Line 26 line mode registers are used.

I2CWriteByte(TVP5151, 0xF8, 0x08);    // line 26 field 1 (0xF8), mode bits = 0x08
I2CWriteByte(TVP5151, 0xF9, 0x08);    // line 26 field 2 (0xF9), mode bits = 0x08
I2CWriteByte(TVP5151, 0xCD, 0x01);    // disable ANC data, enable FIFO access.

////////////////////////////////////////////////////////////////////////////////
// check status and get sliced data
////////////////////////////////////////////////////////////////////////////////

I2CReadBuffer(TVP5151,0xC6,&Status,1);  //read 1 byte(status)from register C6h

if ((Status & 0x20) ==1)
{
  I2CReadBuffer(TVP5151,0x94,&WSSData[0],3);  //if WSS/CGMS bit set,
                                               // read the 3 WSS/CGMS bytes
                                               // at WSS/CGMS data registers 94h-96h.
  I2CWriteByte(TVP5151,0xC6,0x20);            // clear WSS/CGMS available status bit
}
```

Appendix D VBI Raw Data I²C Registers

Luminance Processing Control #1 Register

Address	07h

7	6	5	4	3	2	1	0
Luma bypass mode	Pedestal not present	Disable raw header	Luma bypass during vertical blank	Luminance signal delay with respect to chrominance signal			

Luma bypass mode:

0 Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero (default).

1 Input video bypasses the whole luma processing. Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply with ITU-R BT.601 coding range. Only valid for 8-bit YUV output format (YUV output format = 100 or 111 at register 0Dh)

Pedestal not present:

0 7.5 IRE pedestal is present on the analog video input signal (default).

1 Pedestal is not present on the analog video input signal.

Disable raw header:

0 Insert 656 ancillary headers for raw data.

1 Disable 656 ancillary headers.

Luminance bypass enabled during vertical blanking:

0 Disabled (default)

1 Enabled

Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range -8 to +7 pixel clocks):

1111 -8 pixel clocks delay

1011 -4 pixel clocks delay

1000 -1 pixel clocks delay

0000 0 pixel clocks delay (default)

0011 3 pixel clocks delay

0111 7 pixel clocks delay

Vertical Blanking Start Register

Address	18h

7	6	5	4	3	2	1	0
Vertical blanking start							

Vertical blanking (VBLK) start:

0111 1111	127 lines after start of vertical blanking interval
0111 1111	127 lines after start of vertical blanking interval
0000 0000	Same time as start of vertical blanking interval (default)
1000 0001	1 line before start of vertical blanking interval
1111 1111	128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank. The setting in this register also determines the duration of the luma bypass function (see register 07h).

Vertical Blanking Stop Register

Address	19h

7	6	5	4	3	2	1	0
Vertical blanking stop							

Vertical blanking (VBLK) stop:

0111 1111	127 lines after stop of vertical blanking interval
0000 0001	1 line after stop of vertical blanking interval
0000 0000	Same time as stop of vertical blanking interval (default)
1000 0001	1 line before stop of vertical blanking interval
1111 1111	128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

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